AEC-NASA TECH BRIEF

Space Nuclear Systems Office
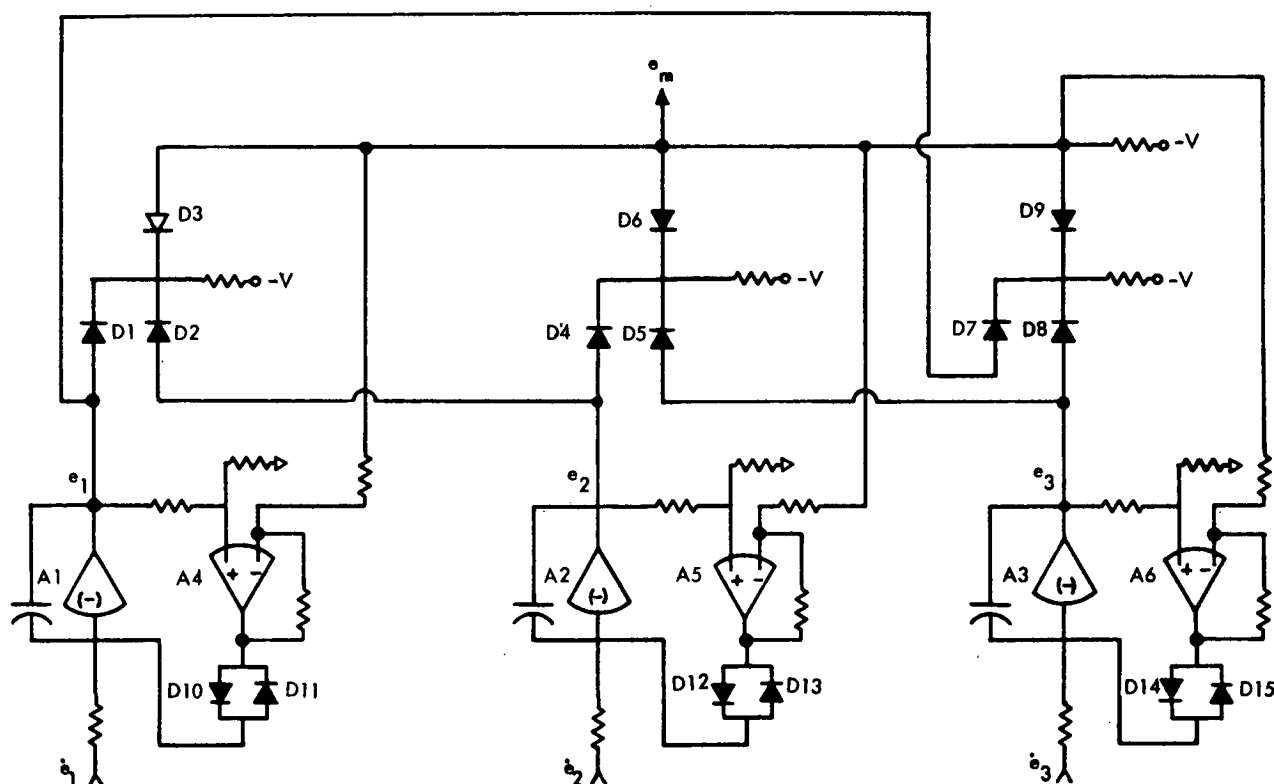
Active Parallel Redundancy for Electronic Integrator-Type Control Circuits

A new circuit extends the concept of redundant feedback control from type-0 to type-1 control systems. The inactive channels are slaves to the active

Circuit Providing Redundancy; Schematic

channel; if the latter fails, it is rejected and a slave channel is activated.

High reliability and the elimination of single-component catastrophic failure are important requirements in many closed-loop control systems. This redundancy problem is especially acute in systems incorporating electronic integrators. Earlier redundancy attempts included either deleting the integral requirement or using a single integrator with parallel rate stages. The existence of finite static and infinite ramp errors greatly reduced the applicability of the first method; and the use of a single integrator, in the second method, effectively retained a component whose failure would result in complete loss of closed-loop control.

In the circuit developed (see fig.), the integrator outputs are compared by a median-selecting logic

gate (diodes D1 through D9). The gate output, e_m = median (e_1, e_2, e_3), is fed back and compared with each individual channel where an error is developed. If the error exceeds the prescribed value

$$/(\theta_m - \theta_i)/ > \Delta$$

determined by error-amplifier gain and threshold diode drops, the inactive channels are made slaves to the selected median channel. Inherent drifts of the open-loop inactive integrators is eliminated and, if the selected channel fails, one of the inactive channels is activated. Transfer is automatic, with no substantial transient.

Consider, for example, the case where $e_1 > e_2 > e_3$. Diode gate (D_1, D_2) compares e_1 and selects the maximum; i.e., e_1. Similarly, diode gate (D_4, D_5) compares e_3 and e_2 and selects e_2, and diode gate (D_7, D_8) selects e_1, given that $e_1 > e_3$. Diode gate (D_3, D_6, D_9) compares the outputs of gates (D_1, D_2), (D_4, D_5), and (D_7, D_8), and selects the minimum output. For this case, $e < e_1$, and e_2 is selected as the desired output e_m, the median of e_1, e_2, e_3. The output signal e_m (i.e., e_2 in this case) is then fed back to differential amplifiers and compared with the individual integrator outputs. For integrator A_1, the difference between e_1 and e_m is generated by A_4. If this difference exceeded a pre-established threshold, determined by diodes (D_{10}, D_{11}) and the differen-

tial amplifier gain, integrator A_1 would be slaved, by the amount of the error, to the output e_m. Similarly, integrator A_3 would be slaved by the difference between e_m and e_3. Since, however, no error exists between e_2 and e_m for the example given, no slaving signal is generated by amplifier A_5, and A_2 operates as an integrator.

The parameters of the electronic components are not important in this application, because arbitrary values may be selected and the system will correct any mismatch.

Note:

Requests for further information may be directed to:
Technology Utilization Officer
AEC-NASA Space Nuclear Systems Office
U.S. Atomic Energy Commission
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