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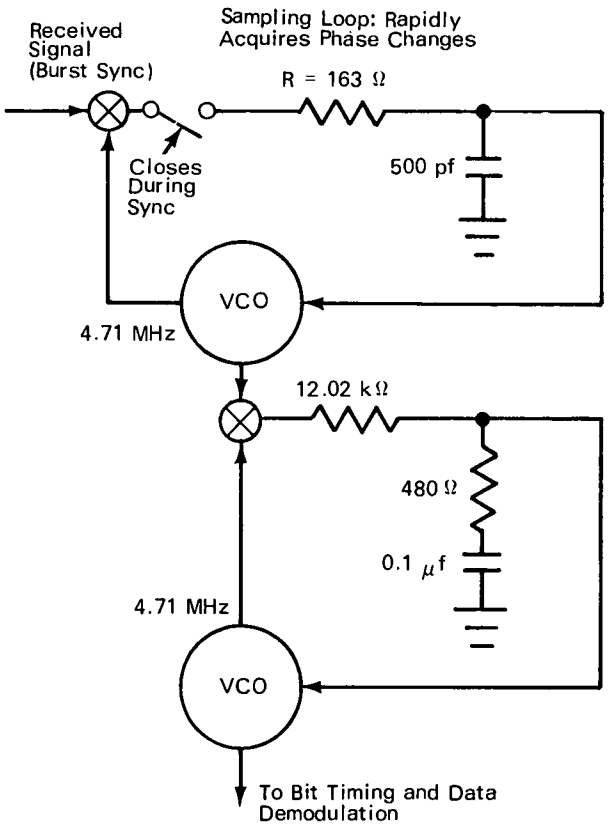
NASA TECH BRIEF

Goddard Space Flight Center

Double Phase-Lock Loop With Rapid Transient Response: A Concept

The problem:

In a burst synchronized, time-division-multiplexed communication system, the duration of the sync burst is on the order of one microsecond. A single narrowband second-order phase-lock loop cannot respond fast enough during the sync interval to remain in synchronism with the received signal.



Integration Loop: Gradually Acquires Phase Changes, Responds 600 Times More Slowly than Upper Loop

Double Loop Circuit: Extracts Bit-Timing from a Burst-Synchronized TDM Signal

The solution:

Two second-order phase-lock loops could be employed. The sampling loop would have a wide bandwidth and quick response to the phase steps of the burst sync interval. The integration loop, with a narrow bandwidth and correspondingly long response time, would integrate the phase estimate of the sampling loop, and the result would be a slower but less jittery response to the phase step changes.

How it's done:

During a sync interval, the switch in the sampling loop (see fig.) is closed, charging the capacitor through resistor R. The voltage change on the capacitor changes the frequency of the voltage-controlled oscillator (VCO) to keep it in phase with the received signal. After the sync interval, the switch is opened and the charge on the capacitor maintains the VCO frequency until the next sync interval, when the capacitor voltage and VCO frequency are changed again, keeping them locked to the received signal. The maximum timing error that develops in the sampling loop is only that error which results from frequency drift during the interval between sync bursts.

The integration loop is continually tracking to find and lock onto the sampling loop VCO frequency. Since the integration loop responds more slowly, it can never be in phase lock, but will always be within a certain phase difference. This phase difference can be made as large or as small as desired by varying the integration loop's

(continued overleaf)

response time. In most cases, the limit on the phase difference is determined by the maximum allowable timing error in the system. The double loop provides a timing reference within 1% of the received signal timing and has a signal-to-noise ratio which is 30 dB greater than a reference produced by a single loop.

Note:

No additional documentation is available. Specific questions, however, may be directed to:

Technology Utilization Officer
Code 207.1
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Greenbelt, Maryland
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Patent status:

No patent action is contemplated by NASA.

Source: J. F. Balcewicz of
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