

FORMULATION OF DESIGN RULES
FOR PCM TELEMETRY
FRAME SYNCHRONIZATION

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Formulation of Design Rules for PCM Telemetry Frame Synchronization		October 10, 1970
Computer Transmission Corporation 1508 South Cotner Avenue Los Angeles, California 90025		Contract No. NAS5-21196
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The objective of this report is to produce easily understandable and readily applicable design rules for choosing frame synchronization codes and associated parameters for PCM telemetry systems. The design rules are based upon an extensive experience survey to assure that all known operational problems associated with frame synchronization are solved. The resulting rules are based upon experience, the results of GSFC Study "Performance Evaluation and Frame Synchronization Codes for PCM Telemetry" by Maury and Styles, and the analyses of this report.		
Frame Synchronization Word (FSW) length, code and mechanization. Processing strategy		
Unclassified	Unclassified	

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PREFACE

The objective of this study and final report is to produce easily understandable and readily applicable design rules for choosing frame synchronization codes and associated parameters for space-to-ground PCM data systems. The study pertains to those systems which can be implemented with existing hardware. The scope of work is specifically worded to formulate results based upon both practical experience and the conclusions of theoretical studies. The tasks performed were:

- a. To survey the operating synchronization experience obtained with currently used PCM systems.
- b. To produce a simple analytical model of the frame synchronization problem.
- c. To investigate methods of frame sync pattern generation as to their ability to be implemented in the spacecraft. The survey investigated how these codes have been generated to date.
- d. To formulate design rules for obtaining frame synchronization patterns based upon the results of the GSFC study, "Performance Evaluation of Frame-Synchronization Codes for PCM Telemetry" by Maury and Styles (Reference 1). The formulated rules are written for the design specialist who desires to conform to the GSFC PCM Aerospace Data System Standards.
- e. To determine how the selected codes compare with shift-register generated codes.

The results of the theoretical studies clearly support the design practices and operating procedures which were analyzed during the survey of NASA experience. This final report provides design practices and operating procedures which do not deviate from past practices and procedures as understood during the experience survey. This document provides justification for existing practices and provides reasonable tolerances for the salient design and operating parameters. The conclusions are summarized as follows:

- a. The experience survey did not uncover any specific problems associated with the scope of this study.
- b. The most important single parameter, other than S/N, is the length of the frame synchronization word (FSW).
- c. Within the limits defined in this report, the processing strategy has little effect when the error rate is less than 10^{-2} , but the strategy rapidly becomes of importance as the error rate increases above 10^{-2} and approaches 10^{-1} .
- d. Historically, the code format recommended by the GSFC PCM Aerospace Data System Standard for each frame synch word length has not been used because of the difficulty in mechanization. A simple shift register mechanization is provided for recommended codes of lengths from 7 to 28 bits. A procedure is provided for evaluating the performance of any selected code.

I. INTRODUCTION

The design and operation of a satellite telemetry system includes many system and subsystem analyses resulting in subsystem and component specifications and recommended operating procedures. The salient parameters for both the design and operation of a telemetry system are summarized in Section II of this report. This document presents the results of a study of frame synchronization design rules and associated operating parameters. The study pertains to those telemetry systems which can be implemented with existing NASA hardware.

Assuming that bit synchronization is not a problem, the parameters which affect frame synchronization include the frame length, frame synchronization word length and code, the number of errors allowed during acquisition and the number of errors allowed during the maintenance (lock) mode. The frame synchronization is then evaluated by the acquisition time and the percentage of data lost. All of those parameters and performance criteria are interrelated. This report examines the tolerances of the frame synchronization parameters as a function of expected error rate.

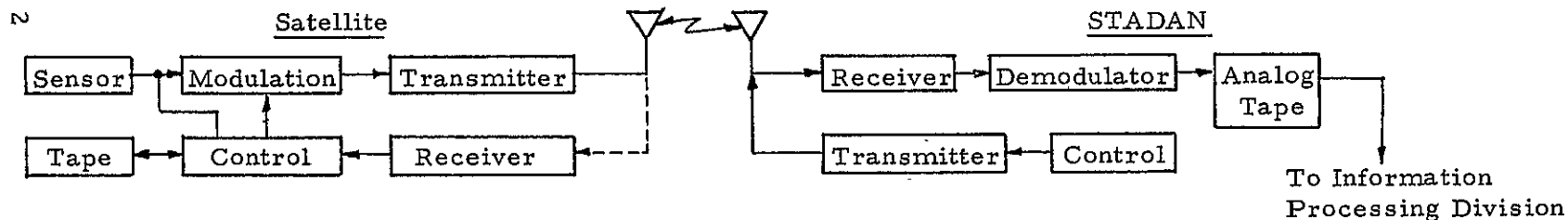
Section III assumes that an efficient system frame code has been determined and describes the effects of frame synchronization word length. Section IV analyzes the importance of the frame synchronization word code and means of mechanization. Section V is devoted to the selection of the operating parameters and investigates the effects of error rate. The conclusions and recommendations are presented in Section VI and VII, and acknowledgment of many contributions are included in Section VIII.

This study is primarily concerned with developing readily applicable design and operating rules which are based upon a survey of operating experience and supported by appropriate analyses. The rules are briefly summarized in Appendix C. Appendices E and F are reports prepared by Dr. Solomon W. Golomb while working as a consultant on this contract, and data from these reports are used throughout the text of this report.

II. SUMMARY OF SYSTEM CONSIDERATIONS

The description of the complete design of a telemetry system is beyond the scope of this report. The purpose of this section is to define those system parameters which are considered in this report and to categorize them as either design or operating parameters. The study analyzes frame synchronization parameters while assuming a well designed system in all other aspects.

Simplified block diagrams of the satellite and a Space Tracking and Data Acquisition Network (STADAN) station are shown in Figure 1. All parameters within the satellite which are initial design parameters affecting



Design Parameters

1. Frame Length
2. FSW Length
3. FSW Code
4. Tape Recorder Specs.
5. User's data organization
6. Threshold control

Tracking and Strategy

1. Tracking in azimuth, elevation and frequency
2. Recording of analog signals with precise ground time reference
3. Satellite Tape Recorder controls
4. Control signals and synchronization monitoring
5. Tape recorder performance
6. Preventive maintenance

Performance

1. Energy per bit to noise power density ratio is between 25 and 50 db at the ground receiver.
2. Continuous lock at elevation angles greater than 10° above horizon.
3. Errors:
 - a. systematic
 - b. atmospheric
 - c. multipath fades
 - d. tape recorders
 - e. threshold level control
4. Use Gaussian model when errors from bit-to-bit are independent and a Rayleigh model when errors are not independent.

FIGURE 1. GROUND TRACKING AND DATA COLLECTION ON TAPES

frame synchronization include frame length, frame synchronization word (FSW) length, and FSW code. The format and organization of the user's data is of extreme importance since quiescent data sensors can provide systematic data resulting in loss of frame synchronization. Each system design must analyze this possibility in great detail prior to establishing the FSW length and code.

STADAN's have the responsibility of acquiring satellites as early as possible and providing analog tapes of received telemetry data. The design goal is to provide a system for providing data for analog tapes which are satisfactory for frame and word synchronization at elevation angles not greater than 10 degrees above the local horizon. During the experience survey and examination of recorded data, it was learned that this requirement has not been a problem at higher elevation angles and with a normally operating system. However, the practical procedure is to acquire at the lowest possible elevation angles to provide the maximum data, and the low-angle acquisition is a problem, principally because of multipath fades.

At elevation angles above 10° , the energy per bit to noise power density ratio (E_b/N_0) is typically between 25 to 50 dB and the bit-to-bit errors are independent, permitting the use of a Gaussian model. Some of the sources of errors are those summarized in Figure 1. Systematic errors are immediately recognized during processing of tape as further explained in Section V. The most severe source of errors are the multipath fades occurring at low elevation angles during initial acquisition. With the resulting rapid signal fades of 30 to 40 dB, both bit and frame synchronization are often lost. Since these data occurring during fades are unreliable, the principal interest is the initial acquisition time when workable signal levels return. The multipath fades are also of major significance in attempting to evaluate the telemetry link performance since the evaluation of the loss of data can be severely biased by losing several frames of data during fades.

Errors are also introduced by atmospheric disturbances resulting in non-stationarity and thereby greatly complicating a classical systems analysis. During the survey of experience it was determined that the resulting poor data quality was acceptable for Control Center's use because of the short duration time and because of the low probability of correcting the situation. Once again, the salient point is to enhance the system to maintain synchronization and to possess the ability to rapidly re-acquire frame synchronization.

Another important function of the STADAN is to record accurate ground time. This provides the ability to predict the satellite position and arrivals at tracking stations and to correlate time on tapes to improve the data recovery per orbit.

The analog tapes collected by the STADAN's are sent to the Information Processing Division at the Goddard Space Flight Center (Figure 2). The

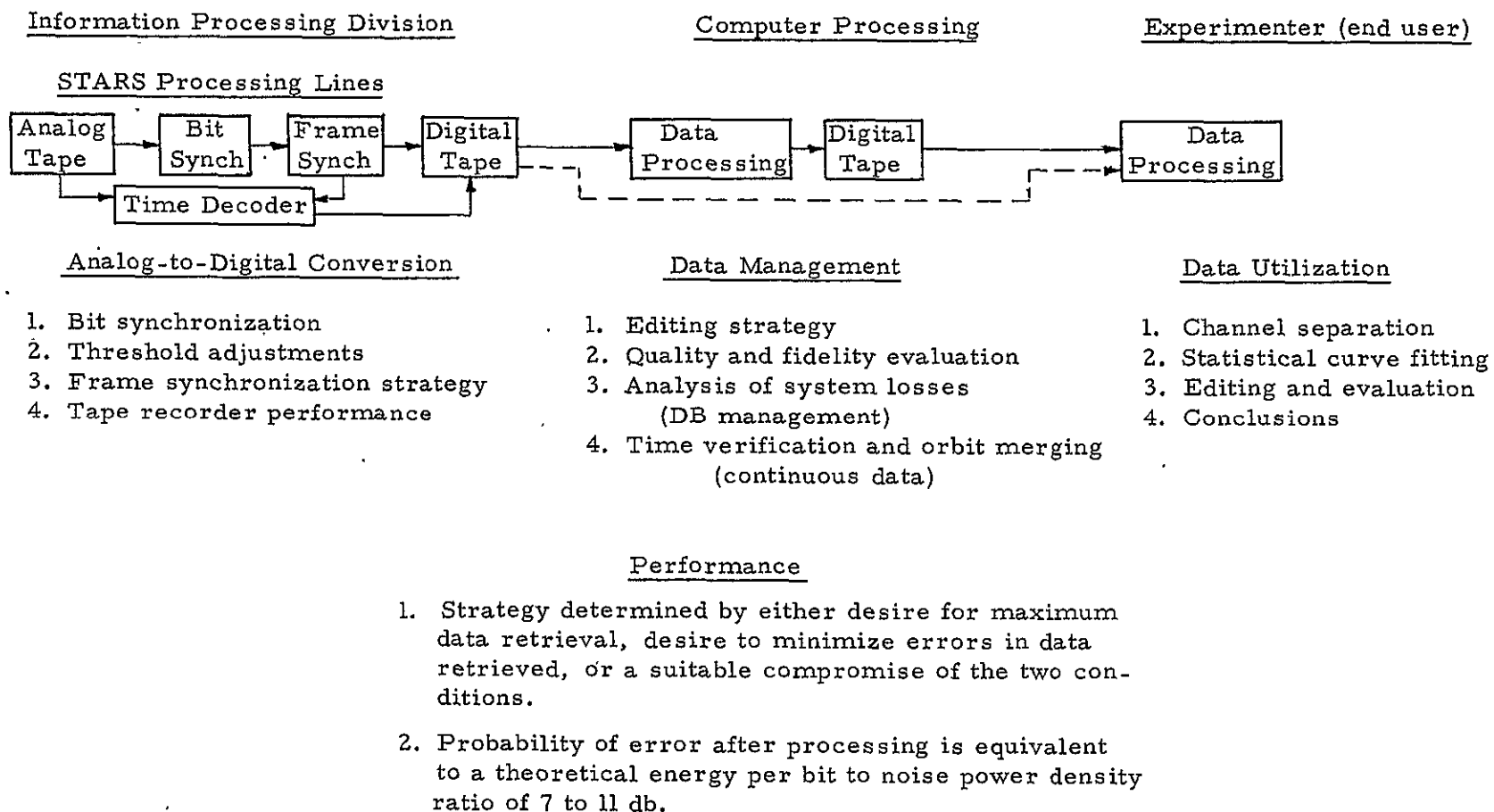


FIGURE 2. PROCESSING OF TAPES

first step is to convert the analog tapes to digital tape by processing through the Satellite Telemetry Automatic Reduction System (STARS) processing lines. Several operational parameters can be manipulated during this processing including the errors allowed during frame acquisition, the errors allowed during the maintenance (lock) mode, and the number of flywheels allowed during acquisition and maintenance. Since bit synchronization was not considered a problem for the scope of work of this report, this report will evaluate only the operating parameters listed above. Bit synchronization can become a problem, principally during signal fades at elevation angles and because of jitter produced by on-board tape recorders.

The output of the STARS line is a digital tape which can then be further processed and edited. Although all of the functions shown in Figure 2 can be performed during the "data management" processing, perhaps the most significant improvements have recently occurred as the result of an effort to evaluate the quality and fidelity of the data and to analyze system performance, through an analysis of system losses (Reference 5, 6, and 7). This phase of the effort could be improved with greater feedback from the end user of the telemetry data. At the present time, statistical parameter estimations must be developed based upon the performance of frame retrieval since this is the only available measure of errors. The resulting computed error rates appear to be commensurate with a theoretical E_b/N_0 of 7 to 11 dB, while the estimated E_b/N_0 at the STADAN receiver is 25 to 50 dB. The limited data available at the Information Processing Division is inadequate to predict the overall system performance. For example, perhaps greater overhead for parity or self-correcting codes would provide an overall system efficiency improvement by greatly reducing the processing time required by the end user. By flagging the detected errors with a parity scheme, good data can be passed on immediately while low quality data, via error correction, can be improved and later sent to the experimenter. Also, parity checks can be used as an S/N estimation to improve the evaluation of the system.

The design parameters which affect frame synchronization are the frame length and the frame synchronization word length and code. The processing parameters to be analyzed are the number of errors allowed during acquisition, the number of errors allowed during the maintenance (lock) mode, and the number of consecutive hits or misses (flywheels) required before a decision is made. Since the scope of work for this report is based upon the work of Maury and Styles (Reference 1), this report analyzes only those decisions determined by the first hit or miss.

III. FRAME SYNCHRONIZATION WORD LENGTH

The most important single parameter, other than signal-to-noise ratio, for frame synchronization is the length of the FSW. The most severe problem is false recognition or false detection of a FSW pattern. Section IV will investigate the impact of the FSW code.

Given a frame length of L bits, the problem is to determine a minimum acceptable FSW length of N bits.

This section is organized as follows:

- a. A technique is developed for evaluating the importance of error rate upon the FSW length.
- b. Performance criteria are developed for evaluating the desired FSW length, N , as a function of frame length, L .
- c. The selection of FSW length N is then examined as a function of error rate.

As explained in Appendix E, two types of frame synchronization errors can be experienced. Type 1 errors are those errors which occur when N consecutive bits duplicate the FSW code when there is some overlap of the N bits of the FSW, and Type 2 errors occur outside of the FSW overlap when N random bits within the frame satisfy the criteria for FSW detection. The probability of N consecutive bits looking exactly like the FSW code when there is no overlap (Type 2 errors) is 2^{-N} . In a frame of L bits (where L is large with respect to N), the expected number of times that N bits will duplicate the FSW code is effectively $L2^{-N}$. If the bit error rate due to noise produces independent errors occurring at random, then the probability of the Type 2 error is independent of error rate. However, Type 2 errors are extremely dangerous when systematic errors which duplicate a portion of the FSW code are allowed to occur. Although the probability of systematic errors producing synchronization errors can be reduced by increasing the FSW length, it is extremely important that the designer analyze the user's data to organize the data word coding to minimize the probability of systematic errors duplicating the FSW code.

The expected number of false frame synchronization detections occurring as the result of a Type 1 error is developed in Appendix E. The important point which determines the effect of error rate on the choice of the FSW length is the relative frequency of the Type 1 and Type 2 errors. Since the Type 2 errors are independent of error rate, the FSW length is independent of error rate as long as the frequency of the Type 2 errors predominates.

The analysis for Type 1 errors is developed assuming that an autocorrelation of the FSW is made when the N bits are displaced γ bits on itself. The FSW coincides in all N bit positions when $\gamma = 0$. Appendix E develops the fact that the danger of Type 1 errors is greatest for small displacements ($\gamma \geq 1$) unless special care has been taken in selecting the FSW code. It is shown that the probability of Type 2 errors is a function of the number of bits in disagreement when the FSW is shifted on itself by γ bits. Assuming an optimum code, the maximum number of disagreements is the integer equal to or just below $\frac{N-1}{2}$.

Appendix E develops a sufficient condition for Type 2 errors being more frequent than Type 1 errors when

$$D(\gamma) > \frac{N - \gamma}{\log_2 \left(\frac{1 - \gamma}{\gamma} \right)}, \quad (1)$$

where $D(\gamma)$ is the number of disagreements for a displacement of γ bits and an error rate of γ .

From above, $\frac{N}{2}$ is substituted for $D(\gamma)$. For acceptable FSW codes, as developed in Appendix E, the highest probability of a Type 1 error usually occurs for very small displacements of γ ($\gamma = 1$), and $N - \gamma$ is replaced by N . Also, for practical values of γ ,

$$\log_2 \left(\frac{1 - \gamma}{\gamma} \right) \approx -\log_2 \gamma. \quad (2)$$

The Type 1 errors are less frequent than Type 2 errors for error rates which satisfy the condition of the simplified equation.

$$\frac{N}{2} > \frac{N}{-\log_2 \gamma}, \quad \text{or} \quad 0.5 > \frac{1}{-\log_2 \gamma}, \quad (3)$$

which gives an error rate of 0.25.

The conclusion is that the FSW length is independent of practical values of error rates for FSW codes selected to satisfy the requirements developed in Appendix E. Conversely, there exist codes which can make a given FSW length sensitive to lower values of error rates.

The detailed calculations performed in the next part of this section verify that the FSW length is effectively independent of error rates less than 0.01, but the calculations are also performed for an error rate of 0.1 to show the effect of higher error rates. The recommended codes are used for these calculations.

To determine a minimum acceptable FSW length, performance criteria are selected. After computing the FSW length required for the selected criteria, the sensitivity of performance as a function of FSW length is examined.

The assumed performance criteria are that the average acquisition time, A , must be less than two frames and the percentage of data lost, λ , must be less than 0.01%. The acquisition time and lost data are excellent performance criteria since they include the acquisition time, number of false acquisitions, and the loss of frame synchronization.

Equations developed by Williard (Reference 2) and the documented results by Maury and Styles (Reference 1) were used to reduce the computational time in determining the FSW length, N , as a function of frame length, L . The results of the data interpolation from Reference 1 are shown in Figure 3. The processing strategy selected for obtaining these results are those commonly used in the STARS processing lines, which are as follows:

- a. Errors allowed during acquisition, ϵ , is between 5% and 10% of N .
- b. Errors allowed during the maintenance mode, ϵ' , are approximately 30% of N .
- c. A decision is made upon the first crossing of one of the above thresholds.

As developed in the first part of this section, the FSW length is independent of error rate as long as the Type 2 error dominates. As the error rate is increased, a value is reached at which the Type 2 error ceases to dominate, and the FSW length required is dependent upon error rate. The data computed by Maury and Styles (Reference 1) verified that the FSW length was independent of error rates less than 0.01, but the results show the effect upon the FSW length for error rates of 0.1 (Figure 3). The error rate which begins to affect the FSW length is a function of the FSW code (refer to example in Section IV).

As an example, the results in Figure 3 show that an FSW length of 16 bits is adequate for a frame length of 1000 bits for all error rates less than 0.01, but the FSW length must be increased to 21 bits to maintain the same selected performance criteria with an error rate of 0.1.

Figure 4 maintained a frame length of 1000 bits and shows the sensitivity of acquisition time (in frames) and percentage of data lost as a function of error rate for frame lengths of 12, 16, and 24 bits. The conclusions from this curve are as follows:

- a. For each frame length, there exists a critical FSW length which must be equaled or exceeded to achieve specific performance criteria.
- b. The most critical performance parameter in selecting the FSW length is the acquisition time.
- c. Once the selected performance criteria are met by selecting an appropriate minimum frame length, the error rate has no noticeable effect until the error rate exceeds 10^{-2} .

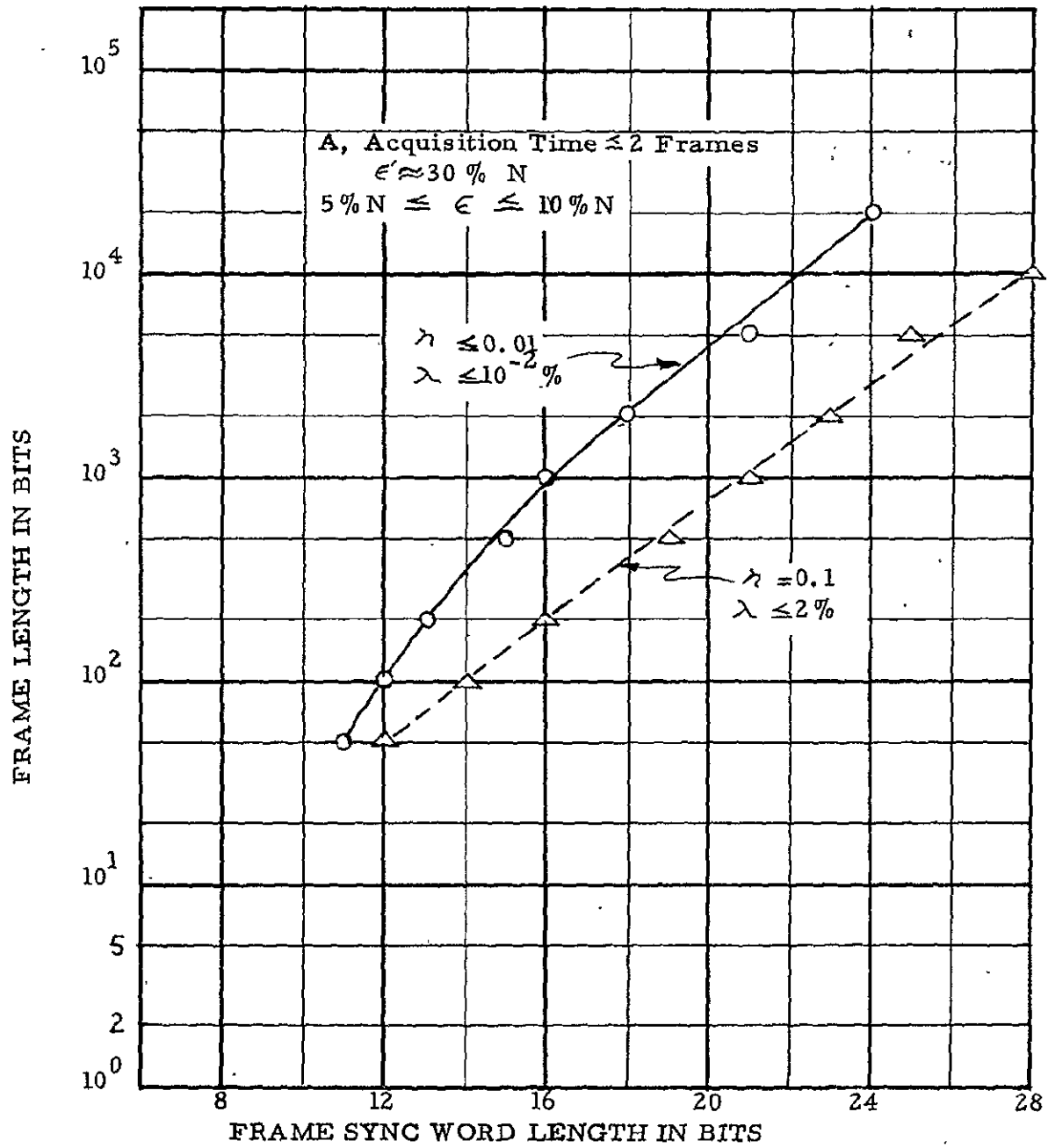


FIGURE 3

FRAME SYNC WORD LENGTH AS A FUNCTION OF FRAME LENGTH

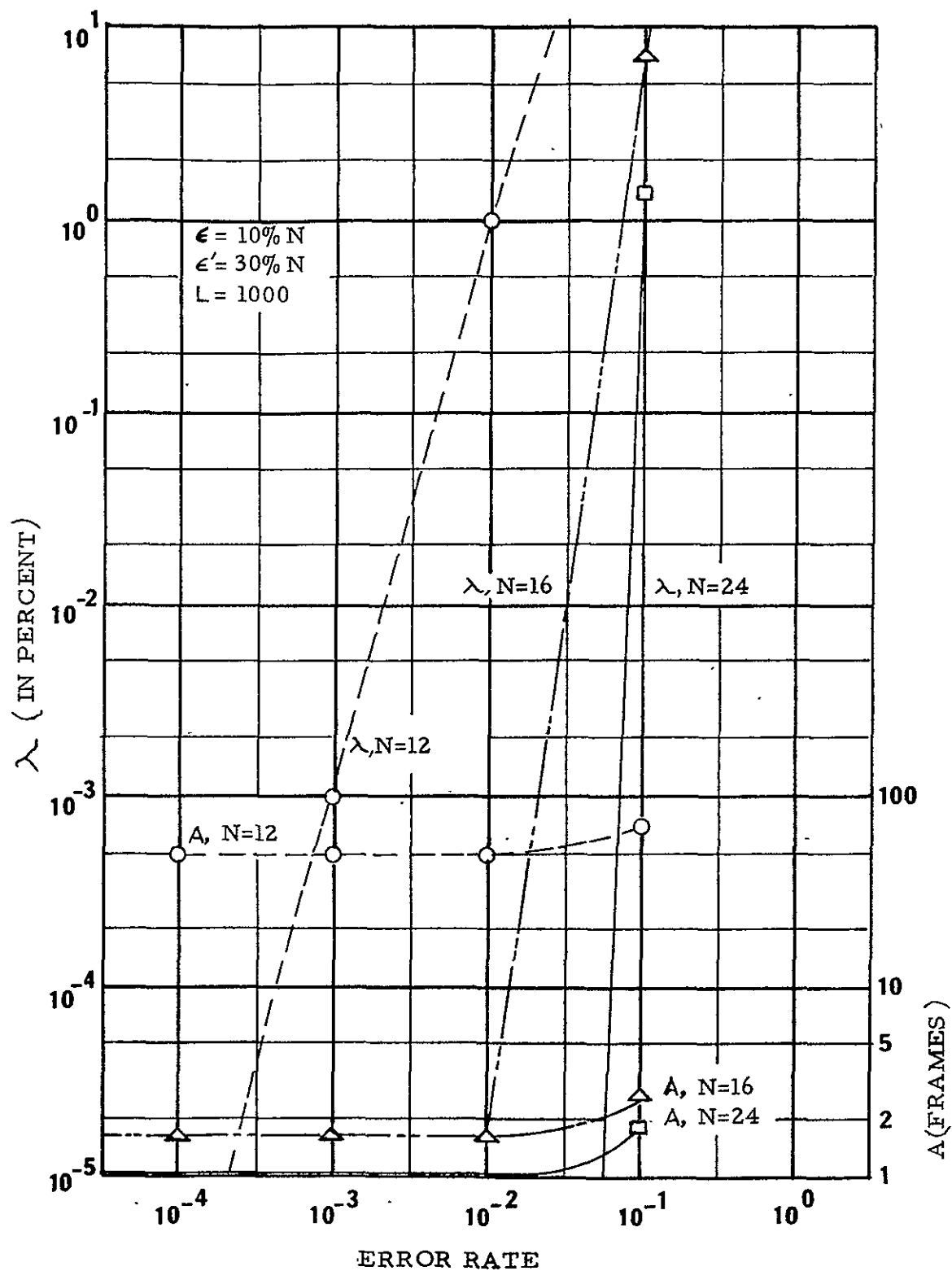


FIGURE 4

PERCENT DATA LOST (λ) AND ACQUISITION TIME (A);
 AS FUNCTION OF ERROR RATE FOR VARIOUS FRAME SYNC WORD
 LENGTHS (N)

IV. FRAME SYNCHRONIZATION WORD CODE SELECTION

Considerable effort has been expended in the past in computing the code for each FSW length, N , which possesses the lowest total probability of false sync recognition over the entire overlap portion of the code, assuming random data in all bit positions outside of the N bits of the FSW, after all 2^N possibilities were examined. These selected codes were then made a part of the existing GSFC PCM Telemetry Standard (Reference 4) and referred to as the "recommended code". It is not obvious that any of the recommended codes can be easily generated by a shift register. During the experience survey, it was learned that designers seldom used the recommended codes in favor of utilizing a close approximation which could be easily implemented with a shift register to save power and hardware within the satellite. The purpose of this section is to develop a procedure for rapidly evaluating any selected code as compared to the recommended code and to develop a shift register mechanization of the FSW recommended codes of lengths from 7 through 28 bits.

Dr. Solomon Golomb, while working as a consultant on this contract, wrote two reports. The first report provides a unique analytical means of evaluating the expected performance of any selected FSW code (Appendix E). However, the significant conclusion of this report is the analytical proof of the apparent insensitivity of the selection of the FSW code as long as the code is randomly chosen (refer to Appendix E). The conclusion is that the length of the FSW is far more critical than the code selection, which supports the results of experimental investigations conducted over the last several years. Another important conclusion is that the most practical danger is that data patterns or overlap of data patterns may systematically resemble the chosen FSW code. Certainly this is a danger which must be carefully analyzed during the initial design phase. The greatest protection is always to provide the longest practical FSW length.

Appendix D develops $D(\gamma)$ as the measure of performance of a FSW code. $D(\gamma)$ is the number of bits which disagrees when the FSW is shifted on itself by γ bits. The conclusion that the code selection is of little importance was based upon the fact that for typical S/N found in practice, the probability of Type 2 errors occurring is higher than the probability of Type 1 errors occurring, and Type 2 errors are independent of error rate. The sufficient condition that the frequency of Type 2 errors exceeds that of Type 1 errors is;

$$D(\gamma) > \frac{N - \gamma}{\log_2 \left(\frac{1 - \gamma}{\gamma} \right)} \quad \text{for } 1 \leq \gamma \leq N - 1. \quad (4)$$

The conclusion in Appendix E that the FSW code is of little importance was derived by using an error rate of 10^{-3} , which gives,

$$D(\gamma) > \frac{N - \gamma}{10}, \quad (5)$$

which is indeed satisfied for nearly any random code.

Section III developed two FSW lengths, one sufficient for error rates less than 10^{-2} and a second sufficient for error rates less than 10^{-1} . Section III assumed that the recommended FSW codes were used, which provided the optimum behavior of $D(\gamma)$ (approaching a uniform monotonic decrease as γ is increased).

The conclusion to be drawn in this section is that a designer must take precaution in the selection of the FSW code if error rates between 10^{-2} and 10^{-1} are expected. To be sure that the performance is not degraded when using a selected FSW code at these higher error rates, the entire autocorrelation function $C(\gamma)$ and disagreements function $D(\gamma)$ should be investigated

$$D(\gamma) = \frac{(N - \gamma) - C(\gamma)}{2}. \quad (6)$$

The converse of this is to use the recommended codes (Reference 4) for all designs. The only disadvantage with this approach is the apparent difficulty in using a shift register mechanization of the code. For this reason, a minimal shift register mechanization is presented (Appendix F) for FSW code lengths of 7 through 28 bits. To assure the validity of the design, the truth tables, Karnaugh charts, and all state diagrams are included.

The conclusion is that little, if any, is gained by not using a "recommended code" with a shift register mechanization (the most complicated logic can be implemented with two standard T^2L integrated circuit packages). The greatest exception in the number of stages required is for the case of $N=27$. The minimum number of stages required to mechanize a code is determined by the number of bits which are repeated in a sequence within the code. For $N=27$, the recommended code is 111110101101001100110000000. The brackets show two individual sequences of seven bits which are identical. Therefore, a minimum of eight stages are required to mechanize the recommended code.

Since 5 stages provide 32 states, a 27-bit code can be mechanized with 5 stages. This example is included in Appendix E. The procedure of this example should be followed for all code choices which deviate from the recommended (standard) codes (Reference 4).

For the selected 27-bit code mechanized with 5 stages, the greatest chance for error (minimum disagreement $D(\gamma)$) occurs at $\gamma = 10$, where $D(10)$ is 5 for the assumed code requiring 5 stages, and $D(10)$ is 8 for the

recommended (standard) code requiring 8 stages for mechanization. Using the equation

$$D(\gamma) > \frac{N - \gamma}{\log_2 \left(\frac{1 - \gamma}{\gamma} \right)}, \quad (7)$$

$N - \gamma$ is 17 ($\gamma = 10$). Therefore, the denominator need only exceed 3.4 for 5 stages and 2.1 for 8 stages. Using these values, the error rate becomes a salient factor at 0.09 for the 5-bit register and 0.18 for the 8-bit register. Theoretically, the recommended (standard) code will provide improved performance whenever the error rate exceeds 0.09.

The above example develops the conclusion that for $N=27$, a very slight cost savings in mechanization is obtained with practically no change in performance when deviating from the "recommended code". It is obvious that this is true primarily because of the long FSW length.

The mechanization of the recommended code (8 stages) requires 6 standard integrated circuit packages, and the 5-stage code requires 4 1/2 standard integrated circuit packages. For standardization, it is recommended that the shift register mechanizations of the recommended or standard codes be implemented. For $N=27$, a simpler mechanization is developed if the reduction in hardware resulting in going from 8 to 5 stages is considered important.

V. SELECTION OF OPERATING PARAMETERS

This section examines the effect of varying the parameters (strategy) during the processing of telemetry data. This section assumes that the FSW code and length are correctly selected for the desired frame length. The parameters which can be varied during processing of telemetry data are the number of errors allowed during acquisition, the number of errors allowed during the maintenance (lock) mode, and the number of hits or misses (flywheels) required for a decision. This report is based upon the work of Maury and Styles (Reference 1) and assumes all decisions are made upon the first hit or miss.

The performance criteria used in this section are the average acquisition time in frames and the percentage of data lost. The results of this section verify that the processing strategy described during the experience survey is optimum.

The required FSW length as a function of frame length was developed in Section III, assuming a certain processing strategy. The first part of this section assumes an example to show the effects of FSW length when the processing strategy is varied.

Using the computed results of Maury and Styles (Reference 1), an example is systematically pursued to show the effects of varying the allowed number of errors. For all practical purposes, the acquisition time is independent of the number of errors allowed during the maintenance mode. Proof is presented to show that the number of errors allowed during the acquisition must be less than 10% N to maintain the average acquisition time less than 2 frames. Having established limits for the allowed number of errors during acquisition, the percentage of data lost is evaluated as a function of the number of errors allowed during the maintenance mode. Curves are included to show the sensitivity of acquisition time and percentage of data lost as a function of the allowed errors.

During the experience survey it was learned that when the E_b/N_0 exceeds 3 dB, varying the system parameters has no practical effect upon the system performance. The strategy usually employed varies as a function of signal level at which acquisition is desired. When the signal level exceeds 0 dB, the strategy is typically as follows:

- a. Set the allowed number of errors during acquisition, ϵ , to 7 to 10% of the FSW length.
- b. On the first hit, switch to maintenance (lock) mode.
- c. In the maintenance mode, switch the allowed number of errors to 30 to 40% of the FSW length (random data will cause 40 to 50% errors).

When the signal is below 0 dB E_b/N_0 , bit synchronization becomes a severe problem. The optimum strategy is one which provides the highest probability of maintaining synchronization during short period fades. The strategy used is as follows:

- a. Maintain the allowed number of errors during acquisition at approximately 10% of the FSW length.
- b. After the second consecutive hit, switch from the acquisition mode to the maintenance mode.
- c. Maintain the number of allowed errors in the maintenance mode at approximately 40% of the FSW length.
- d. After the second consecutive miss, return to the acquisition mode.

As previously mentioned, systematic errors are immediately detected. When they are recognized, the strategy is changed to reduce the allowed number of errors during acquisition and/or to require two consecutive hits.

The first problem to be considered is that of the relationship between the allowed number of errors and the FSW length developed in Section III.

The average acquisition time, A , is the parameter most sensitive to variations in both the allowed number of errors during acquisition and the FSW length.

Figure 5 shows acquisition time as a function of FSW length for allowed acquisition errors, ϵ , of 1 and 2 for frame lengths of 5,000, 2,000 and 1,000 bits. Each frame length will be examined individually while maintaining the performance criterion assumed in Section II (the average acquisition time is less than 2 frames).

For a frame length of 1,000 bits, an ϵ of one error ($\approx 6\% N$) requires a FSW length of 16 bits, and an ϵ of two errors ($> 10\% N$) requires an FSW length of 20 bits.

For a frame length of 2,000 bits, an ϵ of one error ($\approx 6\% N$) requires a FSW length of 17 bits, and an ϵ of two errors ($> 10\% N$) requires an FSW length of 20 bits.

For a frame length of 5,000 bits, an ϵ of one error ($\approx 6\% N$) requires a FSW length of 18 bits, and an ϵ of two errors ($> 9\% N$) requires an FSW length of 22 bits.

Figure 5 verifies the choice of FSW length as a function of frame length made in Section III. However, the curves also indicate the critical relationship between the allowed number of errors during acquisition and the FSW length. To better illustrate this point, FSW lengths were chosen from Figure 3 (Section 2) for frame lengths of 100, 500, 1000, 2000, 5000 and 10,000 bits and the acquisition time, A , in frames is shown as a function of the number of allowed errors during acquisition. (Figure 6)

Therefore, the present strategy for allowed errors during acquisition is verified, which validates the FSW length analysis of Section III.

The last parameter to be investigated is the number of errors allowed during the maintenance mode, ϵ' . It has been shown that given the correct FSW length and number of errors allowed during acquisition, the acquisition time is practically independent of ϵ' . Figure 7 shows the data lost in percent as a function of error rate for various values of ϵ' . The present strategy is to set ϵ' at 30 to 40% of the FSW length. Figure 7 indicates that ϵ' of 3 errors ($\approx 20\% N$) is adequate to maintain the data lost below $10^{-2}\%$ for error rates less than 10^{-2} , but indicates that ϵ' must be 5 ($\approx 30\% N$) at an error rate of 0.1 to keep the lost data at 1%. Figure 7 indicates the steepness of the curve of data lost as a function of error rate between error rates of 0.1 and 0.01. The percentage of data lost is well below $10^{-2}\%$ with 5 errors (30% N) until the error rate is very close to 0.1.

In conclusion, Figure 7 is characteristic of the importance of ϵ' when the error rate exceeds 10^{-2} and verifies the present strategy for setting ϵ' for effective performance at higher error rates.

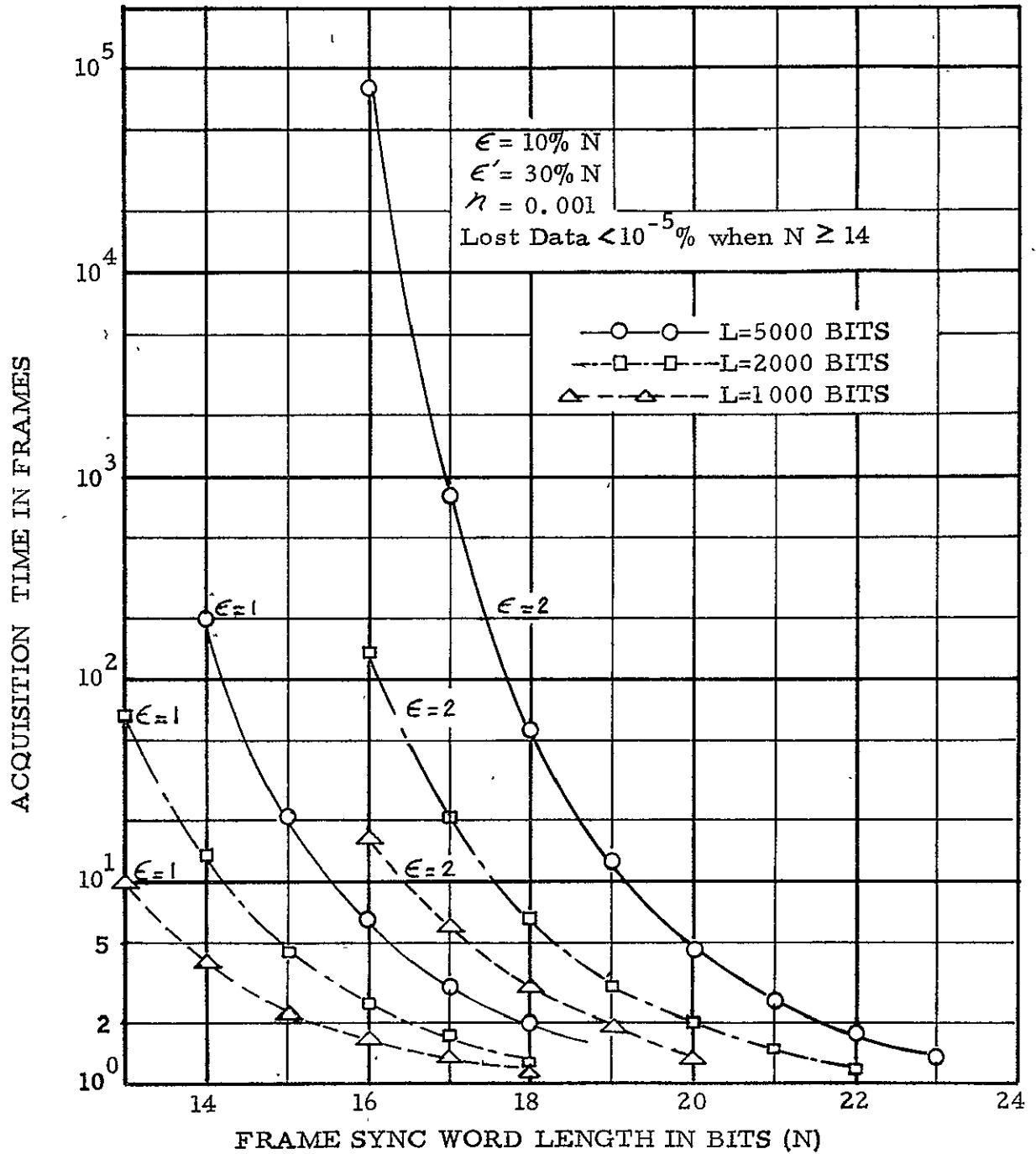


FIGURE 5
 ACQUISITION TIME AS A FUNCTION OF FRAME SYNC WORD
 LENGTHS FOR VARIOUS FRAME LENGTHS (L)

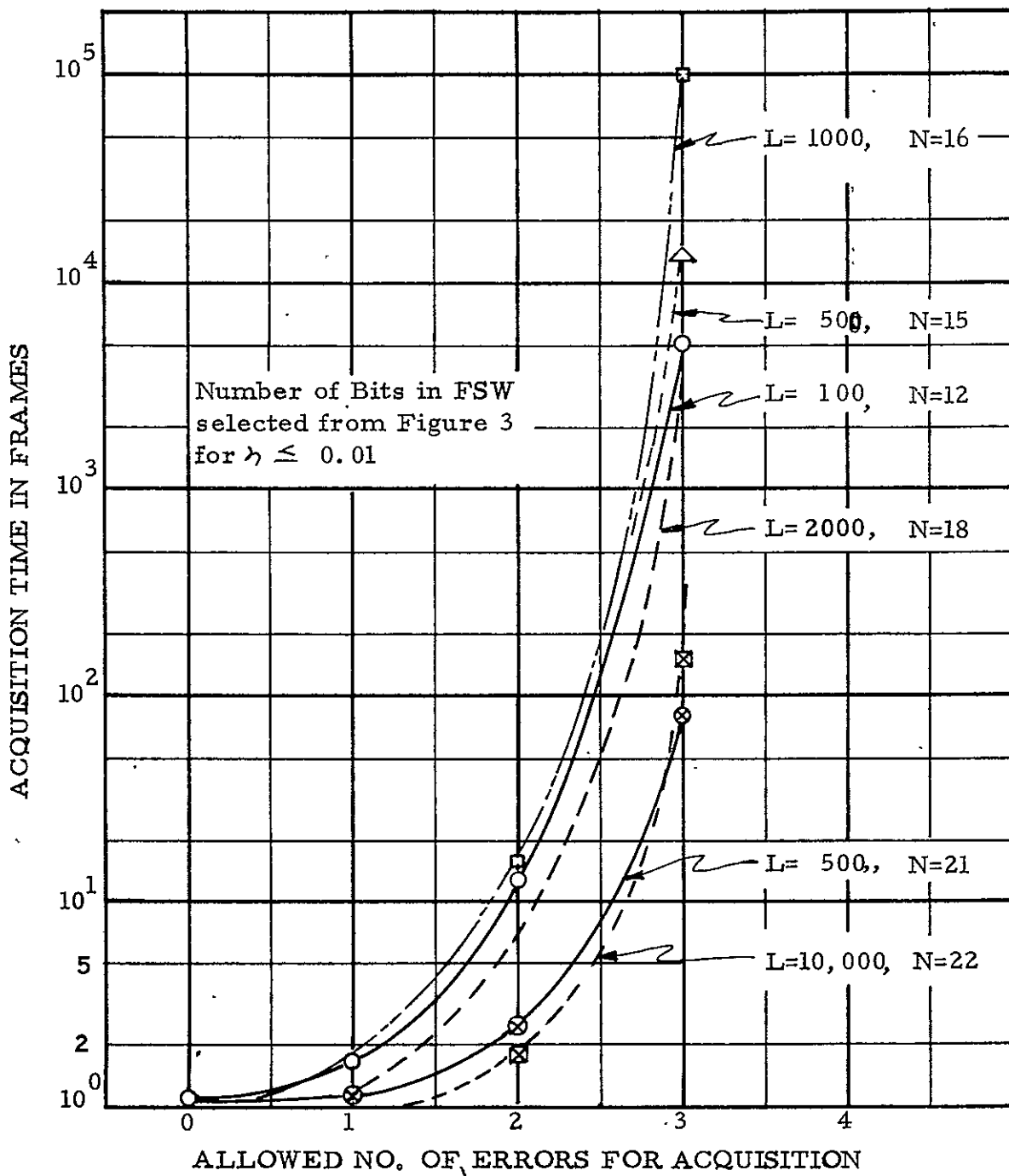


FIGURE 6

ACQUISITION TIME AS FUNCTION OF ALLOWED NO. ERRORS,

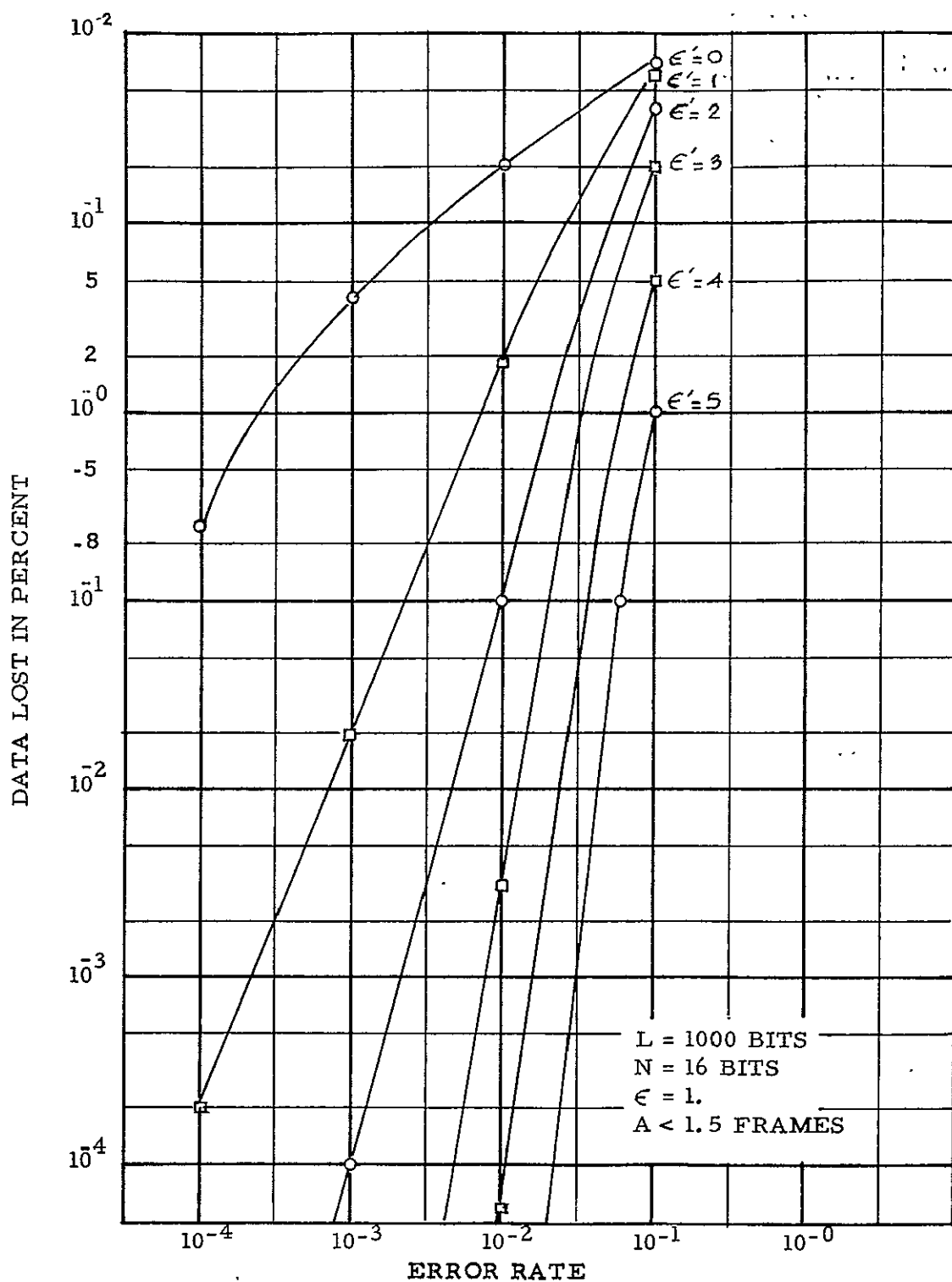


FIGURE 7

PERCENT DATA LOST AS A FUNCTION OF ERROR RATE FOR VARIOUS VALUES OF ALLOWED ERRORS (ϵ') DURING LOCK MODE

VI. CONCLUSIONS

The conclusions are divided into those conclusions reached as the result of the experience survey and those conclusions reached as the result of the analytical study.

Conclusions as the result of the experience survey are as follows:

- a. There are no known frame synchronization problems which could not be solved in any of the past NASA programs.
- b. The strategy used during processing of the telemetry data is verified as satisfactory.
- c. Past FSW codes and lengths were selected as the result of experience and for ease of mechanization.
- d. Considerable effort is being expended in developing a means of evaluating data quality or fidelity based upon the errors occurring during the FSW.
- e. The data quality and percentage of data lost are biased by errors occurring at low elevation angles during the presence of multipath fades. However, the system specifications require that acquisition be completed at an elevation angle not greater than 10° , and there is no reported problem in meeting this requirement.
- f. Although not part of the present scope of work, it should be noted that the dB management analysis indicates a possible discrepancy between the theoretical performance and the actual performance measured in error rate (compared to E_b/N_0 at input to receiver).
- g. It appears that the overall system performance could be more effectively evaluated and improved with more performance feedback from the experimenter (end user).

Conclusions as the result of this study:

- a. The salient points of concern expressed during the experience survey were beyond the scope of work of this study (refer to Recommendations).
- b. The results of the analyses of this report substantiate the present design and operating practices.
- c. The length of the FSW is the most important design parameter pertaining to frame synchronization and a minimum acceptable FSW length is provided herein as a function of the frame length.
- d. As long as the FSW code is random and of adequate length, the chosen code has little practical value with error rates less than

0.01. However, a small performance improvement can be expected with optimum codes as the error rate increases above 0.01, and the degree of improvement depends upon the characteristics of the chosen code.

- e. A technique is provided for analytically evaluating the impact of any chosen FSW code.
- f. A shift register mechanization of recommended FSW codes (reference 4) for FSW lengths of 7 through 28 bits is provided.
- g. For the purpose of standardization, it is recommended that the previously recommended codes be used in the future. The FSW length where the greatest additional complexity is involved is when $N=27$, and an alternate code is provided and analyzed for this length. (At most, the designer will save two integrated circuit packages by not using the recommended code).
- h. The processing strategy only becomes critical when the error rate exceeds 10^{-2} . The performance is evaluated in terms of acquisition time and percentage of lost data. Since the study is based upon the work by Maury and Styles, this report only analyzes those decisions made on a single hit or miss. The allowed number of errors during the maintenance (lock) mode has no practical effect upon the acquisition time, and the number of allowed errors during acquisition must be kept below 10% of the FSW length to provide an acquisition time of less than 2 frames. The remaining variable for controlling the percentage of lost data is the number of errors allowed during the maintenance (lock) mode. The number of errors allowed for a given loss of data is a function of error rate. A minimum threshold of 20% of N is adequate unless it is desired to operate with error rates exceeding 10^{-2} , and the curves for operating between 10^{-2} , and 10^{-1} are very critical. The past procedure of using 30 to 40% of N for the allowed number of errors during the maintenance mode is quite adequate for error rates of the order of 0.05 with the lost data rapidly approaching 1 percent as the error rate rises above 0.05 and approaches 0.1.
- i. Considerable doubt has existed as to the performance of the bit synchronizer as the error rate approaches 0.1. Planned future systems must be capable of operating with error rates of 0.1 and lower to take advantage of new coding techniques.

VII. RECOMMENDATIONS

- a. The present operating and design practices are adequate, but the results of this study should be used to evaluate the inter-relationship of the parameters,

- b. The FSW length should be designed to be as long as feasible.
- c. The telemetry system designer must carefully analyze the final word format and experimenter's data characteristics to prevent systematic errors which could resemble the FSW code.
- d. Any chosen FSW code which deviates from the recommended code should be evaluated using the procedure in this report.
- e. Although not applicable to this report, serious consideration should be given to the system power management to verify the difference between a theoretical E_b/N_0 of 25 dB and the resulting system error rates equivalent to E_b/N_0 7 to 11 dB.
- f. The procedures initiated to evaluate the quality and fidelity of telemetry data should be continued (references 5, 6, and 7). However, the efficiency and ultimate goals could be enhanced if a procedure were devised to provide a systematic feedback from the end user (experimenter) to the code designer and to personnel in the Information Processing Division.
- g. Additional system analyses including the end user's requirements could result in a more cost effective system design by evaluating the tradeoff between frame overhead devoted to error detection correction and the computing time required by the end user.
- h. The theoretical performance analysis should be extended to analyze multiple hits and misses before decisions are made. In particular, a sacrifice in acquisition time will permit two consecutive hits to be required before switching to the maintenance mode, and this would greatly reduce the probability of false acquisition for the same number of allowed errors and shorter FSW lengths.

VIII. ACKNOWLEDGMENTS

The authors acknowledge the contributions of Dr. Solomon Golomb, consultant for this contract, and many people participating as the result of personal interviews and as the result of their published material, which were used as references. Dr. Robert Rochelle, Code 710, provided guidance and arrangements for interviews with many people. People who were interviewed during the experience survey included the following:

John Adolphson, Ed Scobey, John Yagelowich, Warner Miller, Tom Karras, Richard Lee, Carlo Broglio, Bernard Peavey, Bernard Narrow, and Henry Franks of NASA; and Tom Saliga of Paradyne Corporation.

Much of the mathematical analyses and computations used in this report were developed by Messrs. Maury and Styles (References 1 and 3).

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APPENDIX A

GLOSSARY OF TERMS

GLOSSARY OF TERMS

The terminology used in Reference 1 is used whenever possible.

N (n)	Frame-sync code length in bits (see Figure 1)
η (E)	Bit-error rate due to noise
ϵ (e)	Number of errors allowed by the frame-sync code recognizer in the search mode
ϵ' (e')	Number of errors allowed by the frame-sync code recognizer in the lock mode
β	Random data region length in bits
E_b/N_0	Energy per bit to noise power density ratio, usually expressed in dB
ϕ	Overlap region length in bits $\phi = N - 1$
L	Frame length in bits (useful in considering actual frame length for which the frame-sync code performance is plotted) $L = 2\phi + \beta + 1$ also $L = \beta + 2N - 1$
F_f	Probability of at least one false frame-sync code recognition over the entire ϕ overlap region of a single frame
f_{β} (P_i)	Probability of false recognition in a single code-length group of random data bits

$$f_{\beta} = \frac{1}{2^N} \sum_{r=0}^{\epsilon} \binom{N}{r}$$

F_{β} Probability of false recognition in any of the β code-length groups of random data bits in a single frame

$$F_{\beta} = 1 - (1 - f_{\beta})^{\beta}$$

$F_T (P_t)$ Probability of at least one false recognition in a single frame

$$F_T = 1 - (1 - 2 F_{\beta}) (1 - f_{\beta})^{\beta}$$

$P_T (P_c)$ Probability of a true recognition (in the sync position) in a single frame

$$P_T = \sum_{r=0}^{\epsilon} \binom{N}{r} \gamma^r (1 - \gamma)^{N-r}$$

$S (M)$ Average number of frames to a recognition, true or false

$$S = \frac{1}{F_T + P_T (1 - F_T)}$$

$P_s (T)$ Probability that the recognition after S frames will be a true recognition

$$P_s = \frac{P_T (1 - F_T)}{F_T + P_T (1 - F_T)}$$

$R_f (J)$ Average number of false patterns which must be seen by the recognizer in the lock mode before it can decide that it has false sync

$$R_f = \frac{1}{1 - f'_{\beta}}$$

where

$$f'_{\beta} = \frac{1}{2^N} \sum_{r=0}^{\epsilon'} \binom{N}{r}$$

$R_T (K)$ Average number of true codes which will be seen by the recognizer in the lock mode before noise errors cause rejection of true sync

$$R_T = \frac{1}{1 - P'_T}$$

where

$$P'_T = \sum_{r=0}^{\epsilon'} \binom{N}{r} \gamma^r (1 - \gamma)^{N-r}$$

A (L)	Average number of frames before true sync is acquired
	$A = \frac{S + R_F (1 - P_s)}{P_s}$
λ (D _L)	Percent data lost because of loss of frame sync
	$\lambda = \frac{100 A}{A + R_T}$
FSW	Frame synchronization word
STADAN	Space tracking and data acquisition network
STARS	Satellite telemetry automatic reduction system
Type 1 Errors	Frame synchronization errors occurring when the FSW is overlapped during autocorrelation
Type 2 Errors	Frame synchronization errors occurring entirely in data bits (no overlap of the FSW).
τ	Displacement of the FSW on itself measured in bits from the desired autocorrelation position
C (τ)	Un-normalized autocorrelation function $[C (\tau) \text{ is maximum at } C (0)]$.
D (τ)	Disagreements in the autocorrelation for a displacement τ of the FSW
A (τ)	Agreements in the autocorrelation for a displacement τ of the FSW
$C (\tau) = A (\tau) - D (\tau)$	
$A (\tau) + D (\tau) = (N - \tau)$	

APPENDIX B

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APPENDIX C

DESIGN RULES FOR CHOOSING

PARAMETERS FOR FRAME

SYNCHRONIZATION

DESIGN RULES FOR OBTAINING FRAME SYNCHRONIZATION

This document summarizes the design rules for assuring acceptable frame synchronization performance for a pulse code modulation telemetry system. The rules pertain only to those parameters directly affecting frame synchronization of PCM systems which utilize existing NASA hardware employing block sync code formats.

The design rules assume the use of the acceptable processing strategies employed by the Information Processing Division.

Frame Length - Frame lengths not exceeding 4096 bits are recommended with a maximum permissible frame length of 8192 bits.

Frame Synchronization Word Length - The frame synchronization word (FSW) length should be made as long as practical. The minimum acceptable and desired lengths are shown in Table I.

FSW Code - The codes recommended in Table II shall be used. The shift register mechanization is shown in Appendix F for each FSW code of N from 7 through 28 bits. Since the simplest mechanization for N of 27 bits requires 8 stages, Table II shows an alternate code for N of 27 which is acceptable and requires 5 stages to mechanize. A designer desiring to use some code other than those shown in Table II must use the procedure developed in Appendix E to verify performance acceptance and submit results to GSFC Data Systems Requirements Committee for approval.

FRAME <u>LENGTH</u>	<u>FSW LENGTH, N.</u>	
	<u>Minimum Acceptable</u>	<u>Desired Minimum</u>
50	11	12
100	12	14
200	13	16
500	15	19
1000	16	21
2000	18	23
5000	21	25
10000	23	28

TABLE I. Minimum acceptable and recommended FSW length as a function of frame length.

TABLE II
FSW CODES

CODE LENGTH

7	101	100	0							
8	101	110	00							
9	101	110	000							
10	110	111	000	0						
11	101	101	110	00						
12	110	101	100	000						
13	111	010	110	000	0					
14	111	001	101	000	00					
15	111	011	001	010	000					
16	111	010	111	001	000	0				
17	111	100	110	101	000	00				
18	111	100	110	101	000	000				
19	111	110	011	001	010	000	0			
20	111	011	011	110	001	000	00			
21	111	011	101	001	011	000	000			
22	111	100	110	110	101	000	000	0		
23	111	101	011	100	110	100	000	00		
24	111	110	101	111	001	100	100	000		
25	111	110	010	110	111	000	100	000	0	
26	111	110	100	110	101	100	010	000	00	
27	111	110	101	101	001	100	110	000	000	
or	000	110	101	000	010	010	110	011	111	(Refer to text)
28	111	101	011	110	010	110	011	000	000	0
29	111	101	011	110	011	001	101	000	000	00
30	111	110	101	111	001	100	110	100	000	000

APPENDIX D

SUMMARY OF EXPERIENCE SURVEY

SUMMARY OF EXPERIENCE SURVEY

Please refer to Section 8 for the acknowledgment of personnel who contributed to this survey.

The survey summary is divided into two parts: the first part contains information pertaining to the initial design of telemetry systems and the second part pertains to the operation and analyses of telemetry systems.

TELEMETRY DESIGN

- a. The design of the telemetry system allows adequate safety margin to more than satisfy the error rate requirement at high elevation angles.
- b. The active PCM programs include OGD-(F and E), OSO-(F and G), RAE-A, ISIS-A, OAO-A2, and ATS-(C and E). None of these systems utilize frame sync word formats recommended by existing PCM standard. The designers were constrained to use designs requiring less power consumption and lower cost. There have been no comments fed back to the designer regarding the inadequacy of any of the designs.
- c. Increasing the number of bits in the frame sync word reduces the mean acquisition time and the probability of false alarm. The only disadvantage is the increased overhead.

TELEMETRY SYSTEM ANALYSIS AND DATA PROCESSING

- a. Test data indicate that the acquisition and maintenance mode strategies are unimportant as long as the E_b/N_0 ratio exceeds 3 dB.
- b. Bit synchronization has not been detected as a problem except for jitter of on-board tape recorders and at low elevation angles.
- c. Except for abnormal atmospheric noise and RFI, the energy per bit to noise power density ratio nearly always exceeds 3 dB except at low elevation angles where multipaths cause severe fades both during acquisition and drop-sync periods.
- d. The severe elevation low-angle fades are accompanied by severe increases in error rates which can severely bias the apparent data quality.
- e. There exists some doubt as to whether any experimenters can use low elevation angle data containing high error rates (approaching 10^{-1}).
- f. Some question exists as to the usefulness of processed experimenter's data at high error rates because of subframe problems -- a problem which can be answered only by the end user. In addition, there is speculation that the user of the processed experimenter's data could derive more information with much less data processing cost by adding parity checks, etc.
- g. Because the present processing strategies are selected for low S/N experienced at low elevation angles, it is normally very difficult to lose frame synchronization.

- h. Test data indicate that as long as the FSW length exceeds sixteen bits, the actual FSW format is not important as long as the format is "random".
- i. There is no record of operational synchronization problems. Some programs have had repetitive control signals which look like FSW, but this situation is immediately apparent and thereafter avoided. The objective of acquiring the maintenance mode at elevation angles below 10° above the local horizon is always satisfied.
- j. The existing systems typically operate with less than 1.0% lost data and error rates less than 10^{-4} , and the percentage of lost data is severely biased by including the performance at low elevation angles.

APPENDIX E

THE IMPACT OF THE CHOICE OF A SYNCHRONIZATION
CODE WORD ON SYNCHRONIZATION PERFORMANCE

By:

DR. SOLOMON W. GOLOMB

NASA CONTRACT NO. NAS5-21196

I. INTRODUCTION

The existing NASA standard for PCM telemetry systems recommends a specific code for each frame sync word length, N , none of which was specifically chosen as a code which could be easily generated by a shift register. The specific code recommended for each length, N , was chosen by examining all 2^N binary patterns and determining that code pattern with the lowest total probability of false sync recognition over the entire overlap portion of the code (assuming random data in the overlap region). Empirical data have verified that the specific choice of frame sync code word pattern is really irrelevant as long as the pattern is random and of sufficient length ($N \geq 16$). Since cost and power consumption are still important design parameters, the use of shift register generated sync codes is desirable. Two approaches to this objective can be followed. One of these is to determine the simplest shift register implementation for the NASA standard synchronization code words. In a separate report, this has been done for all lengths, N , with $7 \leq N \leq 28$. The other approach is to examine the sensitivity of successful synchronization to the specific choice of sync code word, so that a larger class of shift-register generated sync patterns can be considered which will not noticeably degrade sync performance. It is this second approach which will be followed in the present report.

2. SOURCES & FREQUENCIES OF SYNCHRONIZATION ERRORS

Suppose that one uses a synchronization code word of length N at a standard position (e. g. at the beginning) in every frame of length L . We may distinguish between synchronization errors by amounts less than N (errors of Type 1), and synchronization errors by amounts equal to or greater than N (errors of Type 2). In the former case, it is necessary that part of the true sync word form a portion of the spuriously detected sync word, while in the latter case the spurious sync word is composed entirely of other "data bits". No matter how carefully the optimum sync word of length N is chosen, this can only contribute to reducing the former type of errors. Having picked the synchronization word, one can reduce the frequency of errors of Type 2 by making sure that neither data words nor overlaps of data words will resemble the sync word any more often than would be encountered on a random basis.

Suppose that errors occur independently and at random, with a bit error probability γ . The probability that N consecutive random bits of data look exactly like the sync word is 2^{-N} , independent of the value of γ , since random errors in a random bit stream produces yet another random bit stream. The expected number of spurious sync words in a frame of L random bits is effectively $L \cdot 2^{-N}$, representing the incidence of sync errors of Type 2.

The computation for sync errors of Type 1 is somewhat more complicated. For a displacement by γ bits, for $0 < \gamma < N$, the correlation of the sync word with itself consists of $A(\gamma)$ agreements and $D(\gamma)$ disagreements, with $A(\gamma) + D(\gamma) = N - \gamma$, and the un-normalized autocorrelation $C(\gamma)$ is

given by $C(\gamma) = A(\gamma) - D(\gamma)$. The probability of incorrectly detecting the sync word displaced by γ from its true position is accordingly given by

$$u(\gamma) = \gamma^{D(\gamma)} (1-\gamma)^{A(\gamma)} 2^{-\gamma},$$

and the expected number of false sync detections of the first type, per frame, M , is then obtained by summing $u(\gamma)$ over $-(N-1) \leq \gamma \leq (N-1)$, $\gamma \neq 0$, as follows:

$$(\star) M = 2 \sum_{\gamma=1}^{N-1} u(\gamma) = 2(1-\gamma)^N \sum_{\gamma=1}^{N-1} \left(\frac{\gamma}{1-\gamma}\right)^{D(\gamma)} 2^{-\gamma}.$$

This is minimized by keeping $D(\gamma)$ large when γ is small. Specifically, any word which nearly coincides with a small shift of itself (such as all 0's, or all 1's, or 01010101---01, etc.) is a particularly poor choice as a sync word. On the other hand, since $\frac{\gamma}{1-\gamma}$ is not likely to exceed 2^{-10} , any code word for which $D(\gamma) > \frac{N-\gamma}{10}$ for all γ , $0 \leq \gamma < N$ will have fewer false synchronizations of the first type than of the second type.

Thus, a sufficient condition for sync errors of the first type to be less frequent than sync errors of the second type is that $D(\gamma) > \frac{N-\gamma}{\log_2 \left(\frac{1-\gamma}{\gamma} \right)}$ for $1 \leq \gamma \leq N-1$, where γ is the largest value of bit error probability

which the system will encounter.

For a randomly chosen sync word, we would expect $D(\gamma) = \frac{N-\gamma}{2}$,

on the average, and this is (fortunately) much larger than $\frac{N-\gamma}{10}$, or $\frac{N-\gamma}{\log_2 \left(\frac{1-\gamma}{\gamma} \right)}$ for any reasonable bit error rate γ . Almost any shift register sequence chosen will satisfy a reasonable constraint on $D(\gamma)$, and it is a simple computation to test the $D(\gamma)$.

It may seem that errors of the first type are more serious than errors of the second type, because they may be more likely to occur spaced exactly L bits apart, thus seeming to confirm an erroneous synchronization determination. In fact, however, if a reasonable $D(\gamma)$ condition is met, the probability of first type errors in two consecutive frames is vanishingly small, and even when they do occur in consecutive frames, there will be no necessity that the spurious sync detections occur exactly L bits apart.

A far greater practical danger is that there will be particular data words or patterns, or overlaps of such patterns, that will resemble or coincide with the sync word. This would engender rather frequent synchronization errors of the second type. Practical experience as well as a prior reasoning indicates that this problem is far more serious than any which could cause sync errors of the first type.

3. COMPUTATIONAL SIMPLIFICATIONS

Assuming that the bit error rate γ is small (e. g. $\gamma \leq 10^{-3}$) we may use the following approximations for the purpose of computational simplification:

$$\begin{aligned} \frac{\gamma}{1-\gamma} &\approx \gamma \\ \log_2 \frac{(1-\gamma)}{\gamma} &\approx -\log_2 \gamma \\ u(\tau) &\approx \gamma^{D(\tau)} 2^{-\tau} \\ \text{and} \quad M &= 2 \sum_{\tau=1}^{N-1} u(\tau) \approx 2 \sum_{\tau=1}^{N-1} \gamma^{D(\tau)} 2^{-\tau}. \end{aligned}$$

This exhibits very directly the requirement that $D(\tau)$ be large when τ is small in order to keep M small.

If $\gamma = 2^{-k}$, then $-\log_2 \gamma = k$, and the requirement on $D(\tau)$ for acceptable sync code words is $D(\tau) > \frac{N-\tau}{k}$, for all τ , $1 \leq \tau \leq N-1$.

4. SUMMARY AND CONCLUSIONS

In a frame of length L and using a synchronization word of length N , the expected number of sync errors of the second type, per frame, is $L2^{-N}$, assuming random data.

Under the same assumptions, and with a bit error rate γ , the expected number of sync errors of the first type, per frame, is

$$M = 2(1-\gamma)^N \sum_{\tau=1}^{N-1} \left(\frac{\gamma}{1-\gamma}\right)^{D(\tau)} 2^{-\tau} \approx 2 \sum_{\tau=1}^{N-1} \gamma^{D(\tau)} 2^{-\tau}$$

where $D(\tau)$ is the number of disagreements between the sync word and its shift by τ .

$$\text{Any sync word for which } D(\tau) > \frac{N-\tau}{\log_2 \left(\frac{1-\gamma}{\gamma} \right)},$$

for $1 \leq \tau \leq N-1$, will have fewer expected sync errors of the first type than of the second type, and hence will not contribute significantly to the sync problem. In particular, most shift register sequences will satisfy this condition, and can be readily tested before being selected as sync words. Here γ should be chosen as the highest bit error rate against which the system is expected to operate. If $\gamma = 2^{-k}$, the condition on $D(\tau)$ is basically:

$$D(\tau) > \frac{N-\tau}{k} \quad \text{for } 1 \leq \tau \leq N-1.$$

A more serious practical danger is that data patterns or overlaps of data patterns may systematically resemble or coincide with the sync word which has been chosen. This possibility should be considered and eliminated before finally adopting both the sync word and the data format.

5. CORRELATION FUNCTIONS OF THE TELEMETRY STANDARD CODEWORDS

In Table I, we present the function $D(\gamma)$ computed for the synchronization codewords (from the NASA telemetry standard) of lengths 7 through 30, and in Table II, we present the function $C(\gamma)$ computed for the same set of codewords.

As shown in this report, it is the function $D(\gamma)$ which is relevant to the problem of synchronization errors of the first type. For the optimum codewords shown in Table I, it is striking how nearly the behavior of $D(\gamma)$ approaches uniform monotonic decrease from around $.4N$ at $\gamma = 1$ down to 1 at $\gamma = N - 1$. This is the type of behavior corresponding to the requirement that M be minimized. The values of $C(\gamma)$ for $1 \leq \gamma \leq N - 1$ correspondingly start slightly positive, and then become negative for larger values of γ . The average behavior of $C(\gamma)$ is determined by the equation

$$A^2 = \left(\sum_{\gamma=1}^N a_{\gamma} \right)^2 = \sum_{\gamma=1}^{(N-1)} C(\gamma)$$

where $\{a_{\gamma}\}$ is the codeword of length N consisting of $+1$'s and -1 's. For the codewords in question, A^2 has the values 0 or 1, or in only a few cases, 4. Thus, since $C(0) = N$, we have

$$\text{and} \quad A^2 = N + 2 \sum_{\gamma=1}^{N-1} C(\gamma)$$

$$\sum_{\gamma=1}^{N-1} C(\gamma) = \frac{A^2 - N}{2}$$

so that the average of $C(\gamma)$ for $1 \leq \gamma \leq (N - 1)$ is

$$\overline{C(\gamma)} = \frac{A^2 - N}{2(N-1)} \approx -\frac{1}{2}$$

For a randomly chosen codeword, $C(\gamma)$ would fluctuate randomly around the $-\frac{1}{2}$ value, while for the optimum list of codewords, there is a clear bias in $C(\gamma)$, starting from positive values for small γ , and then going over to negative values.

TABLE I: Correlation Behavior of the PCM Telemetry Standard Synchronization Code Words:
The Function $D(\tau)$.

<u>Length</u>	<u>Sequence</u>	<u>$D(\tau), 1 \leq \tau \leq N-1$</u>
7	1011000	3, 3, 2, 2, 1, 1.
8	10111000	3, 3, 4, 2, 2, 1, 1.
9	101110000	3, 3, 4, 3, 3, 2, 1, 1.
10	1101110000	3, 4, 4, 3, 3, 3, 2, 2, 1.
11	10110111000	5, 5, 4, 4, 3, 3, 2, 2, 1, 1.
12	110101100000	5, 4, 4, 5, 3, 3, 3, 3, 2, 2, 1.
13	1110101100000	5, 4, 5, 5, 4, 3, 3, 4, 3, 3, 2, 1.
14	11100110100000	5, 6, 5, 5, 5, 3, 4, 3, 3, 3, 3, 2, 1.
15	111011001010000	7, 6, 5, 5, 5, 4, 5, 3, 4, 3, 3, 3, 2, 1.
16	1110101110010000	7, 6, 7, 5, 5, 5, 4, 6, 4, 3, 3, 3, 3, 2, 1.
17	11110011010100000	7, 6, 7, 6, 6, 5, 6, 4, 4, 4, 3, 4, 4, 3, 2, 1.
18	111100110101000000	7, 6, 7, 6, 6, 6, 6, 5, 4, 5, 4, 4, 4, 4, 3, 2, 1.
19	1111100110010100000	7, 8, 7, 6, 7, 6, 6, 6, 5, 5, 4, 4, 4, 5, 4, 3, 2, 1.
20	11101101111000100000	7, 8, 7, 7, 6, 6, 6, 7, 6, 6, 8, 5, 4, 4, 4, 3, 3, 2, 1.
21	111011101001011000000	9, 8, 7, 9, 8, 7, 7, 6, 5, 6, 6, 5, 4, 5, 5, 4, 3, 3, 2, 1.
22	1111001101101010000000	9, 8, 7, 8, 8, 8, 7, 7, 7, 7, 6, 5, 5, 5, 5, 4, 4, 4, 3, 2, 1.
23	11110101110011010000000	9, 8, 9, 8, 8, 7, 7, 7, 10, 6, 7, 5, 6, 6, 5, 5, 5, 4, 4, 3, 2, 1.
24	111110101111001100100000	9, 10, 9, 8, 9, 8, 7, 7, 7, 7, 8, 7, 8, 5, 5, 5, 5, 4, 5, 4, 3, 2, 1.
25	1111100101101110001000000	9, 10, 9, 10, 9, 9, 10, 9, 7, 8, 6, 7, 7, 6, 6, 5, 5, 4, 5, 5, 4, 3, 2, 1.
26	11111010011010110001000000	11, 10, 9, 10, 9, 9, 11, 9, 7, 8, 8, 7, 6, 7, 6, 6, 5, 5, 5, 5, 5, 4, 3, 2, 1.
27	111110101101001100110000000	11, 12, 9, 10, 9, 11, 10, 9, 9, 8, 8, 8, 7, 7, 6, 6, 6, 5, 5, 6, 5, 5, 4, 3, 2, 1.
28	1111010111100101100110000000	11, 12, 11, 12, 10, 9, 9, 9, 11, 8, 9, 8, 7, 8, 7, 8, 7, 6, 5, 5, 5, 5, 4, 4, 3, 2, 1.
29	11110101111001100110100000000	11, 12, 11, 10, 10, 11, 9, 10, 10, 9, 9, 8, 8, 11, 7, 8, 6, 7, 7, 6, 6, 5, 5, 4, 4, 3, 2, 1.
30	111110101111001100110100000000	11, 12, 11, 10, 11, 11, 10, 10, 10, 9, 9, 9, 9, 11, 7, 9, 7, 7, 7, 7, 6, 6, 6, 5, 5, 4, 3, 2, 1.

NOT REPRODUCIBLE

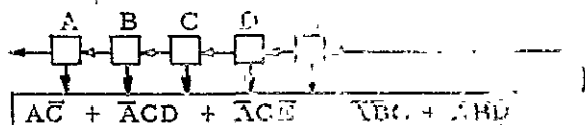
[illegible]

6. A SIMPLE SHIFT REGISTER OF LENGTH 27

A simple modulo-2 shift register of length 27 yields a sequence of period 31 which satisfies the synchronization relation,

$$A_n = A_{n-3} \oplus A_{n-27}$$

yields a sequence of period 27, as shown by the shift register shown below:



Starting with the identified state 00011, we get the 27-bit synchronization codeword:

000 110 101 001 010 010 110 011 111.

The auto-correlation function of this sequence is as follows:

	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26
D(γ)	0	13	12	11	10	9	8	7	6	5	4	3	2	1	0	1	2	3	4	5	6	7	8	9	10	11	12
C(γ)	27	0	1	2	-3	4	-1	5	-2	0	7	-4	-1	-2	-3	0	-1	-2	-1	1	0	-1	-2	-3	-2	-1	

In contrast with the optimum codeword, selected in paragraph 5, the behavior of $D(\gamma)$ is a different function of γ . In the case of $D(10) = 5$ and $D(20) = 2$. (For the optimum codeword of length 27, $D(10) = 3$ and $D(20) = 6$.) However, even these small values have a significant impact on the value of M , in that synchronization errors of the first type will be far less frequent than sync errors of the second type for the shift register of length 27.

The contrast in behavior can be observed in the function $C(\gamma)$, where the optimum codeword of length 27 will be $C(\gamma) = 6$ for $\gamma > 11$, and $C(\gamma) < 0$ for $\gamma > 16$. For the shift register selected, $C(\gamma) > 0$ at $\gamma = 20$, and $C(\gamma) = 0$ at $\gamma = 21$. Still, this desirable characteristic has no real significance under operating conditions.

APPENDIX F

SHIFT REGISTER MECHANIZATION OF RECOMMENDED (STANDARD)

FRAME SYNCHRONIZATION WORD CODE

By:

DR. SOLOMON W. GOLOMB

NASA CONTRACT NO. NAS5-21196

N=7

SEQUENCE: 1011000

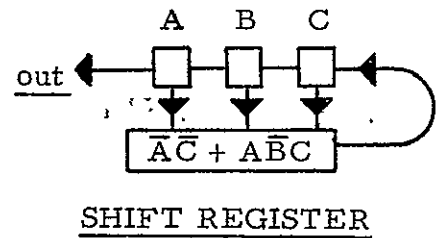
SPAN:

TRUTH TABLE

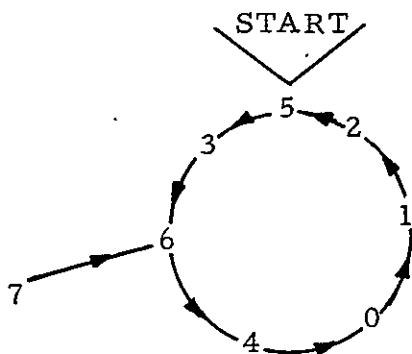
	A	B	C	f
5	1	0	1	1
3	0	1	1	0
6	1	1	0	0
4	1	0	0	0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1

		C
	1	0
	1	0
A	0	1
	0	1
		B

KARNAUGH CHART



STATE DIAGRAM:



	A	B	C	f	
0	0	0	0	1	1
1	0	0	1	0	2
2	0	1	0	1	5
3	0	1	1	0	6
4	1	0	0	0	0
5	1	0	1	1	3
6	1	1	0	0	4
7	1	1	1	0	6

SUCCESSOR TABLE

SEQUENCE: 10111000

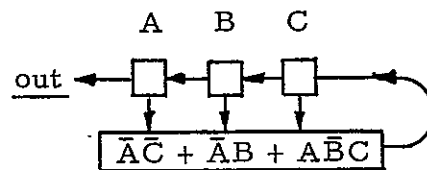
SPAN: 3

TRUTH TABLE

	A	B	C	f
5	1	0	1	1
3	0	1	1	1
7	1	1	1	0
6	1	1	0	0
4	1	0	0	0
0	0	0	0	1
1	0	0	1	0
2	0	1	0	1

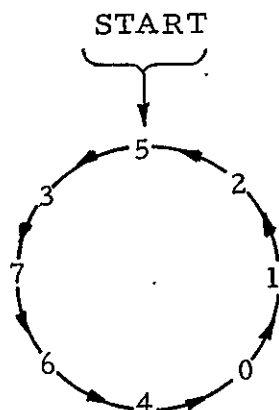
		C
	1	0
	1	1
A	0	0
	0	1
		B

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SHIFT REGISTER

STATE DIAGRAM:



	A	B	C	f	
0	0	0	0	1	1
1	0	0	1	0	2
2	0	1	0	1	5
3	0	1	1	1	7
4	1	0	0	0	0
5	1	0	1	1	3
6	1	1	0	0	4
7	1	1	1	0	6

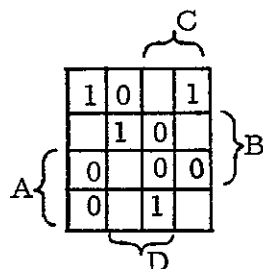
SUCCESSOR TABLE

SEQUENCE: 101110000

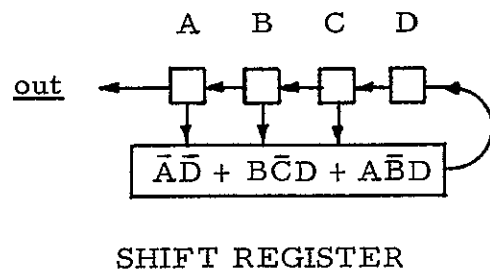
SPAN:

TRUTH TABLE

	A	B	C	D	f
11	1	0	1	1	1
7	0	1	1	1	0
14	1	1	1	0	0
12	1	1	0	0	0
8	1	0	0	0	0
0	0	0	0	0	1
1	0	0	0	1	0
2	0	0	1	0	1
5	0	1	0	1	1

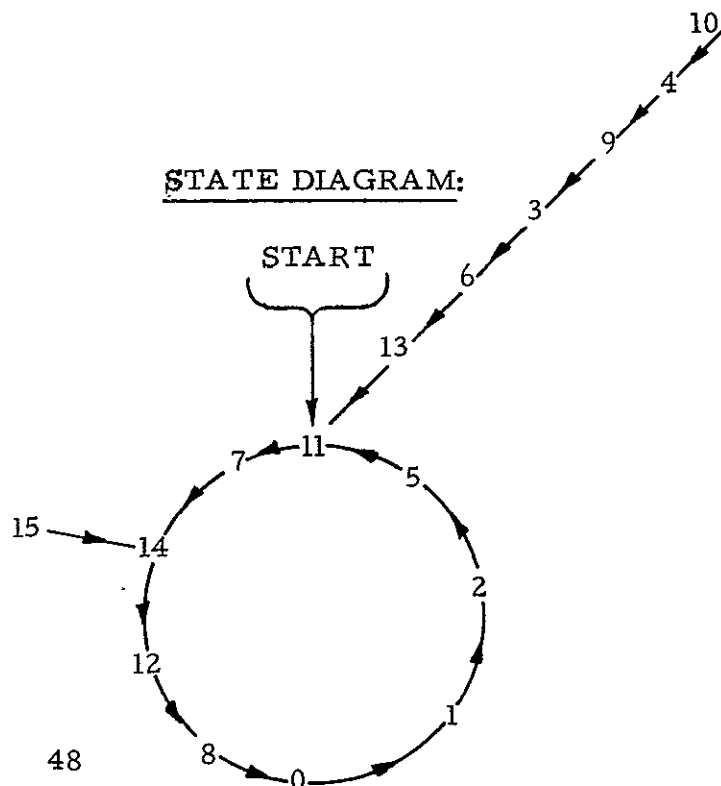


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SHIFT REGISTER

STATE DIAGRAM:



	A	B	C	D	f	
0	0	0	0	0	1	1
1	0	0	0	1	0	2
2	0	0	1	0	1	5
3	0	0	1	1	0	6
4	0	1	0	0	1	9
5	0	1	0	1	1	11
6	0	1	1	0	1	13
7	0	1	1	1	0	14
8	1	0	0	0	0	0
9	1	0	0	1	1	3
10	1	0	1	0	0	4
11	1	0	1	1	1	7
12	1	1	0	0	0	8
13	1	1	0	1	1	11
14	1	1	1	0	0	12
15	1	1	1	1	0	14

SUCCESSOR TABLE

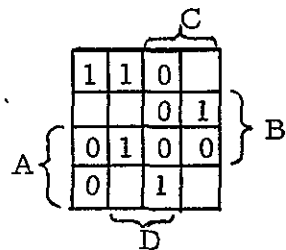
N=10

SEQUENCE: 1101110000

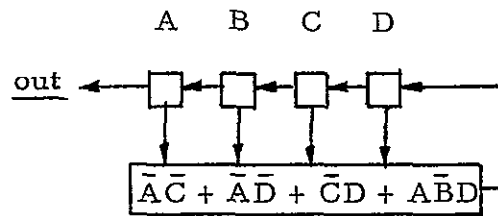
SPAN: 4

TRUTH TABLE

	A	B	C	D	f
13	1	1	0	1	1
11	1	0	1	1	1
7	0	1	1	1	0
14	1	1	1	0	0
12	1	1	0	0	0
8	1	0	0	0	0
0	0	0	0	0	1
1	0	0	0	1	1
3	0	0	1	1	0
6	0	1	1	0	1

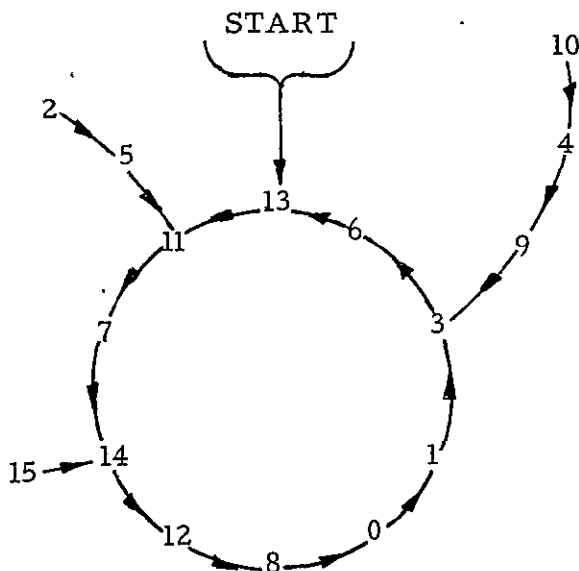


KARNAUGH CHART



SHIFT REGISTER

STATE DIAGRAM:



	A	B	C	D	f	
0	0	0	0	0	1	1
1	0	0	0	1	1	3
2	0	0	1	0	1	5
3	0	0	1	1	0	6
4	0	1	0	0	1	9
5	0	1	0	1	1	11
6	0	1	1	0	1	13
7	0	1	1	1	0	14
8	1	0	0	0	0	0
9	1	0	0	1	1	3
10	1	0	1	0	0	4
11	1	0	1	1	1	7
12	1	1	0	0	0	8
13	1	1	0	1	1	11
14	1	1	1	0	0	12
15	1	1	1	1	0	14

SUCCESSOR TABLE

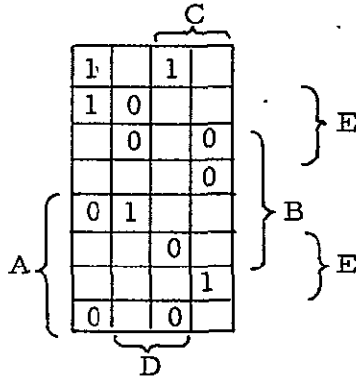
100

110101100000

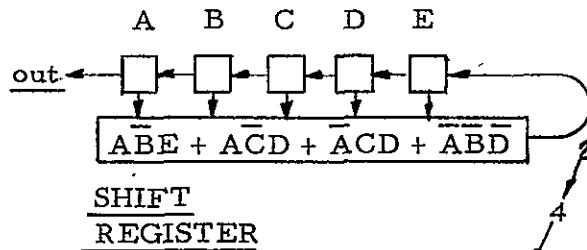
5

TRUTH TABLE

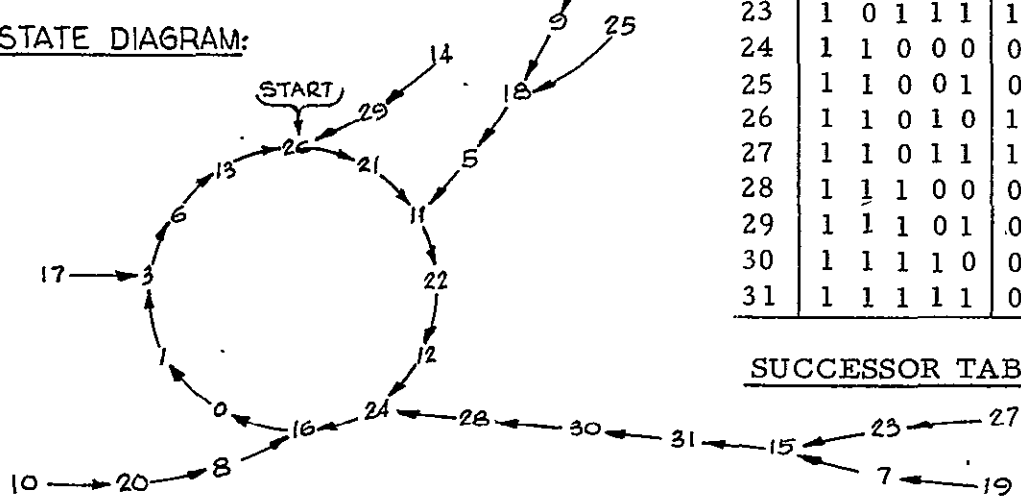
	A	B	C	D	E	f
26	1	1	0	1	0	1
21	1	0	1	0	1	1
11	0	1	0	1	1	0
22	1	0	1	1	0	0
12	0	1	1	0	0	0
24	1	1	0	0	0	0
16	1	0	0	0	0	0
0	0	0	0	0	0	1
1	0	0	0	0	1	1
3	0	0	0	1	1	0
6	0	0	1	1	0	1
13	0	1	1	0	1	0



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STATE DIAGRAM:



SUCCESSOR TABLE

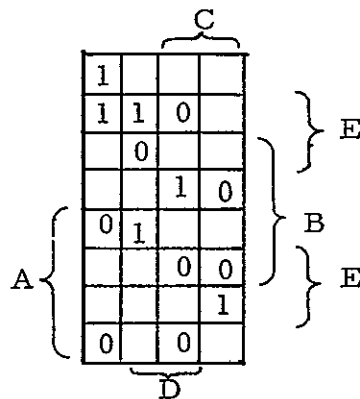
	A	B	C	D	E	♀	
0	0	0	0	0	0	1	1
1	0	0	0	0	1	1	3
2	0	0	0	1	0	0	4
3	0	0	0	1	1	0	6
4	0	0	1	0	0	1	9
5	0	0	1	0	1	1	11
6	0	0	1	1	0	1	13
7	0	0	1	1	1	1	15
8	0	1	0	0	0	0	16
9	0	1	0	0	1	0	18
10	0	1	0	1	0	0	20
11	0	1	0	1	1	0	22
12	0	1	1	0	0	0	24
13	0	1	1	0	1	0	26
14	0	1	1	1	0	1	29
15	0	1	1	1	1	1	31
16	1	0	0	0	0	0	0
17	1	0	0	0	1	1	3
18	1	0	0	1	0	1	5
19	1	0	0	1	1	1	7
20	1	0	1	0	0	0	8
21	1	0	1	0	1	1	11
22	1	0	1	1	0	0	12
23	1	0	1	1	1	1	15
24	1	1	0	0	0	0	16
25	1	1	0	0	1	0	18
26	1	1	0	1	0	1	21
27	1	1	0	1	1	1	23
28	1	1	1	0	0	0	24
29	1	1	1	0	1	0	26
30	1	1	1	1	0	0	28
31	1	1	1	1	1	0	30

N=13

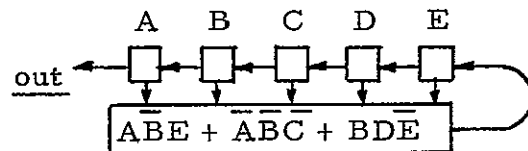
5

TRUTH TABLE

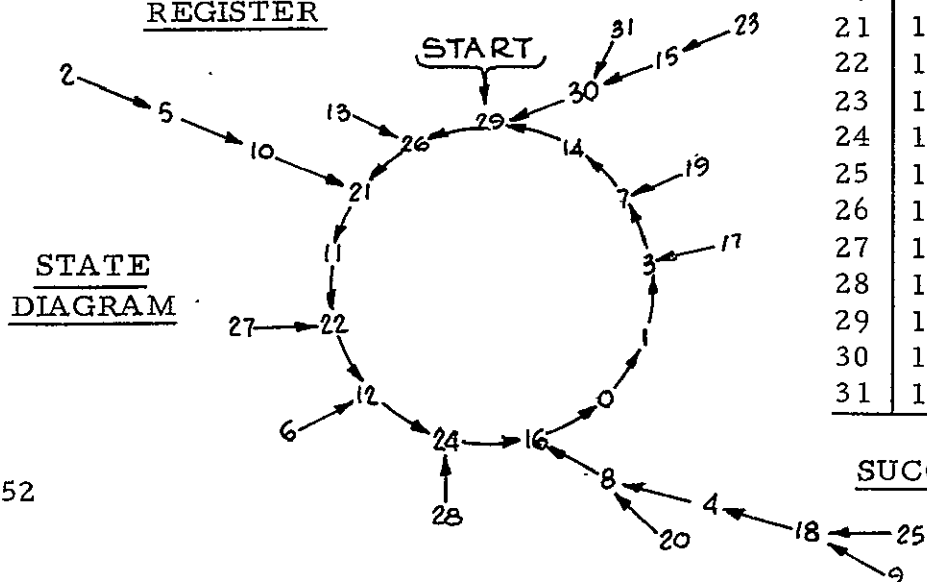
	A	B	C	D	E	f
29	1	1	1	0	1	0
26	1	1	0	1	0	1
21	1	0	1	0	1	1
11	0	1	0	1	1	0
22	1	0	1	1	0	0
12	0	1	1	0	0	0
24	1	1	0	0	0	0
16	1	0	0	0	0	0
0	0	0	0	0	0	1
1	0	0	0	0	1	1
3	0	0	0	1	1	1
7	0	0	1	1	1	0
14	0	1	1	1	0	1



KARNAUGH CHART



SHIFT
REGISTER



	A	B	C	D	E	ϕ	
0	0	0	0	0	0	1	1
1	0	0	0	0	1	1	3
2	0	0	0	1	0	1	5
3	0	0	0	1	1	1	7
4	0	0	1	0	0	0	8
5	0	0	1	0	1	0	10
6	0	0	1	1	0	0	12
7	0	0	1	1	1	0	14
8	0	1	0	0	0	0	16
9	0	1	0	0	1	0	18
10	0	1	0	1	0	1	21
11	0	1	0	1	1	0	22
12	0	1	1	0	0	0	24
13	0	1	1	0	1	0	26
14	0	1	1	1	0	1	29
15	0	1	1	1	1	0	30
16	1	0	0	0	0	0	0
17	1	0	0	0	1	1	3
18	1	0	0	1	0	0	4
19	1	0	0	1	1	1	7
20	1	0	1	0	0	0	8
21	1	0	1	0	1	1	11
22	1	0	1	1	0	0	12
23	1	0	1	1	1	1	15
24	1	1	0	0	0	0	16
25	1	1	0	0	1	0	18
26	1	1	0	1	0	1	21
27	1	1	0	1	1	0	22
28	1	1	1	0	0	0	24
29	1	1	1	0	1	0	26
30	1	1	1	1	0	1	29
31	1	1	1	1	1	0	30

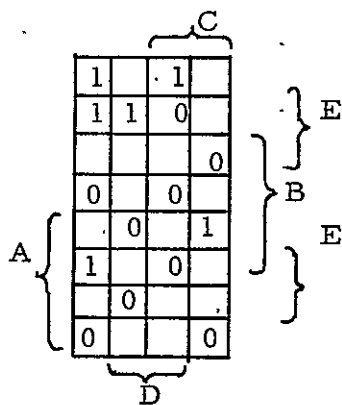
SUCCESSOR TABLE

11100110100000

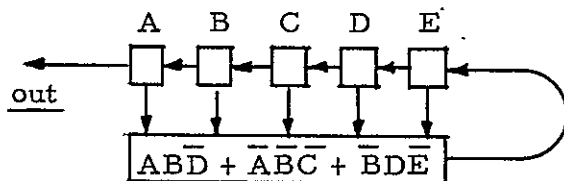
SPAN:

5

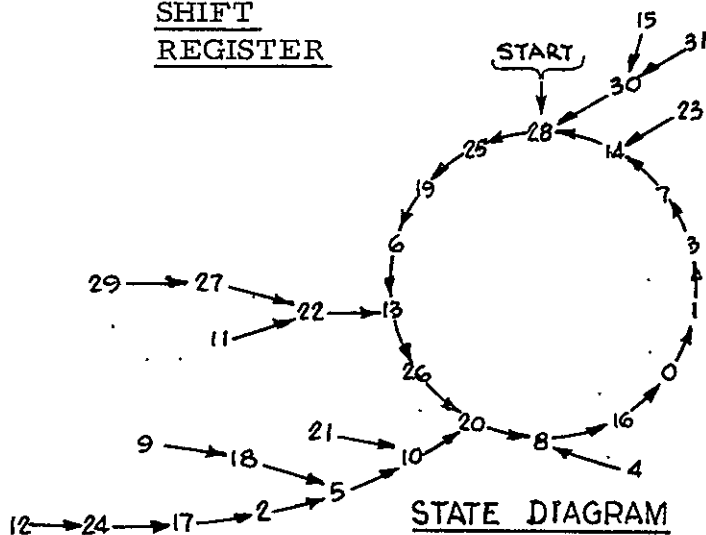
	A	B	C	D	E	f
28	1	1	1	0	0	1
25	1	1	0	0	1	1
19	1	0	0	1	1	0
6	0	0	1	1	0	1
13	0	1	1	0	1	0
26	1	1	0	1	0	0
20	1	0	1	0	0	0
8	0	1	0	0	0	0
16	1	0	0	0	0	0
0	0	0	0	0	0	1
1	0	0	0	0	1	1
3	0	0	0	1	1	1
7	0	0	1	1	1	0
14	0	1	1	1	0	0



KARNAUGH CHART



SHIFT
REGISTER



	A	B	C	D	E	f	
0	0	0	0	0	0	1	1
1	0	0	0	0	1	1	3
2	0	0	0	1	0	1	5
3	0	0	0	1	1	1	7
4	0	0	1	0	0	0	8
5	0	0	1	0	1	0	10
6	0	0	1	1	0	1	13
7	0	0	1	1	1	0	14
8	0	1	0	0	0	0	16
9	0	1	0	0	1	0	18
10	0	1	0	1	0	0	20
11	0	1	0	1	1	0	22
12	0	1	1	0	0	0	24
13	0	1	1	0	1	0	26
14	0	1	1	1	0	0	28
15	0	1	1	1	1	0	30
16	1	0	0	0	0	0	0
17	1	0	0	0	1	0	2
18	1	0	0	1	0	1	5
19	1	0	0	1	1	0	6
20	1	0	1	0	0	0	8
21	1	0	1	0	1	0	10
22	1	0	1	1	0	1	13
23	1	0	1	1	1	0	14
24	1	1	0	0	0	1	17
25	1	1	0	0	1	1	19
26	1	1	0	1	0	0	20
27	1	1	0	1	1	0	22
28	1	1	1	0	0	1	25
29	1	1	1	0	1	1	27
30	1	1	1	1	0	0	28
31	1	1	1	1	1	0	30

SUCCESSOR TABLE

SEQUENCE:

1110101110010000

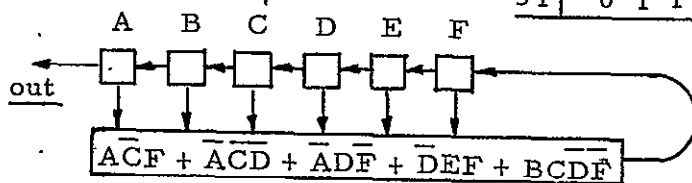
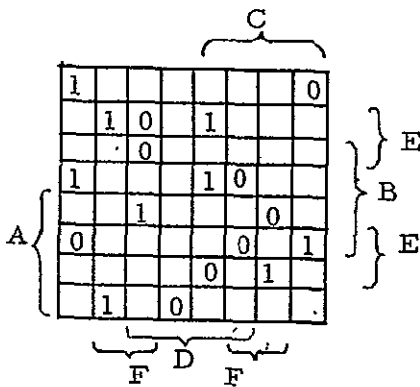
N=16

SPAN:

6

TRUTH TABLE

	A	B	C	D	E	F	f
58	1	1	1	0	1	0	1
53	1	1	0	1	0	1	1
43	1	0	1	0	1	1	1
23	0	1	0	1	1	1	0
46	1	0	1	1	1	0	0
28	0	1	1	1	0	0	1
57	1	1	1	0	0	1	0
50	1	1	0	0	1	0	0
36	1	0	0	1	0	0	0
8	0	0	1	0	0	0	0
16	0	1	0	0	0	0	1
33	1	0	0	0	0	1	1
3	0	0	0	0	1	1	1
7	0	0	0	1	1	1	0
14	0	0	1	1	1	0	1
29	0	1	1	1	0	1	0

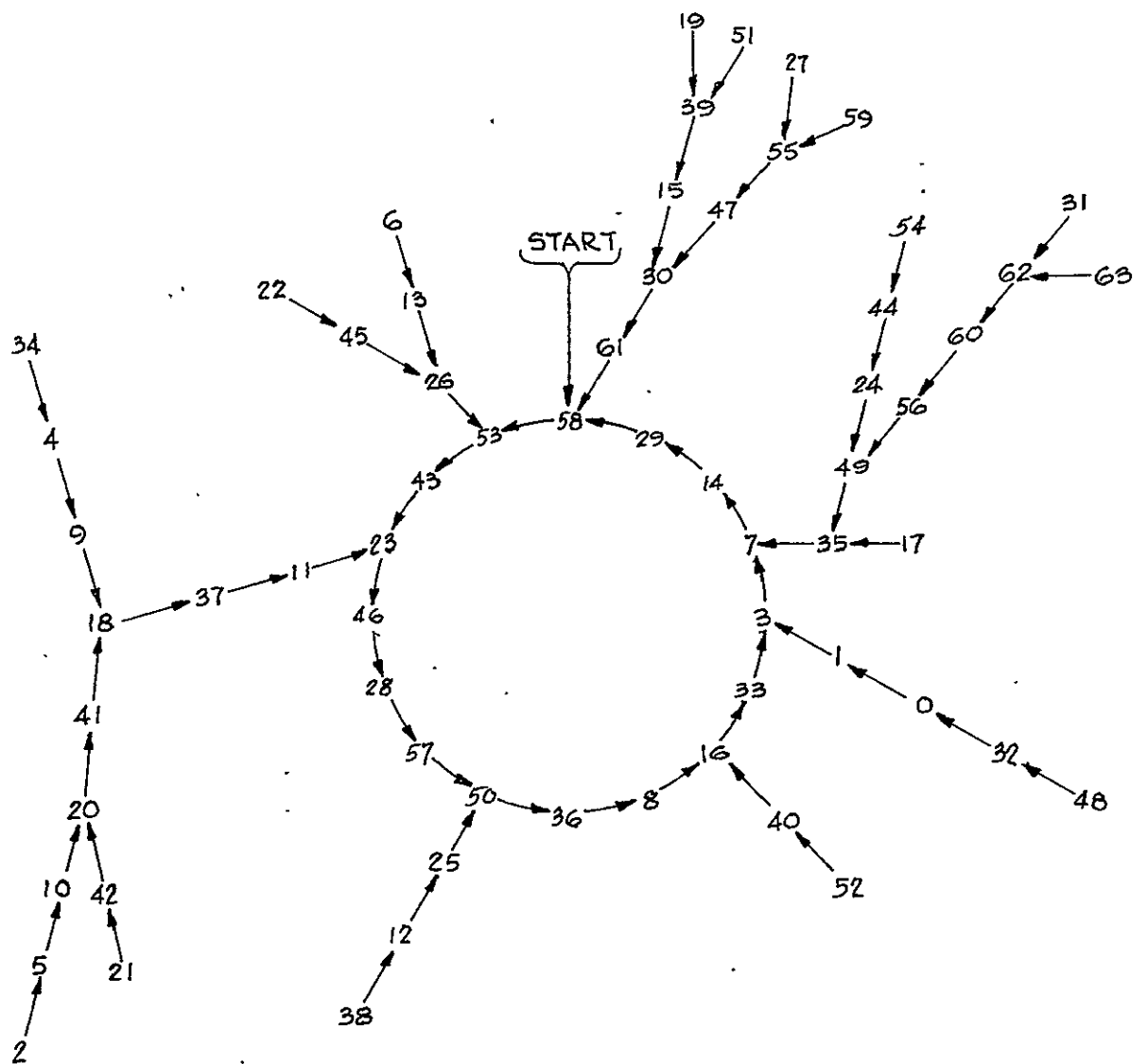


SHIFT REGISTER

	A	B	C	D	E	F	f		A	B	C	D	E	F	f	
0	0	0	0	0	0	0	1	1	32	1	0	0	0	0	0	0
1	0	0	0	0	0	1	1	3	33	1	0	0	0	0	1	1
2	0	0	0	0	1	0	1	5	34	1	0	0	0	1	0	0
3	0	0	0	0	1	1	1	7	35	1	0	0	0	1	1	1
4	0	0	0	1	0	0	1	9	36	1	0	0	1	0	0	0
5	0	0	0	1	0	1	0	10	37	1	0	0	1	0	1	1
6	0	0	0	1	1	0	1	13	38	1	0	0	1	1	0	0
7	0	0	0	1	1	1	0	14	39	1	0	0	1	1	1	1
8	0	0	1	0	0	0	0	16	40	1	0	1	0	0	0	0
9	0	0	1	0	0	1	0	18	41	1	0	1	0	0	1	0
10	0	0	1	0	1	0	0	20	42	1	0	1	0	1	0	0
11	0	0	1	0	1	1	1	23	43	1	0	1	0	1	1	1
12	0	0	1	1	0	0	1	25	44	1	0	1	1	0	0	0
13	0	0	1	1	0	1	0	26	45	1	0	1	1	0	1	0
14	0	0	1	1	1	0	1	29	46	1	0	1	1	1	0	0
15	0	0	1	1	1	1	0	30	47	1	0	1	1	1	1	0
16	0	1	0	0	0	0	1	33	48	1	1	0	0	0	0	0
17	0	1	0	0	0	1	1	35	49	1	1	0	0	0	1	1
18	0	1	0	0	1	0	1	37	50	1	1	0	0	1	0	0
19	0	1	0	0	1	1	1	39	51	1	1	0	0	1	1	1
20	0	1	0	1	0	0	1	41	52	1	1	0	1	0	0	0
21	0	1	0	1	0	1	0	42	53	1	1	0	1	0	1	1
22	0	1	0	1	1	0	1	45	54	1	1	0	1	1	0	0
23	0	1	0	1	1	1	0	46	55	1	1	0	1	1	1	1
24	0	1	1	0	0	0	1	49	56	1	1	1	0	0	0	1
25	0	1	1	0	0	1	0	50	57	1	1	1	0	0	1	0
26	0	1	1	0	1	0	1	53	58	1	1	1	0	1	0	1
27	0	1	1	0	1	1	1	55	59	1	1	1	0	1	1	1
28	0	1	1	1	0	0	1	57	60	1	1	1	1	0	0	0
29	0	1	1	1	0	1	0	58	61	1	1	1	1	0	1	0
30	0	1	1	1	1	0	1	61	62	1	1	1	1	1	0	0
31	0	1	1	1	1	1	0	62	63	1	1	1	1	1	1	0

SUCCESSOR TABLE

N=16



STATE DIAGRAM

N=17

5

TRUTH TABLE

1		1	
1	1	1	
		0	0
0	0		
	1	0	1
1		0	
	0		0
0			0

KARNAUGH CHART



	A	B	C	D	E	f	
0	0	0	0	0	0	1	1
1	0	0	0	0	1	1	3
2	0	0	0	1	0	1	5
3	0	0	0	1	1	1	7
4	0	0	1	0	0	1	9
5	0	0	1	0	1	1	11
6	0	0	1	1	0	1	13
7	0	0	1	1	1	1	15
8	0	1	0	0	0	0	16
9	0	1	0	0	1	1	19
10	0	1	0	1	0	0	20
11	0	1	0	1	1	1	23
12	0	1	1	0	0	0	24
13	0	1	1	0	1	0	26
14	0	1	1	1	0	0	28
15	0	1	1	1	1	0	30
16	1	0	0	0	0	0	0
17	1	0	0	0	1	0	2
18	1	0	0	1	0	0	4
19	1	0	0	1	1	0	6
20	1	0	1	0	0	0	8
21	1	0	1	0	1	0	10
22	1	0	1	1	0	0	12
23	1	0	1	1	1	0	14
24	1	1	0	0	0	1	17
25	1	1	0	0	1	1	19
26	1	1	0	1	0	1	21
27	1	1	0	1	1	1	23
28	1	1	1	0	0	1	25
29	1	1	1	0	1	1	27
30	1	1	1	1	0	0	28
31	1	1	1	1	1	0	30

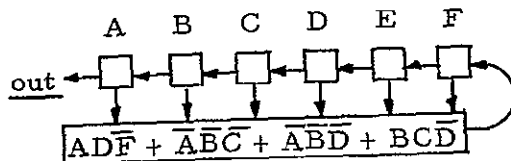
SEQUENCE: 111100110101000000

N=18

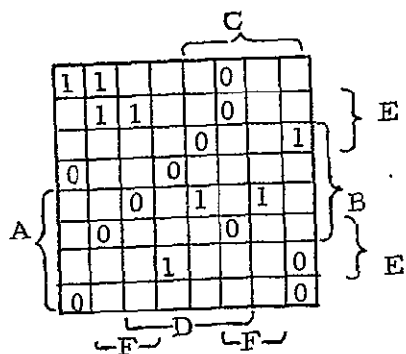
SPAN: 6

TRUTH TABLE

	A	B	C	D	E	F	f
60	1	1	1	1	0	0	1
57	1	1	1	0	0	1	1
51	1	1	0	0	1	1	0
38	1	0	0	1	1	0	1
13	0	0	1	1	0	1	0
26	0	1	1	0	1	0	1
53	1	1	0	1	0	1	0
42	1	0	1	0	1	0	0
20	0	1	0	1	0	0	0
40	1	0	1	0	0	0	0
16	0	1	0	0	0	0	0
32	1	0	0	0	0	0	0
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	1
3	0	0	0	0	1	1	1
7	0	0	0	1	1	1	1
15	0	0	1	1	1	1	0
30	0	1	1	1	1	0	0



SHIFT REGISTER

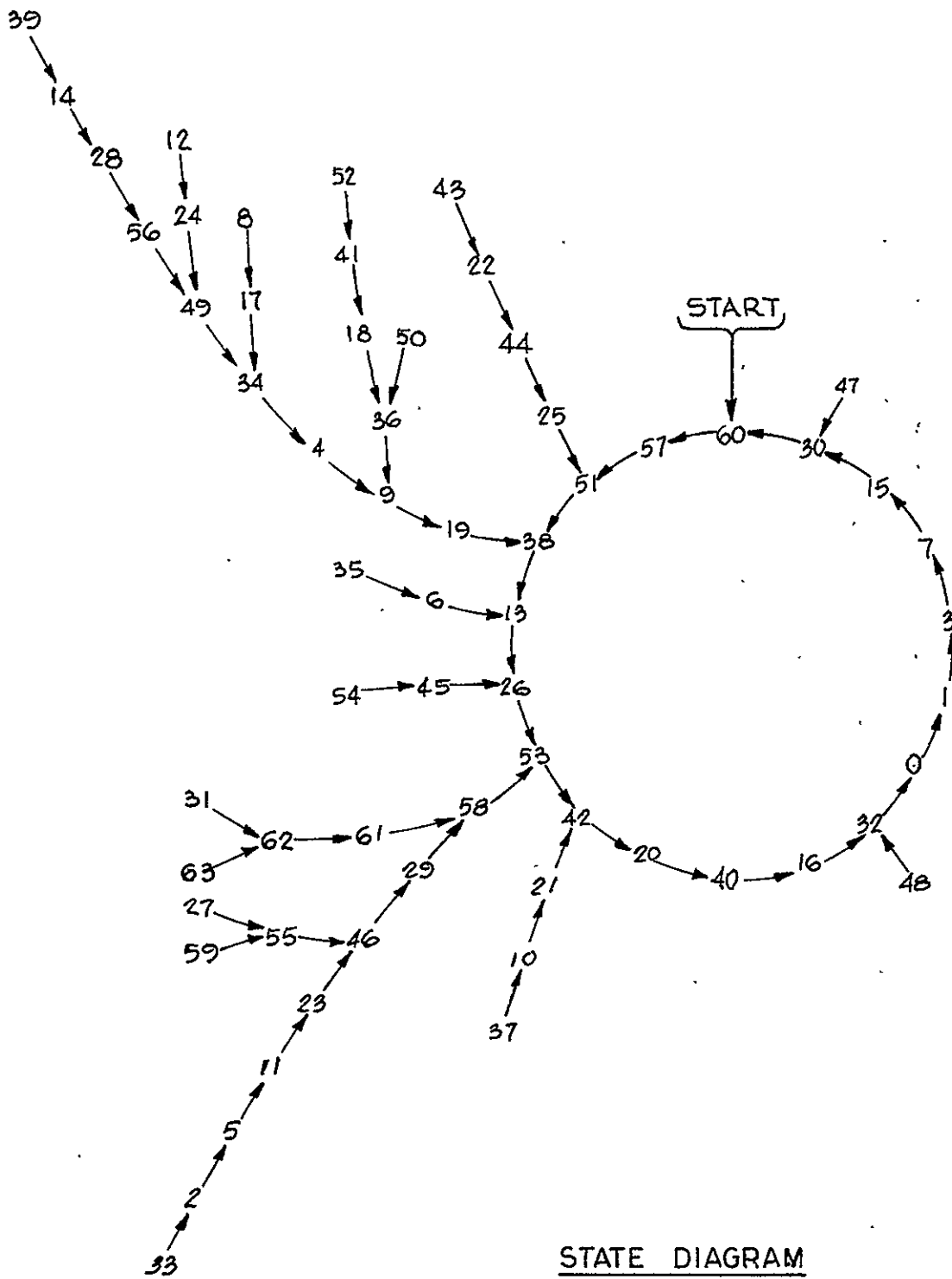


KARNAUGH CHART

	A	B	C	D	E	F	f		A	B	C	D	E	F	f
0	0	0	0	0	0	0	1	1	32	1	0	0	0	0	0
1	0	0	0	0	0	1	1	3	33	1	0	0	0	0	1
2	0	0	0	0	1	0	1	5	34	1	0	0	0	1	0
3	0	0	0	0	1	1	1	7	35	1	0	0	0	1	1
4	0	0	0	1	0	0	1	9	36	1	0	0	1	0	0
5	0	0	0	1	0	1	1	11	37	1	0	0	1	0	1
6	0	0	0	1	1	0	1	13	38	1	0	0	1	1	0
7	0	0	0	1	1	1	1	15	39	1	0	0	1	1	1
8	0	0	1	0	0	0	1	17	40	1	0	1	0	0	0
9	0	0	1	0	0	1	1	19	41	1	0	1	0	0	1
10	0	0	1	0	1	0	1	21	42	1	0	1	0	1	0
11	0	0	1	0	1	1	1	23	43	1	0	1	0	1	1
12	0	0	1	1	0	0	0	24	44	1	0	1	1	0	0
13	0	0	1	1	0	1	0	26	45	1	0	1	1	0	1
14	0	0	1	1	1	0	0	28	46	1	0	1	1	1	0
15	0	0	1	1	1	1	0	30	47	1	0	1	1	1	1
16	0	1	0	0	0	0	0	32	48	1	1	0	0	0	0
17	0	1	0	0	0	1	0	34	49	1	1	0	0	0	1
18	0	1	0	0	1	0	0	36	50	1	1	0	0	1	0
19	0	1	0	0	1	1	0	38	51	1	1	0	0	1	1
20	0	1	0	1	0	0	0	40	52	1	1	0	1	0	0
21	0	1	0	1	0	1	0	42	53	1	1	0	1	0	1
22	0	1	0	1	1	0	0	44	54	1	1	0	1	1	0
23	0	1	0	1	1	1	0	46	55	1	1	0	1	1	1
24	0	1	1	0	0	0	1	49	56	1	1	1	0	0	0
25	0	1	1	0	0	1	1	51	57	1	1	1	0	0	1
26	0	1	1	0	1	0	1	53	58	1	1	1	0	1	0
27	0	1	1	0	1	1	1	55	59	1	1	1	0	1	1
28	0	1	1	1	0	0	0	56	60	1	1	1	1	0	0
29	0	1	1	1	0	1	0	58	61	1	1	1	1	0	1
30	0	1	1	1	1	0	0	60	62	1	1	1	1	1	0
31	0	1	1	1	1	1	0	62	63	1	1	1	1	1	1

SUCCESSOR TABLE

N=18



STATE DIAGRAM

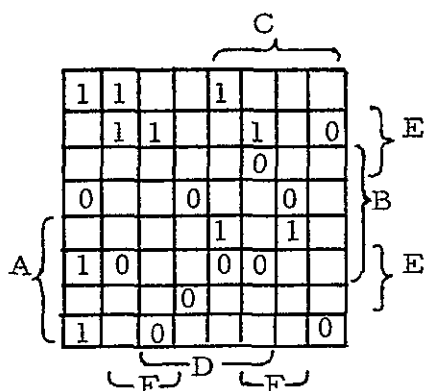
N=19

SEQUENCE: 1111100110010100000

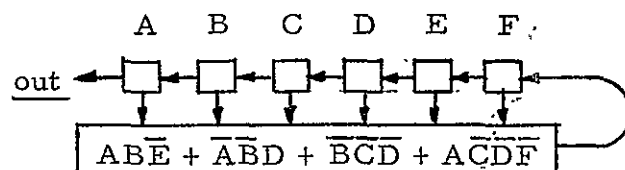
SPAN: 6

TRUTH TABLE

	A	B	C	D	E	F	f
62	1	1	1	1	1	0	0
60	1	1	1	1	0	0	1
57	1	1	1	0	0	1	1
51	1	1	0	0	1	1	0
38	1	0	0	1	1	0	0
12	0	0	1	1	0	0	1
25	0	1	1	0	0	1	0
50	1	1	0	0	1	0	1
37	1	0	0	1	0	1	0
19	0	0	1	0	1	0	0
20	0	1	0	1	0	0	0
40	1	0	1	0	0	0	0
16	0	1	0	0	0	0	0
32	1	0	0	0	0	0	1
1	0	0	0	0	0	1	1
3	0	0	0	0	1	1	1
7	0	0	0	1	1	1	1
15	0	0	1	1	1	1	1
31	0	1	1	1	1	1	0



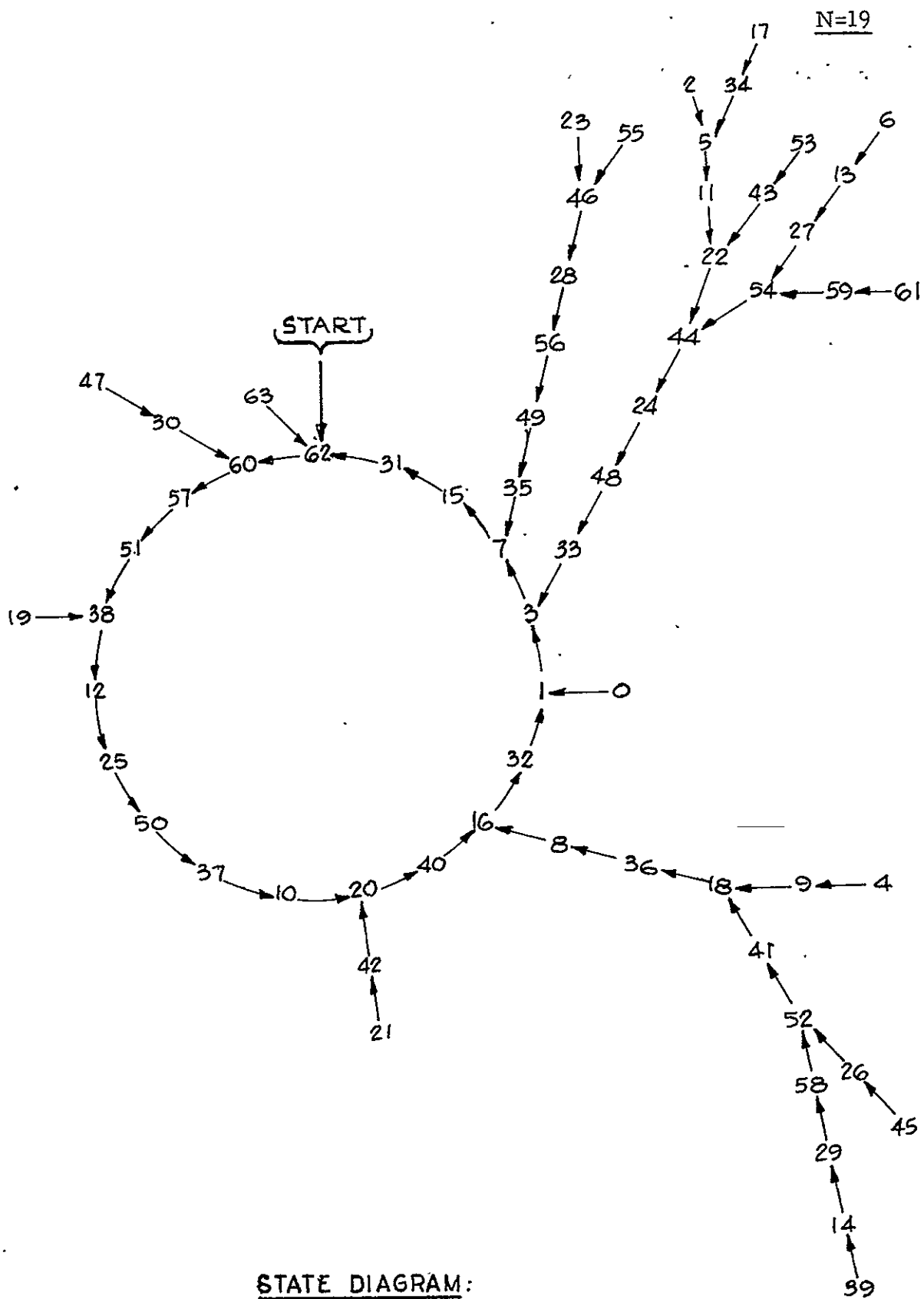
KARNAUGH CHART



SHIFT REGISTER

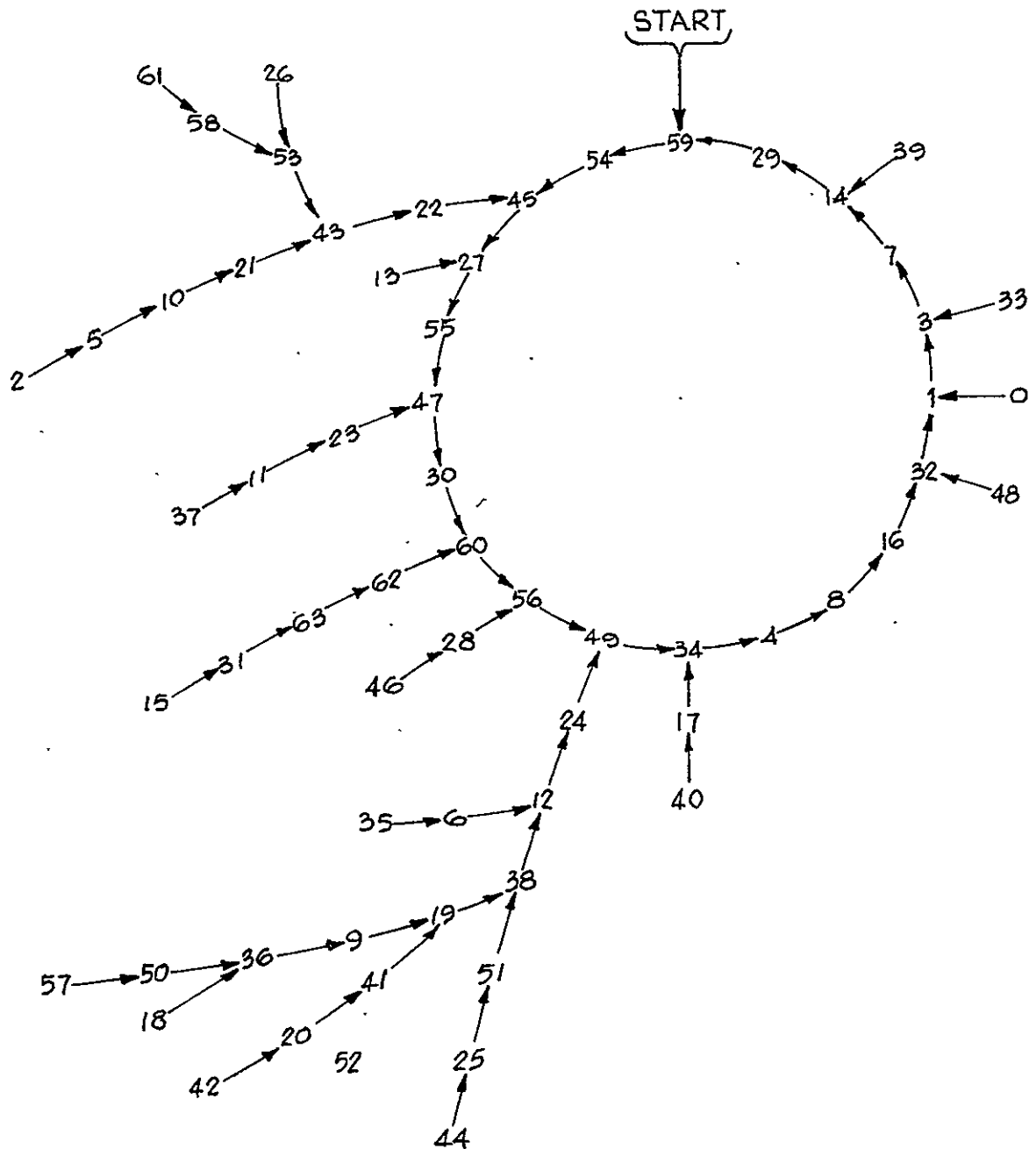
	A	B	C	D	E	F	f		A	B	C	D	E	F	f	
0	0	0	0	0	0	0	1	1	32	1	0	0	0	0	0	1
1	0	0	0	0	0	1	1	3	33	1	0	0	0	0	1	3
2	0	0	0	0	1	0	1	5	34	1	0	0	0	1	0	5
3	0	0	0	0	1	1	1	7	35	1	0	0	0	1	1	7
4	0	0	0	1	0	0	1	9	36	1	0	0	1	0	0	8
5	0	0	0	1	0	1	1	11	37	1	0	0	1	0	1	10
6	0	0	0	1	1	0	1	13	38	1	0	0	1	1	0	12
7	0	0	0	1	1	1	1	15	39	1	0	0	1	1	1	14
8	0	0	1	0	0	0	0	16	40	1	0	1	0	0	0	16
9	0	0	1	0	0	1	0	18	41	1	0	1	0	0	1	18
10	0	0	1	0	1	0	0	20	42	1	0	1	0	1	0	20
11	0	0	1	0	1	1	0	22	43	1	0	1	0	1	1	22
12	0	0	1	1	0	0	1	25	44	1	0	1	1	0	0	24
13	0	0	1	1	0	1	1	27	45	1	0	1	1	0	1	26
14	0	0	1	1	1	0	1	29	46	1	0	1	1	1	0	28
15	0	0	1	1	1	1	1	31	47	1	0	1	1	1	1	30
16	0	1	0	0	0	0	0	32	48	1	1	0	0	0	0	33
17	0	1	0	0	0	1	0	34	49	1	1	0	0	0	1	35
18	0	1	0	0	1	0	0	36	50	1	1	0	0	1	0	37
19	0	1	0	0	1	1	0	38	51	1	1	0	0	1	1	38
20	0	1	0	1	0	0	0	40	52	1	1	0	1	0	0	41
21	0	1	0	1	0	1	0	42	53	1	1	0	1	0	1	43
22	0	1	0	1	1	0	0	44	54	1	1	0	1	1	0	44
23	0	1	0	1	1	1	0	46	55	1	1	0	1	1	1	46
24	0	1	1	0	0	0	0	48	56	1	1	1	0	0	0	49
25	0	1	1	0	0	1	0	50	57	1	1	1	0	0	1	51
26	0	1	1	0	1	0	0	52	58	1	1	1	0	1	0	52
27	0	1	1	0	1	1	0	54	59	1	1	1	0	1	1	54
28	0	1	1	1	0	0	0	56	60	1	1	1	1	0	0	57
29	0	1	1	1	0	1	0	58	61	1	1	1	1	0	1	59
30	0	1	1	1	0	0	0	60	62	1	1	1	1	1	0	60
31	0	1	1	1	0	1	0	62	63	1	1	1	1	1	1	62

SUCCESSOR TABLE



STATE DIAGRAM:

N=20



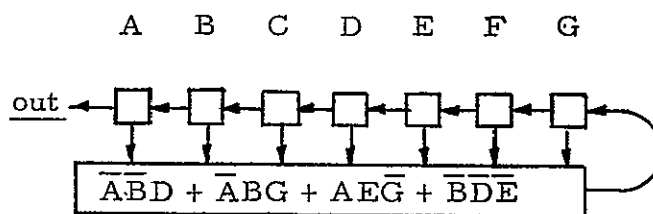
STATE DIAGRAM

SEQUENCE: 111011101001011000000

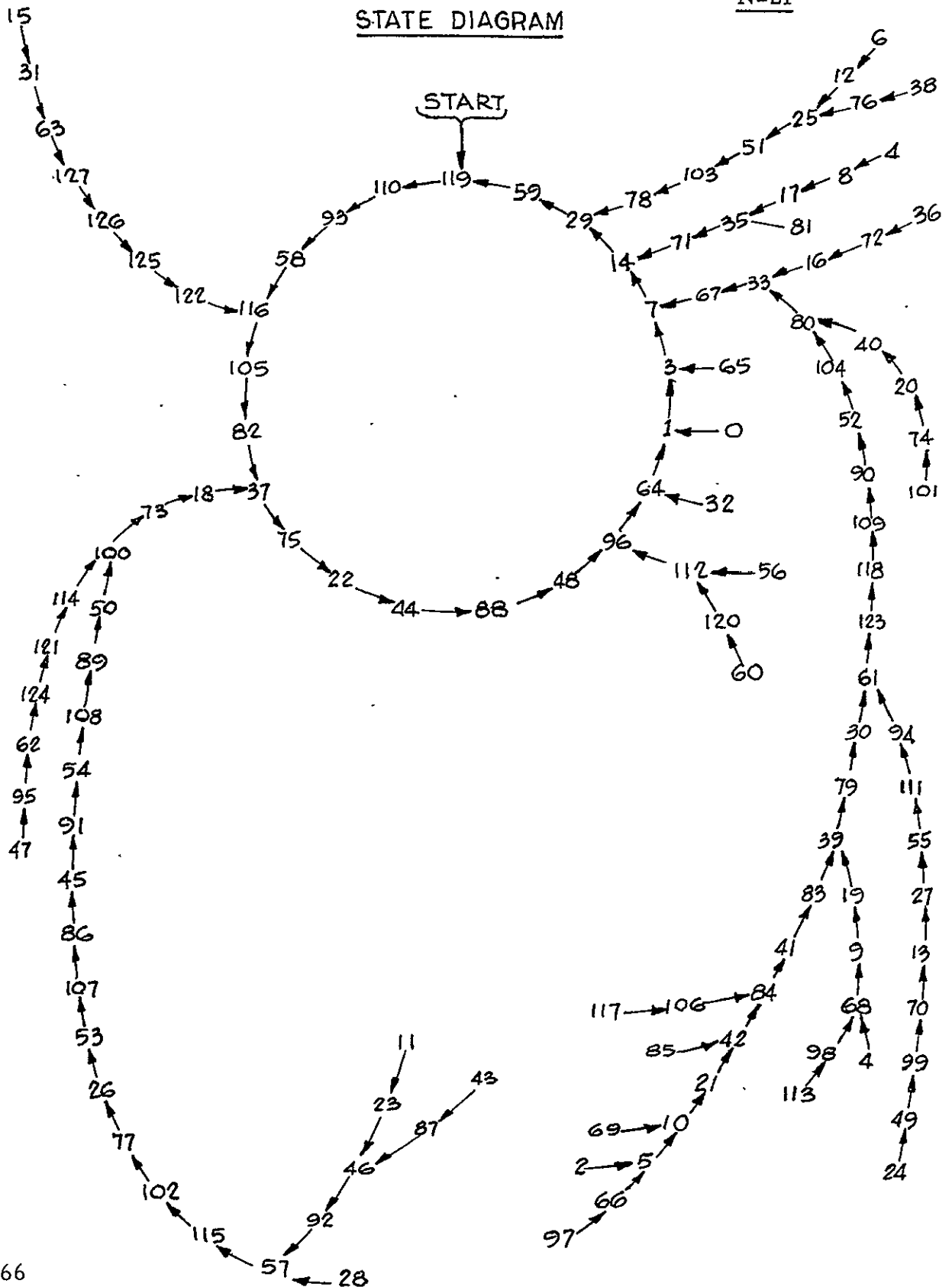
SPAN: 7

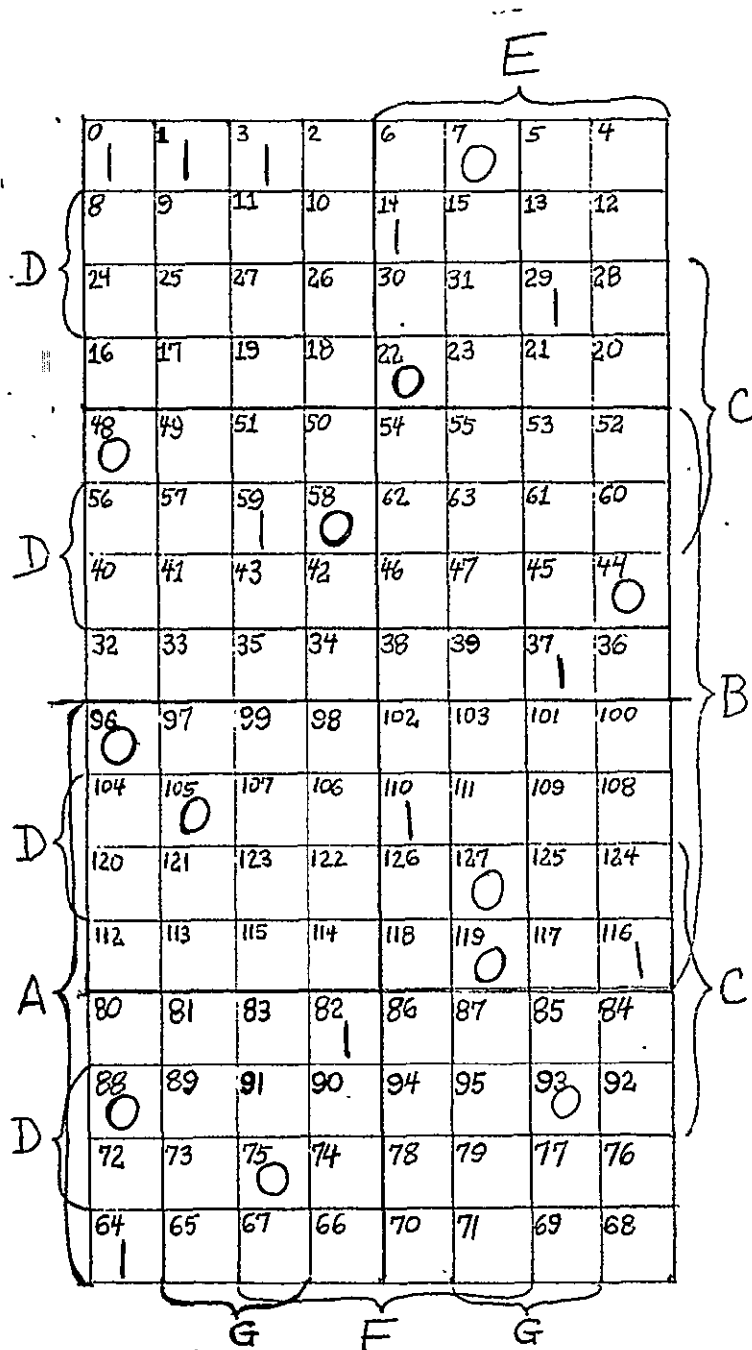
TRUTH TABLE

	A	B	C	D	E	F	G	f
119	1	1	1	0	1	1	1	0
110	1	1	0	1	1	1	0	1
93	1	0	1	1	1	0	1	0
58	0	1	1	1	0	1	0	0
116	1	1	1	0	1	0	0	1
105	1	1	0	1	0	0	1	0
82	1	0	1	0	0	1	0	1
37	0	1	0	0	1	0	1	1
75	1	0	0	1	0	1	1	0
22	0	0	1	0	1	1	0	0
44	0	1	0	1	1	0	0	0
88	1	0	1	1	0	0	0	0
48	0	1	1	0	0	0	0	0
96	1	1	0	0	0	0	0	0
64	1	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	1
3	0	0	0	0	0	1	1	1
7	0	0	0	0	1	1	1	0
14	0	0	0	1	1	1	0	1
29	0	0	1	1	1	0	1	1
59	0	1	1	1	0	1	1	1

SHIFT REGISTER

N=21





Karnaugh Chart

N=21

ABCDEFGF							f	ABCDEFGF							f
0	0000000	1	1					64	1000000	1	1				
1	0000001	1	3					65	1000001	1	3				
2	0000010	1	5					66	1000010	1	5				
3	0000011	1	7					67	1000011	1	7				
4	0000100	0	8					68	1000100	1	9				
5	0000101	0	10					69	1000101	0	10				
6	0000110	0	12					70	1000110	1	13				
7	0000111	0	14					71	1000111	0	14				
8	0001000	1	17					72	1001000	0	16				
9	0001001	1	19					73	1001001	0	18				
10	0001010	1	21					74	1001010	0	20				
11	0001011	1	23					75	1001011	0	22				
12	0001100	1	25					76	1001100	1	25				
13	0001101	1	27					77	1001101	0	26				
14	0001110	1	29					78	1001110	1	29				
15	0001111	1	31					79	1001111	0	30				
16	0010000	1	33					80	1010000	1	33				
17	0010001	1	35					81	1010001	1	35				
18	0010010	1	37					82	1010010	1	37				
19	0010011	1	39					83	1010011	1	39				
20	0010100	0	40					84	1010100	1	41				
21	0010101	0	42					85	1010101	0	42				
22	0010110	0	44					86	1010110	1	45				
23	0010111	0	46					87	1010111	0	46				
24	0011000	1	49					88	1011000	0	48				
25	0011001	1	51					89	1011001	0	50				
26	0011010	1	53					90	1011010	0	52				
27	0011011	1	55					91	1011011	0	54				
28	0011100	1	57					92	1011100	1	57				
29	0011101	1	59					93	1011101	0	58				
30	0011110	1	61					94	1011110	1	61				
31	0011111	1	63					95	1011111	0	62				
32	0100000	0	64					96	1100000	0	64				
33	0100001	1	67					97	1100001	0	66				
34	0100010	0	68					98	1100010	0	68				
35	0100011	1	71					99	1100011	0	70				
36	0100100	0	72					100	1100100	1	73				
37	0100101	1	75					101	1100101	0	74				
38	0100110	0	76					102	1100110	1	77				
39	0100111	1	79					103	1100111	0	78				
40	0101000	0	80					104	1101000	0	80				
41	0101001	1	83					105	1101001	0	82				
42	0101010	0	84					106	1101010	0	84				
43	0101011	1	87					107	1101011	0	86				
44	0101100	0	88					108	1101100	1	89				
45	0101101	1	91					109	1101101	0	90				
46	0101110	0	92					110	1101110	1	93				
47	0101111	1	95					111	1101111	0	94				
48	0110000	0	96					112	1110000	0	96				
49	0110001	1	99					113	1110001	0	98				
50	0110010	0	100					114	1110010	0	100				
51	0110011	1	103					115	1110011	0	102				
52	0110100	0	104					116	1110100	1	105				
53	0110101	1	107					117	1110101	0	106				
54	0110110	0	108					118	1110110	1	109				
55	0110111	1	111					119	1110111	0	110				
56	0111000	0	112					120	1111000	0	112				
57	0111001	1	115					121	1111001	0	114				
58	0111010	0	116					122	1111010	0	116				
59	0111011	1	119					123	1111011	0	118				
60	0111100	0	120					124	1111100	1	121				
61	0111101	1	123					125	1111101	0	122				
62	0111110	0	124					126	1111110	1	125				
63	0111111	1	127					127	1111111	0	126				

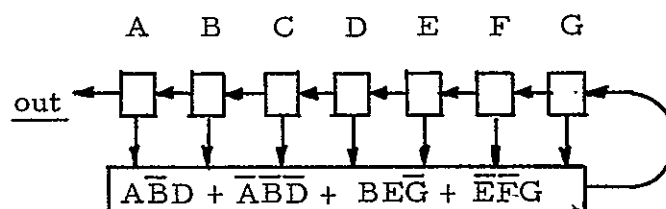
Successor Table

N=22

SEQUENCE: 1111001101101010000000

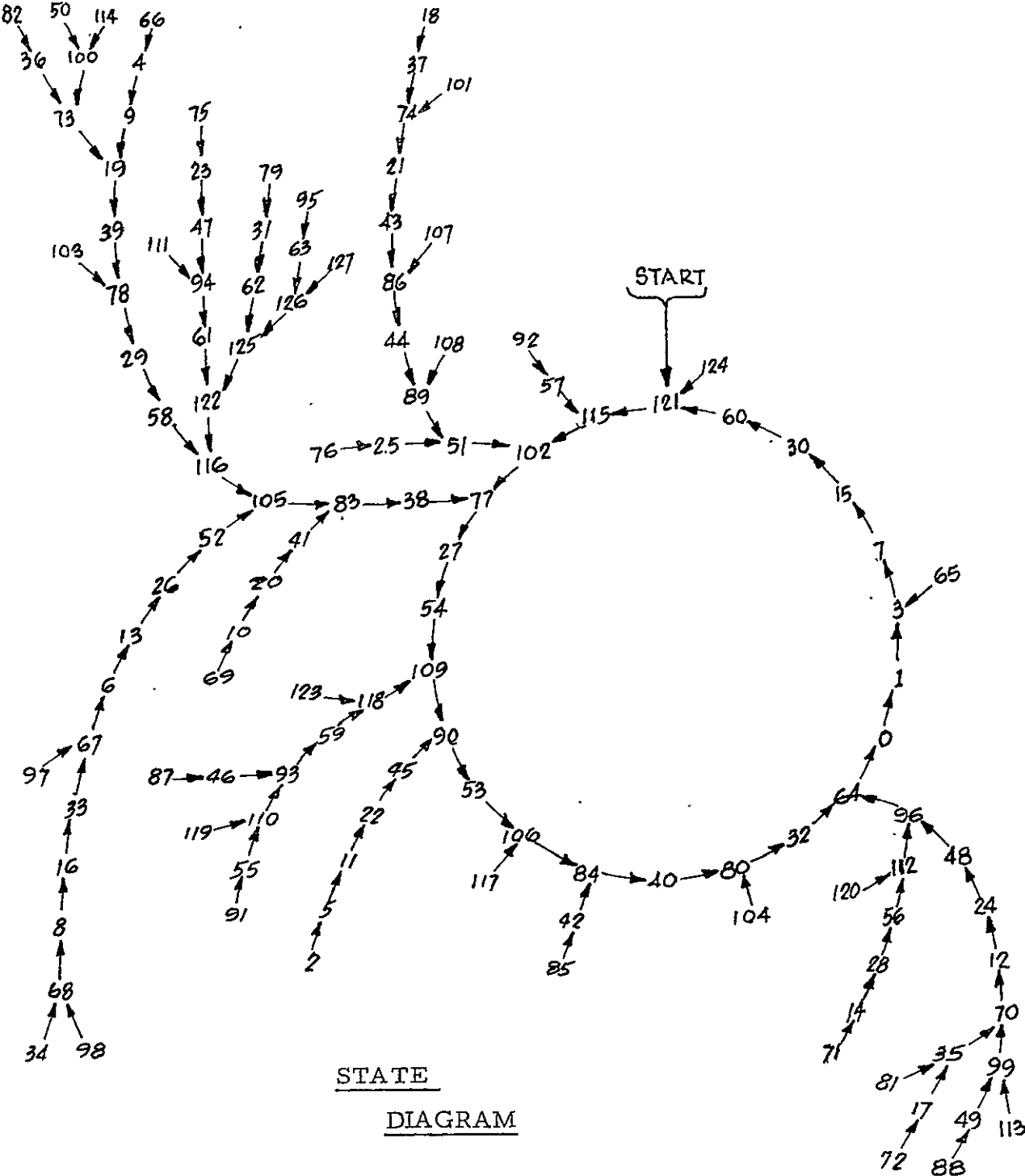
SPAN: 7

TRUTH TABLE							
	A	B	C	D	E	F	G
121	1	1	1	1	0	0	1
115	1	1	1	0	0	1	1
102	1	1	0	0	1	1	0
77	1	0	0	1	1	0	1
27	0	0	1	1	0	1	1
54	0	1	1	0	1	1	0
109	1	1	0	1	1	0	1
90	1	0	1	1	0	1	0
53	0	1	1	0	1	0	1
106	1	1	0	1	0	1	0
84	1	0	1	0	1	0	0
40	0	1	0	1	0	0	0
80	1	0	1	0	0	0	0
32	0	1	0	0	0	0	0
64	1	0	0	0	0	0	0
0	0	0	0	0	0	0	0
1	0	0	0	0	0	0	1
3	0	0	0	0	0	1	1
7	0	0	0	0	1	1	1
15	0	0	0	1	1	1	1
30	0	0	1	1	1	1	0
60	0	1	1	1	1	0	0



SHIFT REGISTER

N=22



N=22

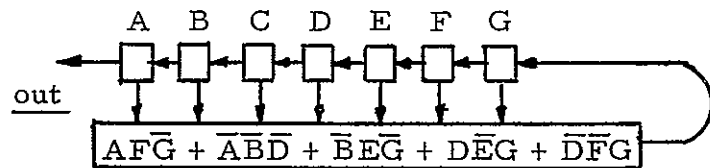
ABCDEFg	f	ABCDEFg	f
0	0000000	1	1
1	0000001	1	3
2	0000010	1	5
3	0000011	1	7
4	0000100	1	9
5	0000101	1	11
6	0000110	1	13
7	0000111	1	15
8	0001000	0	16
9	0001001	1	19
10	0001010	0	20
11	0001011	0	22
12	0001100	0	24
13	0001101	0	26
14	0001110	0	28
15	0001111	0	30
16	0010000	1	33
17	0010001	1	35
18	0010010	1	37
19	0010011	1	39
20	0010100	1	41
21	0010101	1	43
22	0010110	1	45
23	0010111	1	47
24	0011000	0	48
25	0011001	1	51
26	0011010	0	52
27	0011011	0	54
28	0011100	0	56
29	0011101	0	58
30	0011110	0	60
31	0011111	0	62
32	0100000	0	64
33	0100001	1	67
34	0100010	0	68
35	0100011	0	70
36	0100100	1	73
37	0100101	0	74
38	0100110	1	77
39	0100111	0	78
40	0101000	0	80
41	0101001	1	83
42	0101010	0	84
43	0101011	0	86
44	0101100	1	89
45	0101101	0	90
46	0101110	1	93
47	0101111	0	94
48	0110000	0	96
49	0110001	1	99
50	0110010	0	100
51	0110011	0	102
52	0110100	1	105
53	0110101	0	106
54	0110110	1	109
55	0110111	0	110
56	0111000	0	112
57	0111001	1	115
58	0111010	0	116
59	0111011	0	118
60	0111100	1	121
61	0111101	0	122
62	0111110	1	125
63	0111111	0	126
64	1000000	0	0
65	1000001	1	3
66	1000010	0	4
67	1000011	0	6
68	1000100	0	8
69	1000101	0	10
70	1000110	0	12
71	1000111	0	14
72	1001000	1	17
73	1001001	1	19
74	1001010	1	21
75	1001011	1	23
76	1001100	1	25
77	1001101	1	27
78	1001110	1	29
79	1001111	1	31
80	1010000	0	32
81	1010001	1	35
82	1010010	0	36
83	1010011	0	38
84	1010100	0	40
85	1010101	0	42
86	1010110	0	44
87	1010111	0	46
88	1011000	1	49
89	1011001	1	51
90	1011010	1	53
91	1011011	1	55
92	1011100	1	57
93	1011101	1	59
94	1011110	1	61
95	1011111	1	63
96	1100000	0	64
97	1100001	1	67
98	1100010	0	68
99	1100011	0	70
100	1100100	1	73
101	1100101	0	74
102	1100110	1	77
103	1100111	0	78
104	1101000	0	80
105	1101001	1	83
106	1101010	0	84
107	1101011	0	86
108	1101100	1	89
109	1101101	0	90
110	1101110	1	93
111	1101111	0	94
112	1110000	0	96
113	1110001	1	99
114	1110010	0	100
115	1110011	0	102
116	1110100	1	105
117	1110101	0	106
118	1110110	1	109
119	1110111	0	110
120	1111000	0	112
121	1111001	1	115
122	1111010	0	116
123	1111011	0	118
124	1111100	1	121
125	1111101	0	122
126	1111110	1	125
127	1111111	0	126

Successor Table

SEQUENCE: 11110101110011010000000

SPAN: 7

TRUTH TABLE								
	A	B	C	D	E	F	G	f
122	1	1	1	1	0	1	0	1
117	1	1	1	0	1	0	1	1
107	1	1	0	1	0	1	1	1
87	1	0	1	0	1	1	1	0
46	0	1	0	1	1	1	0	0
92	1	0	1	1	1	0	0	1
57	0	1	1	1	0	0	1	1
115	1	1	1	0	0	1	1	0
102	1	1	0	0	1	1	0	1
77	1	0	0	1	1	0	1	0
26	0	0	1	1	0	1	0	0
52	0	1	1	0	1	0	0	0
104	1	1	0	1	0	0	0	0
80	1	0	1	0	0	0	0	0
32	0	1	0	0	0	0	0	0
64	1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	1
3	0	0	0	0	0	1	1	1
7	0	0	0	0	1	1	1	1
15	0	0	0	1	1	1	1	0
30	0	0	1	1	1	1	0	1
61	0	1	1	1	1	0	1	0



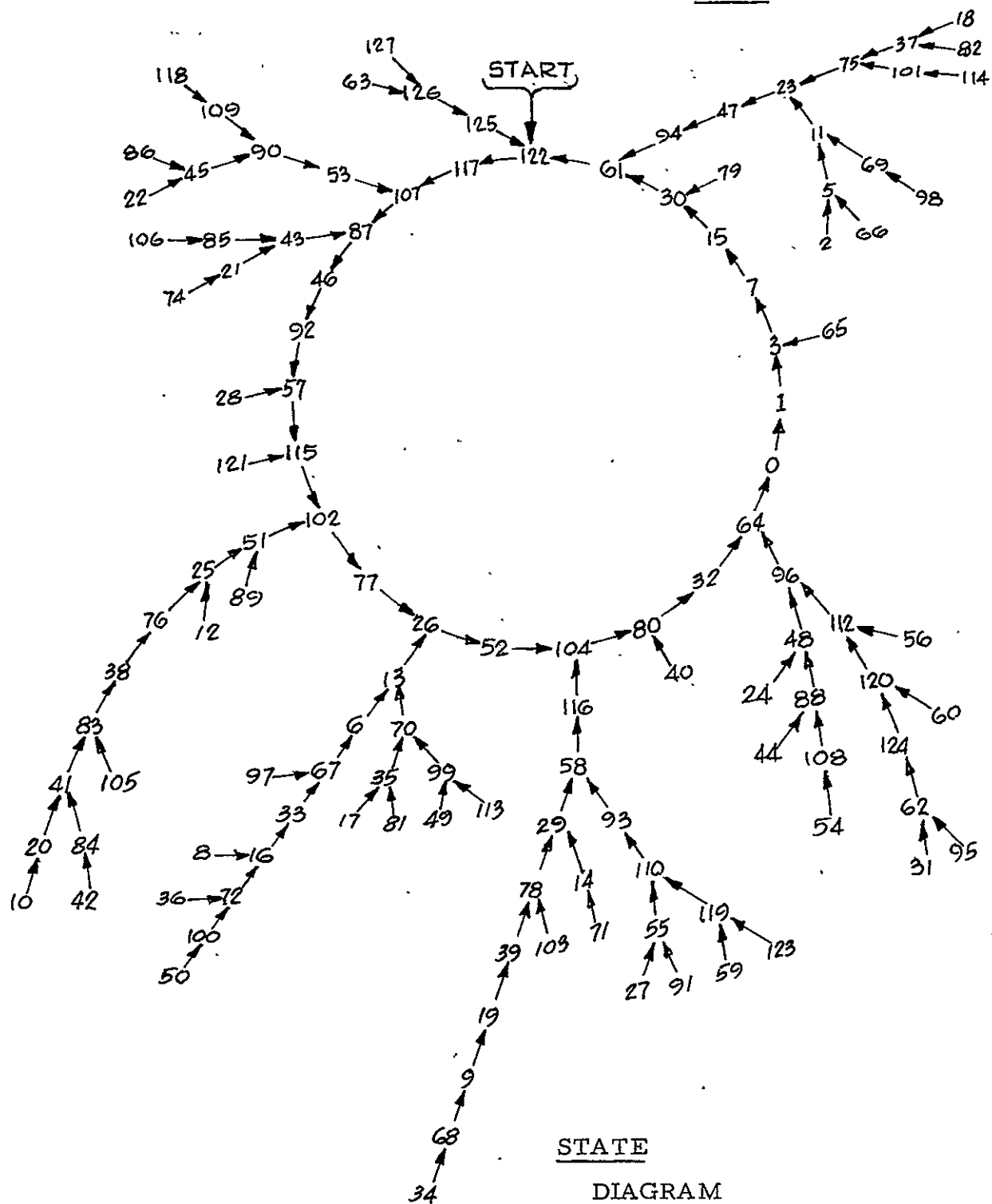
SHIFT REGISTER

N=23

								E	
D	0	1	3	2	6	7	5	4	
	1	1	1			1			
	8	9	11	10	14	15	13	12	
						0			
D	24	25	27	26	30	31	29	28	
				0	1				
	16	17	19	18	22	23	21	20	
D	48	49	51	50	54	55	53	52	
								0	
	56	57	59	58	62	63	61	60	
		1					0		
D	40	41	43	42	46	47	45	44	
					0				
	32	33	35	34	38	39	37	36	
	0								
D	96	97	99	98	102	103	101	100	
					1				
	104	105	107	106	110	111	109	108	
	0		1						
A	120	121	123	122	126	127	125	124	
				1		0			
	112	113	115	114	118	119	117	116	
			0				1		
D	80	81	83	82	86	87	85	84	
	0					0			
	88	89	91	90	94	95	93	92	
								1	
D	72	73	75	74	78	79	77	76	
							0		
D	64	65	67	66	70	71	69	68	
	0								
G				F		G			

KARNAUGH CHART

N=23



N=23

ABCDEF	g		ABCDEF	g	
0	0000000	1	64	1000000	0
1	0000001	3	65	1000001	3
2	0000010	5	66	1000010	5
3	0000011	7	67	1000011	6
4	0000100	9	68	1000100	9
5	0000101	11	69	1000101	11
6	0000110	13	70	1000110	13
7	0000111	15	71	1000111	14
8	0001000	16	72	1001000	16
9	0001001	19	73	1001001	19
10	0001010	21	74	1001010	21
11	0001011	23	75	1001011	23
12	0001100	25	76	1001100	25
13	0001101	26	77	1001101	26
14	0001110	29	78	1001110	29
15	0001111	30	79	1001111	30
16	0010000	33	80	1010000	32
17	0010001	35	81	1010001	35
18	0010010	37	82	1010010	37
19	0010011	39	83	1010011	38
20	0010100	41	84	1010100	41
21	0010101	43	85	1010101	43
22	0010110	45	86	1010110	45
23	0010111	47	87	1010111	46
24	0011000	48	88	1011000	48
25	0011001	51	89	1011001	51
26	0011010	52	90	1011010	53
27	0011011	55	91	1011011	55
28	0011100	57	92	1011100	57
29	0011101	58	93	1011101	58
30	0011110	61	94	1011110	61
31	0011111	62	95	1011111	62
32	0100000	64	96	1100000	64
33	0100001	67	97	1100001	67
34	0100010	68	98	1100010	67
35	0100011	70	99	1100011	70
36	0100100	72	100	1100100	72
37	0100101	75	101	1100101	75
38	0100110	76	102	1100110	77
39	0100111	78	103	1100111	78
40	0101000	80	104	1101000	80
41	0101001	83	105	1101001	83
42	0101010	84	106	1101010	85
43	0101011	87	107	1101011	87
44	0101100	88	108	1101100	88
45	0101101	90	109	1101101	90
46	0101110	92	110	1101110	93
47	0101111	94	111	1101111	94
48	0110000	96	112	1110000	96
49	0110001	99	113	1110001	99
50	0110010	100	114	1110010	101
51	0110011	102	115	1110011	102
52	0110100	104	116	1110100	104
53	0110101	107	117	1110101	107
54	0110110	108	118	1110110	109
55	0110111	110	119	1110111	110
56	0111000	112	120	1111000	112
57	0111001	115	121	1111001	115
58	0111010	116	122	1111010	117
59	0111011	119	123	1111011	119
60	0111100	120	124	1111100	120
61	0111101	122	125	1111101	122
62	0111110	124	126	1111110	125
63	0111111	126	127	1111111	126

Successor Table

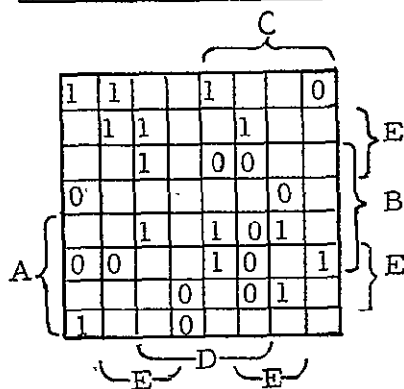
SEQUENCE:

11111010111001100100000

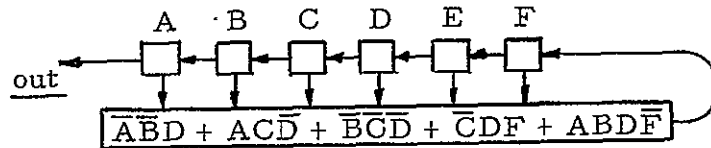
SPAN:

6

	A	B	C	D	E	F	f
62	1	1	1	1	1	0	1
61	1	1	1	1	0	1	0
58	1	1	1	0	1	0	1
53	1	1	0	1	0	1	1
43	1	0	1	0	1	1	1
23	0	1	0	1	1	1	1
47	1	0	1	1	1	1	0
30	0	1	1	1	1	0	0
60	1	1	1	1	0	0	1
57	1	1	1	0	0	1	1
51	1	1	0	0	1	1	0
38	1	0	0	1	1	0	0
12	0	0	1	1	0	0	1
25	0	1	1	0	0	1	0
50	1	1	0	0	1	0	0
36	1	0	0	1	0	0	0
8	0	0	1	0	0	0	0
16	0	1	0	0	0	0	0
32	1	0	0	0	0	0	1
1	0	0	0	0	0	1	1
3	0	0	0	0	1	1	1
7	0	0	0	1	1	1	1
15	0	0	1	1	1	1	1
31	0	1	1	1	1	1	0



KARNAUGH CHART



SHIFT REGISTER

	A	B	C	D	E	F	f		A	B	C	D	E	F	f	
0	0	0	0	0	0	0	1	1	32	1	0	0	0	0	0	1
1	0	0	0	0	0	1	1	3	33	1	0	0	0	0	1	3
2	0	0	0	0	1	0	1	5	34	1	0	0	0	1	0	5
3	0	0	0	0	1	1	1	7	35	1	0	0	0	1	1	7
4	0	0	0	1	0	0	1	9	36	1	0	0	1	0	0	8
5	0	0	0	1	0	1	1	11	37	1	0	0	1	0	1	11
6	0	0	0	1	1	0	1	13	38	1	0	0	1	1	0	12
7	0	0	0	1	1	1	1	15	39	1	0	0	1	1	1	15
8	0	0	1	0	0	0	0	16	40	1	0	1	0	0	0	17
9	0	0	1	0	0	1	0	18	41	1	0	1	0	0	1	19
10	0	0	1	0	1	0	0	20	42	1	0	1	0	1	0	21
11	0	0	1	0	1	1	0	22	43	1	0	1	0	1	1	23
12	0	0	1	1	0	0	1	25	44	1	0	1	1	0	0	24
13	0	0	1	1	0	1	1	27	45	1	0	1	1	0	1	26
14	0	0	1	1	1	0	1	29	46	1	0	1	1	1	0	28
15	0	0	1	1	1	1	1	31	47	1	0	1	1	1	1	30
16	0	1	0	0	0	0	0	32	48	1	1	0	0	0	0	32
17	0	1	0	0	0	1	0	34	49	1	1	0	0	0	1	34
18	0	1	0	0	1	0	0	36	50	1	1	0	0	1	0	36
19	0	1	0	0	1	1	0	38	51	1	1	0	0	1	1	38
20	0	1	0	1	0	0	0	40	52	1	1	0	1	0	0	41
21	0	1	0	1	0	1	1	43	53	1	1	0	1	0	1	43
22	0	1	0	1	1	0	0	44	54	1	1	0	1	1	0	45
23	0	1	0	1	1	1	1	47	55	1	1	0	1	1	1	47
24	0	1	1	0	0	0	0	48	56	1	1	1	0	0	0	49
25	0	1	1	0	0	1	0	50	57	1	1	1	0	0	1	51
26	0	1	1	0	1	0	0	52	58	1	1	1	0	1	0	53
27	0	1	1	0	1	1	0	54	59	1	1	1	0	1	1	55
28	0	1	1	1	0	0	0	56	60	1	1	1	1	0	0	57
29	0	1	1	1	0	1	0	58	61	1	1	1	1	0	1	58
30	0	1	1	1	1	0	0	60	62	1	1	1	1	1	0	61
31	0	1	1	1	1	1	0	62	63	1	1	1	1	1	1	62

SUCCESSOR TABLE

N=24



SEQUENCE:

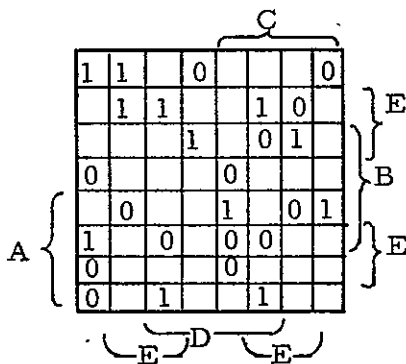
1111100101101110001000000

SPAN:

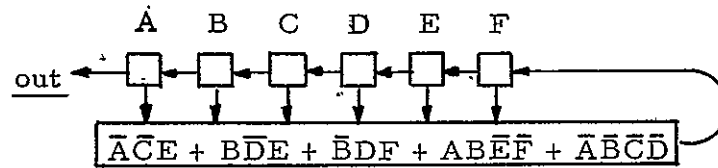
6

TRUTH TABLE

	A	B	C	D	E	F	f
62	1	1	1	1	1	0	0
60	1	1	1	1	0	0	1
57	1	1	1	0	0	1	0
50	1	1	0	0	1	0	1
37	1	0	0	1	0	1	1
11	0	0	1	0	1	1	0
22	0	1	0	1	1	0	1
45	1	0	1	1	0	1	1
27	0	1	1	0	1	1	1
55	1	1	0	1	1	1	0
46	1	0	1	1	1	0	0
28	0	1	1	1	0	0	0
56	1	1	1	0	0	0	1
49	1	1	0	0	0	1	0
34	1	0	0	0	1	0	0
4	0	0	0	1	0	0	0
8	0	0	1	0	0	0	0
16	0	1	0	0	0	0	0
32	1	0	0	0	0	0	0
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	1
3	0	0	0	0	1	1	1
7	0	0	0	1	1	1	1
15	0	0	1	1	1	1	1
31	0	1	1	1	1	1	0



KARNAUGH CHART

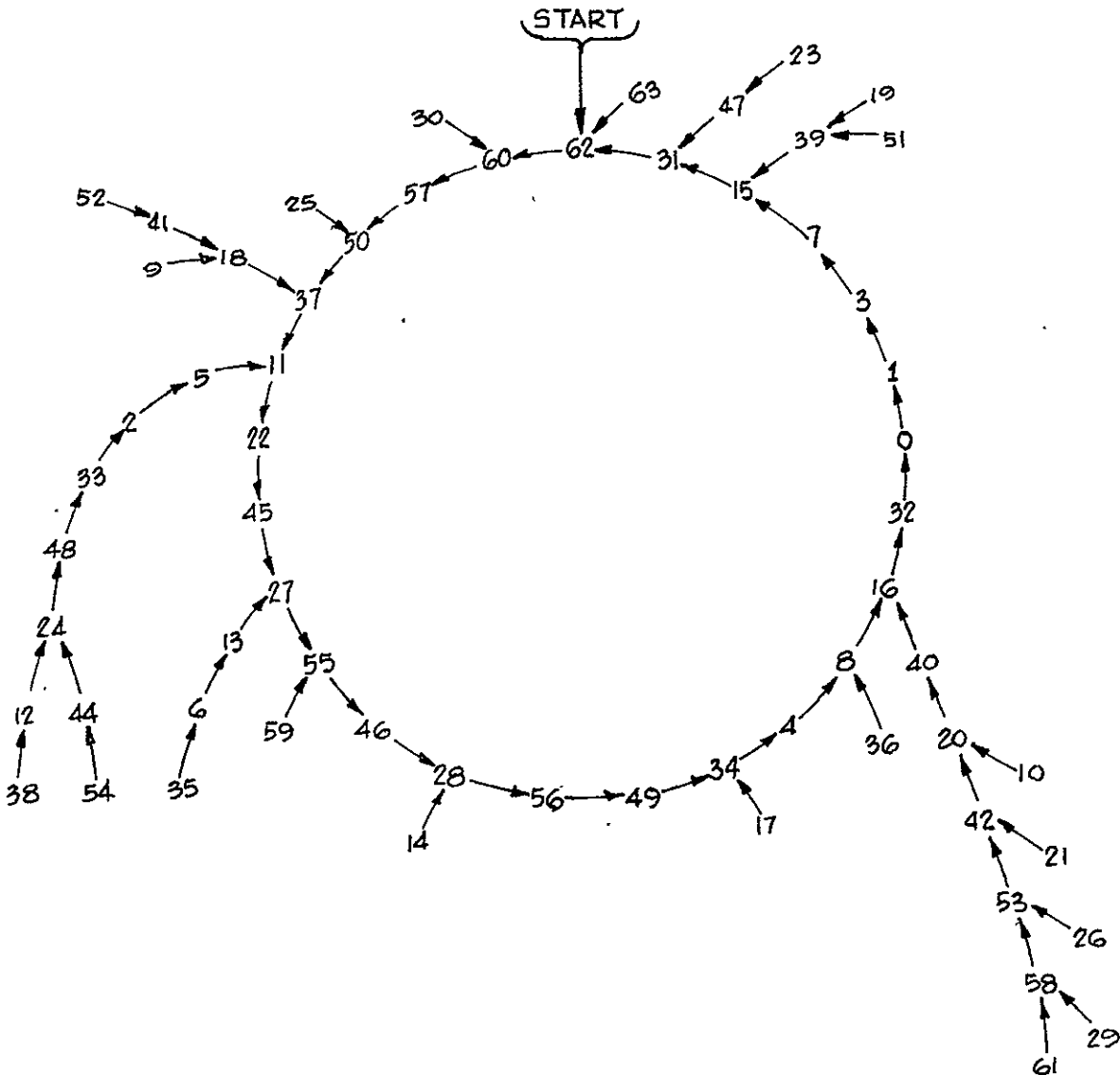


SHIFT REGISTER

	A	B	C	D	E	F	f			A	B	C	D	E	F	f	
0	0	0	0	0	0	0	1	1	32	1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	3	33	1	0	0	0	0	1	0	2
2	0	0	0	0	1	0	1	5	34	1	0	0	0	1	0	0	4
3	0	0	0	0	1	1	1	7	35	1	0	0	0	1	1	0	6
4	0	0	0	1	0	0	0	8	36	1	0	0	1	0	0	0	8
5	0	0	0	1	0	1	1	11	37	1	0	0	1	0	1	1	11
6	0	0	0	1	1	0	1	13	38	1	0	0	1	1	0	0	12
7	0	0	0	1	1	1	1	15	39	1	0	0	1	1	1	1	15
8	0	0	1	0	0	0	0	16	40	1	0	1	0	0	0	0	16
9	0	0	1	0	0	1	0	18	41	1	0	1	0	0	1	0	18
10	0	0	1	0	1	0	0	20	42	1	0	1	0	1	0	0	20
11	0	0	1	0	1	1	0	22	43	1	0	1	0	1	1	0	22
12	0	0	1	1	0	0	0	24	44	1	0	1	1	0	0	0	24
13	0	0	1	1	0	1	1	27	45	1	0	1	1	0	1	1	27
14	0	0	1	1	1	0	0	28	46	1	0	1	1	1	0	0	28
15	0	0	1	1	1	1	1	31	47	1	0	1	1	1	1	1	31
16	0	1	0	0	0	0	0	32	48	1	1	0	0	0	0	1	33
17	0	1	0	0	0	1	0	34	49	1	1	0	0	0	1	0	34
18	0	1	0	0	1	0	1	37	50	1	1	0	0	1	0	1	37
19	0	1	0	0	1	1	1	39	51	1	1	0	0	1	1	1	39
20	0	1	0	1	0	0	0	40	52	1	1	0	1	0	0	1	41
21	0	1	0	1	0	1	0	42	53	1	1	0	1	0	1	0	42
22	0	1	0	1	1	0	1	45	54	1	1	0	1	1	0	0	44
23	0	1	0	1	1	1	1	47	55	1	1	0	1	1	1	0	46
24	0	1	1	0	0	0	0	48	56	1	1	1	0	0	0	1	49
25	0	1	1	0	0	1	0	50	57	1	1	1	0	0	1	0	50
26	0	1	1	0	1	0	1	53	58	1	1	1	0	1	0	1	53
27	0	1	1	0	1	1	1	55	59	1	1	1	0	1	1	1	55
28	0	1	1	1	0	0	0	56	60	1	1	1	1	0	0	1	57
29	0	1	1	1	0	1	0	58	61	1	1	1	1	0	1	0	58
30	0	1	1	1	1	0	0	60	62	1	1	1	1	1	0	0	60
31	0	1	1	1	1	1	0	62	63	1	1	1	1	1	1	0	62

SUCCESSOR TABLE

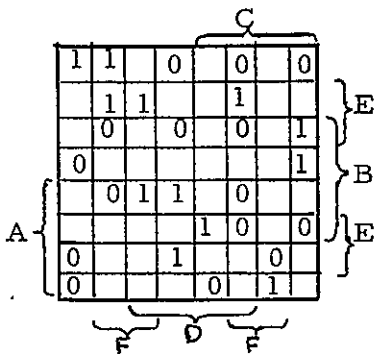
N=25



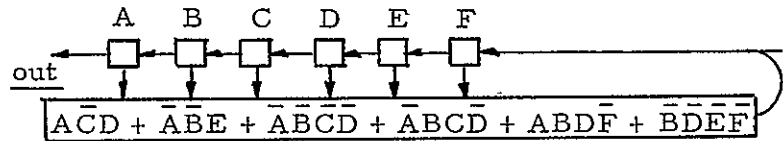
STATE DIAGRAM

SPAN: 6

	A	B	C	D	E	F	f
62	1	1	1	1	1	0	1
61	1	1	1	1	0	1	0
58	1	1	1	0	1	0	0
52	1	1	0	1	0	0	1
41	1	0	1	0	0	1	1
19	0	1	0	0	1	1	0
38	1	0	0	1	1	0	1
13	0	0	1	1	0	1	0
26	0	1	1	0	1	0	1
53	1	1	0	1	0	1	1
43	1	0	1	0	1	1	0
22	0	1	0	1	1	0	0
44	1	0	1	1	0	0	0
24	0	1	1	0	0	0	1
49	1	1	0	0	0	1	0
34	1	0	0	0	1	0	0
4	0	0	0	1	0	0	0
8	0	0	1	0	0	0	0
16	0	1	0	0	0	0	0
32	1	0	0	0	0	0	0
0	0	0	0	0	0	0	1
1	0	0	0	0	0	1	1
3	0	0	0	0	1	1	1
7	0	0	0	1	1	1	1
15	0	0	1	1	1	1	1
31	0	1	1	1	1	1	0



KARNAUGH CHART

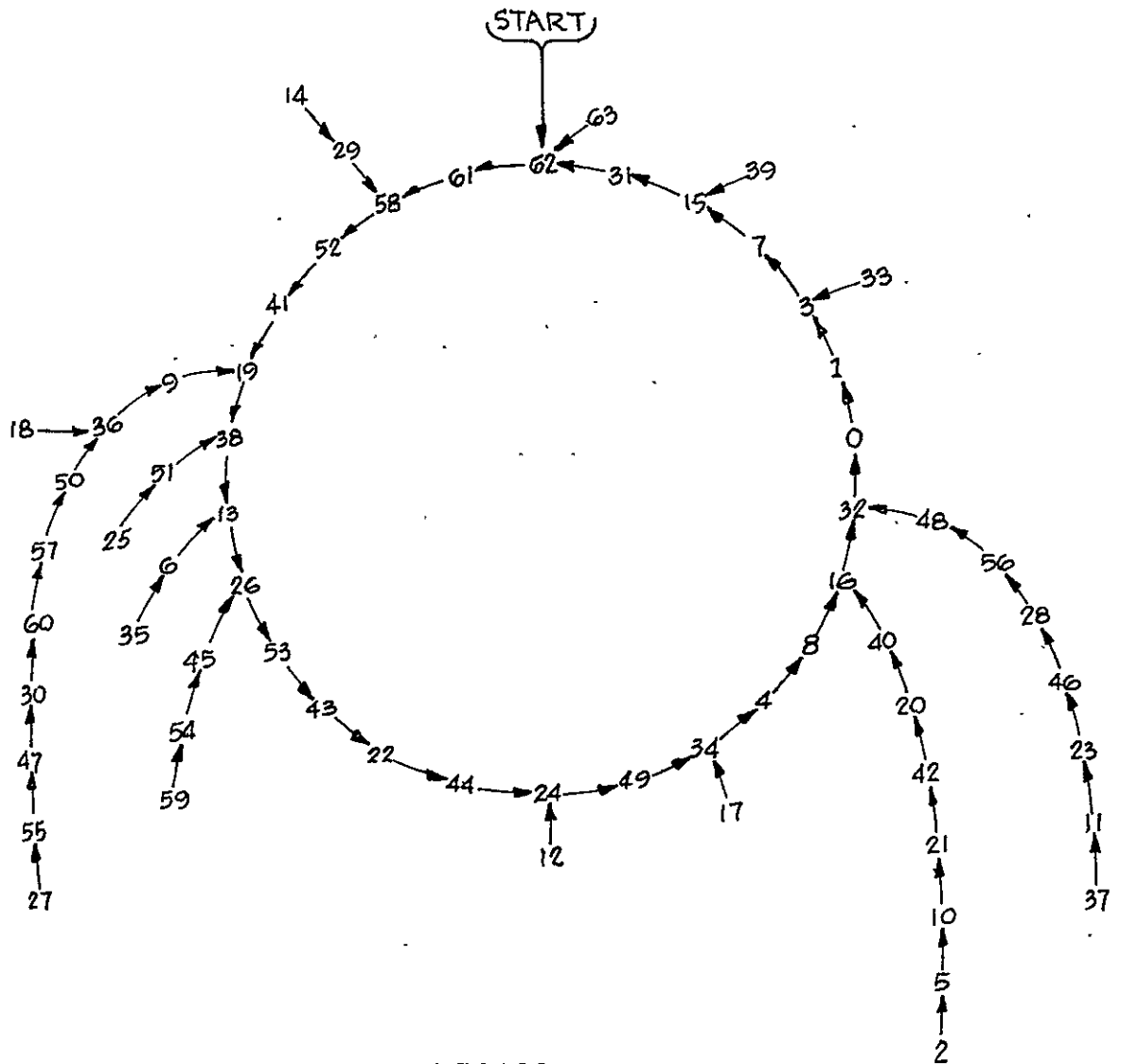


SHIFT REGISTER

	A	B	C	D	E	F	f			A	B	C	D	E	F	f	
0	0	0	0	0	0	0	1	1	32	1	0	0	0	0	0	0	0
1	0	0	0	0	0	1	1	3	33	1	0	0	0	0	1	1	3
2	0	0	0	0	1	0	1	5	34	1	0	0	0	1	0	0	4
3	0	0	0	0	1	1	1	7	35	1	0	0	0	1	1	0	6
4	0	0	0	1	0	0	0	8	36	1	0	0	1	0	0	1	9
5	0	0	0	1	0	1	0	10	37	1	0	0	1	0	1	1	11
6	0	0	0	1	1	0	1	13	38	1	0	0	1	1	0	1	13
7	0	0	0	1	1	1	1	15	39	1	0	0	1	1	1	1	15
8	0	0	1	0	0	0	0	16	40	1	0	1	0	0	0	0	16
9	0	0	1	0	0	1	1	19	41	1	0	1	0	0	1	1	19
10	0	0	1	0	1	0	1	21	42	1	0	1	0	1	0	0	20
11	0	0	1	0	1	1	1	23	43	1	0	1	0	1	1	0	22
12	0	0	1	1	0	0	0	24	44	1	0	1	1	0	0	0	24
13	0	0	1	1	0	1	0	26	45	1	0	1	1	0	1	0	26
14	0	0	1	1	1	0	1	29	46	1	0	1	1	1	0	0	28
15	0	0	1	1	1	1	1	31	47	1	0	1	1	1	1	0	30
16	0	1	0	0	0	0	0	32	48	1	1	0	0	0	0	0	32
17	0	1	0	0	0	1	0	34	49	1	1	0	0	0	1	0	34
18	0	1	0	0	1	0	0	36	50	1	1	0	0	1	0	0	36
19	0	1	0	0	1	1	0	38	51	1	1	0	0	1	1	0	38
20	0	1	0	1	0	0	0	40	52	1	1	0	1	0	0	1	41
21	0	1	0	1	0	1	0	42	53	1	1	0	1	0	1	1	43
22	0	1	0	1	1	0	0	44	54	1	1	0	1	1	0	1	45
23	0	1	0	1	1	1	0	46	55	1	1	0	1	1	1	1	47
24	0	1	1	0	0	0	1	49	56	1	1	1	0	0	0	0	48
25	0	1	1	0	0	1	1	51	57	1	1	1	0	0	1	0	50
26	0	1	1	0	1	0	1	53	58	1	1	1	0	1	0	0	52
27	0	1	1	0	1	1	1	55	59	1	1	1	0	1	1	0	54
28	0	1	1	1	0	0	0	56	60	1	1	1	1	0	0	1	57
29	0	1	1	1	0	1	0	58	61	1	1	1	1	0	1	0	58
30	0	1	1	1	1	0	0	60	62	1	1	1	1	1	0	1	61
31	0	1	1	1	1	1	0	62	63	1	1	1	1	1	1	0	62

SUCCESSOR TABLE

N=26



STATE DIAGRAM

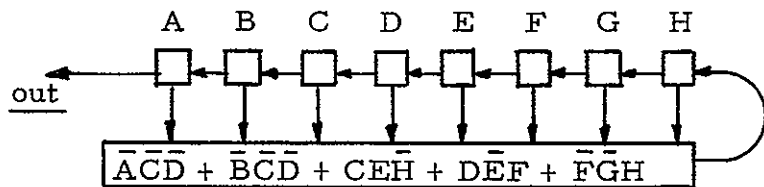
N=27

SEQUENCE: 111110101101001100110000000

SPAN: 8

TRUTH TABLE

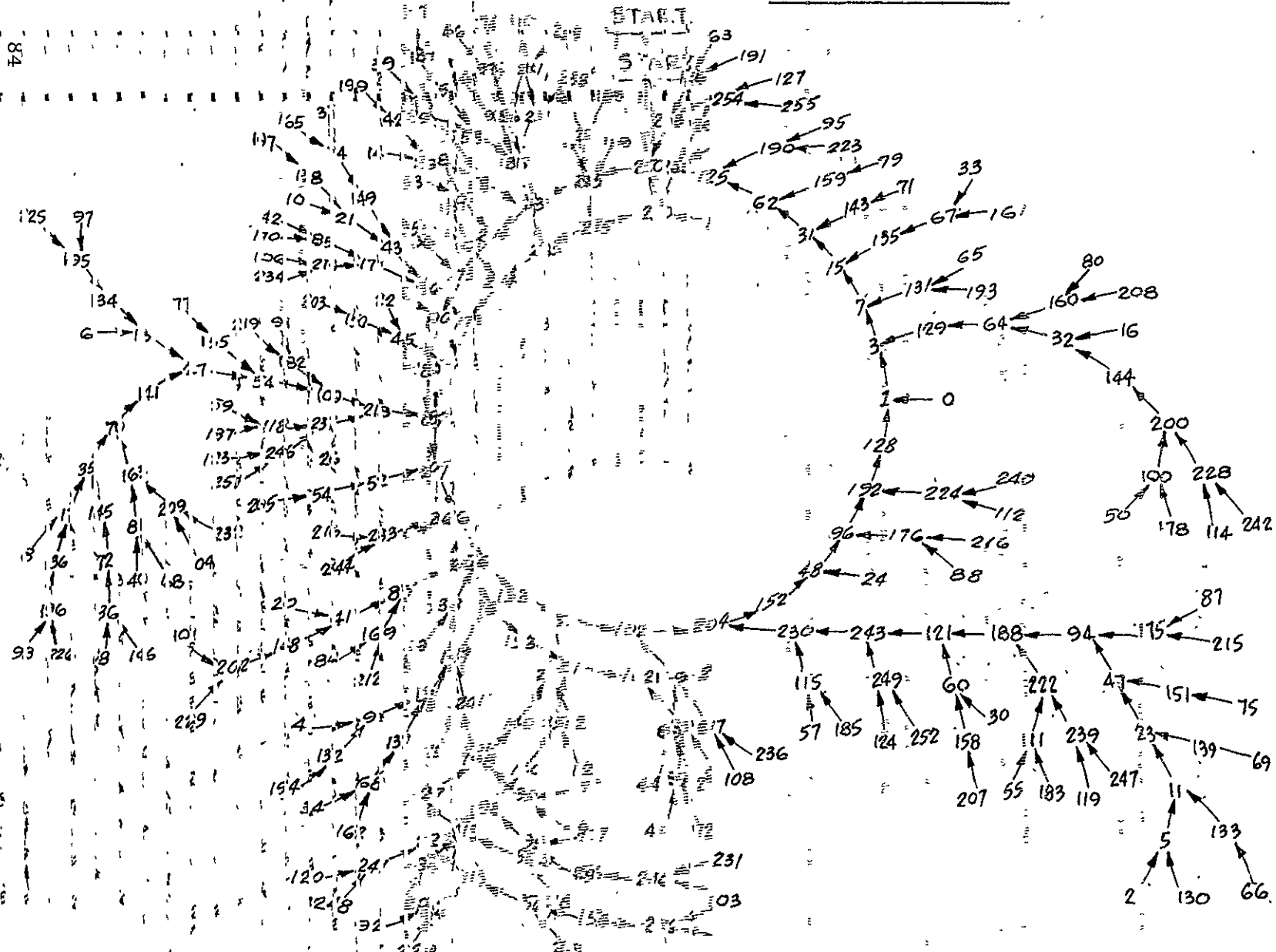
	A	B	C	D	E	F	G	H	f
250	1	1	1	1	1	0	1	0	1
245	1	1	1	1	0	1	0	1	1
235	1	1	1	0	1	0	1	1	0
214	1	1	0	1	0	1	1	0	1
173	1	0	1	0	1	1	0	1	0
90	0	1	0	1	1	0	1	0	0
180	1	0	1	1	0	1	0	0	1
105	0	1	1	0	1	0	0	1	1
211	1	1	0	1	0	0	1	1	0
166	1	0	1	0	0	1	1	0	0
76	0	1	0	0	1	1	0	0	1
153	1	0	0	1	1	0	0	1	1
51	0	0	1	1	0	0	1	1	0
102	0	1	1	0	0	1	1	0	0
204	1	1	0	0	1	1	0	0	0
152	1	0	0	1	1	0	0	0	0
48	0	0	1	1	0	0	0	0	0
96	0	1	1	0	0	0	0	0	0
192	1	1	0	0	0	0	0	0	0
128	1	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	0	1	1
3	0	0	0	0	0	0	1	1	1
7	0	0	0	0	0	1	1	1	1
15	0	0	0	0	1	1	1	1	1
31	0	0	0	1	1	1	1	1	0
62	0	0	1	1	1	1	1	0	1
125	0	1	1	1	1	1	0	1	0



SHIFT REGISTER

N=27

STATE DIAGRAM



H				H				H				E		H			
D	0	1	3	2	6	7	5	4	12	13	15	14	10	11	9	8	
	1	1	1			1					1						
	16	17	19	18	22	23	21	20	28	29	31	30	26	27	25	24	
	48	49	51	50	54	55	53	52	60	61	63	62	58	59	57	56	
	0		0									1					
D	32	33	35	34	38	39	37	36	44	45	47	46	42	43	41	40	
	96	97	99	98	102	103	101	100	108	109	111	110	106	107	105	104	
	0				0										1		
	112	113	115	114	118	119	117	116	124	125	127	126	122	123	121	120	
										0							
D	80	81	83	82	86	87	85	84	92	93	95	94	90	91	89	88	
	64	65	67	66	70	71	69	68	76	77	79	78	74	75	73	72	
									1								
	192	193	195	194	198	199	197	196	204	205	207	206	202	203	201	200	
	0								0								
D	208	209	211	210	214	215	213	212	220	221	223	222	218	219	217	216	
			0		1												
	240	241	243	242	246	247	245	244	252	253	255	254	250	251	249	248	
							1				0		1				
A	224	225	227	226	230	231	229	228	236	237	239	238	234	235	233	232	
														0			
	160	161	163	162	166	167	165	164	172	173	175	174	170	171	169	168	
					0					0							
D	176	177	179	178	182	183	181	180	188	189	191	190	186	187	185	184	
								1									
	144	145	147	146	150	151	149	148	156	157	159	158	154	155	153	152	
															1	0	
D	128	129	131	130	134	135	133	132	140	141	143	142	138	139	137	136	
	1																
G				F				G									

KARNAUGH CHART

$n=27$

	ABCDEFGH	f
0	00000000	1
1	00000001	3
2	00000010	5
3	00000011	7
4	00000100	9
5	00000101	11
6	00000110	13
7	00000111	15
8	00001000	17
9	00001001	19
10	00001010	21
11	00001011	23
12	00001100	25
13	00001101	27
14	00001110	29
15	00001111	31
16	00010000	32
17	00010001	35
18	00010010	36
19	00010011	38
20	00010100	41
21	00010101	43
22	00010110	45
23	00010111	47
24	00011000	48
25	00011001	51
26	00011010	52
27	00011011	54
28	00011100	56
29	00011101	58
30	00011110	60
31	00011111	62
32	00100000	64
33	00100001	67
34	00100010	68
35	00100011	70
36	00100100	72
37	00100101	74
38	00100110	76
39	00100111	78
40	00101000	81
41	00101001	83
42	00101010	85
43	00101011	86
44	00101100	89
45	00101101	90
46	00101110	93
47	00101111	94
48	00110000	96
49	00110001	99
50	00110010	100
51	00110011	102
52	00110100	105
53	00110101	107
54	00110110	109
55	00110111	111
56	00111000	113
57	00111001	115
58	00111010	117
59	00111011	118
60	00111100	121
61	00111101	122
62	00111110	125
63	00111111	126

Successor Table

	ABCDEFGH	f
64	01000000	129
65	01000001	131
66	01000010	133
67	01000011	135
68	01000100	137
69	01000101	139
70	01000110	141
71	01000111	143
72	01001000	145
73	01001001	147
74	01001010	149
75	01001011	151
76	01001100	153
77	01001101	155
78	01001110	157
79	01001111	159
80	01010000	160
81	01010001	163
82	01010010	164
83	01010011	166
84	01010100	169
85	01010101	171
86	01010110	173
87	01010111	175
88	01011000	176
89	01011001	179
90	01011010	180
91	01011011	182
92	01011100	184
93	01011101	186
94	01011110	188
95	01011111	190
96	01100000	192
97	01100001	195
98	01100010	196
99	01100011	198
100	01100100	200
101	01100101	202
102	01100110	204
103	01100111	206
104	01101000	209
105	01101001	211
106	01101010	213
107	01101011	214
108	01101100	217
109	01101101	218
110	01101110	221
111	01101111	222
112	01110000	224
113	01110001	227
114	01110010	228
115	01110011	230
116	01110100	233
117	01110101	235
118	01110110	237
119	01110111	239
120	01111000	241
121	01111001	243
122	01111010	245
123	01111011	246
124	01111100	249
125	01111101	250
126	01111110	253
127	01111111	254

Successor Table

	ABCDEFGH	f
128	10000000	1
129	10000001	3
130	10000010	5
131	10000011	7
132	10000100	9
133	10000101	11
134	10000110	13
135	10000111	15
136	10001000	17
137	10001001	19
138	10001010	21
139	10001011	23
140	10001100	25
141	10001101	27
142	10001110	29
143	10001111	31
144	10010000	32
145	10010001	35
146	10010010	36
147	10010011	38
148	10010100	41
149	10010101	43
150	10010110	45
151	10010111	47
152	10011000	48
153	10011001	51
154	10011010	52
155	10011011	54
156	10011100	56
157	10011101	58
158	10011110	60
159	10011111	62
160	10100000	64
161	10100001	67
162	10100010	68
163	10100011	70
164	10100100	72
165	10100101	74
166	10100110	76
167	10100111	78
168	10101000	81
169	10101001	83
170	10101010	85
171	10101011	86
172	10101100	89
173	10101101	90
174	10101110	93
175	10101111	94
176	10110000	96
177	10110001	99
178	10110010	100
179	10110011	102
180	10110100	105
181	10110101	107
182	10110110	109
183	10110111	111
184	10111000	113
185	10111001	115
186	10111010	117
187	10111011	118
188	10111100	121
189	10111101	122
190	10111110	125
191	10111111	126

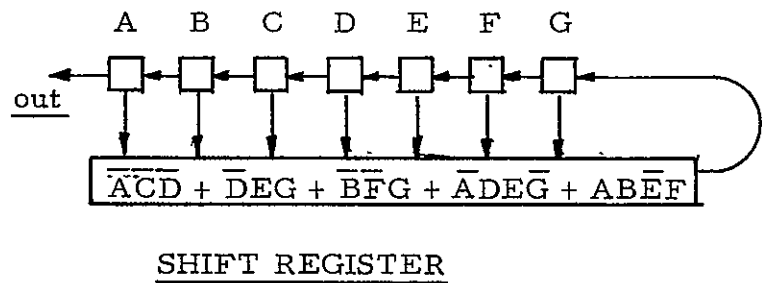
	ABCDEFGH	f
192	11000000	128
193	11000001	131
194	11000010	132
195	11000011	134
196	11000100	136
197	11000101	138
198	11000110	140
199	11000111	142
200	11001000	144
201	11001001	147
202	11001010	148
203	11001011	150
204	11001100	152
205	11001101	154
206	11001110	156
207	11001111	158
208	11010000	160
209	11010001	163
210	11010010	164
211	11010011	166
212	11010100	169
213	11010101	171
214	11010110	173
215	11010111	175
216	11011000	176
217	11011001	179
218	11011010	180
219	11011011	182
220	11011100	184
221	11011101	186
222	11011110	188
223	11011111	190
224	11100000	192
225	11100001	195
226	11100010	196
227	11100011	198
228	11100100	200
229	11100101	202
230	11100110	204
231	11100111	206
232	11101000	209
233	11101001	211
234	11101010	213
235	11101011	214
236	11101100	217
237	11101101	218
238	11101110	221
239	11101111	222
240	11110000	224
241	11110001	227
242	11110010	228
243	11110011	230
244	11110100	233
245	11110101	235
246	11110110	237
247	11110111	239
248	11111000	241
249	11111001	243
250	11111010	245
251	11111011	246
252	11111100	249
253	11111101	250
254	11111110	253
255	11111111	254

N=28

SEQUENCE: 1111010111100101100110000000

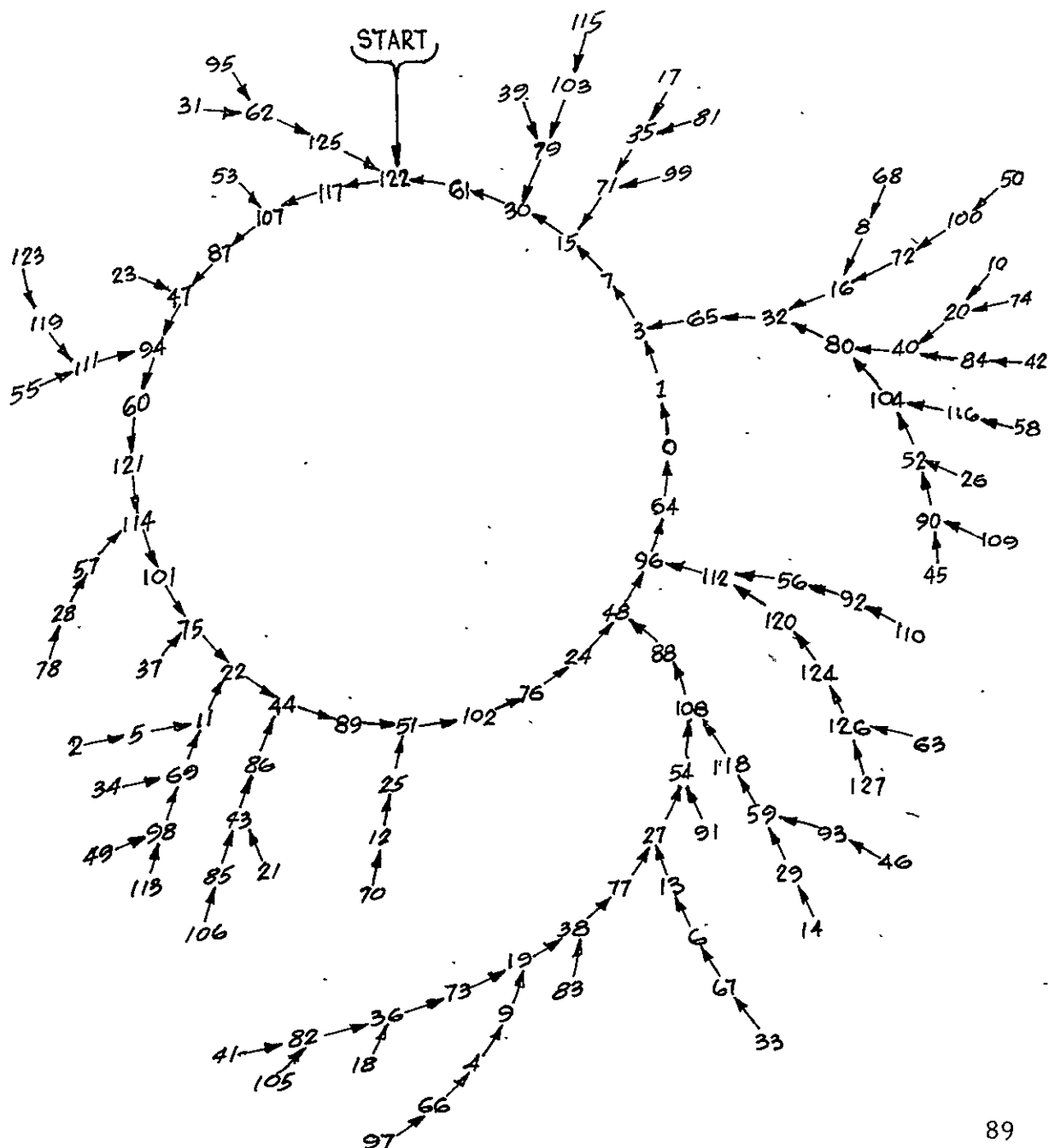
SPAN: 7

TRUTH TABLE								
	A	B	C	D	E	F	G	f
122	1	1	1	1	0	1	0	1
117	1	1	1	0	1	0	1	1
107	1	1	0	1	0	1	1	1
87	1	0	1	0	1	1	1	1
47	0	1	0	1	1	1	1	0
94	1	0	1	1	1	1	0	0
60	0	1	1	1	1	0	0	1
121	1	1	1	1	0	0	1	0
114	1	1	1	0	0	1	0	1
101	1	1	0	0	1	0	1	1
75	1	0	0	1	0	1	1	0
22	0	0	1	0	1	1	0	0
44	0	1	0	1	1	0	0	1
89	1	0	1	1	0	0	1	1
51	0	1	1	0	0	1	1	0
102	1	1	0	0	1	1	0	0
76	1	0	0	1	1	0	0	0
24	0	0	1	1	0	0	0	0
48	0	1	1	0	0	0	0	0
96	1	1	0	0	0	0	0	0
64	1	0	0	0	0	0	0	0
0	0	0	0	0	0	0	0	1
1	0	0	0	0	0	0	1	1
3	0	0	0	0	0	1	1	1
7	0	0	0	0	1	1	1	1
15	0	0	0	1	1	1	1	0
30	0	0	1	1	1	1	0	1
61	0	1	1	1	1	0	1	0



N=28

STATE DIAGRAM



	ABCDEFG	f		ABCDEFG	f
0	0000000	1	64	1000000	C
1	0000001	3	65	1000001	1
2	0000010	5	66	1000010	0
3	0000011	7	67	1000011	C
4	0000100	9	68	1000100	0
5	0000101	11	69	1000101	1
6	0000110	13	70	1000110	0
7	0000111	15	71	1000111	1
8	0001000	16	72	1001000	0
9	0001001	19	73	1001001	1
10	0001010	20	74	1001010	0
11	0001011	22	75	1001011	0
12	0001100	25	76	1001100	0
13	0001101	27	77	1001101	1
14	0001110	29	78	1001110	0
15	0001111	30	79	1001111	0
16	0010000	32	80	1010000	0
17	0010001	35	81	1010001	1
18	0010010	36	82	1010010	0
19	0010011	38	83	1010011	0
20	0010100	40	84	1010100	0
21	0010101	43	85	1010101	1
22	0010110	44	86	1010110	0
23	0010111	47	87	1010111	1
24	0011000	48	88	1011000	C
25	0011001	51	89	1011001	1
26	0011010	52	90	1011010	0
27	0011011	54	91	1011011	0
28	0011100	57	92	1011100	0
29	0011101	59	93	1011101	1
30	0011110	61	94	1011110	0
31	0011111	62	95	1011111	0
32	0100000	65	96	1100000	0
33	0100001	67	97	1100001	0
34	0100010	69	98	1100010	1
35	0100011	71	99	1100011	1
36	0100100	73	100	1100100	0
37	0100101	75	101	1100101	1
38	0100110	77	102	1100110	0
39	0100111	79	103	1100111	1
40	0101000	80	104	1101000	C
41	0101001	82	105	1101001	C
42	0101010	84	106	1101010	1
43	0101011	86	107	1101011	1
44	0101100	89	108	1101100	0
45	0101101	90	109	1101101	0
46	0101110	93	110	1101110	0
47	0101111	94	111	1101111	0
48	0110000	96	112	1110000	0
49	0110001	98	113	1110001	0
50	0110010	100	114	1110010	1
51	0110011	102	115	1110011	1
52	0110100	104	116	1110100	0
53	0110101	107	117	1110101	1
54	0110110	108	118	1110110	0
55	0110111	111	119	1110111	1
56	0111000	112	120	1111000	0
57	0111001	114	121	1111001	0
58	0111010	116	122	1111010	1
59	0111011	118	123	1111011	1
60	0111100	121	124	1111100	0
61	0111101	122	125	1111101	0
62	0111110	125	126	1111110	0
63	0111111	126	127	1111111	0

Successor Table