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STUDY AND DESIGN OF A CESIUM BOMBARDMENT ION ENGINE SYSTEM

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16. Abstract

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Preface

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1. INTRODUCTION

This report describes a program to study the feasibility of designing a cesium bombardment ion engine system whose control logic and power conditioning subsystem is based on welded electronic modular construction, and, upon establishment of feasibility, carry out the design of such a system. System specifications and design are based on a one millipound thrust system developed at EOS under Air Force Contract F33615-67-C-1268 and are described in the Final Report issued under that contract (Ref. 1).

Section 2 of this report discusses modifications to the original circuit design and the verification testing conducted in conjunction with them, and Section 3 describes the system design. Section 4 contains the required New Technology report.

2. CIRCUIT DESIGN

2.1 ARC DIPPER

Of the problems identified in the engineering model electronics system developed under Air Force contract, the most serious was that of the large surges of input current following high voltage sparks. During the momentary absence of high voltage caused by a spark, the plasma in the discharge chamber extruded out between the screen and accelerator electrodes. When the high voltage came back on, the plasma between the electrodes provided a high conductance path and the resulting large current was reflected as excessive system input current.

Originally the goal was merely to prevent the high voltage overload circuit from responding to the current surge caused by plasma extrusion, to avoid the continuous on-off cycling which would result. Since the I_+ trip point was already set at 200 mA, this was accomplished by incorporating a delay in the I_- overload sensing circuit. Because of the characteristics desired of this delay circuit, about seven components were used which otherwise would not have been needed. This scheme worked fairly well most of the time but was never really considered finalized.

When it became obvious that the resulting input current surges were a serious problem (peaks of around 8 amperes with a duration of several milliseconds) the most promising solution seemed to be to automatically reduce the discharge voltage momentarily following each high voltage spark. This method of "arc-dipping" was commonly used manually when operating ion thrusters with laboratory power supplies.

The addition of the arc-dipper function to the CLPC was simplified by the fact that the discharge power was already supplied by a separate arc converter with its own overload protection circuit.

Several approaches were considered. The one finally selected involved the use of a PNP power transistor to control the power supplied to the arc converter. Since this transistor also had the capability of completely shutting off this power, it could be used in both the arc dipper and overload protection modes. A circuit incorporating all these features was built and tested. It was found to work as expected and was connected to the system breadboard for a test with an actual thruster. This was performed with good results.

When the 15-day continuous thruster system test was begun, it was found that the delayed I_{-} sensing circuit was not performing adequately, and the arc dipper circuit was removed from the breadboard and adapted to the engineering model CLPC. The arc dipper was in operation throughout the entire test and was very successful.

A modified version of this circuit was developed and tested with the system breadboard and the same thruster. It uses somewhat fewer components and allows the arc dip parameters (degree of dip, risetime) to be changed independently; the PNP power transistor is retained. The entire arc dipper circuit, including the PNP transistor, consumes about one watt in normal operation. A check of the system input current during high

voltage sparking shows that no measurable increase occurs during the onset of the overload; recovery produces about a 6% increase with a duration of about 250 milliseconds. It was decided to incorporate this version in the system design. This solved the input surge problem and also allowed a simplification of the I_{-} overload sense circuit.

2.2 DEFLECTION CIRCUITRY

Another problem was the temperature dependence of the magamps used to control the power to the deflection leg heaters. The variation in RMS output current over a temperature range of 25°C to 75°C, approximately the expected range, was about 15%. Since deflection is proportional to power, this was clearly not tolerable.

No modification of the existing circuit seemed acceptable. A reduction of the temperature extremes seen by the magamps was limited by the ambient spacecraft mounting temperature which would vary at least 20°C. Controlling the magamp temperatures thermostatically would consume too much power. Using current transformers and feedback loops would mean considerable additional weight and complexity.

It was finally decided to try a completely new approach, using all-digital circuitry to transform the command information, which of course is a digital count, into heater power duty cycle, which can also be varied digitally.

A very promising circuit was designed with the assistance of R. Bartlett of GSFC. This circuit controls heater power by counting the individual cycles of the 10 kHz power waveform and switching the correct fraction of these cycles to the heaters. This is accomplished by comparing the count in the four-bit command register with the count in a continuously running four-bit counter which is counting the 10 kHz cycles. When

the 10 kHz counter fills (every 16 cycles) and resets to zero, the power switch transistor is turned on. When the comparator senses that the 10 kHz counter and the command register contain the same count, the transistor is turned off. There is a separate switch transistor for each deflection polarity (X+ and X-) and an additional flip-flop ensures that the polarity alternates after each sixteen command pulses. An identical circuit is used for the Y axis.

Because the power to the deflection heaters must be supplied at a low impedance (about 1.3 Vrms and 0.5 amp) and since an output transformer must be used to provide voltage isolation, the switching is done at a level of 30 volts. The switching circuit utilizes a center-tapped winding on the master converter transformer connected by steering diodes to the center-tapped output transformers. One such transformer, with its associated switch transistor, is of course required for each set of deflection legs (X+, X-, Y+, Y-). The switch transistors are protected against voltage transients by zener diodes.

Four suitable center-tapped output transformers were constructed. Two of these were sent to GSFC and were incorporated into a breadboard of this deflection system. The breadboard was sent to EOS for checkout. One minor change to the design was required, after which it was found to count and switch power as intended. Closer investigation showed a tendency of the transformer core to saturate near the end of either the first or second half cycle in each count period. This was found to be due to the effective short-term waveform asymmetry caused by the sudden application of a train of square-wave cycles, and by the propagation times associated with the logic and counter circuits.

While not serious from an operational standpoint, this tendency of the core to saturate caused the switch transistor to come out of saturation and withstand a very short period of relatively high power dissipation. Since the period is very short and the transistor drive is limited,

the transistors were not overstressed. However, several approaches were investigated in an attempt to eliminate or minimize the effect. Several different transformer configurations, including one with a core gap, were tried; none were successful. A modification to the logic, causing it to count half-cycles (instead of full cycles) and skip the first half-cycle, was employed to effectively alternate the polarity of the initial power seen by the core during each 16-count period. This was only moderately successful.

Finally it was decided simply to add another 16-step counter in front of the existing one. Since the core saturation occurs only at the beginning of each "power on" period, this reduces the magnitude of the problem by lowering the switching frequency. With this system, step number one allows 16 cycles of 10 kHz power to the heaters, step number two allows 32 cycles, etc. A complete count period is 256 cycles. Since step zero allows no power to the heaters, the maximum duty cycle is fifteen sixteenths, or 240 cycles in each period of 256. This method has been incorporated in the system design.

2.3 CLPC THERMAL/VACUUM TESTS

Thermal/vacuum tests of the engineering model CLPC were run at -20°C, +20°C, and +50°C with the CLPC mounted in a thermal enclosure inside the vacuum chamber. No problems were encountered with starting the converters or commanding the various functions. The only problem occurred after one hour and fifty minutes of continuous full power operation at 50°C. A failure of the V_+ rectifier module, apparently due to overheating the rectifier diodes, caused one of the high voltage converter transistors to short, disabling the converter and the CLPC. An identical rectifier module was fabricated and installed in the CLPC, and its temperature monitored in a similar test at -20°C. The temperature of the side opposite the mounting side was found to increase from -20°C to +59°C in an hour and five minutes, and was still increasing when the system was turned off.

Subsequent investigation showed that the thermal design of the module was indeed inadequate. The rectifier diodes were positioned at the top of the module, forcing the heat they produced to travel through about one-half inch to the bottom mounting surface. Also, the potting material chosen was filled with tiny hollow glass spheres for light weight, and consequently had very poor thermal conductivity.

A new module was designed with the rectifiers near the mounting surface and an integral aluminum plate on that surface. Stycast 2651, which has a thermal conductivity about ten times that of the glass-filled material, was used.

A complete thermal/vacuum test with this new module in the CLPC was attempted but the high voltage could not be turned on because of poor vacuum. Scheduling priorities for the vacuum chamber did not allow another try, so a bench test was done with fibrous insulating material surrounding the new module. Its temperature was found to increase only 2°C after five hours of full-power operation.

The V- rectifier module will be changed to a similar configuration in future units.

2.4 COMMAND INTERFACE CIRCUITS

New circuits designed include command interface circuits to accept the -5V to +5V pulses now anticipated, and modification of the command registers for the anode and cathode vaporizers to the "simmer-mode" configuration. This basically involved the addition of a flip-flop to each register, but the logic required necessitated some redesign of the registers. The resulting operating sequence is such that the first cathode vaporizer on command produces a low-level arc current; and the second and all subsequent cathode vaporizer on commands produce full arc current; a cathode vaporizer off command will reset the circuit so that the next

cathode vaporizer on command again yields a low arc current. The anode vaporizer circuitry controls the beam current in a similar manner. These circuits have been breadboarded, tested to assure satisfactory operation, and incorporated in the system design.

2.5 SYSTEM TEST

To verify the basic soundness of the system design, a test having goals of 15 days continuous operation and 15 days cyclic operation was planned and conducted. The thruster subsystem was operated in vacuum; the CLPC was operated in air and was connected to the thruster by means of a hermetic bulkhead connector.

The system thruster and CLPC was operated continuously for 360 hours with no failures. On-off cycling was begun simulating expected spacecraft duty cycle: 6 hours on, 18 hours off. After five cycles without event, it was clear that the system was compatible with cyclic operation. The engineering model CLPC was replaced with the breadboard version to allow evaluation of alternate circuit techniques for control functions. An additional 13 on-off cycles were conducted in this mode. When circuit evaluation was complete the test was stopped.

At the conclusion of testing a total of 465 hours of on-time had been logged and the system had undergone 18 on-off cycles. Mass efficiency calculated from the propellant weight loss for the test was 93% including startup and shutdown. Thus mass efficiency at full thrust is 94 or 95%. Typical operating parameters for the test are shown in Table 1.

Post test inspection revealed no degradation in thruster components. There was no significant electrode erosion, no cathode or plasma anode erosion and no loss in magnetic field strength.

TABLE 1

465 HOUR RUN DATA

Positive Supply Current	118.5	mA
Negative Supply Current	1.5	mA
Ion Beam Current	117	mA
Plasma Anode Current	1.75	A
Boundary Anode Current	0.150	A
Cathode Vaporizer Power	4.0	W
Anode Vaporizer Power	4.8	W
Neutralizer Vaporizer Power*	5.0	W
Neutralizer Bias Voltage	13.2	V
Neutralizer Probe Voltage	5.8	V
System Input Power*	140.0	W

*Neutralizer control characteristic was abnormal. The neutralizer vaporizer was either full-on or full-off. This table reflects the power condition. Maximum system power was 146W. Maximum neutralizer power was 11W.

There were two problems encountered during the testing. The neutralizer heat shielding shifted, creating a cavity between cathode and striker. The change in control characteristic resulted in oscillation between spot and plume mode. While not a particularly elegant operating mode, neutralizing electrons were provided even during plume mode operation and the control circuit was able to handle the situation. The problem was identified and will be eliminated in future tests. Anticipated mass efficiency for the neutralizer was 15 mg/hr; in this test the actual loss was 24.5 mg/hr.

Thrust vectoring was exercised during the cycling phase of the test. Anomalous results were obtained. A portion of the time normal deflection of 7^{o} was obtained, but a portion of the time only half this deflection was measured. No problem was uncovered in the test equipment and no malfunction was detected during post test inspection of the thruster. The problem appeared when using both breadboard electronics and laboratory power supplies. The problem is not yet understood and is being investigated.

3. SYSTEM DESIGN

The CLPC design effort began with the assumption that the minimum change to the existing package that would be required to reduce weight significantly would be to change from etched-circuit boards to welded modules for the command, control and telemetry circuits. An early start was made by assigning the individual circuit functions to various modules, which allowed the best module package size to be determined. At this time, because of the circuits being added and redesigned, few of the module circuits were finalized sufficiently to allow layout detailing. Therefore a study of the overall packaging configuration was begun.

The allowable package outline, as received from G S F C permitted a maximum length of twenty inches. By rearranging the existing A8 and A10 (power supply) circuitry into a linear configuration (maintaining the basic component position relationships), eliminating the subchassis themselves, and lining up the welded modules along one edge, the result was a package twenty inches long, seven inches wide, and 2 1/2 inches high over most of its length. This package had several advantages. It allowed a better thermal path into the spacecraft mounting plate, it provided a greater effective "floor area" for mounting the power components originally assigned to the A9 subchassis, and it promised excellent accessibility.

Because of the large amount of packaging redesign required, however, it was decided to avoid such a major change and investigate instead the improvements which could be made to the basic existing package.

The primary goal of the design effort is the reduction of total package weight to meet the present 16 pound requirement. Several modifications to the existing package toward this end were suggested:

1. Eliminate the A8 and A10 subchassis and mount the electronic components directly on the package base. This would require relocation of the separation point between upper and lower bases to allow adequate accessibility, but would make available additional floor space by eliminating several mounting points. It would also lower the thermal impedance from the heat-producing components, and would reduce system weight by about one pound.
2. Eliminate the hinge between upper and lower bases, or greatly reduce its size. The hinge is not a load-carrying member in operation, but is only present to eliminate possible overstressing of cables when the package is open.
3. Perform a complete structural analysis to determine how much the weight of the basic package structure can be reduced.

Previously, encapsulation of the magnetic components was under consideration as a means of controlling high-voltage breakdown and also to improve thermal conductivity and mounting problems. However, experience with the engineering model CLPC has shown thermal and mounting problems to be minimal, and years of experience have shown that "open" transformers, with no encapsulation, are the most reliable from the standpoint of voltage breakdown. Therefore it was decided not to encapsulate the magnetic components, which would have added considerable weight.

All of these weight-saving suggestions are valid. However, a tradeoff was necessary between the benefits gained and the expense and time involved in redesign. The result of this tradeoff was the decision to design the unit as follows:

1. Eliminate the card rack and redesign the upper portion of the package to house the welded modules and their mother board.
2. Retain the A8 and A10 subchassis.
3. Redesign the A8 and A10 subchassis as necessary to accommodate the circuit changes (relatively minor).
4. Redesign A9. This means relocating the deflection switching circuitry closer to the output connector if possible, and of course eliminating the deflection magamps and substituting the switch transistors.
5. Eliminating weight by reducing section thickness wherever possible.

Design work has proceeded on this basis. Details of system design are contained in the system drawings, delivered separately under the terms of this contract.

4. NEW TECHNOLOGY

4.1 ALL-DIGITAL DEFLECTION CIRCUIT

The thrust of an ion engine may be deflected by a small lateral translation of the accelerator electrode with respect to the screen electrode; the two electrodes form a pair of parallel planes separated by a few millimeters. The screen electrode is attached both mechanically and electrically to the main body of the thruster (the discharge chamber); the accelerator electrode is at a potential several hundred to several thousand volts different from that of the screen and therefore must be insulated electrically.

This method of beam deflection is used in the MESC ion thruster being developed for the ATS-F spacecraft. The lateral translation of the accel electrode, measured in thousandths of an inch, is produced by differential thermal expansion of support legs, which consist of eight coaxial electric heater elements arranged to operate in four pairs, one for each direction of deflection (+ and - X axis, + and - Y axis).

The system is designed for a maximum deflection of $\pm 7^{\circ}$ and in this range, beam deflection is approximately proportional to deflection heater power. The control system described here provides four-bit resolution (zero deflection plus fifteen steps in each direction). Previous deflection control systems have converted the basically digital command information, which consists of single cumulative command pulses, to an analog reference voltage which is used to control the deflection amplitude. In the new system, information is kept in digital form throughout, eliminating drift problems arising from D-to-A and A-to-D conversion.

Basically the circuit counts the cycles of the 10 kHz system power and treats them as separate periods of 256 cycles each, then switches a selected fraction of the cycles (in each period) to the proper heater pair, through isolation/stepdown transformers.

A schematic of one axis of the system is shown in Figure 1. All the logic circuits operate from +5V, which is obtained from a semi-regulated +6V supply through a suitable dropping resistor (18Ω). The 6V winding is also used to supply information to the 10 kHz counter, which consists of two SN54L93 four-bit counters connected to divide the frequency by a factor of 256 (Z2 and Z3). The A, B, C, and D outputs of Z3 transfer to a "1" state (+) at 16, 32, 64, and 128 cycles respectively, counting from the end of the previous 256-cycle period. The negative-going transition of the D output of Z3 occurs only at the end of this period and is used to set the master flip-flop (1/2 of Z7) to the power-on state by means of one-shot Q5. This power on state continues until the master flip-flop is reset (cleared) when the correct number of cycles have elapsed.

The command register Z1, also a four-bit counter, receives command pulses from the command interface circuit, Q1 and Q2. Z4 is a quadruple 2-input exclusive-or gate and is connected to compare the A, B, C, and D outputs of the command register Z1 with the A, B, C, and D outputs, respectively, of the 10 kHz counter Z3. When the binary count in Z3 is the same as that registered in Z1, all four of the outputs of Z4 are in the "0" state (ground potential). These outputs are inverted in polarity by four of the six open-collector inverters in Z5, and the outputs of these are connected to the four inputs of 1/2 of Z6. Z6 is a dual four-input expander, used as two open-collector gates. The output of this gate is used to reset the master flip-flop, turning off the heater power. Since the above functions are all direct-coupled, the turn-off pulse from Z6 is one cycle long and occurs during the same cycle as does the count coincidence in Z1 and Z3. This means that when the command register contains a zero count, the master flip-flop is maintained in the power off state, and no heater power is applied.

Since a zero step is desired, only fifteen command steps are available which means that the maximum duty cycle is fifteen sixteenths, or 240 cycles in each set of 256.

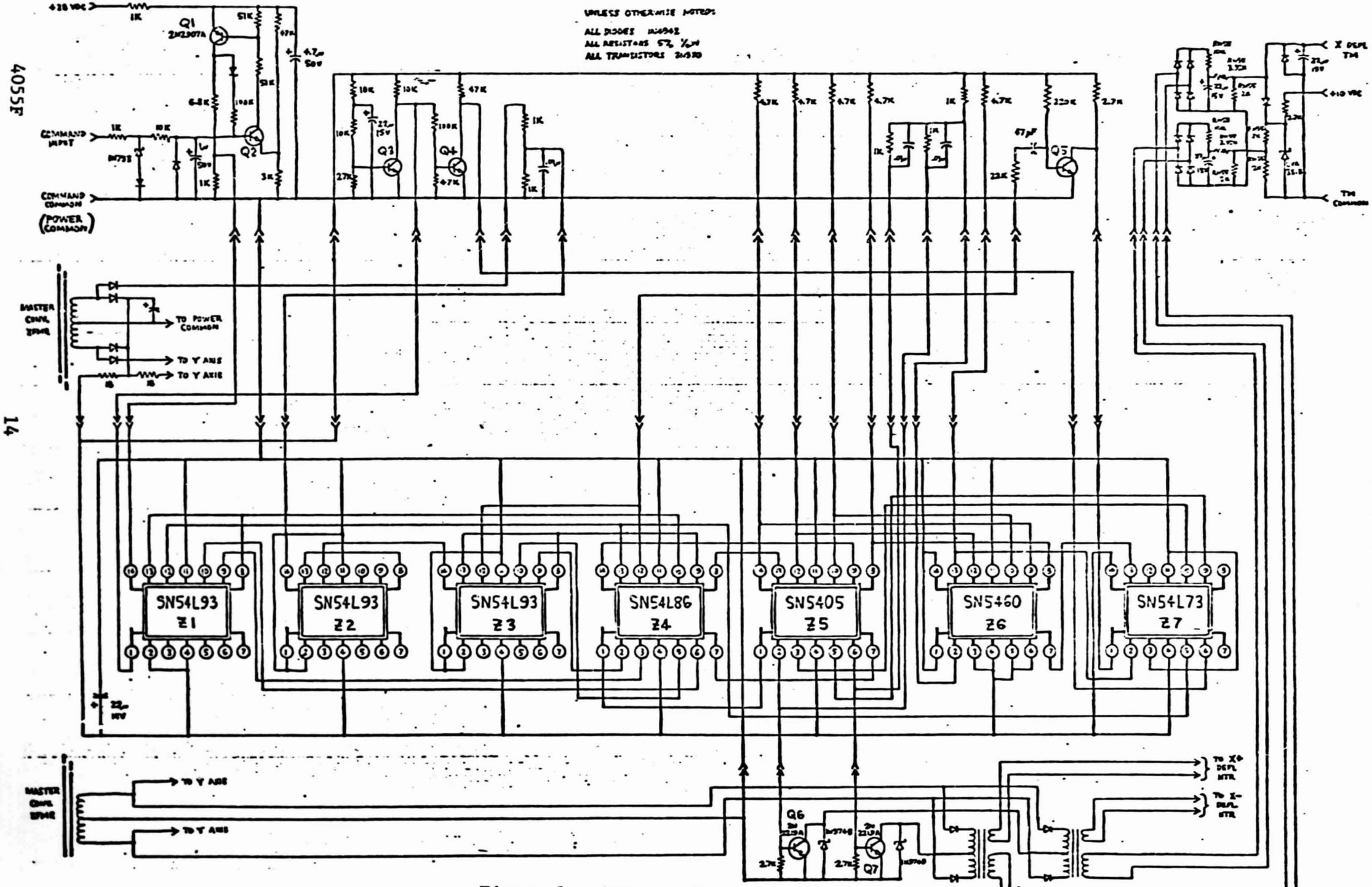


Figure 1. ATS-F Deflection Circuitry
(X-axis and common circuitry shown)

The sixteenth command pulse resets the command register to zero and simultaneously toggles the polarity control flip-flop (1/2 of Z7) so that the next sixteen commands control deflection power to the opposite pair of deflection heaters. This control is effected by the remaining two inverters of Z5, whose inputs are connected to the Q and $\overline{Q}$ outputs of the polarity control flip-flop, and whose outputs shunt the drive current to one of the two switch transistors, Q6 and Q7. This drive current is available only during power on periods due to the switching action of the remaining gate (expander) in Z6, which is driven by the master flip-flop in Z7.

A telemetry circuit accepts the duty-cycle information from separate windings on the isolation/stepdown transformers and converts it to an analog level between zero and +5 volts D.C., with 2.5 volts output at zero deflection. X+ deflection produces a higher voltage, and X- deflection a lower one.

Since the system must work in close association with ion thrusters, which can be very noisy electrically, precautions such as the zeners across Q6 and Q7, and adequate filtering of command lines, are necessary.

4.2 ARC DIPPER

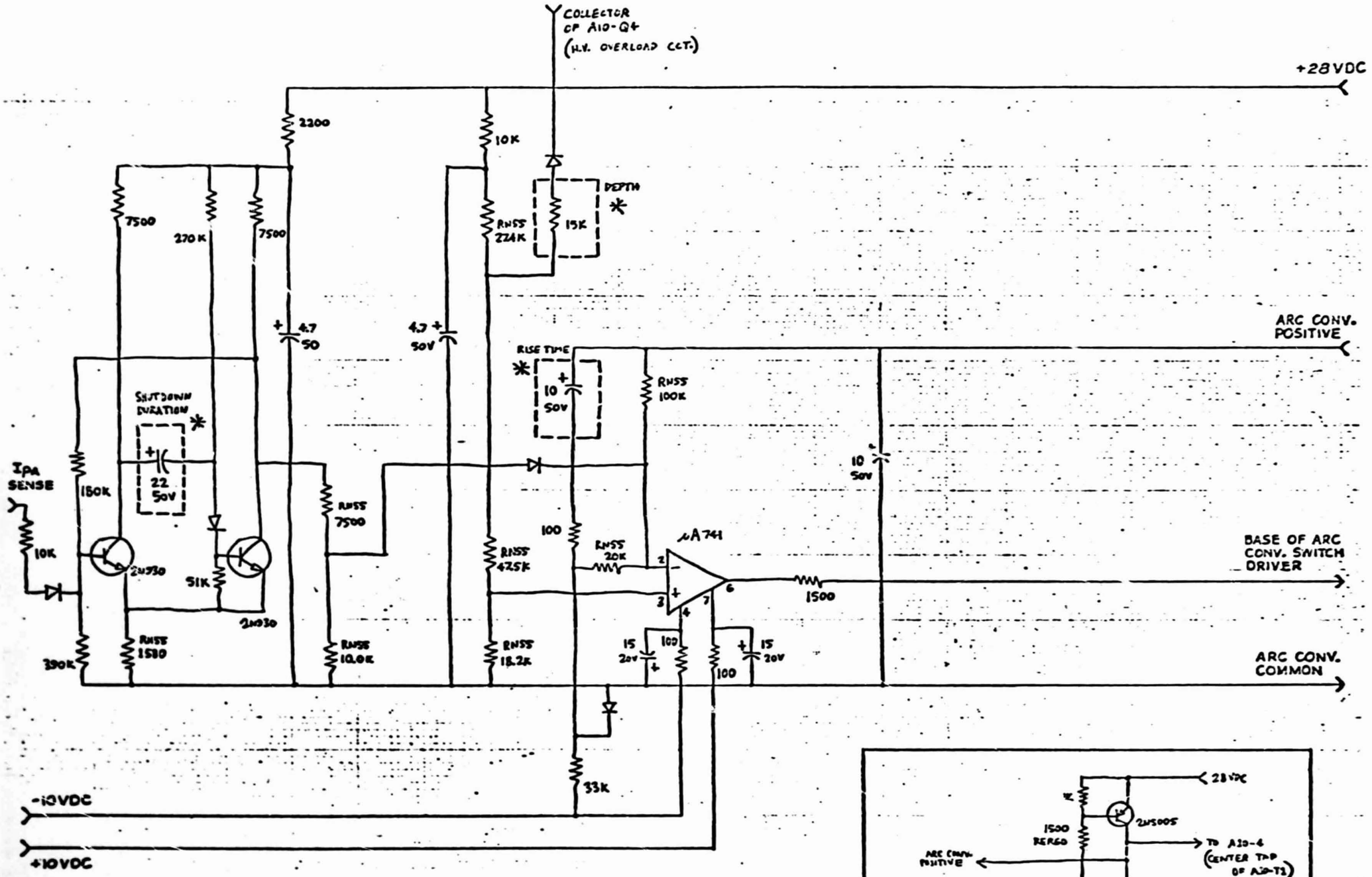
A problem frequently encountered in the development of ion engine power conditioning is that of plasma extrusion. The term refers to the fact that the plasma in the discharge chamber is forced out between the screen (positive) and accelerator (negative) electrodes when the high voltages on these electrodes is removed, such as happens briefly during a spark. The problem results from the presence of this plasma between the electrodes when the high voltages return; the situation can produce continuous sparking with consequent interruption of ion thruster performance.

The simplest approach to a solution is simply to make the high voltage supplies capable of supplying sufficient current for a long enough time (around fifty milliseconds) to clear the plasma from between the electrodes. This will work, but the resulting system input power surges are very large and undesirable.

A preferable approach is to reduce the voltage supplied to the discharge chamber whenever the high voltage supplies are overloaded. Thus when a spark occurs the electrostatic field in the discharge chamber is momentarily reduced and no appreciable amount of plasma is extruded, providing only that the discharge voltage return to its nominal level at a gradual rate, around 20 volts/sec or less.

Since the plasma discharge supply (arc supply) in the ATS-F thruster system consists of a DC-to-DC converter separate from the other power conversion functions, the addition of the "arc dipper" function was relatively straightforward. The converter is a conventional driven parallel transistor type operating from the 28VDC system power. Previously it was connected directly to the 28VDC and controlled by interrupting the base drive power; since the arc converter function requires gradual voltage changes. A PNP power transistor was connected to control the amount of power available from the 28VDC line. The base drive control circuitry was then eliminated, and on/off control is now effected through the PNP transistor.

Figure 2 shows a schematic of the arc dipper and arc overload circuit. The arc dipper portion consists basically of an operational amplifier connected in a feedback loop to control the voltage supplied to the arc converter by controlling the drive to an NPN transistor which drives the 2N5005 PNP power transistor (these are shown in the block at lower right). The op amp is provided with a reference voltage of five volts by the voltage divider connected to pin 3; the 100K and 20K feedback resistors were selected so that the 2N5005 is normally saturated and the control loop is consequently open.



* COMPONENTS WITHIN DASHED LINES TO BE ACCESSIBLE AFTER ENCAPSULATION

Figure 2. Arc Dipper and I_{PA} Overload Circuit

When a spark or other high voltage overload occurs, the high voltage overload cirucit pulls the arc dip input, shown at the top of the schematic, down to about two volts. This lowers the op amp's reference voltage from five volts to about three volts. This is low enough to allow the control loop to become closed, and the op amp accordingly reduces its output level until the 2N5005 reduces the converter input voltage (arc converter positive) from 27.5 to around 19 volts; this "dips" the arc, since the discharge voltage is proportional to the converter input voltage.

In the case of a single spark, the high voltage overload circuit remains toggled for only about twenty milliseconds; then the high voltage comes back on with a risetime of only one or two milliseconds. Since the risetime of the discharge voltage must be considerably longer, the op amp circuit incorporates a capacitor connected so that it provides negligible delay during the fall-time of the output voltage, but causes a slow semi-linear risetime of about 200 to 300 milliseconds, depending on the value of the capacitor.

In the quiescent state, the control loop is open, so no stability problems are present. When the arc is dipped, and during the risetime period, the control loop stability is determined by the risetime-determining capacitor which provides a very slow, stable loop.

As stated above, the arc overload function operates through the same 2N5005 power transistor. This is accomplished by connecting the output of the arc overload one-shot to the op amp circuit so that it provides the equivalent of excessive feedback voltage. This causes the op amp to shut off the arc converter completely for the period of the one-shot, which is about five seconds. At the end of this time the control loop is restored and the risetime capacitor again provides a slow turn-on characteristic.

REFERENCES

1. Worlock, R., James, E., Gant, G. et al: "Prototype Cesium Bombardment System," Air Force Aero Propulsion Laboratory Technical Report AFAPL-TR-70-62, September 1970.