THE IMPACT OF LSI (LARGE-SCALE INTEGRATION) ON SYSTEM PACKAGING

by

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The Manned Spacecraft Center has undertaken a feasibility study to develop an LSI microprocessor. The stacked multilayer circuit module concept was developed to package this processor in one cubic inch.

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SUMMARY

The potential advantages of large-scale integration will be gained or lost by the system packaging engineer. To fully realize these advantages it is necessary to move in the direction of physically integrating the whole system. Just as the interconnection of circuits in a piece of silicon is the key to LSI, so are the various levels of interconnection in a system the key to its integration. The improved packing density brought about by the systematic application of the physical integration philosophy is quantitatively given. The way in which LSI influences the packaging of circuitry which cannot be realized in LSI form is also discussed.

SOMMAIRE

Les avantages que présentent l'intégration sur grande échelle (LSI) ne peuvent etre exploités que par l'ingénieur chargé de la configuration des systèmes. Pour tirer pleinement part de ces avantages, il faut envisager l'intégration physique de l'ensemble des systemes. Les raccords entre circuits dans une barre de silicone constituent le probleme essentiel de la LSI, de la même façon, la clef de l'intégration d'un système dans la définition des differents niveaux de ses raccords. Les progrés réalisés dans la miniaturisation grâce a l'application systématique de la philosophie de l'intégration physique font l'objet d'une description quantitative. Cet exposé s'interesse aussi à l'influence de la LSI sur les circuits "dans la masse," que l'on ne peut réaliser sous la forme LSI.

INTRODUCTION

The potential advantages of large-scale integration will be gained or lost by the system packaging engineer. Some of these advantages seem obvious, such as a savings in weight. However, it will be shown that LSI can be exploited to a much greater degree than immediately obvious, through good system packaging, or what we prefer to call system physical integration.

The potential advantages of LSI are very interrelated and it is impossible to discuss one fully without reference to the others. For example, the fact that LSI will consume less power for a given function can be translated into a weight savings in power supplies, voltage regulators, power transmission wires, electrical generators, thermal cooling equipment, and eventually even in the aircraft or vehicle frame itself. Thus a savings of power in the logic of an air or spaceborne computer represents a considerable, but not completely obvious, saving in craft weight.

A list of the advantages we may expect to gain through the knowledgable exploitation of LSI is as follows:

1. Reduced weight and volume are particulary avantageous in mobile and spaceborne systems.
2. Shorter connection paths produce proportionately shorter signal time delays.
3. Shorter connection paths are less susceptible to noise.
4. Shorter connection paths have less stray capacitance and may have less resistance and inductance.
5. Less system power is required to drive the lower connection path capacitance.
6. Although total system power will be lower, power density will be higher. This can actually be an aid in removing heat. For example, if heat is removed by conduction, a shorter heat

path means that it can also be of smaller cross section for a fixed heat flow and temperature drop.

7. Improved reliability is made possible through the use of batch processes to make interconnections which previously would have been made by wire bonding, soldering, welding, etc.
8. Reduced cost.

Cost deserves special attention in the above list. Cost represents a common denominator for measuring improvement resulting from gaining the other advantages cited. The example above regarding the relationship between power and weight savings makes it evident that a system user cannot just say that cost savings can be calculated in terms of the difference in cost between one LSI circuit and a handful of lesser integrated circuits which could be interconnected to perform the same function. Furthermore, he cannot get a complete cost picture by comparing a system made with LSI against an older system, unless he also considers the cost of using, repairing, and transporting the system for its lifetime.

Reduced volume (or increased packing density) is a common denominator for realizing the advantages cited above. For example, a reduction in system volume will result in shorter connection paths and the benefits of lower capacitance, shorter delays, etc. It may also allow the substitution of one technology for another, such as an epoxy-glass multilayer wiring board in place of a wire-wrap field which will in turn reduce system volume more. It is therefore reasonable to expect that efforts to make systems smaller may be rewarded by gains in many or all of the advantage areas cited.

DEFINITIONS

The terms, large-scale integration and packaging, are described below in a somewhat restricted sense, which suits the needs of this paper.

Large-Scale Integration

The term LSI, or large-scale integration, can be considered as a level of complexity in a single silicon chip. LSI is defined as a silicon chip containing the equivalent of 100 or more gates. Obviously this makes little sense when talking about a semiconductor LSI memory, but we can rationalize this by accepting the idea that 600 or 700 components in a chip is equivalent in complexity to 100 gates.

Packaging

The term packaging can be applied to a wide range of activities. It can be used for putting resistors in a carton for shipping, for designing a TO-5 can and putting a transisitor chip in it for physical protection, or for the physical design and assembly of a complete electronic system. This paper will discuss the latter two aspects of packaging. The term packaging will be used hereinafter for the design of a protective unit (package) and the act of mounting a component, integrated circuit chip, LSI chip, multiple semiconductor chips or unprotected hybrid circuit in it. A term for the physical design and assembly of an electronic system is discussed below.

Physical Integration

In order to focus on the new emphasis required for the physical design of systems incorporating new components such as LSI and hybrid circuits the term "physical integration" will be used. The term alludes not only to integration in a material sense, but also to integration based on applicable physical laws applied to the system as a whole. For example, the designer of a system connector must consider not only such things as connector size, resistance, and reliability, but also whether it will contribute to system heat transfer and structural integrity.

The human nervous system is a good example of a physically well integrated system. Of course economics and repairability place limits on building such a system even if we had the technology. Physical integration will require that system designers apply their knowledge of logic, device physics, materials,

heat transfer, high-speed data transmission, electromagnetic interference, reliability, repairability, and testing concepts. All these factors must be considered and compromises must be made to achieve future system goals.

The complexity of these tradeoffs is more evident when we realize that a study of heat transfer alone must consider thermal properties of materials, thermal interfaces at mechanical and electrical joints, the distribution of thermal sources and sinks, device dissipation, device temperature rise versus reliability, and cooling methods available.

DISCUSSION

Single-Chip Packaging and Interconnection

This section deals with the interconnection of packaged LSI circuits using conventional interconnection methods. LSI circuits can be purchased in three basic forms:

1. In a commercial package such as the 24-lead dual-in-line package (DIP) shown in Figure 1.
2. In a space saving package such as the flat pack shown in Figure 2.
3. As bare chips. These chips may be provided with beam leads or bumps and may also be provided with a protective coating such as glass or silicon nitride.

In Figure 3 we see dual-in-line packaged LSI and small integrated circuits are plugged into a wire-wrap board. In this board, power and ground are provided through the printed circuits on both sides. The LSI package is large for two reasons, first, to provide two rows of 18 pins which are on 100-mil centers, and second, to provide enough surface area to dissipate the 600 milliwatts required by the scratchpad memory chip. In many cases the LSI chip power dissipation will not be this high. A smaller quad-in-line package may well be developed with leads on a 100 mil grid to package lower power LSI.

Looking again at Figure 3 it can be seen that seven LSI packages can be put in the same space required for 24 sixteen-lead DIPS. If we assume that each DIP contains four gates and that each LSI package contains a minimum of 100 gates (equivalent), we find that LSI has allowed us to interconnect 700 or more gates where previously 96 would have been interconnected.

We might also look at a system consisting of flat packs on a multilayer wiring board. Figures 4 and 5 show such a board interconnecting dual-NOR gates packaged in 10-lead flat packs. Tight packing will allow about seven of these flat packs to be interconnected on one square inch of multilayer wiring board.

A square LSI flat pack with 36 leads on 50-mil centers will require one square inch of multilayer board for interconnection. See Figure 6. Here LSI has allowed us to put 100 or more gates in the same area that would be occupied by 14 gates in dual-gate flat packs. Table I summarizes these comparisons in its first four entries.

In the previous example we might question the effect of using a LSI package with leads on 25-mil centers instead of 50. We have assumed a multilayer wiring board is being used for interconnection. Normal design of such a board would call for a 50 mil center through hole spacing if space were allowed for one conductor to be run between holes on each layer. The net result is that, even if the LSI package is made appreciablly smaller by using a smaller lead spacing, the restriction on through-hole spacing will still require that almost one square inch of multilayer board area be devoted to interconnecting each package. A general lesson to be learned from this example is that one must consider the means of interconnection before one can truly predict the volume saving made possible by LSI on a system basis. This example also indicates that an improvement in LSI package volume may not be passed on as a system saving unless the interconnection problem is successfully attacked, too.

LSI, a Building Block for Physical Integration

The prior discussion has demonstrated the limited increases in packing density that might be achieved by using individually packaged LSI instead of conventional integrated circuits, and applying conventional interconnection techniques. We may gain some insight into what can be done to increase packing density on a system basis by examining LSI itself to see what makes it so attractive. The immediate and somewhat superficial answer is because many packages are replaced by one package, many interconnections are eliminated, and many of those connections that remain are on the chip itself, which reduces cost and increases reliability.

Perhaps more basic to the success of LSI, and indeed the reason for its name, is the fact that all parts of the LSI chip serve multiple basic functions. The components and interconnections in a LSI structure compose only a small part of the volume of a chip, however, the remaining part of the chip contributes to its overall strength and thermal dissipation, the prime functions of the larger part of the otherwise unused silicon. We might conclude that the design of parts of a system to serve two or more basic functions is a desirable guide in working toward a "physically integrated" system.

Table I

Comparison of equivalent gate packaging density
for various circuits, packages, and interconnection methods.

Circuit	Package	Interconnection Method	Equivalent Gates per cubic inch including interconnections
4 Gates	16-Lead Dual-in-Line	Wire-wrap	6
LSI Circuit (100-Gate Equiv.)	36-Lead Dual-in-Line	Wire-wrap	44
2 Gates	10-Lead Flat Pack	Epoxy-glass Multilayer Wiring Board	70
LSI Circuit (100-Gate Equiv.)	36-Lead Flat Pack	Epoxy-glass Multilayer Wiring Board	500
9 LSI Circuits (900-Gate Equiv.)	Multichip LSI Package	Epoxy-glass Multilayer Wiring Board	2310
45 LSI Circuits (4500-Gate Equiv.)	5 Multichip LSI Packages	Riser Pin System	9000

PHYSICAL DESIGN FEATURES

Physical design, in the most basic terms, consists of designing for the electrical interconnection of components, extraction of heat, and mechanical integrity in a specified environment. One must bear in mind at all times the trade offs between these areas while evolving a design. System logic designers must consult with the people responsible for the physical design and realization of the system and with the LSI vendors, in the conceptual phase, to achieve the goals of physical integration. A good system design can only be achieved if good compromises are made in the areas of LSI design, system electrical design, and system physical design.

Interconnections

In a previous example it was shown that designing with smaller LSI packages than presently available (with leads on 25-mil centers) would save little or no space in a system unless the interconnections (in the example a multilayer wiring board) could be made compatible with the package. Beyond this, it can be flatly stated that interconnections make up the majority of the volume in present-day electronic systems. This fact alone compels one to study the interconnection problem.

Interconnections are best when eliminated. If this is not possible, permanent interconnections are preferred to demountable ones. Unfortunately, the need for repair, modification, economy, and electrical test preclude this ideal situation. As a compromise situation we must resort to partitioning a piece of equipment or system into manageable portions which may be interconnected by demountable connections. Good partitioning requires the cooperation of the electrical, LSI, and physical designer. For example, increasing the number of gates in a LSI chip may reduce the lead/gate ratio. However, the number of lead connections which can be made to a chip is a function of the chip periphery length, while the number of gates that can be put on a chip is a function of area. Of course there are, and always will be, technology limits on how big a chip can be made and packaged. These variables leave considerable room for tradeoffs. As another example of an area for designer compromise, it might be desirable to use serial instead of parallel transmission to reduce interconnections. Such a change may or may not be compatible with system speed requirements.

When analyzing a system from a physical integration point of view it is helpful to consider the levels of interconnection in the system and the method of connection. A complex system may have 4 (or possibly more) levels as listed below:

Level 1 - can be represented by interconnections in a hybrid circuit. Interconnections are usually non-repairable. A failure in a component would require replacement of this level as the unit is not repairable.

Level 2 - can be represented by a multilayer wiring board, or cordwood welded matrix interconnections. Connections are semipermanent. Repairs can be made at the fabrication facility.

Level 3 - can be represented by pin connectors with a wire-wrap field interconnection. Connectors are demountable and therefore a replacement module can easily be installed.

Level 4 - can be represented by a cable and connectors interconnecting subsystems. These connectors are demountable and therefore subsystems can be replaced easily.

These defined levels of interconnection aid in dividing the physical integration problem into portions of managable size at the hazard of neglecting the effect that a decision made in one area will have in the other areas. Keeping this hazard in mind, the physical designer must consider for each level the items listed below:

1. Heat transfer within each level and to the next level.
2. Type of connection or connector.
3. Type of interwiring.
4. Partitioning for a minimum number of connections, ease of testing, and ease and cost of repair.
5. Ability to stand environmental stresses.
6. Reliability.
7. Volume.
8. Weight.
9. Cost.

Mechanical Integrity

The environmental conditions under which a system may be required to operate vary over a wide range. Ground-based computers may be in environmentally controlled rooms isolated from all but the mildest vibrations. Spaceborne computers may be required to operate reliably under severe shock, vibration, and temperature excursion conditions in a vacuum as well as under atmospheric conditions. Care is required in the selection of materials for matched thermal expansion and, if this is not possible, methods of stress relief must be built in. Substantial amounts of material may have to be added for structural rigidity. Everything must be held firmly in place with screws, cement, potting, etc. A physical designer should repeatedly ask himself whether the material added for mechanical integrity can also be made to act effectively to help solve the heat transfer problem and/or double as part of a connector structure.

Heat Transfer

The higher packing densities possible with LSI imply a significant increase in heat dissipation per unit volume despite the fact that the power per function is reduced. The cooling technique for a particular system must take into account coolants already available. For example, cooling air might easily be bled from a jet-engine compressor. One should design for a minimum weight of the electronics and cooling system taken as a whole, particularly for spaceborne and airborne systems. The ability of the cooling system to remove large amounts of heat from small volumes is important to prevent hot spots. For high power density equipment, cooling by liquid flow or cooling by boiling might be considered. Thermoelectric cooling and heat pipes should be considered for hot-spot control. It is of course advantageous if material added for thermal control doubles either as a structural member or as part of a connector.

LSI IN SPACEBORNE COMPUTERS

The remainder of this paper deals with a practical application of the physical integration philosophy. A method for utilizing LSI in an aerospace system will be presented.

Multiple Chip Packages

It is already common practice to interconnect several integrated circuits in one package. This is the level 1 interconnections previously discussed. LSI has put these interconnections right on the silicon chip. We will call interconnections on the chip level 0. Because interconnections typically take more space at higher levels, it would seem wise to make use of level-1 wiring instead of omitting this level and going directly to level 2. This suggests a multichip LSI package. The resulting savings in space and number of connections is obvious. The immediate reaction to such a proposal might be an objection to the cost of a multichip LSI package which must be thrown away if an internal failure occurs. One must balance this against weight and volume savings and improved reliability. We believe in the advantage of the multichip approach and have proceeded to develop this idea and to study its impact up to the system level.

The first practical question is how to provide enough LSI chips in one package to allow some system partitioning flexibility. A limitation is the fact that a conservative, high-reliability approach still demands that the LSI chips be placed in a hermetic package, and it is difficult to seal packages larger than about one-inch square. The solution to this problem should provide LSI chip interconnections which also serve as a structural member and/or as an aid to heat transfer.

One solution utilizes a product which has recently become available. This is a ceramic multilayer wiring board. In many respects it is like an epoxy-glass multilayer wiring board. It is different in a few important areas. A ceramic multilayer wiring board conducts heat well because the dielectric is alumina. The alumina can also serve as part of a hermetic package. Also, conductor paths and through holes can be made in smaller geometries in ceramic boards than in epoxy-glass multilayer wiring boards.

The board as shown in Figure 7 is one-inch square, can accommodate nine 140-mil-square LSI chips with 36-lead pads each, and has 72 input/output pins. Up to ten layers of circuitry can be provided in the board. The internal tungsten, platinum, or moly-manganese wiring has a sheet resistance of about 0.01 ohm per square which means that a one-inch long conductor ten-mils wide would have a resistance of one ohm. The alumina layer between wiring planes is typically five- to ten-mils thick. The metallized ring inside the I/O pads can be used for applying a hermetic cover.

The number of I/O pins for the package can be changed by changing from a square to a rectangular form factor and/or by adding a second row of I/O pins around the periphery. The pins shown are brazed into blind metallized holes in the ceramic plate. Other I/O pins or tabs may be used. For example nail head pins can be butt brazed to metallized pads on the bottom surface of the ceramic thereby removing the requirement for holes in the ceramic. Or if metallized holes are provided through the ceramic, pins

can be swaged into the plate cold or they can be heated during the swaging process using a resistance welder. We must look at the next level of interconnections (level 2) to select which option is best.

This package can hold and interconnect the equivalent of 900 or more gates. Figure 8 shows how these packages can be interconnected to form a module using an epoxy-glass multilayer wiring loard. Heat is removed from the package by conduction to a pillar, a part of the structural plate which extends through the epoxy-glass multilayer wiring board. A module built in this way would have an effective electronic density of 2310 gates per cubic inch which is more than a factor of four better than that achieved with individually packaged LSI chips. See table 1. We have neglected the module mounting hardware and input/output connections to the module as in previous examples.

Level of Wiring, Key to a New Module

In the preceding example we made the obvious choice of using an epoxy-glass multilayer wiring board to interconnect multichip LSI packages. Epoxy-glass boards are of limited value as a heat transfer medium or structural member under high mechanical-stress conditions. The obvious next question is how to change this level of interconnection to a more effective system which will provide better heat transfer, or mechanical integrity, or both. Level-0 and level-1 interconnections have been made on parallel planes. It would be advantages to make level-2 interconnections in the third dimension to prevent our subsystems from taking on the form factor of a large thin slab.

Figure 9 shows one method of accomplishing this goal. Here five multichip LSI packages are stacked and joined by oven-soldering the pins from one package to the next lower package in the stack. Separate electrical connections can be made to the pin and corresponding hole in the multichip LSI package, or else they can be made electrically common. Repairs can be made by removing a defective multichip LSI package and replacing it. The pins provide both mechanical integrity and an excellent heat transfer path vertically through the module.

Thermal calculations show that this module can easily dissipate five watts. These calculations were made assuming that a 0.7 x 0.7-inch 50^{o}C sink is in good thermal contact with the bottom multichip LSI package in the stack. Only cooling by conduction was assumed. The temperature differential between the heat sink and the center of the top multichip LSI package was found to be about 25^{o}C.

The riser pins serve both the interconnection function of the epoxy-glass mulitlayer wiring board and the heat transfer function of the heatsinks shown in Figure 9. As a result this module can achieve an electronic density equivalent to 9000 or more gates per cubic inch if we again neglect connections to the next level of interconnection. This is a factor of four gain over the multichip-LSI package interconnected using a multilayer epoxy-glass wiring board. Table 1 shows that this is more than an order of magnitude gain in volume efficiency over individually packaged LSI circuits interconnected by an epoxy-glass wiring board.

Interconnecting the LSI Module

The module assembly is an expensive item. In many instances ease of equipment repair will require that the module be connected in the system with a demountable connector. In other applications, weight and space may be at such a premium that repairability may have to be sacrificed. An extreme case would be a deep-space probe where repair is not possible after the mission has started. Therefore, two possible methods for connecting modules to the next level of interconnections will be shown. We have chosen an epoxy-glass multilayer wiring board as the interconnection method.

Figure 10 shows the LSI module in a Malco pin connector assembly. Malco pins on 100-mil centers were chosen because of their proven reliability. A heat path is provided to the main frame through the connector by cementing the LSI module to the connector housing and making a pressure grease joint between the connector housing and plate. Connectors are available with contacts on 50-mil centers which would use appreciablly less space, but one must then make the tradeoff between weight, volume, and reliability.

Figure 11 shows a method similar to that used for the multichip LSI package for semipermanent connection to a multilayer epoxy-glass wiring board. The large space saving over the demountable connector is obvious.

LSI Power Supply —Not Yet

Unfortunately, no way has been found to put power supplies, ladder networks, coils, and some other discrete components in LSI form. Neither has LSI been able to replace all memory functions. We must therefore consider how these necessary system parts and LSI can be made compatible from a system integration standpoint.

We have already described the use of hybrid-circuit technology in the form of a ceramic multilayer board. The same technology offers a solution to the packaging of circuits where power or passive component tolerances preclude their conversion to LSI form. Hybrid circuits are planar in form. They can be stacked to form the same type of modules as made by stacking multiple LSI packages. They might even be included in a stack of multiple LSI packages. For example, it might be desirable to have a local voltage regulator for a logic module included within the module.

Memories such as core stacks or plated-wire assemblies can be physically integrated with LSI by arranging their dimensions to be some integral multiple of the dimensions of the LSI and hybrid modules (including a connector if used.) Inclusion of auxiliary electronics along with the memory can reduce the number of inputs and outputs to the memory module.

LSI and hybrid technology can be used to provide display decoding and drive circuitry packaged with or immediately adjacent to display devices with little or no increase in volume.

Interconnections Between Subsystems

The number of signals passing between various parts of a sybsystem will grow with increased system complexity. Fortunately, cables need not grow more numerous and bulky. The multiplexing of signals over transmission lines is often economically practical with LSI, and can reduce total system weight and cost even when lines are relatively short. The number of lines and line connections will drop dramatically, but the quality of the connections and lines will have to be carefully controlled to insure good impedance matching.

CONCLUSION

To keep the physical realization of a system abreast of new components, such as LSI, it is necessary to emphasize an approach to the physical design which we have called "physical integration." The effects of the systematic application of this approach have been demonstrated. Ceramic multilayer wiring boards and riser pins are shown to serve double duty as both electrical interconnections and thermal paths. Table 1 summarizes the greatly improved packing density possible for LSI semiconductor chips as a result. The packaging of other system components might best be done using a hybrid approach. Even the physical dimensions of core memories and the harnessing between subsystems will be strongly affected by LSI technology.

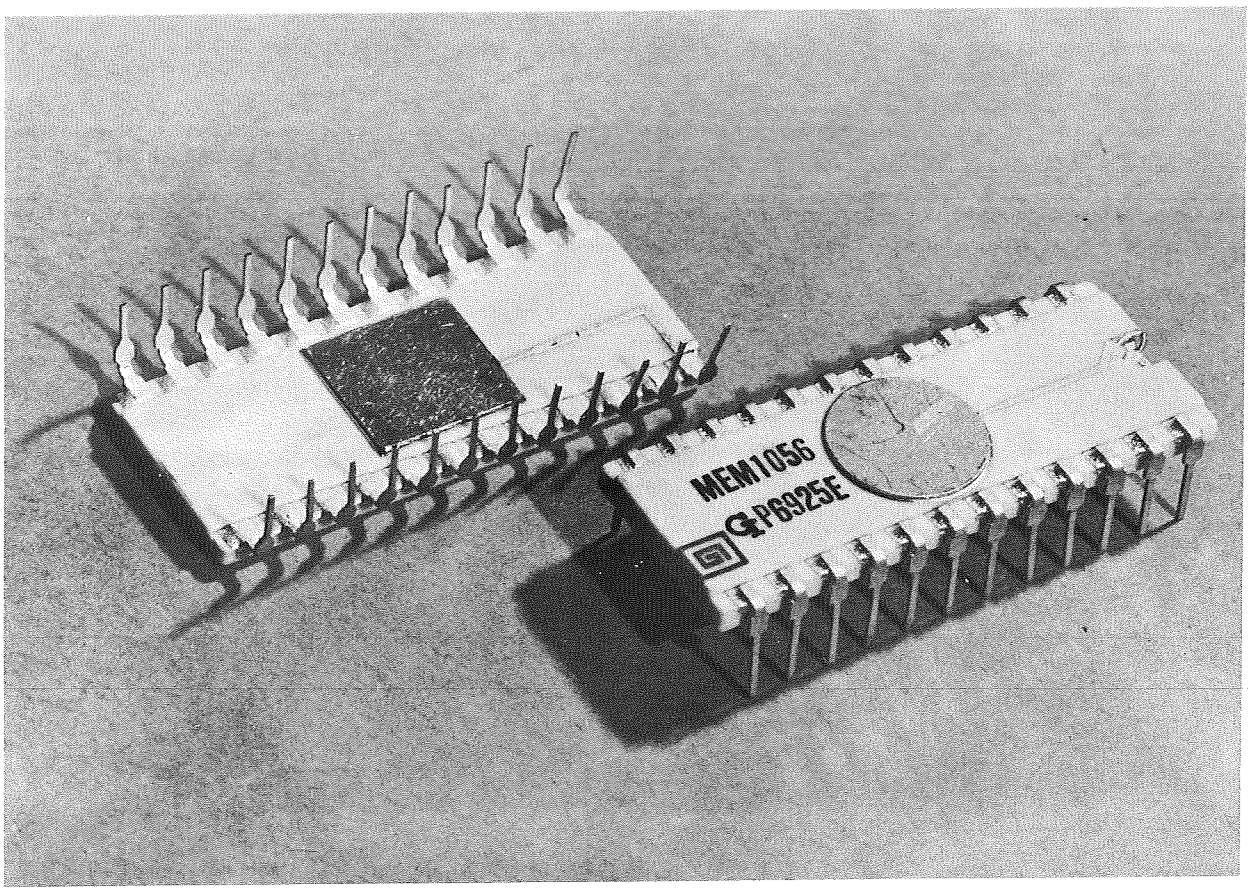

Figure 1

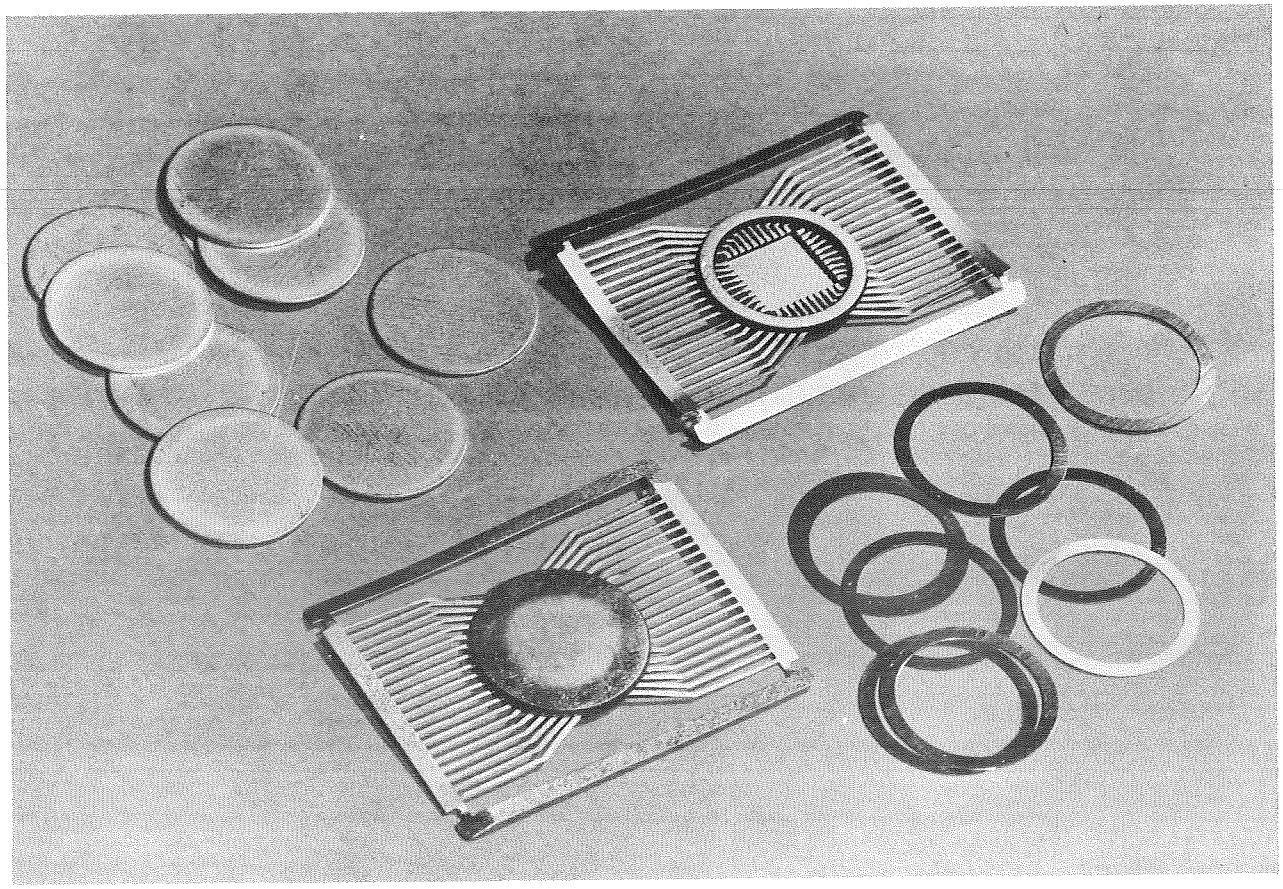

Figure 2

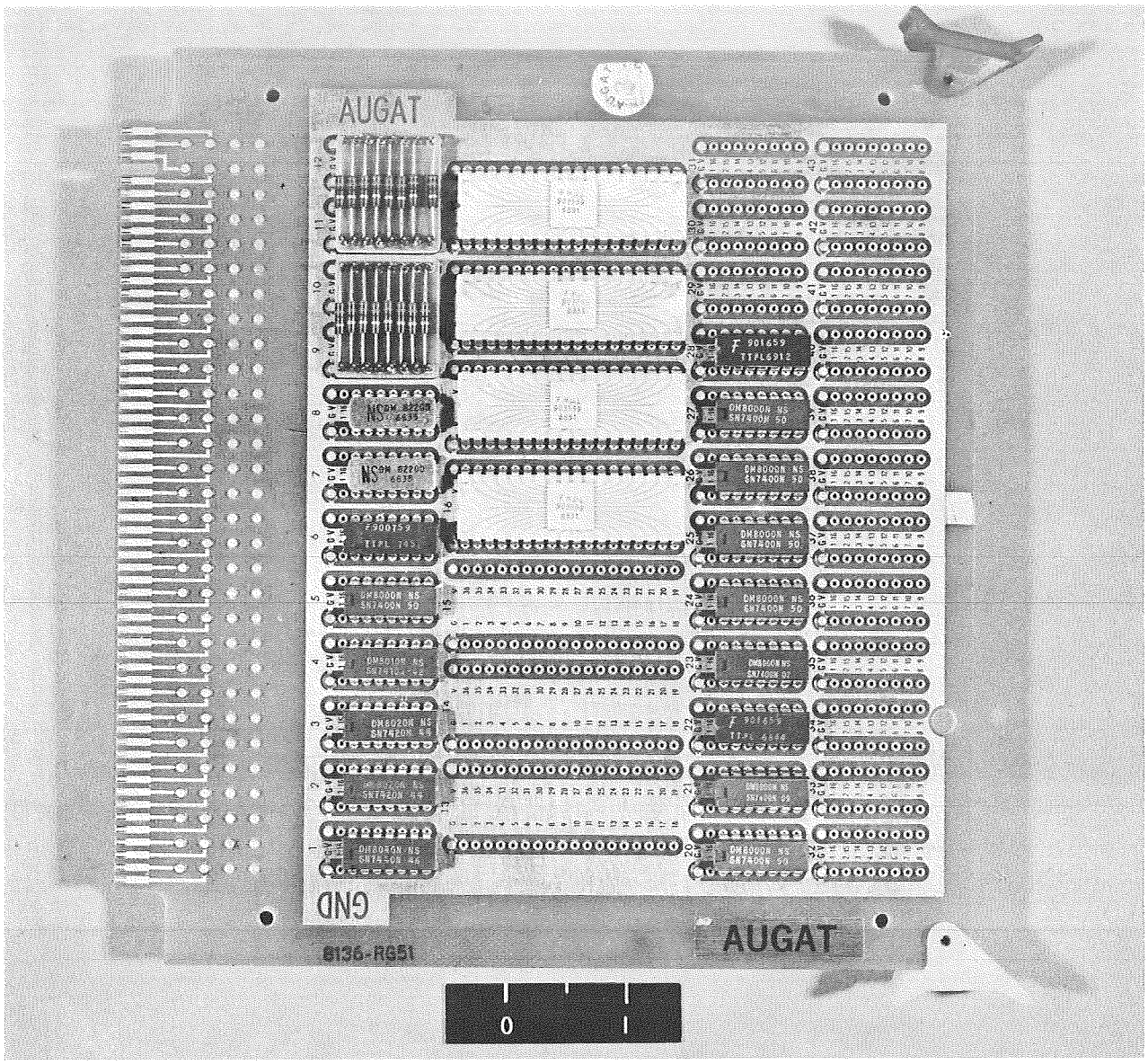

Figure 3

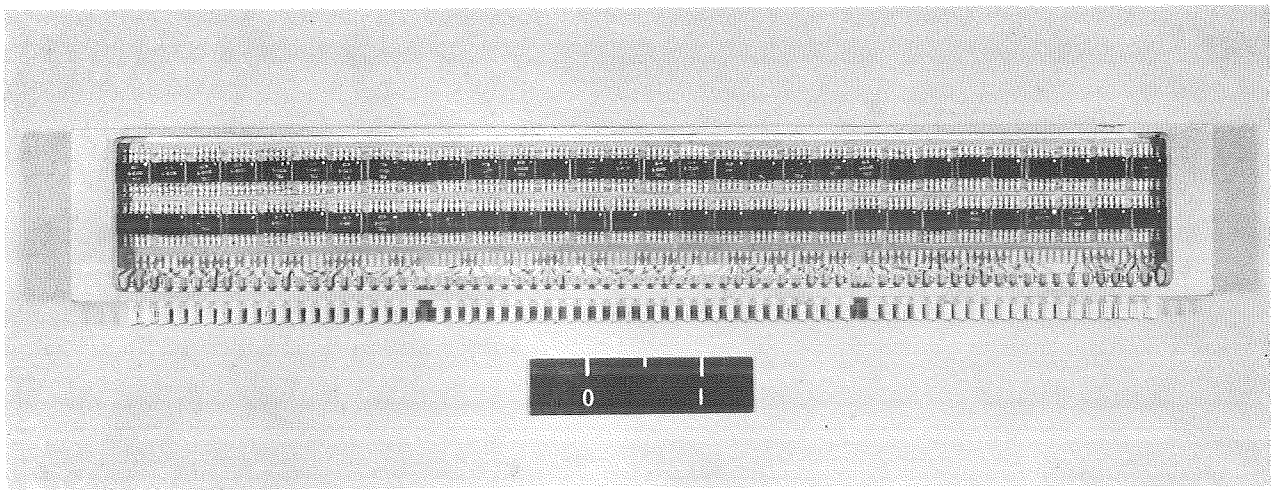

Figure 4

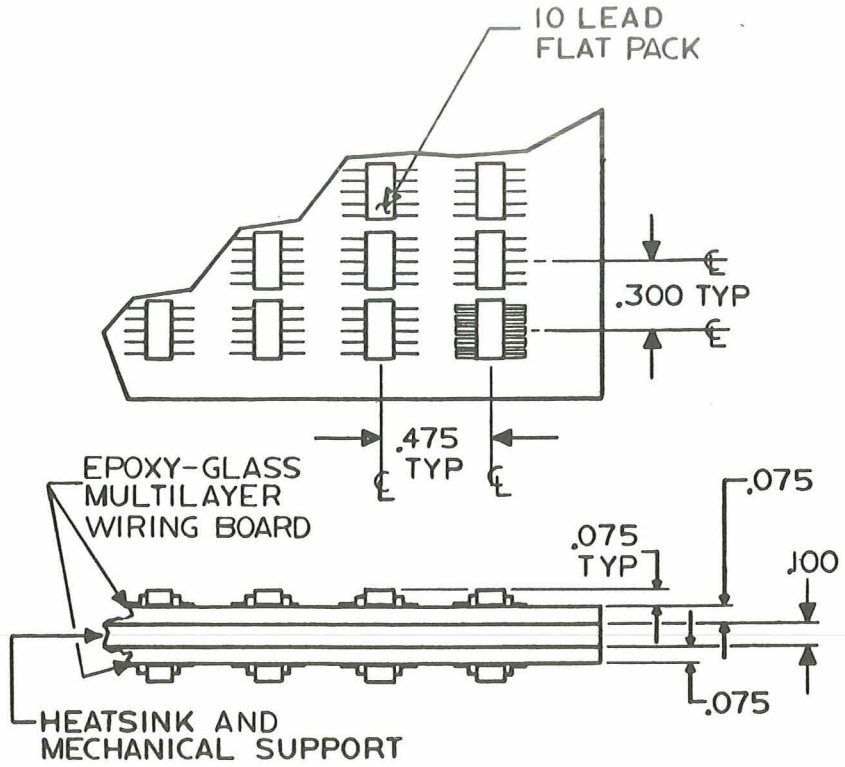

Figure 5 Schematic of ten lead flat packs containing dual nor gates interconnected using an epoxy-glass multilayer wiring board.

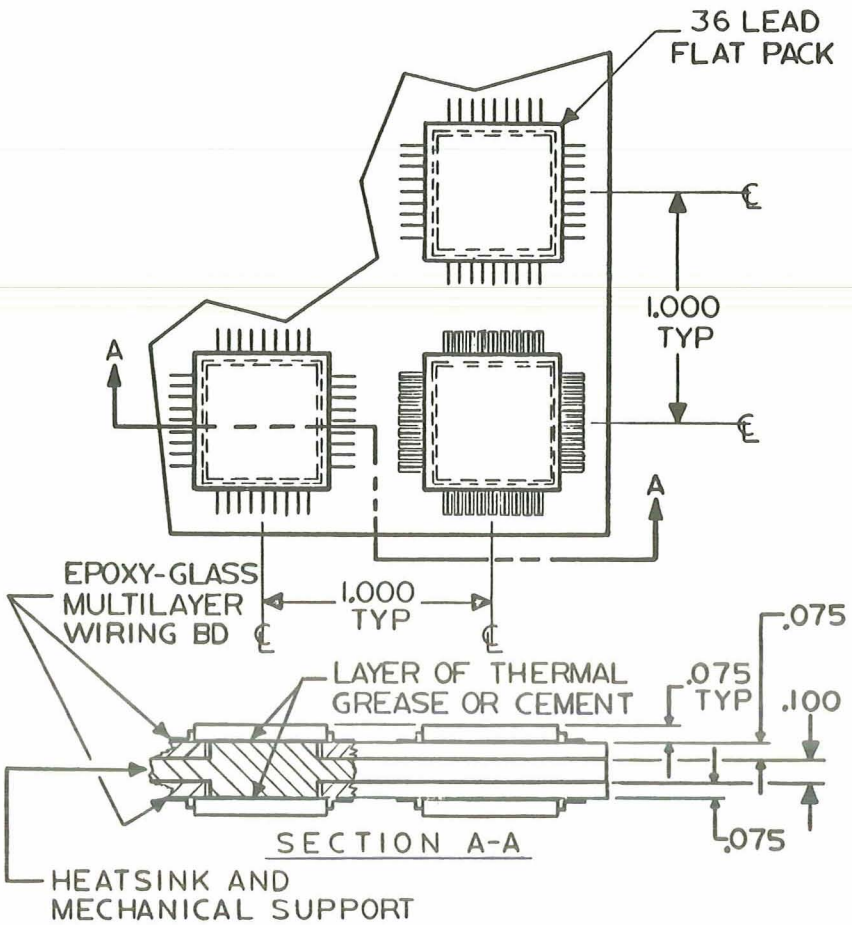

Figure 6 Schematic of thirty-six lead flat packs containing LSI (≧ 100 gate equivalent) interconnected using an epoxy-glass multilayer wiring board.

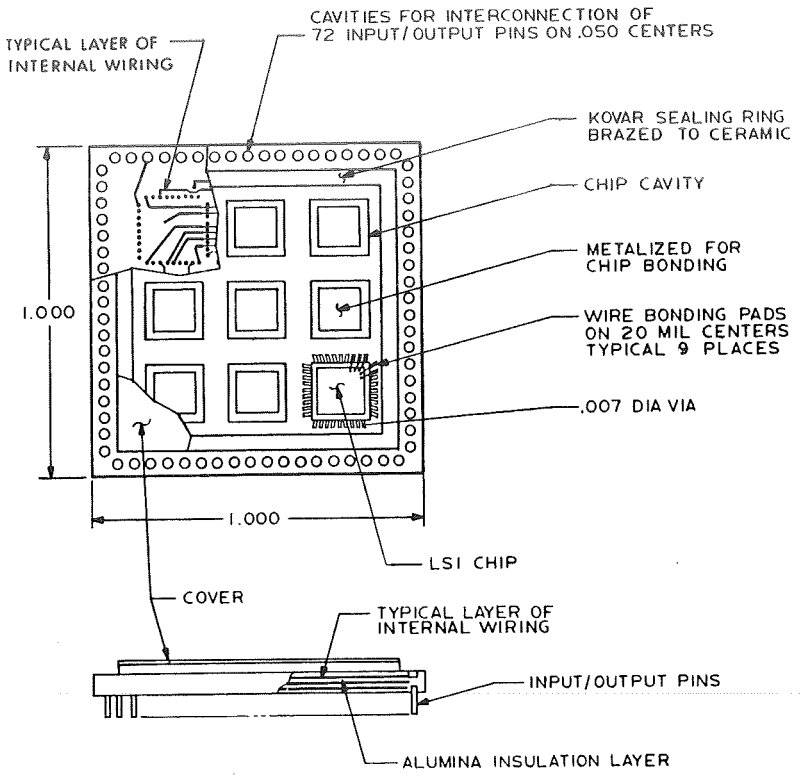

Figure 7 Ceramic multilayer wiring board package for interconnecting and packaging LSI circuits.

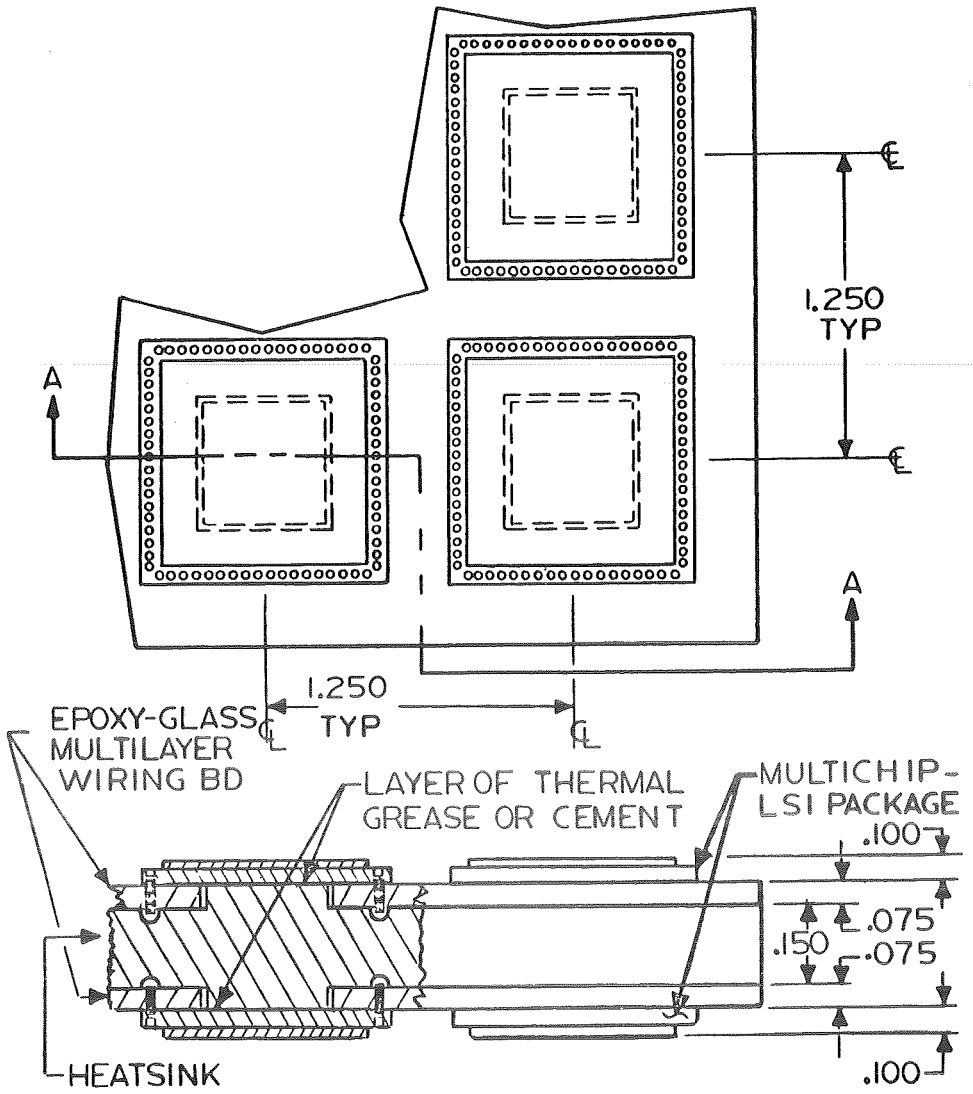

Figure 8 Multichip-LSI packages soldered directly into an epoxy-glass multilayer wiring board.

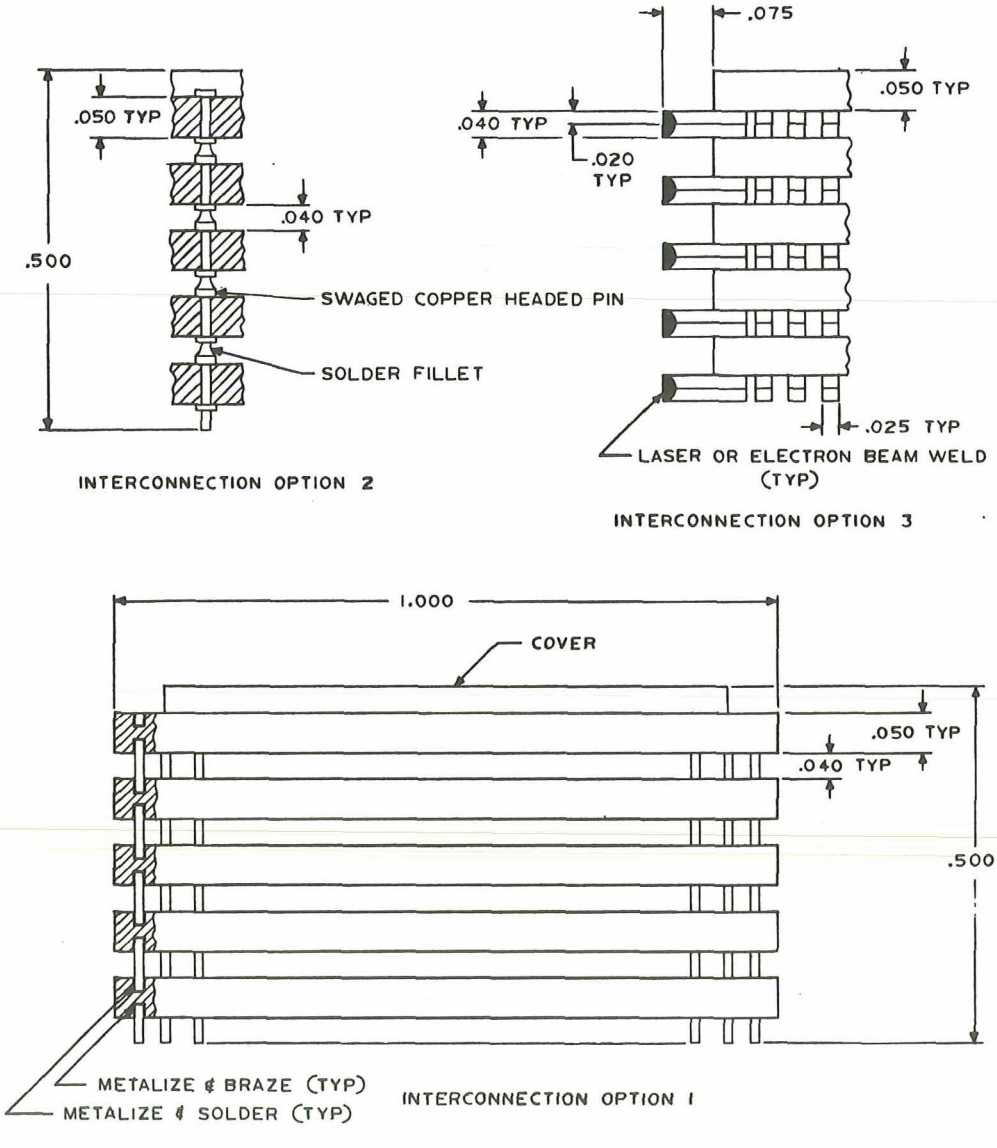

Figure 9 Module formed by stacking and joining five multichip-LSI packages.

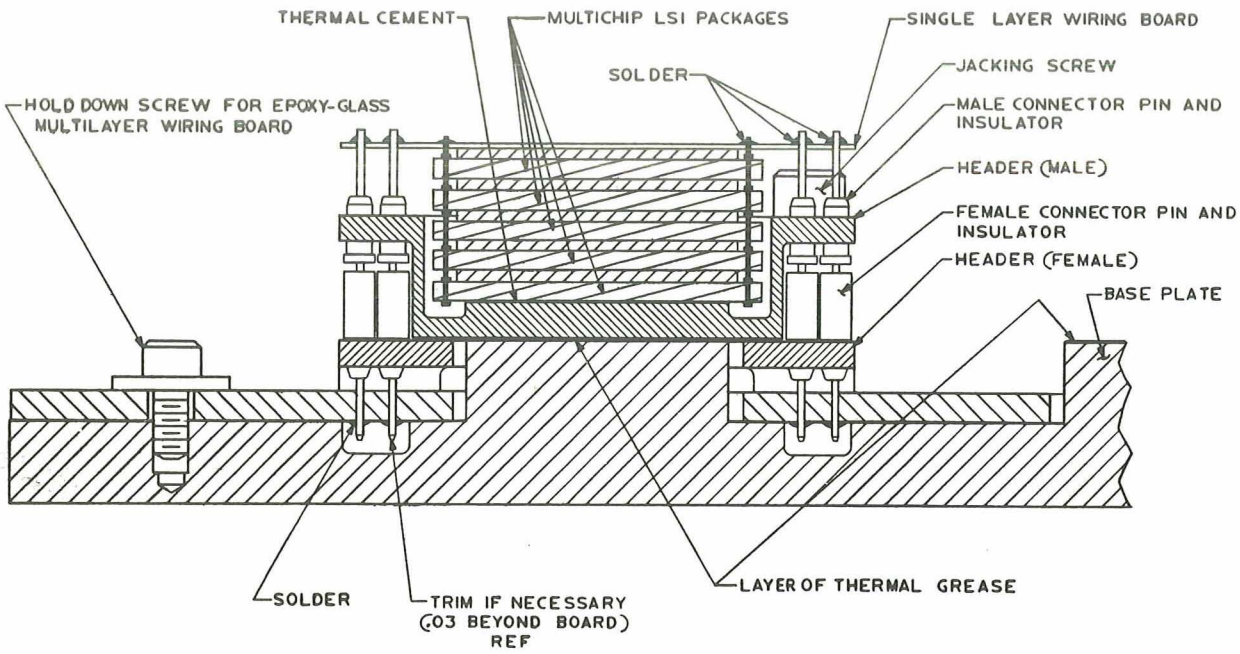

Figure 10 Module (made from five multichip-LSI packages) plus connector interconnected using an epoxy-glass multilayer wiring board.

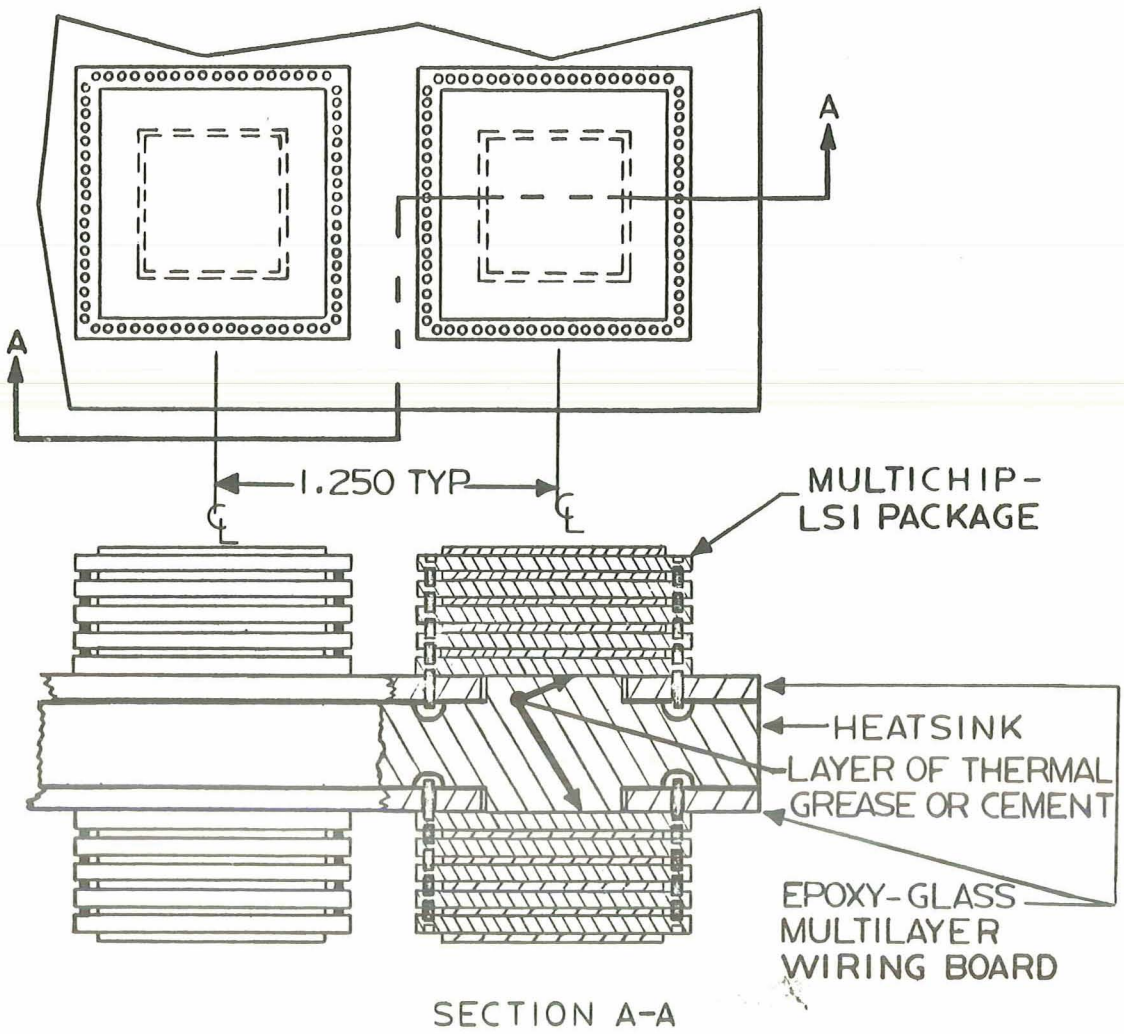

Figure 11 Module (made from five multichip-LSI packages) soldered directly into an epoxy-glass multilayer wiring board.