VOLUME I

FINAL ENGINEERING REPORT for

PLASMA PROBE C, D&E

prepared for

NASA/AMES RESEARCH CENTER

(Contract No. NAS 2 3374)

14

TIME-ZERO corporation
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FINAL ENGINEERING REPORT

PLASMA PROBE C, D & E

CONTRACT NUMBER NAS 2-3374

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ABSTRACT

The Plasma Probe instrument was designed by Marshall Laboratories (now Time-Zero Corporation) for the Pioneer C, D and E spacecraft. The instrument is designed to measure ion and electron density and angular distribution in outer space.

An Electrometer Amplifier converts the negative and positive ion flux collected on its target to a bipolar signal proportional to the energy per unit charge as determined by the optic electro-static potential, solar wind flux, and direction. The output is dc-compressed at 2/3 of full scale input to keep the output swing to a reasonable value in measuring 5 magnitudes of signal range. Output is 3.2 millivolts for $1x10^{-14}$ amperes, approximately 7 volts for $2x10^{-11}$ amperes, and 21.5 volts for 10^{-9} amperes. The output is positive for negative particles (limited to 10^{-10} amperes) and negative for positive ions.

A Compression and Pulse Width Modulator performs a linear logarithmic compression on the piece-wise linear output of the electrometer amplifier. The output of this section is a pulse width modulated signal logarithmically proportional to the input flux. Maximum pulse width is equal to minimum flux and minimum pulse width is equal to maximum flux.

An A/D converter converts the pulse width modulated signal into a 7 bit binary word. It also converts the High Voltage Analog into a logarithmically compressed 7 bit binary number.

The Target Programmer logically controls the 3 targets and related information into other subsystems.

The Sector Programmer's primary function is to divide the spacecraft revolution into 128 (7bit) equal segments. It also furnishes section timing signals to other subsystems.

The Timing and Control section provides all central timing, control and mode signals for the instrument.

The Buffer Storage subsection provides temporary storage of input data to meet the telemetry readout rate.

The High Voltage Programmer controls the High Voltage Power Supply and provides 7 cycles of 30 ion reference steps and one cycle of 15 electron reference steps. It also programs the suppression voltage requirements.

The High Voltage Power Supply generates the balanced stepping high voltage for the analyzer plates in the optics section. It also provides all suppression and related voltages.

The Low Voltage Power Supply converts the spacecraft 28 volts into the required instrument voltages.

Ground Support Equipment (GSE) has been designed to stimulate the spacecraft electronics normally interfacing with the Plasma Probe Instrument. The GSE provides the stimulus, timing signals, and power necessary to operate and test the flight hardware. The GSE also provides a readout capability which is synchronized to the stimulation of the sensor for measuring and recording system inputs, outputs, and performance parameters.

ILLUSTRATIONS

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

ILLUSTRATIONS (Continued)

TABLES

ABBREVIATIONS OF LOGIC SIGNALS

A/D	Analog-to-Digital
AS	Azimuth Scan
BPS	Bits per Second
BS	Buffer Storage
CCC	Cycle Counter Clock
DCSM	Duty Cycle Storage Mode
EHVC	End High Voltage Cycle
ESC	Electron Suppression Code
FHVZ	Force High Voltage Zero
HBR	High Bit Rate
HV	High Voltage
HVA	High Voltage Advance
HVPS	High Voltage Power Supply
HVSRGC	High Voltage Storage Register Gate Control
HVZ	High Voltage Zero
ISC	Ion Suppression Code
LBR	Low Bit Rate
LPWM	Logarithmic Pulse Width Modulator
LTSR	Long Term Storage Register
MCn	Mode Command Status Bit n
MFS	Maximum Flux Scan
PS	Polar Scan
PWM	Pulse Width Modulator
RLTSR	Reset Long Term Storage Register
SDMC	Sun Pulse Delayed Mode Change
SID	Suppressed Identification
S of EC	Start of Electron Cycle

1.0 INTRODUCTION

This engineering report describes the Pioneer C, D and E Plasma Probe instrument and associated Ground Support Equipment designed and fabricated by Marshall Laboratories (now Time-Zero Corporation) for Ames Research Center under NASA Contract NAS 2-3374.

The Plasma Probe instrument measures solar plasma charged particles in terms of flux, corresponding to energy level and incident direction of travel. This flux is detected by optical sensors and is converted to analog signals proportional to energy per unit charge.

1.1 Scope

The report covers the electrical, mechanical, and thermal design of the instrument. Also included is the Ground Support Equipment description, new technology, test results, problem areas, and recommendations.

The Appendix contains pertinent stress analysis, worst case design analysis, description of IC logic, and other appropriate supplemental material.

For clarity and convenience, the electrical description portion of this report is divided into three sections:

a. General Description (Section 2.0)
   This section consists of a general discussion of the instrument's main features and interfaces.
b. System Description (Section 3.0)
   This section is primarily concerned with a more detailed description of instrument operation.

This will include logic networks, sensor mechanics, transfer functions, and information flow between circuit "blocks" without going into detailed circuit analysis.

c. Circuit Description (Section 4.0)
Detailed circuit operation is presented in this section.

1.2 Delivered Units

The following units of Plasma Probe Experiment Model Number ML304-1 were designed, fabricated, tested and delivered:

a. Engineering Prototype, Serial Number 8C05-1
b. Flight 1 Instrument, Serial Number 8C05-2
c. Flight 2 Instrument, Serial Number 8C05-3
d. Flight 3 Instrument, Serial Number 8C05-4

Two sets of Ground Support Equipment were also designed, fabricated, tested and delivered.

2.0 GENERAL DESCRIPTION

The Plasma Probe Instrument is designed to measure ion and electron density and angular distribution in outer space. This flux is detected by optical targets and converted to analog signals whose amplitudes are proportional to the energy per unit charge as determined by the optics electrostatic potential and the solar wind flux and direction.

The input amplifier capability ranges from 1×10^{-14} amps to 1×10^{-9} amps.

This and other pertinent data is arranged in a particular digital format for transmission to earth. This can be seen in Figure 2.0-1, Data Format.

FRAME / BITS	BR 512 & 256					BR 64,16,8 ELECTRON MODE										BR 64,16,8 ION MODE													
	1	2	3	4	5	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
1																														
2	FR'S	FR'S	FR'S	FR'S	FR'S	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR	FR
3	1,6	2,7	3,8	4,9	5,10	1	2	3	4	5	6	7	8	9	10	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
4	& 11	& 12	& 13	& 14	& 15																									
5	HVP	BR	MC1	IFC	SG1	HVP	SG1	SG1	SG1	SG1	HVP	BR	MC1	IFC	SG1	HVP	SG1	SG1	SG1	SG1	HVP	SG1	SG1	SG1	SG1	HVP	BR	MC1	IFC	SG1
6	SID	SCS	MC2	DCSM	SG2	SID	SG2	SG2	SG2	SG2	SID	SCS	MC2	DCSM	SG2	SID	SG2	SG2	SG2	SG2	SID	SG2	SG2	SG2	SG2	SID	SCS	MC2	DCSM	SG2
7																														
8																														
9		HV	AS	AS	AS							HV	AS	AS	AS												HV	AS	AS	AS
10			6	12	18								6	12	18													6	12	18
11																														
12																														
13	PS					MF	MF	MF	MF	MF	PS					MF	MF	MF	MF	MF	MF	MF	MF	MF	MF	PS				
14	2					1	4	7	10	13	2					1	4	7	10	13	16	19	22	25	28	2				
15																														
16		AS	AS	AS	AS							AS	AS	AS	AS												AS	AS	AS	AS
17		1	7	13	19							1	7	13	19												1	7	13	19
18																														
19																														
20																														
21																														
22																														
23		AS	AS	AS	AS							AS	AS	AS	AS												AS	AS	AS	AS
24		2	8	14	20							2	8	14	20												2	8	14	20
25																														
26																														
27	PS					MF	MF	MF	MF	MF	PS					MF	MF	MF	MF	MF	MF	MF	MF	MF	MF	PS				
28	1					2	5	8	11	14	1					2	5	8	11	14	17	20	23	26	29	1				
29																														
30		AS	AS	AS	AS							AS	AS	AS	AS												AS	AS	AS	AS
31		3	9	15	21							3	9	15	21												3	9	15	21
32																														
33																														
34																														
35																														
36																														
37		AS	AS	AS	AS							AS	AS	AS	AS												AS	AS	AS	AS
38		4	10	16	22							4	10	16	22												4	10	16	22
39																														
40																														
41	PS					MF	MF	MF	MF	MF	PS					MF	MF	MF	MF	MF	MF	MF	MF	MF	MF	PS				
42	3					3	6	9	12	15	3					3	6	9	12	15	18	21	24	27	30	3				
43																														
44		AS	AS	AS	AS							AS	AS	AS	AS												AS	AS	AS	AS
45		5	11	17	23							5	11	17	23												5	11	17	23
46																														
47																														
48																														

FOLDOUT FRAME 1

FOLDOUT FRAME 2

Figure 2.0-1 Data Format

NOTES to Figure 2.0-1, Data Format:

SCS: Sector Command Status
HVP: High Voltage Polarity
SID: Suppression ID
MC1, 2: Sup. Mode Command Status
IFC: In Flight Cal Status
SG 1, 2: Sector Generator Status
BR: Bit Rate
DCSM: Duty Cycle Storage Mode

ELECTRON MODE:

MF 1 to MF 15 14 Electron steps plus zero step

POSITIVE ION MODE:

MF 1 to MF 30 30 Ion steps

DEFINITIONS:

DCSM:	1 for DCSM	PS 1:	Bottom target data
	0 for normal operation	PS 2:	Center target data
HVP:	1 for Ion Mode	PS 3:	Top target data
	0 for Electron Mode		
SID:	0 for unsuppressed		
	1 for suppressed		
BR:	1 for High Bit Rate (512 BR, 256 BR)		
	0 for Low Bit Rate		
MC 1, 2:	$\begin{matrix}0\\0\end{matrix}$ for unsuppressed		
	$\begin{matrix}0\\1\end{matrix}$ for suppressed		
	$\begin{matrix}1\\1\end{matrix}$ for Automatic Suppression		
IFC:	1 for IFC on		
	0 for IFC off		
SG 1, 2:	1 for Fast (Lead Sun pulse)		
	0 for Slow (Lag Sun pulse)		
SCS:	1 for normal operation		
	0 for delayed Sector Gen.		

The other data includes High Voltage polarity (to identify positive or negative particle measurement), section information, bit rate (to identify message format), suppression mode, calibration status, and certain other information pertaining to the operation of the instrument.

The spacecraft, using a sun sensor, generates a pulse for each revolution of the spacecraft. The Sun Pulse occurs at a nominal rate of 60 ppm, but the rate can range from 54 to 80 ppm. This Sun Pulse is the basic timing signal for the operation of the instrument. Using this Sun Pulse repetition rate, the instrument divides each revolution of the spacecraft into 128 equal angels called Sectors.

Three techniques are used for collecting flux data:

a. Polar Scan (PS), during which all three targets are used. The instrument detects the sector in which a maximum flux was measured, and the amplitude of this flux at each target.

b. Azimuthal Scan (AS), during which the instrument is programmed to detect the flux collected by the center target at each of 23 particular sectors out of the 128 equal intervals. See Figure 2.0-2 for the Azimuthal Scan Diagram. The shaded areas show the AS Sectors.

c. Maximum Flux Scan (MFS), which is similar to the Polar Scan. Here, the amplitude of the flux collected only by the center target is measured. The amplitude of the maximum flux during each revolution and the sector in which it occurs are detected.

Ion measurements are made at each of thirty levels of analyzer voltage while electrons are measured at each of 15 levels.

When data is transmitted at high bit rates (512 or 256 BPS), one PS and AS is made for each level of high voltage.

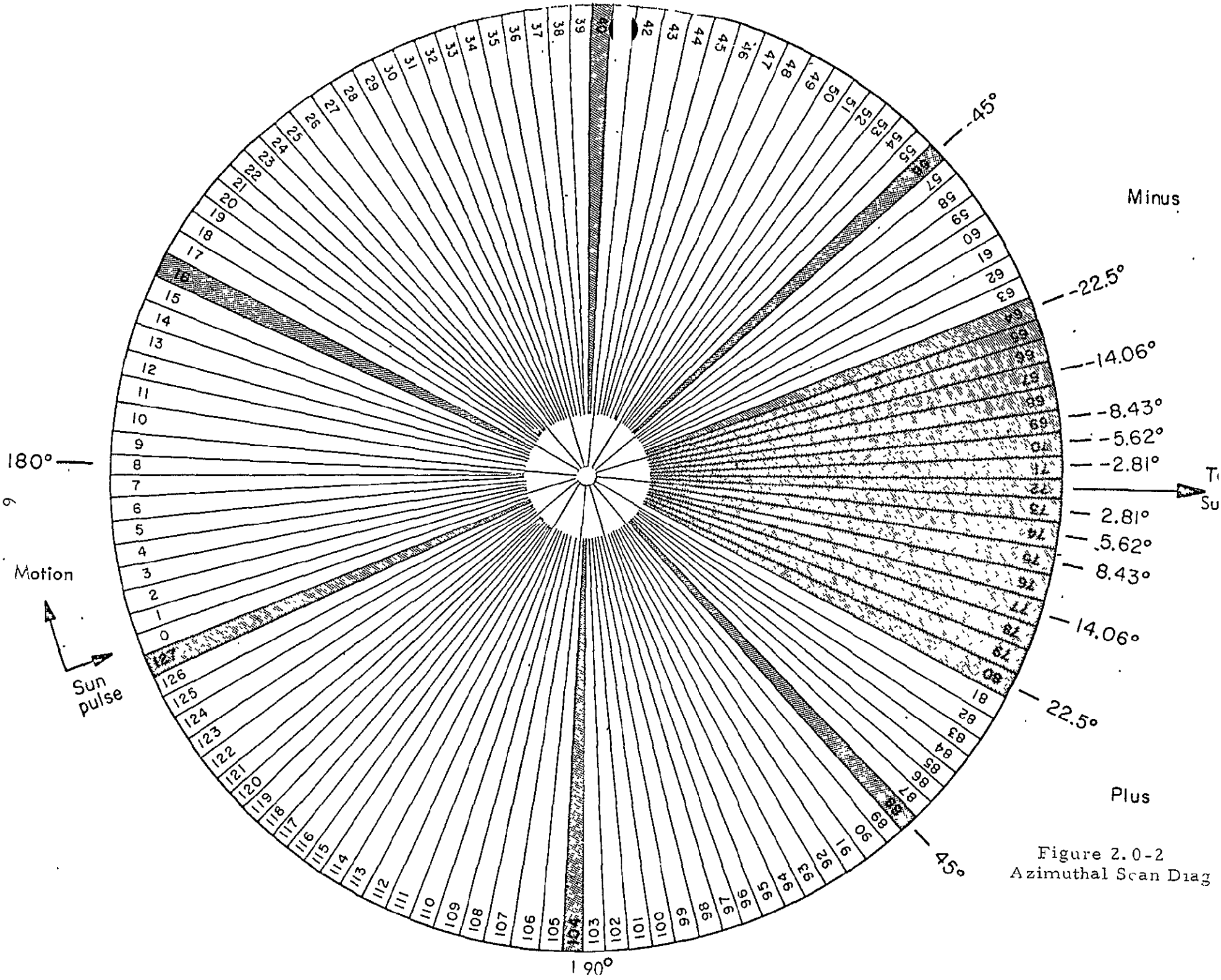


Figure 2.0-2
Azimuthal Scan Diag

At low bit rates (64, 16 or 8 BPS or Duty Cycle Storage Mode-DCSM), one MFS is made for each level of analyzer voltage. After the last voltage step during an Ion cycle, the analyzer voltage is set to that level at which the maximum flux was detected; then one PS and one AS is made.

After the last analyzer voltage step of an Electron cycle, the analyzer voltage is set to the level of the seventh step, and one PS and one AS is made.

Therefore, during high bit rate, in Ion mode, the instrument makes one PS during one revolution and one AS during the next revolution for each of thirty analyzer voltage levels. At a nominal Sun Pulse rate of 60 ppm, 60 seconds are required for one Ion cycle.

During electron mode, the same sequence occurs for each of fifteen levels of high voltage. At the nominal Sun Pulse rate, 30 seconds are required for an electron cycle.

At low bit rates, during Ion mode, the instrument makes one MFS during each revolution for each of thirty analyzer voltage levels, then one PS during an additional revolution and one AS during another revolution. This requires five revolutions minimum for each Ion cycle, which includes three stabilization periods.

During electron mode, the same sequence occurs for each of fifteen levels of analyzer voltage followed by one PS and one AS. 28 revolutions are required for an electron cycle, which includes two stabilization cycles. See Figures 2.0-3 and 2.0-4 for the HV Stepping Sequence diagrams.

The above statements regarding timing are made for explanatory purposes. Practically, these times are several seconds longer. For instance, midway through an Ion cycle the sequence is stopped and the analyzer voltage reduced to zero for two Sun Pulse periods.

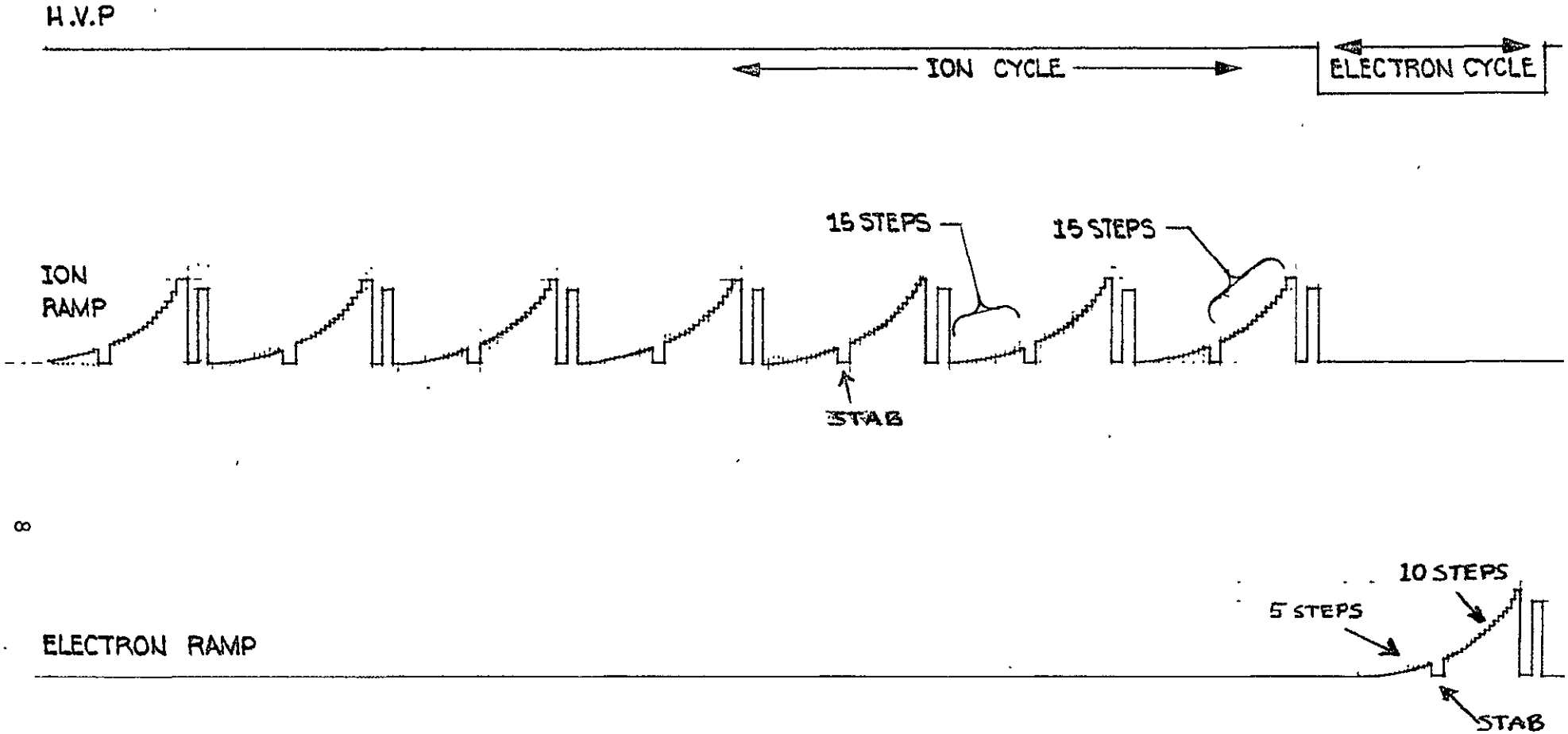


Figure 2.0-3, High Voltage Stepping Sequence, Low Bit Rate

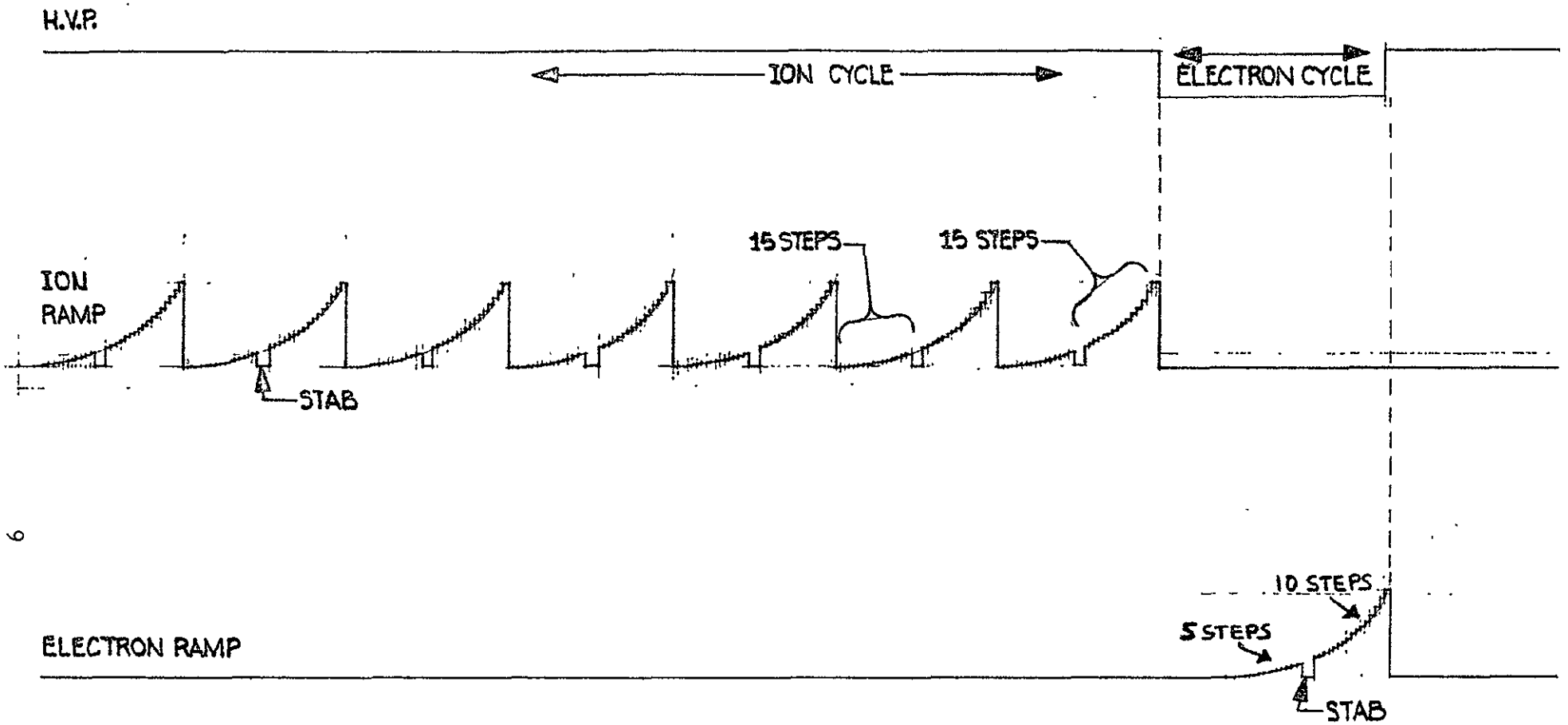


Figure 2.0-4, High Voltage Stepping Sequence, High Bit Rate

The sequence is also stopped and the analyzer voltage is reduced to zero for four Sun Pulse periods any time the suppression mode is changed, such as occurs between the fifth and sixth analyzer voltage steps of an electron cycle or between an Electron and Ion cycle. These analyzer voltage zero periods are used for stabilizing the Electrometer amplifier.

At both high and low bit rates the instrument is sequenced through seven Ion cycles, then through one Electron cycle. For the first five steps of an Electron cycle, the targets are operated with unsuppressed secondary emission and the remaining steps are in a suppressed mode.

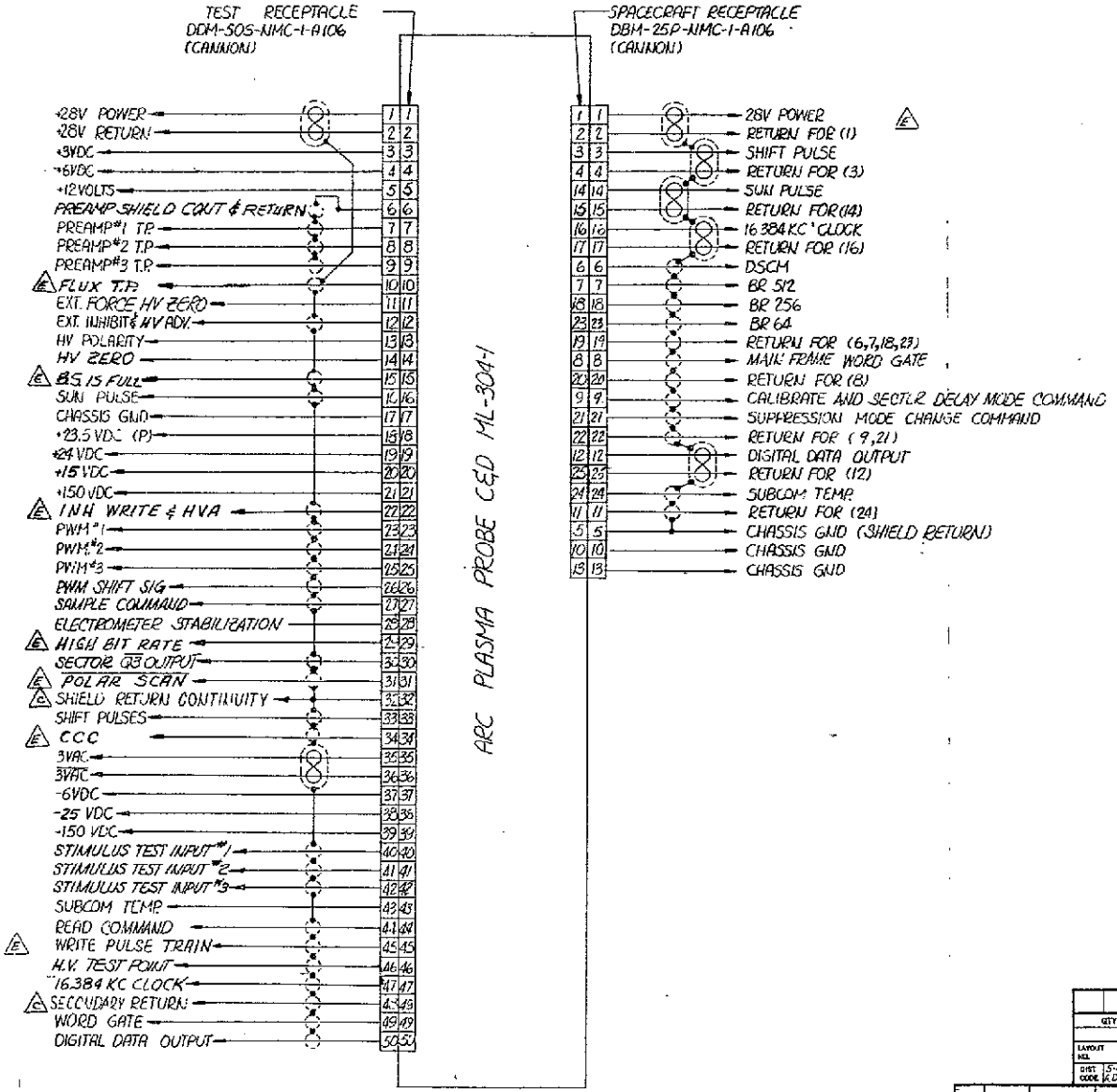
During Ion cycles, the instrument operates in one of three suppression modes. These modes are: all unsuppressed, all suppressed, and automatic suppression. During automatic suppression the first three and the last three Ion cycles are unsuppressed and the fourth Ion cycle is suppressed.

The suppression mode can be changed by Earth Command. This command can be received at any time and stored in the instrument. The command is executed at the start of the next Electron cycle.

See Figure 2.0-5 for the Electrical Interface Wiring Diagram. Appendix A shows the specification of Integrated Circuit logic used in the system.

2.1 Subsystems General Description

The instrument consists of fourteen electrical subsystems plus the Optics section. These subsections are as follows:



Electrical Interface Wiring Diagram

Figure 2.0-5

NOTES: UNLESS OTHERWISE SPECIFIED

DASH NO.	MODEL NO.	NEXT ASSEMBLY	MODEL NO.	FINAL ASSEMBLY	MODEL NO.	APPLICATION			

HL-304-1

PART NO	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	ELEC REF DES	CODE IDENT	ZONE	ITEM NO.

LIST OF MATERIALS

QTY REQD PER NOTED ASSY CONFIGURATION

LAYOUT NO.

DIST CODE A,D,E

INTERPRET THIS DRAWING PER STANDARDS IN MIL-D-70327

DIMENSIONS ARE IN INCHES

TOLERANCES ON DECIMALS: X ± 1, .XX ± .03, .XXX ± .010; ANGLES ± 0° 30'; .XXXX ± .0050

SURFACE ROUGHNESS

HOLE DIA. TOLERANCE

.0135 THRU .125	+.004 −.001
.126 THRU .250	+.005 −.001
.251 THRU .500	+.006 −.001
.501 THRU .750	+.007 −.001
.751 THRU 1.000	+.008 −.001
1.001 THRU 2.000	+.010 −.001
2.001 AND OVER	LINEAR

CONTRACT NO. NAS2-3374

DRAWN Owen Mort. 11-7-65

CHECKED

WELDING

ELEC. ENG.

PROJ. ENG. 7 Dec 65

MFG.

DESIGN ACTIVITY APPD 12-22-65

CUSTOMER

MARSHALL LABORATORIES
TORRANCE, CALIFORNIA

TITLE: ELECTRICAL INTERFACE-WIRING DIAGRAM-ARC PLASMA PROBE PIONEER C&D

SIZE	CODE IDENT NO	DWG NO.	REV
D	13126	544001	E

SCALE — RELEASED — SHEET 1 OF 1

DASH NO.	EFF	ZONE	REV	DESCRIPTION	BY	CK	DATE	APPROVED
4	12 up		A	REVISED S/C CONN. PIN ASSIGNMENTS PER TMO-9-38				
4	15 up		B	CLARIFY CONNECTOR IDENTIFICATION				
4	1 thru 6 up		C	PIN 15 SIGNAL WAS SUN STATUS; PIN 23 SIGNAL WAS +23.5 VDC RETURN; PIN 24 SIGNAL WAS +6 VDC RETURN; PIN 32 SIGNAL WAS +6 VDC RETURN; PIN 45 SIGNAL WAS SEC SIG RETURN; SHIELD CONN. TERMINATED				
4	15 up		D	PIN 30 SIGNAL WAS SECTOR Q3 OUTPUT; PIN 28-SIGNAL WAS SPIN STABILIZATION; PIN 44 SIGNAL WAS READ OUT PULSES; PIN 45 SIGNAL WAS WRITE IN PULSES; PIN 8 SIGNAL WAS H.V. GATE; PIN 9 SIGNAL WAS CALIBRATE COMMAND; PIN 5 SIGNAL WAS CHASSIS GND; PIN 5 SHIELD CONNECTION WAS ADDED				
4	14 up		E	PIN 6 SIGNAL WAS +6 RETURN; PIN 10 SIGNAL WAS PREAMP RETURN; PIN 15 SIGNAL WAS SPARE; PIN 23 SIGNAL WAS +24 RAMP RETURN; PIN 27 SIGNAL WAS ELECTRON RAMP; PIN 31 SIGNAL WAS SECTOR GEN STATUS; PIN 34 SIGNAL WAS +6 RETURN; PIN 45 SIGNAL WAS SEC SIG RETURN				

FOLDOUT FRAME

FOLDOUT FRAME

a. Electrometer Amplifier
b. Attenuation and Pulse Width Modulator
c. Timing and Control
d. Sector Programmer
e. Target Programmer
f. High Voltage Programmer
g. Analog-to-Digital (A/D) Converter
h. Commutator
i. Status Decoder
j. Calibrate and Sector Delay
k. Buffer Storage
l. Temperature Sensor
m. High Voltage Power Supply

These sub-systems are arranged into four sub-assemblies:

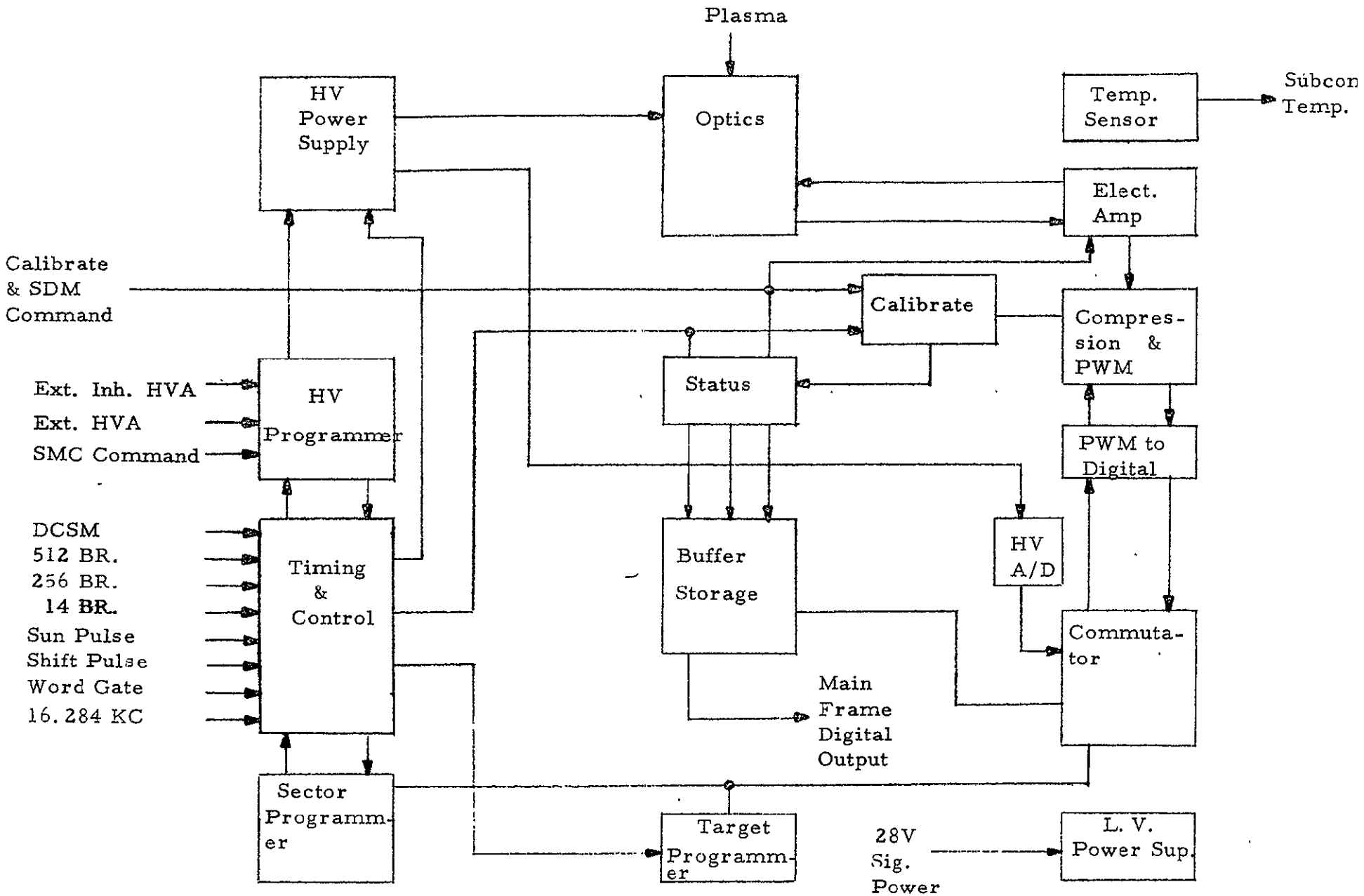
a. Electrometer Amplifier - contains the Optics, Electrometer Amplifier, and the Attenuation and Pulse Width Modulator.

b. Logic - consists of the Analog-to-Digital (A/D) Converter, Target Programmer, Sector Programmer, Timing and Control, Temperature sensor, Status Decoder, Commutator, and High Voltage Programmer.

c. Buffer Storage - contains only the Buffer Storage circuitry.

d. Power Supply - contains the high and low voltage power supplies.

A block diagram of the system is shown in Figure 2.1-1. The Interconnect Schematic can be seen in Figure 2.1-2. See Appendix B for the master drawing list, Operational Test specification, and Flight Acceptance Test Specification. Appendix C shows a typical Flight Acceptance Test Report.



Functional Block Diagram
ARC Plasma Probe
Figure 2.1-1

2.1.1 Electrometer Amplifier

2.1.1.1 Optics

The Optics consist of two concentric spherical analyzer plates that, when properly biased, produce an electrostatic field. Ions entering this field are deflected, and only those having a pre-determined $\frac{E}{Q}$ range can reach the current detectors.

2.1.1.2 Electrometer

Each target is connected to a current amplifier. The amplifier produces a positive output voltage for negative particle inputs, and a negative output voltage for positive particle inputs.

Range of operation is $1x10^{-14}$ amperes to $1x10^{-9}$ amperes for the input, and 0.0032 volts to 21.5 volts for the output. The amplifier has been designed to minimize noise, drift, and response time, and to ensure reliable operation for the life of the instrument.

2.1.1.3 Attenuation and Pulse Width Modulation

The output of the Electrometer is compressed at high levels of input current. This compression is unfolded by the Logarithmic Pulse Width Modulator (LPWM), which produces an output pulse whose width is a logarithmic function of the amplitude of Electrometer input current.

2.1.2 Logic

2.1.2.1 Timing and Control

This subsystem generates the basic timing and control signals for operation of the instrument logic. It receives and executes command signals from external sources. On the basis of these signals, the Sector, Target, and High Voltage circuits are properly sequenced. Signals are also generated to control the A/D functions, Stabilization circuits and the Buffer Storage.

2.1.2.2 Sector Programmer

The Sector Programmer generates the basic timing which divides each revolution of the spacecraft into 128 sectors, each of which is subdivided into 16 segments. The programmer consists of a voltage controlled oscillator operating at 2048 times the Sun Pulse rate, feeding into an 11 stage ripple counter.

2.1.2.3 Target Programmer

The Target Programmer consists of two flip-flops and appropriate NOR gates. It controls the data flow of the three targets (Sector and High Voltage information).

2.1.2.4 High Voltage Programmer

The High Voltage Programmer provides the necessary signals to step the High Voltage Power Supply through thirty logarithmically increasing steps for seven cycles of ion mode followed by fifteen such steps for one cycle of electron mode. Dump and Stabilization is forced every fifteen steps regardless of spin rate or bit rate.

The minimum time between Stabilization commands is 11.25 seconds at 80 RPM in Low Bit Rate, and the maximum is 45 seconds at 40 RPM in High Bit Rate.

2.1.2.5 High Voltage A/D Converter

The High Voltage A/D circuit is similar to the flux A/D circuit. The high voltage level is sampled with a voltage divider and converted to a PWM signal. This in turn is converted to a digital quantity representative of the high voltage level at the time of sampling. The sampled High Voltage analog will vary, in steps, between 0 and 3000 millivolts in Electron mode, and between 40 and 3000 millivolts in Ion mode.

2.1.2.6 Commutator

The Commutator sequentially gates the digital data into an intermediate storage register from which it is then fed into the buffer storage.

2.1.2.7 Status Decoder

The Status Decoder produces one-or-two-bit words which give information relating to the operation of the instrument.

2.1.2.8 Calibrate and Sector Delay Mode

Upon receipt of the Calibrate Command from the Earth Station, two operations occur within the instrument. First, the internally generated Sun Pulse is delayed from the actual Sun Pulse for a period equivalent to four sectors. Whereas, in normal azimuthal scan flux is measured in each of 23 preselected sectors, these measurements are made 4 sectors later when the Sun Pulse is delayed. Secondly, the flux comparators are forced to generate data representing 1/2 full scale flux.

The Comparator calibration is disabled and normal measurements resumed at the start of the next Electron cycle. The internal Sun Pulse returns to the non-delayed condition upon receipt of the next Calibrate Command.

2.1.2.9 Temperature Sensor

The Temperature Sensor consists of a close-tolerance thermistor and a differential amplifier. This amplifier provides a d-c output voltage as a linear function of ambient temperature.

2.1.3 Buffer Storage

The Buffer Storage consists of a core plane with appropriate Read and Write address circuits and counters. The flux and sector data and other information is entered into the core plane in specific locations. This information is read out at a rate which is dictated by telemetry requirements and in a manner corresponding to the message format.

The counters are controlled by the Buffer Logic although the storage unit supplies signals which prevent the Read counters from overtaking the Write counters. Signals are also provided to prevent writing into the core plane sections that have not been read out.

Digital data is also generated which identifies the frames being read out.

2.1.4 Power Supplies

The primary input power to the instrument is an unregulated +28 volts d-c. From this the various voltage sources are developed.

2.1.4.1 Low Voltage Power Supply

The Low Voltage Power Supply furnishes the following well regulated voltages:

a.	+6V	$\pm$0.1%
b.	+12V	$\pm$0.2%
c.	+15V	$\pm$0.2%
d.	-6V	$\pm$0.1%
e.	-25V	$\pm$0.2%

In addition, a 3.3 volts 5KHz square wave is generated to provide filament power for the Electrometer tube and excitation for the chopper.

2.1.4.2 High Voltage Power Supply

The Suppression voltage supplies are +150 and -150 volts, unregulated. The analyzer plate power supply is programmable and provides plus and minus 17.5 to 1250 volts in 30 logarithmic steps during Ion mode.

In Electron mode, the supply provides plus and minus 1.166 to 83.3 volts in 15 logarithmic steps.

3.0 ELECTRICAL SYSTEM DESCRIPTION

3.1 Electrometer Amplifier and Optics

3.1.1 Optics

Refer to Figure 3.1.1-1 for the Optics configuration.

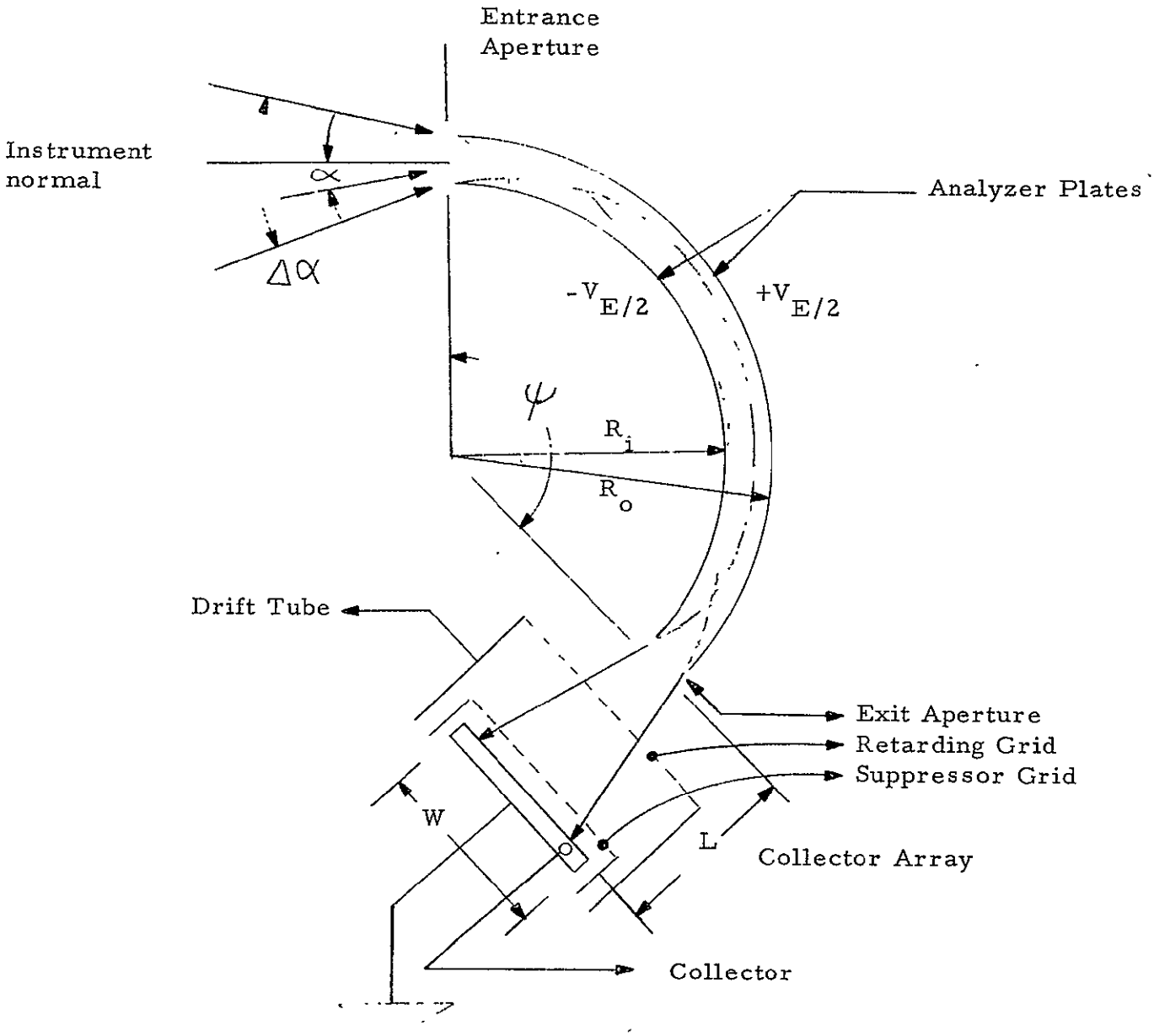
The voltage V_E is applied across the analyzer plates to produce an electrostatic field. The force field (charged particles entering the optics) deflect and only those ions within a range of specific $\frac{E}{Q}$ values can reach a set of current detectors. With a spherical analyzer geometry, the potential between the plates is given by the expression,

$$V_{(r)} = \frac{-V_E}{(R_o - R_i)} \left[\frac{R_o R_i}{r} - \frac{R_o + R_i}{2} \right]$$

where R_o and R_i are the inner and outer plate radii, respectively, and $V_{(r)}$ is the potential difference between the analyzer plates. For ions, the outer plate has a potential of $+V_E/2$, and the inner plate a potential of $-V_E/2$.

The potential energy of an ion between the plates is $Q\,V_{(r)} = U_{(r)}$ where Q is the ion charge. Since the analyzer plate system is spherical, the ions follow elliptical orbits while in the electrostatic field. This is a conservative system neglecting fringe field effects; thus the total energy and angular momentum of the ion is constant.

For a given potential V_r and analyzer plate geometry (R_o, R_i and ψ), the range of possible orbits through the system is limited in both speed (v) and angle of incidence. Thus the analyzer configuration defines the speed and the angular range for a given ion species.



Optics Configuration
Figure 3.1.1-1

A figure that defines the analyzer system is the analyzer constant K_A, where

$$K_A = \frac{E/Q \text{ nom}}{V_E} ,$$

the ratio of nominal acceptance energy to applied analyzer voltage.

The maximum ion density collected by the optics is dependent upon the shape of the entrance aperture, the angle ψ of the analyzer plates, the location of the collectors below the exit aperture, and the angular position and size of the current collectors.

$$V_{(r)} = \frac{-V_E}{(R_o - R_i)} \left[\frac{R_o R_i}{r} - \frac{R_o R_1}{2} \right]$$

$$E = \frac{1}{2} mv^2, \; 1 = \frac{1}{2} mv^2_{(r)} + q V_{(r)} \text{ conservation of energy}$$

At boundary condition

$$\frac{mv_i \cos}{v_i} = \frac{mv_{(r)}}{r} \cos \alpha$$

See Figure 3.1.1-2, Boundary Conditions at Entrance Aperture.

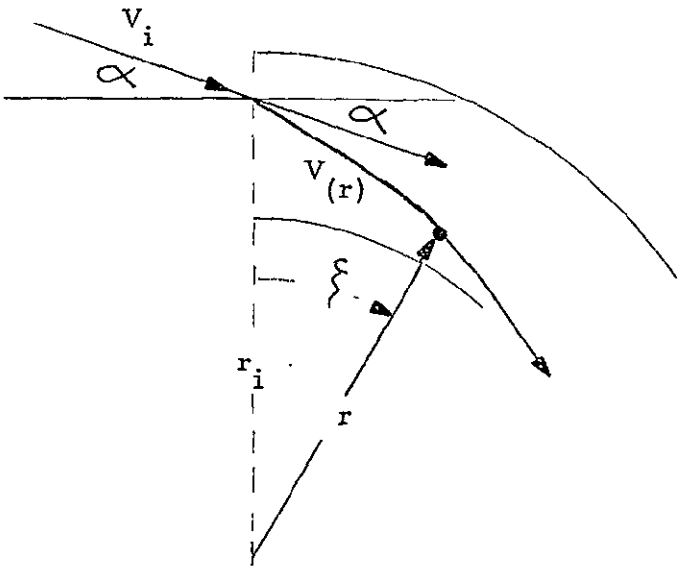


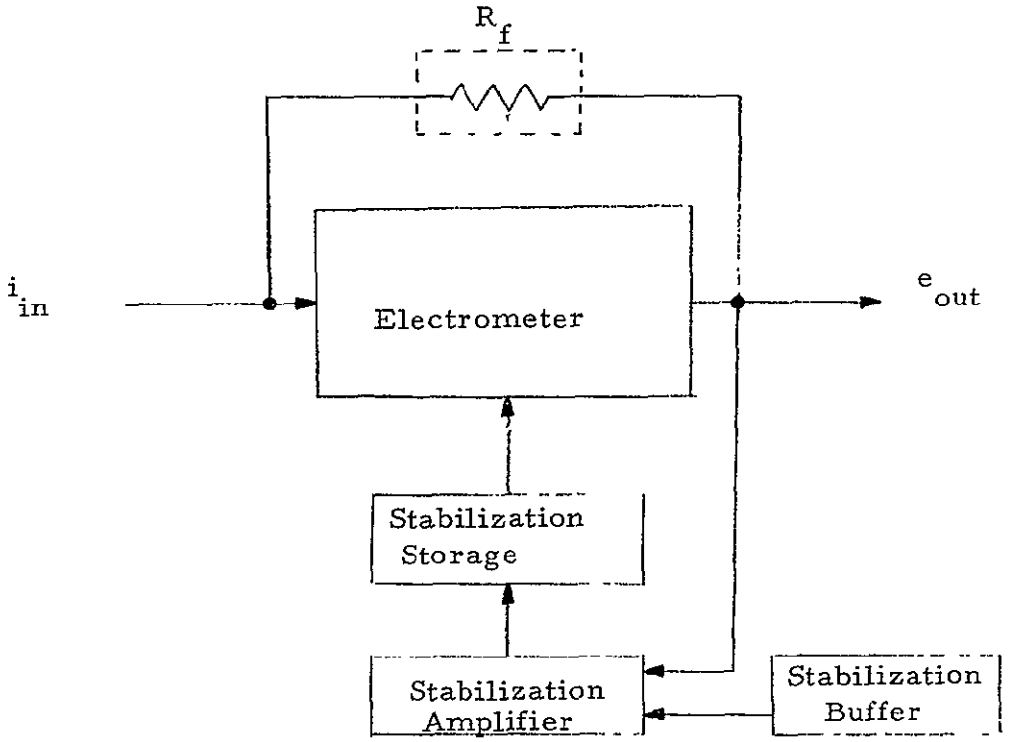
Figure 3.1.1-2, BOUNDARY CONDITIONS AT ENTRANCE APERTURE

3.1.2 Electrometer

See Figure 3.1.2-1 for a simplified block diagram of the Electrometer. The input stage and the heart of the system is an 8520 Electrometer tube manufactured by Raytheon. The selection of this tube was based upon a survey of existing electrometer tubes. The 8520 is superior with respect to grid leakage, stable characteristics in both launch and space environment, low power, small physical size and therefore, smaller magnetic dipole moments. The characteristics of the 8520 are as follows:

Average Characteristics

	Triode, G2 connected to P	Pentode	
Filament Voltage	0.625	0.625	volts
Filament Current	10	10	mA
Plate Voltage	22.5	8	volts
Screen Grid Voltage	---	5.5	volts
Control Grid Voltage	-3.0	-2.0	volts
Plate Load Resistance	200,000	---	ohms
Plate Current	60	6	mAdc
Screen Grid Current	---	2.5	mAdc
Amplification Factor	2.2	---	---
Transconductance	70	14	mho
Voltage Gain	1.85	---	---
Maximum Control Grid Current	1×10^{-13}	---	amp
Approximate Control Grid Current	---	2×10^{-15}	amp



Electrometer Simplified Block Diagram

Figure 3.1.2-1

The tube operates at the quiescent conditions recommended by the manufacturer for optimum performance; namely, fixed cathode, plate, signal grid and filament voltage and fixed plate current. The precise operating point is achieved by adjusting the screen grid bias. In order to reduce system noise, the voltage gain of the tube is made as large as possible by minimizing the plate loading by use of an FET differential stage. The FET is biased for minimum temperature drift.

When the Electrometer is turned on, with no filament voltage applied, the amplifiers are saturated and the output of the Electrometer remains at about +10V. Upon application of the filament voltage, the tube starts conducting and the output of the Electrometer decreases steadily but does not reach zero until the screen grid potential of the tube reaches a level between 7.2 to 7.8 volts; nominally, it should be at 7.2 volts. This is done by stabilizing the system.

The stabilization is achieved in conjunction with the HV dump occurring at the end of every 15 high voltage steps and between the fifth and sixth high voltage Electron step. During the dump mode, all input signals to the Electrometer grid are removed and a logic signal (See Section 3.2.6, High Voltage Zero and Stabilization Control) present at the Stabilization Buffer activates the Stabilization Amplifier causing it to sense any offset due to internal drift in the amplifier.

The error is amplified and the output of the Stabilization Amplifier feeds into the Stabilization Storage circuit which acts as a switch and dumps enough current through a divider network to establish the correct screen grid potential required for lowest zero offset. The output of the Electrometer is d-c compressed at 2/3 of full scale to keep the output swing to a reasonable value in measuring 5 magnitudes of signal.

Refer to Figures 3.1.2.-2 and 3.1.2-3 for a plot of the Electrometer transfer functions for Ion mode and Electron mode, respectively.

The transfer characteristics of the Electrometer at this region follows basically the expression

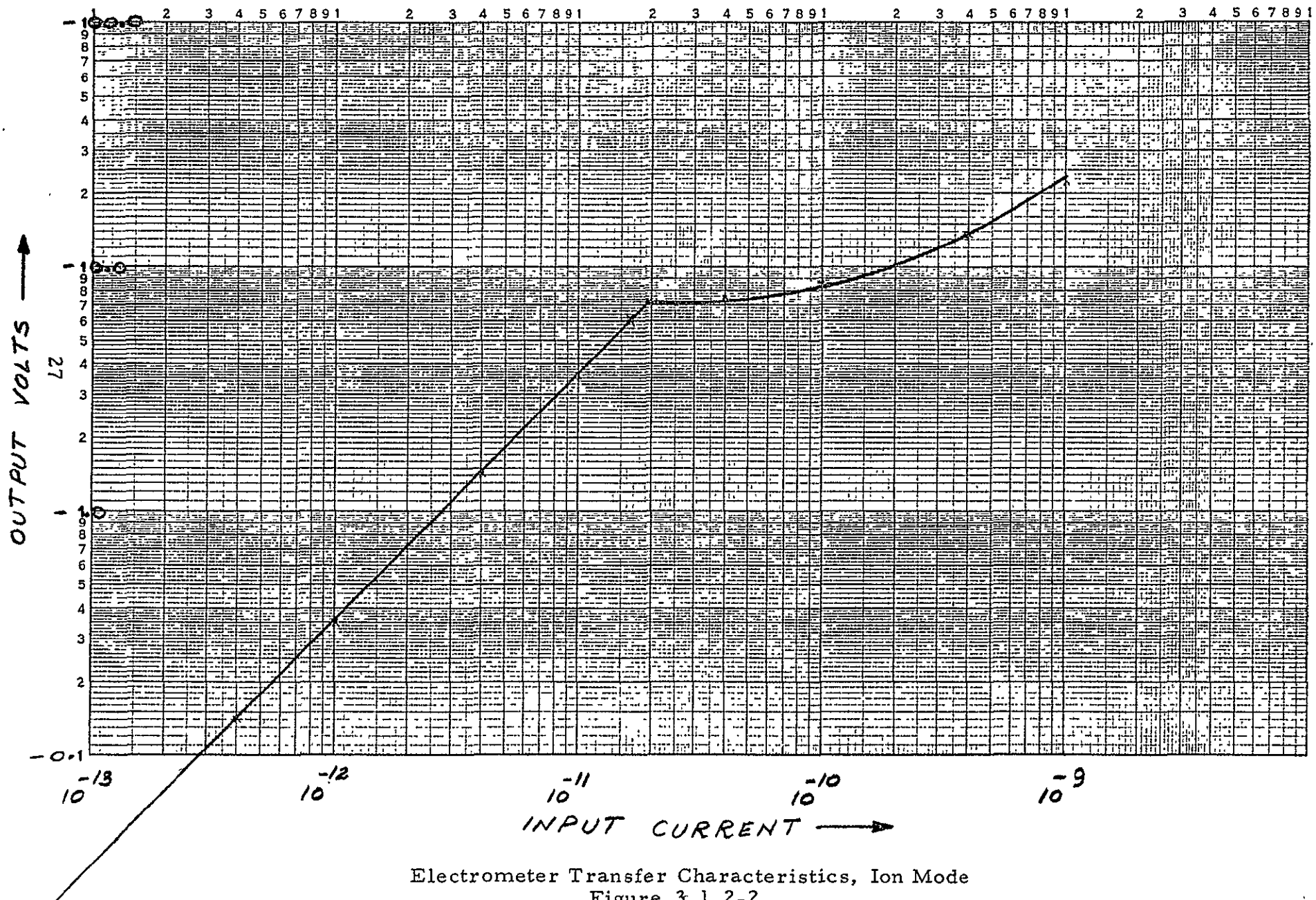
$$E_o = R_f \times I_{in} + V_z$$

which shows that output voltage is a function of the feedback resistor plus the zener breakdown voltage. Below the 2/3 region the transfer characteristic is

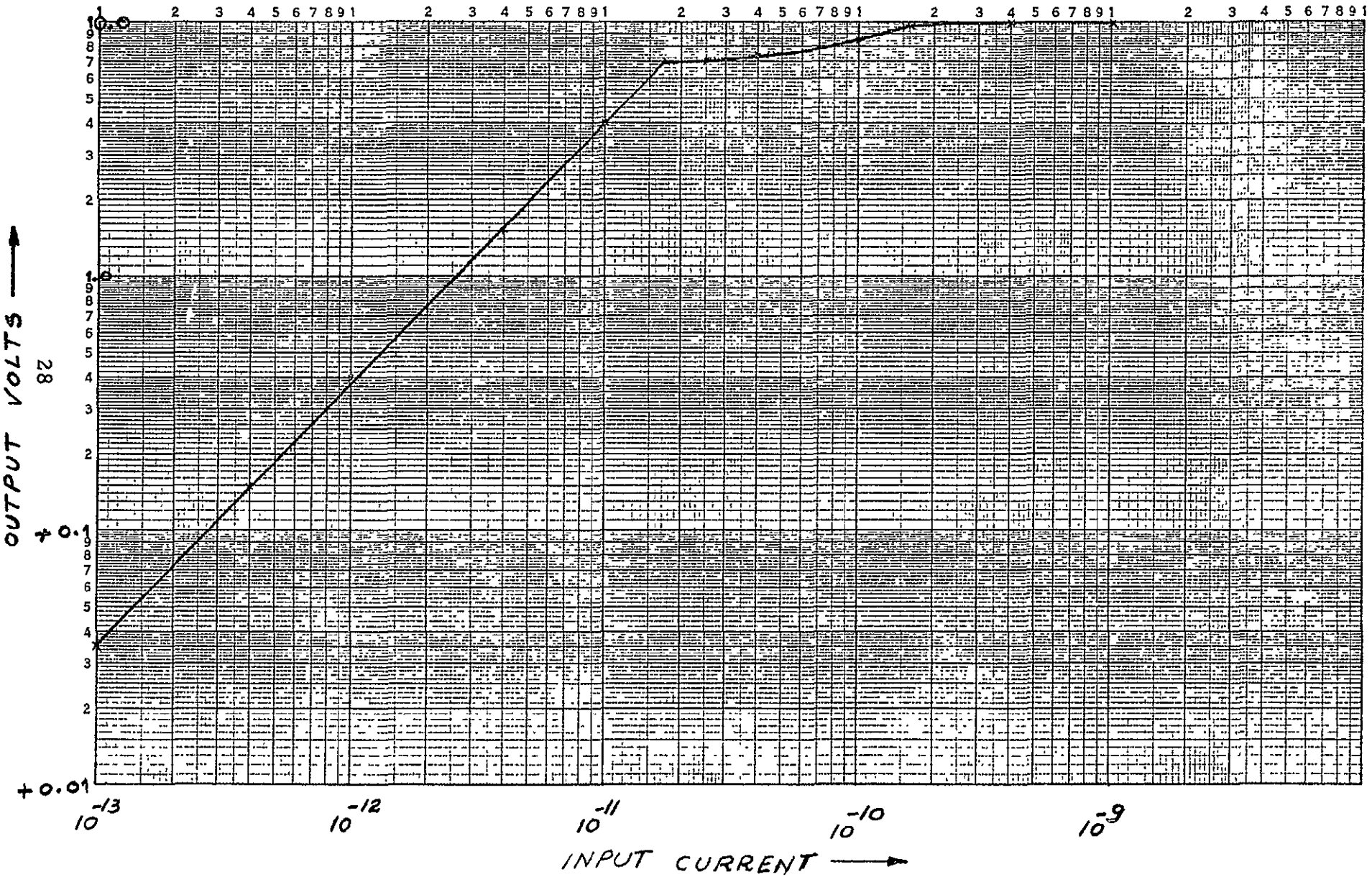
$$E_o = R_f \times I_{in} \times 22$$

Figure 3.1.2-4 shows an equivalent circuit of the Electrometer for analysis purposes. The ratio of R1 to R2 is 22. This network, together with the zener diode and the shielded feedback resistor $R_f (1.5 \times 10^{10} \Omega)$ determines the gain and compression region. The output of the Electrometer is d-c compressed to 2/3 of full scale to keep the output swing to a reasonable value in measuring five magnitudes of signal.

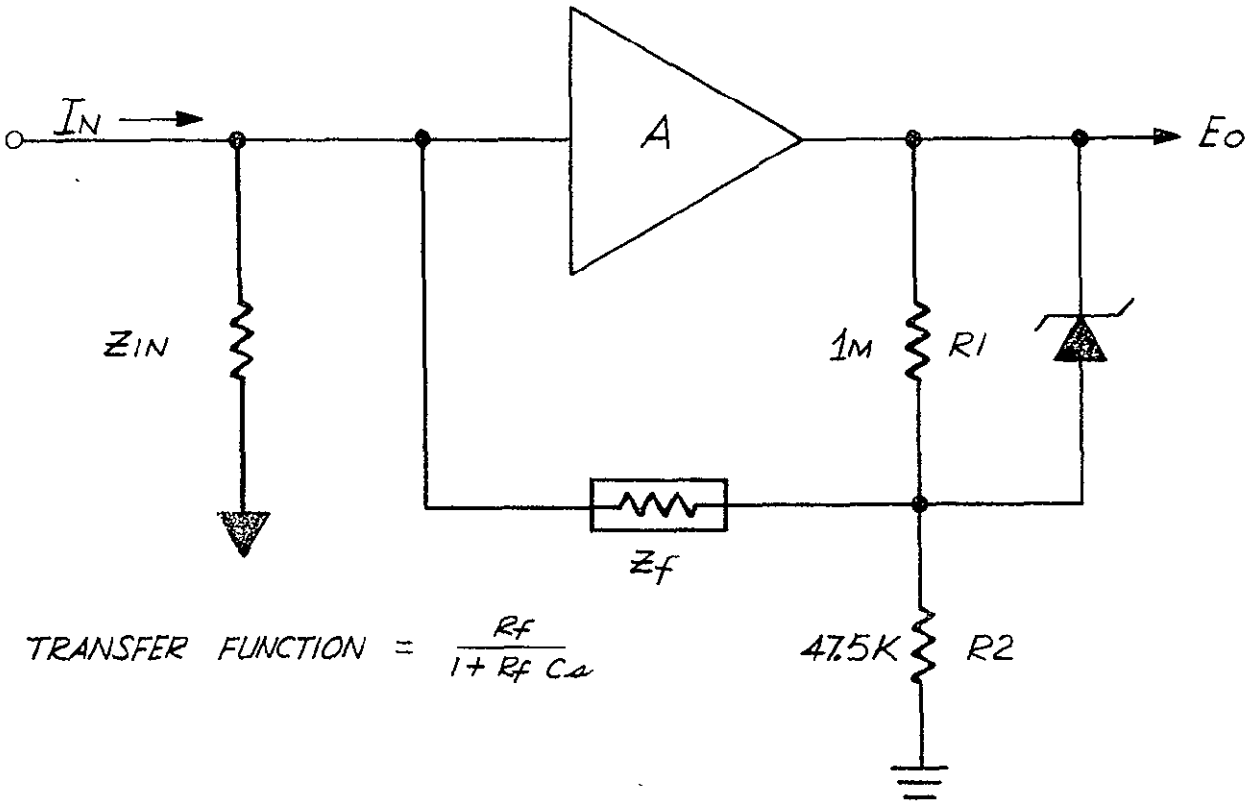
The transfer function for the Electrometer can be derived as follows: Consider Figure 3.1.2-5, Electrometer Feedback Equivalent network.



Electrometer Transfer Characteristics, Ion Mode
Figure 3.1.2-2

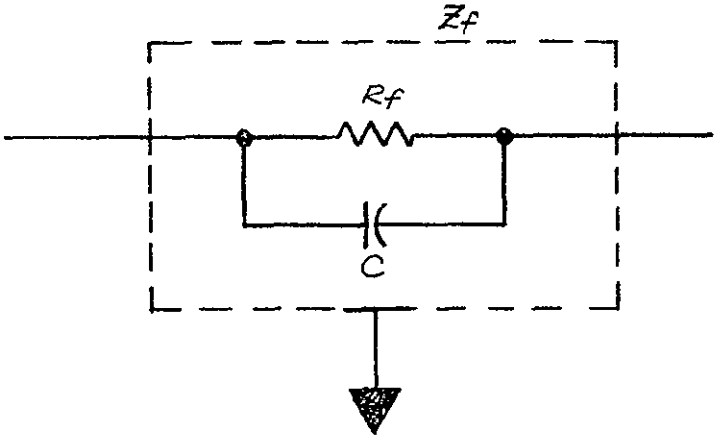


Electrometer Transfer Characteristics, Electron Mode
Figure 3.1.2-3



Electrometer Equivalent Circuit

Figure 3.1.2-4



Electrometer Feedback Equivalent Network (Z_f)

Figure 3.1.2-5

Assuming infinite gain, Zin can be neglected. Therefore,

$$Eo = \frac{Iin\ R_f}{1 + R_f Cs}$$

Thus

$$\frac{Eo}{I\,in} = \frac{R_f}{1 + R_f Cs}$$

Where

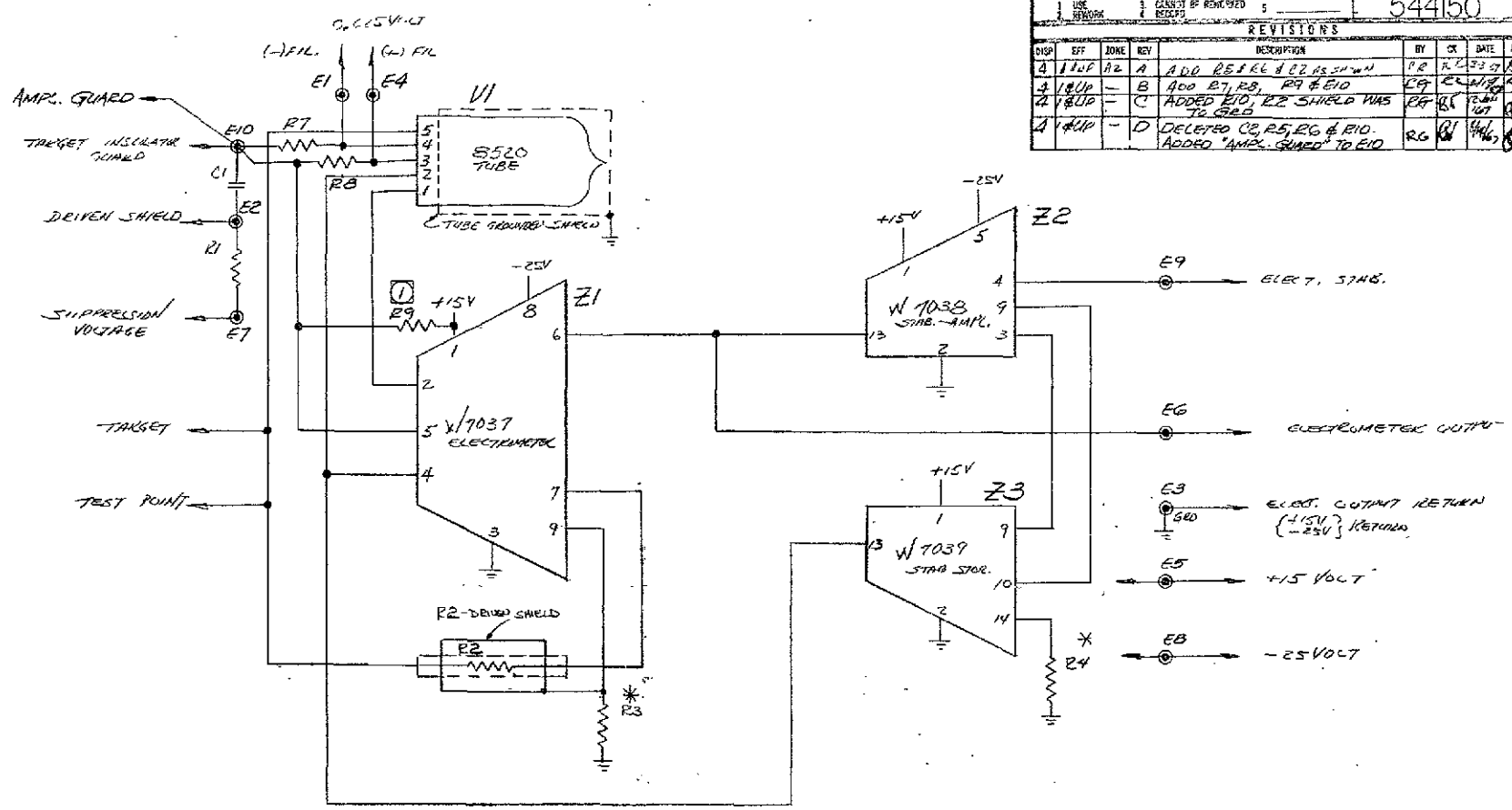
$$RC \approx 1.6 \text{ msec}$$

so that roll-off is about 100 Hz.

A shield is employed on the feedback resistance to reduce the effect of distributed capacity.

In the Electron mode the output is limited because of the supply voltage being +15 volts allowing the amplifiers to saturate at about +10 volts. In the Ion mode the output increases to about -22 volts and then saturates. The compression is achieved by means of the 2 zener diodes (See Schematic, Figure 4.1.4-1). These have sharp knee characteristics and produce a zener breakdown voltage of 6.7 volts at about 100 microamperes. These zener diodes are located in the output of the Electrometer, therefore forcing compression once the output increases above the zener breakdown voltage.

Refer to Figure 3.1.2-6 for the detailed Electrometer interconnect diagram.



PARTS DISPOSITION	DWG NO. 544150	REV
1 USE AS IS 2 REWORK 3 CANNOT BE REWORKED 4 RECORD 5		B

REVISIONS

DISP	SFF	ZONE	REV	DESCRIPTION	BY	CK	DATE	APPROVAL
A	1 UP	A2	A	ADD R8 REL & C2 AS SHOWN	PR	[illegible]	[illegible]	[illegible]
A	1 & UP	—	B	ADD R7, R8, R9 & E10	CG	[illegible]	[illegible]	[illegible]
A	1 & UP	—	C	ADDED E10, E2 SHIELD WAS TO GRD	PR	[illegible]	[illegible]	[illegible]
A	1 & UP	—	D	DELETED C8, R5, R6 & E10. ADDED "AMPL. GUARD" TO E10	RG	[illegible]	[illegible]	[illegible]

* SELECT COMPONENT

Electrometer Interconnect Diagram

Figure 3.1.2-6

R1 = 3 MEG, 5%, 1/8W, RC05GF305J, A-B
R2 1.5X10^10, 2%, RX-15, VICTOREEN
R3 = 17.4K, 1%, 1/8W, RNS5C1742F
R4 RNS5C[ ]--F, (RANGE 20KΩ-80K)
C1 .01μF, 10%, 100V, CP20275-103
R5 SELECT RC05GF---J (TYP. 360K-3.6M)
R6 SELECT RC05GF---J (TYP 100K)
C2 SELECT CP20275--- (TYP. 0.1μF)
R7, R8 510Ω, 1%, 1/8W, RN55C5100F
[1] R9 499K, 1%, 1/8W, RN60C4993F ON SN 1 THRU 8 NO
FOR MECHANICAL ASSEMBLY SEE DWG # 544145.

QTY REQD PER NOTED ASSY	PART NO	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	ELEC REF DES	CODE IDENT	ZONE	ITEM NO.
CONFIGURATION			LIST OF MATERIALS				

DASH NO.	MODEL NO	NEXT ASSEMBLY	MODEL NO	FINAL ASSEMBLY	MODEL NO
APPLICATION					

INTERPRET THIS DRAWING PER STANDARDS IN MIL-D-70327
DIMENSIONS ARE IN INCHES
TOLERANCES ON DECIMALS: X ± .1, XX ± .03, XXX ± .010; ANGLES ± 0° 30'; XXXX ± .0050
✓ SURFACE ROUGHNESS
HOLE DIA. TOLERANCE: .0135 THRU .125 +.004 -.001; .125 THRU .250 +.005 -.001; .251 THRU .500 +.006 -.001; .501 THRU .750 +.008 -.001; .751 THRU 1.000 +.010 -.001; 1.001 THRU 2.000 +.012 -.001; 2.001 AND OVER LINEAR

CONTRACT NO. AF 45 2-3374
DRAWN [illegible] 9/12/66
CHECKED [illegible] 9-22-66
MECHANICAL
ELECTRICAL [illegible] 9/22/66
PROJ. MGR. [illegible] 9/22/66
APPR
DESIGN ACTIVITY APPD
CUSTOMER

MARSHALL LABORATORIES
TORRANCE, CALIFORNIA

TITLE: ELECTROMETER INTERCONNECT DIAGRAM - AMPL PLASMA PROBE PIONEER C-D

SIZE	CODE IDENT NO.	DWG NO.	REV
C	13126	544150	D

SCALE — RELEASED SEP 8 2 1966 SHEET OF

ML FORM 192

3.1.3 Attenuator and Pulse Width Modulator

See Figure 3.1.3-1 for a simplified block diagram of the Attenuator and Logarithmic Pulse Width Modulator (LPWM).

The output of the amplifier is passed through a variable attenuator to the input of a precision voltage Comparator. A sample command signal applies the maximum amplitude of reference voltage to the comparator which initiates the pulse out of the Comparator. The reference voltage input is allowed to decay exponentially, and as soon as it falls below the level of the input signal voltage, the output pulse is terminated.

Thus a maximum flux (least amplifier output) produces a maximum pulse width and maximum flux produces a minimum pulse width.

This width modulated pulse gates a clock signal into a seven-stage digital Comparator which converts the flux amplitude to a 7 bit digit number. The circuit is capable of storing the number representing maximum flux and signaling the sector programmer when this maximum has occurred.

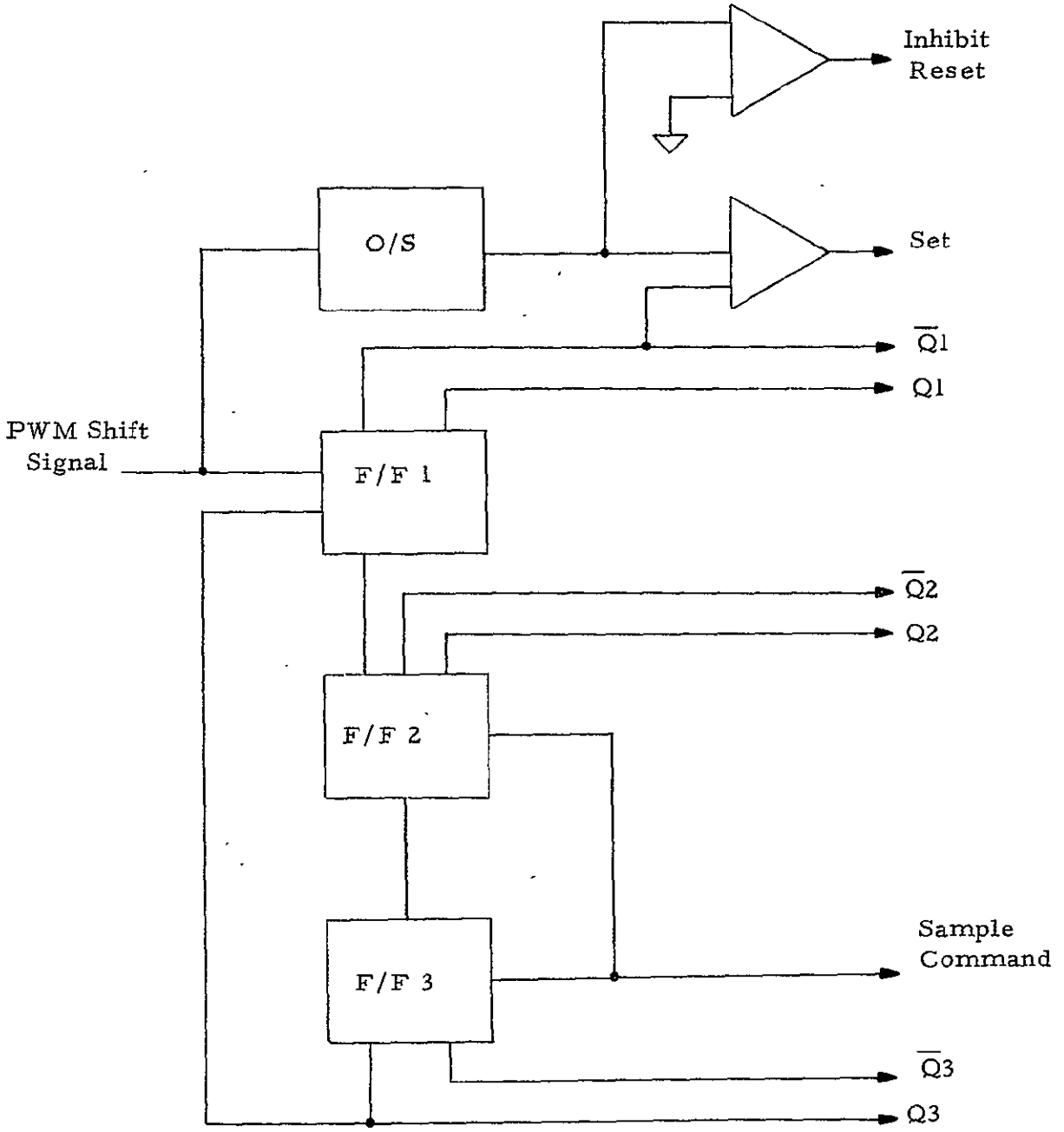
3.1.4 Pulse Width Modulator Programmer

Refer to Figure 3.1.4-1 for a block diagram of the Pulse Width Modulator (PWM) Programmer.

The PWM Programmer controls the Positive and negative Reference Generators. The Q1, Q2, and Q3 outputs (and their complements) drive the Reference Generators to provide three levels of exponentially decaying reference potentials to the Comparators.

The basic timing signal is the PWM Shift Pulse. Input and output waveforms are shown in Figure 3.1.4-2 and 3.1.6-2.

Q2 and Q3 are preset by the sample command. Q1 is preset by Q3.



Pulse Width Modulator Programmer
Block Diagram
Figure 3.1.3-1

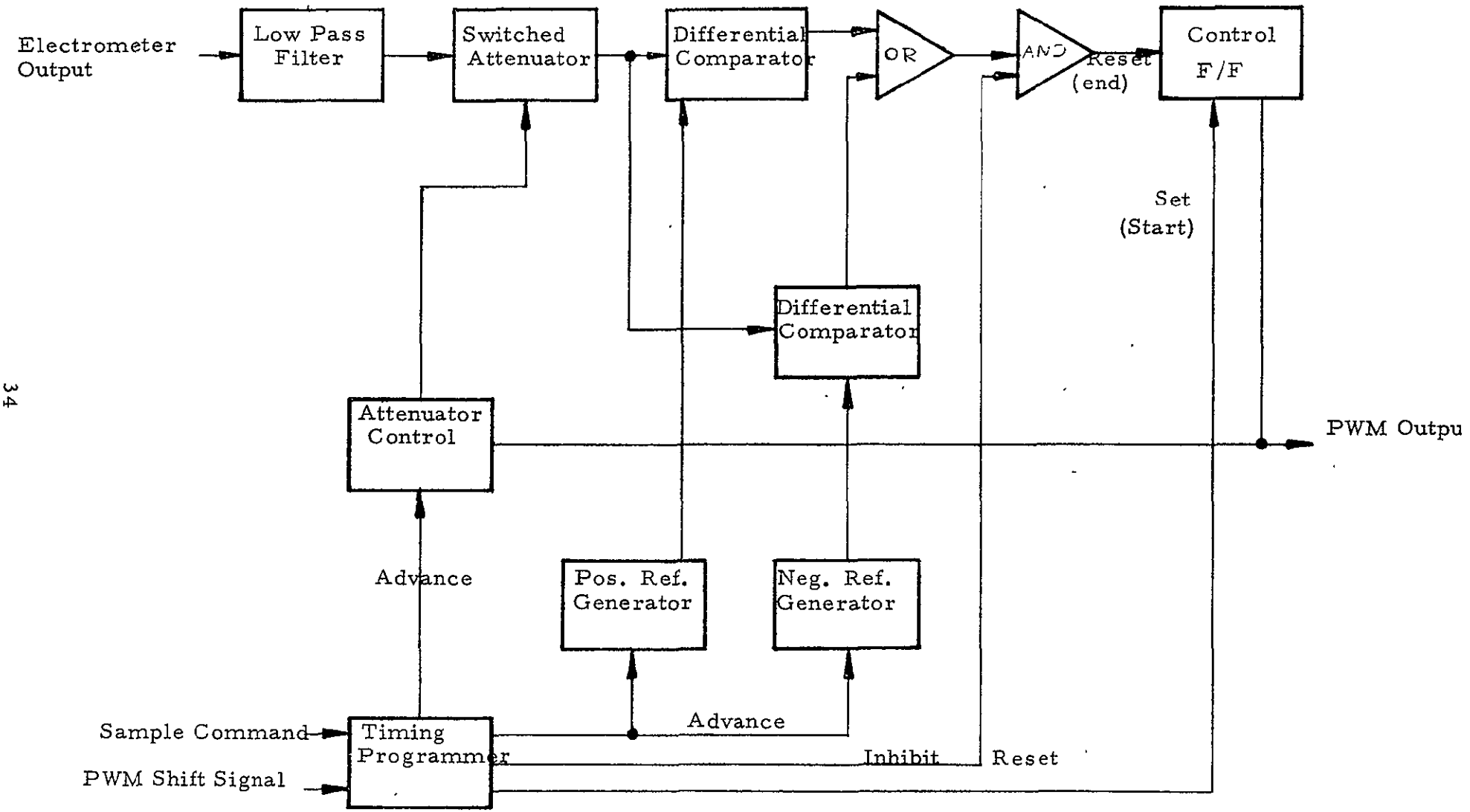
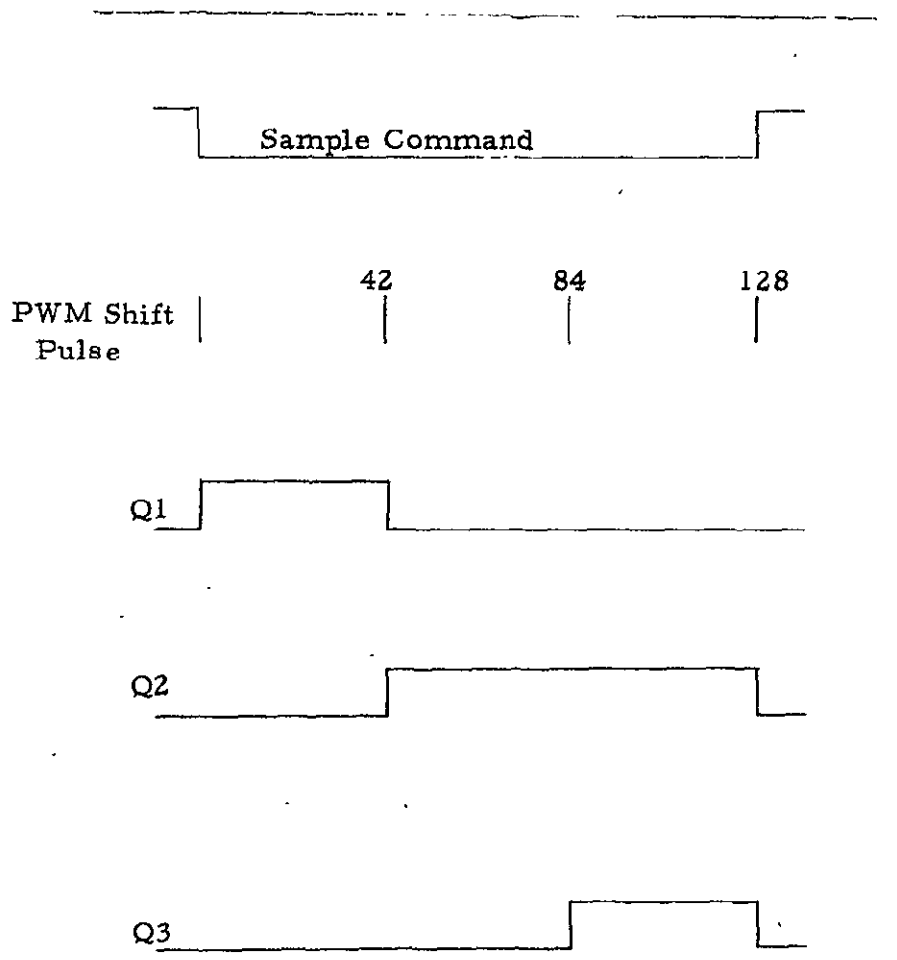


Figure 3.1.4-1 Block Diagram, Pulse Width Modulator and Attenuation



Input and Output Waveforms,
Pulse Width Modulator Programmer
Figure 3. 1. 4-2

The $\overline{PWM}$ signal is generated in conjunction with the Logic Programmer and the output of the Comparators. It is used together with the Q2, Q3, and $\overline{Q3}$ signals from the PWM Programmer, to program the Attenuator Driver. See Figure 3.1.4-3, Logic Programmer Block Diagram.

3.1.5 Comparators

Two Comparators are used in the LPWM: one negative Comparator and one positive Comparator (Figure 3.1.3-1, LPWM Block Diagram). The comparison of an input signal with the exponentially decaying reference input determines the output pulse width. The output of the positive Attenuator is the input to the positive Comparator; the output of the negative Attenuator is the input to the negative Comparator.

The Comparators are each essentially a three-stage differential amplifier. See Figure 3.1.5-1 for the Block Diagram and stage gains.

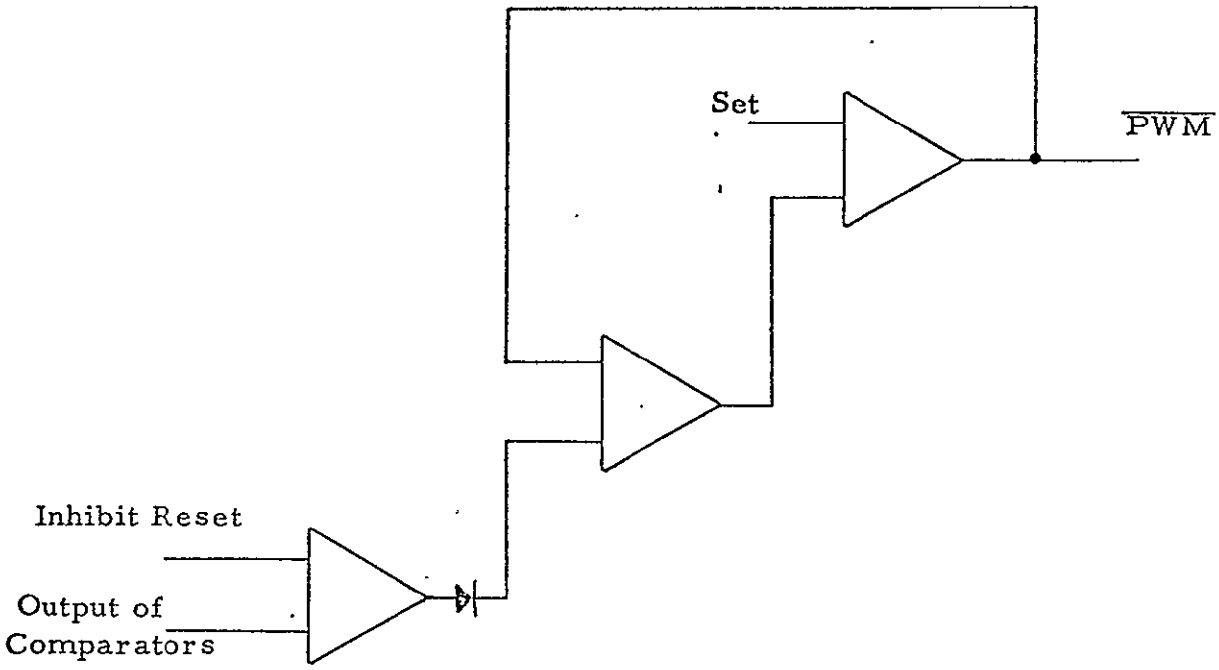
3.1.6 Reference Generator Networks

Two Reference Generator networks provide the exponentially decaying reference levels to the Comparators. The Reference Generator networks consist of:

a. Three Reference Drivers
b. An Offset Generator
c. One positive and one negative Reference Generator (summing networks)

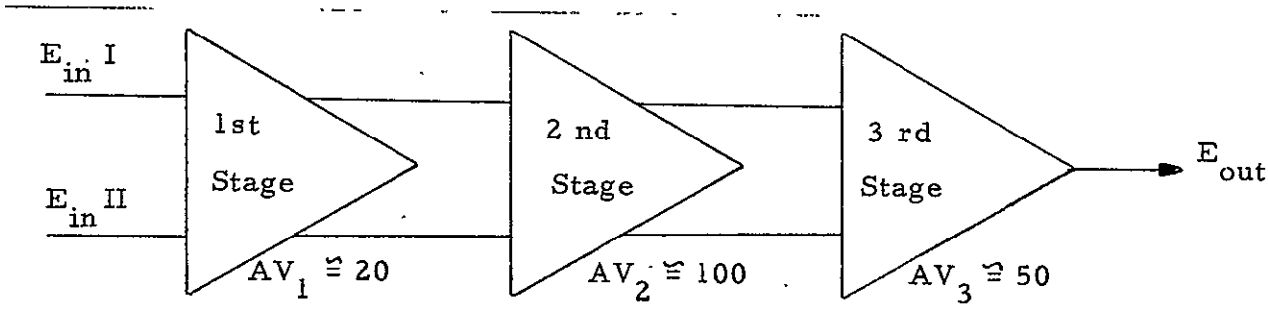
Refer to Figure 3.1.6-1 for the Reference Generator Network Block Diagram.

The Pulse Width Modulator Programmer (Figure 3.1.4-1) controls the Reference Drivers and the Offset Generator.



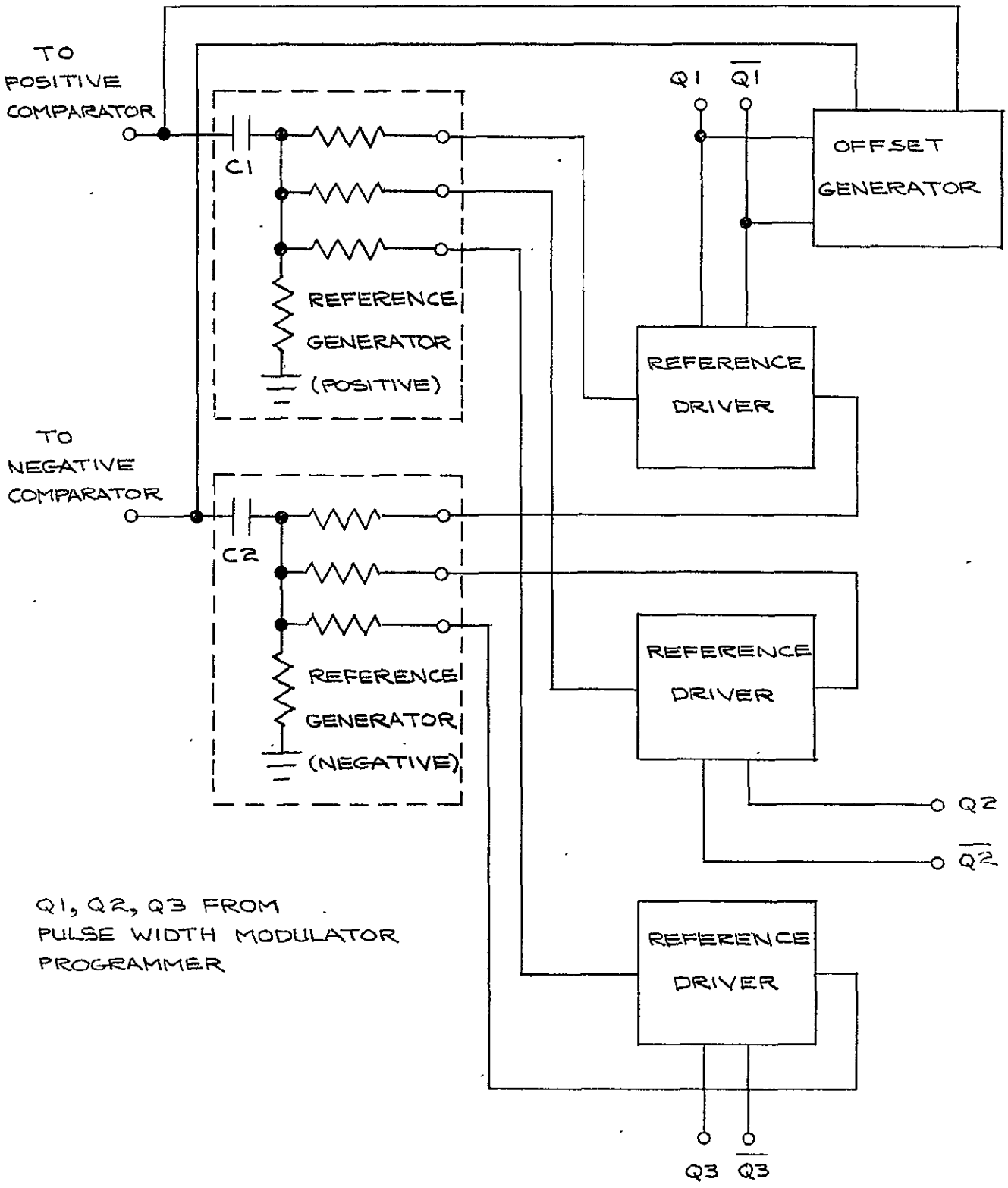
Logic Programmer Block Diagram

Figure 3.1.4-3



$$\text{Total Gain} = AV_1 \times AV_2 \times AV_3$$
$$= 20 \times 100 \times 50.0$$
$$= 1 \times 10^5$$

Comparator Block Diagram
Figure 3.1.5-1



Reference Generator Network, Block Diagram
Figure 3.1.6-1

The three Drivers are sequentially activated to drive each summing resistor in each Reference Generator to consecutively produce three distinct levels at each output. The capacitors C_1 and C_2 form part of an RC network to allow the ouput levels to exponentially decay. The Offset Generator inserts a 450 mv offset to the Reference Generator outputs at the first level. See Figure 3.1.6-2 for the timing diagram of the Reference Generator Network. This is an extension of Figure 3.1.4.-2, Input and Output Waveforms, Pulse Width Modulator.

3.1.7 Suppression Circuit

The function of the Suppression Circuit is to provide all necessary voltages for the Optics section and a +40 volt supply for the drift tube. The Suppression Circuit is an integral part of the amplifier assembly. The output of the suppression circuit is dependent upon logic signals 6+0 and $6+\overline{25}$. Table 3.1.7A illustrates the output combinations of the circuit in conjunction with the logic signals.

$6+\overline{25}$	6+0	Suppression Voltage
0	0	-40
0	1	0
1	0	-25
1	1	+ 6

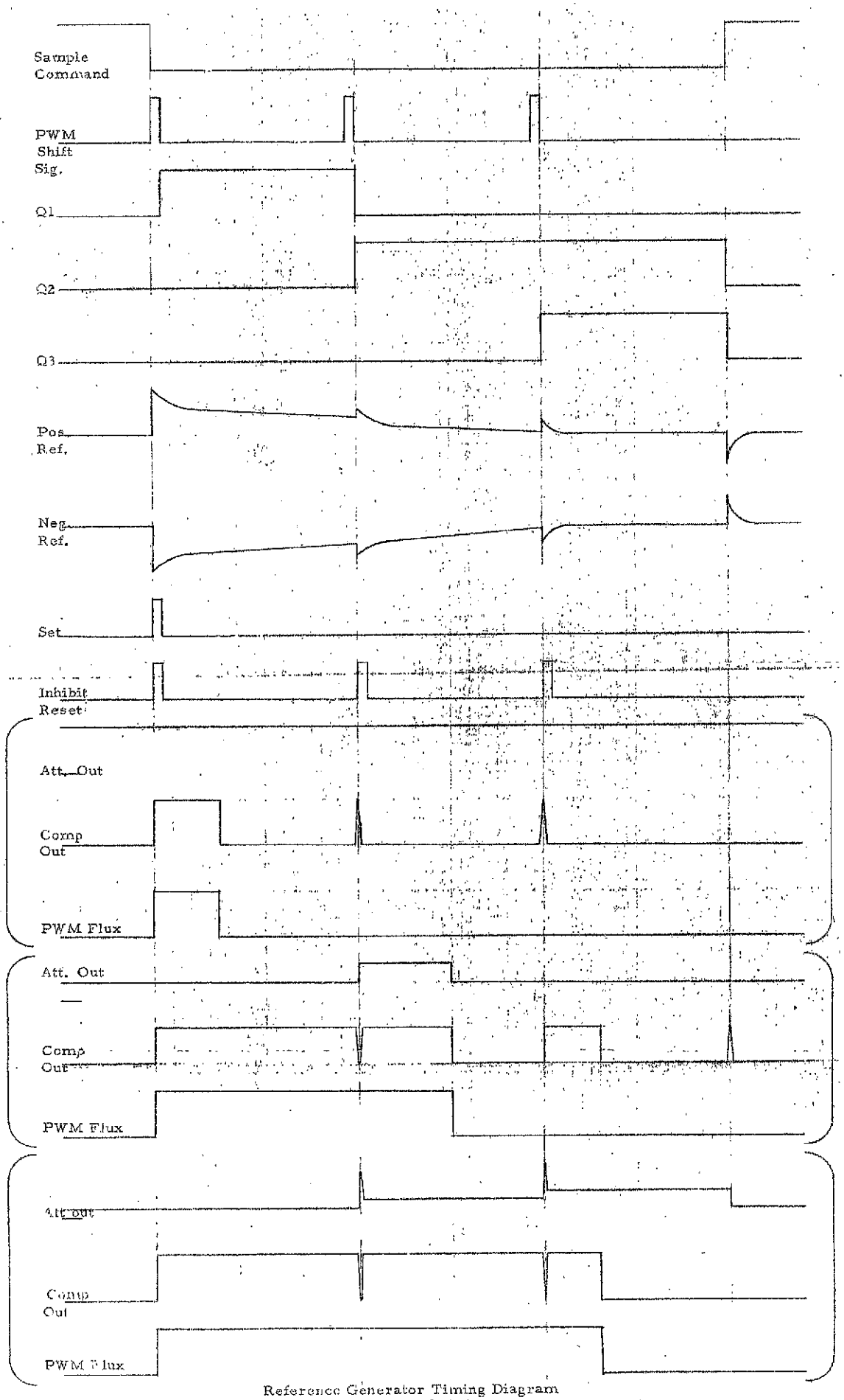
Table 3.1.7A Suppression Circuit Logic

3.2 Buffer Logic

Refer to Figure 3.2-1 for the block diagram of the Buffer Logic.

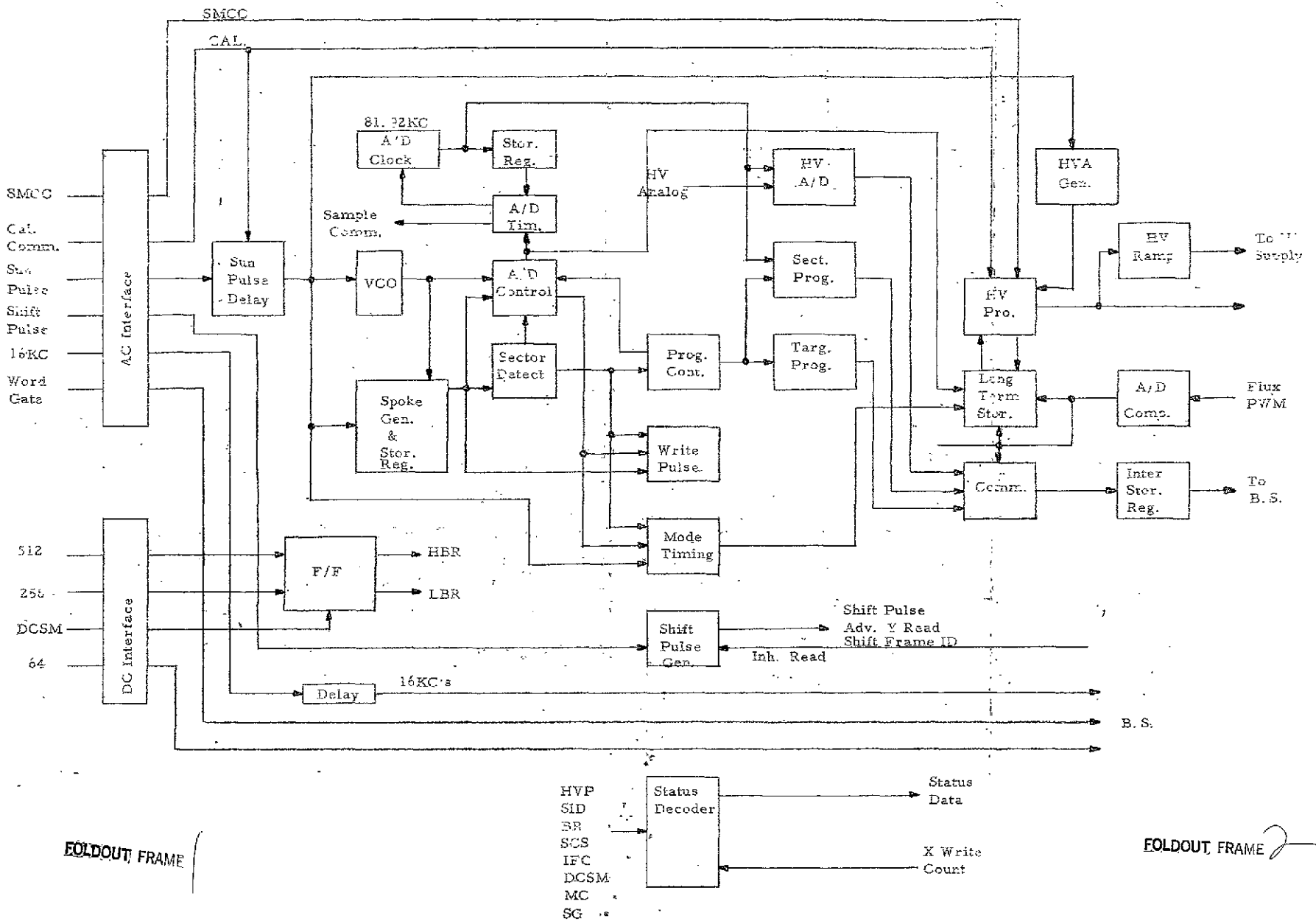
3.2.1 Timing and Control

FOLDOUT FRAME



FOLDOUT FRAME

Reference Generator Timing Diagram
Figure 3.1.6-2



Buffer Logic Block Diagram.
Figure 3.2-1

3.2.1.1 Voltage Controlled Oscillator

See Figure 3.2.1-1 for the Voltage Controlled Oscillator Block Diagram.

The Voltage Controlled Oscillator (VCO) is an astable multivibrator with a symmetical output. It feeds into an eleven stage counter which counts to 2048. The Sun Pulse resets the counter to zero and synchronizes the phase of the oscillator. If the oscillator frequency is higher than 2048 counts between Sun Pulses, the counter overflows and sets the control flip-flop which then acts to reduce the VCO frequency. When frequency is low, the Control flip-flop is reset and the VCO frequency increases.

R and C provide a large time constant of 1500 seconds to achieve a ripple error of less than 0.1%.

3.2.1.2 A/D Clock

Figure 3.2.1-2 shows the block diagram for the A/D Clock.

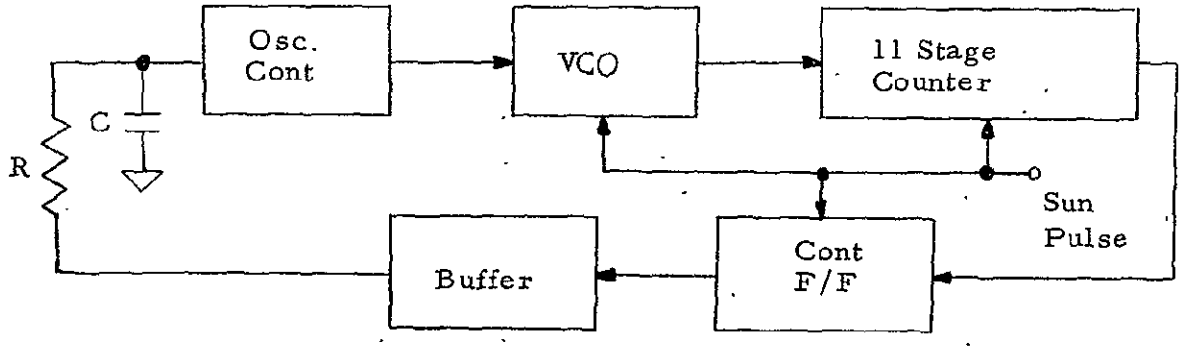
The A/D Clock oscillator is an astable multivibrator whose output is a 4 μsecond pulse with a repetition rate of 81.92 Kpps. The frequency is controlled to within +0.4%. The Stop/Start circuit provides a delay of 8 μseconds between the Start command and the first clock pulse.

3.2.1.3 Sun Pulse Delay

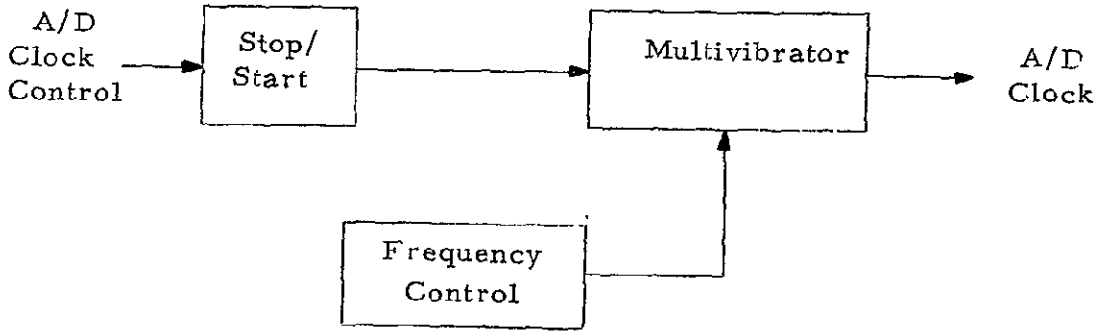
A block diagram of the Sun Pulse Delay network is shown in Figure 3.2.1-3.

In normal operation, Flip-Flop 1 is set by Sun Pulse Delayed Mode Change (SDMC), which is derived from the calibrate signal. This enables Gate 1 and inhibits Gate 2. $\overline{\text{The Interface Sun Pulse}}$ signal appears at the output as $\overline{\text{Sun Pulse}}$.

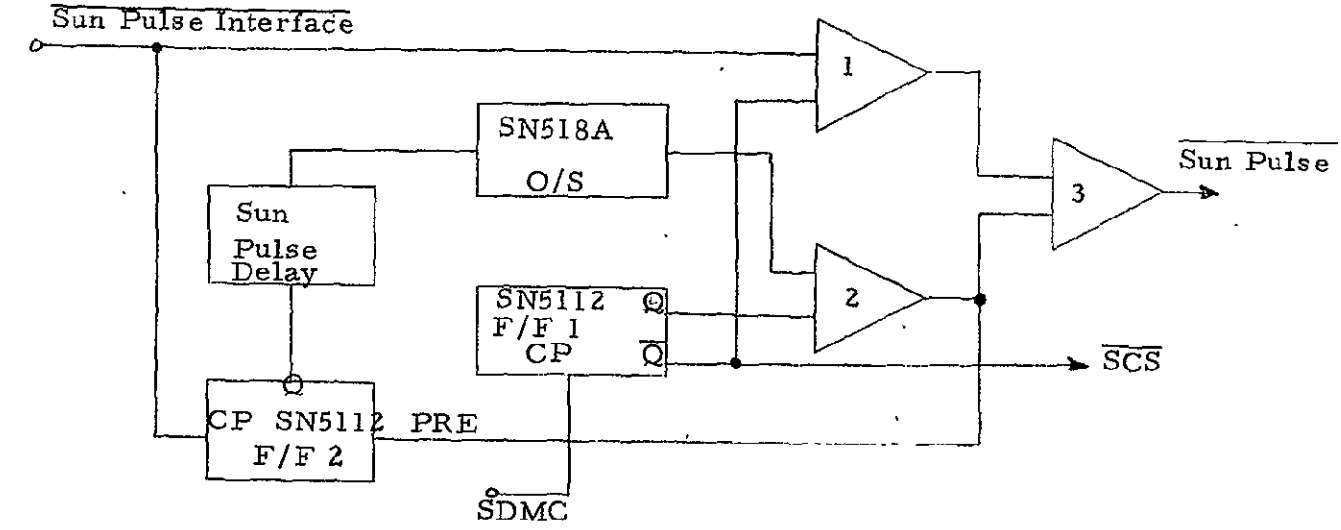
$\overline{\text{Interface Sun Pulse}}$ also toggles Flip-Flop 2, which operates the delay circuit when Q goes positive. The fall of the delay output triggers the One-Shot, but Gate 2 blocks this signal.



Voltage Controlled Oscillator Block Diagram
Figure 3.2.1-1



A/D Clock Block Diagram
Figure 3.2.1-2



Sun Pulse Delay Network
Block Diagram
Figure 3.2.1-3

When another SDMC pulse appears, Flip-Flop 1 is reset. Gate 1 is inhibited and Gate 2 is enabled. The output of the One-Shot then appears as the Sun Pulse.

The width of the delay output is controlled to 32±0.1 msec; therefore, the output of the One-Shot appears 32 msec after the $\overline{\text{Interface Sun Pulse}}$.

3.2.1.4 Spoke Generator

See Figure 3.2.1-4, Spoke Generator Block Diagram.

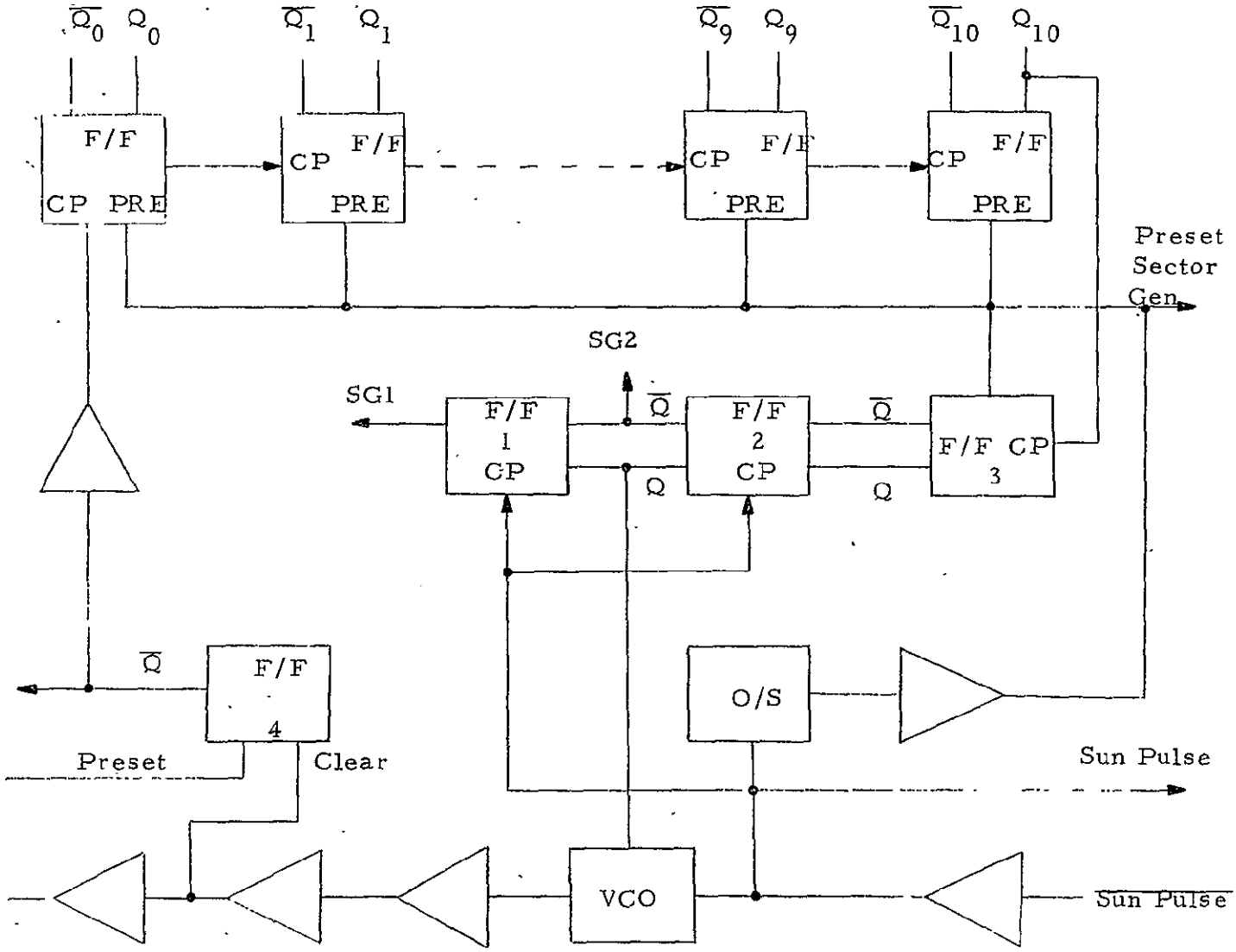
The Spoke Generator is an eleven stage ripple-counter driven by the VCO.

The $\overline{\text{Sun Pulse}}$ is inverted to produce the Sun Pulse. This signal drives the One-Shot which resets the counter and the overflow detector, Flip-Flop 3. The Sun Pulse is also used to toggle the two stage shift register, Flip-Flop 1 and Flip-Flop 2, and to synchronize the VCO.

If the VCO frequency is high, the counter overflows, setting Flip-Flop 3. The next Sun Pulse sets Flip-Flop 2 and the second Sun Pulse sets Flip-Flop 1. The Q output from Flip-Flop 2 acts to reduce the VCO frequency. When the frequency goes low Flip-Flop 3 remains reset and the next two Sun Pulses reset Flip-Flop 1 and Flip-Flop 2. Q of Flip-Flop 2 then increases the frequency. The Q outputs from Flip-Flop 1 and Flip-Flop 2 are used for status information.

The VCO is buffered to set and clear Flip-Flop 4. The $\overline{Q}$ output of Flip-Flop 4 provides the $\overline{V}$ signal which drives the counter; it is also used in the A/D control.

The output of the counter, Q_0 through Q_{10} divides the time between Sun Pulses into 2048 equal segments.



Spoke Generator Block Diagram
Figure 3.2.1-4

3.2.1.5 Sector Detector

The Sector Detector consists of Logic Gates which produce signals corresponding in time to various sectors or groups of sectors. The 128 Sectors are labelled Sector 0 through Sector 127. Each time duration of each sector is equal to 16 counts of the VCO.

Figure 3.2.1-5 shows the logic diagram of the Sector Detector. See Figure 3.2.1-6 for the timing diagram.

Table 3.2.1A lists the register count for each of the appropriate sectors. Table 3.2.1B through 3.2.1H show the Sector Detector Truth Tables.

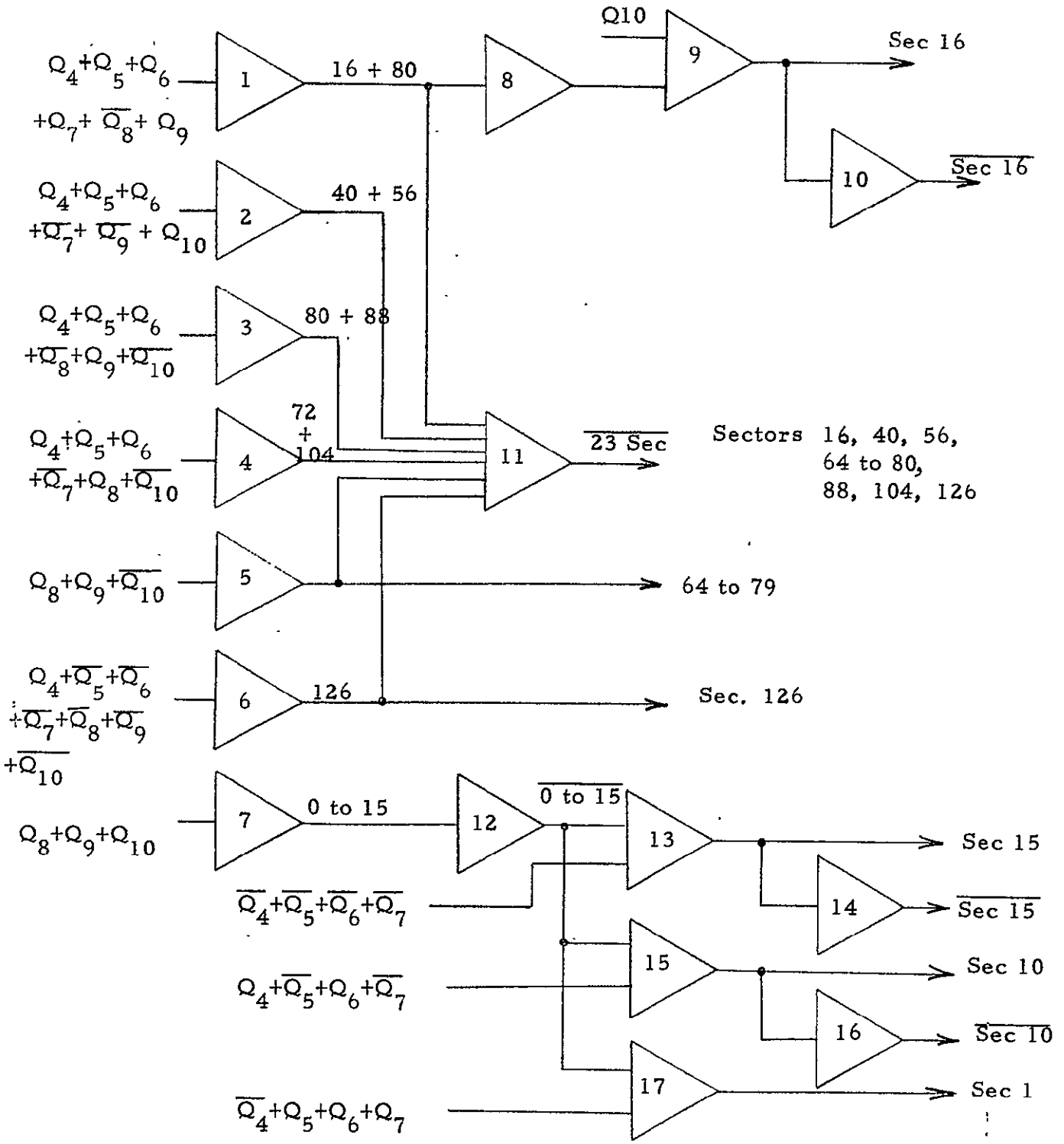
3.2.1.6 A/D Control

This circuit generates the basic timing signals for controlling the A/D functions, Target and High Voltage (HV) advances, and Write Pulses. See Figure 3.2.1-7 for the logic diagram of the A/D Control. Figure 3.2.1-8 shows the A/D Control timing diagram.

Signals 100, 101 and 102 occur during each sector. Signal 100 occurs during the first segment of each sector; signal 101 occurs during the 12th, and 102 during the 13th. 100 is used to generate Start A/D and Reset A/D pulses, and to reset the Write Counters in the Buffer Storage during High Bit Rate (HBR).

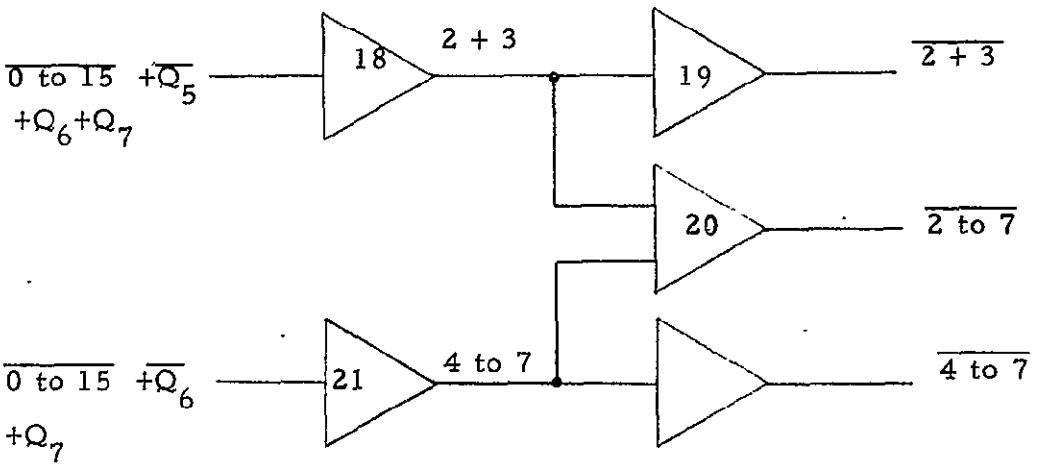
101 is used to generate Write Pulses during Sectors 66, 72 and 78 while in AS or during Sectors 2 and 10 while in PS. It will also Inhibit Data during Sector 15 if the Buffer Storage is full or while the instrument is in stabilization.

102 is used to generate Write Pulses for flux during each of the 23 selected sectors while in AS, during Sectors 2, 4, and 6 while in PS, and in Sector 2 in MFS.



Logic Diagram of Sector Detector
(continued next page)

Figure 3.2.1-5

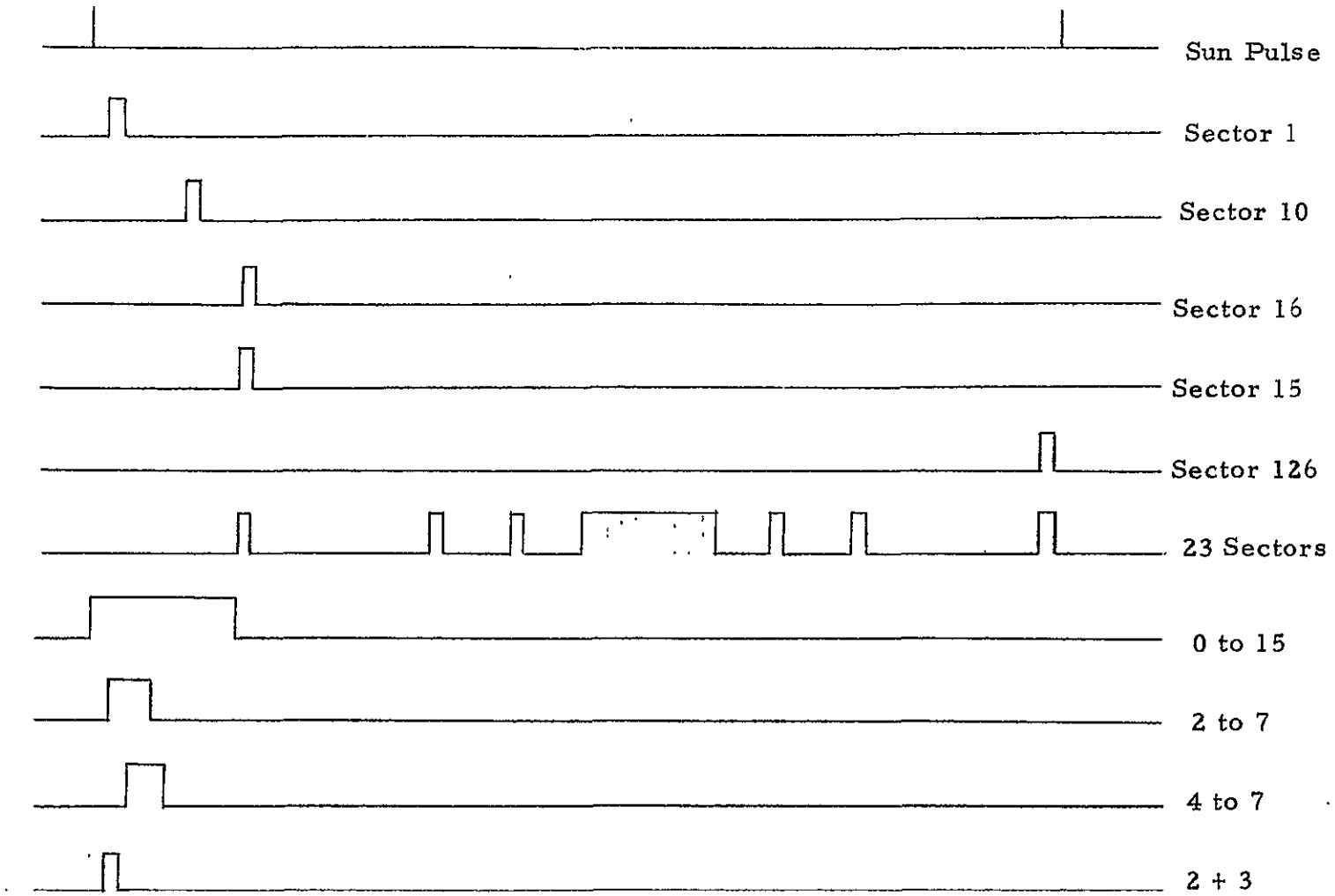


Logic Diagram of Sector Detector (cont.)
Elements are NOR gates.

Figure 3.2.I-5

Sector	Register Count
0	0 → 15
1	16 → 31
2	32 → 47
3	48 → 63
4	64 → 79
5	80 → 95
6	96 → 111
7	112 → 127
8→ 9	128 → 159
10	160 → 175
11→15	176 → 255
16	256 → 271
40	640 → 659
56	896 → 911
64→ 79	1204 → 1279
80	1280 → 1295
88	1408 → 1423
104	1664 → 1679
126	2016 → 2031

Table 3.2.1A, Register Count and Sector



Sector Detector - Timing Diagram
Figure 3.2.1-6

TRUTH TABLE FOR SECTORS 16 AND 80

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
256	0	0	1	0	0	0	0	0	0	0	0
271	0	0	1	0	0	0	0	1	1	1	1
1280	1	0	1	0	0	0	0	0	0	0	0
1281	1	0	1	0	0	0	0	1	1	1	1
	Do Not Care							Do Not Care			

Sector 16 + 80 = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot \overline{Q7} \cdot Q8 \cdot \overline{Q9}$

Input to Gate 1 = $Q4 + Q5 + Q6 + Q7 + \overline{Q8} + Q9$

Inverting

$$= \overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot \overline{Q7} \cdot Q8 \cdot \overline{Q9}$$

Re-inverting through Gate 8 and gives the same expression as at the input to Gate 1. OR'ing Q10 with this gives,

$$Q4 + Q5 + Q6 + Q7 + \overline{Q8} + Q9 + Q10$$

Inverting

$$\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot \overline{Q7} \cdot Q8 \cdot \overline{Q9} \cdot \overline{Q10} = \text{Sector 16}$$

Table 3.2.1B, Sector Detector Truth Tables

TRUTH TABLE FOR SECTORS 40 AND 56

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
640	0	1	0	1	0	0	0	0	0	0	0
659	0	1	0	1	0	0	0	1	1	1	1
896	0	1	1	1	0	0	0	0	0	0	0
911	0	1	1 (Do Not Care)	1	0	0	0	1	1	1 (Do Not Care)	1

Sectors 40 + 56 = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot Q7 \cdot Q9 \cdot \overline{Q10}$

Input to Gate 2 = $Q4 + Q5 + Q6 + \overline{Q7} + \overline{Q9} + Q10$

Inverting = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot Q7 \cdot Q9 \cdot \overline{Q10}$

TRUTH TABLE FOR SECTORS 80 AND 88

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
1280	1	0	1	0	0	0	0	0	0	0	0
1295	1	0	1	0	0	0	0	1	1	1	1
1408	1	0	1	1	0	0	0	0	0	0	0
1423	1	0	1	1 (DON'T CARE)	0	0	0	1	1	1 (Do Not Care)	1

Sectors 80 + 88 = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot Q8 \cdot \overline{Q9} \cdot Q10$

Input to Gate 3 = $Q4 + Q5 + Q6 + \overline{Q8} + Q9 + \overline{Q10}$

Inverting = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot Q8 \cdot \overline{Q9} \cdot Q10$

Table 3.2.1C, Sector Detector Truth Tables

TRUTH TABLE FOR SECTORS 72 AND 104

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
1152	1	0	0	1	0	0	0	0	0	0	0
1167	1	0	0	1	0	0	0	1	1	1	1
1664	1	1	0	1	0	0	0	0	0	0	0
1679	1	1	0	1	0	0	0	1	1	1	1
		Do Not Care						Do Not Care			

Sectors 72 + 102 = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot Q7 \cdot \overline{Q8} \cdot Q10$

Input to Gate 4 = $Q4 + Q5 + Q6 + \overline{Q7} + Q8 + \overline{Q10}$

Inverting = $\overline{Q4} \cdot \overline{Q5} \cdot \overline{Q6} \cdot Q7 \cdot \overline{Q8} \cdot Q10$

TRUTH TABLE FOR SECTORS 64 THRU 79

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
1024	1	0	0	0	0	0	0	0	0	0	0
1264	1	0	0	1	1	1	1	0	0	0	0
1279	1	0	0	1	1	1	1	0	0	0	0
				Do Not Care							

Sectors 64 → 79 = $\overline{Q8} \cdot \overline{Q9} \cdot Q10$

Input to Gate 5 = $Q8 + Q9 + \overline{Q10}$

Inverting = $\overline{Q8} \cdot \overline{Q9} \cdot Q10$

Table 3.2.1D, Sector Detector Truth Tables

TRUTH TABLE FOR SECTOR 126

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
2016	1	1	1	1	1	1	0	0	0	0	0
2031	1	1	1	1	1	1	0	1	1	1	1
								Do Not Care			

Sector 126 = $\overline{Q4} \cdot Q5 \cdot Q6 \cdot Q8 \cdot Q9 \cdot Q10 \cdot Q7$

Input to Gate 6 = $Q4 + \overline{Q5} + \overline{Q6} + \overline{Q7} + \overline{Q8} + \overline{Q9} + \overline{Q10}$

Inverting = $\overline{Q4} \cdot Q5 \cdot Q6 \cdot Q7 \cdot Q8 \cdot Q9 \cdot Q10$

TRUTH TABLE FOR SECTORS 0 THRU 15

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
0	0	0	0	0	0	0	0	0	0	0	0
240	0	0	0	1	1	1	1	0	0	0	0
255	0	0	0	1	1	1	1	1	1	1	1
				Do Not Care				Do Not Care			

Sector 0 → 15 = $\overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Input to Gate 7 = $Q8 + Q9 + Q10$

Inverting = $\overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Table 3.2.1E, Sector Detector Truth Tables

TRUTH TABLE FOR SECTORS 2 AND 3

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
32	0	0	0	0	0	1	0	0	0	0	0
47	0	0	0	0	0	1	0	1	1	1	1
48	0	0	0	0	0	1	1	0	0	0	0
63	0	0	0	0	0	1	1	1	1	1	1

Do Not Care

Sectors 2 + 3 = $Q5 \cdot \overline{Q6} \cdot \overline{Q7} \cdot \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Input to Gate 18 = $\overline{0 \rightarrow 15} + \overline{Q5} + Q6 + Q7$

Inverting = $(0 \rightarrow 15) \cdot Q5 \cdot \overline{Q6} \cdot \overline{Q7}$

Where $(0 \rightarrow 15) = \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

TRUTH TABLE FOR SECTORS 4 THRU 7

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
64	0	0	0	0	1	0	0	0	0	0	0
112	0	0	0	0	1	1	1	0	0	0	0
127	0	0	0	0	1	1	1	1	1	1	1

Do Not Care

Sectors 4 →7 = $Q6 \cdot \overline{Q7} \cdot \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Input to Gate 21 = $\overline{(0 \rightarrow 15)} + \overline{Q6} + Q7$

Inverting = $(0 \rightarrow 15) \cdot Q6 \cdot \overline{Q7}$

Where $(0 \rightarrow 15) = \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Table 3.2.1F, Sector Detector Truth Tables

Input to Gate 11 = 16 + 80 + 40 + 56 + 80 + 88 + 72 + 104 + (64 → 79) + 126

Inverting

$$= \overline{16} \cdot \overline{40} \cdot \overline{56} \cdot \overline{(64 \rightarrow 79)} \cdot \overline{80} \cdot \overline{88} \cdot \overline{104} \cdot \overline{126}$$

$$= \overline{\text{23 Sectors}}$$

TRUTH TABLE FOR SECTOR 15

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
240	0	0	0	1	1	1	1	0	0	0	0
255	0	0	0	1	1	1	1	1	1	1	1

Do Not Care

Sector 15 = $Q4 \cdot Q5 \cdot Q6 \cdot Q7 \cdot \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Input to Gate 13 = $\overline{Q4} + \overline{Q5} + \overline{Q6} + \overline{Q7} + \overline{(0 \rightarrow 15)}$

Inverting = $Q4 \cdot Q5 \cdot Q6 \cdot Q7 \cdot (0 \rightarrow 15)$

Where $(0 \rightarrow 15) = \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

TRUTH TABLE FOR SECTOR 10

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
160	0	0	0	1	0	1	0	0	0	0	0
175	0	0	0	1	0	1	0	1	1	1	1

Do Not Care

Sector 10 = $\overline{Q4} \cdot Q5 \cdot \overline{Q6} \cdot Q7 \cdot \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Inputs to Gate 15 = $Q4 + \overline{Q5} + Q6 + \overline{Q7} + \overline{(0 \rightarrow 15)}$

Inverting = $\overline{Q4} \cdot Q5 \cdot \overline{Q6} \cdot Q7 \cdot (0 \rightarrow 15)$

Where $(0 \rightarrow 15) = \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Table 3. 2. 1G, Sector Detector Truth Tables

TRUTH TABLE FOR SECTOR 1

Count	Q10	Q9	Q8	Q7	Q6	Q5	Q4	Q3	Q2	Q1	Q0
16	0	0	0	0	0	0	1	0	0	0	0
31	0	0	0	0	0	0	1	1	1	1	1

Do Not Care

Sector 1 = $Q4 \cdot \overline{Q5} \cdot \overline{Q6} \cdot \overline{Q7} \cdot \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Inputs to Gate 17 = $\overline{Q4} + Q5 + Q6 + Q7 + \overline{(0 \rightarrow 15)}$

Inverting = $Q4 \cdot \overline{Q5} \cdot \overline{Q6} \cdot \overline{Q7} \cdot (0 \rightarrow 15)$

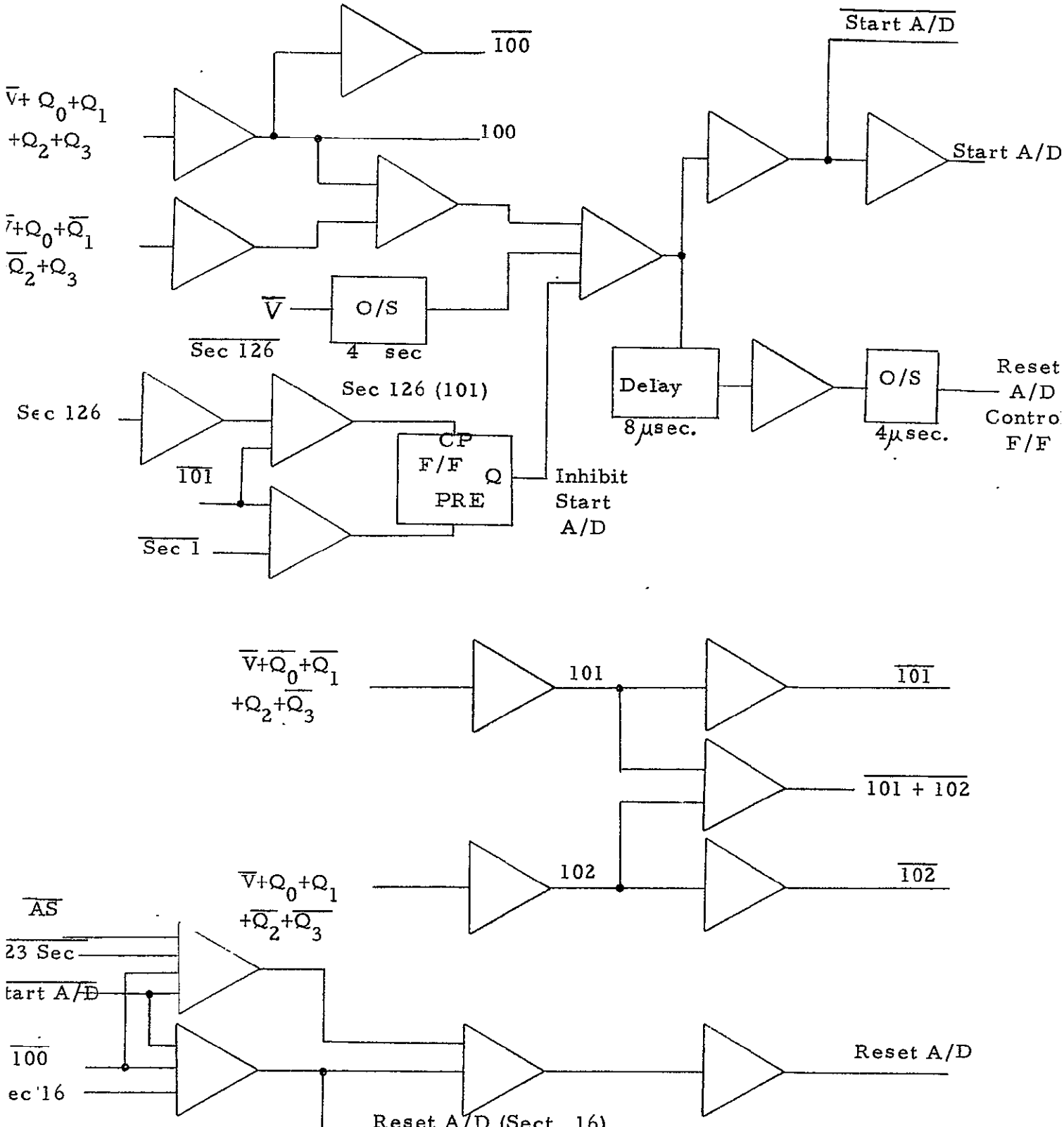
Where $(0 \rightarrow 15) = \overline{Q8} \cdot \overline{Q9} \cdot \overline{Q10}$

Input to Gate 20 = $2 + 3 + (4 \rightarrow 7)$

Inverting = $\overline{2} \cdot \overline{3} \cdot \overline{(4 \rightarrow 7)}$

$= \overline{(2 \rightarrow 7)}$

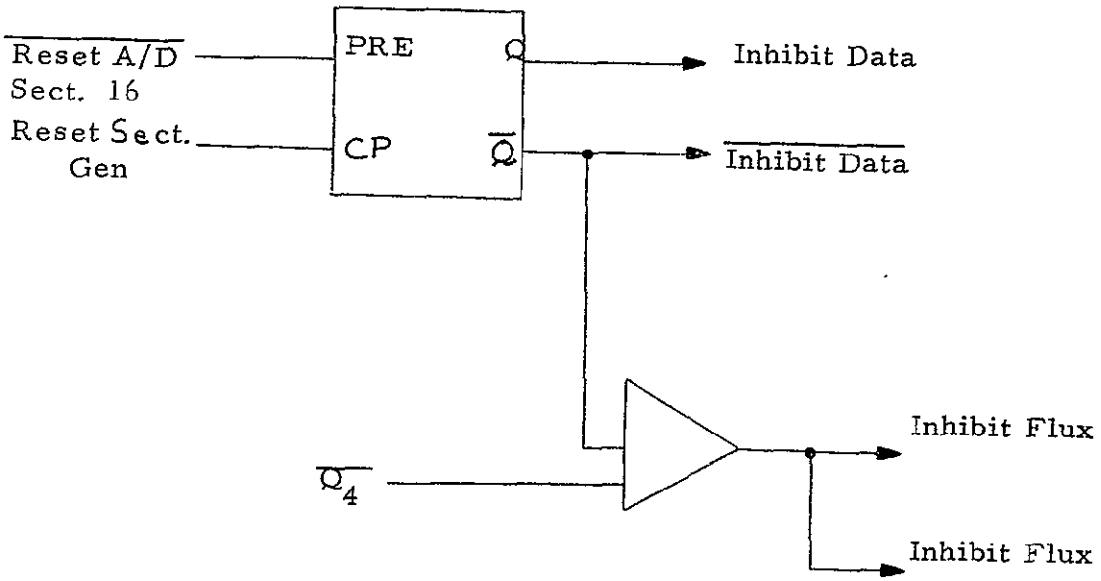
Table 3.2.1H, Sector Detector Truth Tables



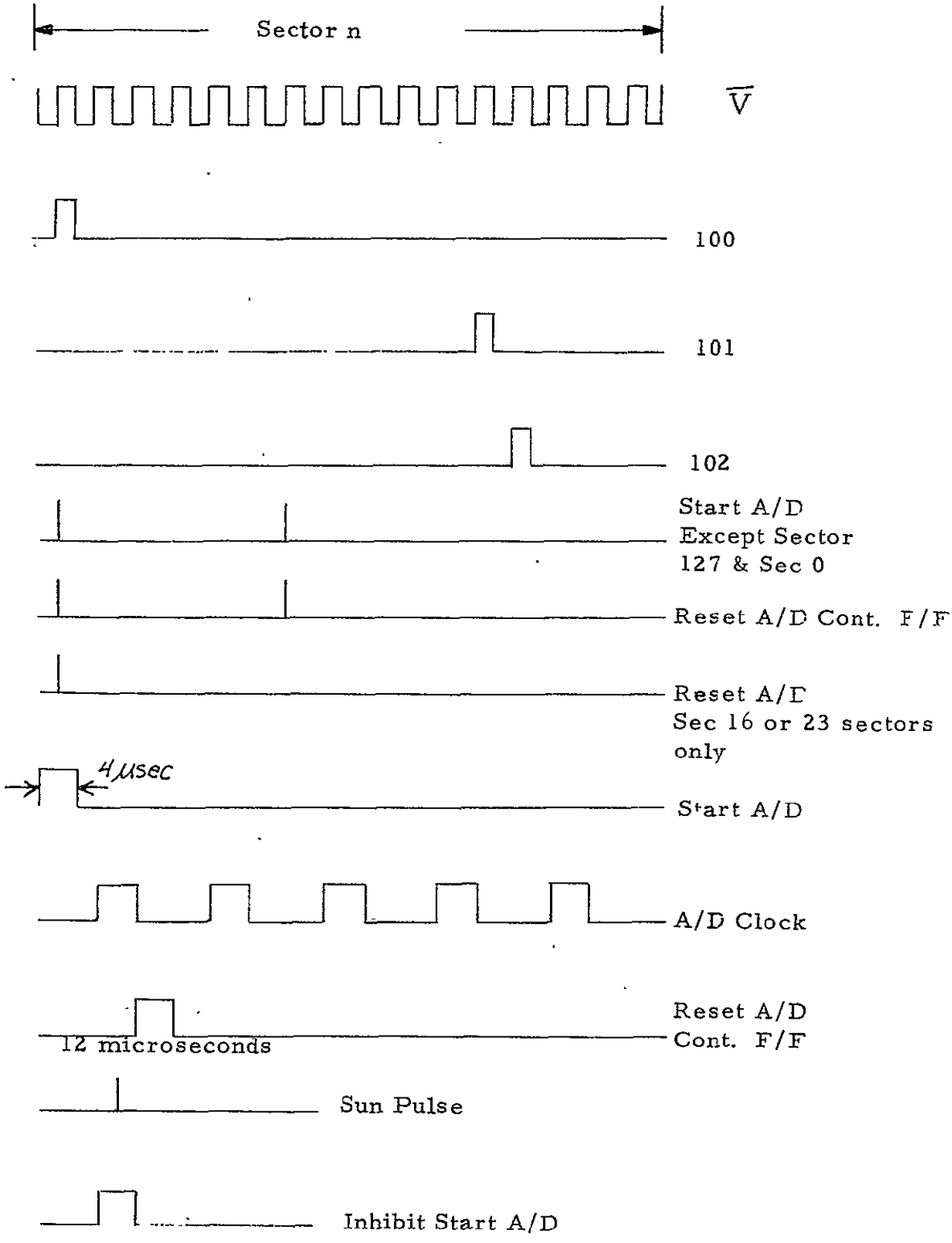
Reset A/D (Sect. 16)

A/D Control Logic Diagram (continued next page)

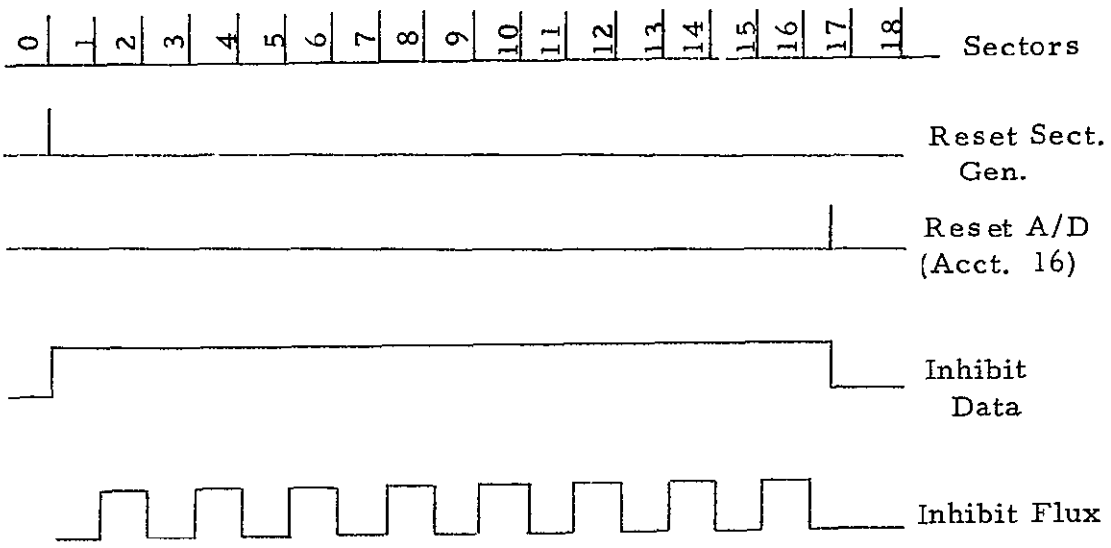
Figure 3.2.1-7



A/D Control Logic Diagram (continued)
Figure 3.2.1-7



A/D Control Timing Diagram
(continued next page)
Figure 3.2.1-8



A/D Control Timing Diagram (continued)
Figure 3.2.1-8

It is used to generate Write Pulses for sector information during Sectors 3, 5 and 7 while in PS and in Sector 3 while in MFS. It also generates a Write Pulse for status information every 3rd Sector 1 during MFS.

There are two Start A/D pulses generated during each Sector: one at the 1st segment, the other at the 7th segment. The fall of each $\overline{V}$ triggers a one-shot whose output is a negative-going 4 μsecond pulse. The pulses are inhibited by setting a flip-flop at time 101 of Sector 126. The inhibit voltage is removed by toggling the flip-flop at time 101 of Sector 1.

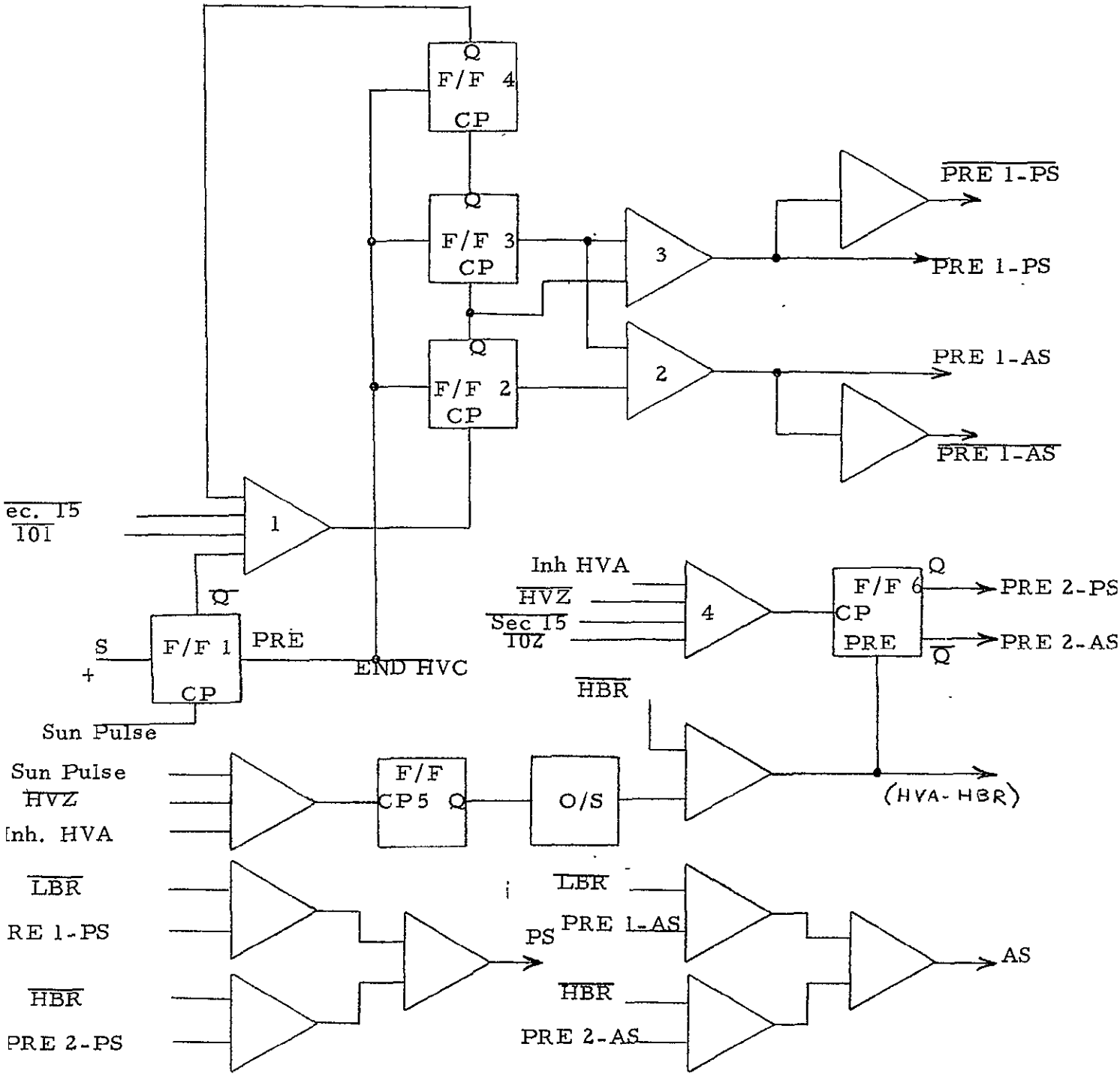
The Reset A/D Control flip-flop is a 4 μsec pulse which is delayed 8 μsecond from the fall of the Start A/D pulse. It occurs during time 100 of each of the 23 sectors while in AS, or Sector 16 otherwise.

The Inhibit Data flip-flop is reset at Sector 16. Inhibit Data (Q) and Inhibit Flux are low until the next Sun Pulse. At this time, the Reset Sector Generator pulse sets the flip-flop. Data taking is then inhibited from Sector 0 through Sector 15. At the same time, the gate is enabled. $\overline{Q4}$ changes state at each sector, causing flux readout to be inhibited at the odd numbered sectors until Sector 16.

3.2.1.7 Mode Timing

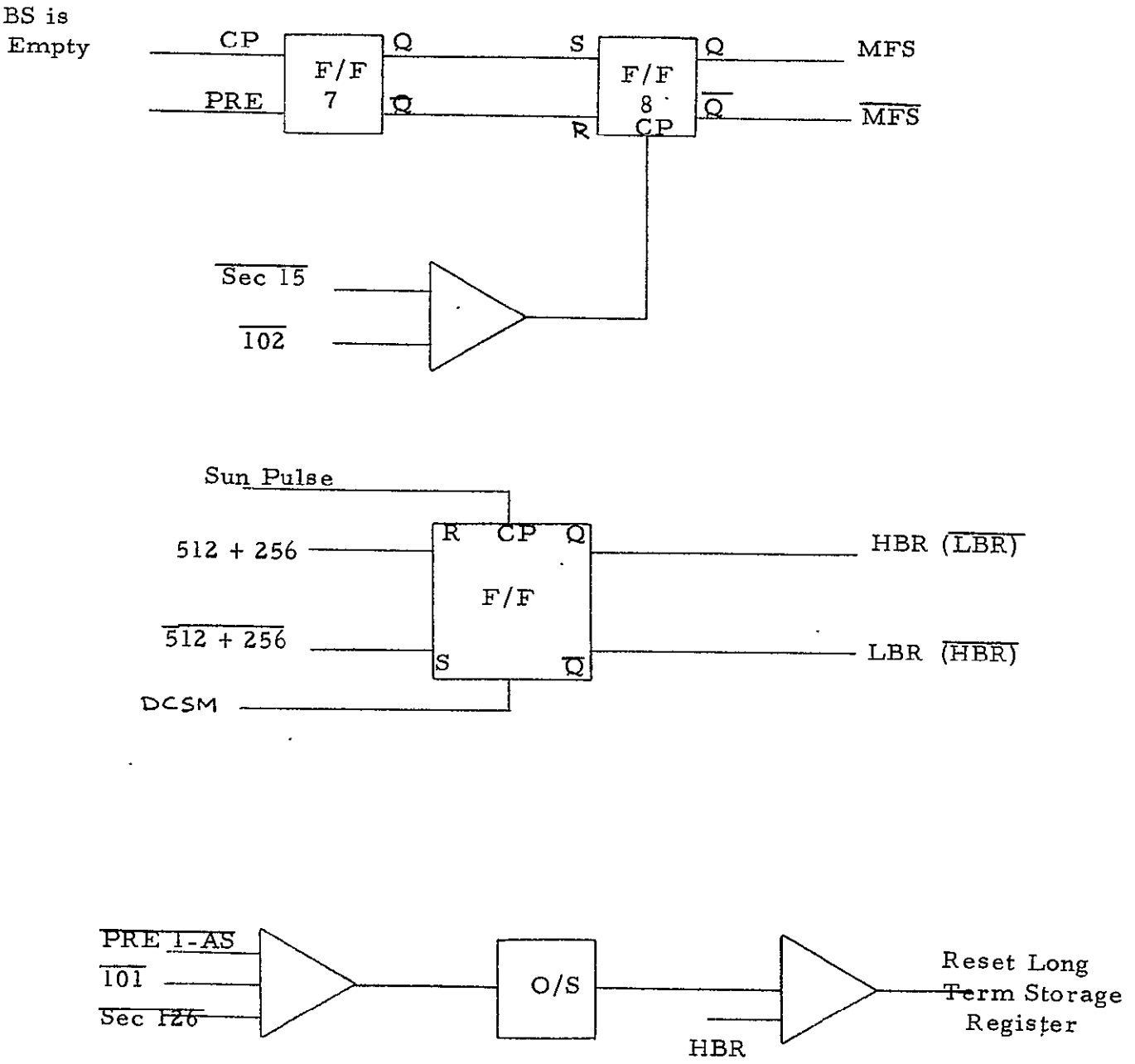
See Figures 3.2.1-9 through 3.2.1-12 for logic and timing diagrams of the Mode Timing network.

The Mode Timing circuit genrates the signals which control the scanning modes of the instrument. The sequence of these modes is determined by the Levels of HBR (High Bit Rate) and LBR (Low Bit Rate).

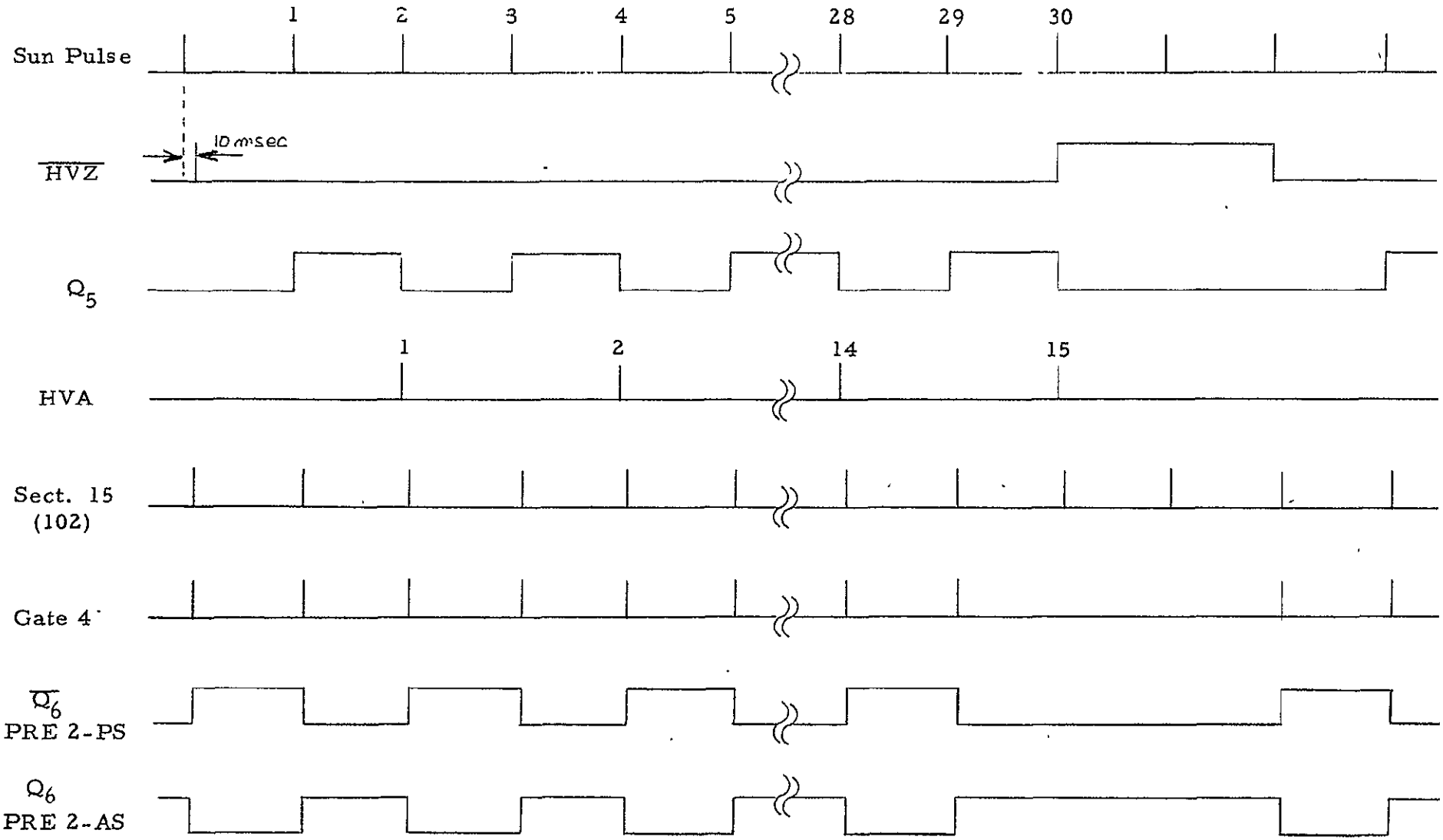


Mode Timing AS and PS Logic Diagram

Figure 3.2.1-9

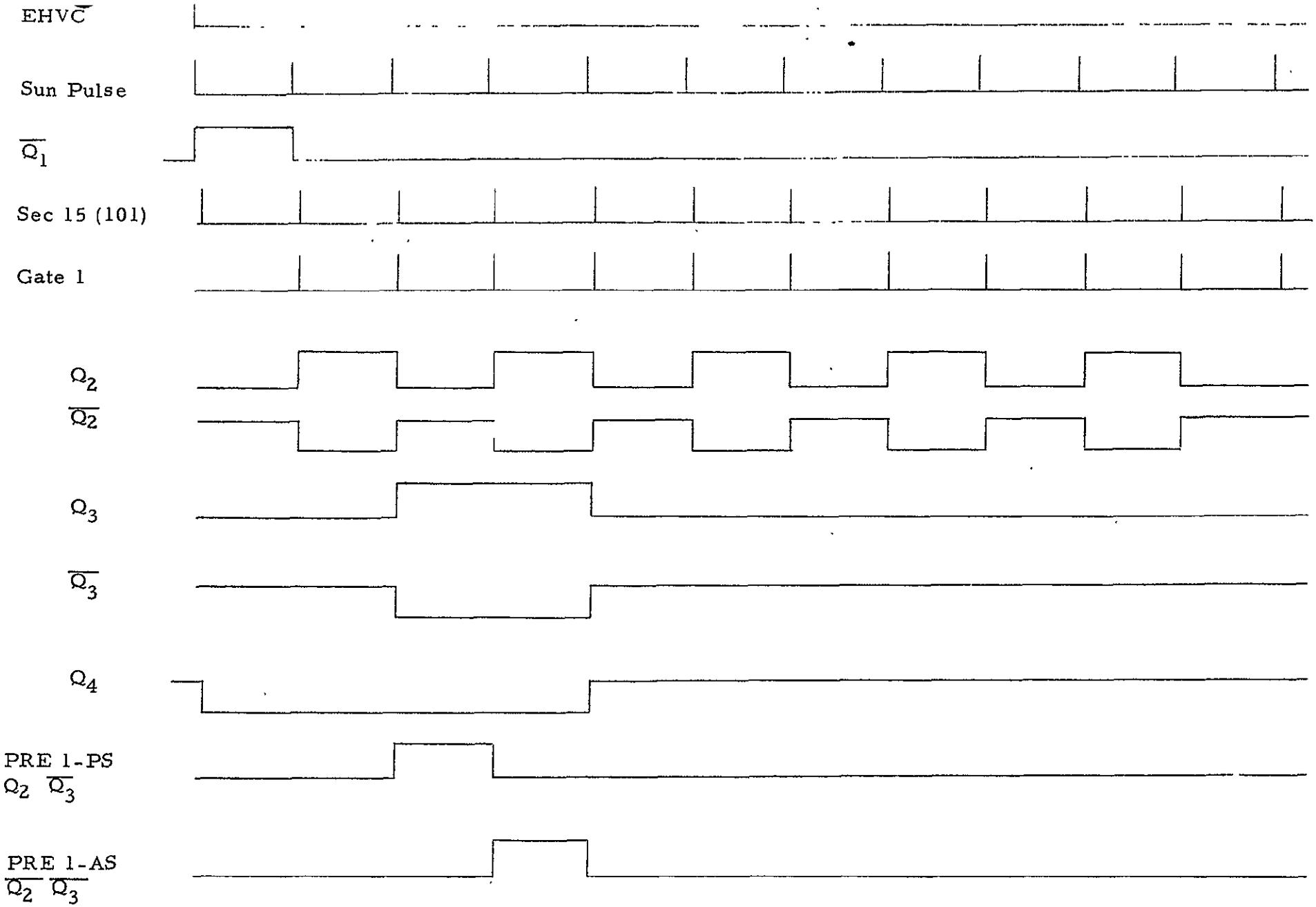


Logic Diagram Mode Timing
MFS, HBR, LBR, RETSR
Figure 3.2.11-10



PRE 2 Timing Diagram

Figure 3.2.1-11



PRE 1 Timing Diagram
Figure 3.2.1-12

The PRE 1 signals determine the AS and PS sequence for LBR operation while the PRE 2 signals determine the sequence for HBR operation.

A pulse which is generated at the end of High Voltage Cycle resets Flip-Flops 1, 2, 3 and 4. $\overline{Q1}$ inhibits Gate 1. The set input of Flip-Flop 1 is connected to +V so that the next Sun Pulse sets Flip-Flop 1; Flip-Flop 1 remains set until the next End High Voltage Cycle (EHVC). The setting of Flip-Flop 1 enables Gate 1.

The next four 101 signals of Sector 15 drive the 3 stage counter. At the 4th count, Q4 goes positive, inhibiting Gate 1. The counter remains in this state until the next EHVC.

Between the counts of 2 and 3 PRE 1-PS is positive and between 3 and 4 PRE 1-AS is positive.

The PRE-2 signals are generated by the toggling of Flip-Flop 6 by the 102 signal of Sector 15. If Flip-Flop 6 is initially in the wrong phase, it will be reset by the High Voltage Advance (HVA) pulse. The 102 signal is inhibited by the $\overline{\text{High Voltage Zero}}$ ($\overline{\text{HV Z}}$) signal which normally occurs every 15th HVA pulse.

The HVA is generated by a one-shot which is triggered by the resetting of Flip-Flop 5. This flip-flop is toggled by the Sun Pulse (except during HVZ).

If Flip-Flop 5 starts out of phase with the PRE-2 signals, they become synchronized at the next HVZ period.

The PRE-1 and PRE-2 signals are then gated with the LBR and HBR voltage levels to produce the proper PS and AS sequences at Low and High Bit Rates.

MFS is generated by the setting and resetting of a flip-flop. This flip-flop is clocked by the 102 signal of Sector 15. The EHVC resets Flip-Flop 7. The next 102 pulse of Sector 15 resets Flip-Flop 8, switching MFS to low. Then when the BS is Empty pulse sets Flip-Flop 7, the next 102 pulse sets Flip-Flop 8, making MFS true.

HBR and LBR are generated by a flip-flop whose state is determined by the Bit Rate levels from the spacecraft. During DCSM, LBR is held in the "True" state.

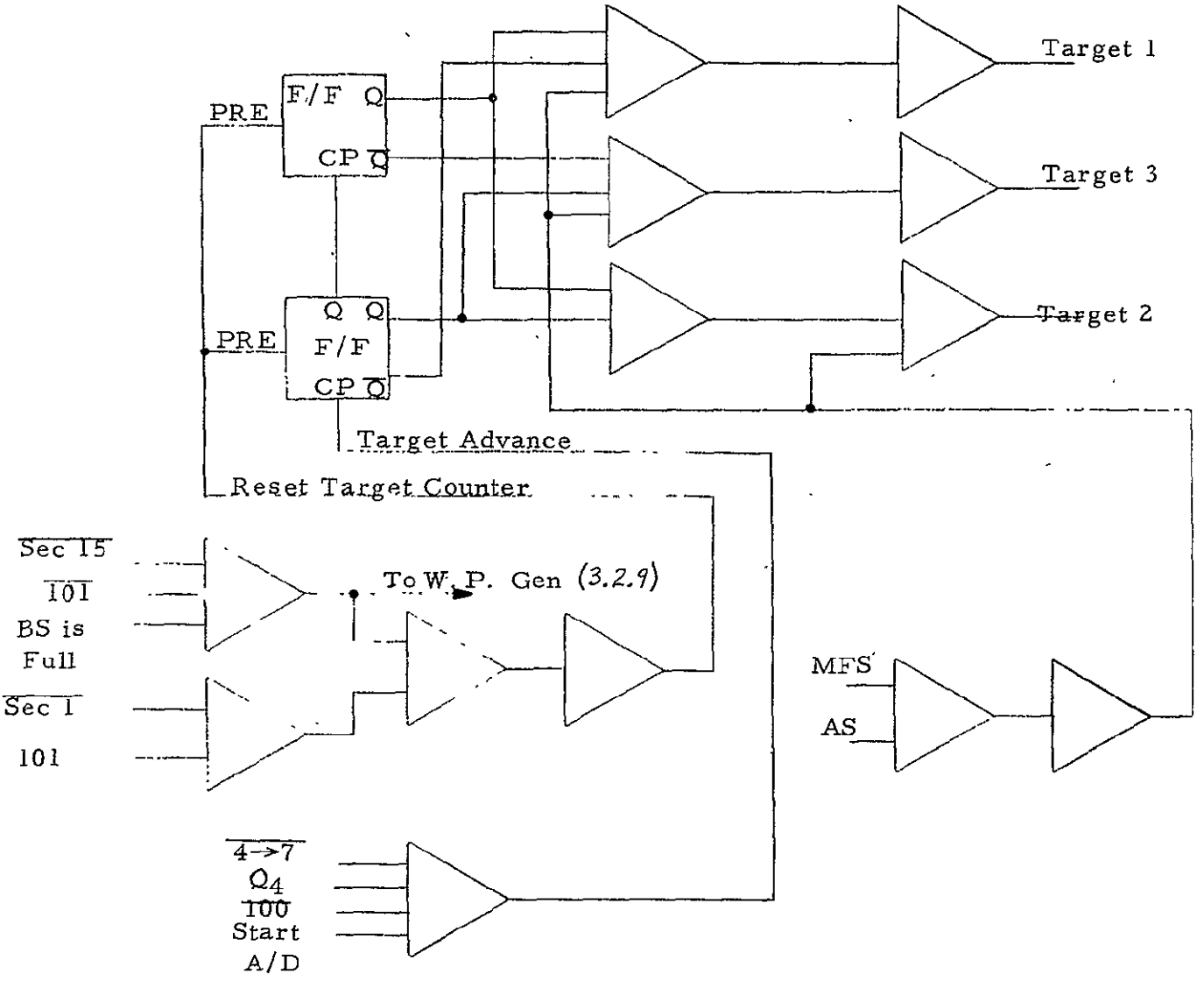
The Reset Long Term Storage Register signal occurs when the instrument is operating at Low Bit Rate. The 101 pulse of Sector 126 during PRE-1 AS triggers a one shot. The output of the one-shot is gated with HBR to produce Reset Long Term Storage Register (RLTSR) at Low Bit Rate.

3.2.2 Target Programmer

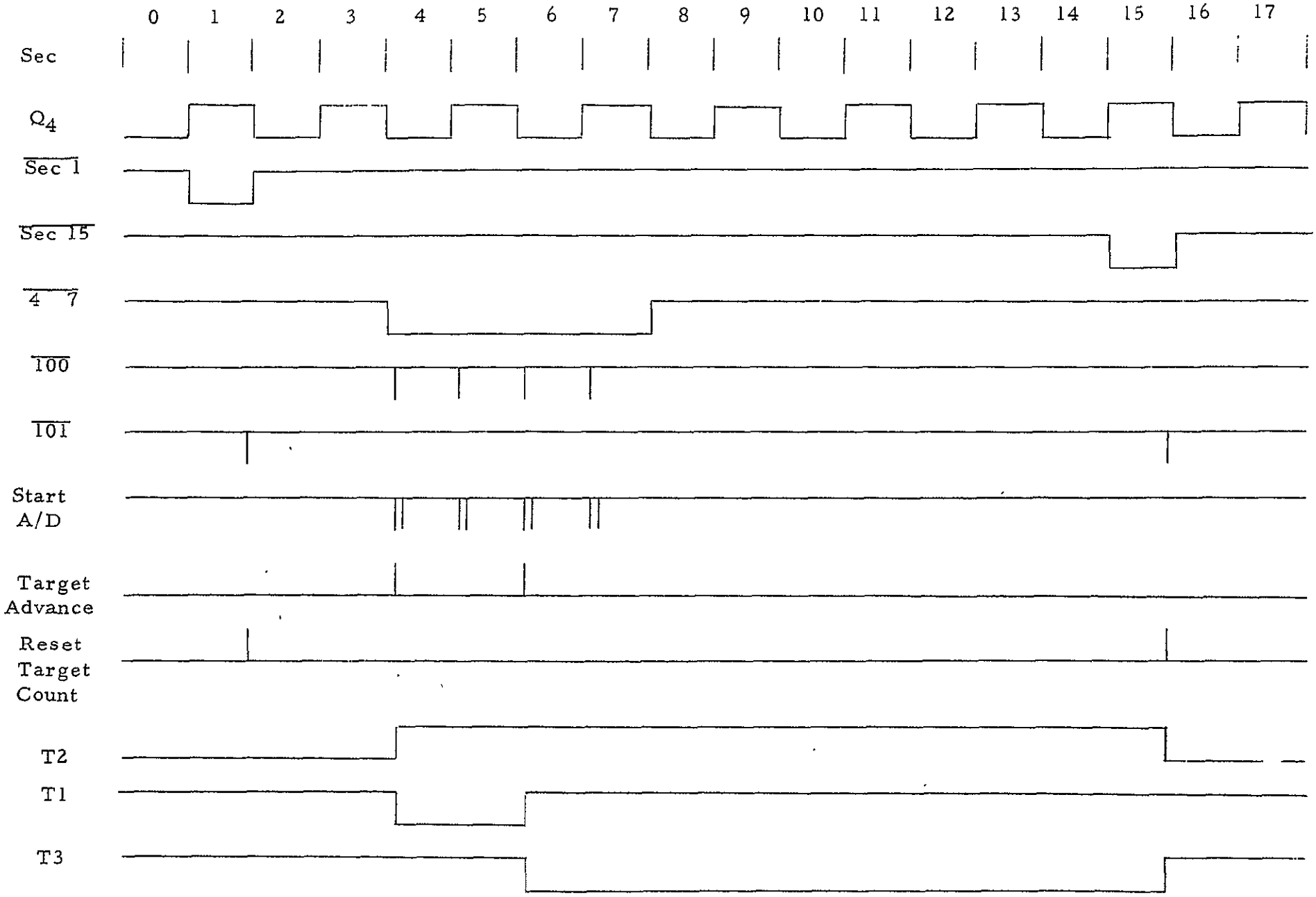
The three targets are continuously generating flux information. However, these outputs are scanned in a pre-determined sequence to allow proper target into an Intermediate Storage Register. The Target Programmer controls this sequencing.

Figures 3.2.2-1 and 3.2.2-2 show the Target Programmer Logic Diagrams and Timing, respectively.

At the Sun Pulse, which initiates Sector 0, the Target Counter should be in the "0" state. To assure this state at the beginning of the PS mode, a Target Counter Reset pulse is generated at 101 time of Section 1. The outputs of the flip-flops are gated to generate the proper scanning sequence. Thus, Target 2 is scanned from Sector 0 until 100 time of Section 4. At this time a Target Advance pulse sets the counter to 1, 0, and target 1 is scanned.



Target Programmer Logic Diagram
Figure 3.2.2-1



Target Programmer Timing Diagram
Figure 3.2.2-2

At 100 of Sector 6 the counter is advanced again to 0, 1, and Target 3 is scanned. At 101 of Sector 15 the counter is reset to 0, 0,, and Target 2 is scanned for the rest of the Sun Pulse period.

During this period the instrument must be in MFS or AS. A signal corresponding to these modes forces the inhibiting of the 1 and 3 Target scans and the enabling of Target 2 scan in case the counter is toggled by noise.

3.2.3 Digital Comparator and Long Term Storage Register

There are three Digital Comparators in the system. Each Pulse Width Modulated (PWM) flux is converted to a digital number in one of these comparators. In addition, one of these circuits is used as a Long Term Storage Register (LTSR). That is, during MFS it is used to determine when a maximum flux has been detected and at what time to signal the HV programmer to "remember" that HV step.

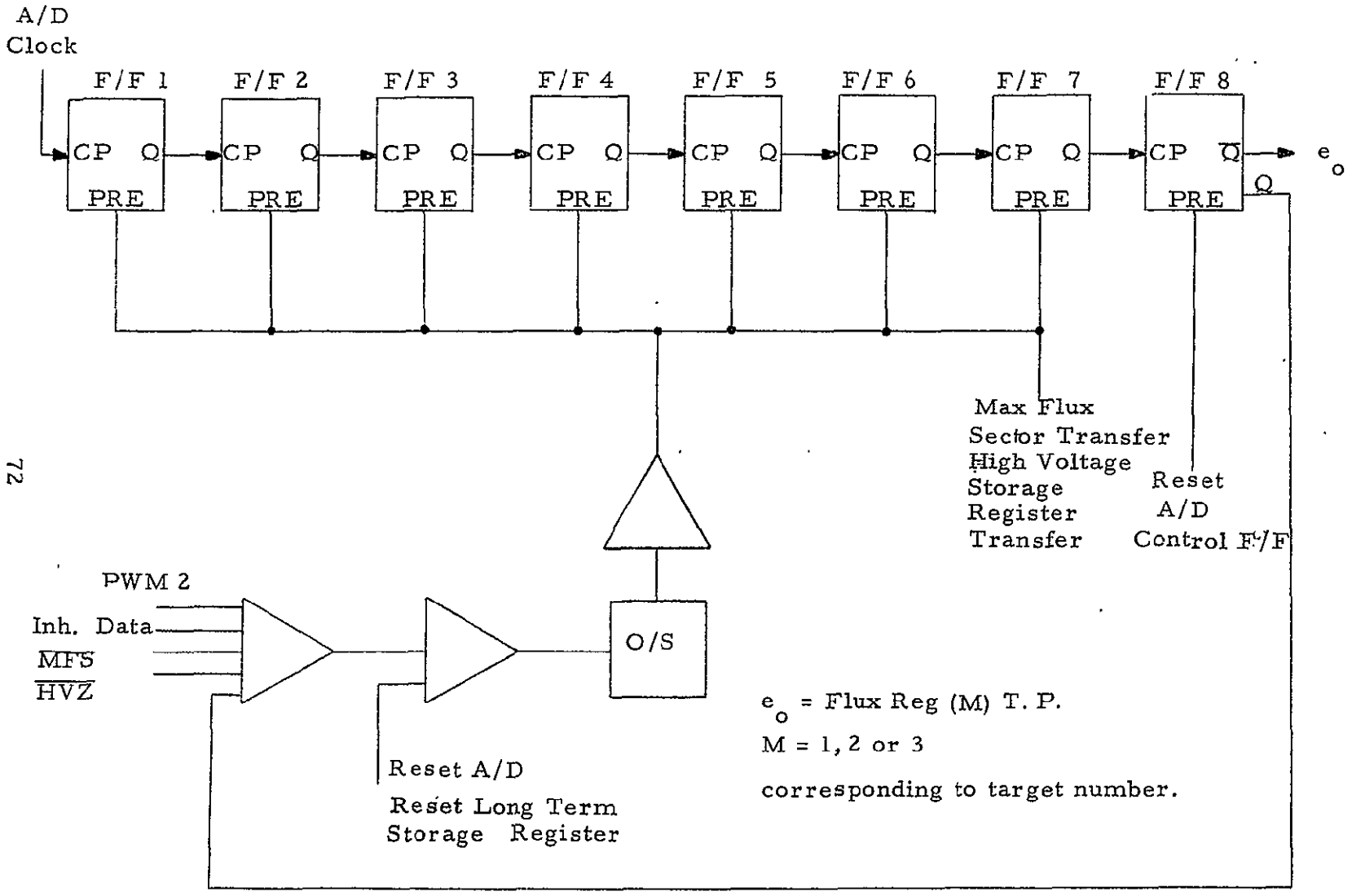
Refer to Figure 3.2.3-1 for the logic diagram of the Digital Comparator and Long Term Storage Register.

Digital Comparator

At the Start A/D pulse, PWM goes high and the A/D clock starts feeding into the counter. When PWM falls, the one shot is triggered and the counter is reset to zero. However, the clock continues. For example, if PWM falls at the count of 30, at the end of the clock burst there would be a count of

$$128-30 = 98P$$

in the counter. At the next Start A/D, PWM again goes high and the clock feeds the counter. If at this time PWM falls at a lower count, for example 25 (representing a larger flux count), the count would have reached 98+25 = 125. The fall of PWM again sets the counter to zero but the remainder of the clock burst enters the counter. Therefore, the counter now has a stored count of 128-25 = 103.



Logic Diagram, Digital Comparator and Long Term Storage Register

Figure 3.2.3-1

If the second PWM mentioned above falls at larger count than the original, for example 35, Flip-Flop 8 will be set at the 30th count. The rise of Q8 prevents the fall of PWM from resetting the counter; therefore, the full 128 counts enter the counter, resulting in the original count of 98.

At the next start A/D, PWM again rises and the clock burst enters the counter. After the first clock pulse, Flip-Flop 8 is reset and the sequence continues as explained above.

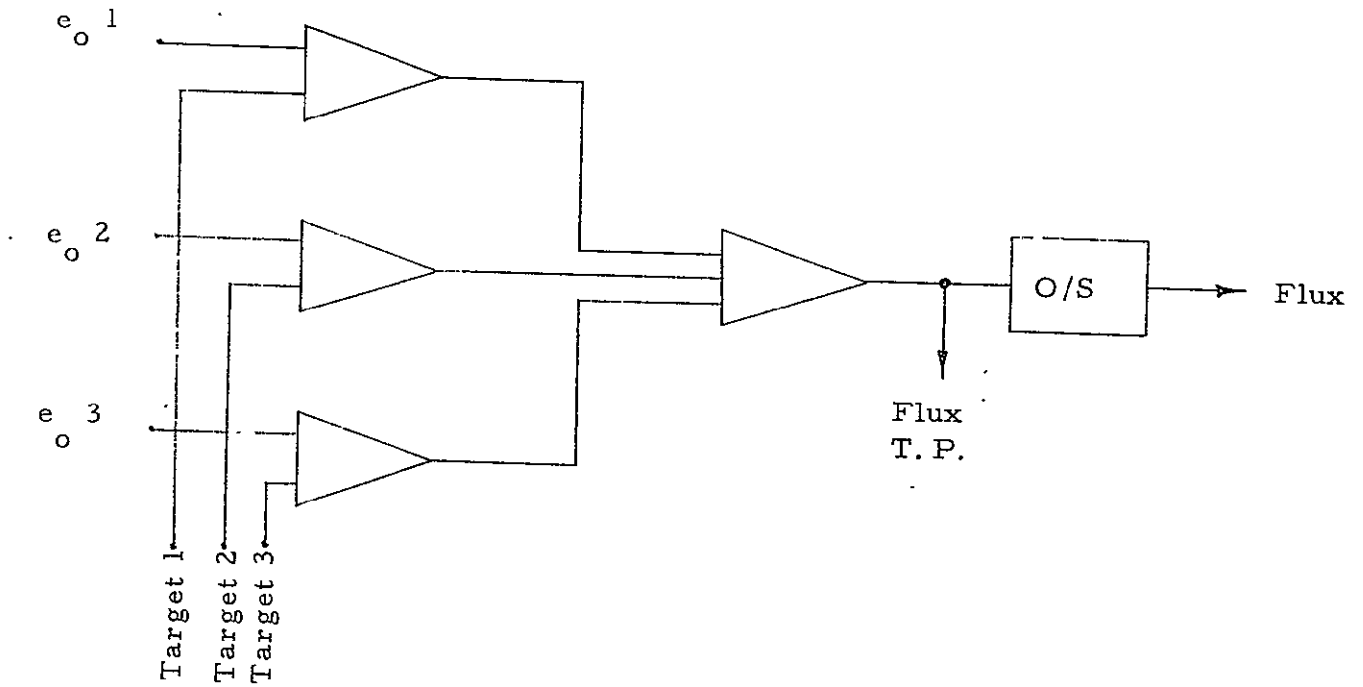
When a new maximum is detected, the fall of PWM again resets the counter. This reset signal is called the Maximum Flux Sector Transfer and operates on the Sector Register.

When the content of the counter is to be read out, Inhibit Data inhibits the PWM signal while the clock burst proceeds to fill the counter, at which time $\overline{Q8}$ (e_o) falls. For example, if a count of 98 were in the counter, the 30th clock pulse sets Flip-Flop 8 and e_o falls. The time required for e_o to fall might be described as the complement of the time duration of the PWM responsible for the count of 98.

The output (e_o) of each counter is gated with the appropriate Target Programmer output so that these counters are read out in the correct sequence (See Figure 3.2.3-2), Flux Register Commutator). The Timing between the Start A/D pulse and the one-shot output pulse (Flux) is a function of measured flux.

Long Term Storage Register

In this usage, the circuit operates identically to the Digital Comparators. The circuit is just reset by the Reset Long Term Storage Register (RLTSR) pulse. The circuit then detects maximum flux from Target 2 only.



Flux Register Commutator
Figure 3.2.3-2

The reset signal caused by PWM2 switching to a "0" level (High Voltage Storage Register Transfer) causes the HV Programmer to "remember" that voltage level at which the maximum flux was measured. PWM2 is inhibited by Inhibit Data or by $\overline{\text{High Voltage Zero (HVZ)}}$; it is also inhibited when not in MFS mode.

The output $\overline{Q8}$ is not used.

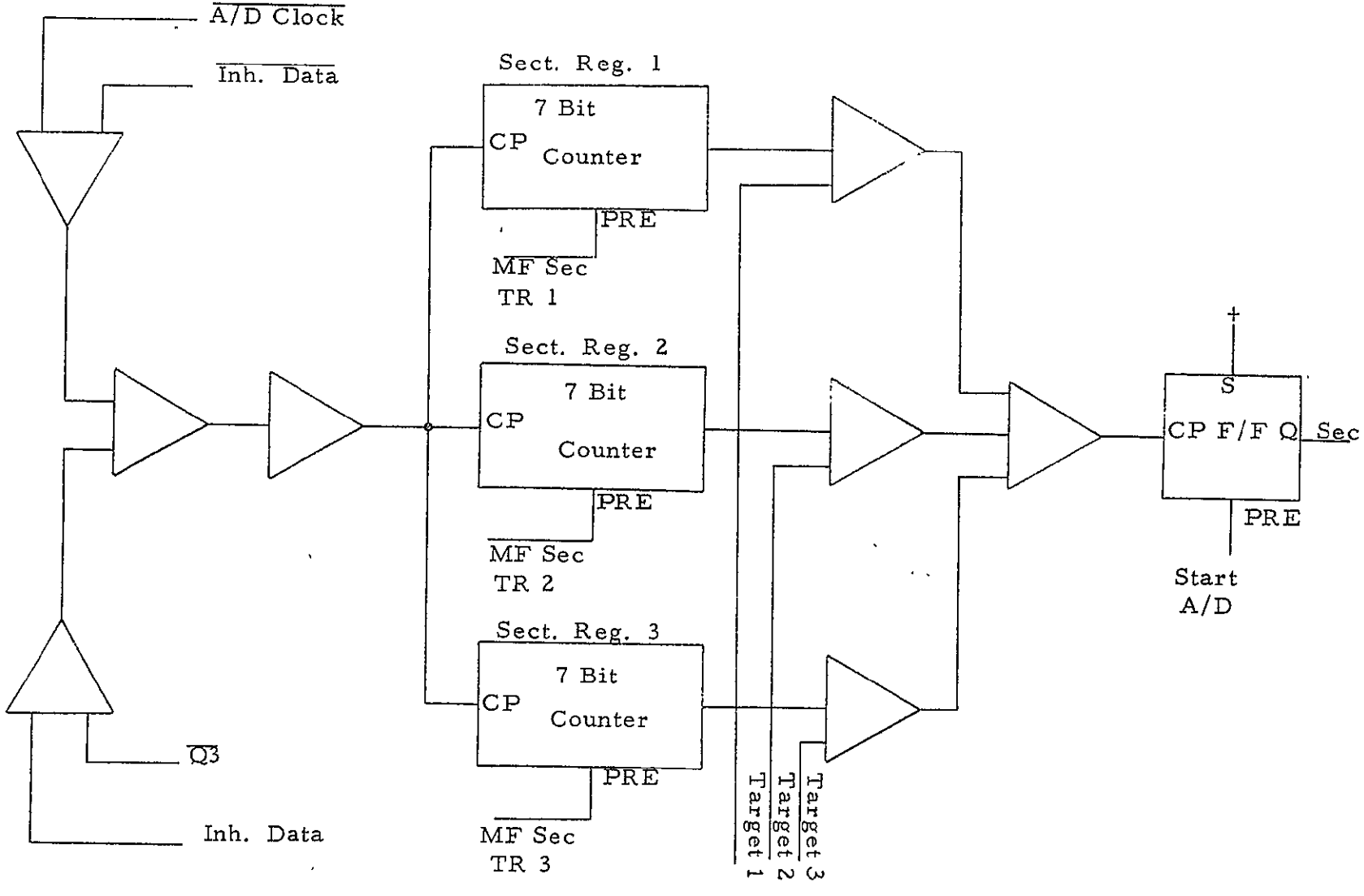
The output (e_o) of each counter is gated with the appropriate Target Programmer output so that these counters are read out in the correct sequence (See Figure 3.2.3-2, Flux Register Commutator). The timing between the Start A/D pulse and the one-shot output pulse (Flux) is a function of measured flux.

3.2.4 Sector Programmer

The Sector Programmer detects that sector between 16 and 127 during which a maximum flux is detected while in MFS and PS modes. During MFS, only that information from Target 2 is used.
Refer to Figure 3.2.4-1 for the logic diagram.

At Sector 16 Inhibit Data goes low and the $\overline{Q3}$ signal from the Spoke Generator toggles the 7 bit counters once each sector. When a maximum flux has been detected, for example at Target 1, that 7 bit counter is reset to zero. However, $\overline{Q3}$ keeps toggling the counter until Sector 127. At this time a number representing the complement of the Sector number is stored in the counter.

At Sector 0, $\overline{\text{Inhibit Data}}$ goes low and the A/D clock circulates the data through the counters, once for each A/D burst. Assume Target 1 Line is enabling the Sector Register 1 Gate. When this counter reaches the count of 128, the output flip-flop is set.



Sector Programmer Logic Diagram
Figure 3.2.4-1

The output of this flip-flop is a pulse whose width corresponds to the number of clock pulses which represents the Sector number whose complement is stored in the Sector Register.

As an example, suppose a maximum flux was detected at Sector 30 by Target 1. At this time, Sector Register 1 is reset to zero. The register is then toggled 97 more times by $\overline{Q3}$; Inhibit Data then goes True. The next A/D clock burst circulates the number 97 in the register. It will take 30 clock pulses to fill the counter and reset to zero. If Target 1 line is down, this overflow from the register sets the output flip-flop. Thus, it takes 30 A/D clock pulses to set the output flip-flop.

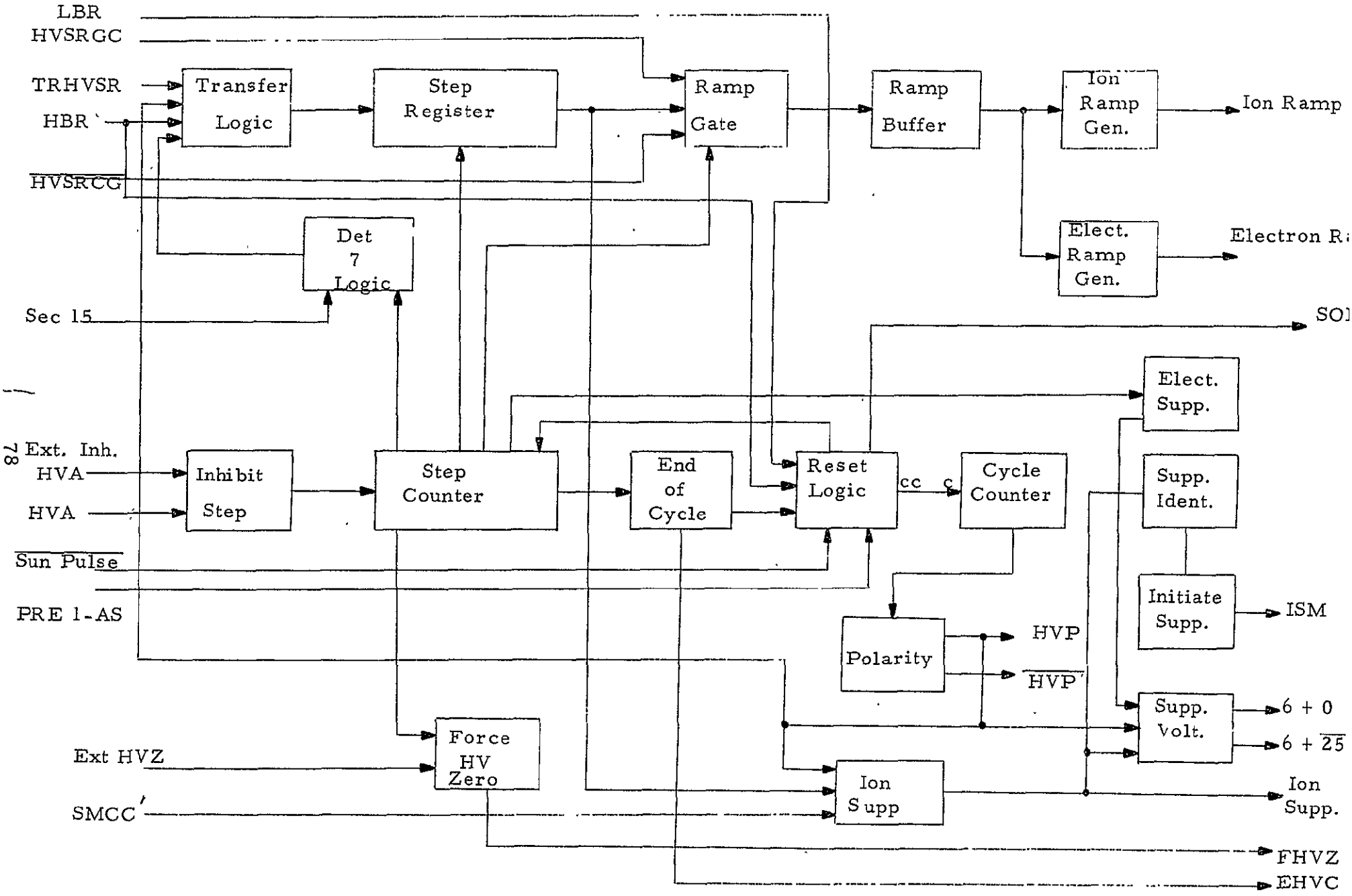
The contents of the other two registers are detected in like manner.

3.2.5 High Voltage Programmer

Figure 3.2.5-1 shows the High Voltage Programmer Block Diagram.

Characteristics of the High Voltage Programmer are as follows:

- Generates 30 logarithmic ion ramp steps (From 42 mv ± 1 mv to 3.000 v ±45 mv)
- Generates 15 logarithmic electron ramp steps (From 0.000 mv ±2 mv to 3.000 v ± 30 mv).
- Generates 7 cycles of 30 ion steps followed by 1 cycle of 15 electron steps in both High Bit Rate and Low Bit Rate.
- Operates in one of 3 modes of Electron suppression during Ion analysis cycles:
    a. All Ion cycles suppressed
    b. All Ion cycles unsuppressed
    c. First 3 Ion cycles unsuppressed, 4th suppressed, last 3 unsuppressed (Automatic)
- These modes can be changed from one to another by Earth Command.



High Voltage Programmer Block Diagram
Figure 3.2.5-1

The first 5 steps of Electron cycle are unsuppressed, the last 10 steps are suppressed.

During Ion cycles at Low Bit Rates and while in MFS, a register stores that HV level at which maximum flux was detected. Then during the following PS and AS, that HV level can be selected. During Electron cycle, the register stores the 7th step.

- Provides a forced HV Zero (FHVZ) at the end of the 15th step.
- Provides that the step response of the reference signal be compatible with the HVPS step response requirements.
- Is capable of reducing the energy threshold from 15,000 to 9,000 ev in Ion mode and from 1,000 to 480 ev in Electron mode by changing one module in the programmer and one gain resistor in the HVPS.
- Generates an End of Hi Voltage Cycle (EHVC) signal at the end of each Ion and Electron cycle.
- Provides polarity reversal logic to the HVPS.

Refer to Figure 3.2.5-1 for a block diagram of the HV Programmer.

The Programmer consists of 2 counters, a register, 2 ramp generators and associated control logic.

The High Voltage Advance (HVA) signal causes the 5 bit step counter to step through 30 counts, which are associated with the 30 Ion steps. The External Inhibit HVA prevents the programmer from stepping during test and calibration.

After 30 steps, a count is placed in the cycle counter. After 7 Ion cycles, the reset logic resets the step counter to 17. Then the next 15 electron steps fill the counter; it is reset to a count of 2 and is ready for the next 30 Ion steps.

An End High Voltage Cycle (EHVC) pulse is generated at the end of 30 Ion steps or 15 Electron steps.

Force High Voltage Zero (FHVZ) forces the High Voltage to zero at the end of each 15th step.

During Ion cycle at LBR, the Step Register stores the HV level at which maximum flux was detected. During Electron cycle at LBR, the Detect logic detects the 7th HV level. The output of this circuit transfers the 7th step from the step counter to the step register.

The Ion Suppression logic determines when Ion suppression will occur.

The Electron Suppression logic determines when Electron suppression will occur.

The Suppression Identification logic supplies a signal to indicate when suppression is ON or OFF.

The Polarity Logic causes the analyzer plate voltages to assume the correct polarity.

The Ramp Gates determine which outputs from the Step Register shall be supplied to the Ramp Buffer.

The Ramp Buffer interfaces the Ramp Gates to the Ramp Generators.

The Ion Ramp Generator is a 30 step logarithmic staircase generator.

The Electron Ramp Generator is a 15 step logarithmic staircase generator.

The Initiate Suppression Logic generates a command to start the suppression mode.

3.2.5.1 High Voltage Advance

The Sun Pulse is gated with $\overline{LBR}$ to generate the HVA at Low Bit Rate (LBR). The development of $\overline{HVA}$ at High Bit Rate is explained in Section 3.2.1.7 (Mode Timing). The Sun Pulse is gated with $\overline{HBR}$ to generate HVA at High Bit Rate (HBR).

See Figure 3.2.5-2 and 3.2.5-3 for the High Voltage Advance Logic and Timing Diagrams, respectively.

HVA is inhibited whenever $\overline{HVZ}$ or Inhibit HVA and Write Pulse is high. At Low Bit Rate, HVA is also inhibited when $\overline{MFS}$ is True.

3.2.5.2 Inhibit Step Logic

Figure 3.2.5-4 shows the Logic Diagram and Timing Diagram for the Inhibit Step Logic.

The output of the Inhibit Step Logic, HVA', is the clock pulse for the Step Counter. $\overline{HVA'}$ is the signal for the HVZ logic. Ext HVA inhibits HVA and is used during calibration.

3.2.5.3 Step Counter

The Step Counter consists of five flip-flops. It counts 30 steps for an Ion cycle and 15 steps for an Electron cycle. The counter is driven by the HVA' signal.

Refer to Figure 3.2.5-5 for the Logic and Timing diagrams.

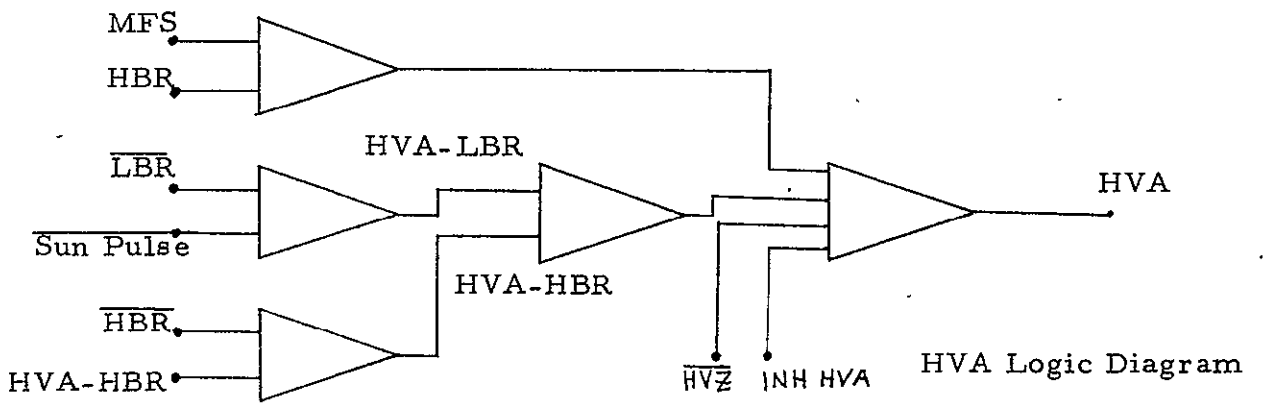
Table 3.2.5A shows the Truth Table for the step Counter.

The Step Counter is composed of 5 flip-flops. It has 30 steps for an Ion cycle and 15 for an Electron cycle. The counter is driven by the HVA' signal.

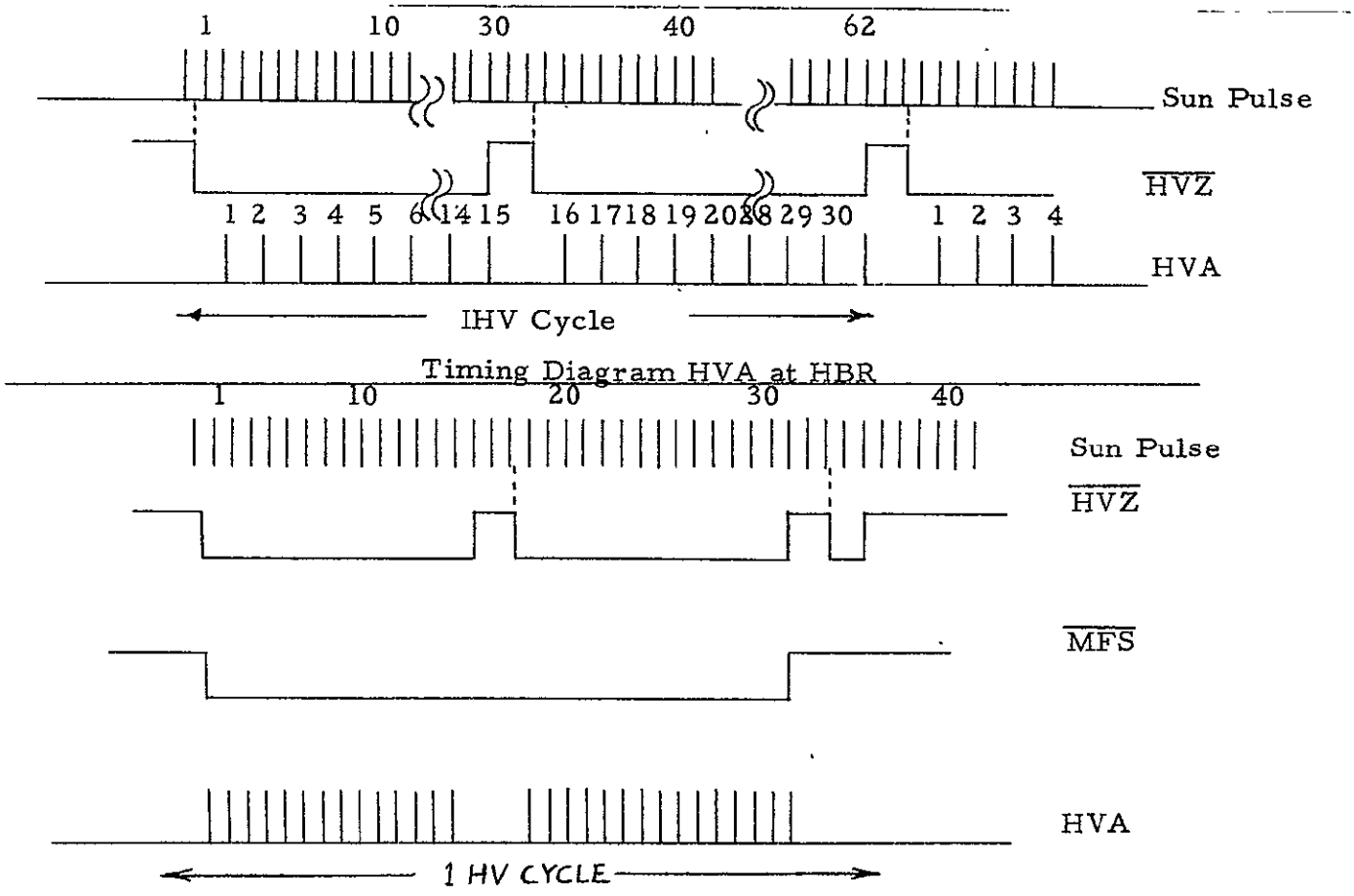
For Ion Reset, the counter is reset to a count of 2. Therefore, 30 counts will fill the counter and cause a reset.

For Electron Reset, the counter is reset to a count of 17. 15 counts are then necessary for fill and reset.

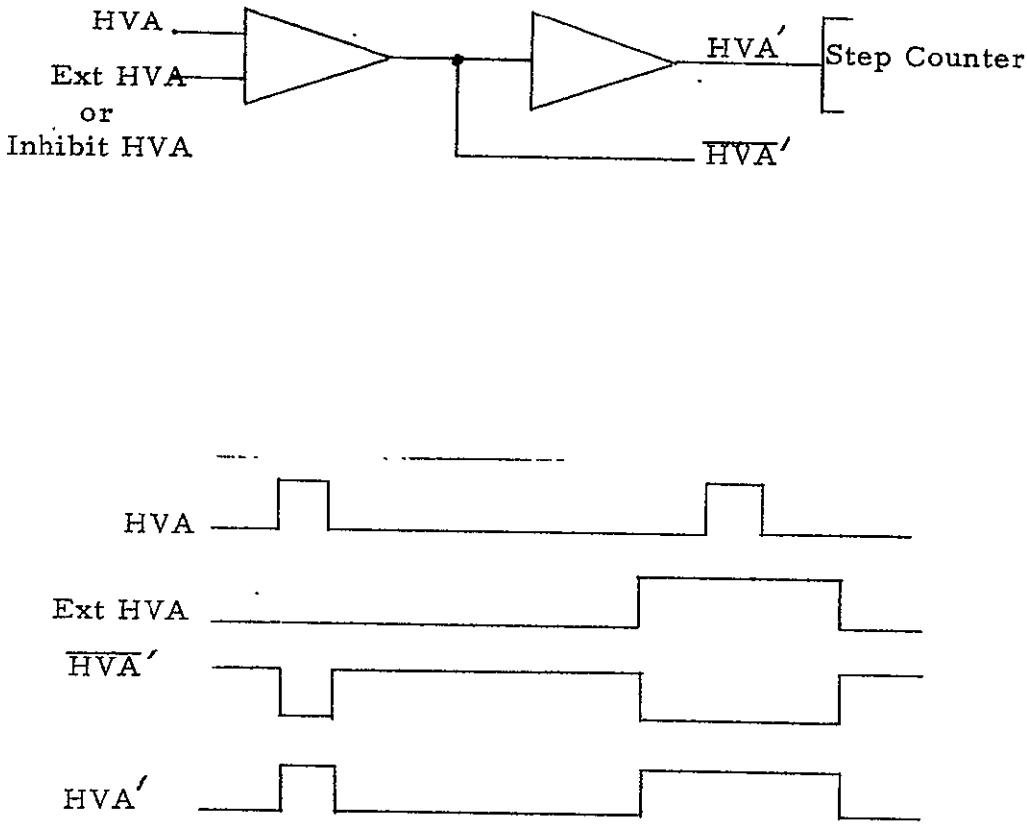
Reset is derived from Reset Logic.



High Voltage Advance Logic Diagram
Figure 3.2.5-2

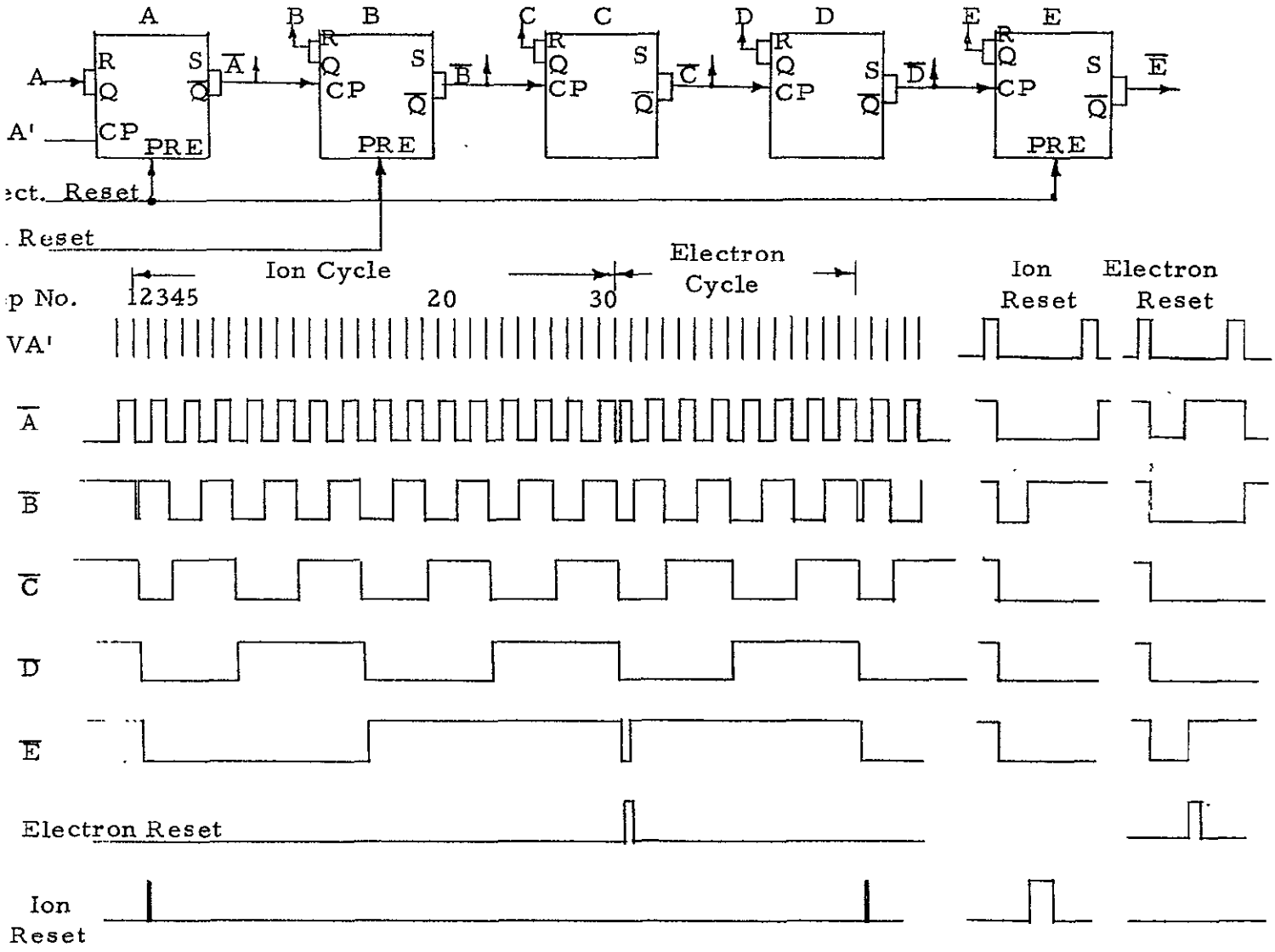


Timing Diagram, High Voltage Advance
Figure 3.2.5-3



Inhibit Step Logic, Logic Diagram
and Timing Waveforms

Figure 3.2.5-4



Step Counter Logic Diagram and
Timing Waveforms
Figure 3.2.5-5

TRUTH TABLE FOR STEP COUNTER

Ion Cycle							Electron Cycle						
Step	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	$\overline{E}$		Step	$\overline{A}$	$\overline{B}$	$\overline{C}$	$\overline{D}$	$\overline{E}$	
1	0	1	0	0	0	Binary No. 2	1	1	0	0	0	1	Bina No.1
2	1	1	0	0	0		2	0	1	0	0	1	
3	0	0	1	0	0		3	1	1	0	0	1	
4	1	0	1	0	0		4	0	0	1	0	1	
5	0	1	1	0	0		5	1	0	1	0	1	
6	1	1	1	0	0		6	0	1	1	0	1	
7	0	0	0	1	0		7	1	1	1	0	1	
8	1	0	0	1	0		8	0	0	0	1	1	
9	0	1	0	1	0		9	1	0	0	1	1	
10	1	1	0	1	0		10	0	1	0	1	1	
11	0	0	1	1	0		11	1	1	0	1	1	
12	1	0	1	1	0		12	0	0	1	1	1	
13	0	1	1	1	0		13	1	0	1	1	1	
14	1	1	1	1	0		14	0	1	1	1	1	
15	0	0	0	0	1		15	1	1	1	1	1	
16	1	0	0	0	1								
17	0	1	0	0	1								
18	1	1	0	0	1								
19	0	0	1	0	1								
20	1	0	1	0	1								
21	0	1	1	0	1								
22	1	1	1	0	1								
23	0	0	0	1	1								
24	1	0	0	1	1								
25	0	1	0	1	1								
26	1	1	0	1	1								
27	0	0	1	1	1								
28	1	0	1	1	1								
29	0	1	1	1	1								
30	1	1	1	1	1								

Table 3.2.5A, Step Counter Truth Table

3.2.5.4 Force High Voltage Zero Logic

This logic consists of 4 gates and one one-shot. At the count of 15, $\overline{HVA}$ generates a Detect 15 signal. This signal, or an Ext HVZ, triggers the one shot which has a typical delay of 785 μsec. The output of the one-shot is inverted to produce the FHVZ signal.

See Figure 3.2.5-6 for the Logic and Timing diagrams.

3.2.5.5 End-of-Cycle Logic

Figure 3.2.5-7 shows the Logic and Timing diagrams for the End-of-Cycle Logic. The negative transition of the E Flip-Flop of the Step Counter triggers the one-shot. The one-shot produces a 5 to 10 μsecond pulse which is inverted to become the End High Voltage Cycle (EHVC) signal.

3.2.5.6 Reset Logic

See Figure 3.2.5-8 and 3.2.5-9 for the Reset Logic and Timing diagrams, respectively.

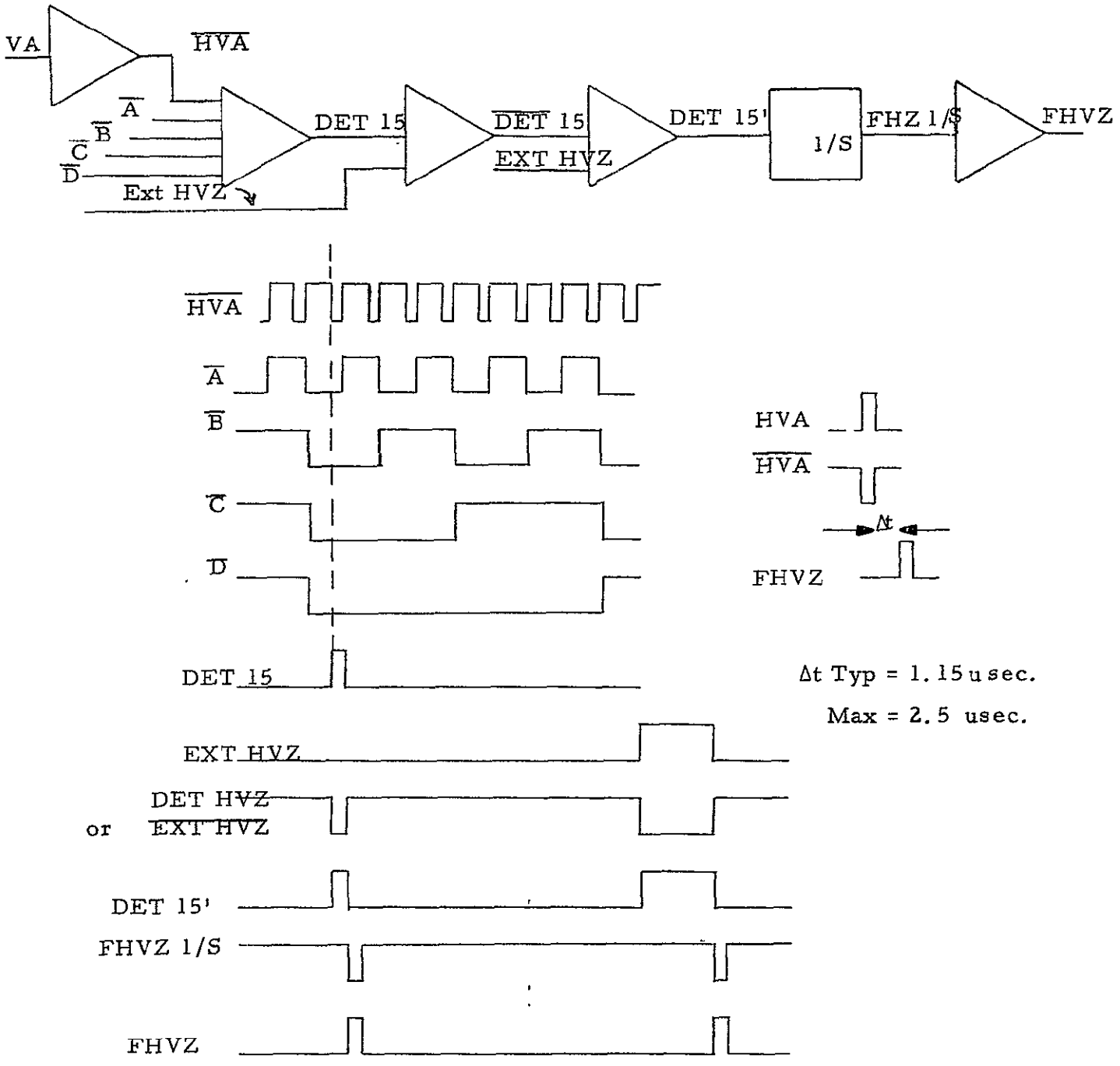
The Cycle Counter Clock (CCC) is generated by the EHVC one-shot at HBR or by the Sun Pulse which occurs at the end of the PRE1-AS period when in LBR. The $\overline{CCC}$ triggers a one-shot which generates the Reset Pulse. Gating this pulse with HVP and $\overline{HVP}$ produces the Ion Reset or the Electron Reset. Start of Electron Cycle (SofEC) is coincident with Electron Reset.

3.2.5.7 Step Register

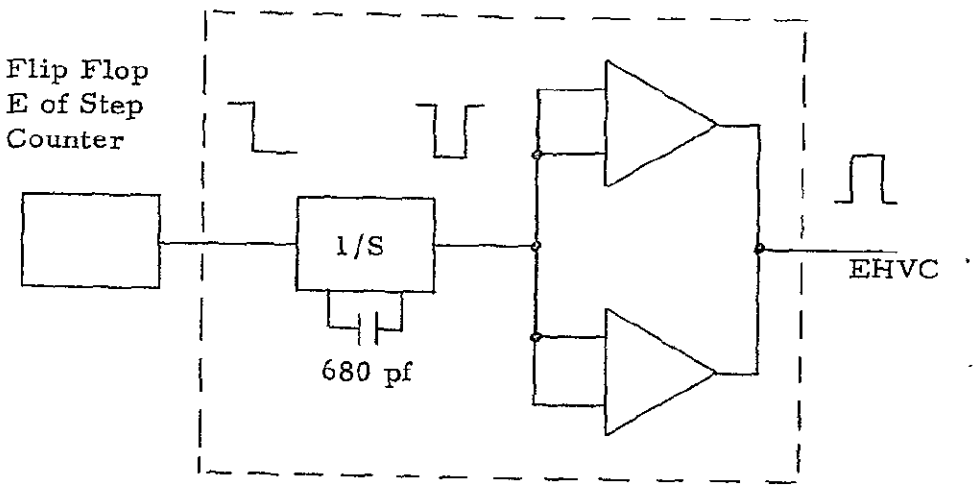
Figure 3.2.5-10 shows the Step Register Logic and Timing diagrams.

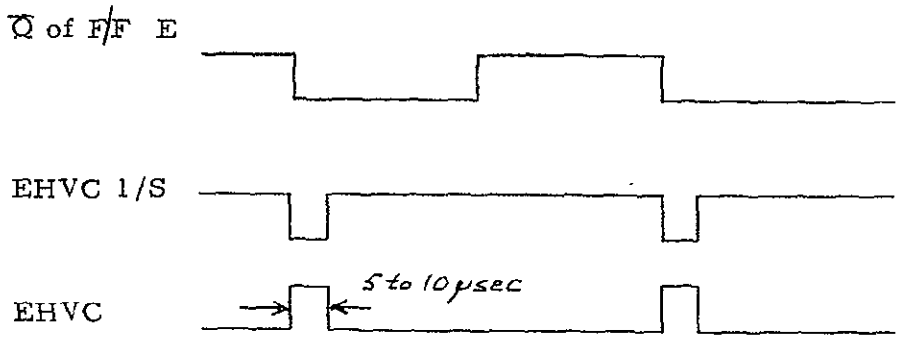
The Q and $\overline{Q}$ outputs of the Step Counter are connected to the Set and Reset inputs of the Step Register. The transfer pulse causes the information in the Step Counter to transfer to the Step Register.

Development of the transfer pulse is treated later.

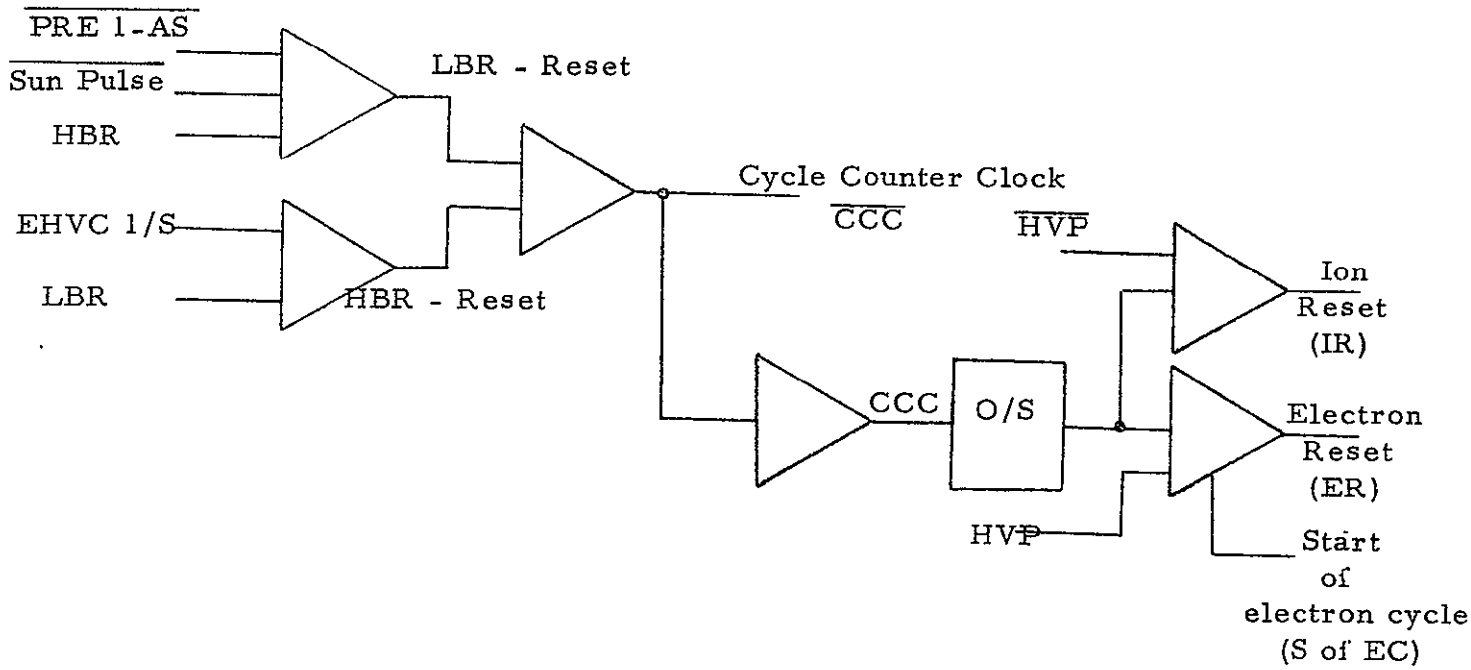


Force High Voltage Zero, Logic
and Timing Waveforms
Figure 3.2.5-6

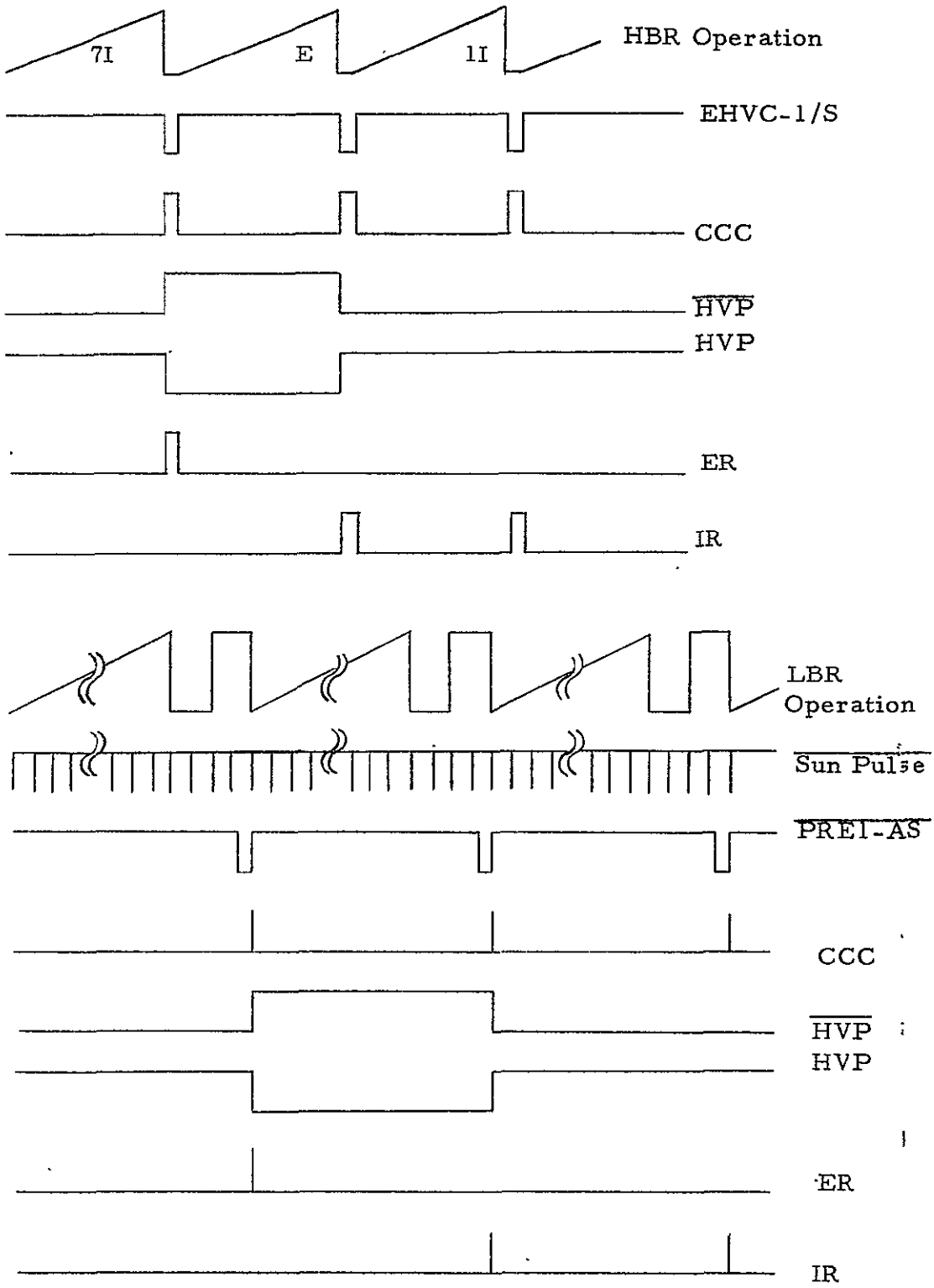




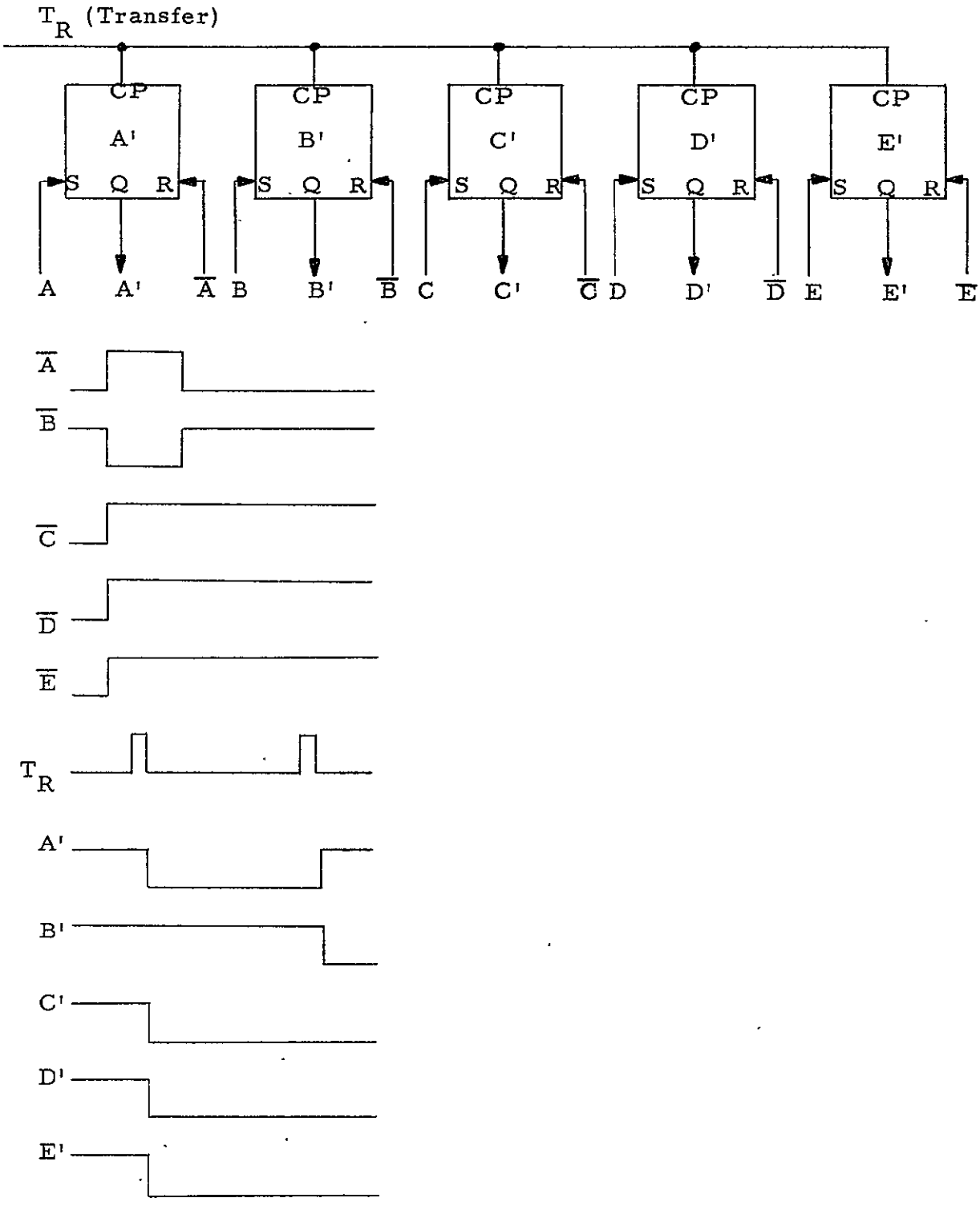
End-of-Cycle Logic Diagram
and Timing Waveforms
Figure 3.2.5-7



Reset Logic Diagram
Figure 3.2.5-8



Reset Logic Timing at HBR and LBR
Figure 3.2.5-9



Step Register Logic Diagram
and Timing Waveforms

Figure 3.2.5-10

3.2.5.8 Detect 7E Logic

See Figure 3.2.5-11, Detect 7E Logic and Timing diagrams.

When the Step Counter has reached a count of 7, a pulse corresponding to Sector 15 generates the Detect 7E signal.

3.2.5.9 Transfer Logic

Transfer High Voltage Storage Register (TR-HVSR) is generated when maximum flux is detected. This signal is gated with $\overline{\text{High Voltage Polarity (HVP)}}$ to produce Ion-Transfer (Ion-Tr). See Figure 3.2.5–12, Transfer Logic and Timing diagrams.

Det-7 is gated with HVP to produce Electron Transfer (El-TR). These signals are inhibited by HBR during High Bit Rate. When they are not being inhibited, they are gated to produce $\overline{\text{TR}}$, and then inverted to produce TR.

3.2.5.10 Ramp Gate

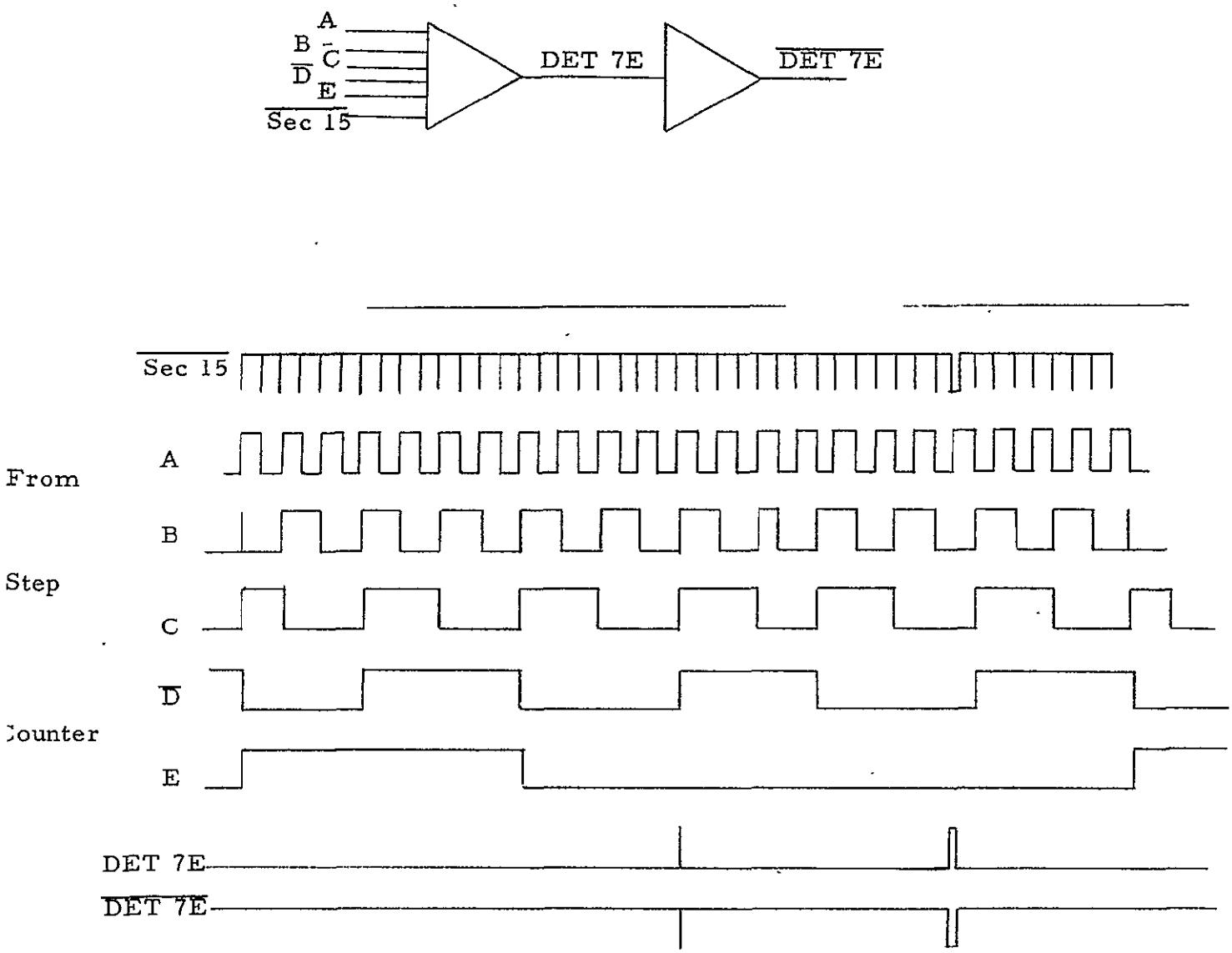
Refer to Figure 3.2.5-13, Ramp Gate Logic and Timing diagrams.

The Ramp Gate selects the outputs of the Step Counter at High Bit Rates or of the Step Register at Low Bit Rates. The High Voltage Storage Register Gate Control (HVSRGC) pulse inhibits the register output at HBR while $\overline{\text{HVSRGC}}$ inhibits the Counter outputs at LBR.

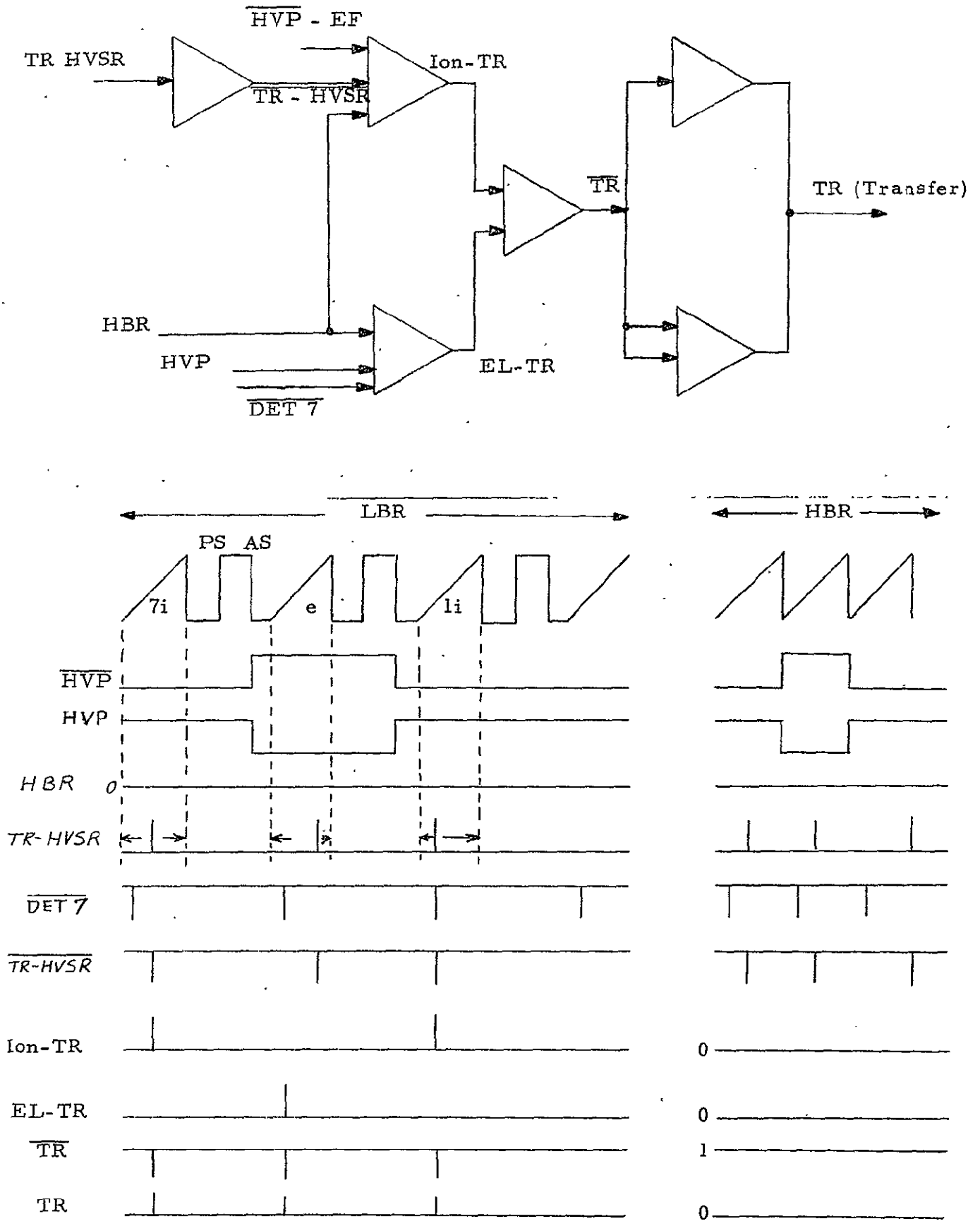
3.2.5.11 Cycle Counter Clock

Figure 3.2.5-14 shows the Logic and Timing diagrams for the Cycle Counter Clock. See Table 3.2.5B for the Truth Table.

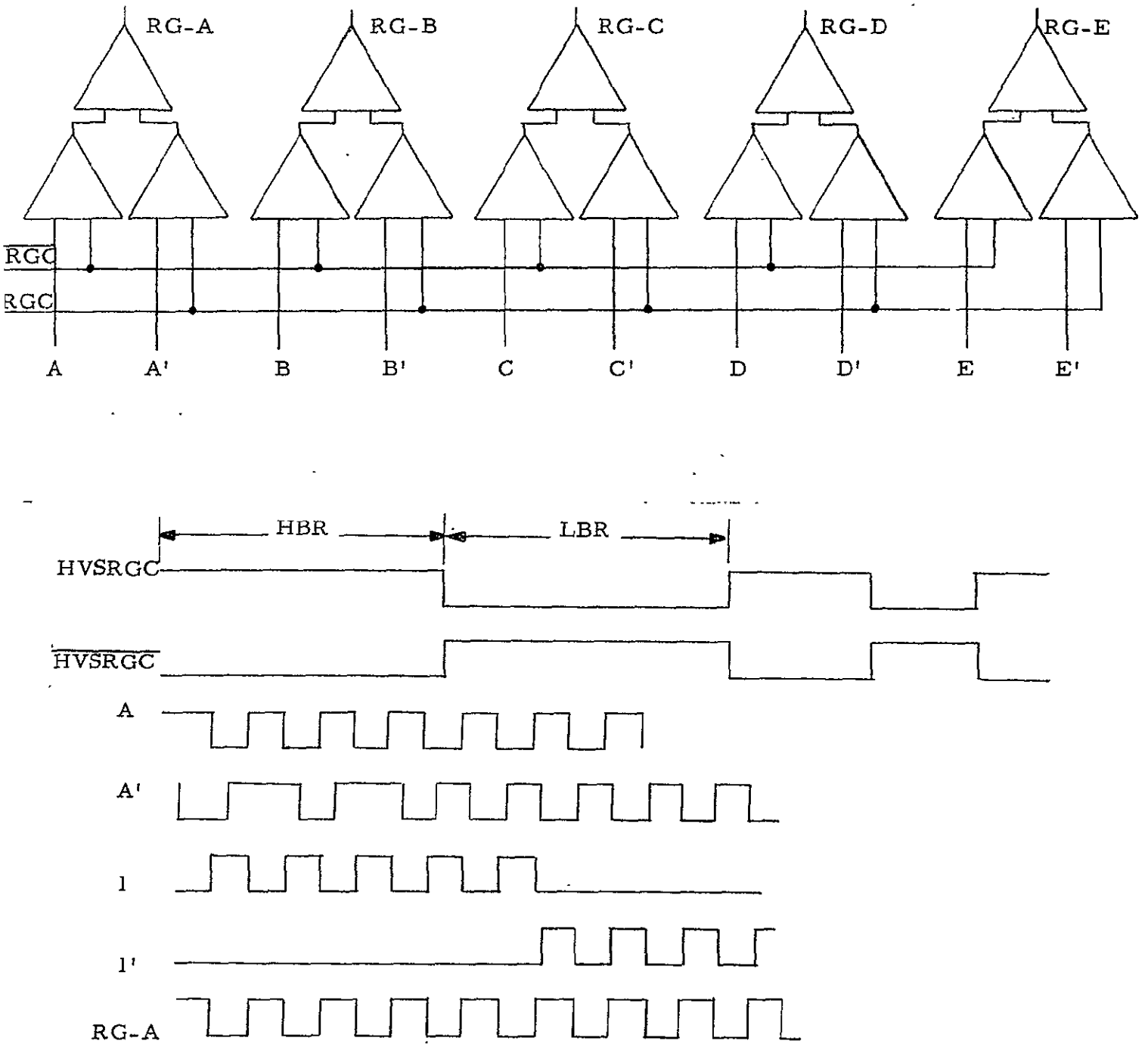
The Cycle Counter is toggled by CCC from the Reset Logic. The Truth Table shows the eight states through which the counter is sequenced. The F and I outputs are gated to reset the G and H Flip-Flops and cause the counter to skip the forbidden states.



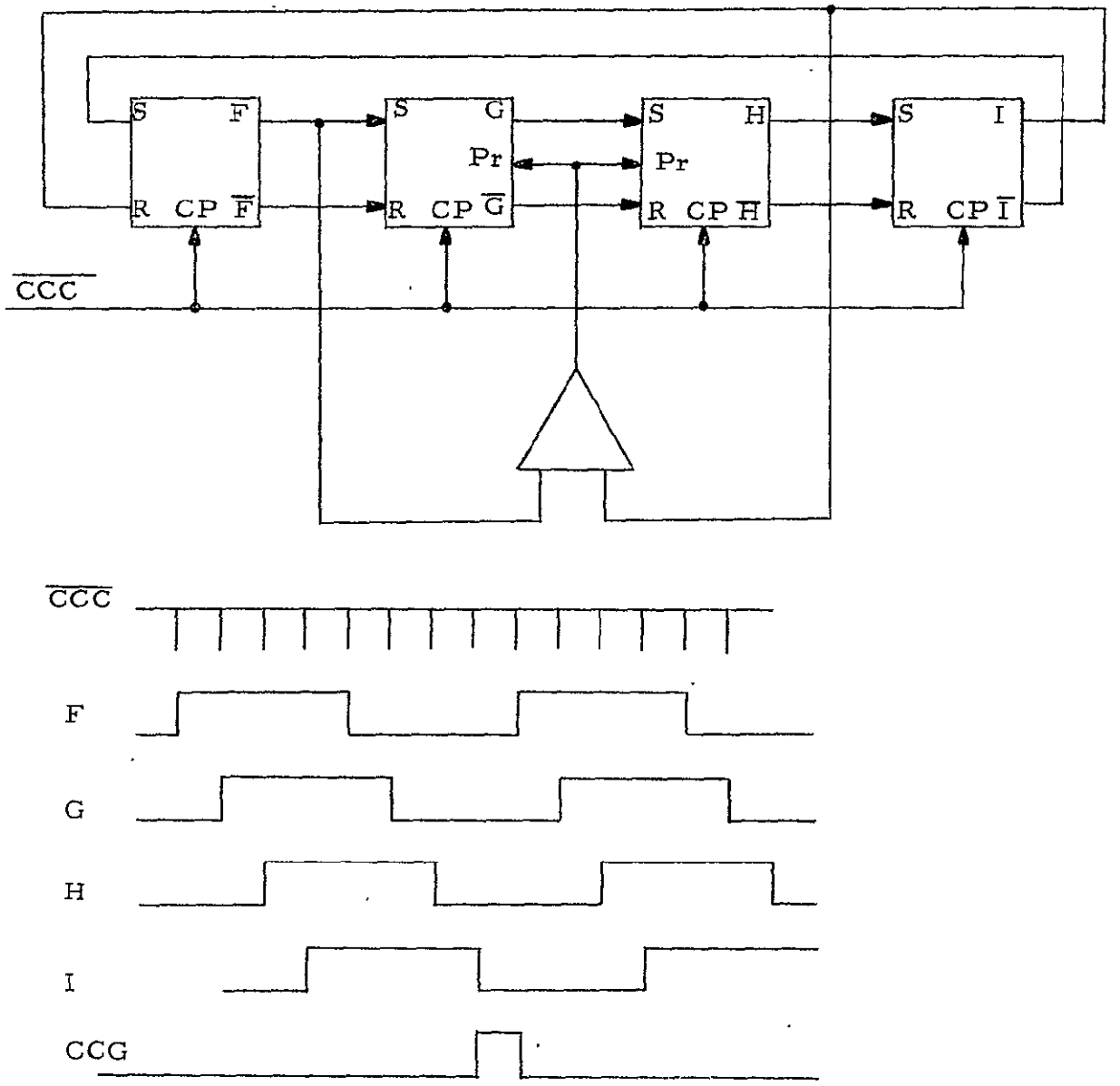
Detect 7E Logic Diagram and Timing Waveforms
Figure 3.2.5-11



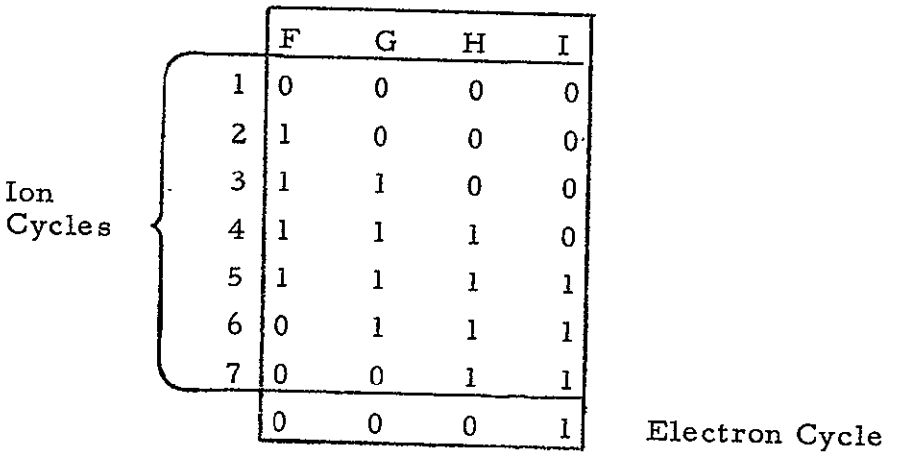
Transfer Logic Diagram and Timing Waveforms
Figure 3.2.5-12



Ramp Gate Logic Diagram and Timing Waveforms
Figure 3.2.5-13



Cycle Counter Clock,
Logic Diagram and Timing Waveforms
Figure 3.2.5-14



Cycle Counter Clock Truth Table
Table 3.2.5B

The H and I outputs are used to detect the 4th Ion Cycle and to generate the High Voltage Polarity (HVP) signal.

3.2.5.12 Polarity Logic

At an Electron cycle, H and $\overline{I}$ of the cycle counter are at a "0". These are gated to produce the $\overline{\text{High Voltage Polarity (HVP)}}$ signal. $\overline{HVP}$ is buffered with an emitter follower, then inverted to produce HVP. See Figure 3.2.5-15 for the Logic and Timing diagrams.

3.2.5.13 Ion Suppression Logic

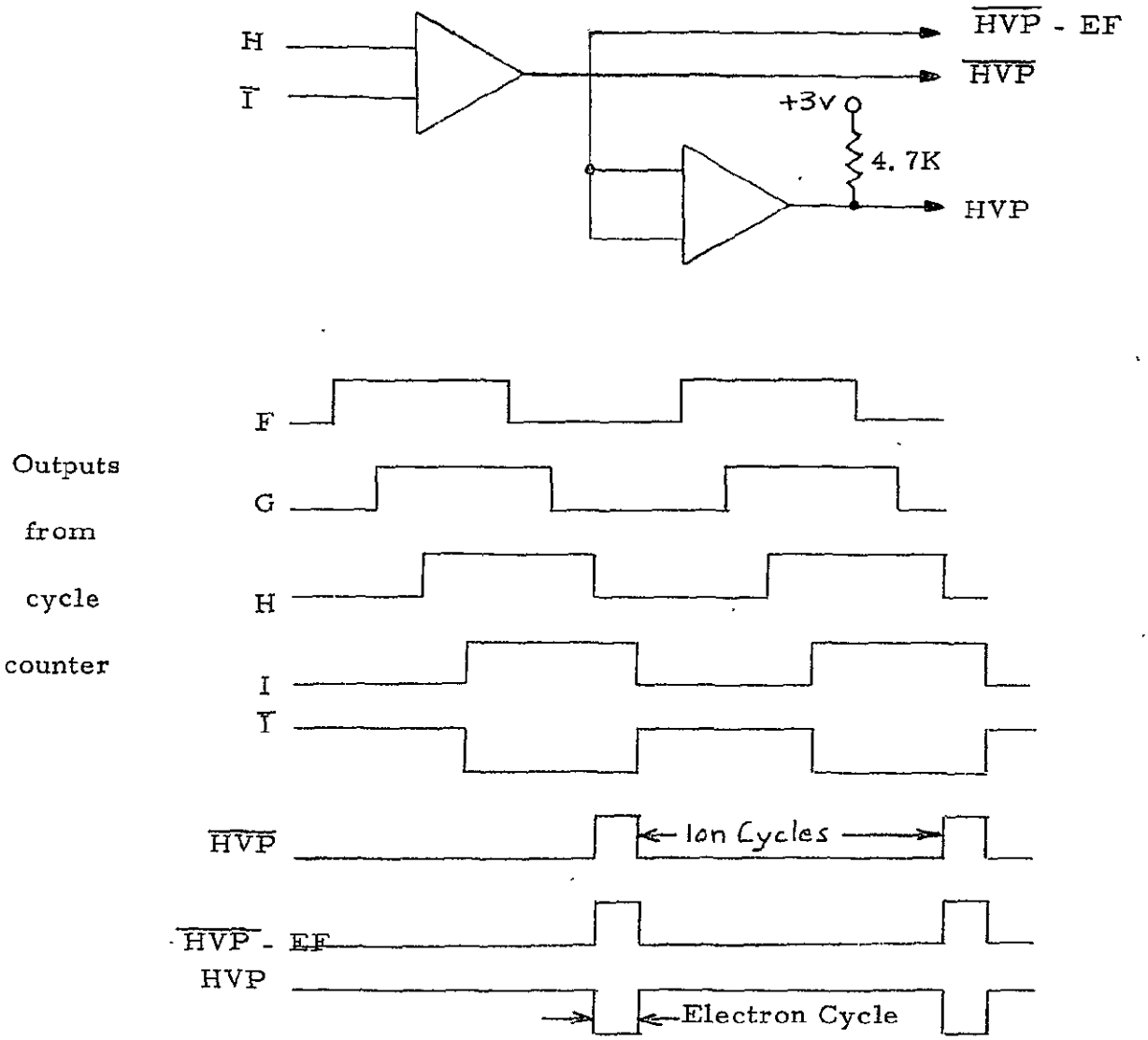
Figure 3.2.5-16 shows the Ion Suppression Logic Diagram. Refer also to Figures 3.2.5-17 and 3.2.5-18 for the Timing diagram for Ion Suppression Code (ISC), $\overline{\text{Mode Command Status Bit 1 (MC1)}}$ and $\overline{\text{Mode Command Status Bit 2 (MC2)}}$. ISC is a function of the states of $\overline{MC1}$ and $\overline{MC2}$. If both are at a "0" level, the Detect (DET) -4th Ion signal is gated through to become ISC. If $\overline{MC1}$ is at a "1" and $\overline{MC2}$ is at a "0", DET-4th Ion is inhibited and $\overline{HVP}$ is gated through to become ISC. When both $\overline{MC1}$ and $\overline{MC2}$ are at a "1", ISC remains down.

Gates 1 and 2 are Inverters cross-connected to form an R-S flip-flop. The buffered SMCC signal sets this flip-flop and the next Start of Electron Cycle (S of EC) pulse resets it. This reset toggles Flip-Flop 1.

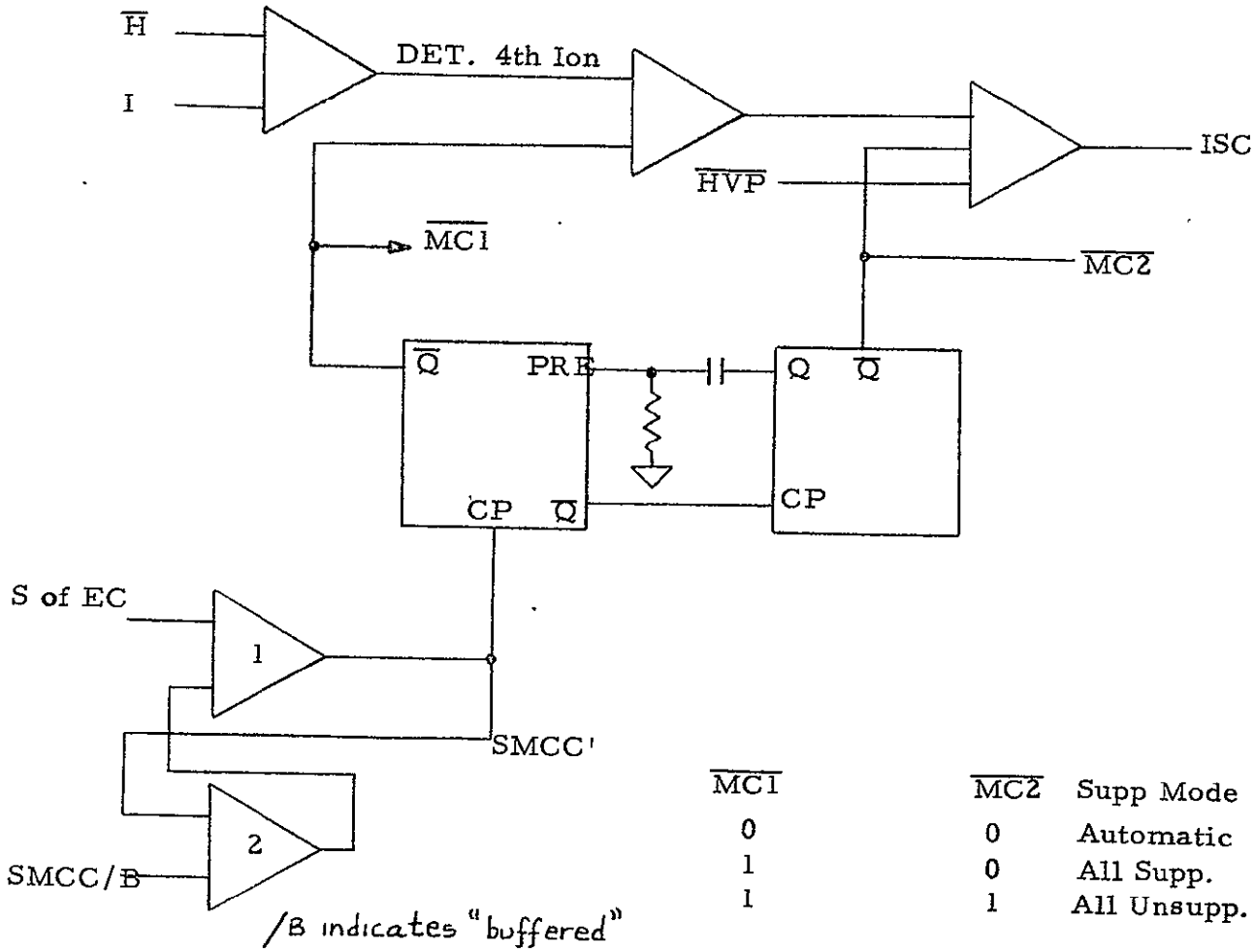
The two stage counter cannot assume the state $\overline{MC}$ = 0, 1. The fall of Q2 presets Flip-Flop 1 so that the counter immediately sets to 1, 1.

3.2.5.14 Electron Suppression Logic

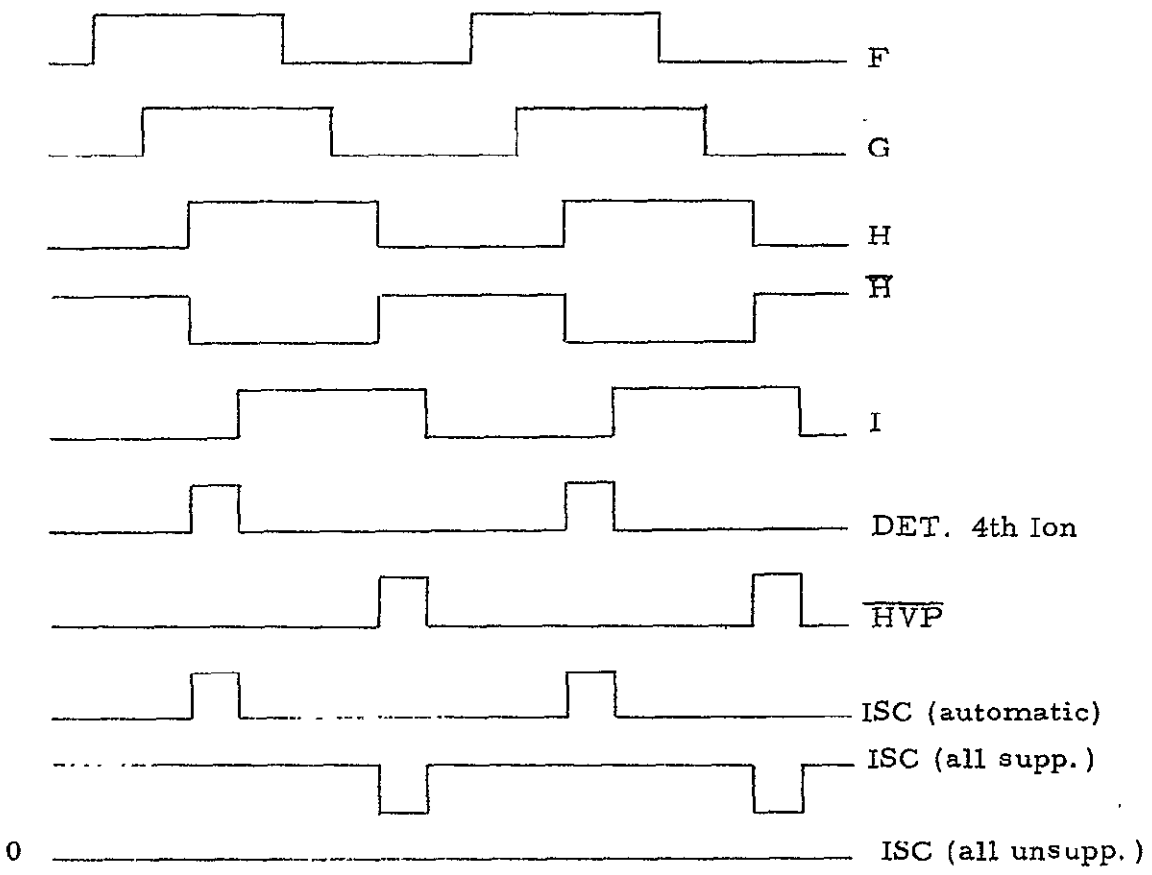
See Figure 3.2.5-19 for the Electron Suppression Logic diagram. Figures 3.2.5-20 and 3.2.5-21 show the associated timing diagrams (LBR and HBR Operation of ESC, and Electron Suppression Logic, respectively).



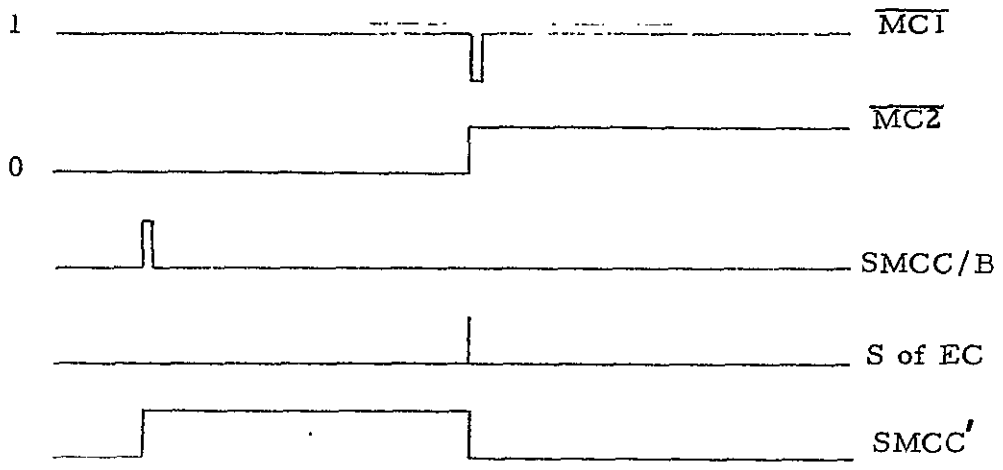
Polarity Logic and Timing Waveforms
Figure 3.2.5-15



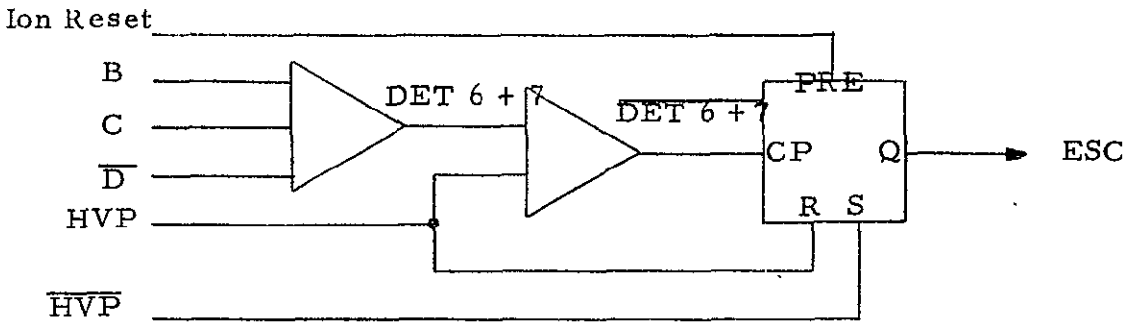
Ion Suppression Logic Diagram
Figure 3.2.5-16



ISC Timing Waveforms
Figure 3.2.5-17

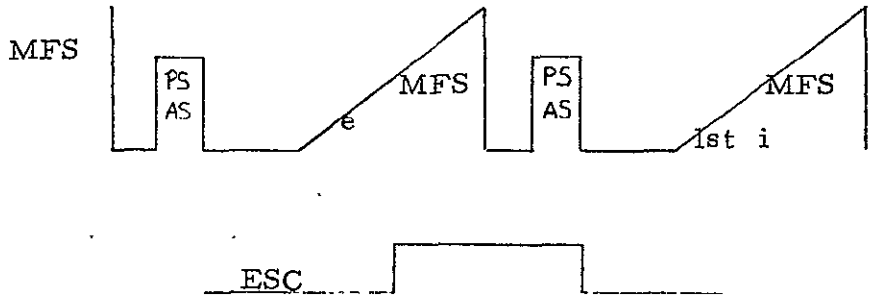


$\overline{MC1}$ and $\overline{MC2}$ Timing Waveforms
Figure 3.2.5-18

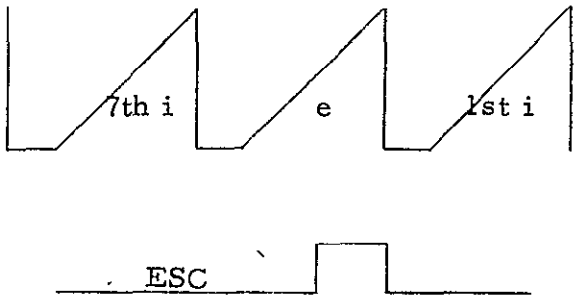


Electron Suppression Logic Diagram
Figure 3.2.5-19

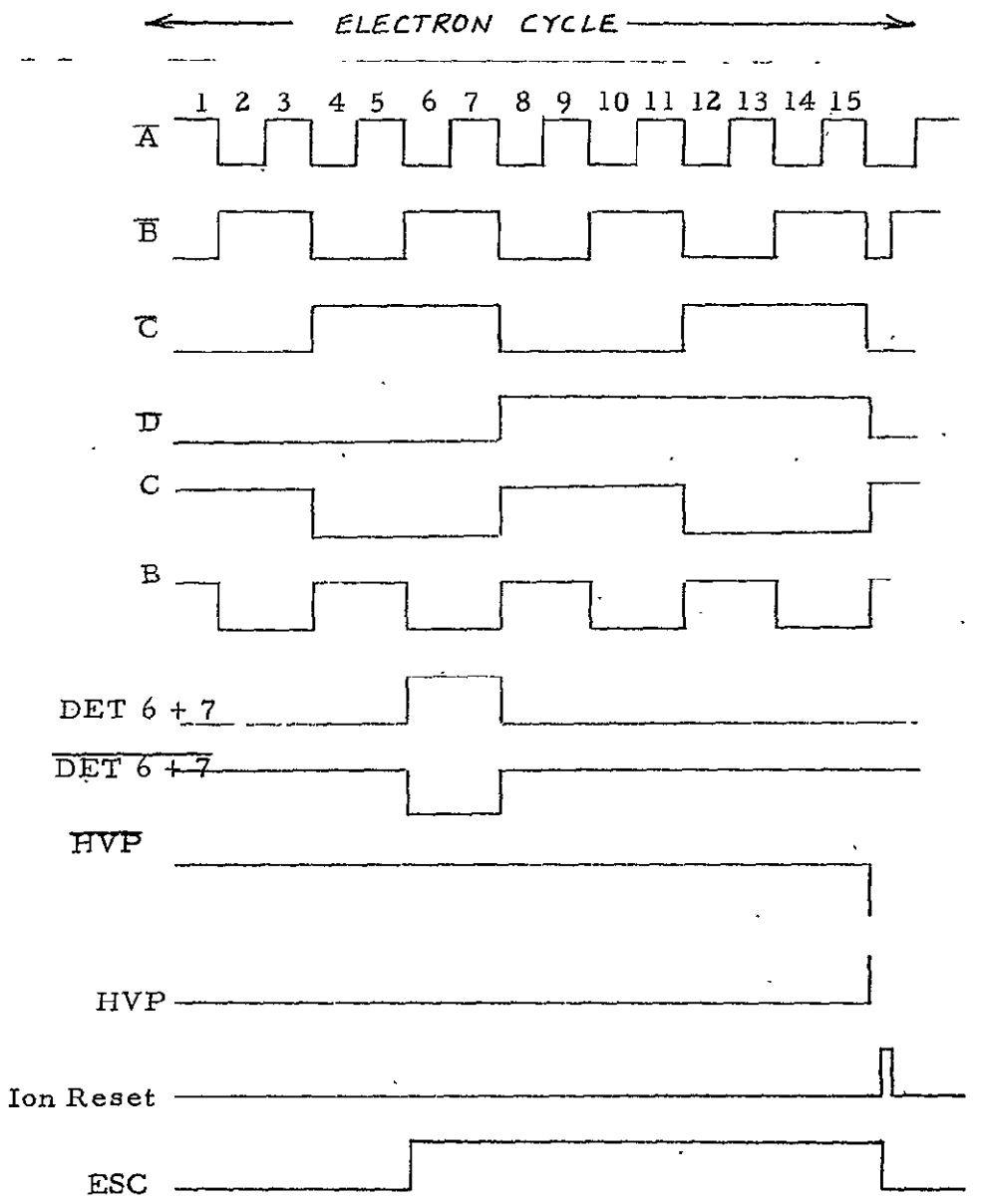
LBR Operation of ESC



HBR Operation of ESC



LBR and HBR Operation of ESC, Timing Diagram
Figure 3.2.5-20



Electron Suppression Logic, Timing Waveform
Figure 3.2.5-21

At the end of the 7th Ion cycle, Ion Reset presets the flip-flop so that Electron Suppression Code (ESC) is low. At the start of the Electron cycle $\overline{HVP}$ goes high and HVP goes low.

At the beginning of the 6th Electron step, (detected by the states of $BC\overline{D}$ of the Step Counter), $\overline{DET\ 6+7}$ goes to zero, setting the flip-flop making ESC positive for the remainder of the cycle. At the end of the cycle, Ion Reset again presets the flip-flop, setting ESC to a low level.

3.2.5.15 Suppressed Identification Logic

Figure 3.2.5-22 shows the Suppressed Identification Logic and Timing diagrams.

When neither Ion Cycle or Electron Cycle is unsuppressed, $\overline{\text{Suppressed Identification}}$ $(\overline{SID})$ is at a "1". When either is unsuppressed, $\overline{SID}$ is at a "0".

$\overline{SID}$ is a status bit indicating suppression condition.

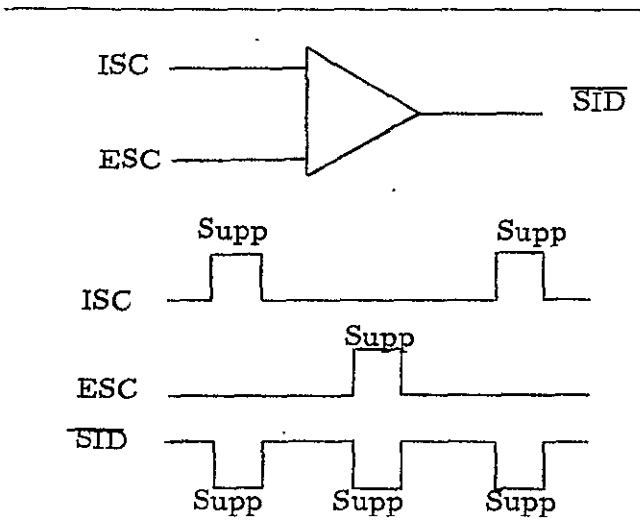
3.2.5.16 Initiate Suppressed Mode Ligic

See Figure 3.2.5-23, Initiate Suppressed Mode (ISM) Logic and Timing diagrams.

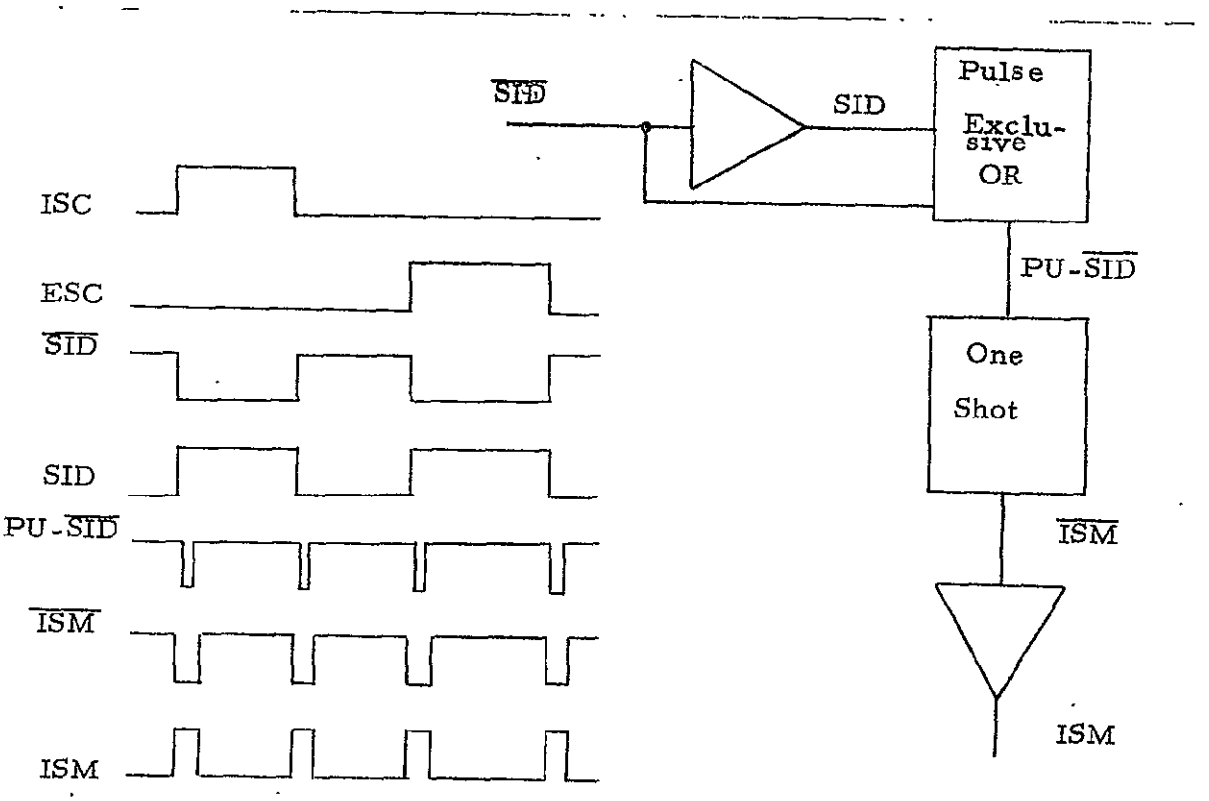
$\overline{SID}$ is inverted to SID; both signals are then combined in an "Exclusive OR" gate to produce PU-SID which occurs at each transition of SID. PU-$\overline{SID}$ triggers the one-shot whose output is an $\overline{ISM}$ pulse which is then inverted to ISM.

3.2.5.17 Suppressed Voltage Logic

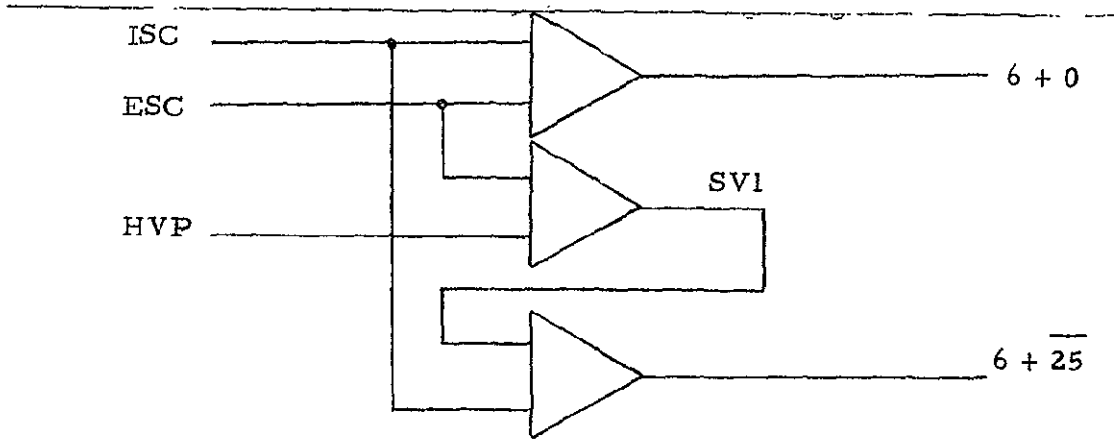
Figure 3.2.5-24 shows the Suppressed Voltage Logic diagram. Figure 3.2.5-25 shows the Truth Table and Timing diagram. ISC and ESC are gated with HVP to produce 6+0 and 6+25, which control the Suppression Voltage Generator in accordance with the truth table in Figure 3.2.5.-25.



Suppressed Identification Logic Diagram and Timing Waveforms
Figure 3.2.5-22

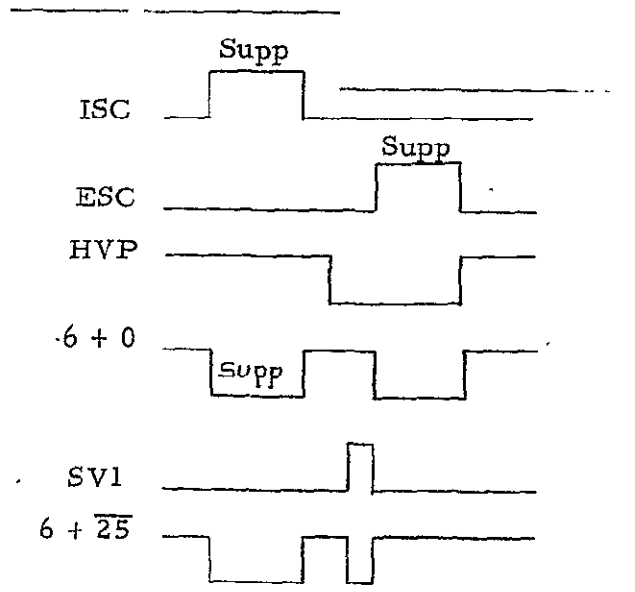


Initiate Suppressed Mode Logic Diagram and Timing Waveforms
Figure 3.2.5-23



Suppressed Voltage Logic Diagram
Figure 3.2.5- 24

6 + 0	6 + $\overline{25}$	Supp. Voltage	Supp. Status
0	0	-40	Supp. Ion
1	0	0	Unsupp. Elect.
0	1	-25	Supp. Elect.
1	1	+6	Unsupp. Ion



Suppressed Voltage Logic Truth Table and Timing Waveforms
Figure 3.2.5-25

3.2.6 High Voltage Zero and Stabilization Control

Refer to Figure 3.2.6-1 for the High Voltage Zero (HVZ) and Stabilization Control Logic diagram, and to Figures 3.2.6-2 and 3.2.6-3 for the Timing diagrams for HVZ and Stabilization. Figure 3.2.6-2 depicts the diagrams for the case of suppression change at HBR, and Figure 3.2.6-3 depicts the diagrams in the case of no suppression change at HBR.

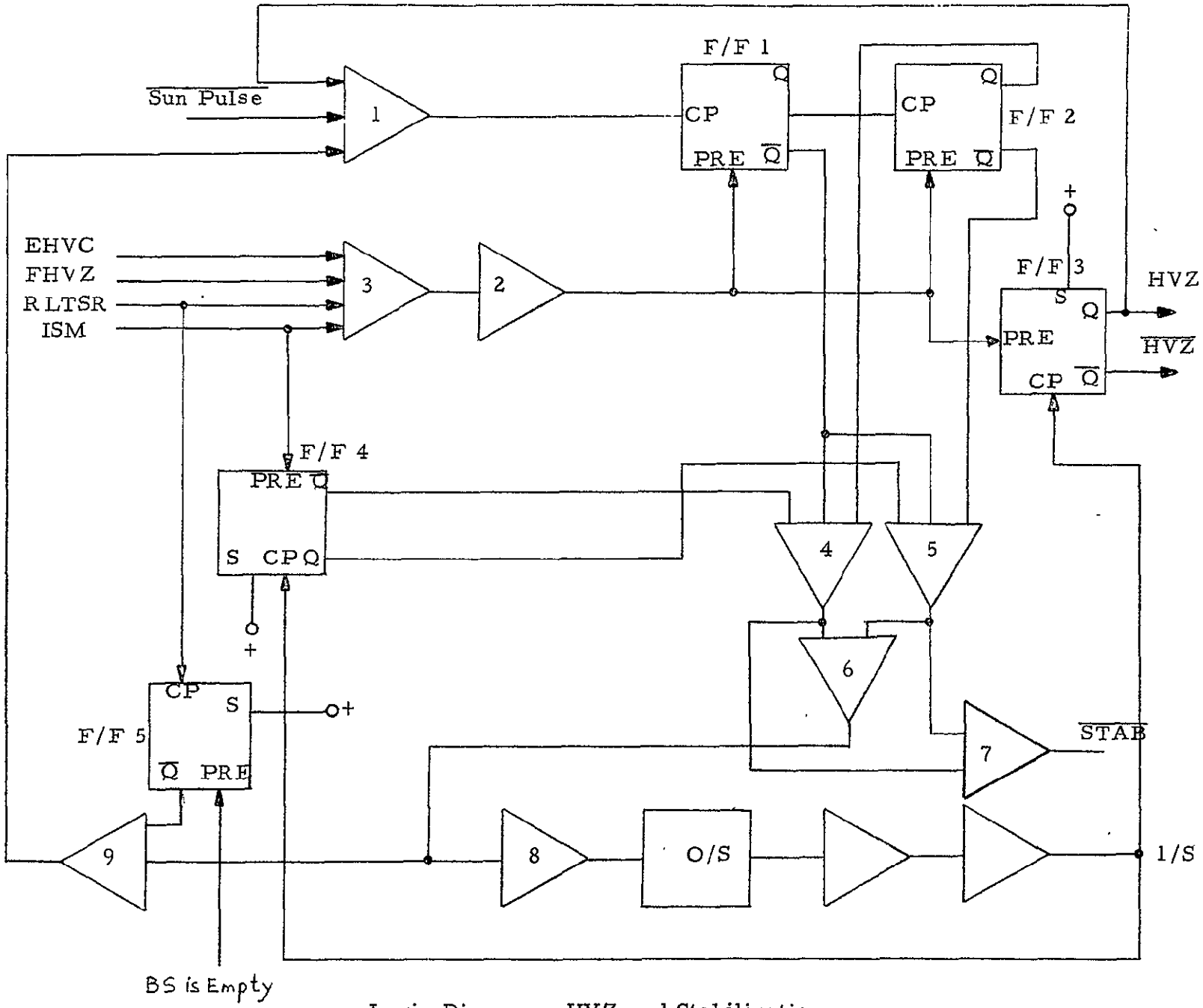
Before the end of a HV cycle, Flip-Flops 1, 2, 3, 4 and 5 are in a set condition. This puts HVZ and $\overline{\text{Stab}}$ at a "1". Sun Pulse is inhibited at Gate 1 by HVZ. When Suppression Status is changed at the end of a cycle in HBR, EHVC resets Flip-Flops 1, 2, and 3, and ISM (Ion Suppression Mode) resets Flip-Flop 4. HVZ goes down, enabling Gate 1. $\overline{Q4}$ inhibits Gate 4.

The first three Sun Pulses set Flip-Flops 1 and 2. $\overline{Q1}$ and $\overline{Q2}$; through Gates 5 and 7, cause $\overline{\text{Stab}}$ to go down, initiating Stabilization. The fourth Sun Pulse resets Flip-Flops 1 and 2, terminating Stabilization.

The resetting of these two flip-flops triggers the one-shot whose output, 1/S, sets Flip-Flop 3, restoring HVZ and inhibiting Sun Pulse at Gate 1. 1/S also sets Flip-Flop 4.

At Low Bit Rate, RLTSR also appears at the end of a cycle. This sets $\overline{Q5}$ low. At the third Sun Pulse, when stabilization starts, the output of Gate 6 goes down and that of Gate 9 goes up, inhibiting Sun Pulse. HVZ and $\overline{\text{Stab}}$ remain down until a BS is Empty signal is received from the Buffer Storage. This resets Flip-Flop 5 and enables Gate 1. The next Sun Pulse resets Flip-Flops 1 and 2 and the sequence proceeds as before.

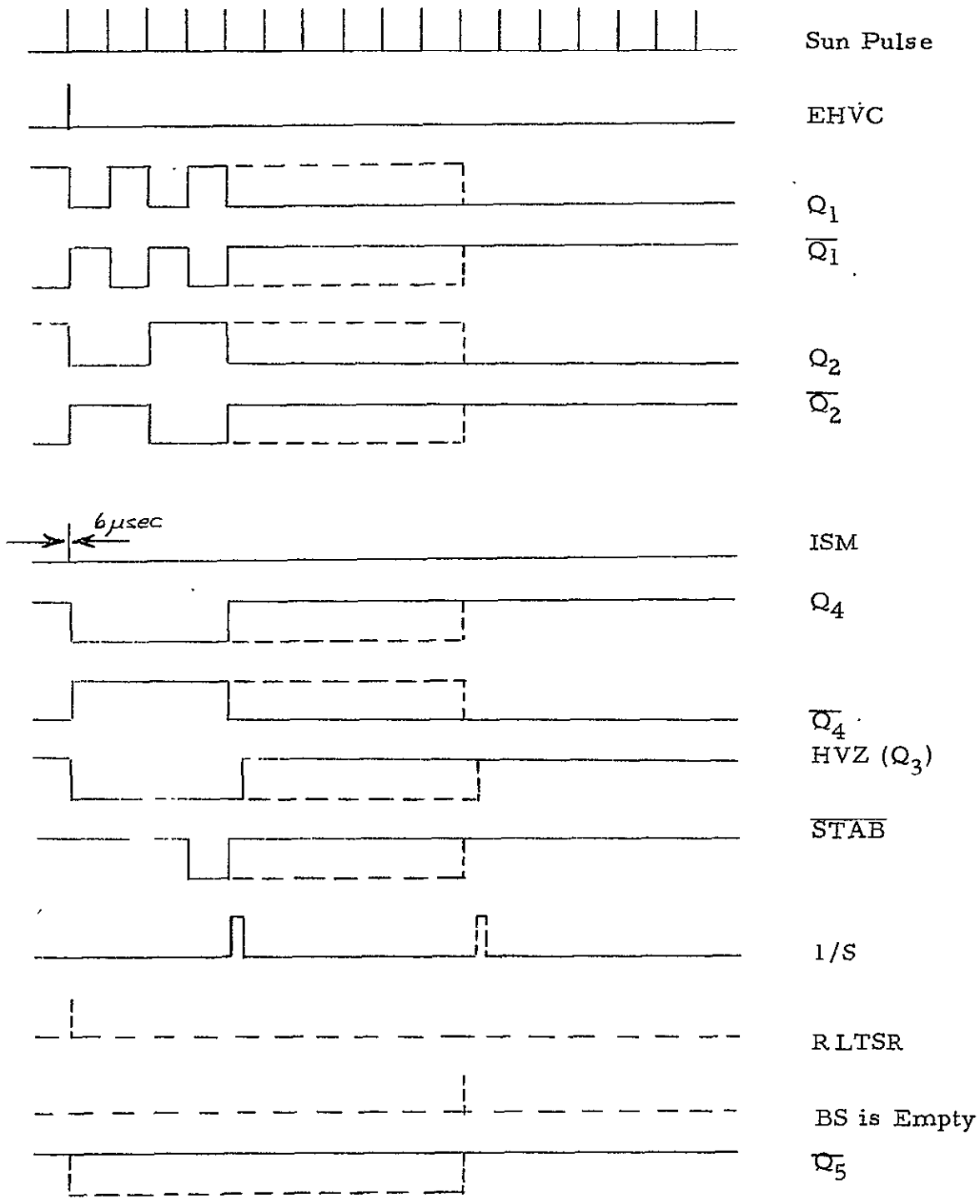
When there is no suppression change at the end of a cycle, Flip-Flop 4 remains set, inhibiting Gate 5 and enabling Gate 4. EHVC resets Flip-Flops 1, 2, and 3. HVZ goes down, enabling Gate 1.



Logic Diagram, HVZ and Stabilization

Figure 3.2.6-1

Dotted lines show operation at EHVC at LBR.

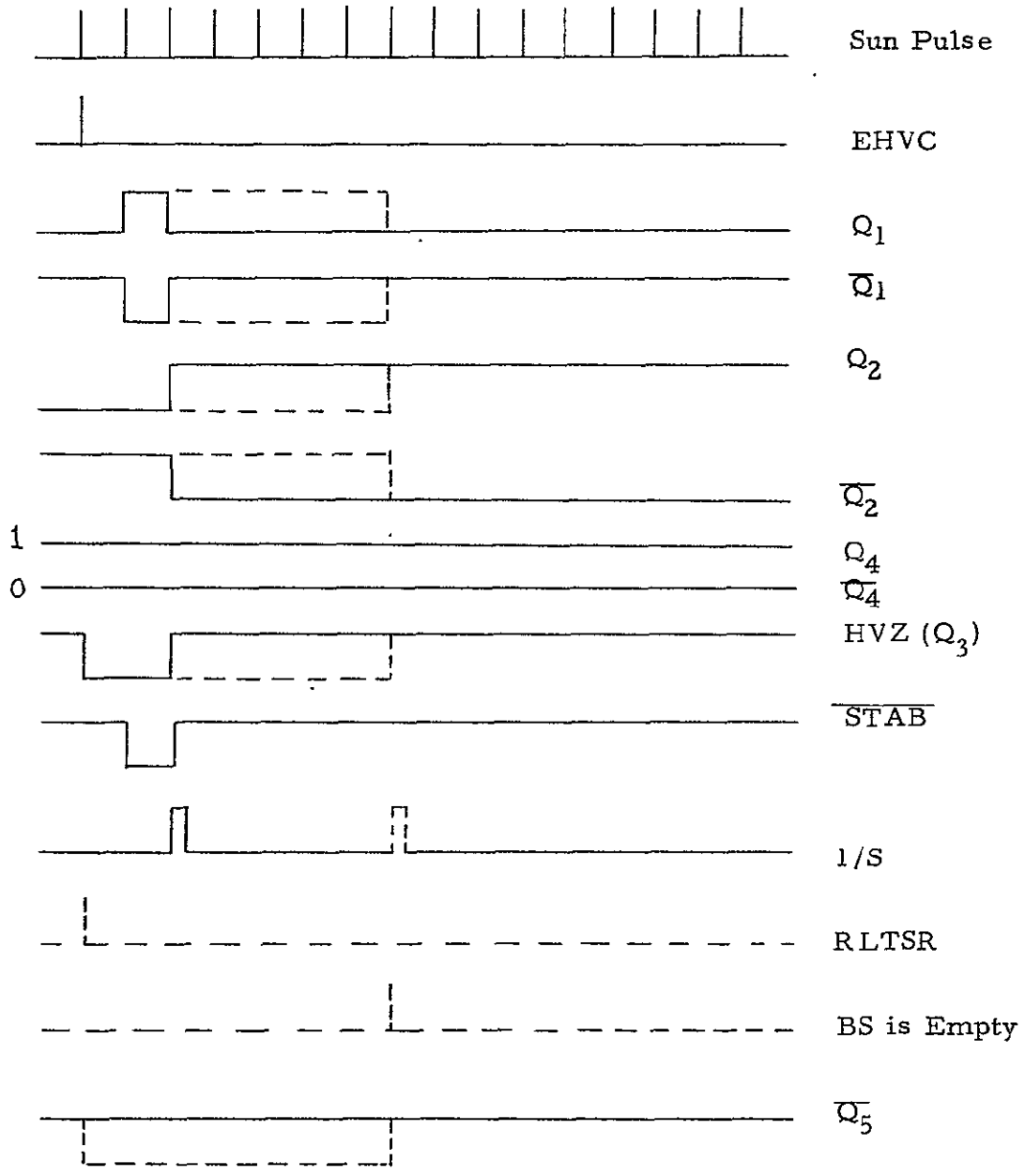


Timing Diagram
HVZ and Stabilization

(Suppression change at HBR)

Figure 3.2.6-2

Dotted lines show operation at EHVC at LBR



Timing Diagram
HVZ and Stabilization
(No Suppression change at HBR)

Figure 3.2.6-3

The next Sun Pulse sets Flip-Flop 1. $\overline{Q1}$ and Q2, through Gates 4 and 7, initiate stabilization. The second Sun Pulse resets Flip-Flop 1 and Flip-flop 2, terminating stabilization; it also triggers the one-shot which sets Flip-Flop 3, restoring HVZ and inhibiting Gate 1.

At Low Bit Rates, RLTSR sets Flip-Flop 5 as before and the Sun Pulse is inhibited until receipt of the BS is Empty signal.

3.2.7 High Voltage A/D

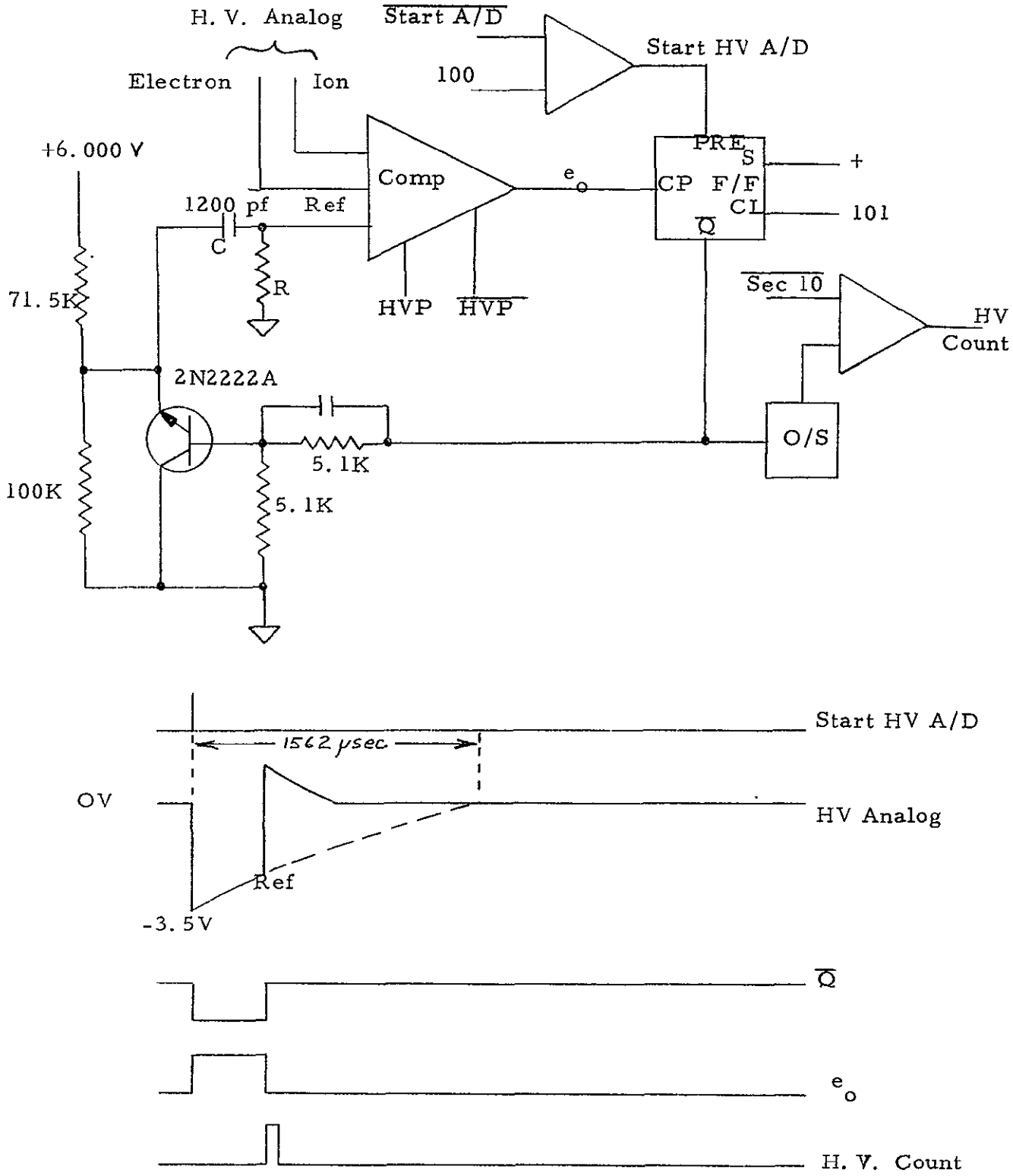
The High Voltage A/D Block diagram and Timing is shown in Figure 3.2.7-1.

The Comparator circuit is a High Gain differential input amplifier, operated open loop. A very small difference between the analog input voltage and the Reference input will cause the output to switch rapidly. The Reference Voltage is connected to one Gate of each pair. The Ion Analog Voltage is connected to the other Gate of one pair, and the Electron Analog Voltage to the other Gate of the second pair. The states of HVP and $\overline{HVP}$ determine which pair is enabled and which analog voltage to be digitized.

The Ion Analog will vary in logarithmic steps between -42mv and -3000mv. The Electron Analog will vary similarly between 0 and -3000mv.

Between samplings, $\overline{Q}$ is low and the 2N2222A is turned OFF. The Reference input to the Comparator is at 0V and C is charged to +3.5v. The selected Analog input is at some negative potential and e_o is 0V.

At the Start HV A/D the flip-flop is preset and $\overline{Q}$ goes up, turning on the transistor. This grounds C. The Reference voltage goes to -3.5v and begins an exponential discharge toward 0V. The Comparator output, e_o, goes to +3.0V. When the Reference crosses the level of the Analog input, e_o rapidly switches to 0V, turning off the transistor and triggering the one-shot. The one-shot output pulse is gated with $\overline{Sec\ 10}$ to produce the HV Count pulse.



High Voltage A/D Block Diagram and Timing Waveforms
Figure 3.2.7-1

The time spacing between Start HV A/D and HV Count is a measure of the Analog input level. The longer the spacing, the lower is the input level.

The 101 input to the Clear terminal of the flip-flop assures the setting of the flip-flop so as to turn off the transistor for recharging of C.

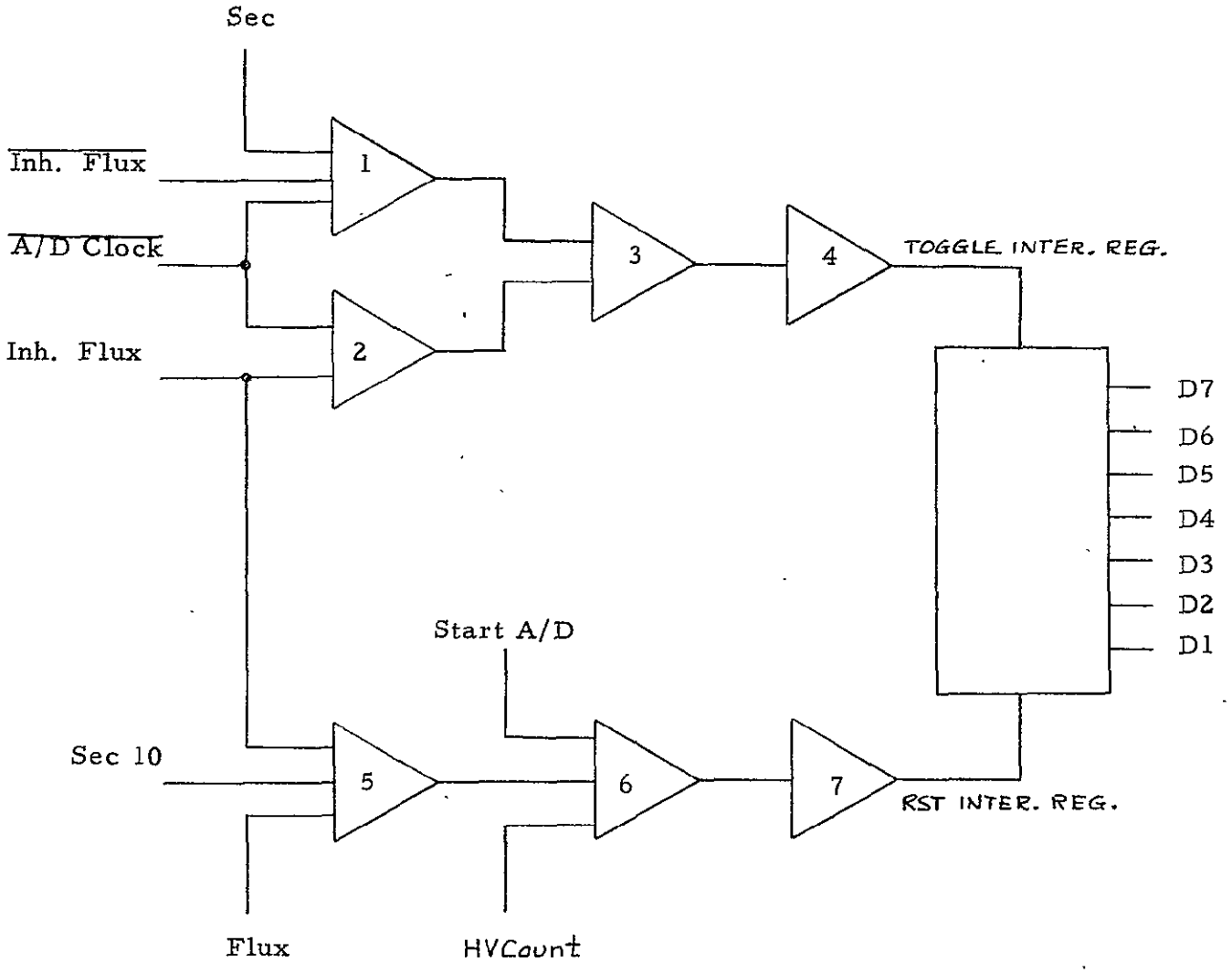
3.2.8 Commutator and Intermediate Storage Register

Refer to Figures 3.2.8-1 and 3.2.8-2, Logic diagrams of Commutator and Intermediate Storage Register.

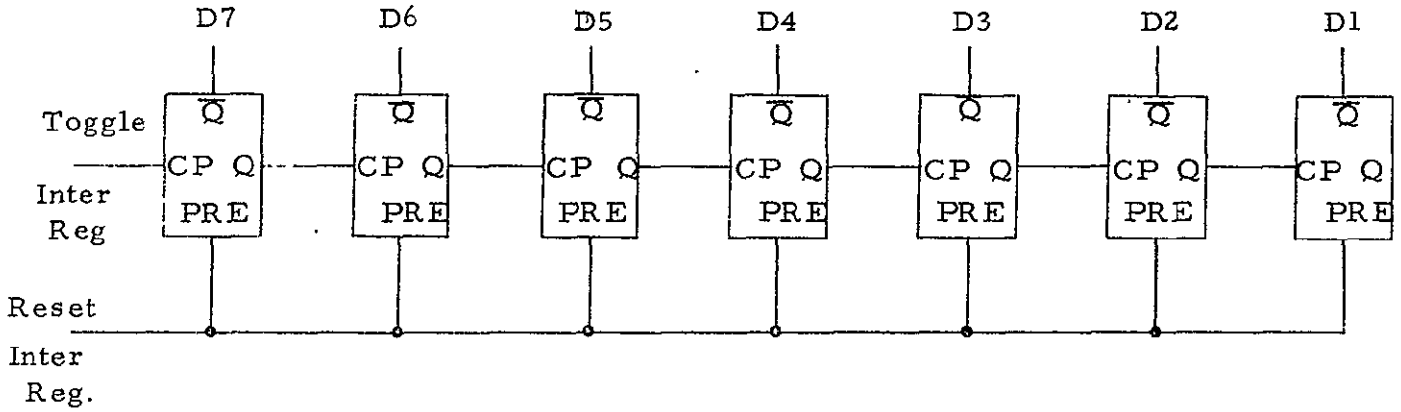
The start A/D pulse resets the Intermediate Register at the start of each A/D Clock burst. Sector information is read out during sectors 3, 5, and 7. At these times, Inhibit Flux is down and the clock toggles the register. When the Sec signal rises, the clock burst is inhibited. The number of pulses which entered and were stored in the register is equal to the sector number which was stored in 0 sector register. The D1 through D7 voltages are then transferred to the Buffer Storage.

Flux is read out during sectors 2, 4, and 6. When Inhibit Flux is down, the clock pulse, through gates 2, 3, and 4, toggles the register. When the Flux pulse occurs, the register is reset to zero, and the remaining pulses of the clock burst are entered into the register. This number represents the flux measurement as stored in a flux register. D1 through D7 is again transferred to the Buffer Storage.

High voltage is read out during sector 10. When sector 10 goes up, the output of gate 5 is held down. Start A/D resets the register and the clock starts toggling the register. The HV count pulse resets the register to zero, then the remainder of the clock burst enters the register. At the end of the sequence the count in the register represents the HV level at which maximum flux was detected during a Polar Scan. D1 through D7 is then transferred to the buffer storage.



Commutator and Intermediate Storage Register
Logic Diagram
Figure 3.2.8-1



Intermediate Storage Register
Figure 3.2.8-2

The Intermediate Storage Register is a seven stage ripple counter. The outputs are the Q's of each stage; D1 is the most significant bit.

3.2.9 Write Pulse Generator

For the description of this section, refer to the following figures:

a. 3.2.9-1 AS and PS Write Pulse (WP) Logic diagram
b. 3.2.9-2 MFS Write Pulse and Write Pulse Gate Logic diagram
c. 3.2.9-3 Write Pulse Timing Diagram
d. 3.2.9-4 Inhibit HVA and Write Pulse at High Bit Rate, Logic and Timing diagram

The functional description is as follows:

AS Write Pulses

During AS mode of operation, the requirement is to generate a Write Pulse at 102 time of each of the 23 selected sectors. In addition, a Write Pulse is required at 101 time of sectors 66, 72, and 78.

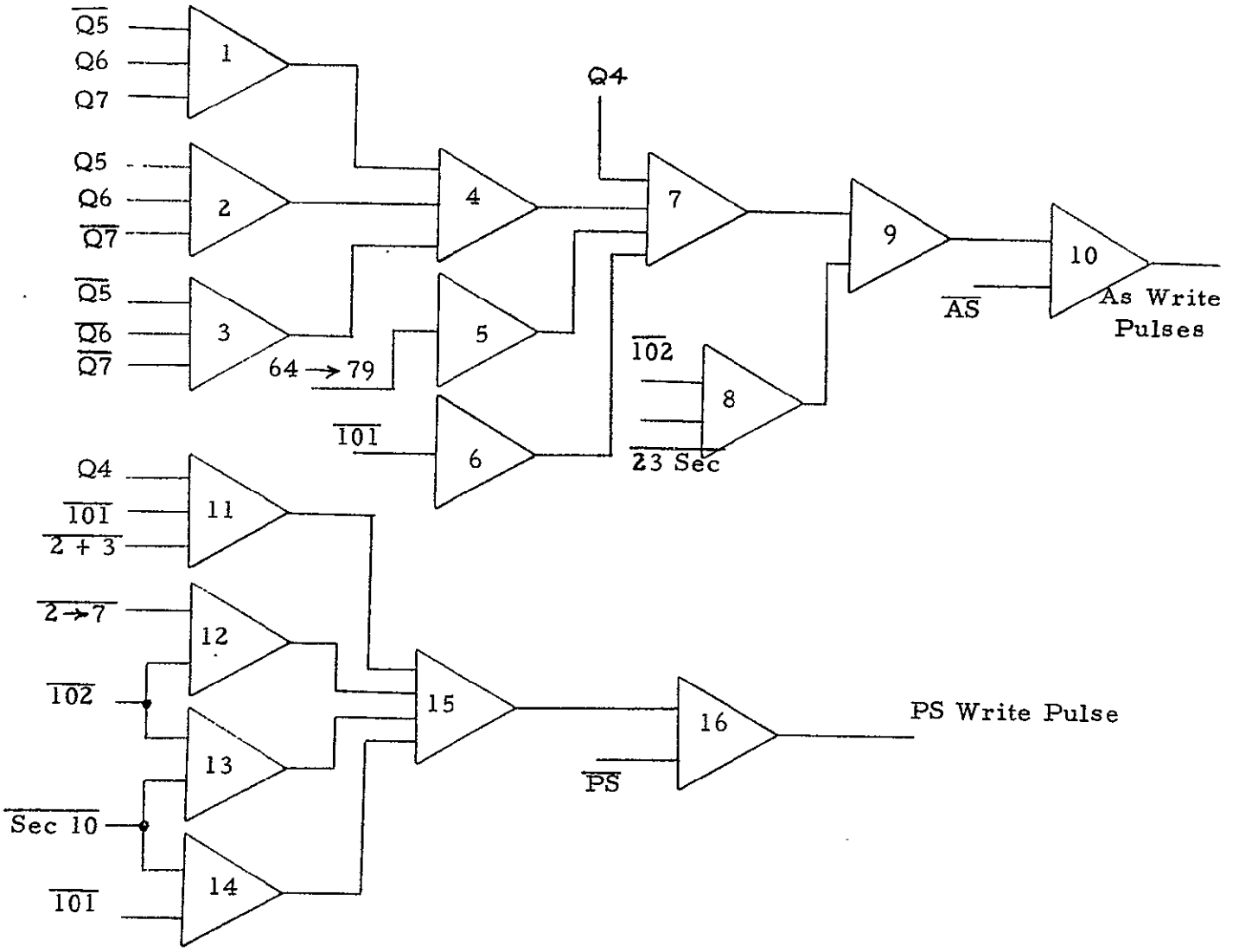
The 102 pulses are gated with the 23 sector signals at Gate 8 to fulfill the first requirement. The second requirement is satisfied in the manner described below.

Refer to Table 3.2.1A (Register Count and Sector), in Section 3.2.1.5 (Sector Detectors). The inputs to Gates 1, 2, 3 and 7 are from the Spoke Generator.

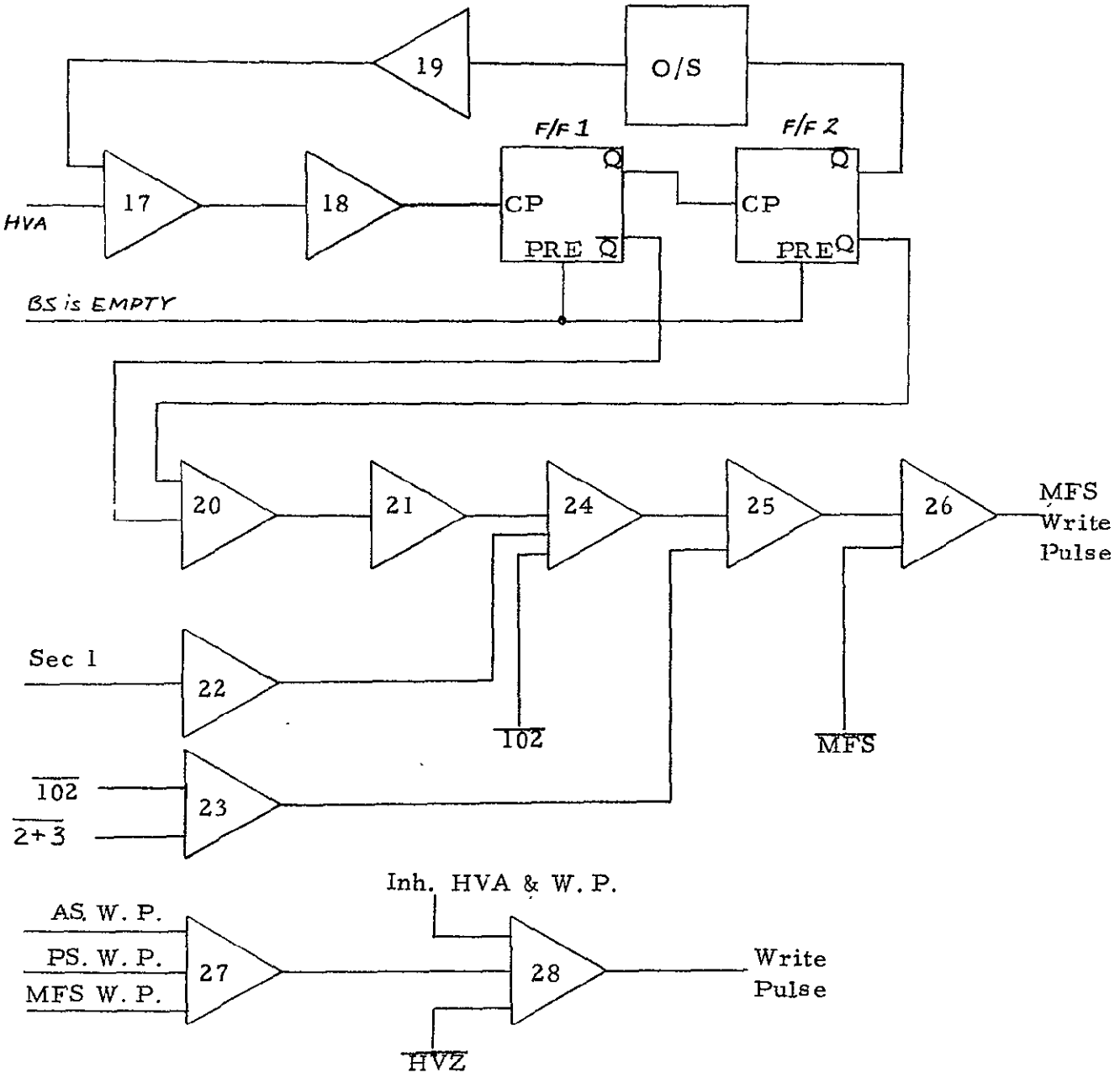
At Gate 1:

$$\overline{\overline{Q5} + Q6 + Q7} = Q5 \cdot \overline{Q6} \cdot \overline{Q7}$$

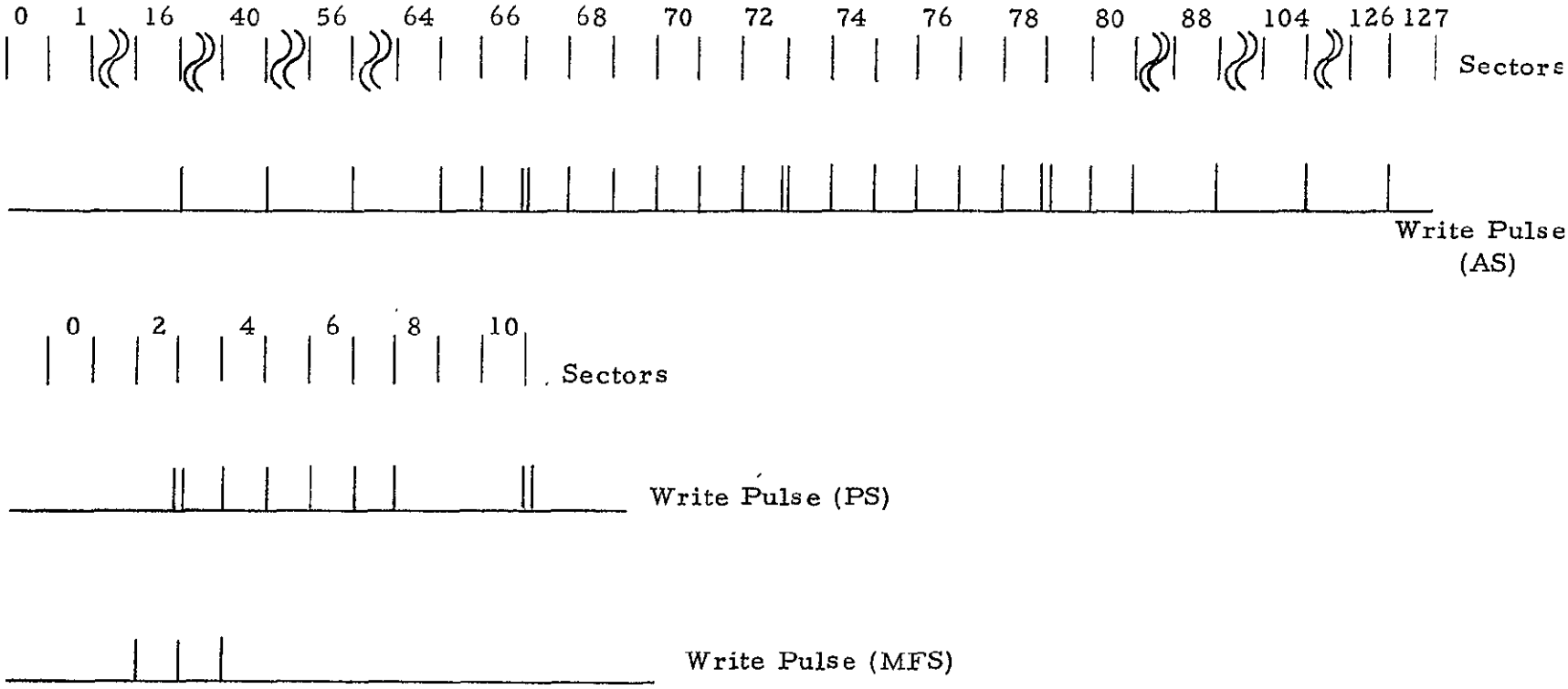
$$= \text{Sectors } [2 + 3 + 18 + 19 + 34 + 35 + 50 + 51 + 66 + 67 + 82 + 83 + 98 + 99 + 114 + 115] = A$$



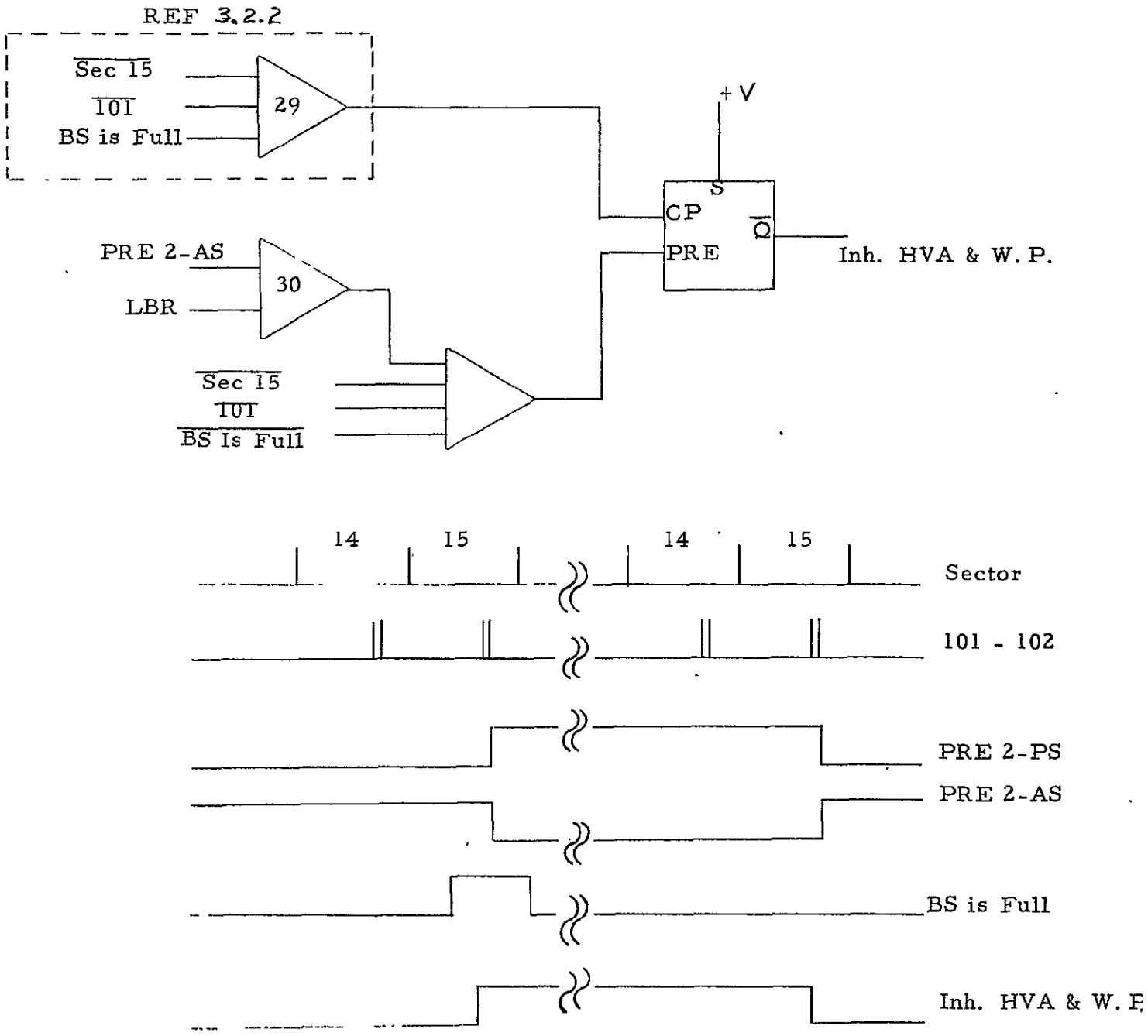
AS & PS Write Pulse Logic Diagram
Figure 3.2.9-1



MFS Write Pulse & Write Pulse Gate Logic Diagram
Figure 3.2.9-2



Write Pulse Timing Diagram
Figure 3.2.9-3



Inhibit HVA & Write Pulse at
High Bit Rate, Logic and Timing Diagram
Figure 3.2.9-4

At Gate 2:

$$\overline{Q5 + Q6 + \overline{Q7}} = \overline{Q5} \cdot \overline{Q6} \cdot Q7$$

$$= \text{Sectors}\,[8 + 9 + 24 + 25 + 40 + 41 + 56 + 57 + 72 + 73 + 88 + 89 + 104 + 105 + 120 + 121] = B$$

At Gate 3:

$$\overline{\overline{Q5} + \overline{Q6} + \overline{Q7}} = Q5 \cdot Q6 \cdot Q7$$

$$= \text{Sections}\,[14 + 15 + 30 + 31 + 46 + 47 + 62 + 63 + 78 + 79 + 94 + 95 + 110 + 111 + 126 + 127] = C$$

At Gate 4:

Q4 is true only for odd numbered sectors,

$$\therefore\ \overline{(\overline{A} \cdot \overline{B} \cdot \overline{C}) + (\overline{64 \rightarrow 79}) + \overline{(Odd)} + \overline{(101)}} =$$

$$= \overline{(\overline{A} \cdot \overline{B} \cdot \overline{C})}\ \overline{(\overline{64 \rightarrow 79})}\ \overline{(Odd)}\ \overline{(101)}$$

$$= (A + B + C)\ (64 \rightarrow 79)\ \overline{(Odd)}\ (101)$$

$$= [A(64 \rightarrow 79) + B(64 \rightarrow 79) + C(64 \rightarrow 79)]\ [Even]\ [101]$$

$$= (66 + 72 + 78)\ (101)$$

This expression, plus the output of Gate 8, through Gates 9 and 10, yield:

$$W.P = AS\ [(23\ \text{sec.})\ (102) + (66 + 72 + 78)\ (101)]$$

PS Write Pulses

During PS mode, the requirement is to generate a Write Pulse at 102 time of Sectors 2, 3, 4, 5, 6, 7, and 10. In addition, a pulse is required at 101 time of sectors 2 and 10.

At Gate 11:

Again Q4 is True for odd numbered pulses,

$$\overline{\text{Odd} + \overline{101} + \overline{(2+3)}} = \overline{(\text{Odd})}\ (101)\ (2+3)$$
$$= (2)\ (101)$$

At Gate 12:

$$\overline{(2 \rightarrow 7) + \overline{102}} = (2 \rightarrow 7)\ (102)$$

At Gate 13:

$$\overline{\text{Sec.}\,10 + \overline{102}} = (10)\ (102)$$

At Gate 14:

$$\overline{\text{Sec.}\,10 + \overline{101}} = (10)\ (101)$$

$\therefore$ Through Gates 15 and 16:

$$W_1 P_1 = PS\ [(2 + 10)\ (101) + (2 \rightarrow 7\ + 10)\ (102)]$$

The BS is Empty signal synchronizes the divide-by-3 counter by presetting Flip-Flop 1 and Flip-Flop 2. The first HVA occurs at the second Sun Pulse after the BS is Empty signal and toggles Flip-Flop 1. The next HVA toggles Flip-Flop 1 again, which in turn toggles Flip-Flop 2. The setting of Flip-Flop 2 triggers the one-shot whose output immediately toggles Flip-Flop 1 again.

The input to Gate 20 and output of Gate 21

$$= \overline{Q1} + Q2$$

At Gate 24:

$$\overline{(\overline{Q1} + Q2) + (\overline{\text{Sec.}\ 1\ + \overline{102}})} = (Q1 \cdot \overline{Q2})\ (\text{Sec. } 1)\ (102)$$

This expression plus the expression (2 + 3) (102) is present at Gate 25. Therefore, at the output of Gate 26,

$$WP = MFS\ [(2 + 3)\ (102) + (Q1 \cdot \overline{Q2})\ (Sec.\ 1)\ (102)]$$

Composite Write Pulse

AS WP, PS WP and MFS WP are OR-gated at Gate 27 and appear at the output of Gate 28. The Write Pulse can be inhibited at Gate 28 by either HVZ or Inhibit HVA and Write Pulse.

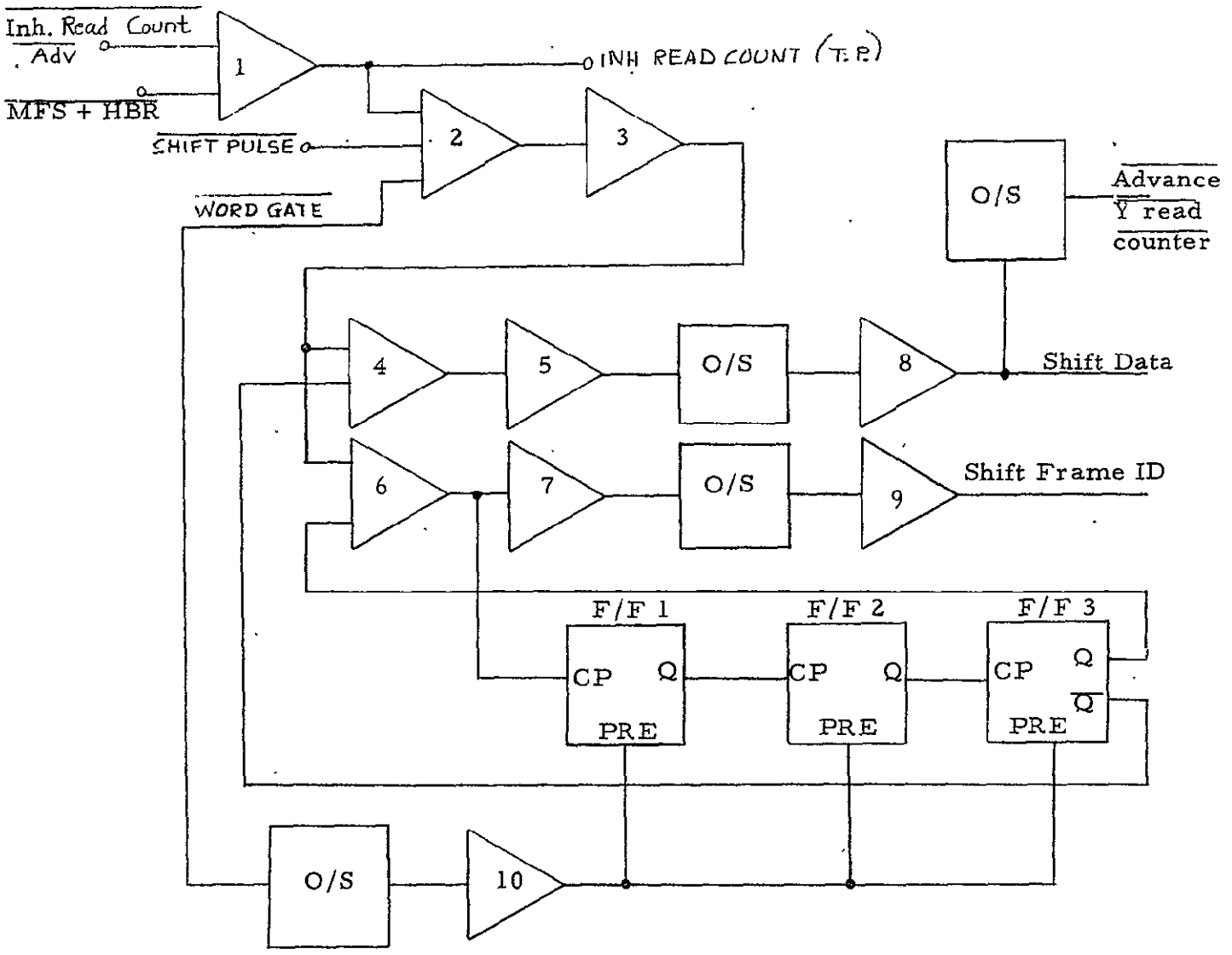
Inhibit HVA and WP

During HBR operation, if the $\overline{\text{BS is Full}}$ signal from the Buffer Storage goes True, and PRE2-AS is False, the 101 signal of Sector 15 presets the flip-flop, generating Inhibit HVA and WP. After $\overline{\text{BS is Full}}$ goes False, the 101 signal of the following sector 15 will set the flip-flop. This causes the Inhibit HVA and WP signal to go False.

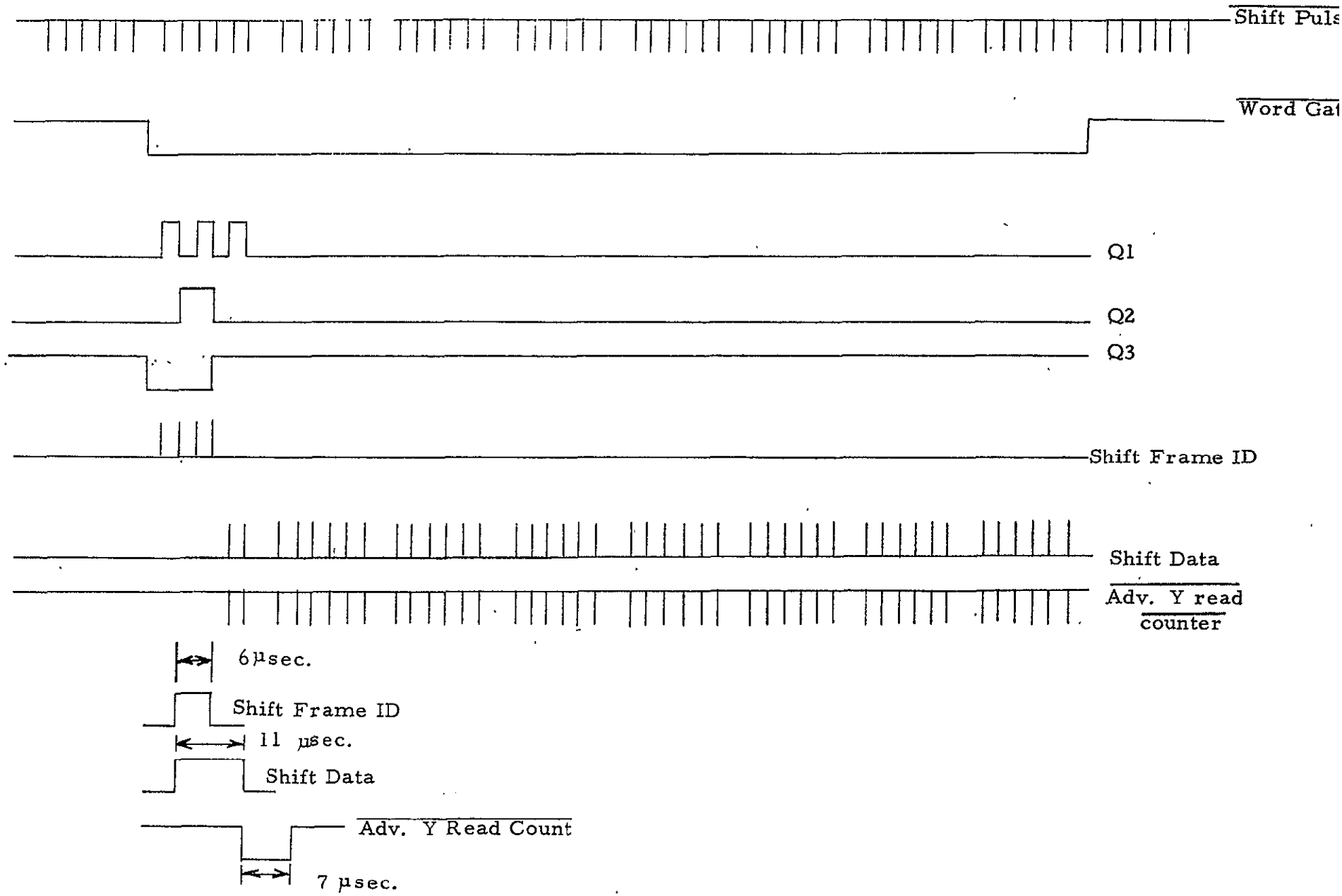
3.2.10 Shift Pulse Generator

Figure 3.2.10-1 shows the Logic diagram for the Shift Pulse Generator. Refer to Figure 3.2.10-2 for the Timing diagram.

The Shift Pulse from the spacecraft is derived from the 16.384 KHz pulse train. The repetition rate of the Shift Pulse determines the Bit Rate at which the Buffer Storage is read out. Dividing the 16.384 KHz by the appropriate factor will determine the bit rate.



Shift Pulse Generator Logic Diagram
Figure 3.2.10-1



Shift Pulse Generator Timing Diagram
Figure 3.2.10-2

Divide By	Bit Rate
32	512
64	256
256	64
1024	16

The resultant Shift Pulse train is composed of groups of six pulses, with separation between groups accomplished by deleting every seventh pulse.

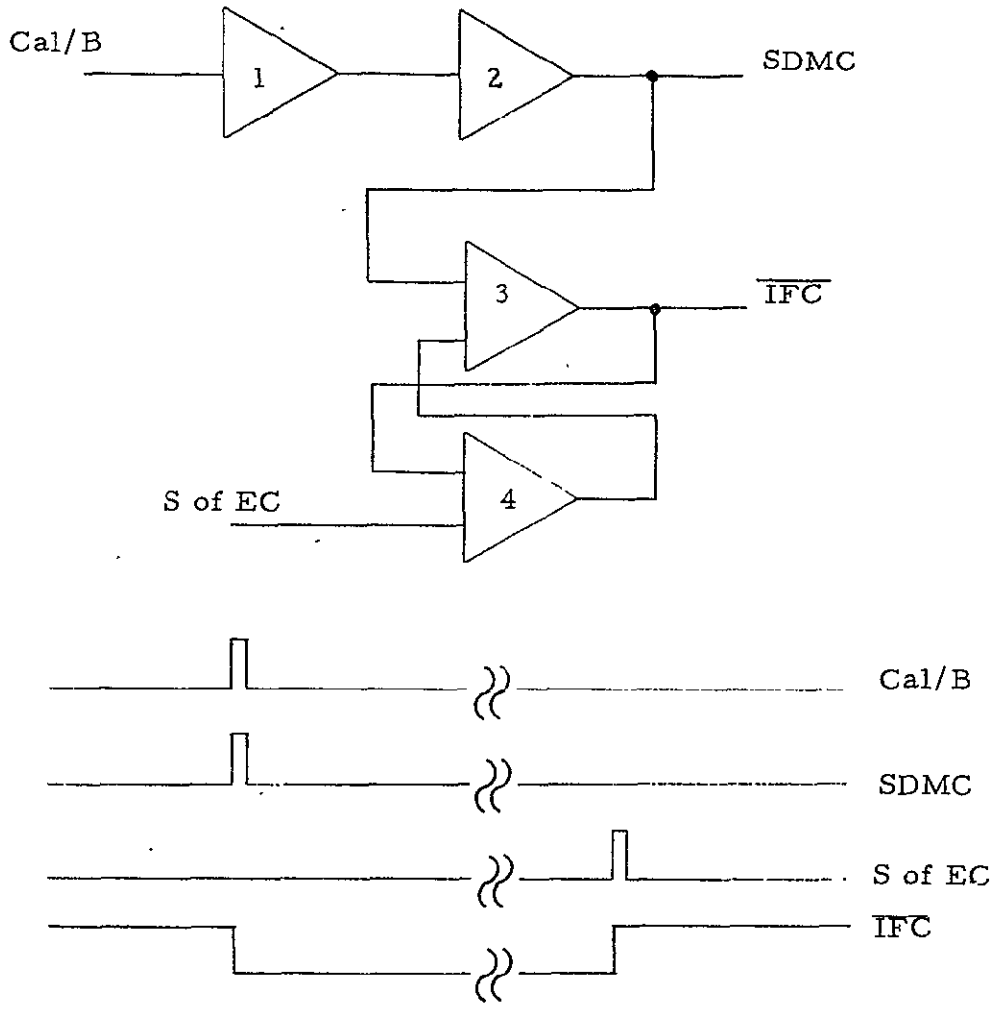
The Word Gate from the spacecraft rises and falls at the time of the missing seventh pulse and is up for eight groups of pulses. It is down for twenty-four groups.

The output of Gate 1 is normally down. When $\overline{WG}$ goes down, the one-shot is triggered which presets the 3 stage counter. $\overline{Q3}$ inhibits Gate 4 while Q3 enables Gate 6. The first 4 shift pulses pass through Gate 6, each triggering the one-shot which generates Shift Frame ID.

The same 4 pulses toggle the counter. At the count of 4, Q3 goes up, inhibiting Gate 6 while Q3 goes down enabling Gate 4. The remaining 44 shift pulses pass through Gates 4 and 5. Each triggers the one-shot to generate the Shift Date pulse train. The fall of each shift data triggers another one-shot which generates the $\overline{\text{Advance Y Read Counter}}$ pulses.

3.2.11 Calibration

See Figure 3.2.11-1 for Logic and Timing diagrams. When the Buffered Calibrate Command appears it is inverted twice to generate SDMC. SDMC acts on the Sun Pulse circuit to introduce or cancel the Sun Pulse delay.



Calibration Logic and Timing Diagram
Figure 3.2.11-1

Gates 3 and 4 are cross-coupled to form an RS flip-flop. Normally, In-Flight Calibrate is high. SDMC drives $\overline{\text{IFC}}$ down which sets the flip-flop. The next start of Electron Cycle pulse resets the flip-flop, driving $\overline{\text{IFC}}$ up.

$\overline{\text{IFC}}$ causes the Flux Pulse Width Modulators to generate a pulse width equivalent to 50% of full scale.

3.2.12 Status Decoder

The Logic diagram for the Status Decoder is shown in Figure 3.2.12-1.

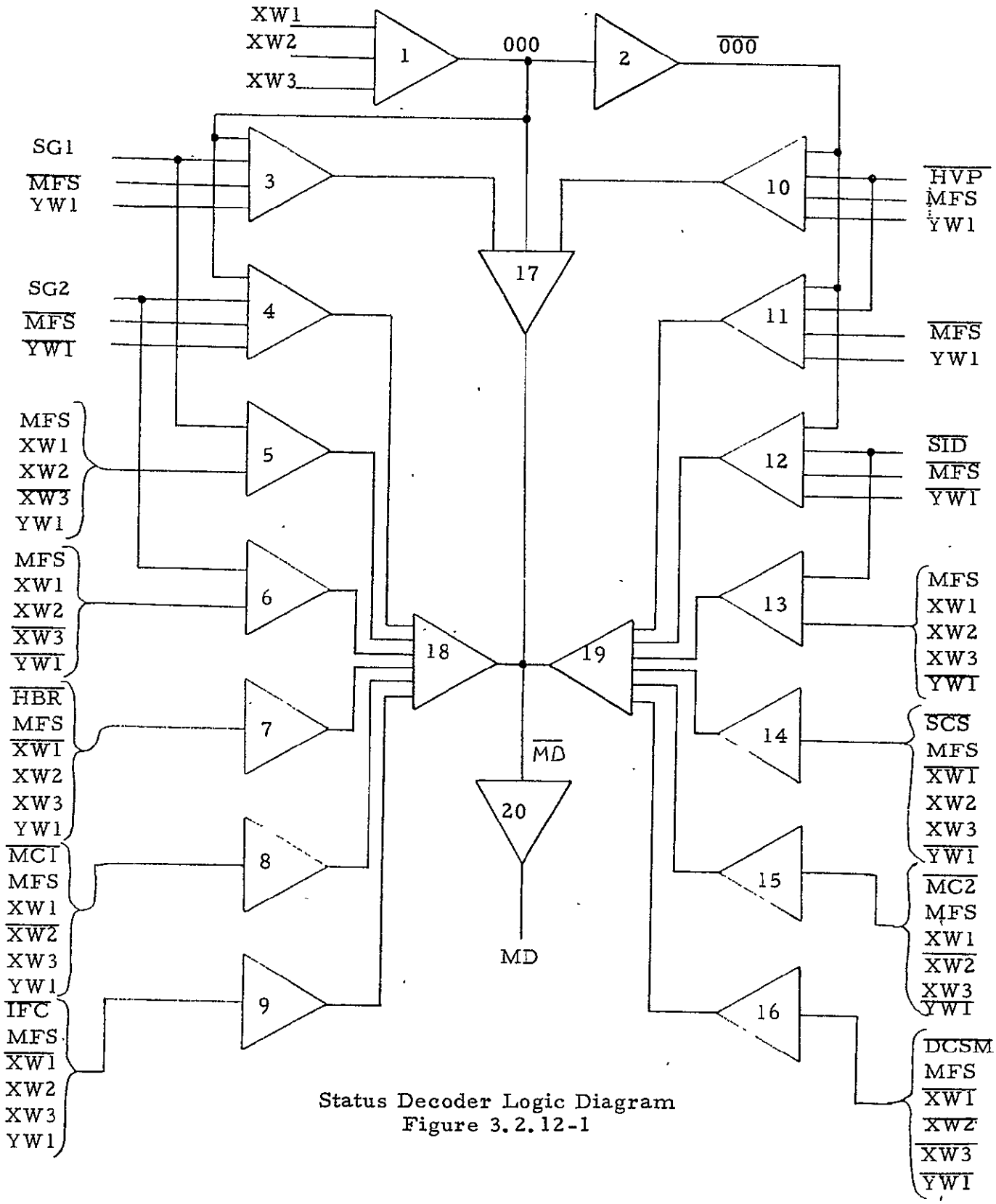
The status decoder gates the various status information to provide the Miscellaneous Data (MD) signal for entry into the Buffer Storage. Refer to Data Format, Fig. 2.0-1, for placement of this information. MD is entered by pairs into Lines 5 and 6 of each of the 15 frames.

Info. (Line 5)	Frame (AS & PS)	Frames (MFS)
HVP	1, 6, 11	1, 6
BR	2, 7, 12	---
MC1	3, 8, 13	---
IFC	4, 9, 14	2→5
SG1	5, 10, 15	7→10, 15
Info. (Line 6)		
SID	1, 6, 11	1, 6
SCS	2, 7, 12	---
MC2	3, 8, 13	---
DCSM	4, 9, 14	---
SG2	5, 10, 15	2→5 7→10, 15

The bit selection for entry into the Buffer Storage is determined by Core Plane Address which is a function of the states of the X and Y Write Counters.

Truth Tables

For Line 5, YW1 is False
For Line 6, YW1 is True



Status Decoder Logic Diagram
Figure 3.2.12-1

Frames	XW1	XW2	XW3
1, 6, 11	0	0	0
2, 7, 12	1	0	0
3, 8, 13	0	1	0
4, 9, 14	1	1	0
5, 10, 15	0	0	1

At Gate 1:

$$\overline{XW1 + XW2 + XW3} = (\overline{Xw1} \cdot \overline{XW2} \cdot \overline{XW3})$$

At Gate 2:

$$\overline{(\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})}$$

At Gate 3:

$$MD = \overline{(\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3}) + \overline{MFS} + YW1 + SG1}$$

$$= (XW1 + XW2 + XW3)(MFS)(\overline{YW1})(\overline{SG1})$$

At Gate 5:

$$MD = \overline{(XW1 + XW2 + \overline{XW3}) + MFS + YW1 + (SG1)}$$

$$= (\overline{XW1} \cdot \overline{XW2} \cdot XW3)(\overline{MFS})(YW1)(\overline{SG1})$$

At Gate 4:

$$MD = \overline{(\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3}) + \overline{MFS} + \overline{YW1} + SG2}$$

$$= (XW1 + XW2 + XW3)(MFS)(YW1)(\overline{SG2})$$

At Gate 6:

$$MD = \overline{(XW1 + XW2 + \overline{XW3}) + MFS + \overline{YW1} + SG2}$$

$$= (\overline{XW1} \cdot \overline{XW2} \cdot XW3)(\overline{MFS})(YW1)(\overline{SG2})$$

At Gate 7:

$$MD = \overline{(\overline{XW1} + XW2 + XW3) + (MFS) + YW1 + \overline{HBR}}$$

$$= (XW1 \cdot \overline{XW2} \cdot \overline{XW3})(\overline{MFS})(\overline{YW1})(HBR)$$

At Gate 8:

$$MD = \overline{(XW1 + \overline{XW2} + XW3) + MFS + YW1 + \overline{MC1}}$$

$$= (\overline{XW1} \cdot XW2 \cdot \overline{XW3})(\overline{MFS})(\overline{YW1})(MC1)$$

At Gate 9:

$$MD = \overline{(\overline{XW1} + \overline{XW2} + XW3) + (MFS) + YW1 + \overline{IFC}}$$

$$= (XW1 \cdot XW2 \cdot \overline{XW3})(\overline{MFS})(\overline{YW1})(IFC)$$

At Gate 10:

$$MD = \overline{(\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3}) + MFS + YW1 + \overline{HVP}}$$

$$= (\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})(\overline{MFS})(\overline{YW1})(HVP)$$

At Gate 11:

$$MD = \overline{\overline{(\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})} + (\overline{MFS}) + YW1 + \overline{HVP}}$$

$$= (\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})(MFS)(\overline{YW1})(HVP)$$

At Gate 12:

$$MD = \overline{\overline{(\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})} + (\overline{MFS}) + \overline{YW1} + \overline{SID}}$$

$$= (\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})(MFS)(YW1)(SID)$$

At Gate 13:

$$MD = \overline{(XW1 + XW2 + XW3) + NFS + \overline{YW1} + \overline{S1D}}$$

$$= (\overline{XW1} \cdot \overline{XW2} \cdot \overline{XW3})\ (\overline{MFS})\ (YW1)\ (S1D)$$

At Gate 14:

$$MD = \overline{(\overline{XW1} + XW2 + XW3) + MFS + \overline{YW1} + \overline{SCS}}$$

$$= (XW1 \cdot \overline{XW2} \cdot \overline{XW3})\ (\overline{MFS})\ (YW1)\ (SCS)$$

At Gate 15:

$$MD = \overline{(XW1 + \overline{XW2} + XW3) + MFS + \overline{YW1} + \overline{MC2}}$$

$$= (\overline{XW1} \cdot XW2 \cdot \overline{XW3})\ (\overline{MFS})\ (YW1)\ (MC2)$$

At Gate 16:

$$MD = \overline{(\overline{XW1} + \overline{XW2} + XW3) + MFS + \overline{YW1} + \overline{DCSM}}$$

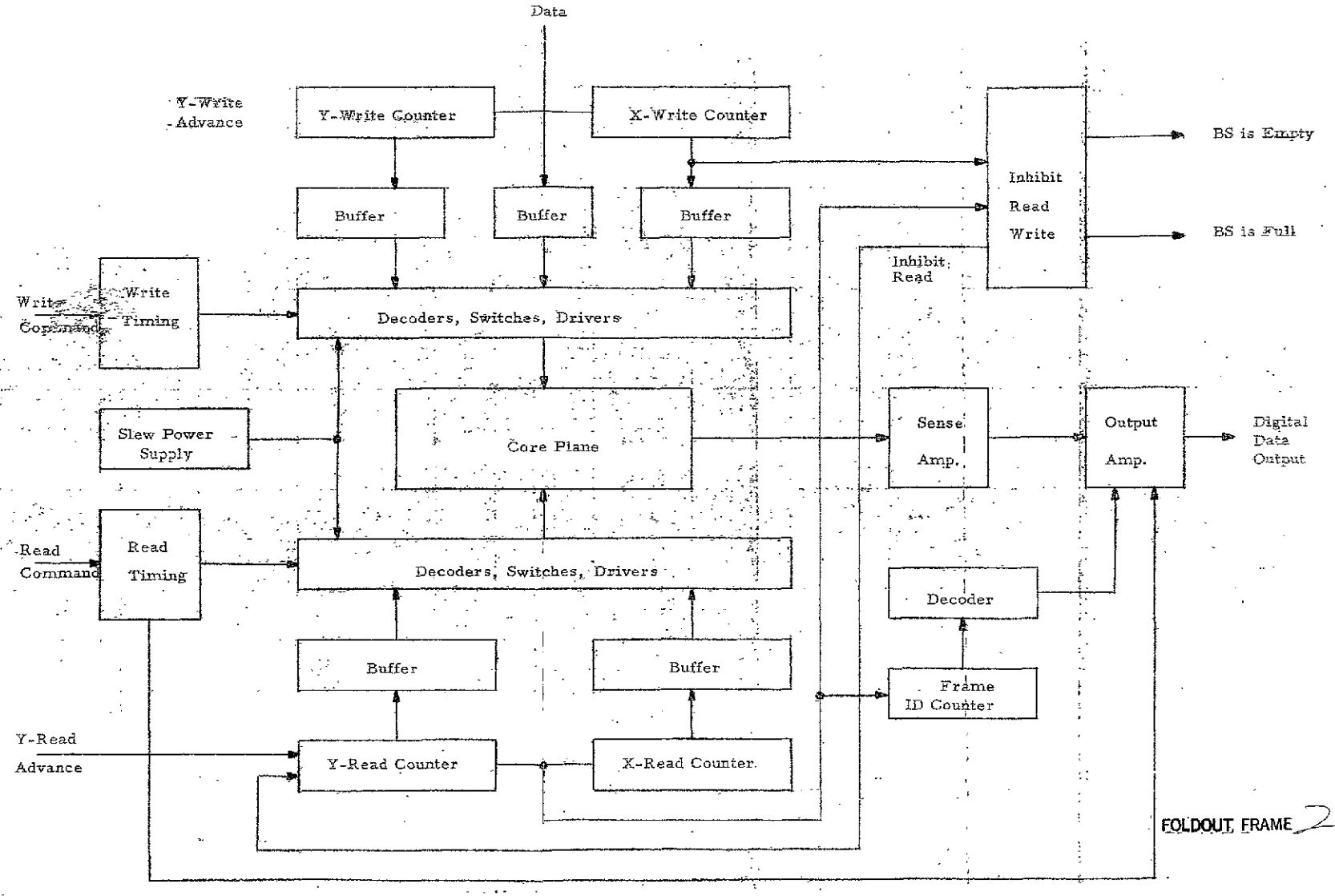
$$= (XW1 \cdot XW2 \cdot \overline{XW3})\ (\overline{MFS})\ (YW1)\ (DCSM)$$

Gates 17, 18 and 19 are three IC gates hard-wired as one 14-input gate to produce a composite $\overline{MD}$. Gate 20 inverts this to give MD

3.3 Buffer Storage.

Flux, Sector, High Voltage and MD information is stored in the Core Plane of the Buffer Storage Unit. This information is read out at a rate consistent with telemetry requirements and in correct sequence.

The Core Plane is divided into three sections of five frames each. Each frame consists of 44 bits. Two bits are used for MD storage and the rest for Flux, Sector or High Voltage.



FOLDOUT FRAME

FOLDOUT FRAME 2

Buffer Storage Block Diagram
Figure 3.3-1

During HBR operation, the instrument will take data for two revolutions of the spacecraft for each High Voltage Step. One revolution will be PS mode and AS mode. One PS and one AS completely fills one section.

At the beginning of each PS, during Sector 15, each section will be scanned in search for an empty section. If there are no empty sections, BS is Full will inhibit data taking for that revolution.

As each section is read out, each bit in that section is returned to 0.

During operation at LBR, data is taken for one revolution of the spacecraft at each High Voltage Step, followed by one revolution of PS and one of AS. This information is stored in one section of the storage.

For Ion cycles, the above sequence completely fills the three sections; then the instrument goes into stabilization while the memory is read out. At 64 BPS, the BS is Empty signal is given at the beginning of the tenth frame read-out, while at 16 and 8 BPS it is given at the beginning of the fifteenth frame read-out.

For an Electron cycle, only two sections (10 frames) are filled by each sequence. At 64 BPS, the BS is Empty signal is given at the beginning of the fifth frame read-out, while at 16 and 8 BPS it is given at the beginning of the 10th frame read-out.

The timing of this BS is Empty signal assures that the write-in counters will not overtake the read out counters.

Core Plane

The core plane consists of magnetic core elements, 80 mil OD, arranged in a 16x48 rectangular array. The assembly allows for spares. The useful array is 15x44.

Drivers and Switches

These circuits are built with discrete components and provide the necessary coincident current for writing into or reading out of the core memory. In order to provide cleaner core currents, the X and Y switches are turned on a short time before the X and Y Drivers. The drivers are then turned off shortly before the switches.

Each driver is simply a voltage switch with a series resistor to set the core current. Each switch, when turned on, provides a sink to ground for the core current.

Sense and Output Amplifiers

The sense line output of the core plane provides a balanced bipolar voltage, of 50-60 mv peak amplitude.

The sense amplifier provides gain for the sense line voltag and also full-wave rectification. Therefore, the output voltage is uni-polar regardless of the input voltage polarity.

The output amplifier receives the output of the sense amplifier and shapes it into a pulse with acceptable characteristics. This amplifier is normally inhibited until Strobe Pulse turns it on. This occurs near the middle of the Read Pulse time.

Write and Read Counters

Separate X and Y counters are used for providing core memory address for the Read Function and the Write Function. The X-Read counter is similar to the X-Write while the Y-Read is similar to the Y-Write.

The Y-Write Counter is driven by the Y-Write Advance pulses while the Y-Read Counter is driven by the Y-Read Advance pulses. Each counter is arranged to count to 44, at which time it produces an X Counter Advance pulse.

Each X Counter is composed of a three stage counter followed by a two stage counter. The three stage circuit counts to 5 then resets to zero. At the same time, it produces an input to the two stage circuit. This circuit counts to 2; then with the third pulse both circuits are reset to zero.

Buffer Interfaces

These provide the necessary buffering between the Integrated Circuit counters and data circuits and the switches and drivers which use discrete components.

Write Pulse Train

This circuit accepts the Write Pulse from the Buffer Logic. Each Write Pulse generates a train of either 2 or 7 Write Commands. The train of two pulses writes in the MD each train of 7 writes in a flux or sector word. Immediately following each Write Command, an Advance Y-Write pulse is generated to step the Y-Write counter.

Write Timing

Each Write Command causes this circuit to generate signals which turn on the Write drivers and switches.

Read Timing

Each Shift Data pulse causes the read-out of one core element. The Read Timing circuit accepts each Shift Data pulse and generates the signals to turn on the Read Drivers and Switches. It also generates the strobe pulse to turn on the Data Output Amplifier.

Frame ID Counter

This circuit consists of a four stage counter, a two stage counter and appropriate gates.

The four stage counter counts from 1 to 15 and is advanced by the Advance X-Read pulse.

The two stage counter counts from 0 to 3 and is advanced by the Shift Frame ID from the Buffer Logic.

The outputs of these counters are gated to produce ID Data which is transmitted through the Data Output Amplifier by the Shift Frame ID pulses.

Inhibit Read-Write

This circuit consists of three flip-flops used as storage elements. Each flip-flop is associated with one of the three memory sections. When Section 1 is empty, Q1 is high. For Section 2 empty, Q2 is high, and likewise for Section 3 and Q3.

When Section 1 is written into, Q1 goes low, and likewise for the other two sections. The flip-flops are set or reset by detecting the changes of state of the two stage sections of the X-Read and X-Write counters.

If the Write Counters are ready to write into a memory section that has not been read out, the BS is FULL signal goes True and data taking is inhibited until that section is read out.

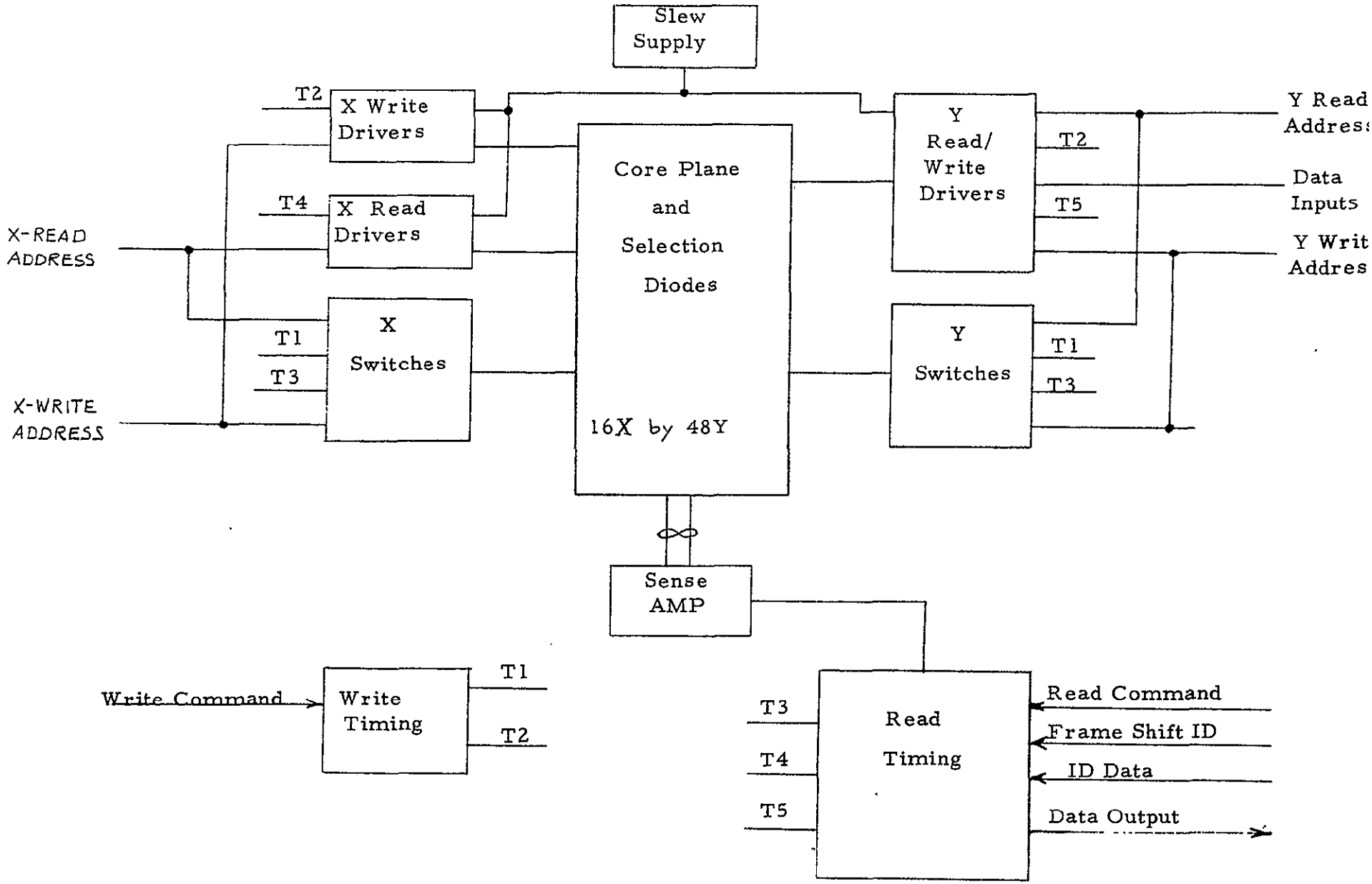
If the Read-Counters are ready to scan an empty section, the Read Counter is inhibited.

3.3.1 Core Plane Memory

For the Memory System Electrical Specification and the Core Memory Plane Specification, refer to Appendix D.

3.3.1.1 Memory Organization

The block diagram of the memory subsystem is shown in Figure 3.3.1-1.



Memory Block Diagram
Figure 3.3.1-1

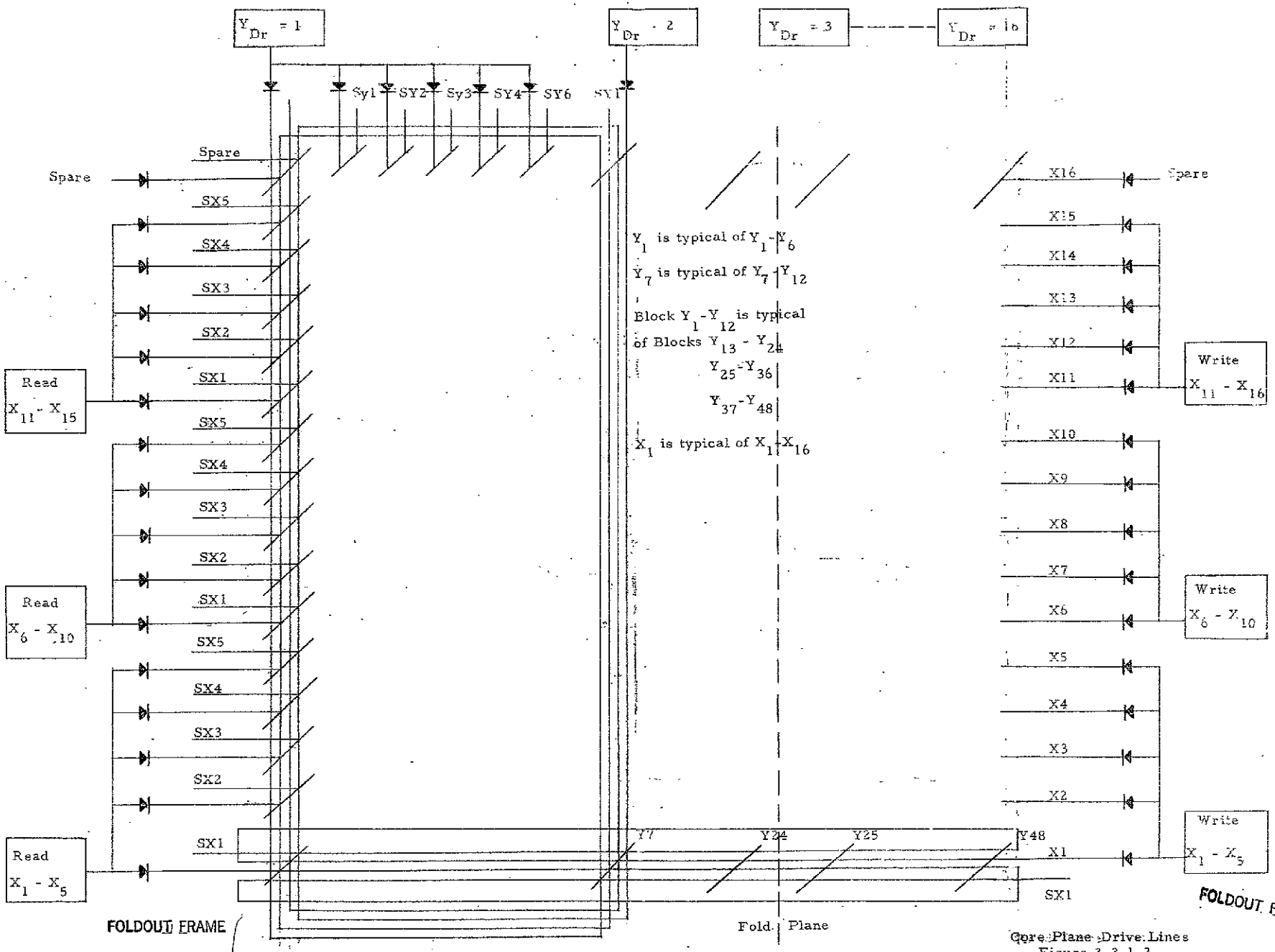
The core plane contains 768 ferrite cores wired for coincident current selection. Figure 3.3.1-2 shows the wiring of the core plan drive lines, and the decoding of these drive lines. Figure 3.3.1-3 shows the wiring of the sense line.

The core memory element used is an 80 mil O.D. ferrite core, Ampex Computer Products part number 32-48068-20.

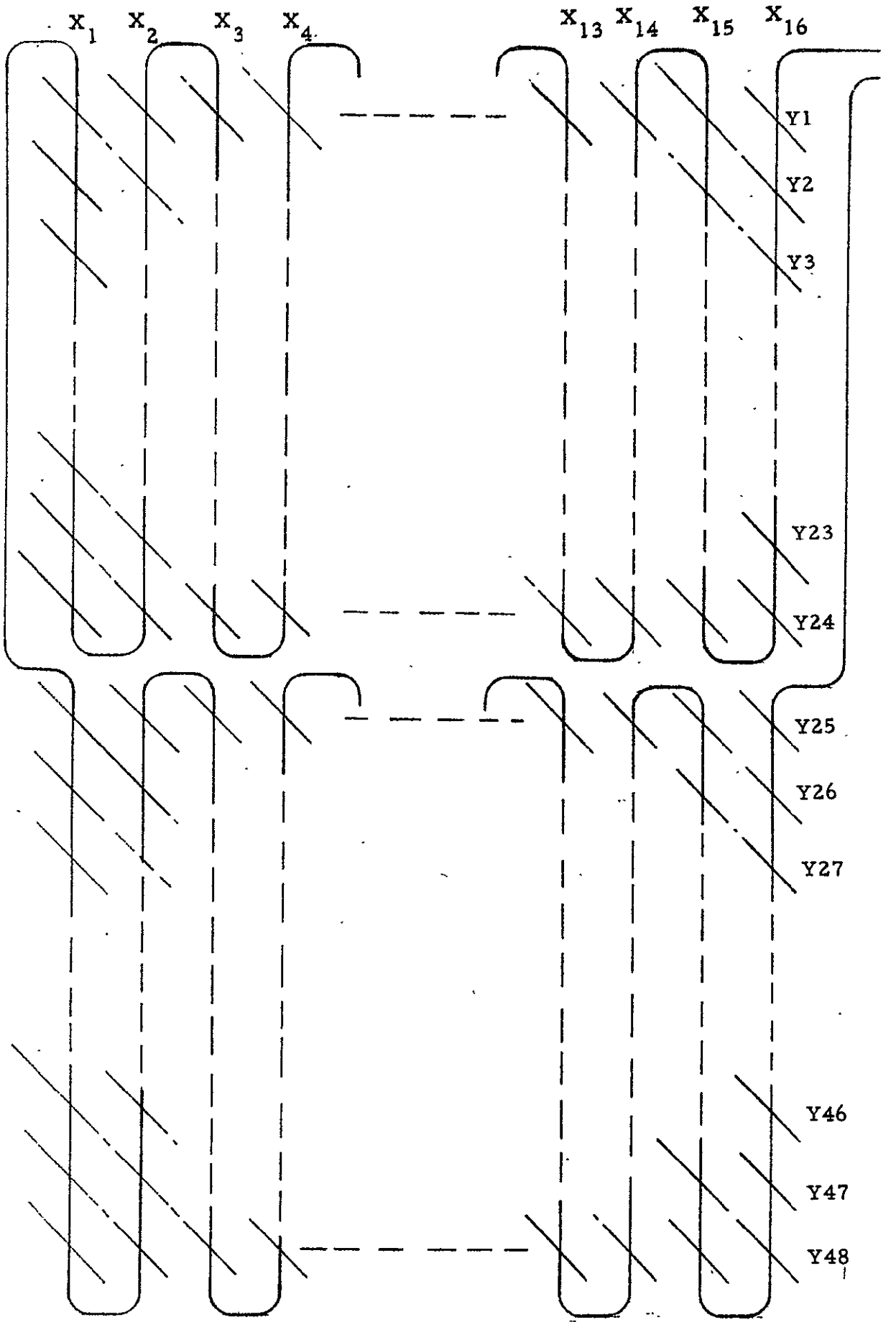
The 768 core memory elements form a rectangular array of 16 X columns, X1-X16, by 48 Y rows, Y1-Y48. The array is physically folded between Y24 and Y25. The maximum required memory capacity is 660 bits. Thus, X16 column is spare and is not normally connected to the X drivers or X switches. The further limiting of the provided array capacity is controlled only by the constraints on the counting sequence used in the address resistors external to the memory. The address register sequence used selects only X1-X15 and Y1-Y44. The resulting used storage capacity is 15x44 = 660 bits.

The core plane wiring technique employs 9 wires. Two turns per core are used on both the X and Y axes to reduce the amplitude of the currents required. In addition, oppositely directed wires are used on each axis for read and write, thus eliminating the necessity of bipolar drivers and switches. The resulting 9 wires per core consist of 4 X axis lines (2X write, 2X read), 4Y axis lines (2Y write, 2Y read), and the sense line. The sense line links every core on the plane and is routed to minimize resultant capacitive coupling from the drive lines.

The 15 X columns are decoded 6 by5 for Read and Write. For Write, 1 of 3 Write drivers is selected as a source, and 1 of 5 common switches is selected as a sink. For Read, 1 of 3 read drivers is selected as a source, and 1 of the 5 common switches is selected as a sink. Diodes are used for unselected X line isolation.



Core Plane Drive Lines
Figure 3.3.1-2



Sense Line Wiring

Figure 3.3.1-3

The 48 Y Rows are decoded by 16 by 6 for read and write; however, only 8 Y drivers and 6 Y switches are employed. The additional factor of 2 in the driver decoding is obtained by linking 2 Y rows with the line from each Y driver; and using this line to write in the first linked Y row or read from the second linked Y row, as determined by the mode and thus the direction of the X current selected for the mode. For a particular mode (Read or Write), 1 of 8 Y drivers is selected as a source; 1 of 6 Y switches is selected as a sink. Diodes are used for unselected Y line isolation.

The slewed Voltage Reference is a voltage source. The output voltage varies with a temperature coefficient of approximately -80 mv/^{o}C. The slewed voltage reference is applied to the X and Y Drivers and is used to provide a temperature compensated current to the core memory elements of the array. A temperature compensated current maintains constant element outputs and simplifies driver and sensing circuit designs.

The Read and Write Drivers and Switches are selected as a function of the status of the Read and Write address registers, data register, and the mode selected. Address, data, and mode are controlled external to the memory.

For a Write mode, the Write timing circuits function to gate and time-sample the Write address and data from the switch and driver logic and thus direct Write currents to the proper element.

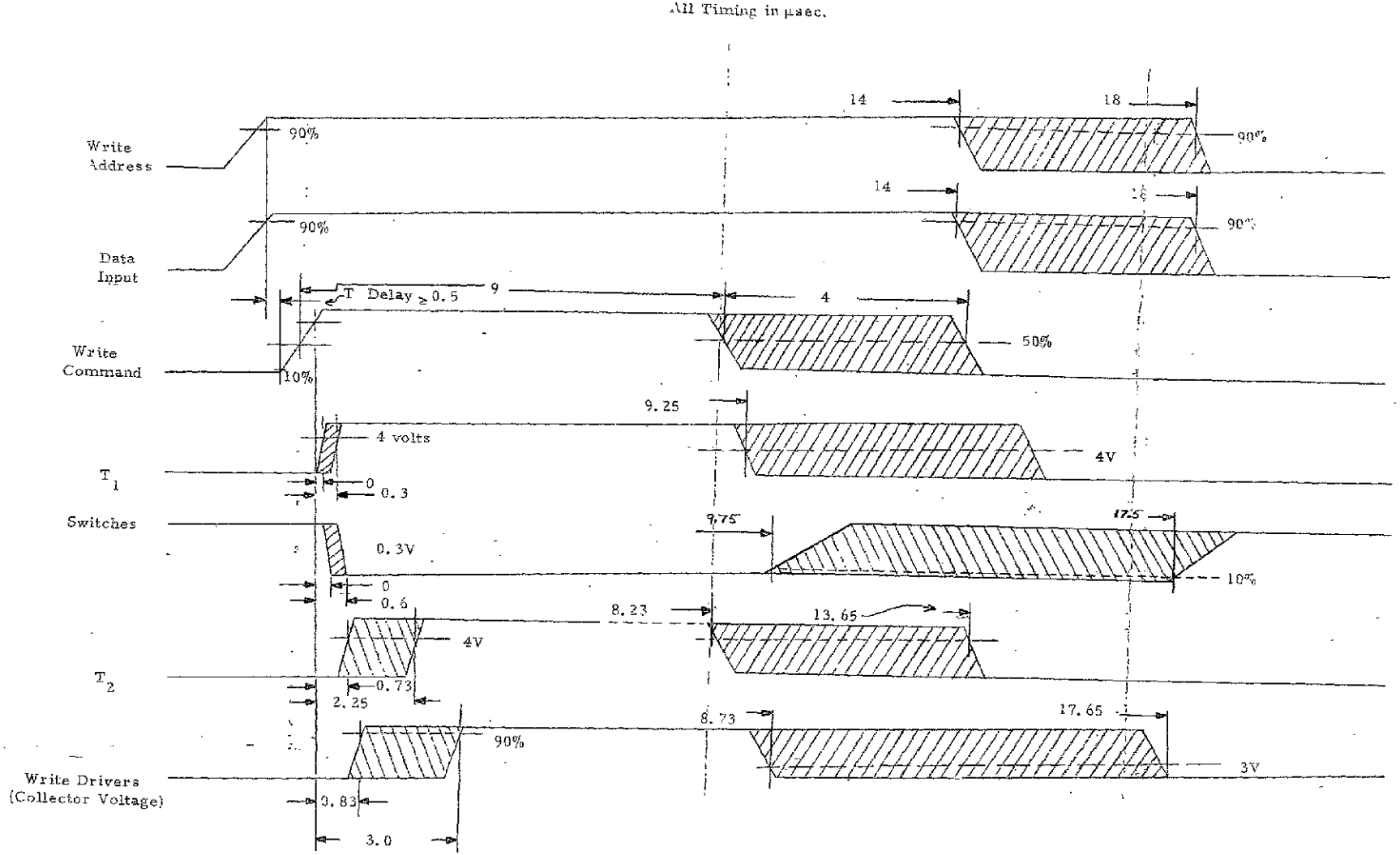
For a Read mode, the Read timing circuits similarly direct read currents to the proper element, time strobe the sense amplifier read out, and form a usable output data pulse. Read timing circuits also allow time-sharing the data output line for frame shift I. D.

3.2.1.2 Memory Operation

The operation of the memory is controlled by the address inputs, data inputs, and the Read and Write command levels. Although the memory has a full random access capability, the operating mode is sequential interlace, i.e., the Read and Write addresses are generated sequentially and Read or Write commands may be interlaced. In fact, separate Read and Write address registers are used, and the Read and Write timing circuits gate the desired address to the drivers and switches depending upon the command levels.

Information is stored and retrieved one bit at a time. Thus 720 Write cycles are required to completely fill the storage capacity, and 720 Read cycles are required to read out the data from all 720 storage locations. Figure 3.3.1-4 is the Write cycle timing diagram.

Consider the sequence of operations required to write a "1" in the first storage location. The Write address input lines and the data input lines must have attained 90% of their final value at least 0.5 microseconds prior to the time that the Write command has reached 10% of its final value. After the Write command has reached +2 volts, the Write timing circuits generate timing pulse T1, which then provides voltage to the logic gates at the inputs of the X and Y switches. The outputs of the selected X and Y switches fall +0.2v maximum providing a low impedance sink for the positive Write currents. X switch SX1 and Y switch SY1 are selected for the first storage location. All other switch outputs remain at the +3 volts level insuring that the diodes on unselected lines remain back biased for this address input.



FOLDOUT FRAME

Write Cycle Timing Diagram

Figure 3.3.1-4

FOLDOUT FRAME

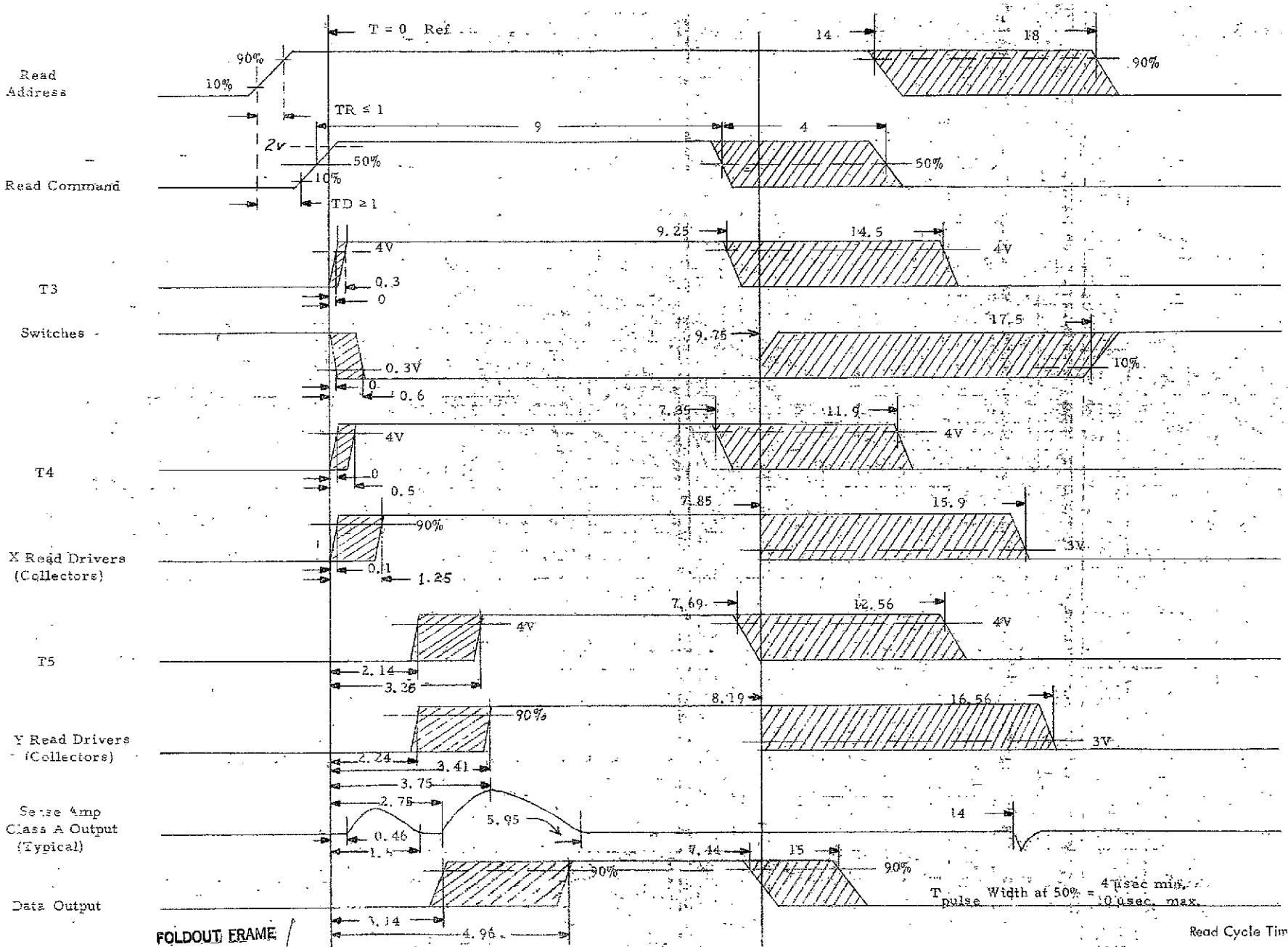
After an internal delay to allow for switch settling, the Write timing circuits generate timing pulse T2. T2 then provides voltage to the logic gates at the inputs of the X Write Drivers and the Y Read/Write Drivers. The outputs of the selected drivers are positive currents. The amplitude of the current is determined by the slew supply output voltage and a precision resistor.

Write X1-X5 Driver and Y Driver No. 2 are selected for the first storage location. All other drivers are off, with outputs at 0 volts.

The X Write current passes through all elements in column X1 twice and returns by way of SX1. The Y Write current passes through all elements in rows Y1 and Y7 twice and returns by way of SY1. The element at S1, Y1 receives a full select Write current and is switched to the remanent state designating a stored "1". The element at X1, Y7 receives zero net current and its state is essentially unchanged. The remainder of the effect elements receive half select currents, shuttle, and return to their original state following the removal of the write currents.

At the end of pulse T2 the driver currents drop to zero. At the end of pulse T1 the switches turn off and the ouputs return to +3 volts. 5 Microseconds after the write command has dropped to 10% of its value the address and data inputs may change state.

Figure 3.3.1-5 is the Read Cycle Timing diagram. Consider the sequence of operations required to read out the data stored in an element, for example the first storage location.



Read Cycle Timing Diagram
Figure 3.3.1-5

The Read address lines must have attained 90% of their final value at least 0.5 microseconds before the Read command has reached 10% of its final value.

After the Read command has reached +2 volts, the Read timing circuits generate timing pulse T3, which then provides voltage to the logic gates at the inputs of the X and Y Switches. The outputs of the selected X and Y Switches fall to +0.2v maximum, providing a low impedance sink for the positive Read currents. Switches SX1 and SY1 are selected for reading from the first storage location. All other switches are off.

After an internal delay for switch settling, the Read timing pulse T4 is generated, providing voltage to the logic gates at the inputs to the X Read Drivers. The driver output is a positive current. Read X1-X5 driver is selected to read this first storage location. All other X drivers are off.

After a second internal delay to allow for the noise coupled to the sense line from the X drive line to settle, Read timing pulse T5 is generated, providing voltage to the logic gates at the current lagging the X current. Y Driver No. 1 is selected, and all other drivers are off.

The X current through X1 column is oppositely directed relative to the Write current but still returns by way of SX1. The Y current rows Y1 and Y7 are also oppositely directed relative to write current but still returns by way of SY1. The element at X1, Y1 receives a full select Read current and switches from the "1" to the "0" state. The switching of the core flux from the "1" to the "0" state causes a differential voltage to be coupled to the sense line via the sense line to the input of the sense amplifier.

The remainder of the selected cores operate essentially the same as in the Write cycle. Driver voltages and current time out and decay as in the Write cycle. The Read address again must be maintained for 5 microseconds after the end of the Read commands.

The differential signal on the sense line is amplified in the Sense Amplifier, and if of sufficient amplitude to be considered as "1", is applied to the Read timing output one-shot.

The sense amplifier output and the time strobe pulse are applied to an "AND" gate on the input of the data output one-shot. For coincidence of signal and strobe, such as in this case of a read out "1", the output one-shot is triggered and an output data pulse must start within 6.5 microseconds after a Read command (Shift Pulse) and be of 4 microseconds minimum duration.

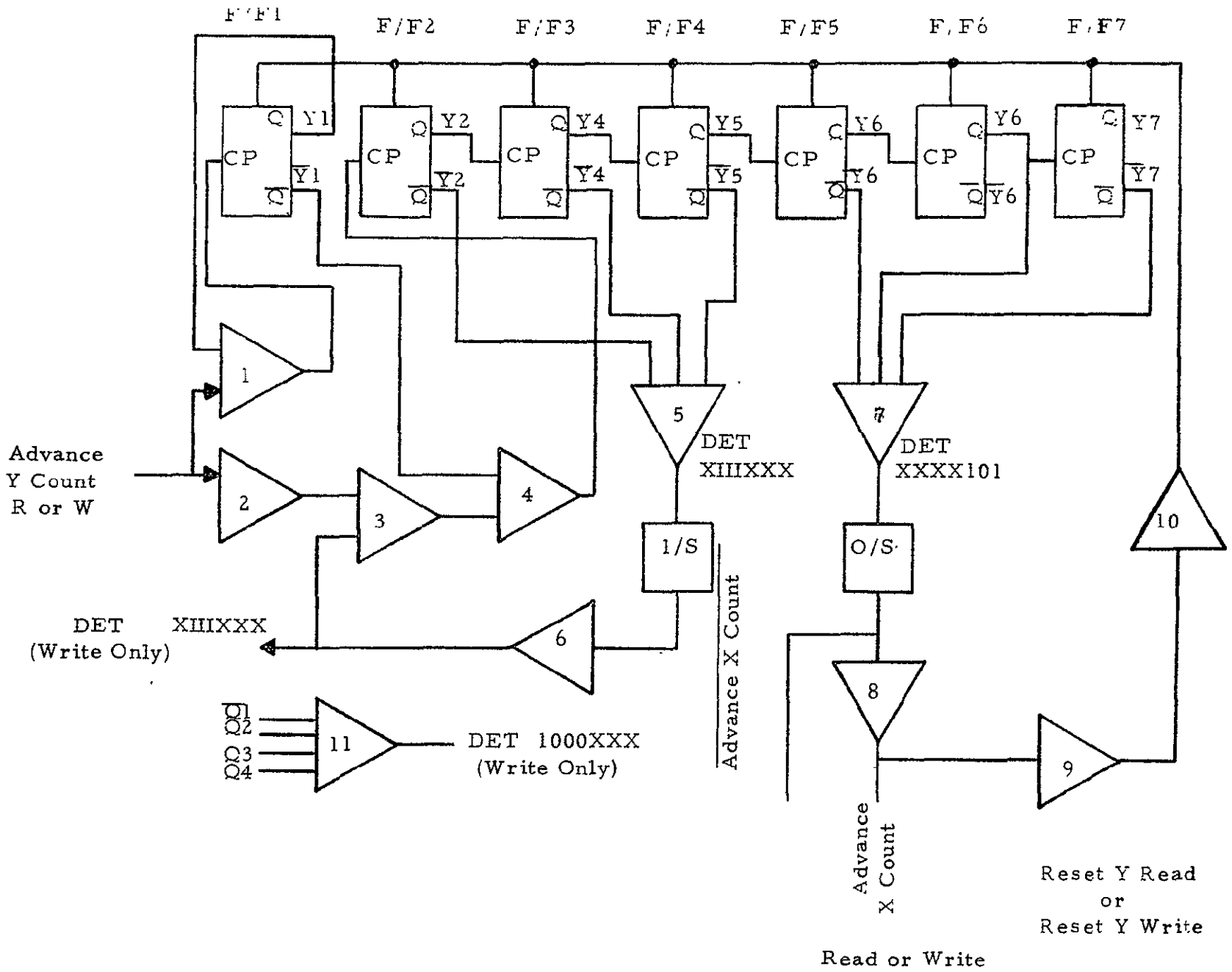
The input to the output data one-shot is a two input OR gate. The first input is that discussed for the Read cycle, the second input is used to provide output pulse, with the same characteristics as a data output pulse, for coincidence of Frame shift ID and 1D Data inputs. As a result the output is time shared by two functions.

3.3.2 Buffer Interfaces

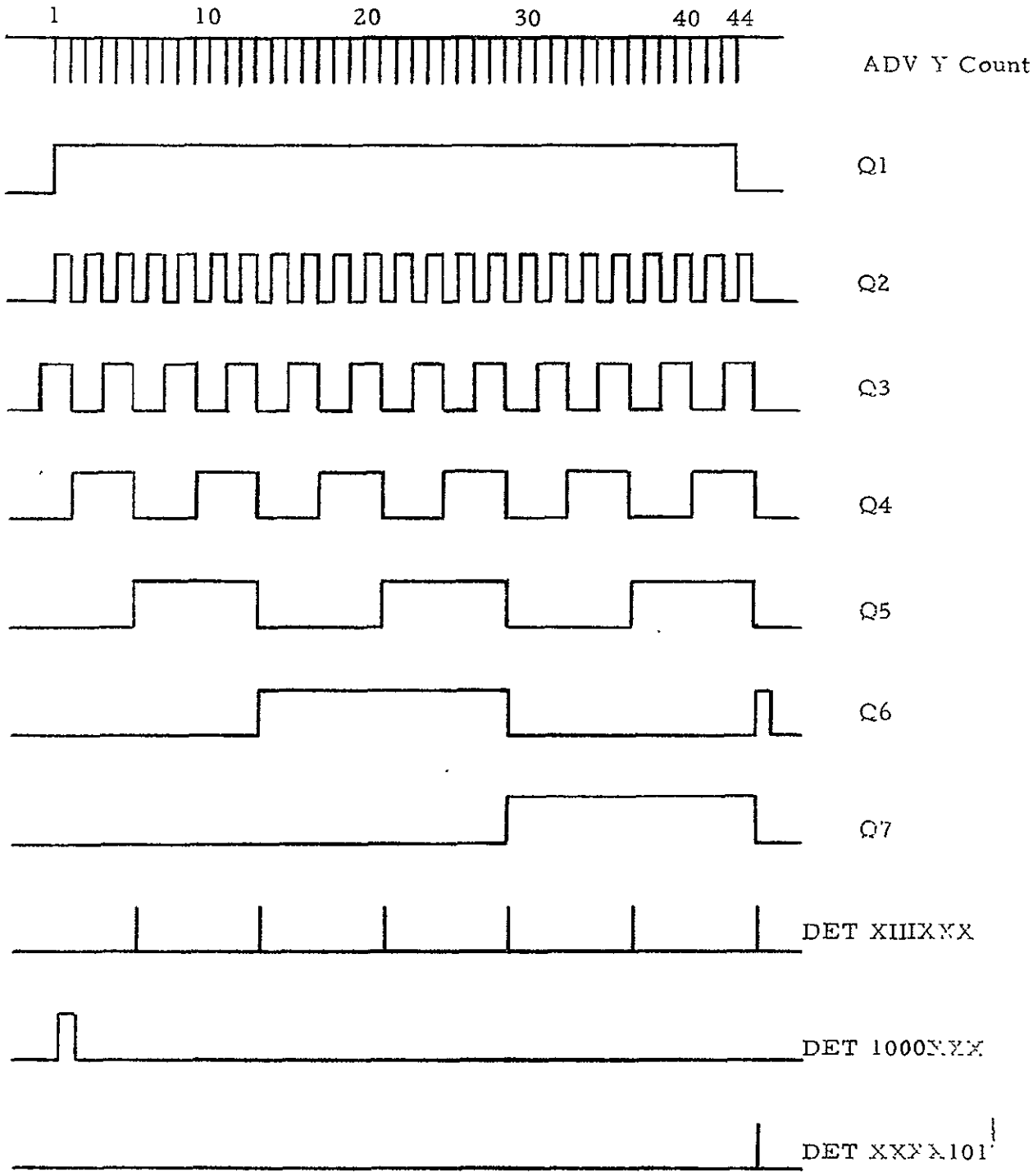
These are Inverting Buffers to reduce the loading on the Write and Read Counter outputs. The Buffer outputs drive the logic gates associated with the Core Plane Drivers and Switches.

3.3.3 Y Counters

The Y Read and Y Write counters are identical. They each take 44 advance pulses to count through a complete sequence. Operation is as follows (refer to Figure 3.3.3-1 for the Logic Diagram and Figure 3.3.3-2 for the Timing Diagrams).



Y Counters Logic Diagram
Figure 3.3.3-1



Y-Counters Timing Diagram
Figure 3.3.3-2

The first advance pulse passes through Gate 1 and sets Flip-Flop 1. Q1 then inhibits Gate 1 and $\overline{Q1}$ enables Gate 4. The remaining 43 pulses of the sequence pass through Gates 2, 3, and 4 to Flip-Flop 2. The eighth pulse sets Flip-Flops 2, 3, and 4. The ninth pulse resets these and sets Flip-Flop 5. At the same time Gate 5 detects every seventh count. The 44th count is detected by Gate 7 which generates a pulse to reset the whole counter to zero. This last pulse is also used to advance the X-counter.

Advance Y Write is derived from the 16 KHz(d) signal, whereas Advance Y Read is derived from the shift data signal.

The detect X111XXX and the detect 1000XXX signals are used by the Write Pulse Train Generator.

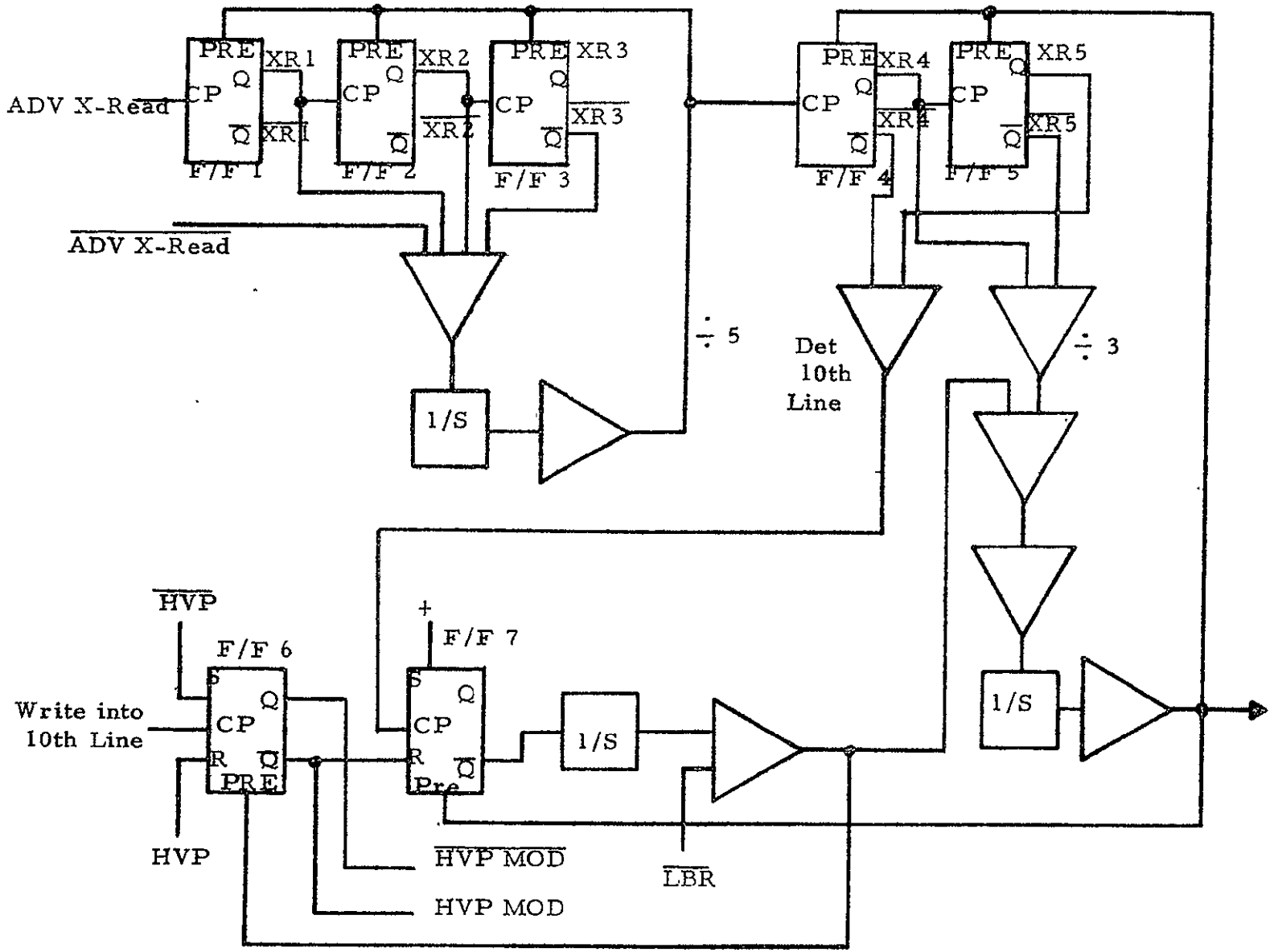
3.3.4 X Counters

Figure 3.3.4-1 shows the X Read Counters Logic Diagram. Figure 3.3.4-2 shows the X-Write Counters Logic Diagram.

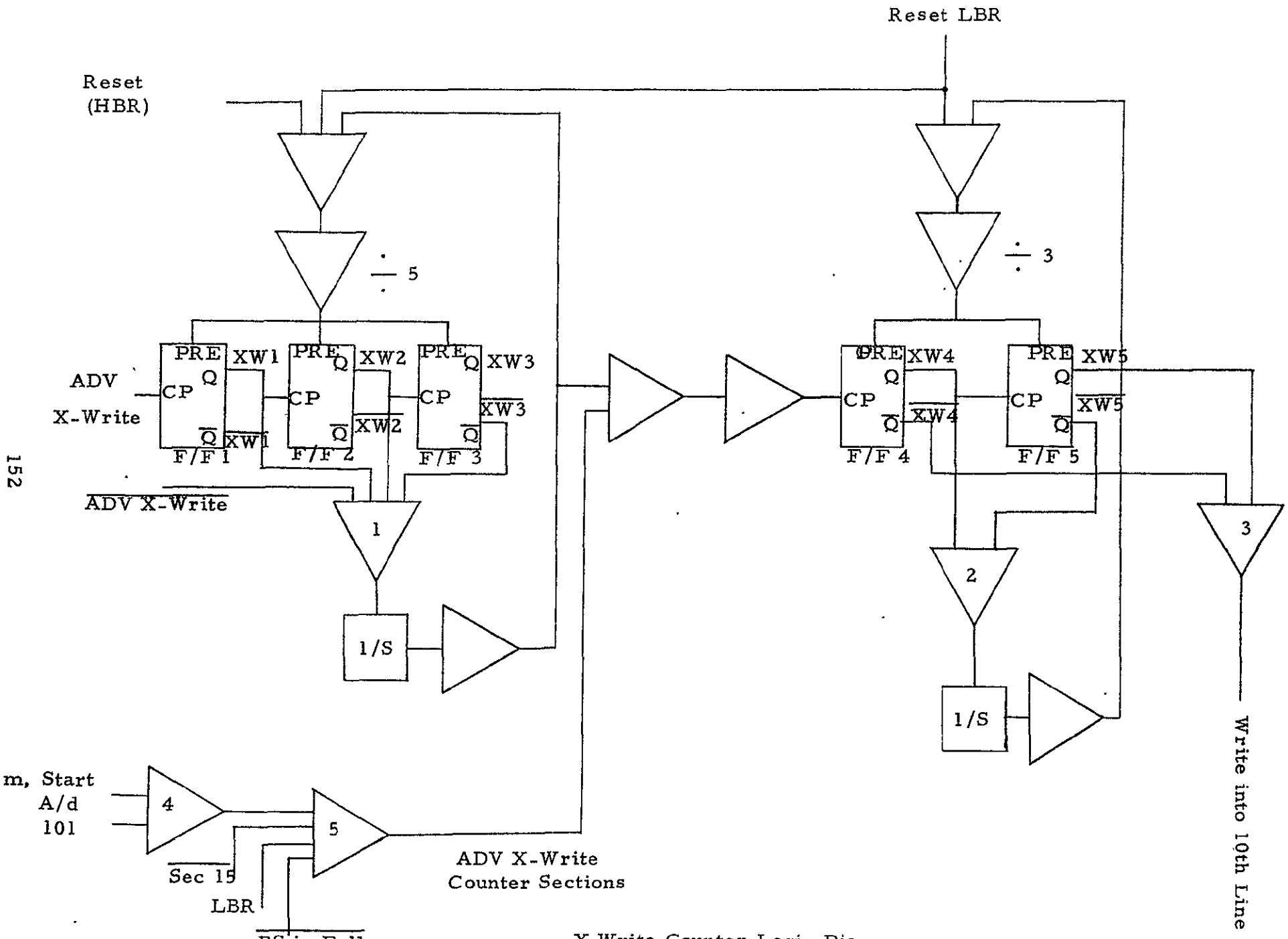
The X-Write Counter consists of a three stage divide-by-5 counter followed by a two stage divide-by-3 counter. The three stage section is driven by the Advance X-Write pulse which is generated by the Y-Write Counter Reset. At the count of five, Q1, Q2 and $\overline{Q3}$ enable Gate 1. The next $\overline{\text{Advance X-Write}}$ pulse triggers a one-shot which resets the three stage section and advances the two stage section.

At the third advance of the two stage section, Gate 2 triggers a one-shot which resets the two stage section.

The output of Gate 3 follows Q4. The trailing edge of this signal is called Write 10th Line and is used to clock the HVP Mod flip-flop which is part of the X-Read counter circuit.



X- Read Counter
Figure 3.3.4-1



X-Write Counter Logic Diagram
Figure 3.3.4-2

As was mentioned previously, when the BS is Full signal is high, that section of the memory being addressed has already been written into but not read out. At this time a search is made for an empty memory section.

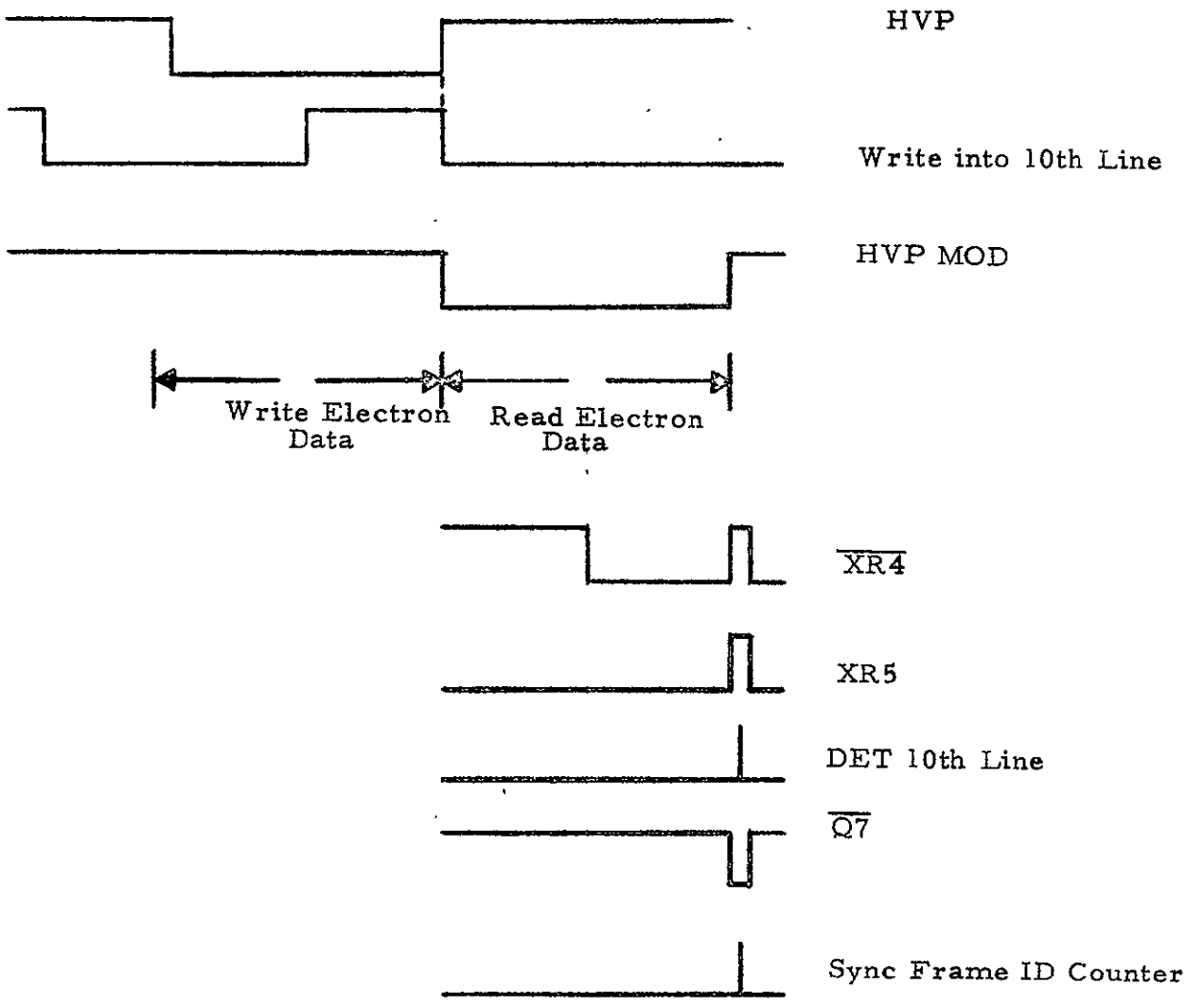
This BS is Full signal is generated by the Inhibit Read-Write Logic (Section 3.3.7) and is a function of the state of the two stage section of the X-Write Counter and the preceding history of the two stage section of the X-Read Counter.

During Section 15, as with the other sectors, 3 pulses are generated: two Start A/D's and one 101. At HBR, if BS is Full, these three pulses will be passed by Gates 4 and 5 to advance the two stage section of this counter. The changes of state of Flip-Flop 4 and Flip-Flop 5 naturally change the core memory address. If the first or second advance sets up an address to an empty section, the BS is Full signal goes down and Gate 5 is inhibited. This empty section is then written into if data is available.

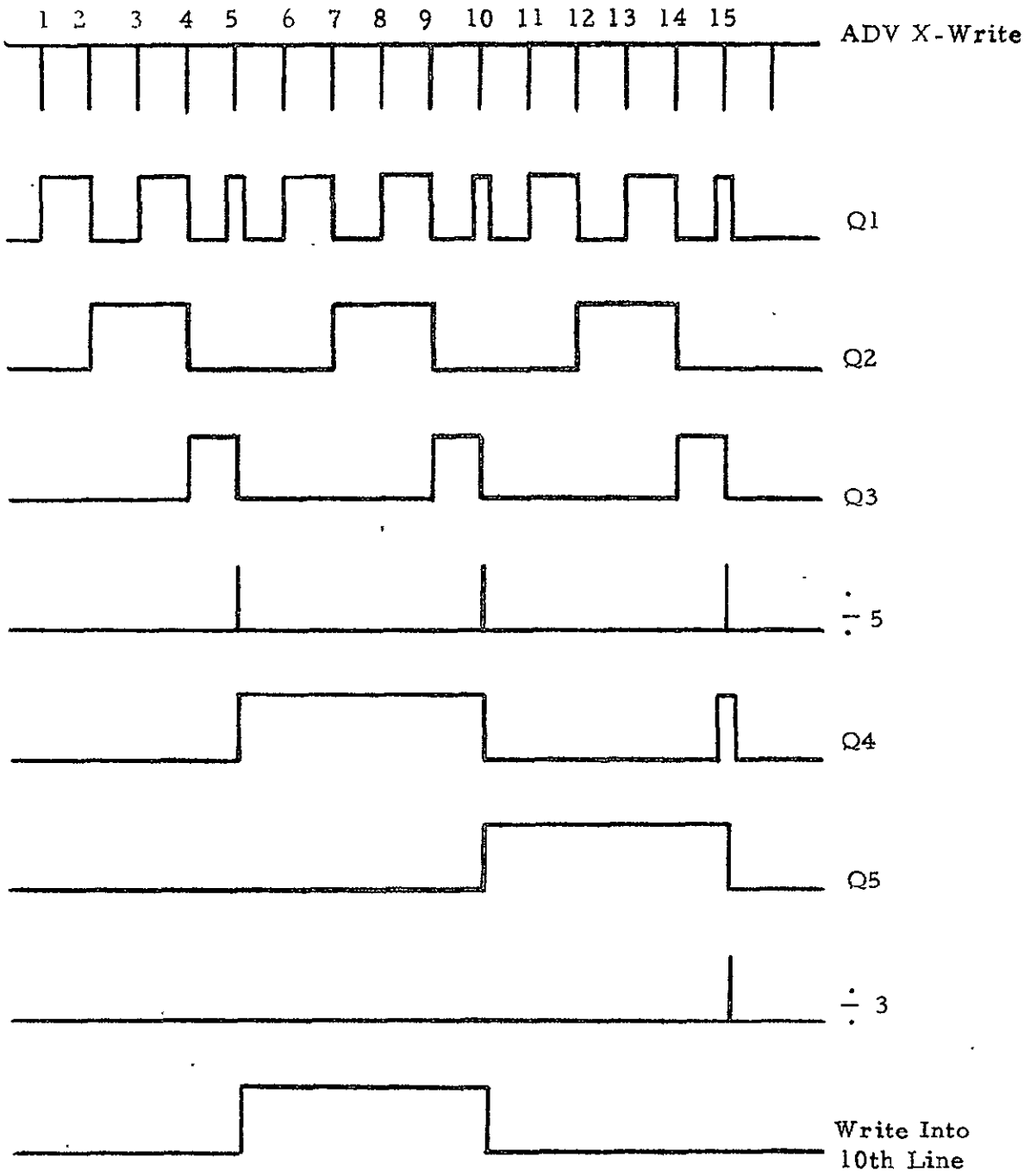
The X-Read Counter counts and resets in the same manner as the X-Write Counter. Its input is the X-Read Advance from the Y-Read Counter Reset. The pulse that resets the two stage section is also used to synchronize the Frame ID Counter.

During Electron Cycle at LBR data is entered into only the first and second sections of the memory; therefore, it is necessary to address only these frames for the read out.

At the start of Electron cycle, HVP goes down and $\overline{\text{HVP}}$ goes up. When the 10th frame has been written into, Flip-Flop 6 is set. This reverses the polarity of HVP Mod and $\overline{\text{HVP Mod.}}$ Then when the 10th frame has been read out, Flip-Flop 7 is set and $\overline{Q7}$ triggers a one-shot. The output of this one-shot resets Flip-Flop 7 and the two stage section of the counter. Refer to Figure 3.3.4-3, HVP Mod Timing Diagram. Also see Figure 3.3.4-4 for the Timing Diagram of the X-Write Counter.



HVP MOD Timing Diagram
Figure 3.3.4-3



X-Write Counter Timing Diagram
Figure 3.3.4-4

3.3.5 Write Pulse Train Generator

This circuit generates the appropriate sequence of pulses for writing into the Core Memory and advancing the Y-Write Counter. See Figures 3.3.5-1 and 3.3.5-2 for the Logic and Timing diagrams.

Assume that Flip-Flop 1 is set. This inhibits Gate 3. Gate 1 is inhibited by One-Shot 1. The Write Pulse from the Buffer Logic triggers One-Shot 1 which is adjusted to produce a 90 μsec pulse which enables Gate 1. This will allow one or two 16 KHz pulses through the gate to trigger One-Shot 2. The output of this one-shot resets Flip-Flop 1, enabling Gate 3. This allows the 16 KHz to trigger One-Shot 3 which is the Write Pulse Train. The first pulse of the train causes Det 1000XXX to go high. The second pulse causes it to go low, and sets Flip-Flop 1 which inhibits Gate 3 again.

The next Write Pulse from the Logic repeats sequence. However, this time 7 pulses of the train go through before the Det X111XXX pulse appears, setting Flip-Flop 1 and inhibiting Gate 3.

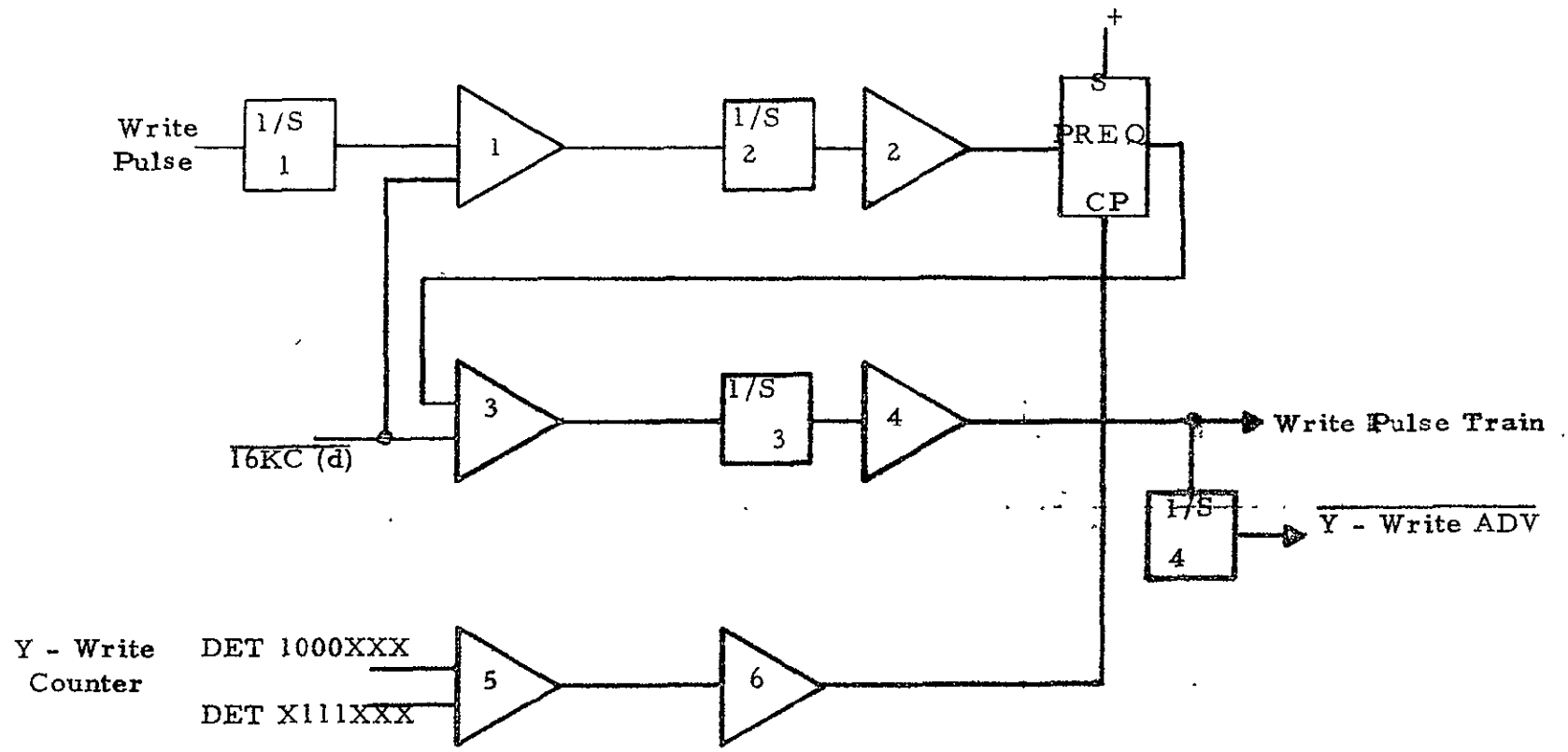
Seven Write Pulses from the Buffer Logic then produce a 44 pulse train. This fills one frame.

The fall of each pulse of the train triggers One-Shot 4 which produces $\overline{\text{Y-Write Advance}}$.

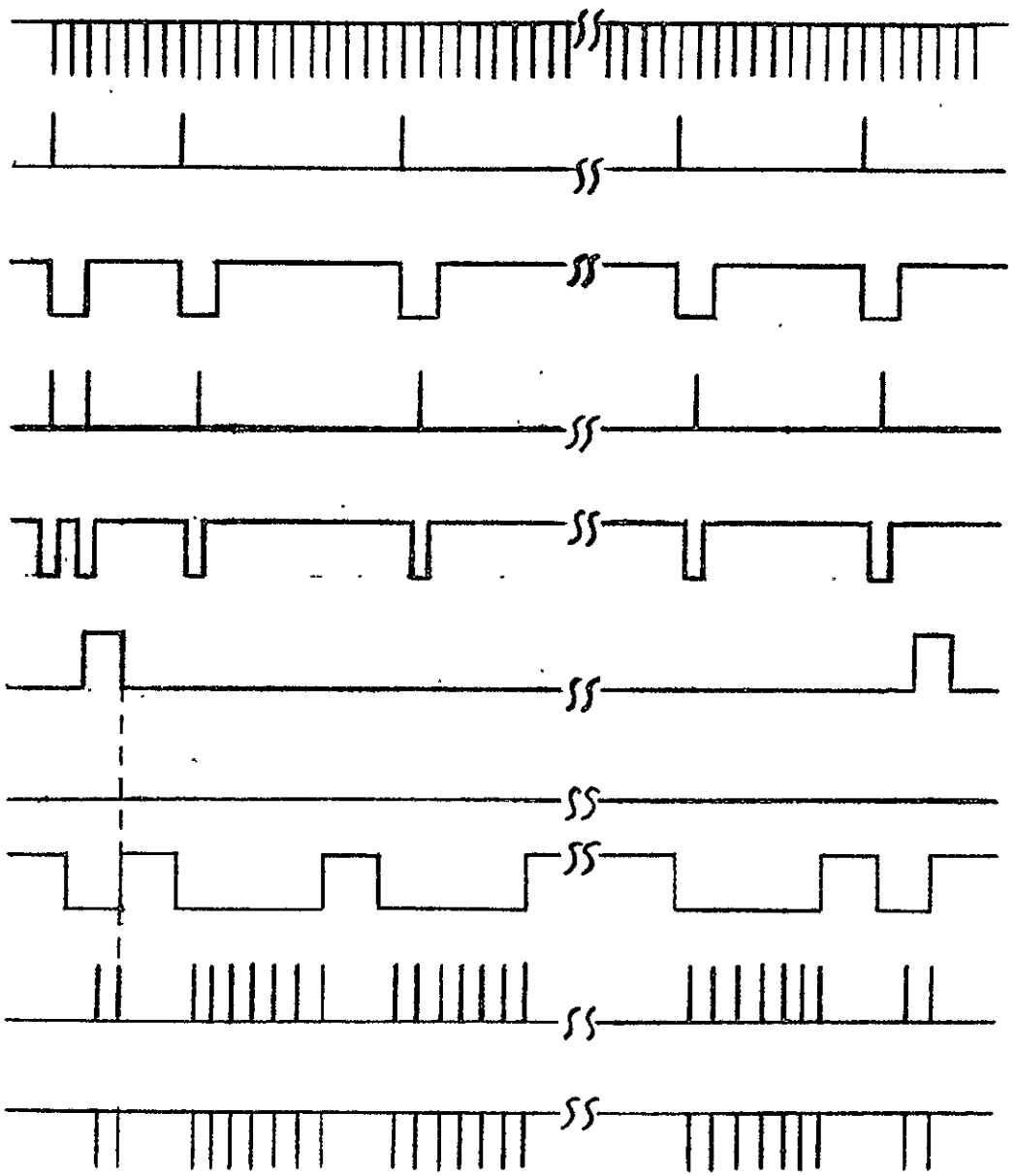
3.3.6 Frame ID Counter

Refer to Figures 3.3.6-1 and 3.3.6-2 for the Frame ID Counter Logic and Timing diagrams.

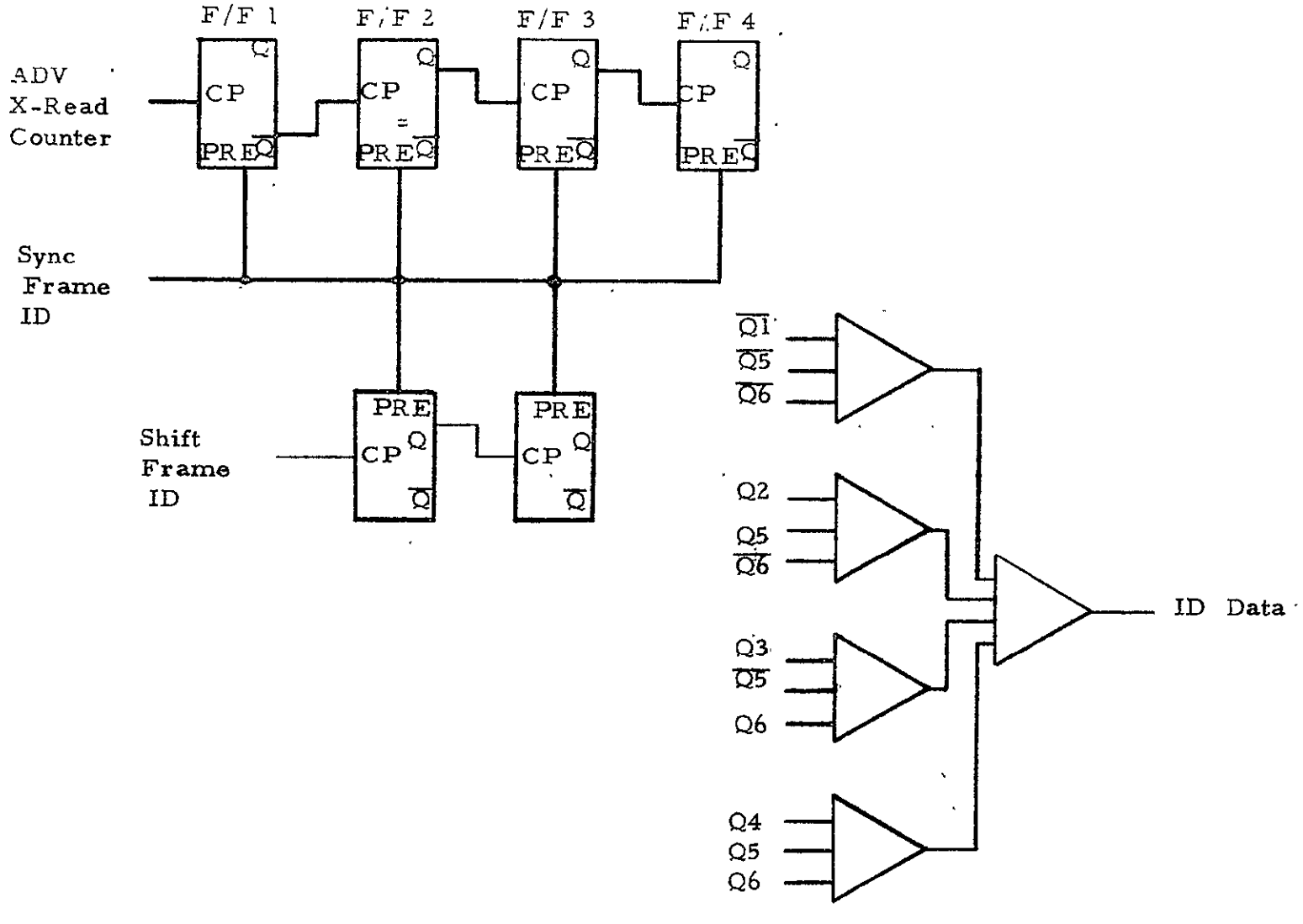
The Frame ID Counter is a simple ripple counter which is driven by the Advance X-Read signal then reset to zero by the Syn Frame ID. This latter signal is identical to that which resets the two stage section of the X-Read Counter.



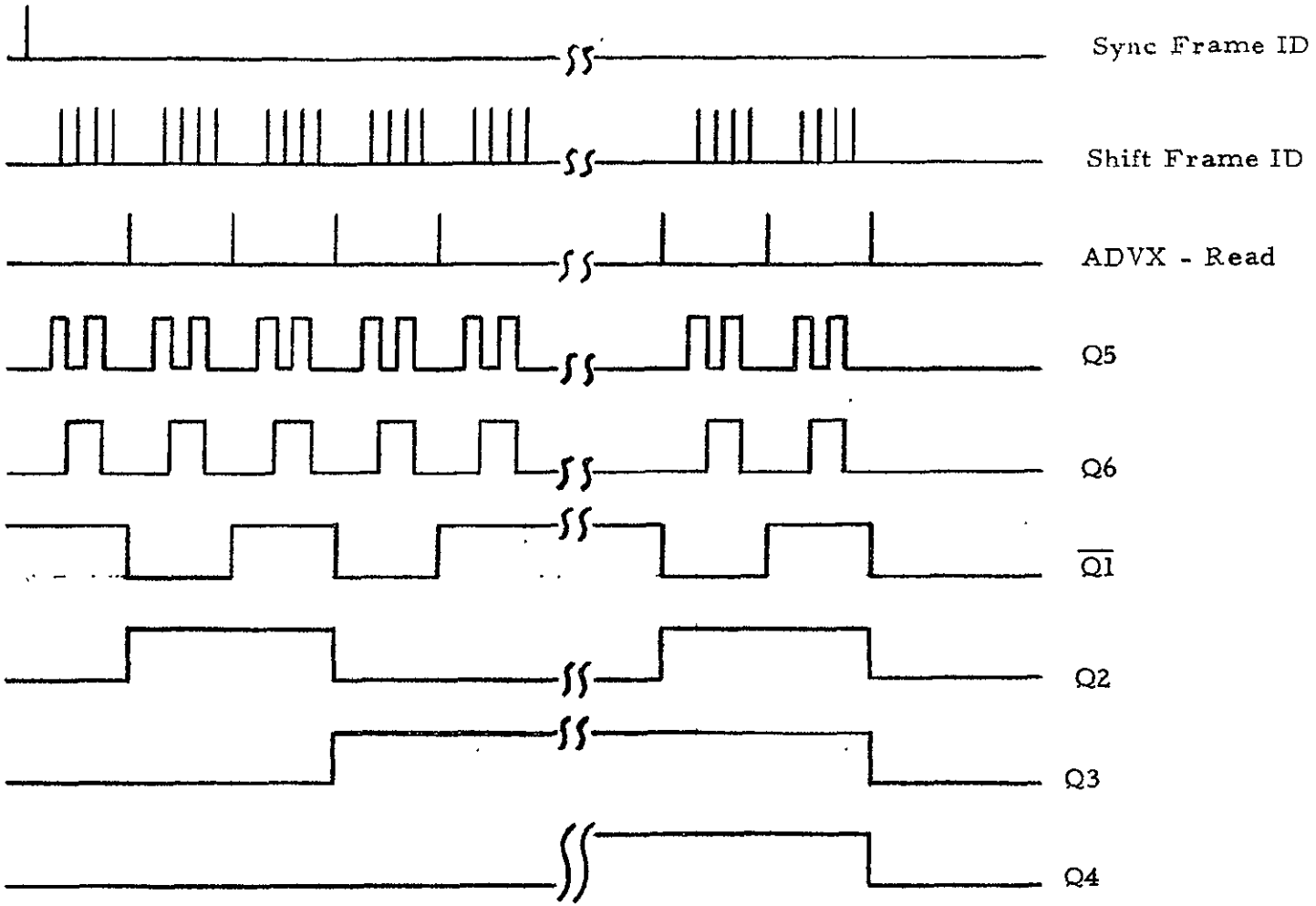
Write Pulse Train Generator Logic Diagram
Figure 3.3.5-1



Write Pulse Train Timing Diagram
Figure 3.3.5-2



Frame ID Counter Logic Diagram
Figure 3.3.6-1



Frame ID Counter Timing Diagram
Figure 3.3.6-2

The ID Data consists of sampling the states of Flip-Flops 1, 2, 3, and 4 consecutively. The sampling begins with the most significant bit, Q4. The four Shift Frame ID pulses at the beginning of each frame toggle the two stage counter (Flip-Flops 5 and 6) from zero through a count of three and back to zero.

Notice that the least significant bit of the Frame ID is $\overline{Q1}$ not Q1. This is so the first frame is read as 1000 before the first $\overline{\text{Advance X-Read}}$ pulse arrives.

3.3.7 Inhibit Read-Write

Figure 3.3.7-1 shows the Inhibit Read-Write Logic diagram. Refer to Figure 3.3.7-2 for the Timing diagram for the BS is Full signal.

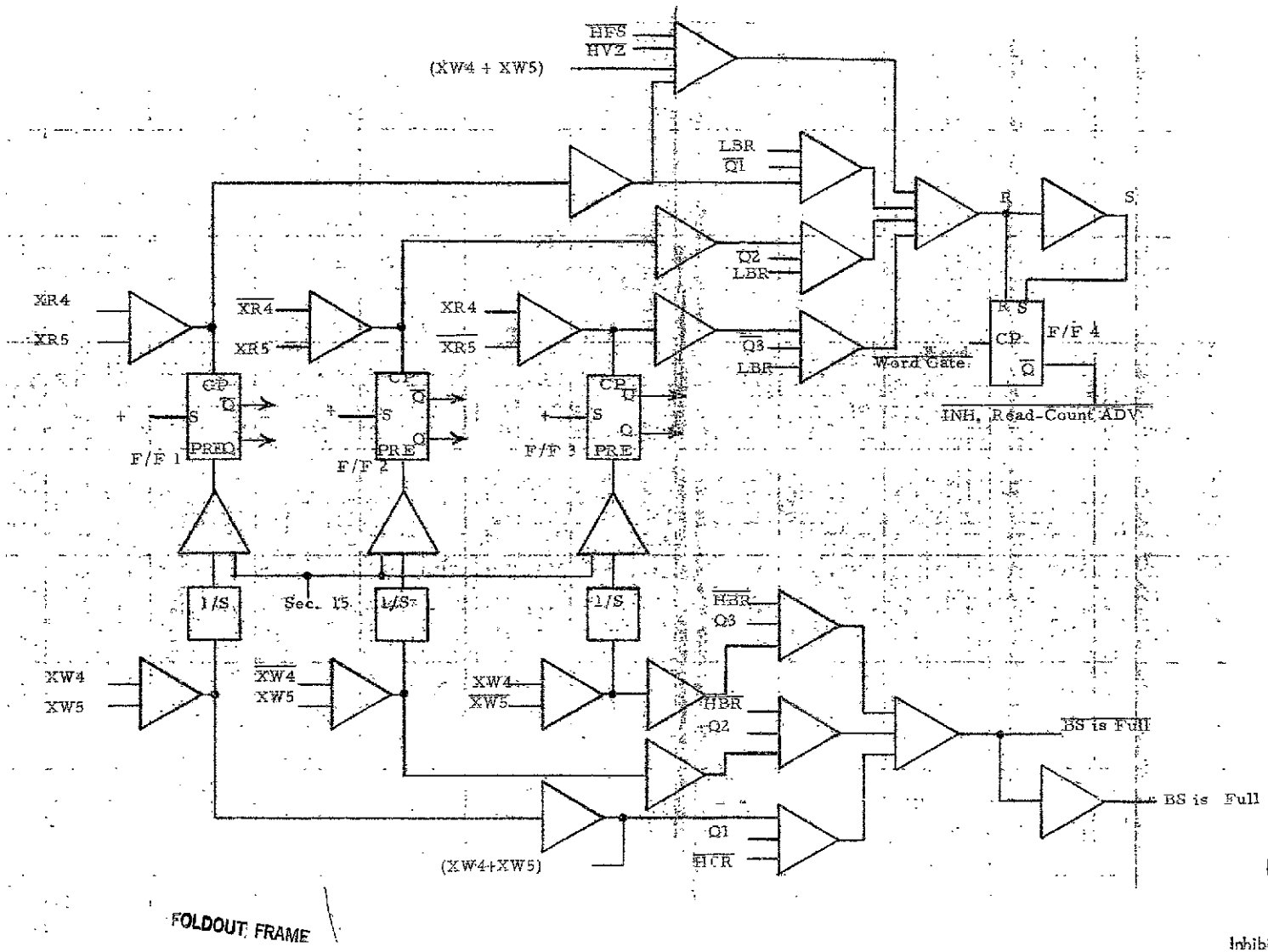
Refer to the Timing diagram. After the first section of the memory has been written into, XW4 is True and resets Flip-Flop 1. After writing into the second section, Flip-Flop 2 is reset, and after writing into the third section, Flip-Flop 3 is reset.

Therefore:

$$\overline{\text{BS is F}} = (XW4 + XW5 + Q1 + \overline{HBR}) + (\overline{XW4} + XW5 + Q2 + \overline{HBR}) + (XW4 + \overline{XW5} + Q3 + \overline{HBR})$$

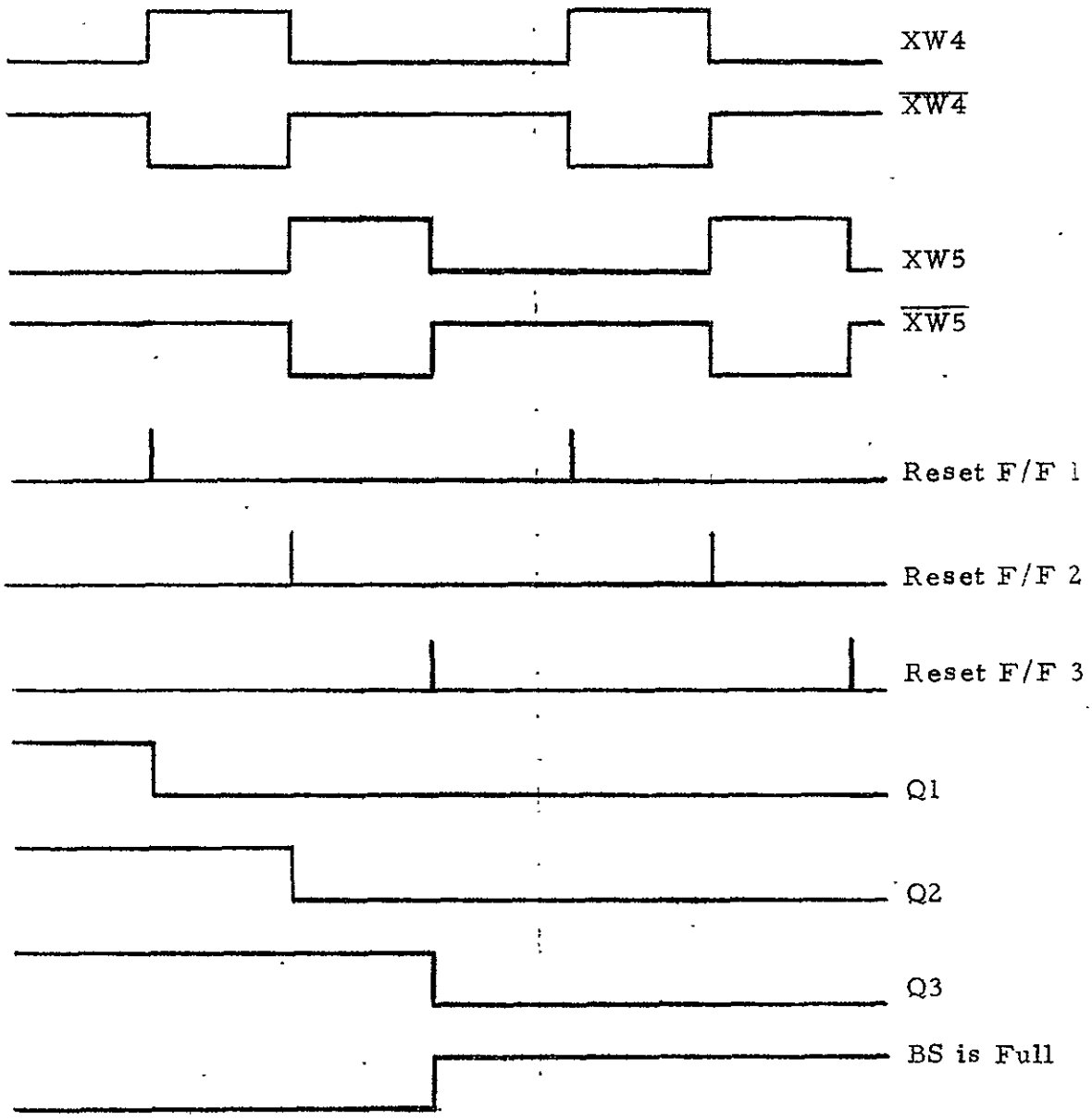
$$\text{BS is F} = (\overline{XW4} \cdot \overline{XW5} \cdot \overline{Q1} \cdot HBR) + (XW4 \cdot \overline{XW5} \cdot \overline{Q2} \cdot HBR) + (\overline{XW4} \cdot XW5 \cdot \overline{Q3} \cdot HBR)$$

It is seen then, that after the flip-flops have been reset, no matter which section of the memory is addressed by the Write Counter, BS is Full will be True and Writing will be inhibited.



Inhibit Read/Write Logic Diagram

Figure 3.3.7-1



BS is Full Timing Diagram
Figure 3.3.7-2

After the first section of the memory has been read out, the transition of XR4 will set Flip-Flop 1. Now when the Write Counter addresses the first section, BS is Full will be False.

When the second section has been read out, Flip-Flop 2 will be set; when the Write Counter addresses this section, BS is Full will be False.

The operation of section three and Flip-Flop 3 is similar.

As is seen from above equation, BS is Full remains False at LBR operation.

The Inhibit Read Function

This function is derived in a manner similar to the derivation of BS is Full. If any memory section has been read out but not subsequently written into, then when the Read Counter addresses that section, the Word gate sets Flip-Flop 4 and the Read Counter Adv is inhibited. When that section is written into, the next Word gate resets Flip-Flop 4 and the Adv Read Counter is enabled.

$$R = (XR4 + XR5 + \overline{Q1} + LBR) + (\overline{XR4} + XR5 + \overline{Q2} + LBR) + (XR4 + XR5 + \overline{Q3} + LBR) + (XW4 + XW5 + XR4 + XR5 + \overline{MFS} + \overline{HVZ})$$

$$S = \overline{R}$$

$$S = (\overline{XR4} \cdot \overline{XR5} \cdot Q1 \cdot \overline{LBR}) + (XR4 \cdot \overline{XR5} \cdot Q2 \cdot \overline{LBR}) + (XR4 \cdot XR5 \cdot Q3 \cdot \overline{LBR}) + (\overline{XW4} \cdot \overline{XW5} \cdot \overline{XR4} \cdot \overline{XR5} \cdot MFS \cdot HVZ)$$

This function also operates at HBR except as shown by the fourth term above.

During HVZ while in MFS and when Read and Write Counters are addressing the first Memory section, the Word Gate will set Flip-Flop 4.

3.3.8 BS is Empty

Figure 3.3.8-1 and 3.3.8-2 show the Logic and Timing diagrams for BS is Empty Reset Counters.

Refer to Section 3.3 (Buffer Storage) for the requirements for BS is Empty signal.

When Electron data is read out at 64 BPS, HVP MOD and $\overline{64}$ are both down. The positive transition of $\overline{XR3}$ and XR4 at the end of the 5th frame triggers the one-shot which generates the BS is Empty signal.

When Ion data is read out at 64 BPS, $\overline{\text{HVP MOD}}$ and $\overline{64}$ are both down. The positive transition of $\overline{XR3}$ and $\overline{XR4}$ at the end of the 10th frame generates the BS is Empty signal.

When Electron data is read out at 16 and 8 BPS or DCSM, HVP MOD and 64 are both down. During the 10th frame all the X inputs to Gate 3 are down. At the first Adv Y-Read of the 10th frame, YR1 goes up, generating BS is Empty at the beginning of the 10th frame.

When Ion data is read out at 16 and 8 BPS or DCSM, $\overline{\text{HVP MOD}}$ and 64 are both down. During the 15th frame all the X inputs to Gate 4 are down. At the first Adv Y-Read of the 15th frame, YR1 goes up, generating BS is Empty at the beginning of the 15th frame.

During HBR operation, Gate 5 disables the output of the one-shot and holds BS is Empty in the True State.

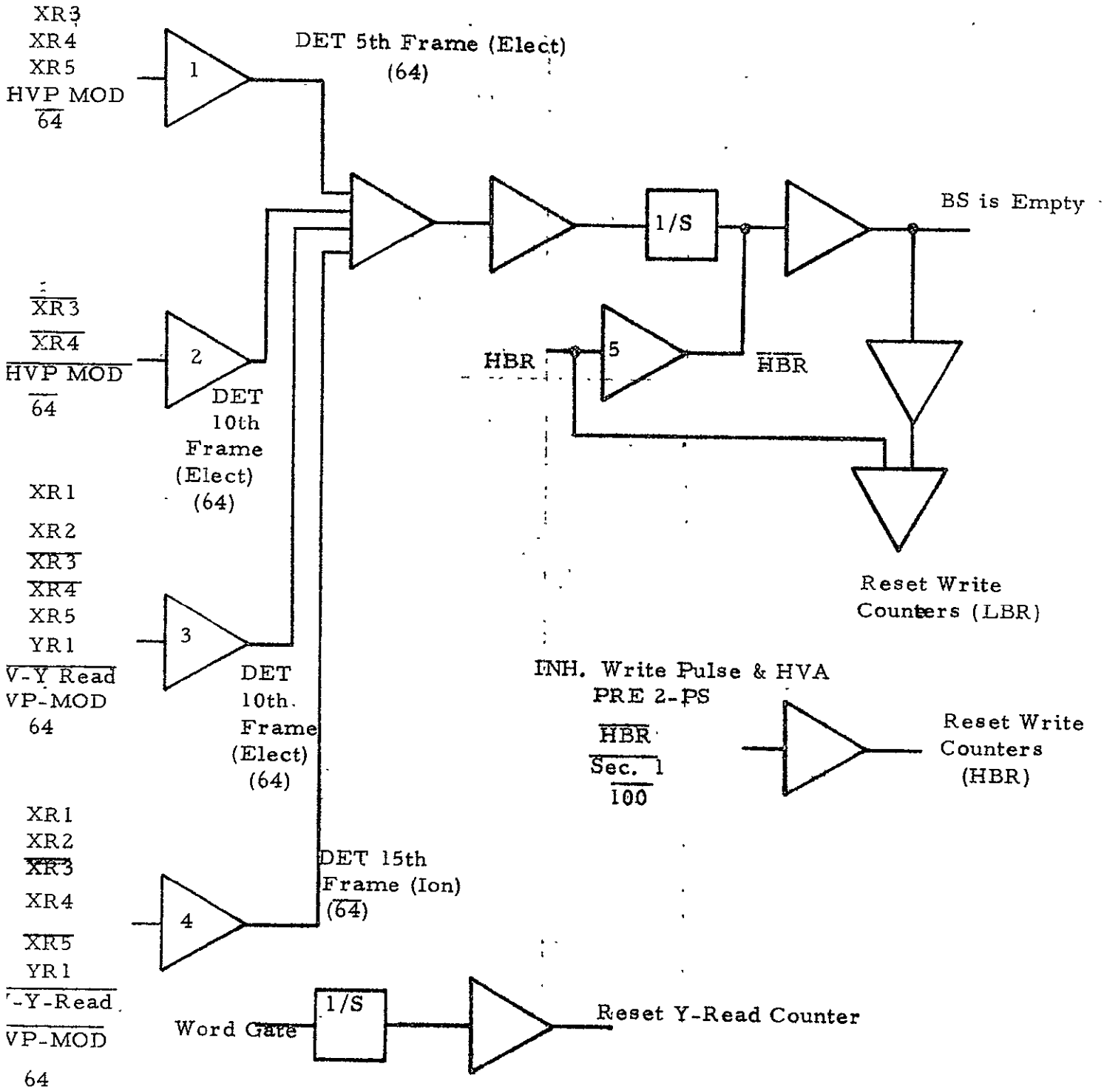
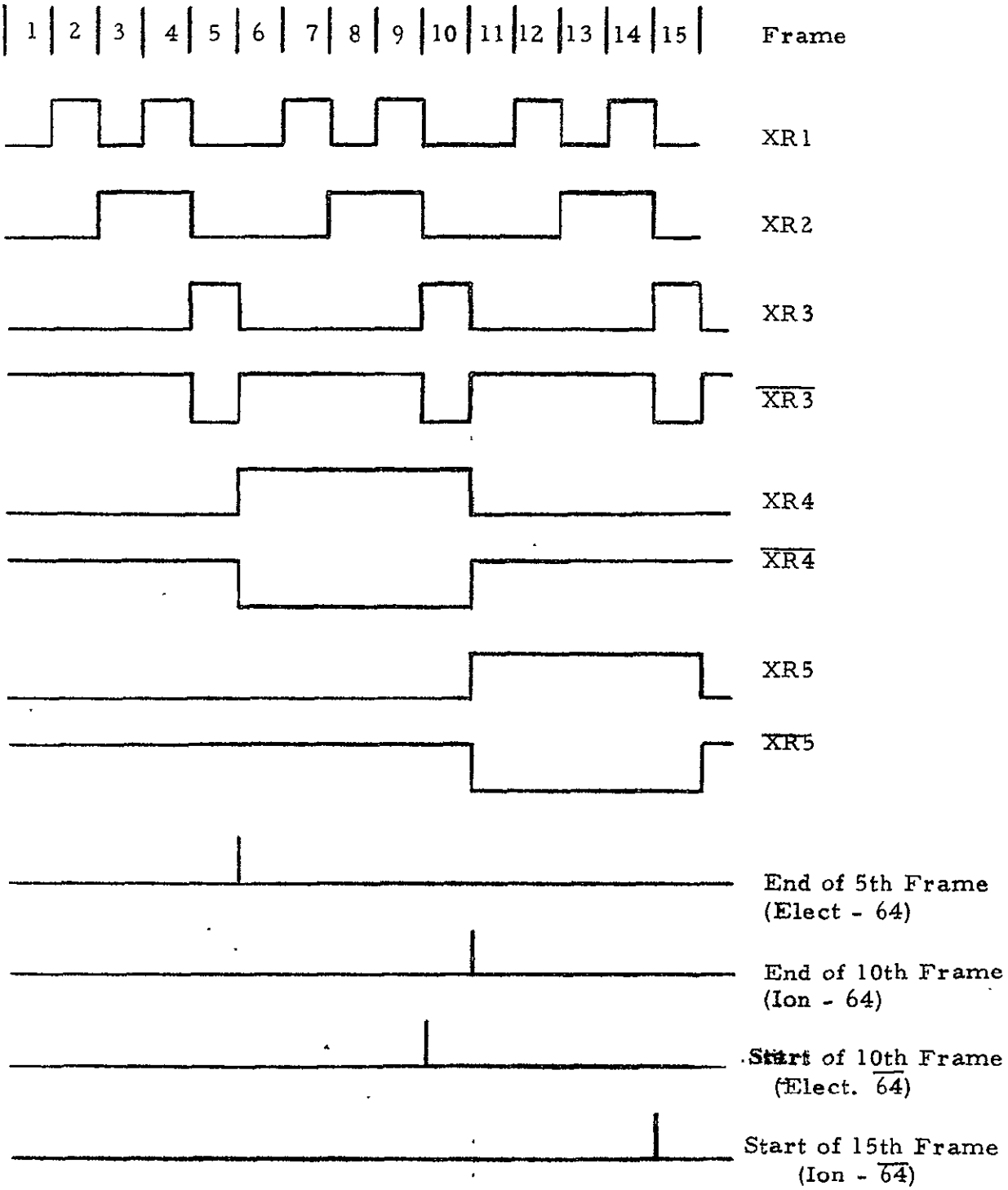


Figure 3.3.8-1
BS Is Empty Reset Counters Logic Diagram
Figure 3.3.8-1



PTY

BS is Empty Timing Diagram
Figure 3.3.8-2

At LBR the BS is Empty pulse is also used to reset the X and Y Write counters.

At HBR, when Polar Scan starts, the 100th pulse of sector 1 resets the Y-Write counter and the 3 stage section of the X-Write counter.

The fall of the $\overline{\text{Word Gate}}$ voltage triggers a one-shot which resets the Y-Read counter.

3.4 High Voltage Power Supply

3.4.1 Inputs and Outputs

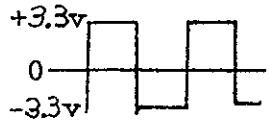
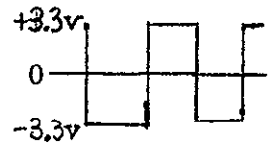
Table 3.4.1A shows a tabulation of inputs to the High Voltage Power Supply. Table 3.4.1B shows a tabulation of the outputs from the High Voltage Power Supply.

3.4.2 Operation

Figure 3.4.2-1 shows a block diagram of the High Voltage Power Supply HVPS. The HVPS consists of two roll-off networks, two d-c feedback amplifiers, two slewing capacitors, two choppers, two transformers, a doublerchain, dump circuitry, an auxiliary power supply, high voltage zero step supply, two full wave rectifiers, and two coupling circuits.

The power supply has two sections: the Ion section and the Electron section.

The High Voltage Power Supply generates the balanced stepping high-voltage for the analyzer plates in the optics section. It also provides all suppression and related voltages. The system consists of two sets of D-C feedback amplifiers (Ion and Electron), choppers, and output transformers which feed the doubler and dump section.

Name	Voltage and Waveform	Impedance or Loading	Source
ION Ramp	30 staircase log. steps 42mv —— 3.0v	500K A-C 7300M D-C	ION Ramp Gen.
Electron Ramp	15 staircase log. steps 0 —— 3.0v	500K A-C 7300M D-C	Electron Ramp Gen.
HVP	Ic Level  +2.5v 0v	43K D-C	HVP
HVZ	Ic Level  +2.5v 0v	43K D-C	Timing and Control
3.3 VAC	SQ. Wave 5KC  +3.3v 0 -3.3v	4K D-C	LVPS
3.3 VAC	SQ. Wave 5KC  +3.3v 0 -3.3v	4K D-C	LVPS
+3v	+3VDC ± 2%	1MA D-C	LVPS
+6v	+6VDC ± .1%	.35MA D-C	LVPS
-6v	-6VDC ± .1%	2MA D-C	LVPS
+12v	+12VDC ± .1%	5.5MA D-C 60 MA Peak	LVPS
+15v	+15VDC ± .1%	1.1 MA D-C	LVPS

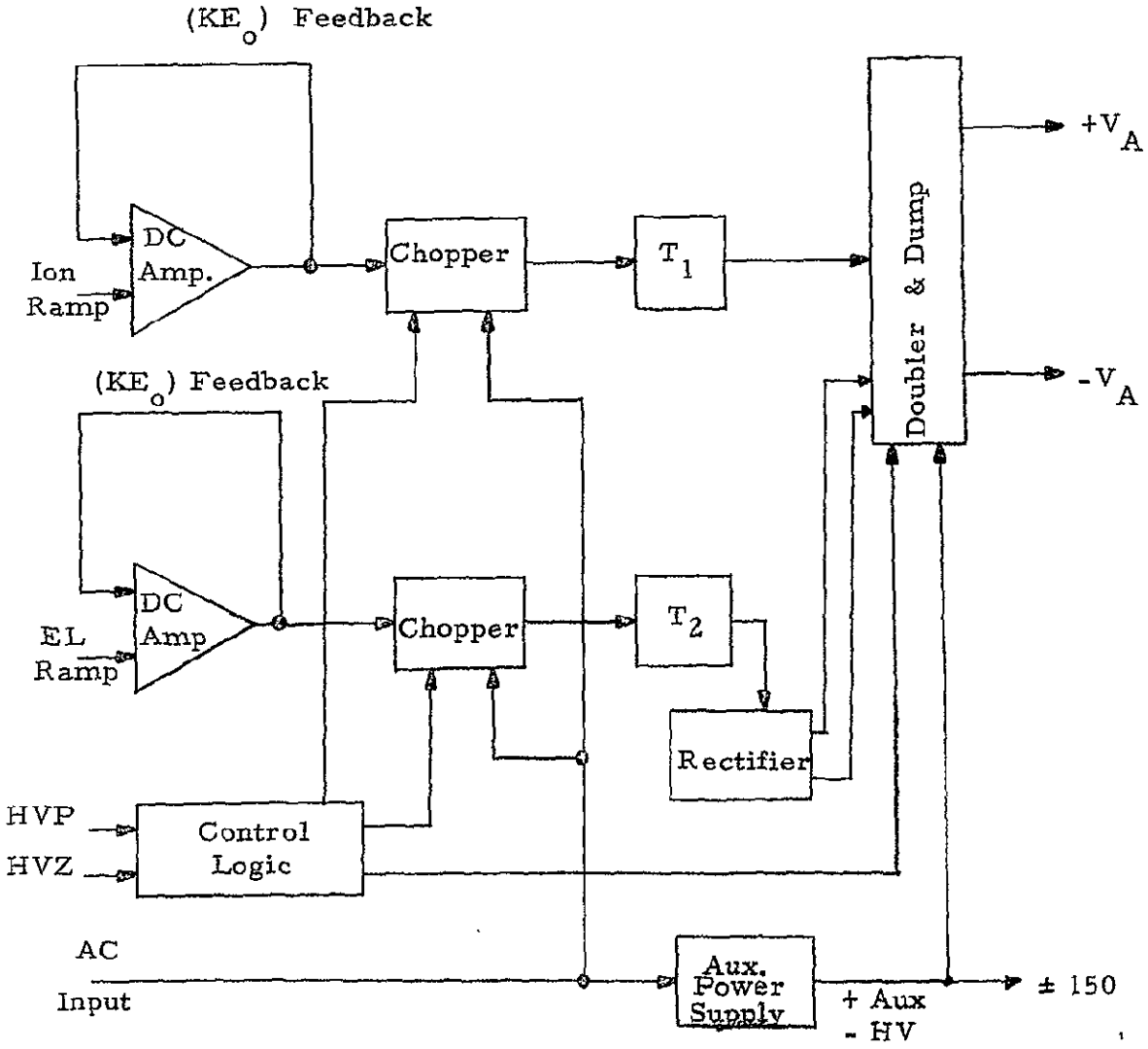
High Voltage Power Supply Inputs

Table 3.4.1A

Name	Voltage and Waveform	Impedance	Destination
+VA	15 Electron Staircase log steps from +0.05 to -83.3 volts 30 ION staircase log steps from +17.5 volts to +1250 volts.	20 Meg D-C	Outer analyzer plates
-VA	15 Electron Staircase log steps from -0.05 volts to +83.3 volts. 30 Ion staircase log steps from -17.5 volts to -1250 volts.	20 Meg D-C	Inner analyzer plates
+150	+150 VDC		Supp. Voltage Gen.
-150	-150 VDC		Supp. Voltage Gen.
ION HV Analog	30 Staircase log steps -42mv to -3.0v		HV A/D
Electron HV Analog	15 Staircase log steps 0 to -3.0v		HV A/D

High Voltage Power Supply Outputs

Table 3.4.1B



High Voltage Power Supply Block Diagram
Figure 3.4.2-1

The control logic section switches the proper section into operation (i.e. Ion or Electron). An A-C voltage from the Low Voltage Power Supply drives the chopper and the auxiliary power supply.

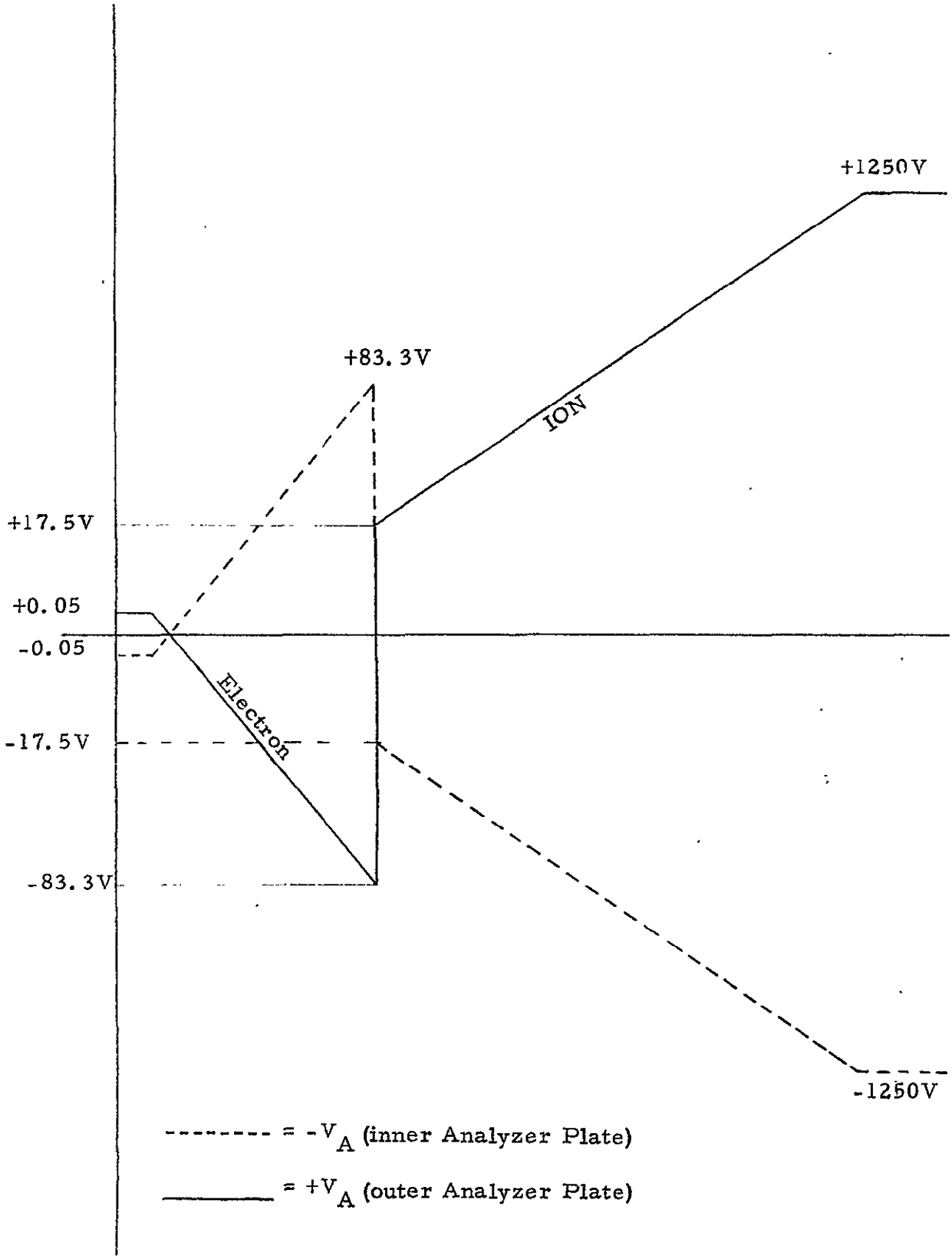
The signals preset at the inputs of the D-C feedback amplifiers (Ion and Electron) are both generated by the Ion and Electron Ramp Generators. These signals are amplified and fed to the choppers which, according to their frequency of operation, transform the output of the D-C amplifier into a square wave that is fed into the transformer and then to the doubler and dump section (Ion Mode only).

The output from the Electron Section is rectified by a full wave bridge and appears as ±83.3V. Since the instrument is sequenced through seven Ion Cycles and one Electron Cycle, the HV power supply is subject to the same sequence which is achieved by the control logic circuit in accordance with the $\overline{HVP}$ and $\overline{HVZ}$ signals.

See Figure 3.4.2-2, Analyzer Plate Voltages/Ion-Electron Mode.

When $\overline{HVP}$ and $\overline{HVZ}$ are high, the control logic circuit is activated in such a manner that the Ion chopper only is energized while the Electron chopper is inactive. The output from the Ion chopper is fed into the Ion transformer, beyond which the doubling action starts. This process continues until one cyle (30 steps) is achieved.

At the end of the 30th step, the highest output from the power supply is realized. Then $\overline{HVZ}$ changes polarity. This enables the control logic circuit to activate the dump circuit which then shorts the output of the doubler to ground through a series of transistors that turn on in an orderly sequence. This is the end of one Ion Cycle.



Analyzer Plate Voltages/Ion-Electron Mode
Figure 3.4.2-2

The process repeats for seven such cycles, at the end of which $\overline{HVP}$ changes polarity, which in turn allows the control logic circuit to energize the Electron chopper while the Ion chopper becomes inactive. The power supply goes into the Electron mode, and generates a plate voltage of +0.050 volts to ±83.3 volts increasing from minimum to maximum in fifteen steps. At the end of the fifteenth step $\overline{HVP}$ changes polarity again and the Ion cycle begins.

3.4.2.1 Slewing Capacitor

The Slewing Capacitor is used to supply peak currents demanded by the voltage doubler and chopper circuitry.

3.4.2.2 Chopper

The chopper converts the d-c amplifier output into an a-c signal. The output of the chopper is a 5KHz square wave. The chopper can be cut off by $\overline{HVP}$ and $\overline{HVZ}$.

The output of the chopper is fed to a step-up transformer.

3.4.2.3 Doubler Gate and Doubler Chain

The positive Doubler Gate and negative Doubler Gate are turned on during Ion mode. During Electron mode, or during a dump mode, the gates are OFF. These gates are turned off in order to allow the reversal of voltage at the inputs to the VA couplers.

The output of the transformer is fed to the doubler chain. The doubler chain consists of two sections: The positive section and the negative section. Each section consists of 8 doublers. The positive doublers charge up to the peak value of the positive transition of the transformer and the negative doublers charge up to the peak value of the negative transition of the transformer. Each doubler charges up to two times the input voltage.

Each doubler charges up to a maximum voltage of 158 volts. The output of the 8th doubler is 1,250 volts maximum. Minimum voltage is 17.5 volts.

3.4.2.4 Dump Circuitry

The doubler chain is discharged by the Dump Circuitry. The operation of the Dump circuit is as follows: On receipt of a signal from HVP' or HVZ', the Dump gate turns on the trickle dump circuit. A delay is provided such that the Dump and Reversal circuitry does not turn on. The trickle dump circuit will cause a slow exponential discharge of the doublers. Dump switch 8 will discharge doubler number 8. After doubler number 8 is discharged, dump switch 7 will cause doubler number 7 to discharge. This action is repeated until doubler number 1 is discharged. Approximately 250 milliseconds after the dump gate has turned on, the Dump and Reversal circuits will cause speed up of dumping, a -150 volts to appear at the input to the +VA coupler, and +150 volts to appear at the input to the -VA coupler.

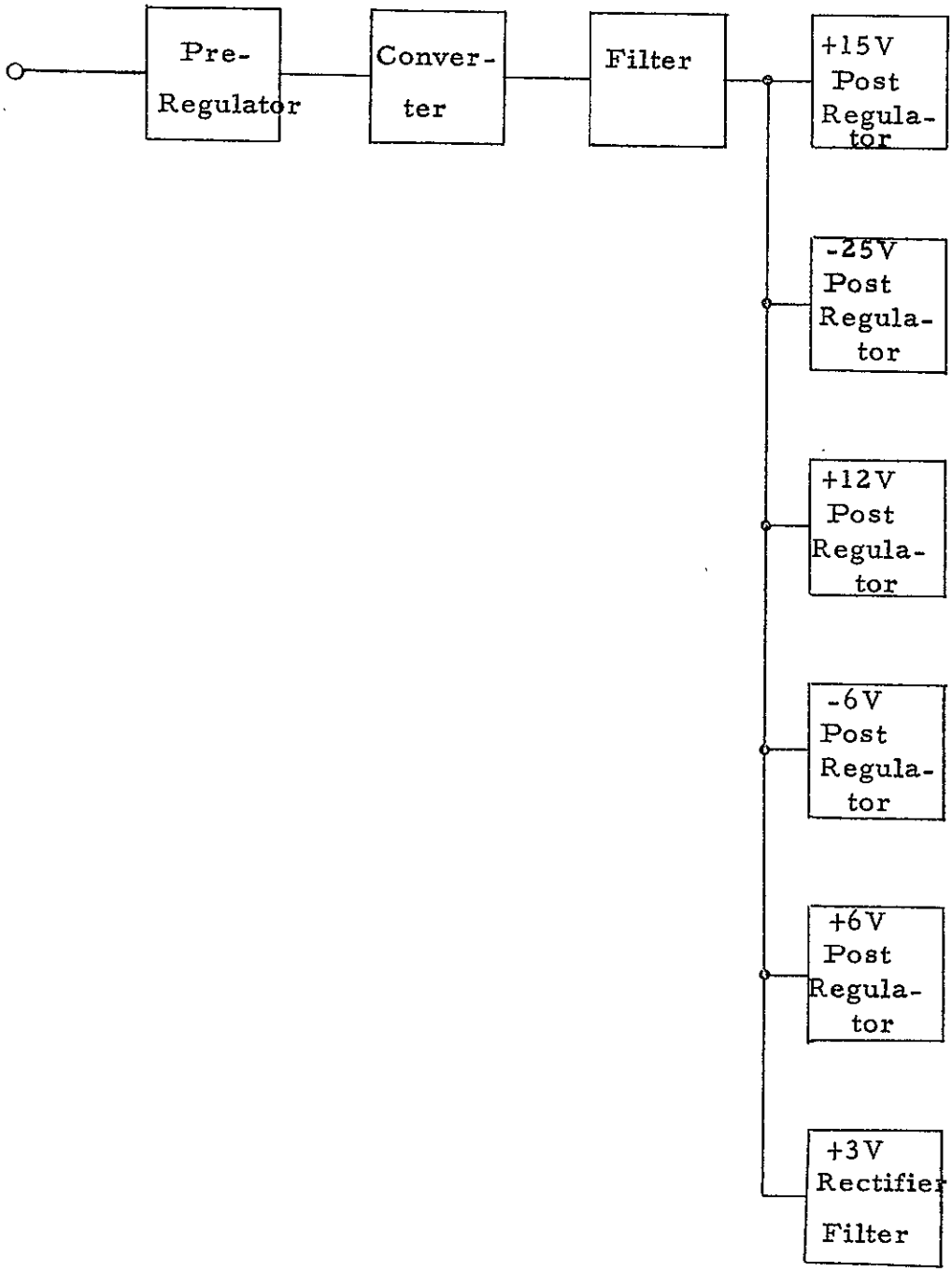
3.4.2.5 Control Logic

The HVP interface converts the low level HVP signal into high level HVP' and $\overline{\text{HVP}}$' signals. The HVZ interface converts the low level $\overline{\text{HVZ}}$ signal into high level HVZ' and $\overline{\text{HVZ}}$' signals.

3.5 Low Voltage Power Supply

Refer to Figure 3.5-1 for the Low Voltage Power Supply Block diagram.

The Low Voltage Power Supply converts the spacecraft +28 volts into the required instrument voltages. The +28 volt supply from the spacecraft is passed through a pre-regulator circuit which converts this voltage into a constant regulated +23.5 volts.



Low Voltage Power Supply Block Diagram
Figure 3.5-1

This voltage is then converted by the chopper circuit into a 5 KHz square wave which is stepped up by a transformer, rectified and regulated by various post-regulators to provide the required voltages.

3.5.1 Pre-Regulator

The Power Supply Pre-regulator consists of a series voltage regulator that provides a stable operating voltage to the chopper to insure reliable operation. Operation of the Pre-regulator is discussed in Section 4.14.1.

3.5.2 Chopper

The function of the Chopper is to convert the +23.5V dc output of the pre-regulator into a 5KHz square wave.

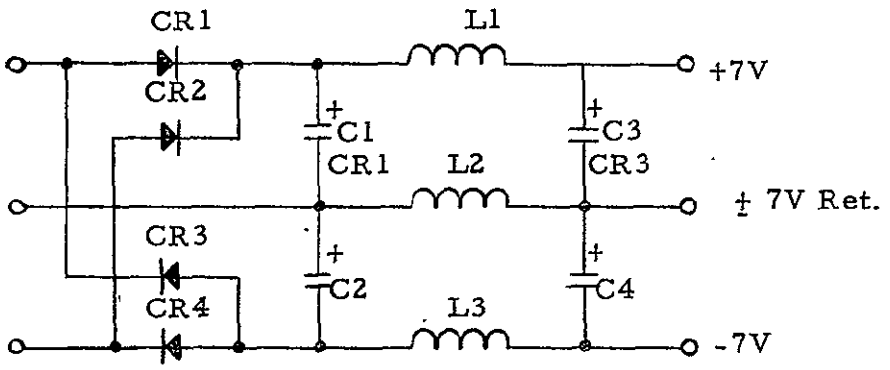
Operation of the Chopper is discussed in Section 4.14.2.

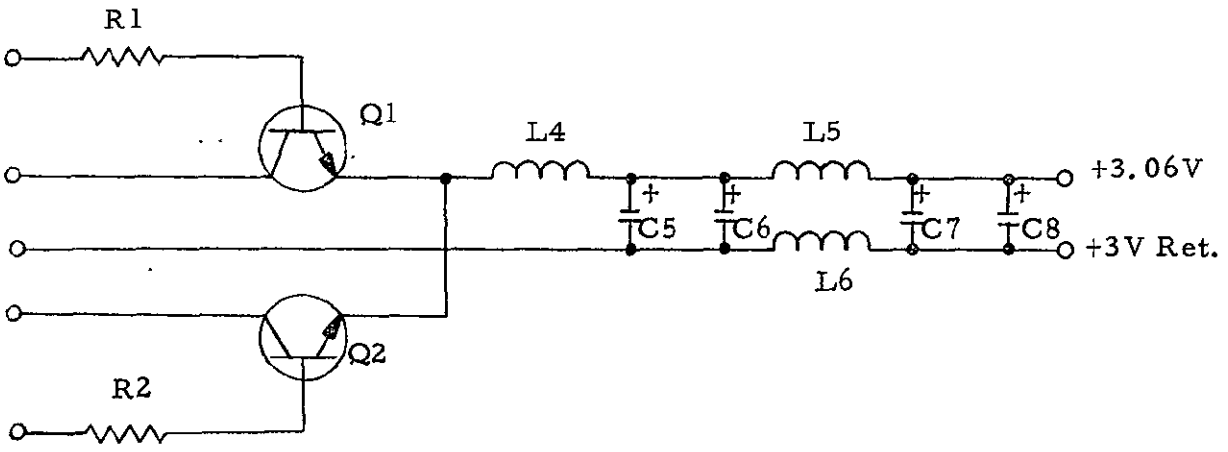
3.5.3 Rectifier Filter

The stepped potential from the transformer is rectified, resulting in a ripple content of less than 5 millivolts. The rectification is produced by means of full wave or half-wave standard rectification circuits. The ripple output is reduced to a minimum by means of π-filters composed of capacitors and chokes. Figure 3.5.3-1 shows two typical rectifier filter configurations. The use of a π-section filter provides an output potential that approaches the peak value of the a-c potential of the source, the ripple components being very small.

3.5.4 Post-Regulator

The Post-regulators each consist of a series voltage regulator that provides a stable operating voltage to the various circuits of the instrument. The Post-regulators are similar to the pre-regulator (Section 3.5.1)aand operate on the same principle.





Typical Rectifier Filter Configurations
Figure 3.5.3-1

3.5.5 Filament Power Supply

The Filament Power Supply provides the correct filament voltage for the operation of the Electrometer tubes. The filament supply uses a synchronous rectifier circuit for greater efficiency and lower power. The input to the supply is the 3.3 vac generated by the Low Voltage Power Supply.

4.0 CIRCUIT DESCRIPTIONS

This section contains detailed descriptions of electrical circuit operation. Design analysis and specifications are included where appropriate. Selected worst-case analyses are found in Appendix E.

4.1 Electrometer Amplifier

4.1.1 Stabilization Buffer

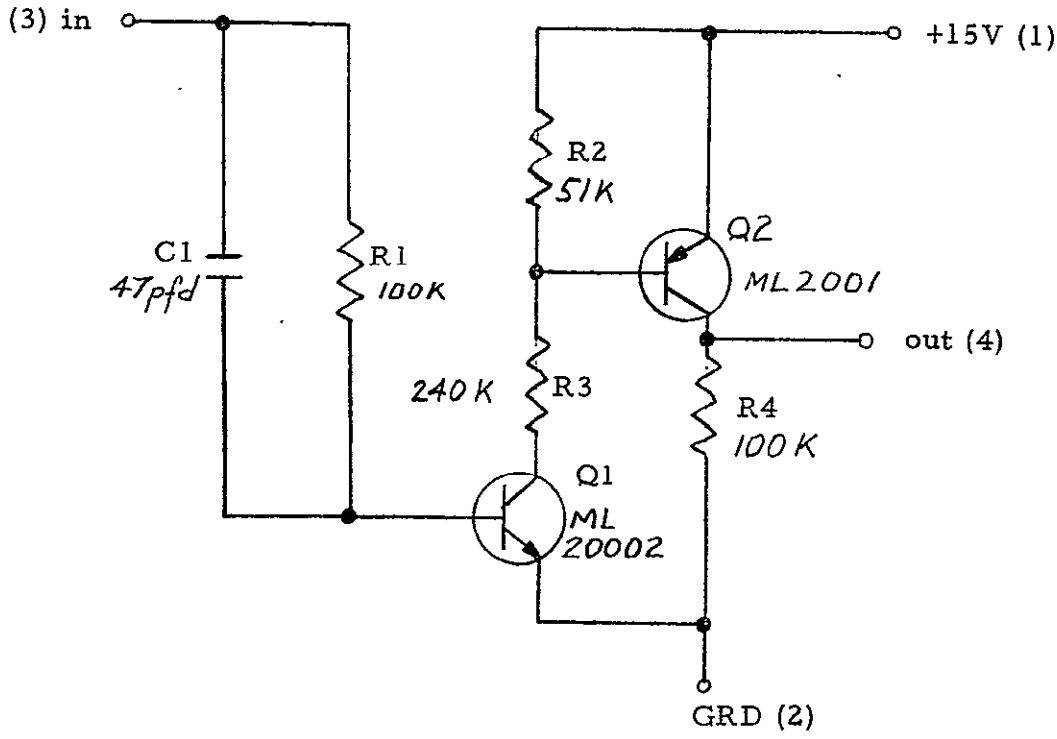
See Figure 4.1.1-1 for the schematic diagram. The Stabilization Buffer is a switching circuit which activates the Stabilization Amplifier and the stabilization storage circuits. The operation of the circuit is initiated by the application of the $\overline{\text{Stab}}$ signal (see Section 3.2.6, High Voltage Zero and Stabilization Control). When Q1 is OFF, its collector is at about +15v.

This is applied to the base of Q2, thereby keeping Q2 OFF and holding the output to 0.01 volts or less.

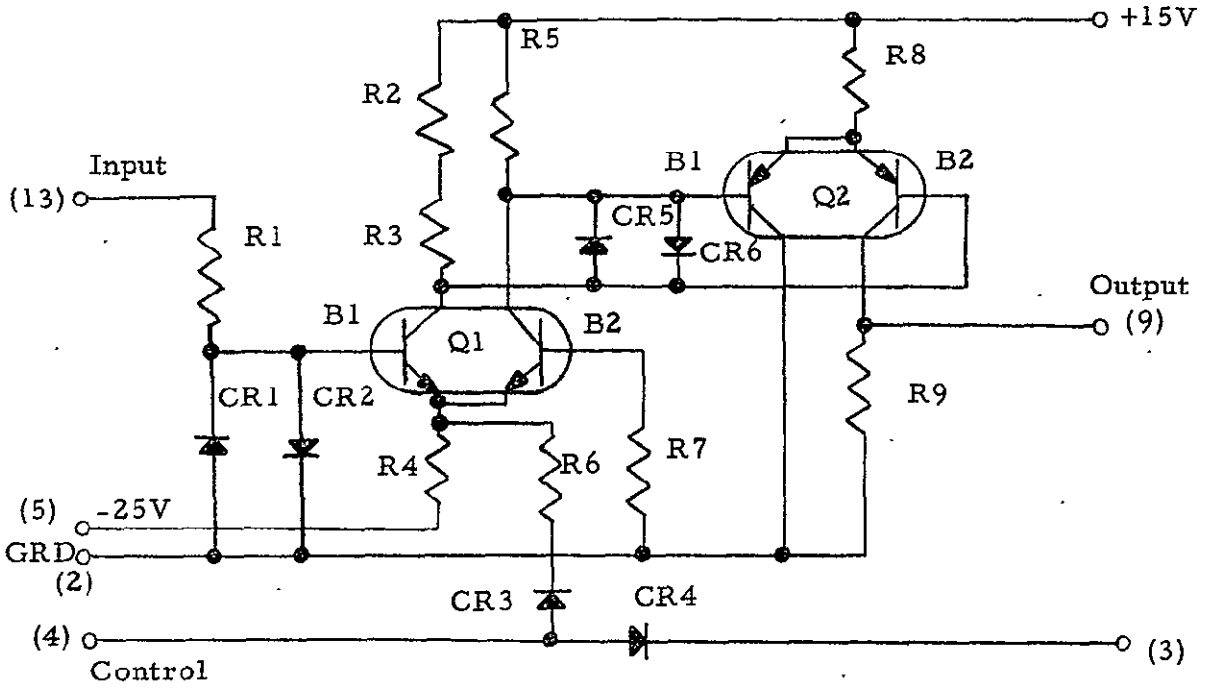
Upon application of signal, Q1 turns ON causing a drop across R2. The emitter of Q2 goes positive with respect to the base, turning Q2 ON. Thus the output is driven to +15 volts.

4.1.2 Stabilization Amplifier

Figure 4.1.2-1 shows the schematic diagram of the Stabilization Amplifier.



Stabilization Buffer Schematic
Figure 4.1.1-1



Q_1 = 2N4042 Transistor

Q_2 = 2N4024 "

CR1 = CR2 = CR3 = CR4 = CR5 = CR6 = SP30265 Diode

$R_1 = R_7 = R_9$ = 100K ± 5% Resistor

R_2 = Select "

R_3 = Select "

R_4 = 1.2M ± 5% "

R_5 = 604K ± 1% Resistor

R_6 = 390K ± 5% "

R_8 = 51K ± 5% "

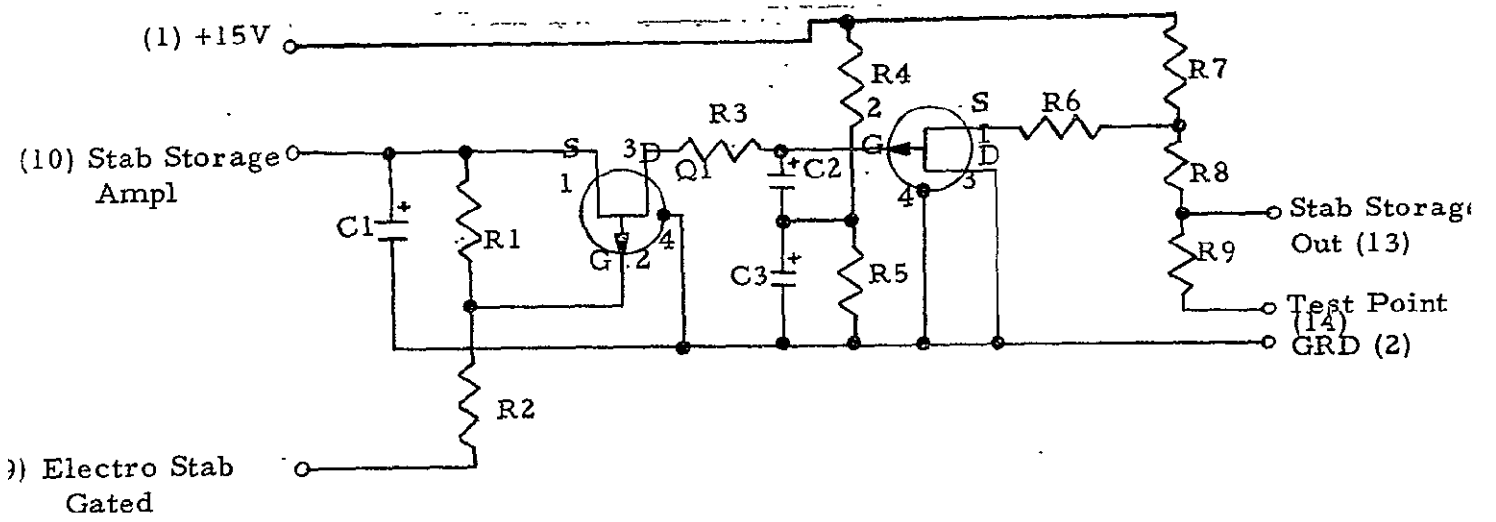
Stabilization Amplifier Schematic
Figure 4.1.2-1

The Stabilization Amplifier senses the offset error from the output of the Electrometer, amplifies the error and drives the Stabilization storage circuit. The Stabilization Amplifier is essentially a two stage differential amplifier with the first stage controlled by the Stabilization Buffer circuit. The output of the Stabilization Buffer circuit is coupled to R_6 via CR3. When this signal is +15 volts, the Differential Amplifier Q_1 is cut OFF. This is due to the positive voltage applied to the emitter of Q_1. When the output from the Stabilization Buffer circuit is 0±0.1v, the Differential Amplifier senses the error signal between base 1 and 2 and amplifies it. The output of the second stage Q_2 is calibrated by means of select resistor R2 to be +5 volts. CR3 and CR4 clamp the input signal to 0.6 volts, limiting the signal swing at the input.

4.1.3 Stabilization Storage

See Figure 4.1.3.-1 for the schematic diagram.

The Stabilization Storage is an FET switching circuit controlled by the Stabilization Buffer and establishes the required voltage on the screen grid of the Electrometer tube. With the output of the Stabilization Buffer applied to the voltage divider network R_1, R_2, a positive voltage is applied to the gate of Q_1, a P channel FET, holding Q_1 OFF. Capacitor C_3 is charged to a positive voltage through the divider network R_4, R_5. With no output from the Stabilization Buffer, Q_1 turns ON and charges C_2. The total potential across C_2 and C_3 is applied to the gate of Q_2, effecting its bias and varying the current flow through the divider network R_7, R_8 and R_9 and applying the potential developed across R_9 to the screen grid of the Electrometer tube.



$Q_1 = Q_2$ = ML20014 Select Transistors

R_1 = 100K ± 5% Resistor

R_2 = 82K ± 5% Resistor

R_3 = 10M ± 5% Resistor

$R_4 = R_9$ = 200K ± 5% Resistor

R_5 = 73.2K ± 1% Resistor

R_6 = 243K ± 1% Resistor

R_7 = 84.5K ± 1% Resistor

R_8 = 90.9K ± 1% Resistor

C_1 = 1uf Capacitor

C_2 = 0.8 ufd Select Capacitor

C_3 = 2.2 ufd Capacitor

Stabilization Storage Schematic
Figure 4.1.3-1

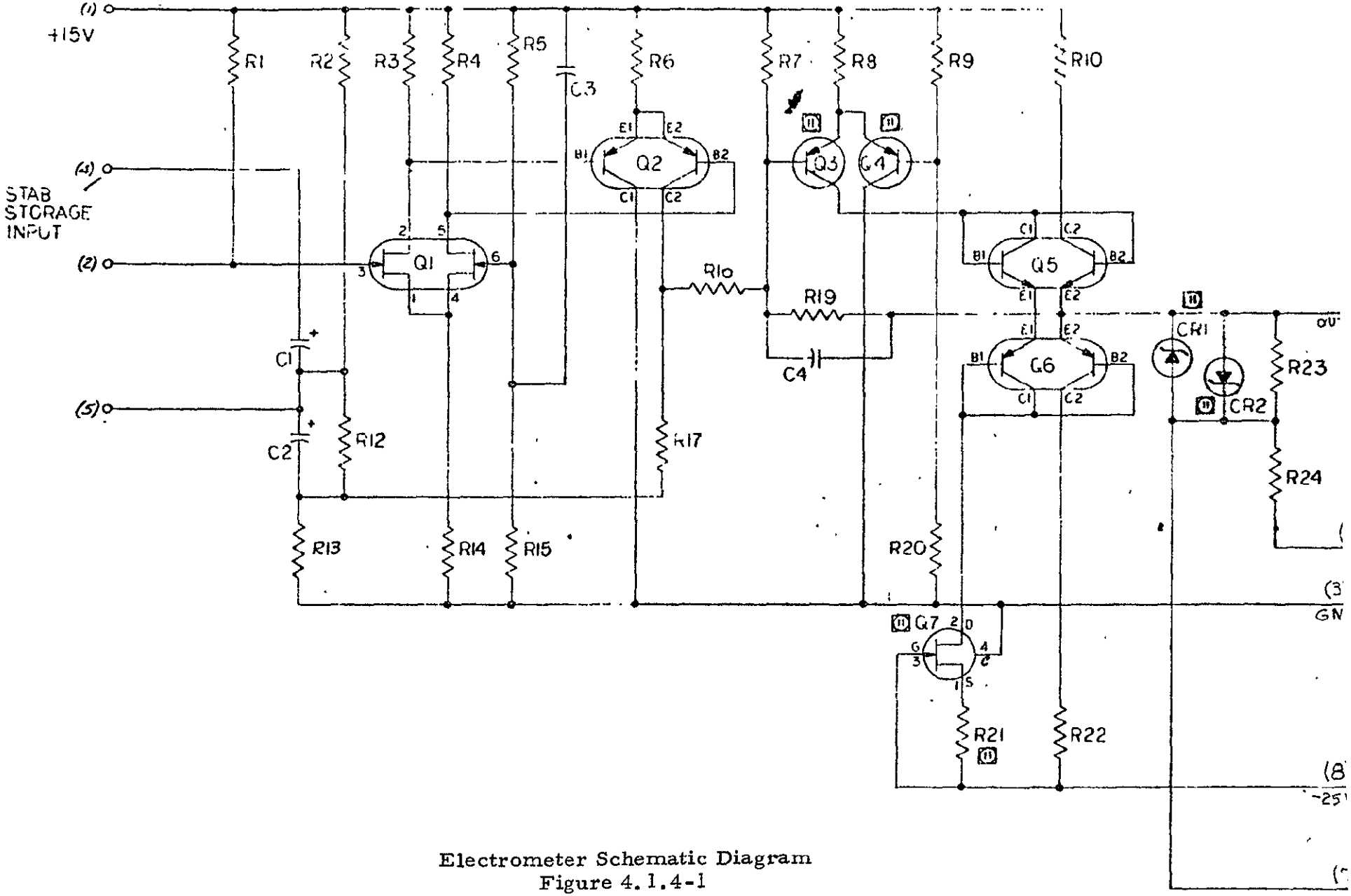
4.1.4 Electrometer

The Electrometer is a high input impedance two-stage differential amplifier that senses and amplifies the signal input on the control grid of the Electrometer tube. Figure 4.1.4-1 shows the schematic diagram.

The input stage, Q_1, is a dual FET transistor used as a differential amplifier. The gate of Q_{1B} is held at +10 volts by means of the divider network R_5, R_{15}. Q_{1A} is the load for the Electrometer tube. The gate of Q_{1A} is biased at +10 volts. Current variations in the plate of the tube are sensed by Q_1, and the difference is amplified by Q_2. Q_3 and Q_4 are selected for matched characteristics and together operate as a differential amplifier. The base of Q_4 is held at +10V by means of the divider network R_9, R_{20}. Q_3 senses the output from Q_2 and drives the emitter followers Q_5 and Q_6. Q_{5A} and Q_{6A} are used as diodes enabling separate operation of Q_{5B} and Q_{6B}. Q_7 is a Field Effect Transistor and acts as a constant current source. R_{19} and C_4 prevent high frequency oscillations that are inherent in high gain amplifiers.

With a negative input to the control grid of the Electrometer tube, the base of Q_{2A} goes negative, driving Q_3 harder and Q_4 towards cut-off. This results in a positive output. The presence of a positive signal on the control grid of the Electrometer tube results in a negative output.

R_{23} and R_{24} set the feedback ratio and determine the closed loop gain of the amplifier. CR_1 and CR_2 are select zener diodes that produce compression once the output reaches the breakdown voltage of the zeners. The selection of the value of the feedback resistor R_f is a compromise between a minimum determined by thermal noise and threshold current and a maximum determined by maximum input current and practical output voltage capabilities.



Electrometer Schematic Diagram
Figure 4.1.4-1

The value of the feedback resistor is 1.5×10^{10} ohms yielding an output of

$$E_o = R_f \times I_n + V_z$$

if $I_n = 1 \times 10^{-10}$ amperes

$$E_o = 1.5 \times 10^{10} \times 1 \times 10^{-10} + 6.7$$

$$E_o = 8.2 \text{ volts}$$

and 3.3 millivolts for 1×10^{-14} amperes.

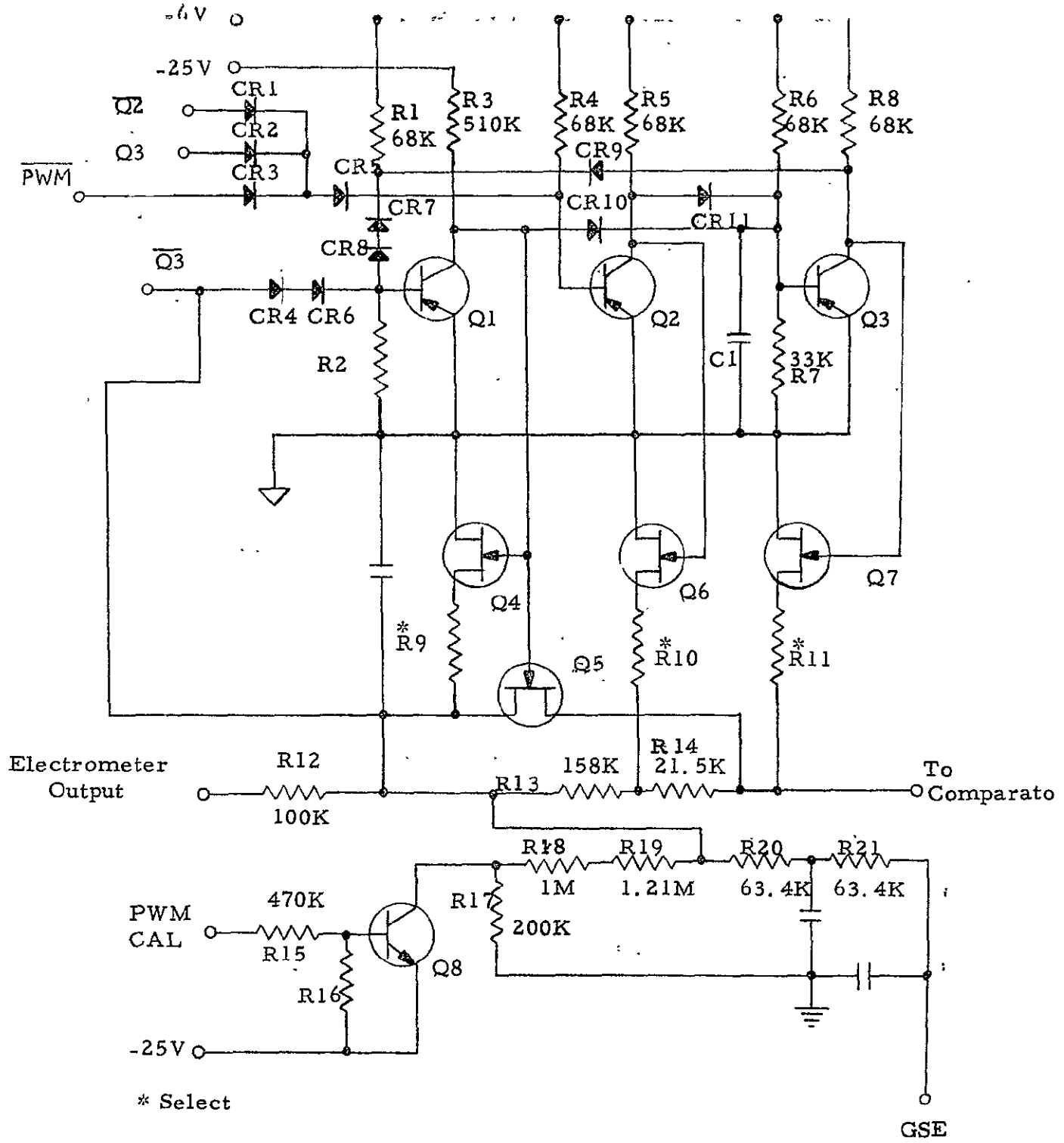
4.1.5 Attenuator Driver and Attenuate and Calibrate
See Figure 4.1.5-1 for the schematic diagram.

The signals Q_1, $\overline{Q}_1$, Q_2, $\overline{Q}_2$, Q_3, $\overline{Q}_3$ are generated by the PWM programmer section. $\overline{Q}_2$, Q_3 and $\overline{Q}_3$ control the operation of the attenuator Driver.

The signals $\overline{Q}_2$ and $\overline{PWM}$ applied to CR_1 and CR_3 respectively, keep transistor Q_2 OFF, and the $\overline{Q}_3$ signal applied to CR_4 keeps transistor Q_1 OFF.

With Q_1 OFF, its collector potential is -25V. This drives the base of transistor Q_3 negative and turns Q_3 ON. At this time, Q_3's collector potential is 0.050V, which is applied to the gate of transistor Q_7. This causes Q_7 to turn ON, forming a voltage division between R_{11} and $R_{12} + R_{13} + R_4$. With Electrometer output voltage E1. Out applied to R_{12}, the output to the comparators will be

$$\frac{R_{11}}{R_{11} + R_{12} + R_{13} + R_{14}} \text{ (E1. Out.)}$$



Attenuator Driver and Attenuate and Calibrate
Figure 4.1.5-1

In the next sequence the signal $\bar{Q}_2$ changes state. This allows the base of transistor Q_2 to go negative, turning ON transistor Q_2, which in turn allows transistor Q_6 to turn ON. During this process, CR_{10} is forward biased; current will flow through R_6 and CR_{10}, transistors Q_2, Q_3, and Q_7 will turn OFF.

The output of the circuit is now

$$\frac{R_{10}}{R_{10} + R_{12} + R_{13}} \text{ (El. Out)}$$

Similarly, when $\bar{Q}_3$ changes state, transistors Q_1, Q_4 and Q_5 turn ON while Q_2 and Q_6 turn OFF. The output of the circuit is now

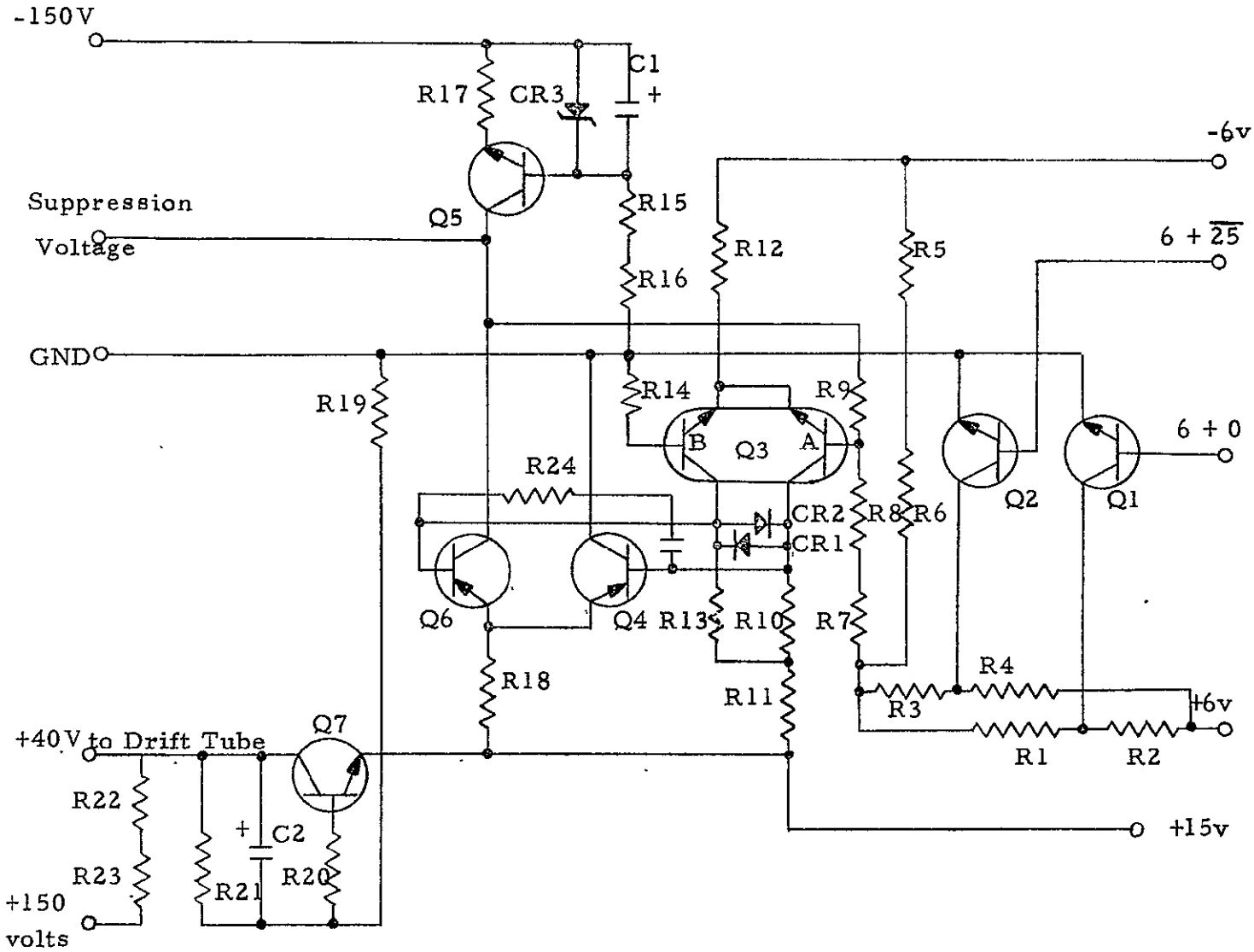
$$\frac{R_9}{R_9 + R_{12} + R_{13} + R_{14}} \text{ (El: Out)}$$

A means for checkout of the operation of remaining circuits in the Pulse Width Modulator section is provided with transistor Q_8 and associated components. This is done by turning ON transistor Q_8 by the PWM calibrate signal. When Q_8 is ON its collector potential is about -25V. This voltage is attenuated through the divider consisting of R_{17}, R_{18} and R_{19}. Thus a negative potential is applied to the comparator circuits, corresponding to half scale digital output (64 bits).

4.1.6 Suppression Circuit

The Suppression Circuit provides all necessary voltages for the Optics section, and a +40 volt supply for the drift tube.

Figure 4.1.6-1 shows the schematic diagram of the Suppression Circuit.



$Q_1 = Q_2$ = ML20005 Transistor
Q_3 = 2N4042 "
Q_4 = ML20001 "
Q_5 = 2N3439 "
Q_6 = 2N3743 "
Q_7 = ML20002 "
CR1 = CR2 = SP30265 Diode
CR3 = ML20027 Diode
R1 = 63.4K ± 1% Resistor
R2 = 44.2K ± 1% Resistor

R3 = R5 = 196K ± 1% Resistor
R4 = R6 = 237K ± 1% "
R7 = 374K ± 1% "
R8 = 1 Meg ± 1% "
R9 = 15 Meg ± 1% "
R10 = R13 = 301K ± 1% "
R11 = 150K ± 5% "
R12 = R18 = 270K ± 5% "
R14 = 1.3 Meg ± 5% "
R15 = R16 = 22 Meg ± 5% "
R17 = 620K ± 5% "
R19 = 1.5 Meg ± 5% "
R20 = 1K ± 5% "
R21 = R23 = 2.4 Meg ± 5% "
R22 = 2.2 Meg ± 5% "
C1 = 6.7 μfd
C2 = 1 μfd

Suppression Circuit Schematic Diagram
Figure 4.1.6-1

Transistors Q_1 and Q_2 act as switches and are activated by the logic signals 6+0 and $6+\overline{25}$ respectively. Depending on the state of Q_1 and Q_2 (ON or OFF), a divider network made of R_9, R_8, R_7, R_6, R_5 applies a potential to the base Q_{3B}. Q_3 is a differential amplifier with the base of Q_{3B} connected to ground through R14. The error signal is amplified by Q_4 and Q_6 operating as a differential amplifier. The output of Q_6 is fed back to the base of Q_{3A} to correct the error signal. Q_5 is a constant current supply source. A positive potential, +150V, applied to R23 provides the +40 volts output for the drift tube. This is done by means of the divider network R23, R22, R21, and R19. Transistor Q_7 acts as the regulator for the +40 volt supply. The table showing the output Suppression Voltage as a function of the logic input signals is repeated here as Table 4.1.6A.

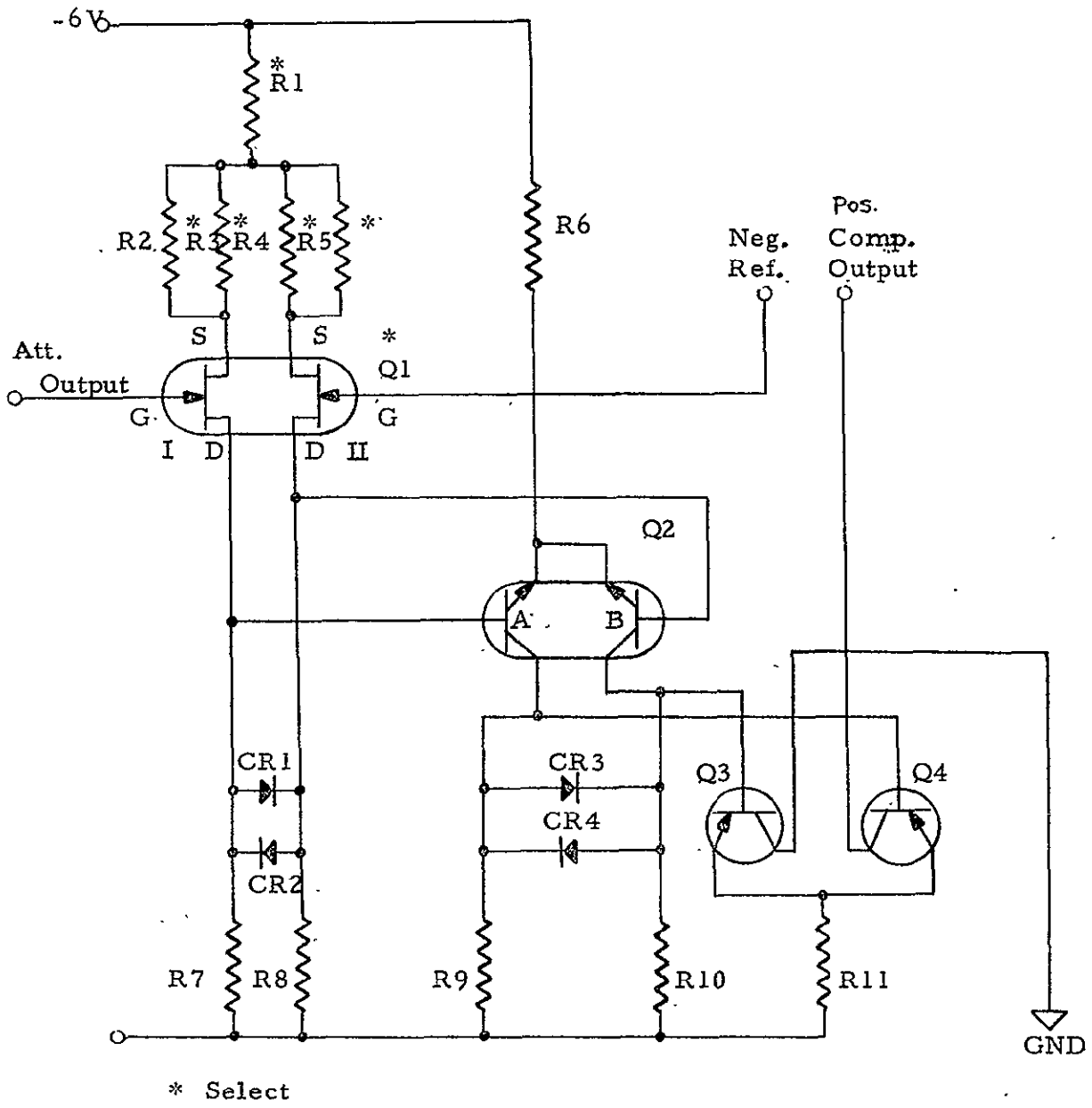
$6+\overline{25}$	6+0	Suppression Voltage
0	0	-40
0	1	0
1	0	-25
1	1	+6

Table 4.1.6A
Suppression Circuit Logic

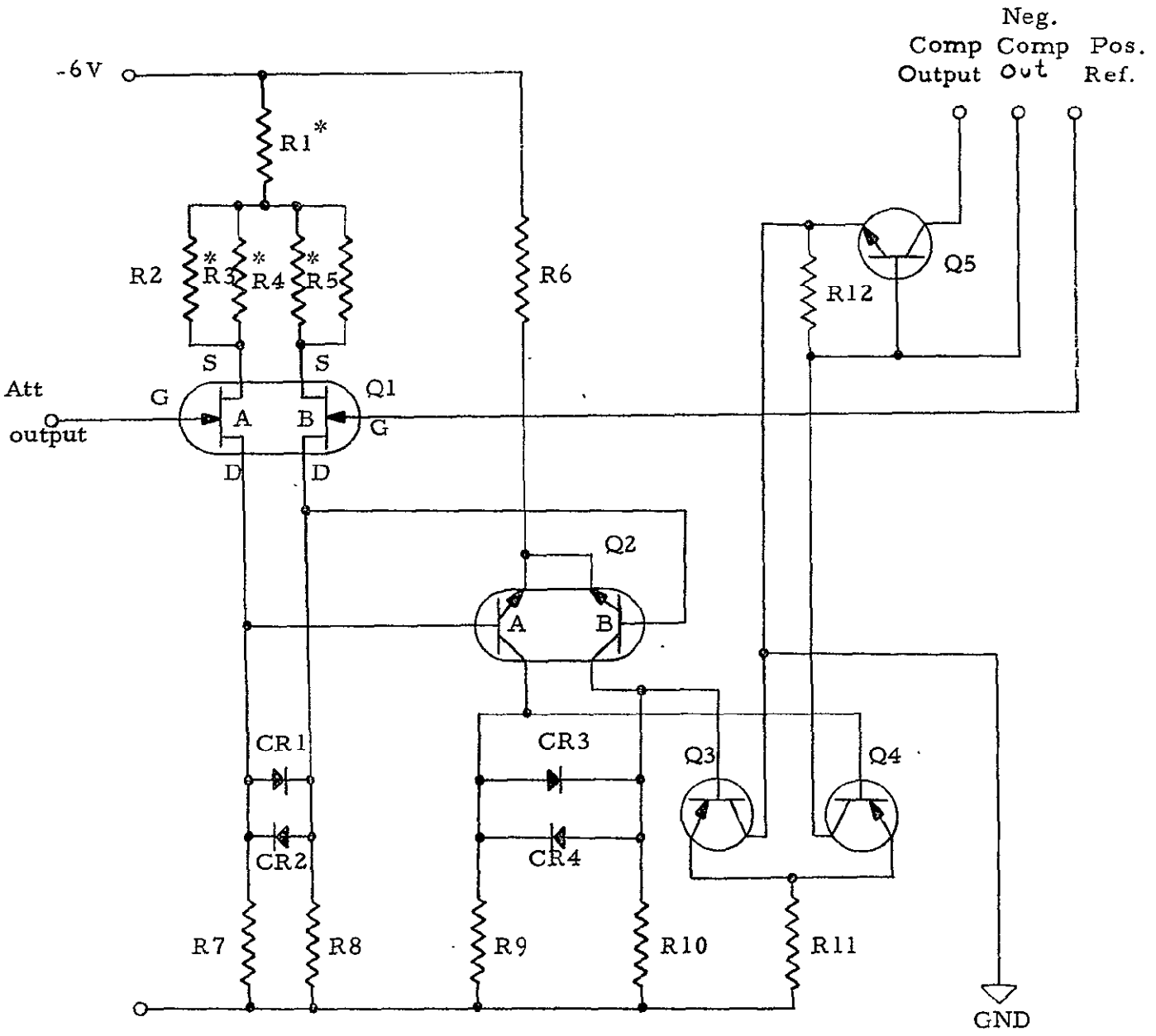
4.1.7 Positive and Negative Comparators

The comparators are each essentially a three-stage differential amplifier. Refer to Figure 4.1.7-1 for the schematic of the Negative Comparator, and to Figure 4.1.7-2 for the schematic of the Positive Comparator.

A high input impedance is achieved by the use of an FET differential input stage.



Negative Comparator Schematic Diagram
Figure 4.1.7-1



Positive Comparator Schematic Diagram
Figure 4.1.7-2

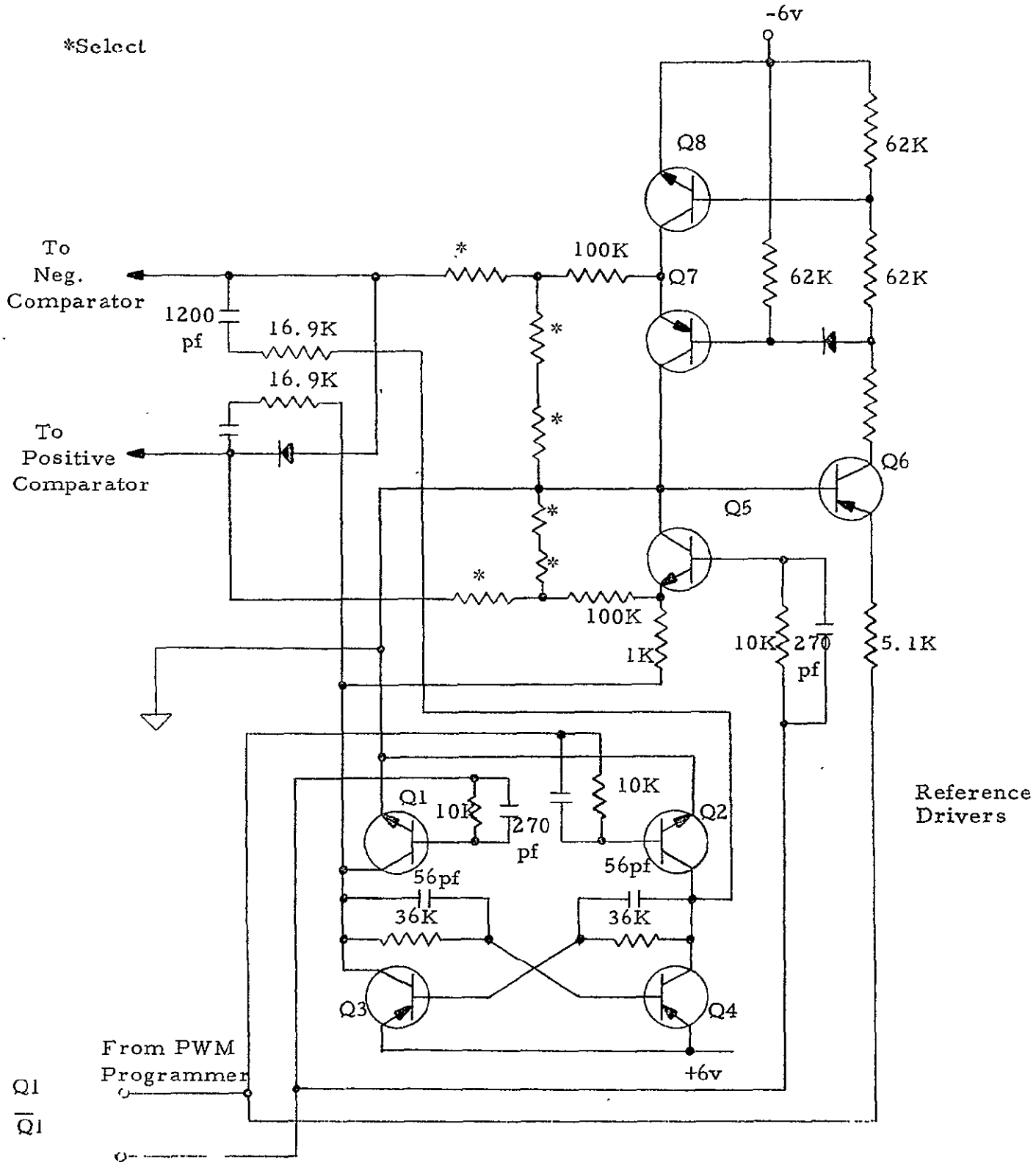
The offset compensation of the FET stage is accomplished by means of select resistors R_2 and R_5 for the Positive Comparator and R_{13} and R_{16} for the Negative Comparator. The output of the Negative Comparator is tied (in the system) to the base of the Positive Comparator's Q_5. This essentially results in an ORing function at Q_5.

The inputs to the FET differential stages can be either negative or positive. The output of the Attenuator Driver circuit is applied to Gate I of the transistor and a reference voltage is applied to Gate II of the transistor. A negative reference voltage is applied to Gate II of the FET in the Negative Comparator, and a positive reference voltage is applied to Gate II of the FET in the Positive Comparator circuit. If the input to Gate I is equal to the reference signal applied to Gate II, then the amplifier is balanced and the output at the collector of the transistor Q_5 will be a zero level. If the input to Gate I is not equal to the reference, the amplifier is unbalanced and the output at collector of transistor Q_5 will be about +1.5 volts.

4.1.8 Reference Generator, Offset Generator, and Reference Drivers

Figure 4.1.8-1 shows the schematic diagram of the Reference Generator, Offset Generator, and Reference Driver. Three Reference Drivers are used. These are interconnected, as shown in Figure 3.1.6-1, Reference Generator Network Block Diagram, with the Reference and Offset Generators.

For convenience, the schematic Figure 4.1.8-1 shows only the first Reference Generator, with logic signals for the case of the first reference level region. This is the case where the Offset Generator is activated by the PWM Programmer. Also, only one screening resistor for each Reference Generator is shown.



Reference Generator, Offset Generator,
and Reference Driver Schematic Diagram
Figure 4.1.8-1

Each set of the complementary signals (Q1, $\overline{Q1}$), (Q2, $\overline{Q2}$), and (Q3, $\overline{Q3}$) generated by the PWM Programmer is applied to one of the three Reference Drivers, as shown in Figure 3.1.6-1. The signal Q1 is applied to the base of transistor Q_2. When Q1 goes positive, transistor Q_2 goes into saturation. At this time, Q_2's collector voltage is about 0.02 volts. This causes transistor Q_3 to be ON, which in turn cuts off transistor Q_4. During this time, transistor Q_1 is held cut off by signal $\overline{Q1}$ which is low.

Signals Q2 and Q3 are likewise being sequenced, causing the remaining two Reference Drivers to respond in a similar number. Refer to the timing diagram, Figure 3.1.6-2.

C_1 and C_2 form part of the RC network that generates the exponential decay. Diode CR1 prevents negative transitions on the positive output and positive transitions on the negative output.

As previously discussed, the output of the Electrometer is compressed between the ranges of 2.16×10^{-11} to 1×10^{-9} amperes. The attenuation ratio is 1/15. The output of the Electrometer in this range contains a constant voltage of $\approx$6.8V due to the two zener diodes in the output circuit.

To compensate for this constant term, the Offset Generator produces a constant voltage of

$$\pm\frac{6.8}{15} = \pm 450 \text{ mv}$$

for the particular attenuation region of 1/15 only. This signal is applied directly to Gate II of the FET's in the comparators. The output signal Q1 of the PWM Programmer is applied to the emitter of transistor Q_6 of the Offset Generator.

This turns Q_6 ON. When Q_6 is ON, transistor Q_8 turns ON, pulling its collector potential to about -6V. Through an attenuator composed of select resistors, this potential is reduced to -450 millivolts and applied to Gate I of the FET in the negative Comparator section.

4.1.8.1 Reference Generator and Offset Generator

Refer to Figure 4.8.1-2 for the equivalent circuit of the Reference and Offset Generators. Also shows is a typical summing network.

The output of the summing network is a function of all signals applied to it.

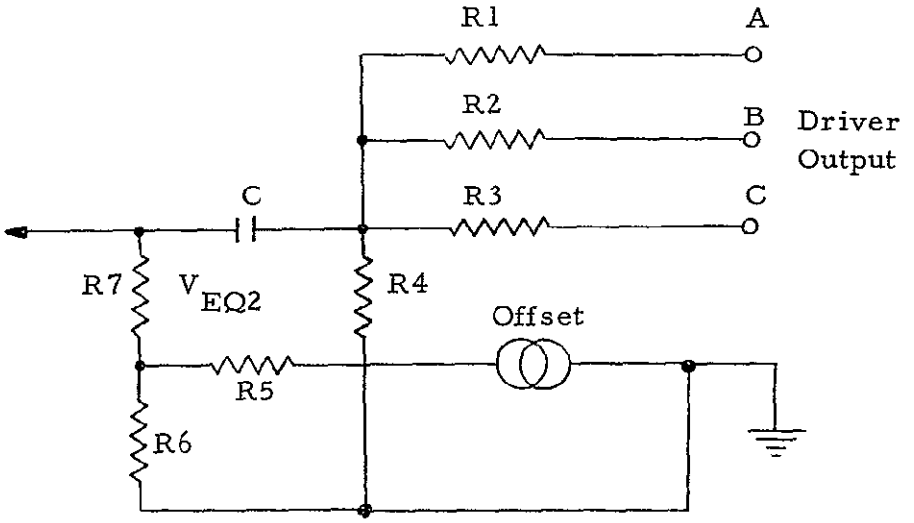
For Region I:

$A = 6V$

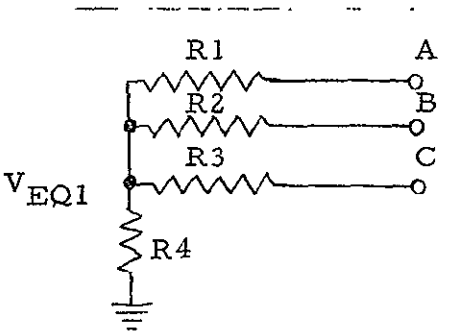
$B = C = 0V$

$$\text{Output } V_{EQ1} = \frac{\dfrac{R_2R_3R_4}{R_2R_3 + R_2R_4 + R_3R_4}}{R_1 + \dfrac{R_2R_3R_4}{R_2R_3 + R_2R_4 + R_3R_4}} \quad X\ (6)$$

V_{EQ1} is different for each region, because the outputs of the drivers do not occur at the same time.



(a) Reference and Offset Generators



(b) Typical Summing Network

Reference Generator and
Offset Generator Equivalent Circuit
Figure 4.1.8-2

For Region II

$$C = A = 0$$

$$B = 6V$$

$$\text{Output } V_{EQ_2} = \frac{\dfrac{R_1R_3R_4}{R_1R_3 + R_1R_4 + R_3R_4}}{R_2 \dfrac{R_1R_3R_4}{R_1R_3 + R_1R_4 + R_3R_4}} \quad (6)$$

For Region III

$$A = 0$$

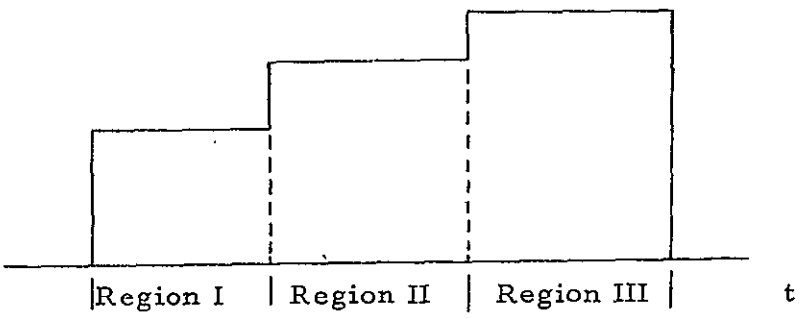
$$B = C = 6V$$

$$\text{Output } V_{EQ_3} = \frac{\dfrac{R_1R_4}{R_1+R_4}}{\dfrac{R_2R_3}{R_2+R_3} + \dfrac{R_1R_4}{R_1+R_4}} \quad (6)$$

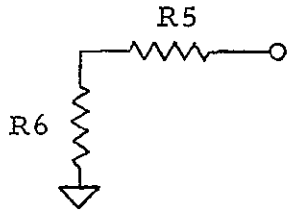
Total resistance of summing point:

$$R_{EQ_1} = \frac{R_1R_2R_3R_4}{R_1R_2R_3 + R_1R_2R_4 + R_1R_3R_4 + R_2R_3R_4}$$

V_{EQ_1};



V_{EQ_2} is the potential developed by the dividing network formed by R_5 and R_6 for Region I.



$$A = 6V \quad B = 0 \quad C = 0$$

$$V_{EQ_2} = 6 \frac{R_6}{R_5 + R_6}$$

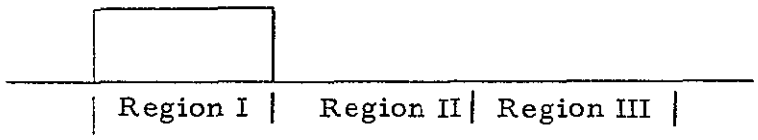
For Region II

$$A = 0 \quad B = 0 \quad C = 0$$

Therefore: $V_{EQ_2} = 0$

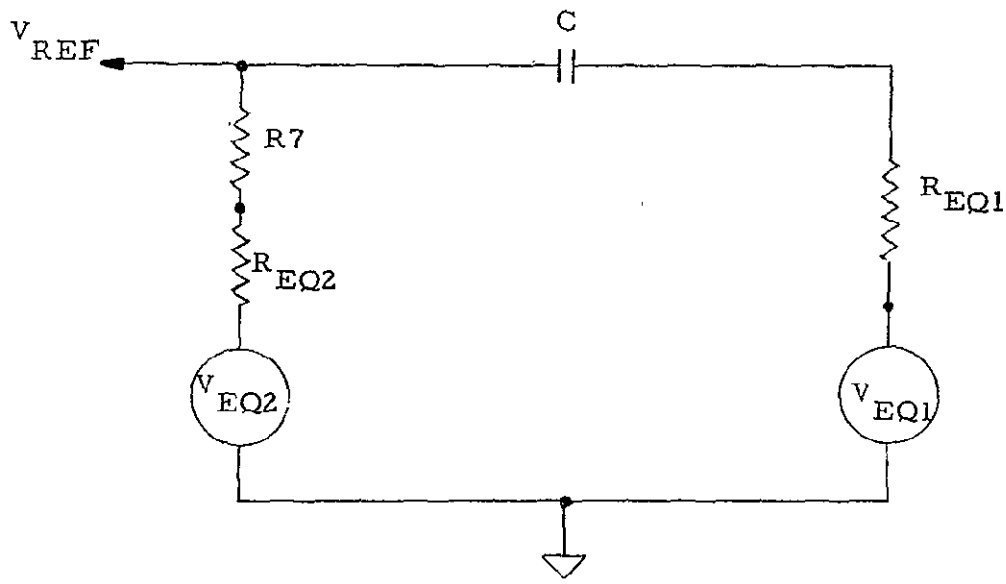
and for Region III $V_{EQ_2} = 0$

V_{EQ_2} can be represented by the figure below:



Total resistance is: $R_{EQ_2} = \frac{R_5 R_6}{R_5 + R_6}$

The network for generating the reference signal could be represented now by:



Equivalent circuit, reference generator

$V_{Ref.}$ can be computed by use of Laplace Transforms.

$$V_{Ref.(s)} = V_{EQ_1} \frac{R_7 + R_{EQ_2}}{R_7 + R_{EQ_2} + R_{EQ_1} + \frac{1}{SC}} + V_{EQ_2} \frac{R_{EQ_1} + \frac{1}{SC}}{R_7 + R_{EQ_2} + R_{EQ_1} + \frac{1}{SC}}$$

OR

$$V_{Ref.(s)} = V_{EQ_1} \frac{(R_7 + R_{EQ_2})SC}{(R_7 + R_{EQ_2} + R_{EQ_1})SC + 1} + V_{EQ_2} \frac{(R_{EQ_1})SC + 1}{(R_7 + R_{EQ_2} + R_{EQ_1})SC + 1}$$

Let $(R_7 + R_{EQ_2} + R_{EQ_1})C = \gamma$

and

$$\frac{R_7 + R_{EQ_2}}{R_7 + R_{EQ_2} + R_{EQ_1}} = K$$

We now can write

$$V_{Ref(S)} = V_{EQ_1}\left[\frac{K\gamma S}{\gamma S + 1}\right] + V_{EQ_2}\left[\frac{1 + (k-1)\gamma S}{\gamma S + 1}\right]$$

OR

$$V_{Ref(S)} = V_{EQ_1}\frac{\left[KV_{EQ_1} + (K-1)V_{EQ_2}\right]S}{\gamma S + 1} + \frac{V_{EQ_2}}{\gamma S + 1}$$

V_{EQ_1} and V_{EQ_2} can be represented in the time domain with the following expressions.

$$V_{EQ_{1(t)}} = \underset{RI}{V_{EQ_1}}\,\mu(t-I) + (\underset{RII}{V_{EQ_1}} - \underset{RI}{V_{EQ_1}})\,(t-II) + (\underset{RIII}{V_{EQ_1}} - \underset{RII}{V_{EQ_2}})\,\mu(t-III)$$

$$V_{EQ_{2(t)}} = \underset{RI}{V_{EQ_2}}\,\mu(t-I) - \underset{RI}{V_{EQ_2}}\,\mu(t-II)$$

These equations expressed in Laplace notation yield

$$V_{EQ_{1(S)}} = \frac{1}{S}\left[\underset{RI}{V_{EQ_1}}\,e^{-IS} + (\underset{RII}{V_{EQ_1}} - \underset{RI}{V_{EQ_1}})\,e^{-IIS} + (\underset{RIII}{V_{EQ_1}} - \underset{RII}{V_{EQ_1}})\,e^{-IIIS}\right]$$

and

$$V_{EQ_{2(S)}} = \frac{1}{S}\left[V_{\underset{RI}{EQ_2}}\, e^{-IS} - V_{\underset{RII}{EQ_2}}\, e^{-IIS}\right]$$

Substituting the expressions for V_{EQ_1} and V_{EQ_2} in the $V_{Ref(s)}$ equation we obtain

$$V_{Ref(s)} = e^{-IS}\left\{\frac{\left[K V_{\underset{RI}{EQ_1}} + (K-1)\, V_{\underset{RI}{EQ_2}}\right]\gamma}{\gamma S + 1} + \frac{1}{S}\,\frac{V_{\underset{RI}{EQ_2}}}{\gamma S + 1}\right\} +$$

$$e^{-IIS}\left\{\frac{K\left(V_{\underset{RII}{EQ_1}} - V_{\underset{RI}{EQ_1}}\right) + (K-1)\left(V_{\underset{RII}{EQ_2}} - V_{\underset{RI}{EQ_2}}\right)\gamma}{\gamma S + 1} + \frac{1}{S}\,\frac{\left(V_{\underset{RII}{EQ_2}} - V_{\underset{RI}{EQ_2}}\right)}{\gamma S + 1}\right.$$

$$\left. + e^{-IIIS}\left\{\frac{-K\left(V_{\underset{RIII}{EQ_1}} - V_{\underset{RII}{EQ_1}}\right)}{\gamma S + 1}\right\}\right.$$

Let

$$a = KV_{\underset{RI}{EQ_1}} + (K-1)\, V_{\underset{RI}{EQ_2}}$$

$$b = V_{\underset{RI}{EQ_2}}$$

$$c = K\left(V_{\underset{RII}{EQ_1}} - V_{\underset{RI}{EQ_1}}\right) + (K-1)\left(V_{\underset{RII}{EQ_2}} - V_{\underset{RI}{EQ_2}}\right)$$

$$d = \left(V_{\underset{RII}{EQ_2}} - V_{\underset{RI}{EQ_2}}\right)$$

$$f = K\left(V_{\underset{RIII}{EQ_1}} - V_{\underset{RII}{EQ_1}}\right)$$

Substitute these in the $V_{Ref}(s)$ expression and transfer into the time domain.

$$V_{REF} = u(t-I)\left[b + (a-b)\,e^{\left(\frac{-t-I}{\gamma}\right)}\right] +$$

$$u(t+II)\left[d + (c-d)e^{\left(\frac{-t-II}{\gamma}\right)}\right] +$$

$$u(t-III)\left[fe^{\left(\frac{-t-III}{\gamma}\right)}\right]$$

A graphical representation of the prescaling is shown in Figure 4.1.8-3, Reference Generator Output Diagrams.

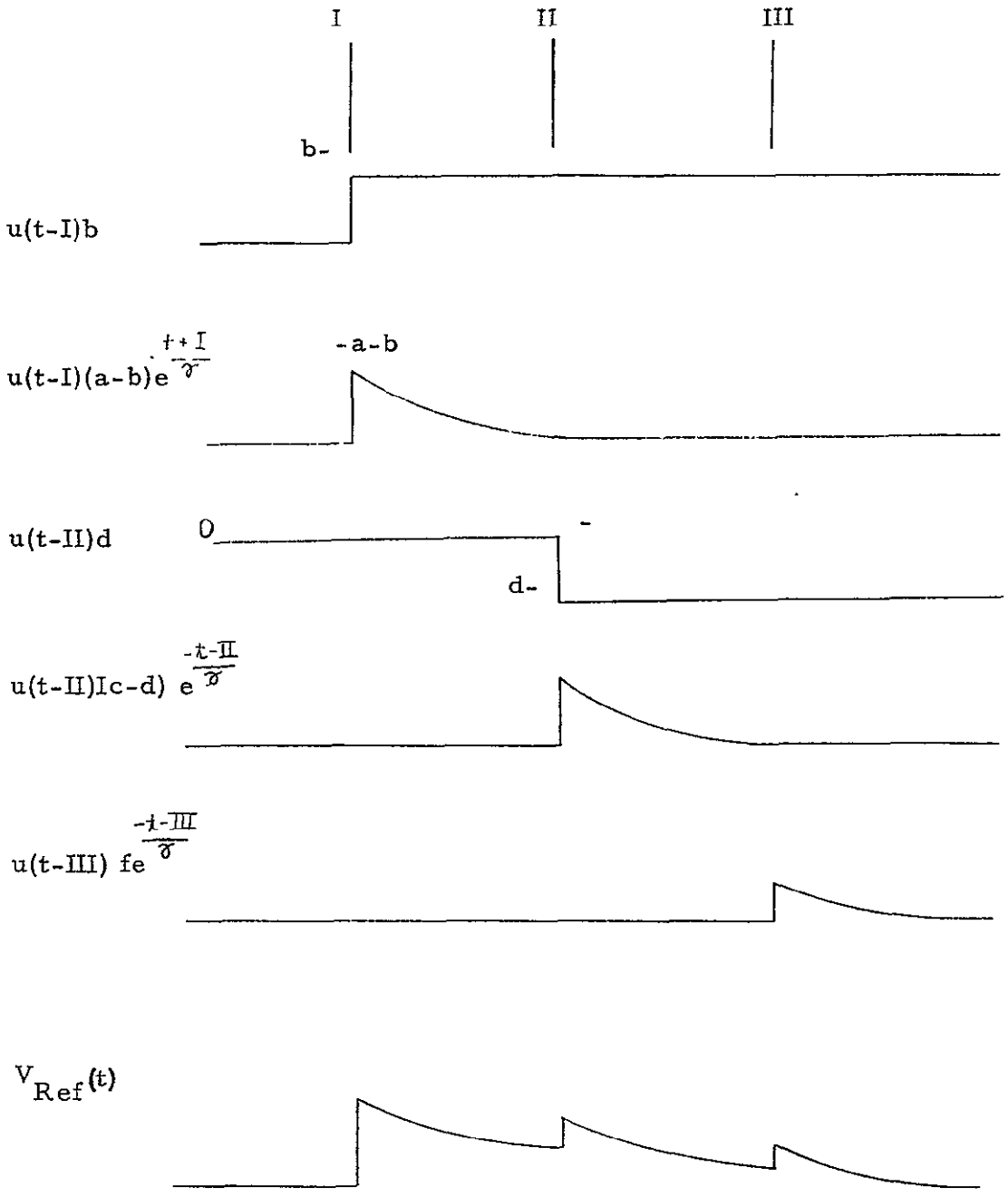
4.2 High Voltage Comparator

Figure 4.2-1, High Voltage Comparator Simplified Schematic, shows the basic elements of the comparator.

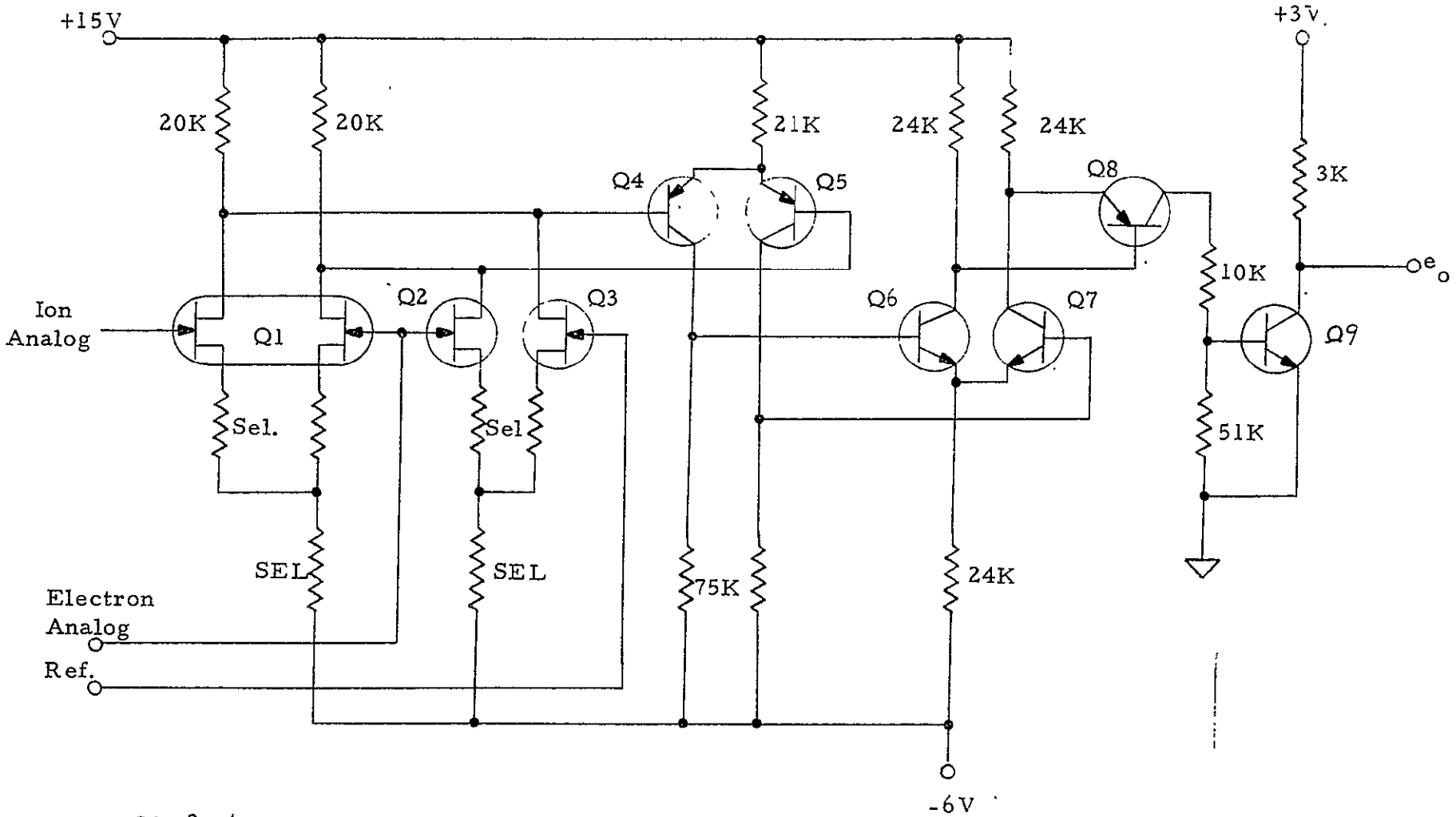
The control circuit for selecting the input pair is not shown. The FET's are selected for a limited range of pinch-off voltage. The biasing resistors are selected at zero input voltage for circuit balance and drain currents of about 340μa.

The important requirement is the resolution of the differential input voltage necessary to switch the output from full ON to full OFF.

Assume that Q_8 and Q_9 operate as switches and that the necessary differential voltage swing at the collectors of Q_6 and Q_7 is 1v. The required voltage resolution at the input is 50 μvolts, which is a gain of 20,000.



Reference Generator Output Waveforms
Figure 4.1.8-3



Q1, 3, 4	-	2N3954
Q5, 6, 9	-	2N2907A
Q8,	-	2N2484
Q10	-	2N2369

High Voltage Comparator Simplfied Schematic
Figure 4.2-1

Using the following parameters:

Minimum g_m of FET = 1000

Minimum Beta of bipolars = 20

Differential input Z of the first bipolar pair = 2K ohms

The approximate differential gain of the FET pair is

$$G_1 = 2g_m R_L$$

$$= 2 \times 10^{-3} \times 2 \times 10^{3} = 4$$

The approximate gain of the two bipolar stages is

$$G_2 = 2B_1 B_2 \frac{R_L}{R_{IN}}$$

$$= 2 \times 20 \times 20 \times \frac{24K}{2K}$$

$$= 800 \times 12 = 9600$$

Total Gain = $G_1 \times G_2$

$$= 4 \times 9600$$

$$= 38400$$

4.3 Temperature Sensor

The function of the Temperature Sensor is to provide a d-c output proportional to the change in temperature sensed by the instrument electronics. The sensing element is a YSI 44018 thermistor.

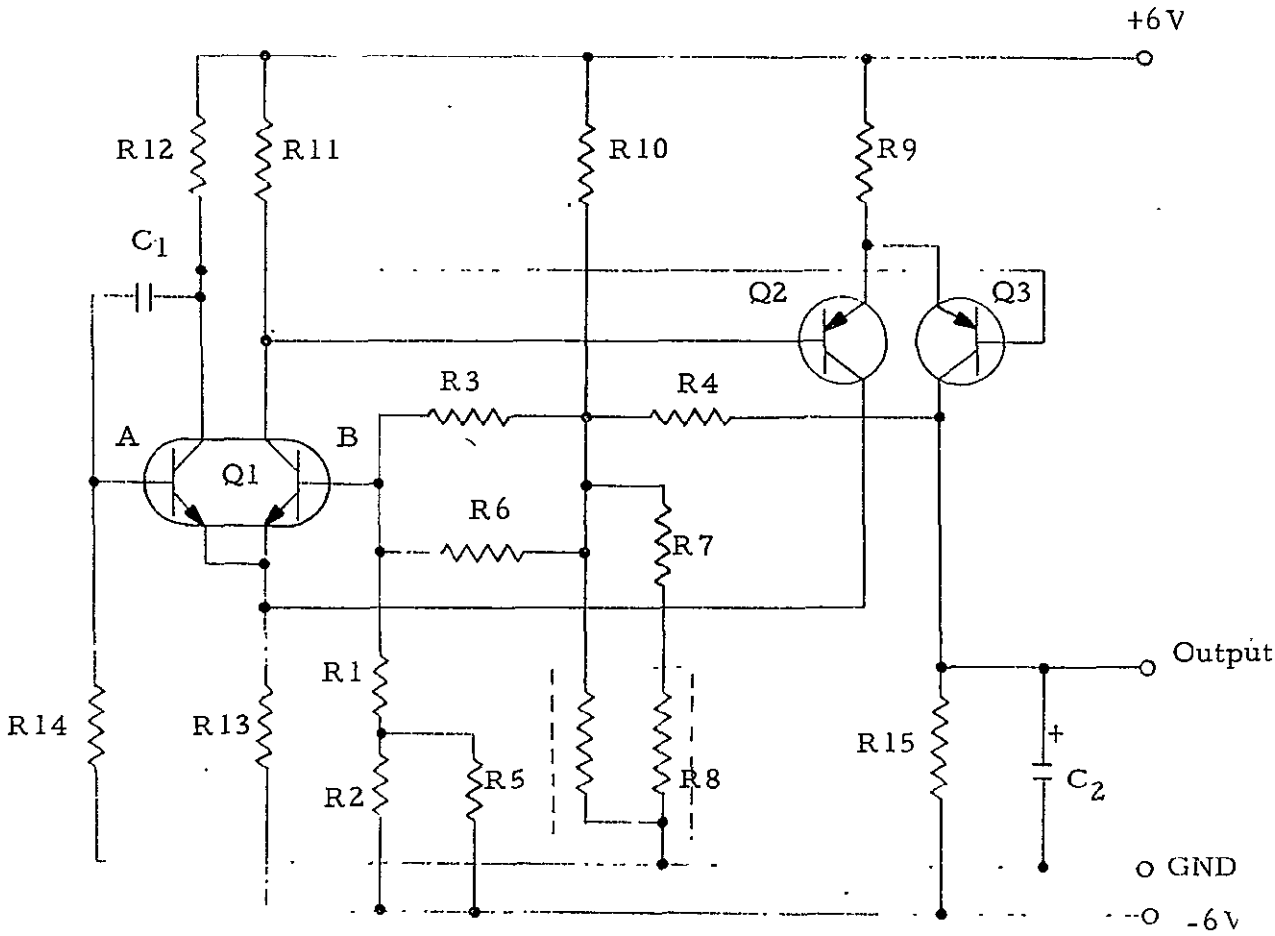
The Temperature Sensor is essentially a two stage differential amplifier, the output of which is dependent on the change in the resistance of the thermistor. See Figure 4.3-1 for the Temperature Sensor schematic.

Q_1 is a differential amplifier stage that senses a change in voltage applied to Q_{1B} by means of the divider network R_8, R_7, R_{10}, and R_6. Q_{1A} is connected to ground through R_{14}. The error signal is amplified by Q_2 and Q_3, a matched pair of transistors operating as a differential amplifier. The output is fed back to Q_{1B} continuously through the divider network R_1, R_2, R_5, and R_3, R_4. The temperature sensor circuit is calibrated for high and low temperature changes by the select resistors R_1, R_2, R_5 and R_3, R_4. The thermistor is a double element sensing device and the parallel combination of the two provides for a better linearity and accuracy of the output verus temperature. An ideal curve of output versus temperature is shown in Figure 4.3-2.

4.4 Current Switches

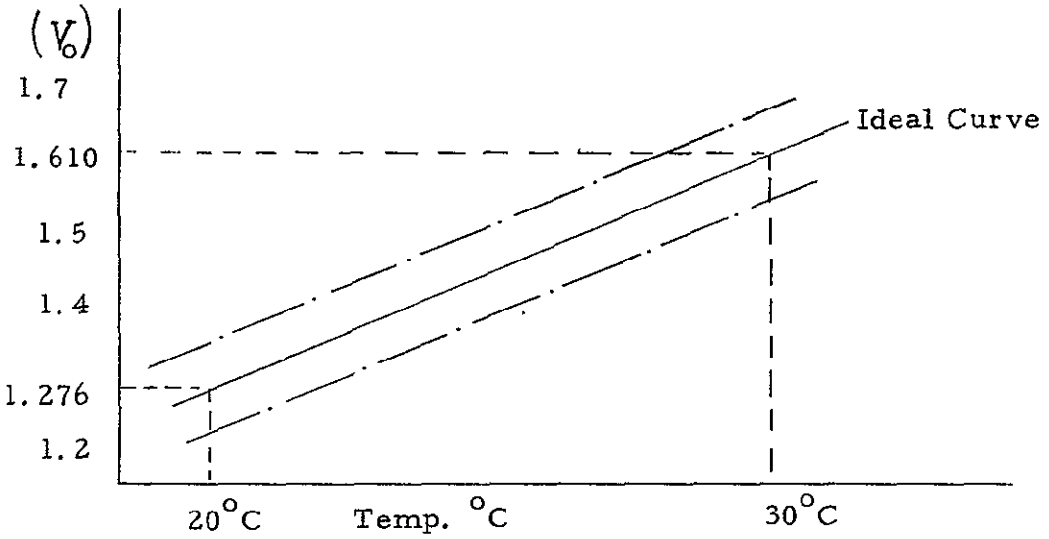
The Current Switches are three-stage saturated switches used to select the X and Y lines (refer to Figure 3.3.1-2, Core Plane Drive Lines, for the configuration). Figure 4.4-1 shows the schematic diagram of a typical Current Switch.

The input gating structure is AND/OR. The switch is selected when the Read Address and Read Timing are High, or when Write Address and Write timing are High. The two front end storages provide the current gain required to insure a low impedance path for the select current coming from the current source through the drive lines. The switch is turned on before the current source to allow time for the output to saturate before the drive current is turned on.



Q_1 = 2N4042 Transistor
$Q_2 = Q_3$ = ML20001
R_1 = Select Resistor
R_2 = " "
R_3 = " "
R_4 = " "
R_5 = Select Resistor
R_6 = 11.5K ± 1% Resistor
R_7 = 14.7K ± 1% Resistor
R_8 = YSI44018 Thermistor
R_9 = 6.8K ± 5% Resistor
R_{10} = 23.2K ± 1% Resistor
$R_{11} = R_{12}$ = 53.6K ± 1% Resistor
R_{13} = 39K ± 5% Resistor
R_{14} = 10K ± 5% Resistor
C_1 = 1000 pf Capacitor
C_2 = 2.2 ufd Capacitor

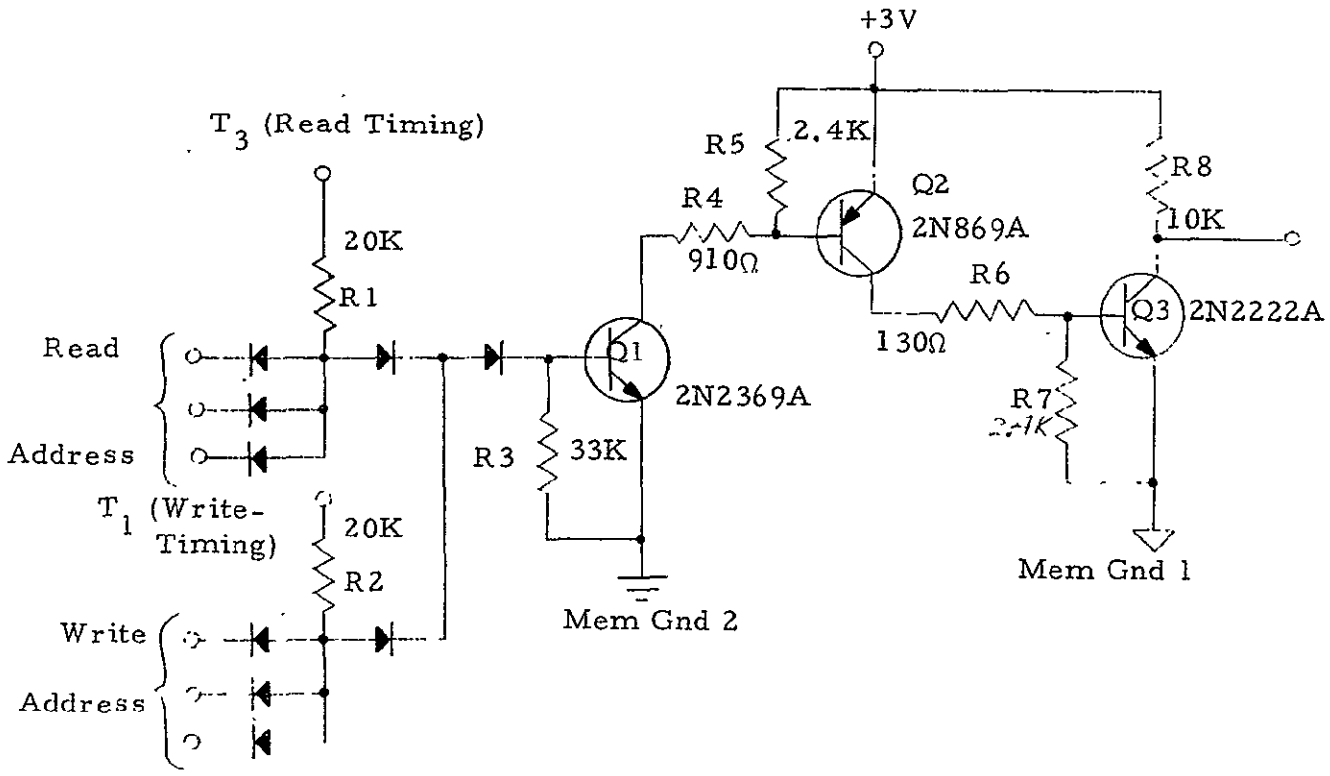
Temperature Sensor Schematic
Figure 4.3-1



$$T(^{\circ}C) = \frac{V_o}{33.4 \times 10^{-3}} - 18.2$$

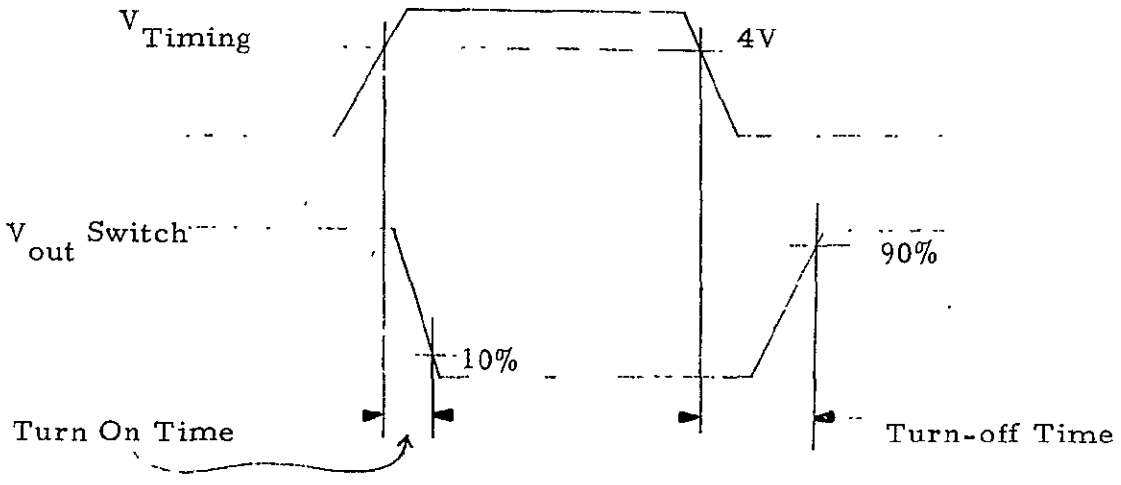
slope = 33.4mv/°C

Temperature Sensor Output versus Temperature
Figure 4.3-2



Current Switch Schematic Diagram

Figure 4.4.-1



Current Switch Turn-on and Turn-off Time
Figure 4.4-2

The output stages are referenced to the high current ground to minimize ground noise in the decoding section. The collector resistor reverse biases the stack decoding diodes when the switch is off.

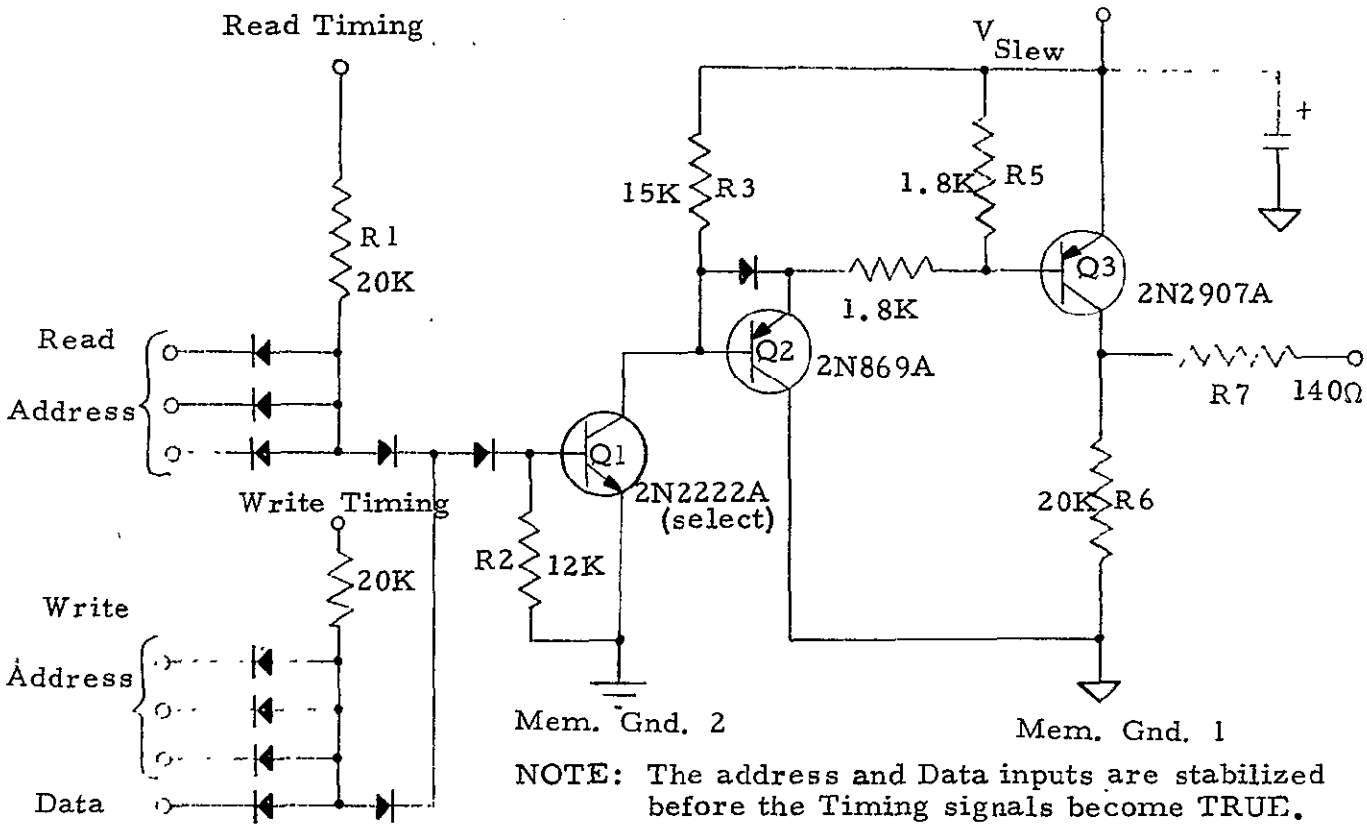
The following are electrical parameters for the Current Switches:

Operating Temperature		$-15^{\circ}C$ to $+55^{\circ}C$
Address inputs:	True level	2v minimum
	False level	0.22v maximum
Timing inputs:	True level	5.85 ±0.15v
	False level	0.1v maximum
Output:	Load current	135ma. maximum
	Output voltage with full load	0.3v maximum
	Load capacitance	100μμf maximum
	Input noise rejection	0.25v minimum
	Turn-on time (See Figure 4.4-2)	0.3 microseconds maximum
	Turn-off time (See Figure 4.4-2)	3 microseconds maximum

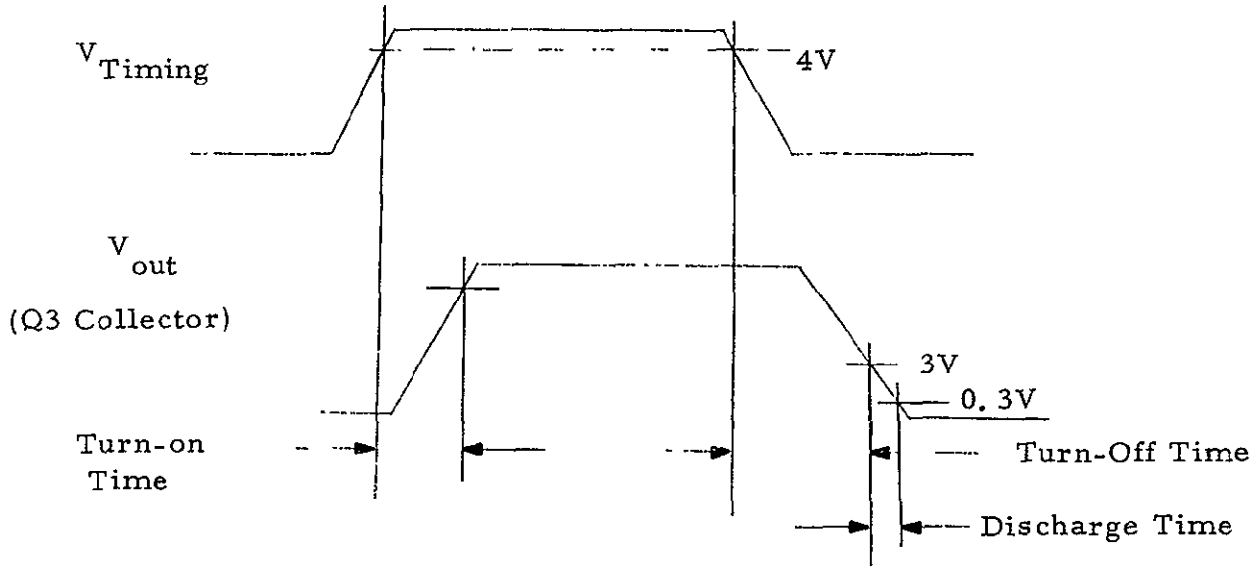
4.5 Current Drivers

The Current Drivers are three-stage saturating drivers used to provide the stack select currents (refer to Figure 3.3.1-2, Core Plane Drive Lines). See Figure 4.5-1 for the schematic diagram of a typical Current Driver.

The input gating is AND/OR. The Current Driver is ON when the Read Address or Read Timing are High, or when Write Address, Write Timing, and Data are High. The current supplied by the driver is determined by R7 and the collector supply V_{slew}; V_{slew} varies with temperature, thus adjusting the select current to that required for optimum stack operation at the operating temperature.



Current Driver Schematic Diagram
Figure 4.5-1



Current Driver Turn-on and Turn-off Times
Figure 4.5-2

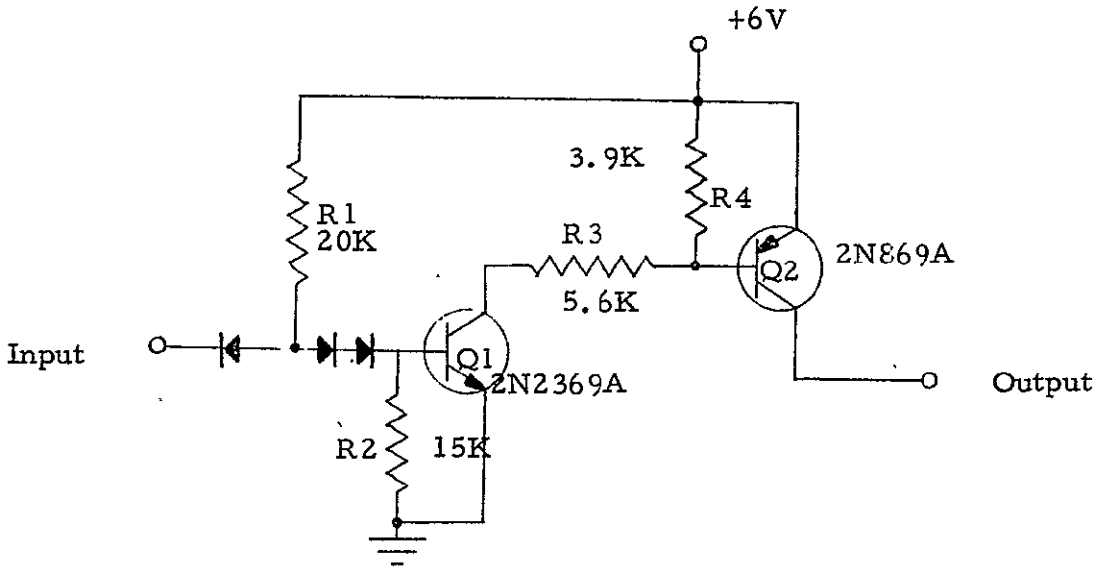
The following are electrical parameters for the Current Drivers:

Operating temperature		-15°C to +55°C
Address and data inputs:	True level	2v minimum
	False level	0.22v maximum
Timing inputs:	True level	5.85 ±0.15v
	False level	0.1v maximum
Output:	Load current	135ma maximum @-15°C 84ma minimum @+55°C
	Input noise rejection	0.25v minimum
	Turn-on time (See Figure 4.5-2)	0.75 microseconds maximum
	Turn-off time (See Figure 4.5-2)	4 microseconds maximum
	Discharge time (See Figure 4.5-2)	3.8 microseconds maximum

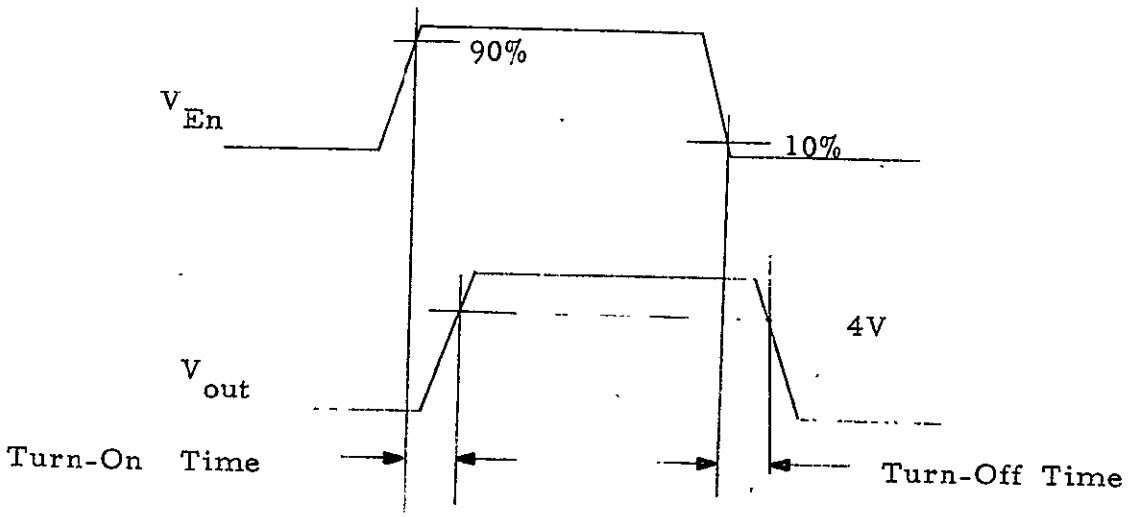
4.6 Gate Switch

The schematic diagram of the Gate Switch is shown in Figure 4.6-1. The Gate Switches are two stage saturating drivers used to gate the timing signals to the Current Drivers and Switches.

The following are operating characteristics of the Gate Switches:



Gate Switch
Figure 4.6-1



Gate Switch Turn-On and Turn-Off Times
Figure 4.6-2

Operating Temperature		-15°C to +55°C
Input:	True level	2v minimum
	False level	0.22v maximum
Output:	Load current	4ma maximum
	Output voltage with full load	5.85 ±0.15V
	Load capacitance	10μμf maximum
	Input noise rejection	0.25V minimum
	Turn-on time (See Figure 4.6-2)	0.3 microseconds maximum
	Turn-off time (See Figure 4.6-2)	1.5 microseconds maximum

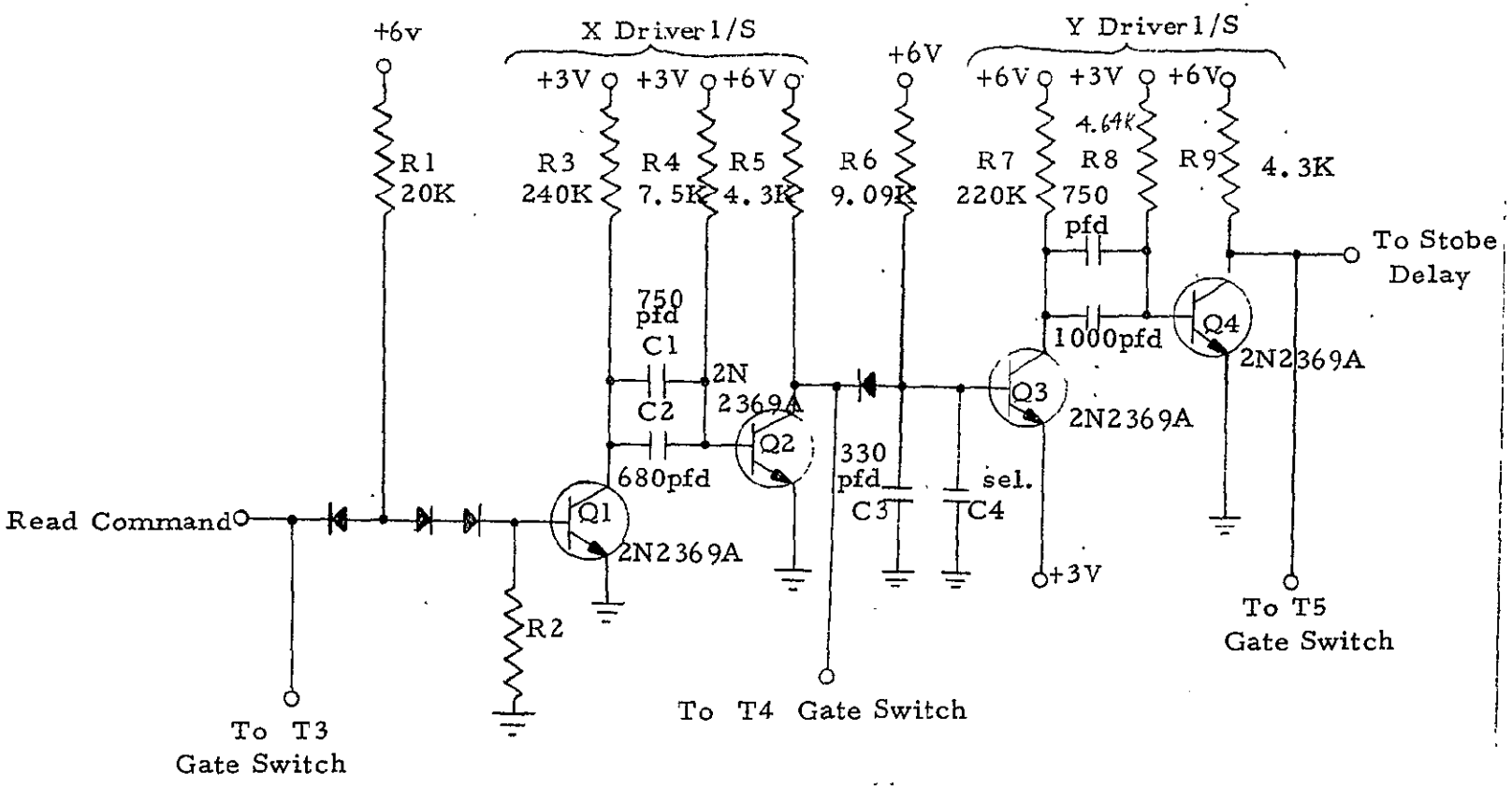
4.7 Read Timing Circuit

The Read Timing Circuit (Figure 4.7-1) is used to provide the timing signals for the memory read cycle.

A Read Command, sensed at the Timing Circuit input, turns on the Current Switches through the Gate Switch whose input is T3. The Selected X Read drivers are turned on through Gate Switch T4 and after a delay of 2.5 microseconds ±0.36 microseconds. The selected Y Current drivers are enabled by the T5 gate switch. The X and Y driver on-times are limited by the X and Y driver one-shots.

The following are electrical characteristics for the Read Timing Circuit:

Operating temperature		-15°C to +55°C
Read Command Input:	True level	2v minimum
	False level	0.22v maximum
	Pulse width	11 ±2 microseconds @ 50% pts
	Rise time	1 microsecond maximum



Read Timing Circuit Schematic Diagram
Figure 4.7-1

Fall time	1 microsecond maximum
Rep rate	512 hz maximum

T_3 Output: Connected to T_3 Gate Switch (Switches)
Specifications same as Read Command

T_4 Output: Connected to T_4 Gate Switch (X Drivers)

True level	6v ±60 mv
False level	0.3v maximum
Pulse width @ 50% pts	7.6 microseconds minimum/9.9 microseconds maximum

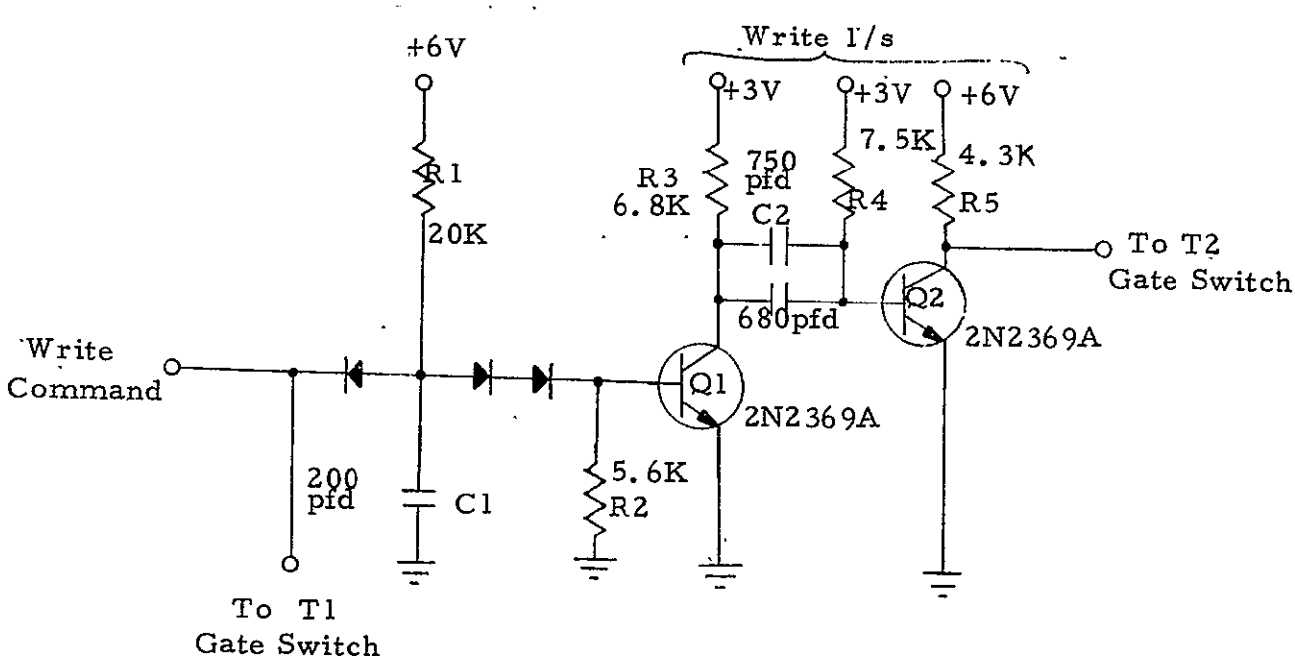
T_5 Output: Connected to T_5 Gate Switch (Y Drivers) and strobe delay circuit

True level	6v ±60 mv
False level	0.3v maximum
Turn -on delay from T_4	2.14 microseconds minimum 2.86 microseconds maximum
Pulse width @ 50% pts	7.7 microseconds maximum 5.3 microseconds minimum

4.8 Write Timing Circuit

The Write Timing Circuits (Figure 4.8-1) are used to provide the timing signals for the memory write cycle.

The input signal (Write Command) turns on the Current Switches through Gate Switch T1. After a 1.19 μsec ±0.63 μsec delay, the Current Drivers are enabled by timing signal T2.



Write Timing Circuit Schematic Diagram
Figure 4.8-1

The Write one-shot limits the Write driver ON-time to 9.9 μsec maximum.

The following are electrical characteristics of the Write Timing circuit:

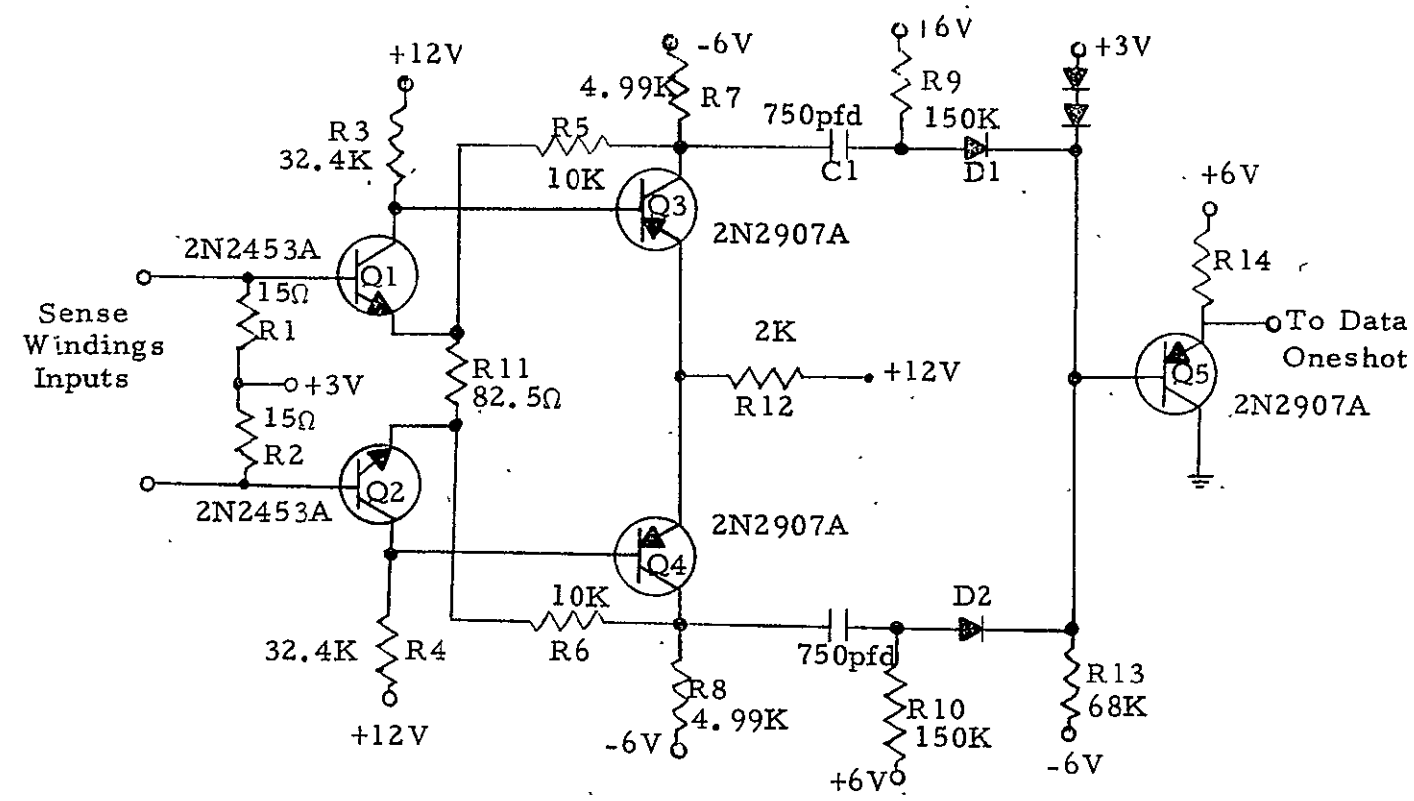
Operating temperature		-15°C +55°C
Write command input:	True level	2v minimum
	False level	0.22v maximum
	Pulse width	11 ±2 microseconds @ 50% pts
	Rise time	1 microsecond maximum
	Fall time	1 microsecond maximum
	Rep rate	20 KC maximum

T_1 Output: Connected to T_1 Gate Switch (Switches)
Specifications same as Write Command

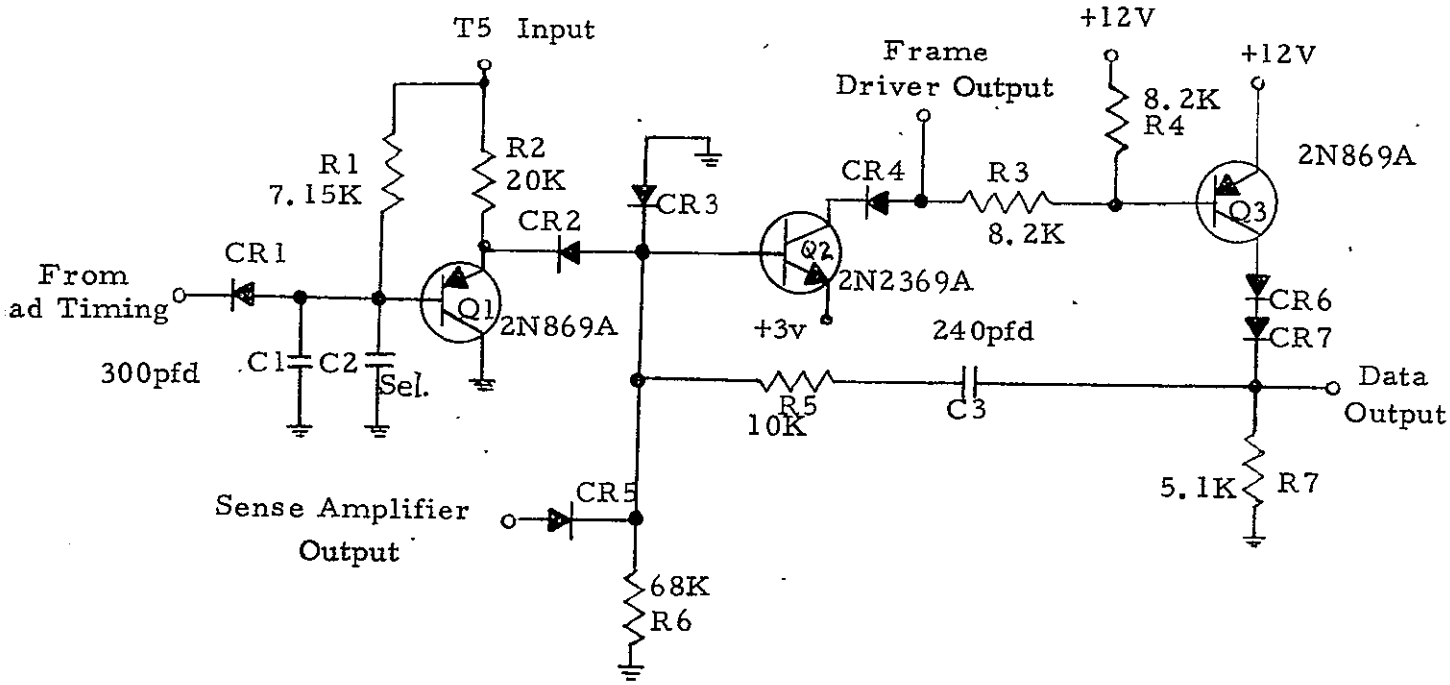
T_2 Output:	Connected to T_2 Gate Switch (Drivers)	
	True level	6v ±60 mv
	False level	0.3v maximum
	Pulse width @ 50% pts	7.6 microseconds minimum
		9.9 microseconds maximum
	Turn-on delay from T_1	0.56 microseconds minimum
		1.82 microseconds maximum

4.9 Sense Amplifier

The Sense Amplifier (Figure 4.9-1) is used to amplify the output signal from the core-plane.



Sense Amplifier Schematic Diagram
Figure 4.9-1



Strobe Delay and Data One-Shot
Figure 4.10-1

The circuit is a two-stage differential amplifier. The first stage uses matched transistors to minimize offset and provide bias stability. To stabilize the d-c operating point and a-c gain, feedback is used from the collector of the second stage to the emitter of the first stage. The bipolar output from the amplifier is rectified by diodes D_1 and D_2. The rectified signal referenced to the clipping level is fed to the discriminator circuitry through an emitter follower. The emitter follower is used to provide isolation and prevent loading of the amplifier. The amplified signal is a-c coupled to the rectifier to prevent any d-c drift from appearing as a signal.

The following are electrical characteristics of the sense amplifier:

Gain	100 minimum
Gain stability	±9.5%
Dynamic range	3.5v minimum
High frequency cutoff	1 MHz minimum
Transient recovery time	0.6 microseconds maximum
Input from sense line:	
Signal	30 mv minimum
	1.5 - 3.0 microseconds duration
Noise	20 mv maximum
	0.5 microseconds duration

4.10 Strobe Delay and Date One-Shot

See Figure 4.10-1 for the schematic diagram. The Strobe Delay and Data One-Shot circuit is the final data-output stage. The Read Timing and T5 timing input signals strobe the Sense Amplifier output to trigger the output one-shot (Refer to Figure 3.3.1-5, Read Cycle Timing Diagram).

The emitter of Q_1 is normally below +3 volts, preventing the input transistor of the Data One-Shot (Q_2) from triggering on a noise output from the Sense Amplifier, which is clamped to the emitter of Q_1 by CR2 and CR5.

When T5 goes high, the Real timing signal is High and CR1 is reverse-biased. The emitter of Q1 starts to rise as C1 is charged and the output of the Sense Amplifier moves up. The emitter of Q1 rises at such a rate that Q2 cannot become forward biased for 0.9 - 1.1 microseconds after T5 comes true. When a core storing a "1" is read out, the amplified signal referenced to the clipping level is high enough in amplitude and long enough in duration to allow the Sense Amplifier output to rise above the threshold voltage of Q2 and trigger the output one-shot. The output one-shot limits the duration of the data output signal.

The following are electrical characteristics of the Strobe-Delay and Data One-Shot:

Operating temperature		-15°C to +55°C
Input 1:	From Read Timing	
T5 input:	From T5 Gate Switch	
Sense Amp input:	From Sense Amplifier output	
Frame Driver inpt:	From Frame Driver	
Date Output:	Load	3.9K to ground
		300μμf to ground
	True level	10v ±1v
	False level	0.2v maximum
	Rise time	0.5 microseconds maximum
	Fall time	3 microseconds maximum
	Pulse width @ 50% pts	7 ±3 microseconds

4.11 Frame ID Driver

The Frame ID Driver, shown in Figure 4.11-1, is used to transmit frame information through the output one-shot.

The following are electrical characteristics of the Frame ID Driver:

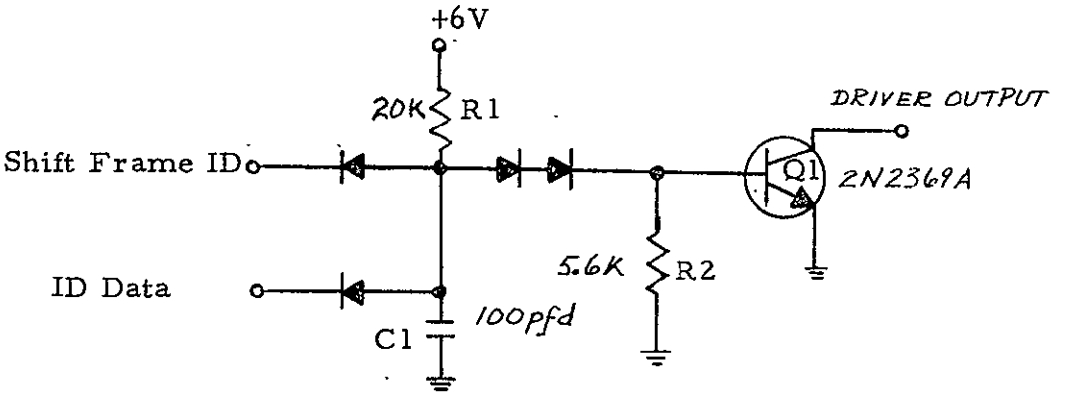
Operating temperature		-15°C +55°C
Input:	True level	2v minimum
	False level	0.22v maximum
	Pulse width @ 55% pts	4 microseconds minimum
		8 microseconds maximum
Output:	Load	Drives data one-shot
	Turn-on delay	0.34 microseconds minimum
		1.04 microseconds maximum

4.12 Ion DC Amplifier

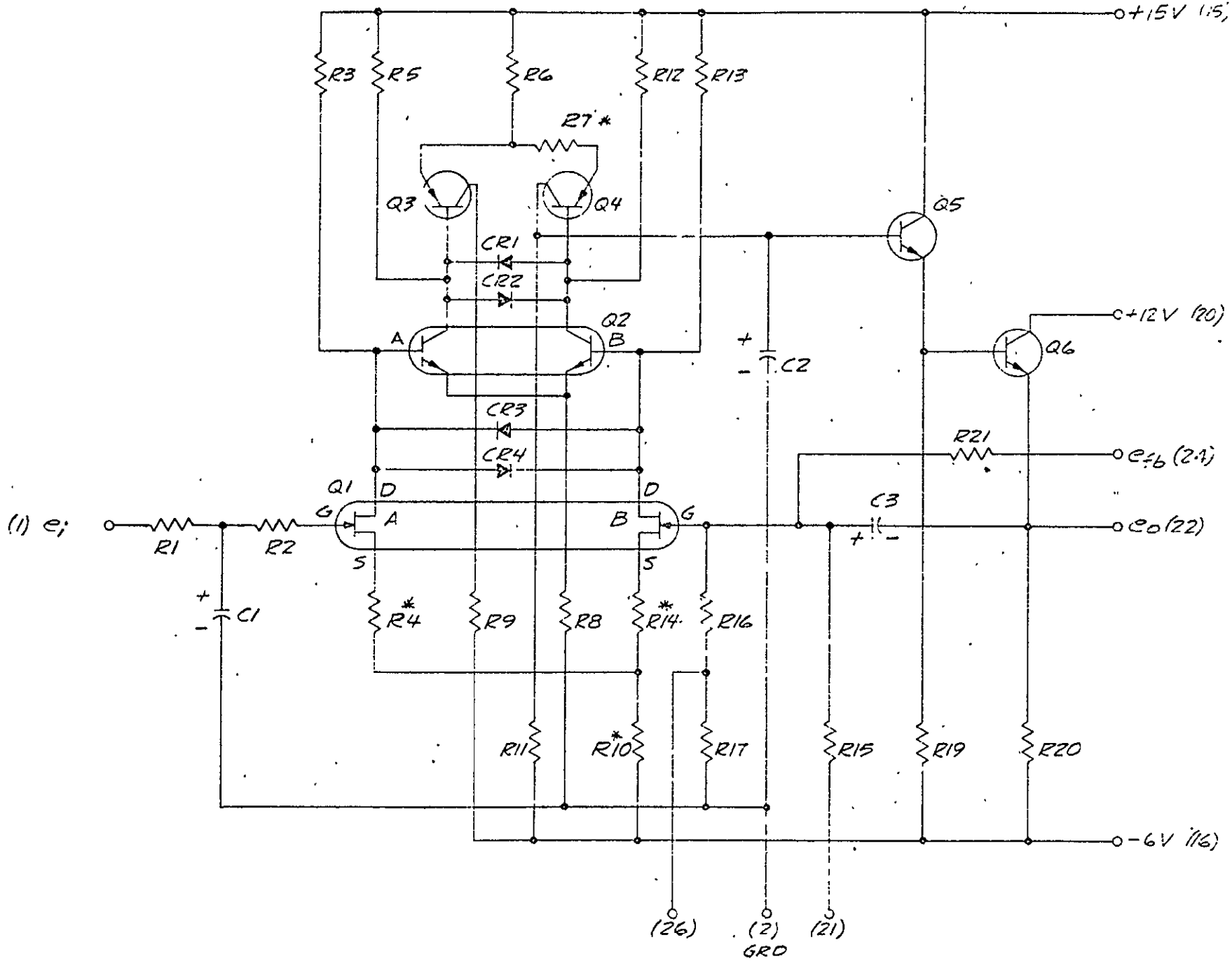
Refer to Figure 4.12-1 for the Ion DC Amplifier schematic.

The Ion DC amplifier is a three stage differential amplifier. The amplifier amplifies the error signal which is the difference between the input ramp voltage and the ion feedback network voltage. The amplifier has a gain of approximately 3.3.

A high input impedance is achieved by the use of an FET differential input stage. The gain of the amplifier is a function of the feedback elements and is determined by the following ratio:



Frame ID Driver
Figure 4.11-1



Ion D-C Amplifier
Figure 4.12-1

$$A_f = \frac{R_f + R_{16}\dfrac{R_{17} \times R_{18}}{R_{17} + R_{18}}}{R_{16} + \dfrac{R_{17} \times R_{18}}{R_{17} + R_{18}}}$$

R_{18} = select resistor in parallel with R_{17}

The offset compensation of the FET stage is accomplished by means of select resistors R_4 and R_{14}.

4.13 High Voltage Power Supply

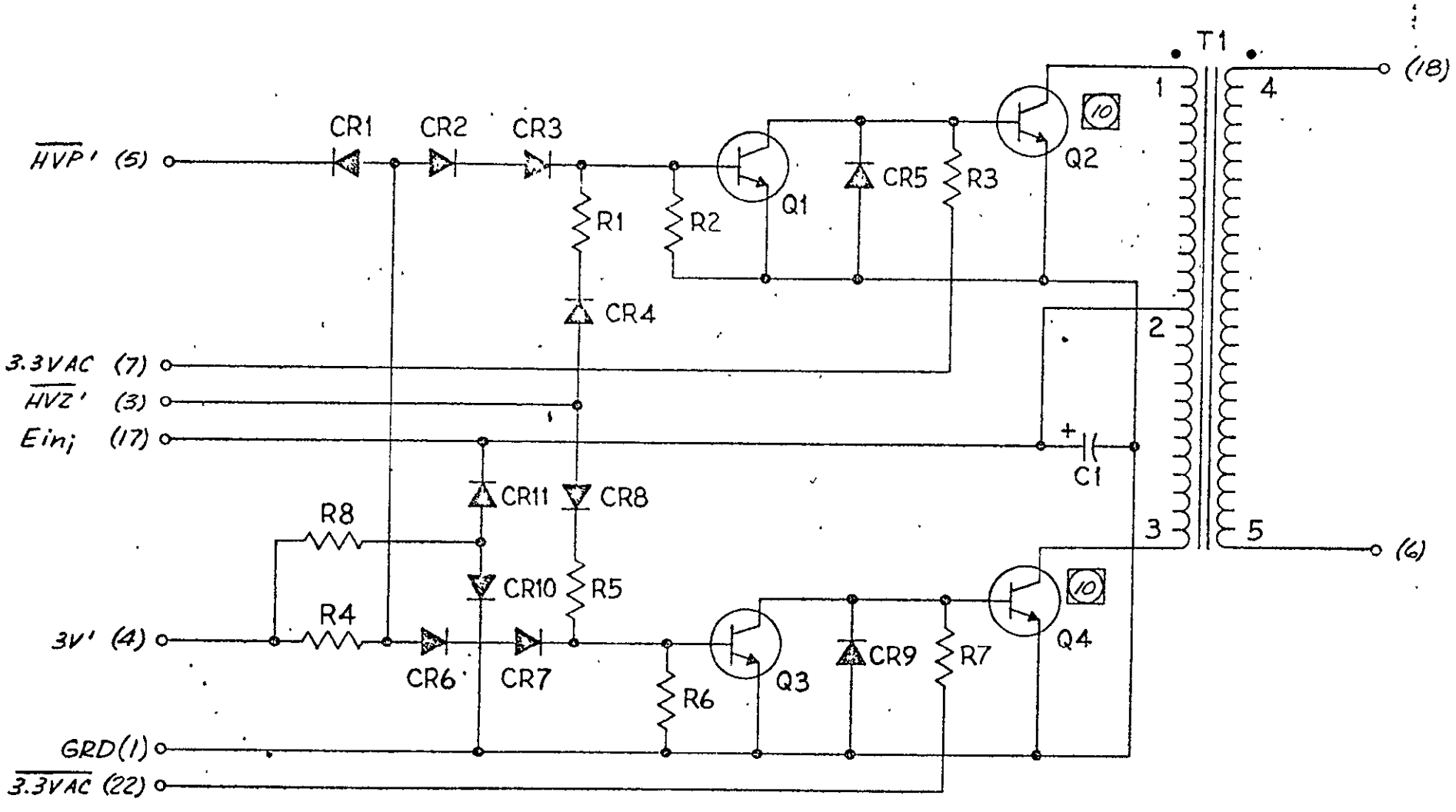
4.13.1 Chopper

The chopper converts the d-c from the d-c amplifier into an a-c signal. The output of the choppers is a 5KHz square wave. The chopper can be cut off with $\overline{HVP}$ signal and the $\overline{HVZ}$ signal. The output of the chopper is fed into a transformer which steps up the voltage from the chopper. See schematic, Figure 4.13.1 -1.

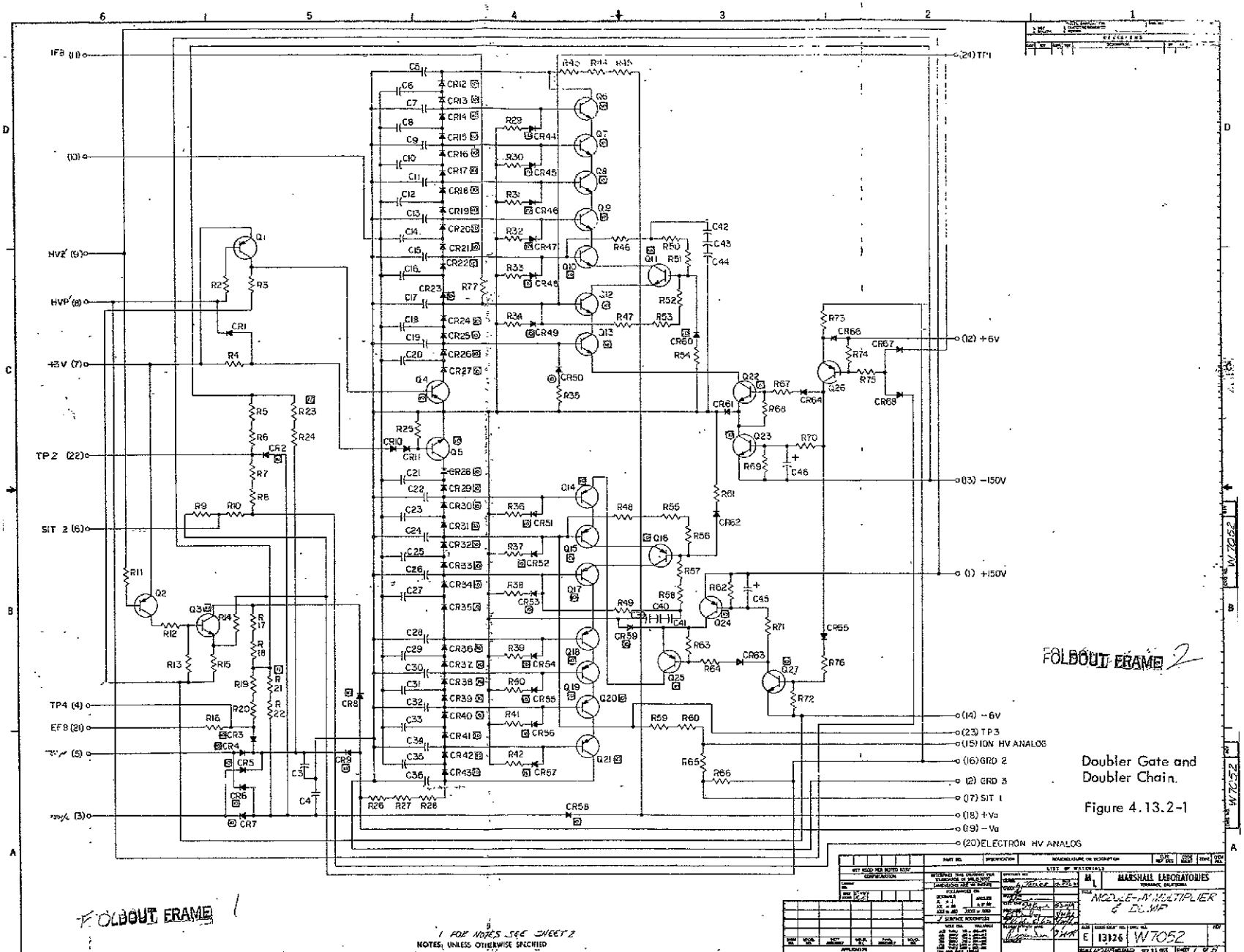
In normal operation, transistors Q_2 and Q_4 are switched ON and OFF due to the 3.3 VAC applied to their respective bases, allowing current to flow through the primary winding of transformer T_1 and inducing a voltage in the secondary. This voltage is stepped up by a ratio of 7.8 to 1. Transistors Q_1 and Q_3 are being held OFF during this time, since CR_1 is reverse biased. When $\overline{HVP}$ changes state, CR_1 becomes forward biased, turning ON transistors Q_1 and Q_3 and turning OFF Q_2 and Q_4, regardless of the state of the complimentary signals 3.3 VAC and $\overline{3.3\ VAC}$.

4.13.2 Doubler Gate and Doubler Chain

See Figure 4.13.2-1 for the schematic diagram.

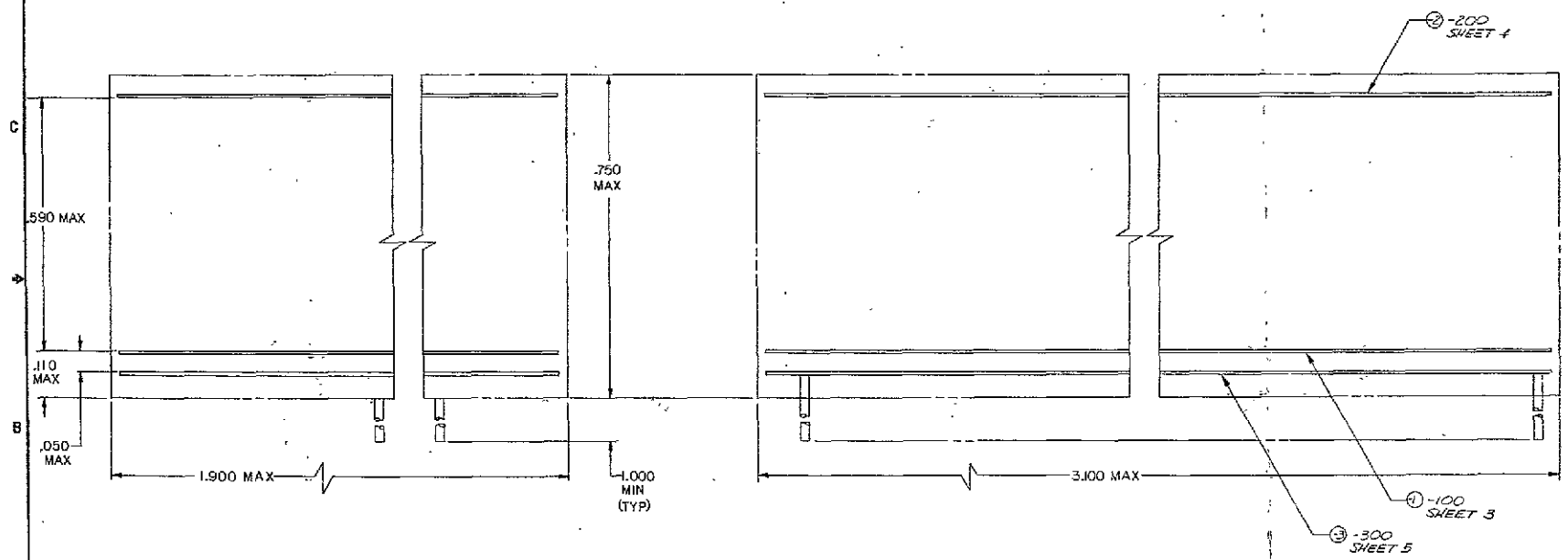


Chopper Schematic Diagram
Figure 4.13.1-1



Doubler Gate and Doubler Chain.

Figure 4.13.2-1



12. O INDICATES WELDED RISER. DO NOT PUNCH WAFER.
11. SELECTED AT MODULE TEST PER SH6176
10. SELECTED PRIOR TO FABRICATION PER SH6S7
9. FOR TEST SPEC NO. SEE ITEM NO. 7
8. CORRELATE REF DESIGNATIONS TO FIND NO. BY LIST OF MAT'L
7. REDUCE DWG SO REDUCTION DIM SCALES 3.100±.005 REPRODUCE IN BLACK ON .007 MYLAR
6. SEE SEPARATE LIST OF MAT'L
5. NO. NEXT TO WELD IS FOR REF ONLY
4. ⊖ INDICATES FEEDTHRU
3. ● INDICATES COMPONENT LEAD
2. ⊕ INDICATES EXTERNAL MODULE LEAD
1. ASSEMBLE PER ITEM NO. 6

NOTES: UNLESS OTHERWISE SPECIFIED

WELD NO. USED	DELETED
-100	
-200	

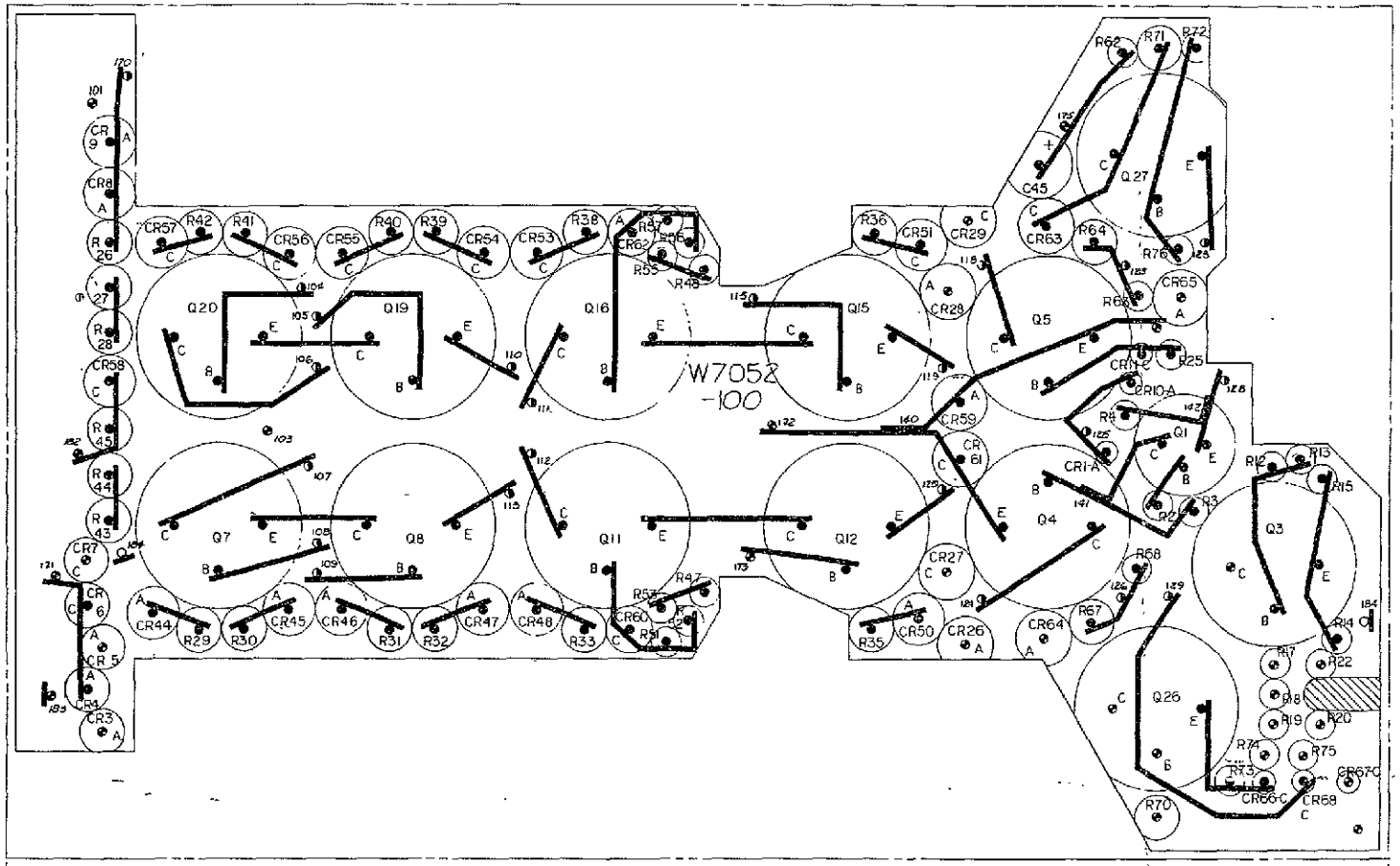
FOLDOUT FRAME

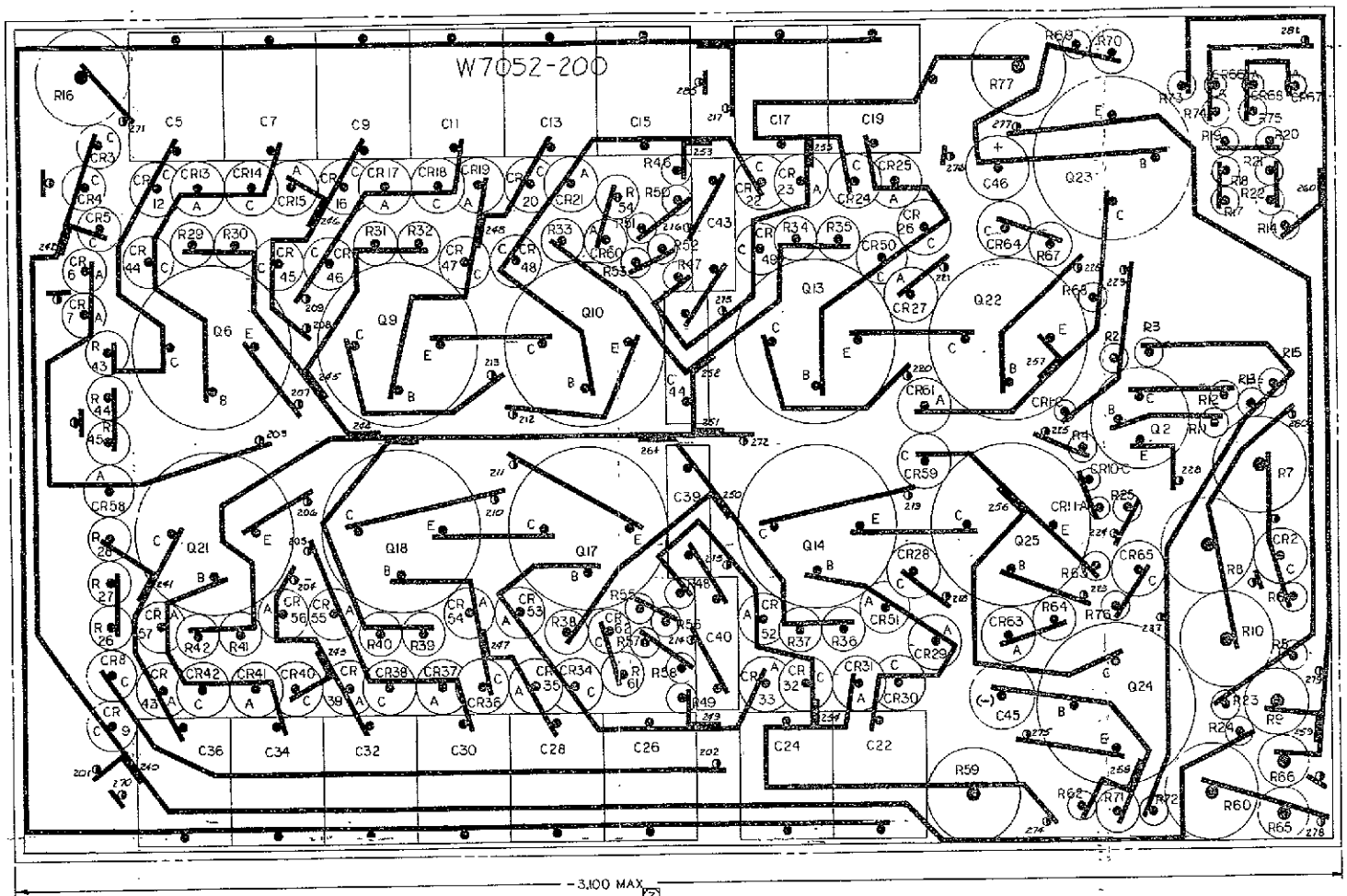
FOLDOUT FRAME 2

SIZE	CODE IDENT NO.	DWG NO.	REV
F	13126	W7052	
SCALE 10/1	RELEASED SEP 21 1966	SHEET 2 OF 5	

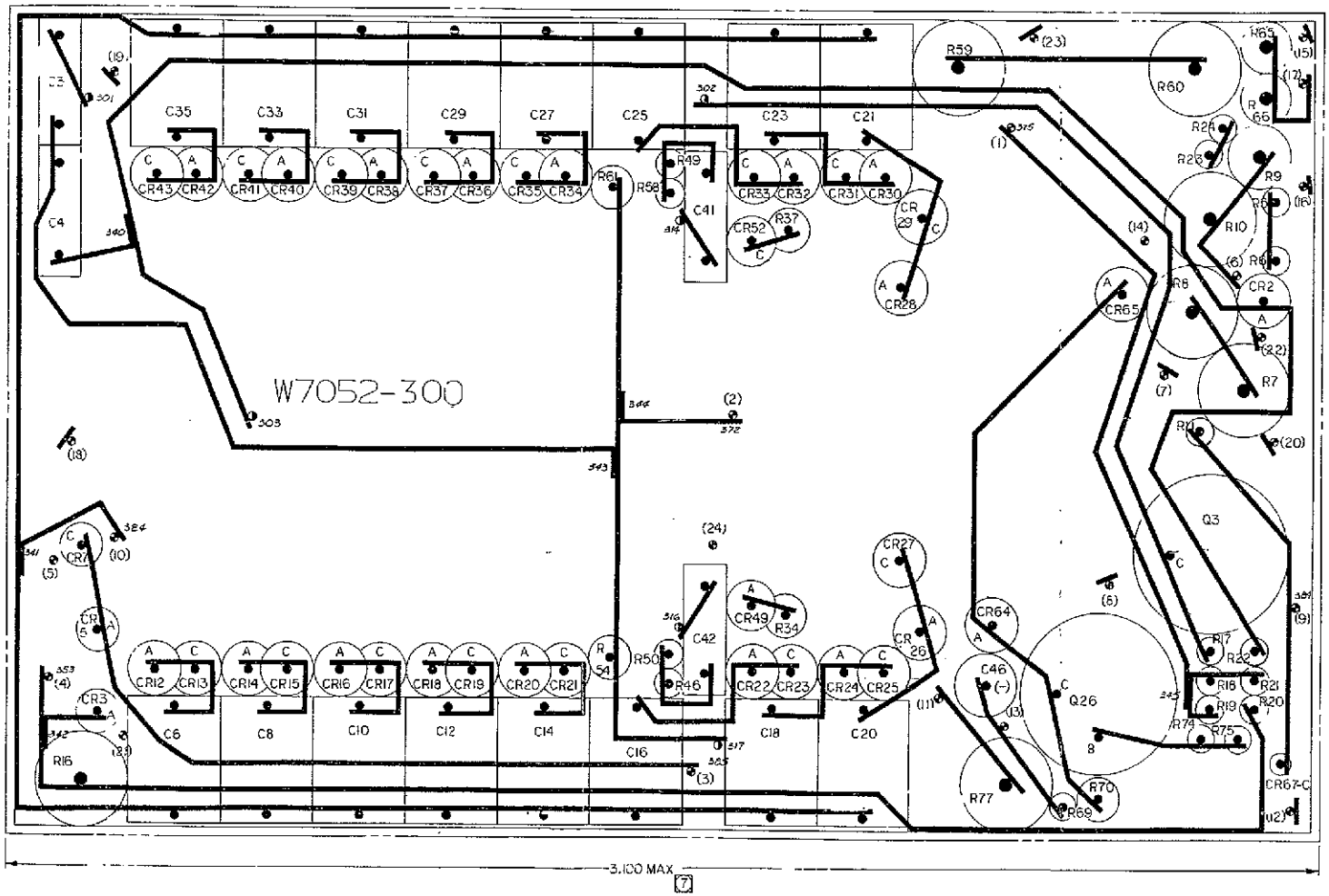
W7052 REV

W7052 REV


W7052
-100
3.100 MAX
FOLDOUT FRAME
FOLDOUT FRAME 2
-100
F 13126 W7052



SIZE	CODE IDENT NO.	DWG NO.	REV
F	13126	W7052	
SCALE 10/1	RELEASED	SHEET 2 OF 3	



SIZE	CODE IDENT NO	DWG NO	REV
F	13126	W7052	

SCALE 10/1 RELEASED SHEET 5 OF 5

During Ion mode, transistors Q_4 and Q_5 are turned ON. The Doubler circuit operates by charging C_{20}, during one half cycle, through CR27 to the transformer peak potential. During the next half cycle, C19 through C26 are charged to the potential determined by that across C20 and the transformer in series. An eight-fold multiplication is provided in this matter to produce +VA. -VA is produced by charging C21 through CR28 and C22 through CR29, and so on.

During the Electron mode Q_4 and Q_5 are turned OFF thereby disabling the doubler circuits.

4.13.3 Dump Circuitry

Refer to schematic, Figure 4.13.2-1.

The doubler chain is discharged by the Dump circuitry. The operation of the Dump circuit is as follows: On receipt of a signal from HVP' or HVZ', the Dump gate turns on the Trickle Dump circuit. A delay is provided such that the Dump and Reversal circuit does not turn on. The Trickle dump circuit causes a slow exponential discharge of the doublers. Dump switch 8 will discharge doubler No. 8. After doubler No. 8 is discharged, dump switch 7 will cause doubler No. 7 to discharge; this action is repeated until doubler No. 1 is discharged. Approximately 250 milliseconds after the dump gate has turned on, the dump and reversal circuit will cause (1) speed up of dumping, (2) a -150 volts to appear at the input to the +VA coupler and +150 volts to appear at the input to the -VA coupler.

With HVZ' and HVP' applied to the cathode of CR67 and CR68, these diodes become forward biased and start conducting; with R74 and R75 as a divider network, the voltage at the base of transistor Q_{26} is about 3 volts. At this time transistor Q_{26} is turned ON, turning ON transistors Q_{22}, Q_{27}, and Q_{25}. Q_{23} and Q_{24} turn ON with a time delay T equal to $R_{70} C_{46}$.

When Q_{22} turns ON, the sequential turn-on of transistors Q_{13} through Q_6 occurs. By this time, Q_{23} turns ON and its collector potential rises to approximately -150 volts. This voltage appears at the collector of Q_6 and is attenuated by the resistors R43, R44 and R45. At the same time the +150 volts applied to resistors R21 and R22 is attenuated and is applied to +VA through CR58. This voltage is about +100 millivolts. Similarly, Q_{25} starts the sequential turn-on of transistors Q_{14} through Q_{21}. A potential of +150 volts appears at the collector of Q_{21} and is attenuated by resistor R26, R27 and R28. At the same time Q_3 turns ON and a negative potential of about -4 volts is applied to -VA through CR8.

When HVZ' and HVP' change state, CR67 and CR68 become reverse biased and transistor Q_{26} is in the OFF condition, holding all other transistors in the dump circuit OFF.

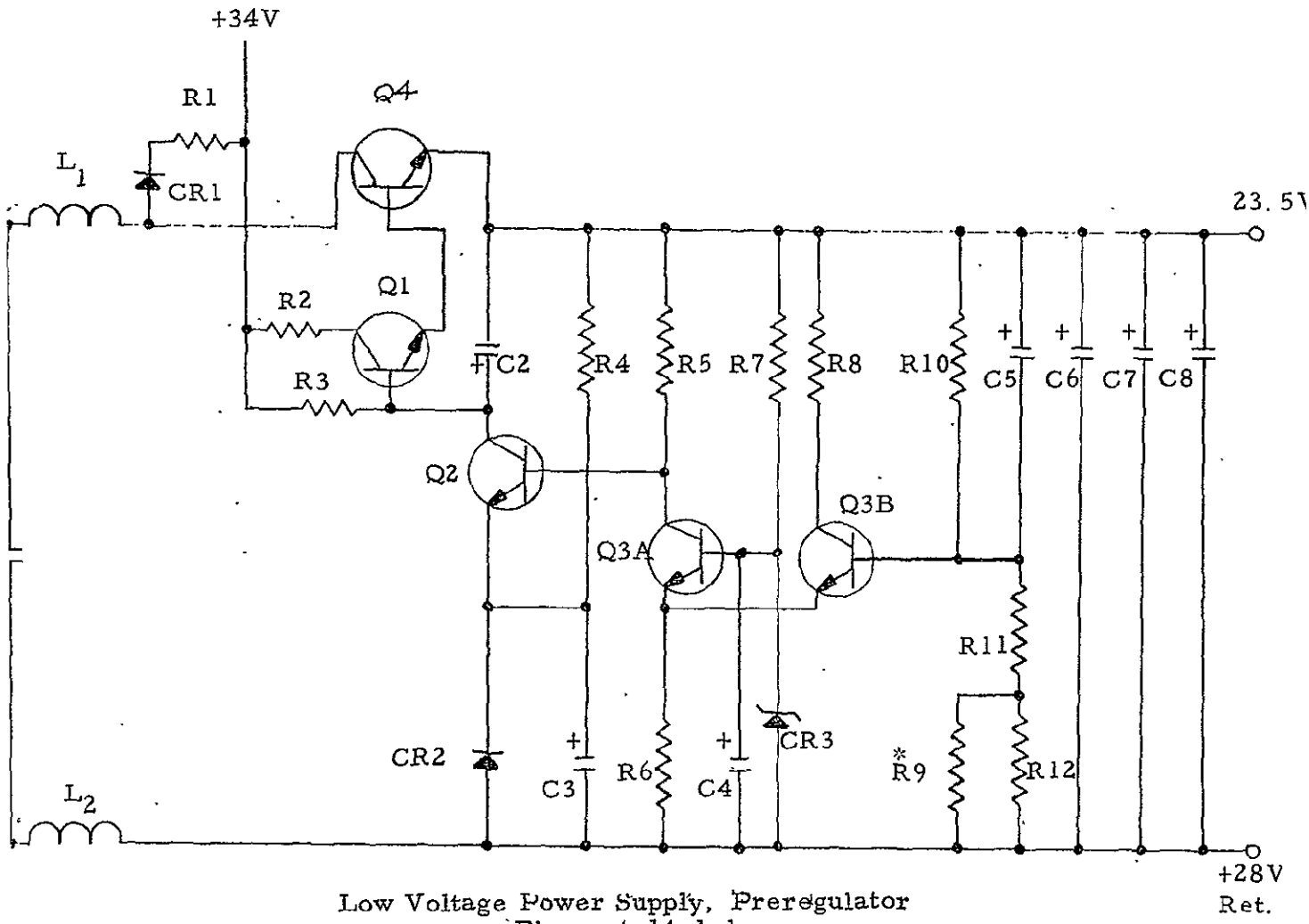
4.14 Low Voltage Power Supply

4.14.1 Pre-regulator

Refer to Figure 4.14.1-1 for the schematic diagram of the Low Voltage Power Supply Pre-regulator.

The Pre-regulator consists of a series voltage regulator that provides a stable operating voltage to the chopper, ensuring reliable operation. CR3, a zener diode, provides the reference voltage to Q_3, a differential amplifier. Q_3 drives transistors Q_2 and Q_1. The voltage divider network R_{10} and R_{11} is selected to set the output voltage to 23.5 volts d-c. The collector voltage supply, +34 volts, for Q_1 and Q_2 is provided by an isolated source which is higher than that of Q_4.

The higher potential allows Q_4 to operate at a low collector voltage which minimizes power loss.



Low Voltage Power Supply, Preregulator
Figure 4.14.1-1

$Q_1 = Q_2$ = ML20002
Q_3 = 2N4042
CR_1 = 1N649
CR_2 = 1N695
CR_3 = FCT 1121
$L_1 = L_2$ = 1000 μh
R_1 = 5.1K
R_2 = 2.4K
R_3 = 82K
R_4 = 120K
R_5 = 820K
R_6 = 332K
R_7 = 165K
R_8 = 820K
R_9 = Select
R_{10} = 165K
R_{11} = 63.4K
R_{12} = 6.81K
$C_1 = C_2 = C_3 = C_5$ = 1μf
C_4 = 3.3 μfd
$C_6 = C_7 = C_8$ = 4.7 μfd

In order to stay within the spacecraft's turn-on surge current requirements, the inductors L_1 and L_2 are introduced into the circuit.

4.14.2 Chopper

The function of the Chopper is to convert the +23.5Vdc output from the Pre-regulator into a 5KHz square wave.

See Figure 4.12.2-1 for the Chopper schematic diagram.

Upon turn-on, +23.5 volts is applied to the emitter of Q1 and pin 5 of T_2. Since the circuit has been OFF, there is no voltage across C_1, hence Q_1 turns ON and drives current into the base of Q_2, turning Q_2 ON. Q_2 saturates and holds pin 4 of T_2 at about ground potential while pin 6 of T_2 rises to 47 volts. This 47 volts induces a voltage equivalent to

$$\frac{47}{2} = 23.5 \text{ volts}$$

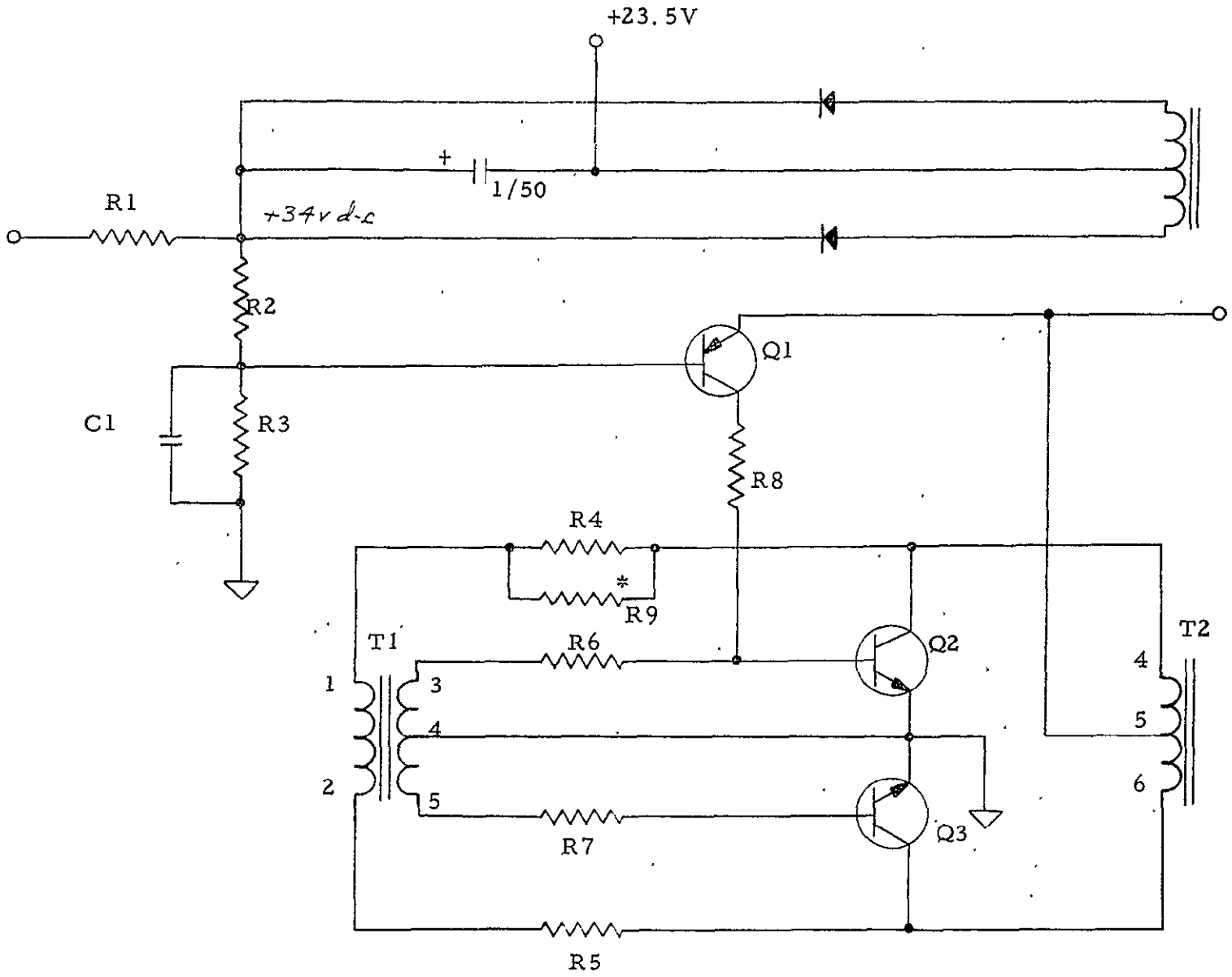
between pins 1 and 3 of T_2, or

$$\frac{23.5}{2} = 11.75 \text{ volts}$$

from center tap, pin 2 to either pins 1 and 3. Since the center tap is held to a fixed potential, 23.5 volts, the total rectified voltage is now

$$23.5 + 11.75 = 34.25 \text{ volts}$$

This voltage, applied to the divider network formed by R2 and R3, charges the capacitor C1 to about 25 volts which is applied to the base of Q_1 and turns it OFF. This process insures a "sure-start" of the chopper circuit.



Low Voltage Power Supply Chopper,
Schematic Diagram
Figure 4.14.2-1

The +47 volts appearing across pins 4 and 6 of T_2 are coupled via R4 and R5 to pins 1 and 2 of T_1 (the feedback winding). This voltage induces a potential at pins 3 and 5 such that the polarities at pin 1 and 5 are the same and the polarities of pins 1 and 3 are reversed. The induced voltage turns ON Q_3 and turns OFF Q_2. This removes the short to ground at pin 4 of T_2, causing the voltage at pin 4 to rise towards +23.5 volts and the voltage at pin 6 of T_2 to drop towards +23.5 volts. This couples a step voltage to the feedback winding of T_1 of such polarity that Q_3 cuts OFF and Q_2 turns ON. Q_2 goes into saturation and the cycle continues. The frequency of oscillation is regulated closely by R4 and R5. A select resistor R9 in parallel with R4 acts as a fine tuning resistor.

4.14.3 Post-regulators

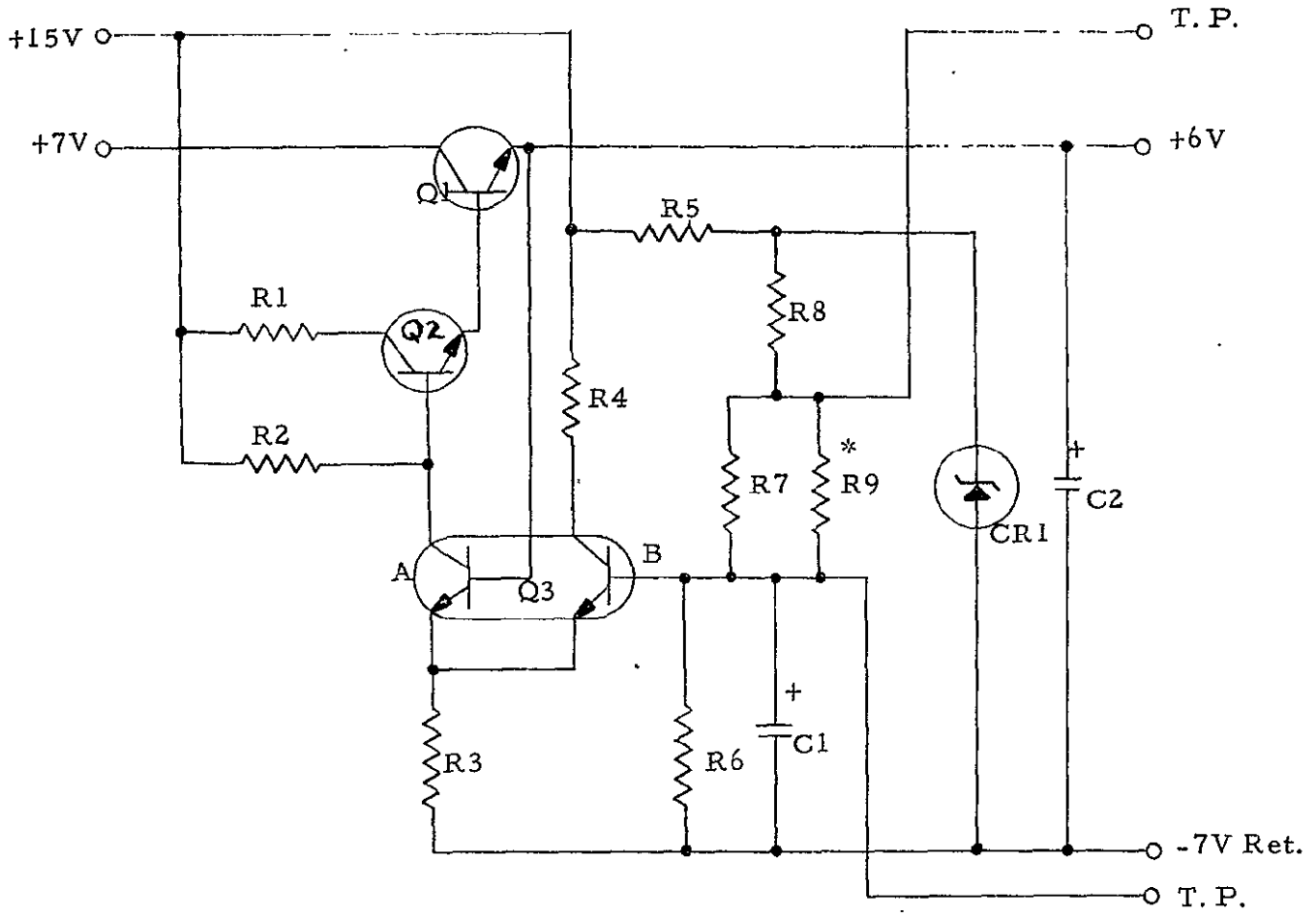
The Post-regulators each consist of a series voltage regulator providing stable operating voltages to the system. They are similar in operation to the Pre-regulator (see Section 4.14.1).

The following figures show the indicated post-regulator schematics:

Figure	Post-regulator
4.14.3-1	+ 6v
4.14.3-2	- 6v
4.14.3-3	+12v
4.14.3-4	+15v
4.14.3-5	-25v

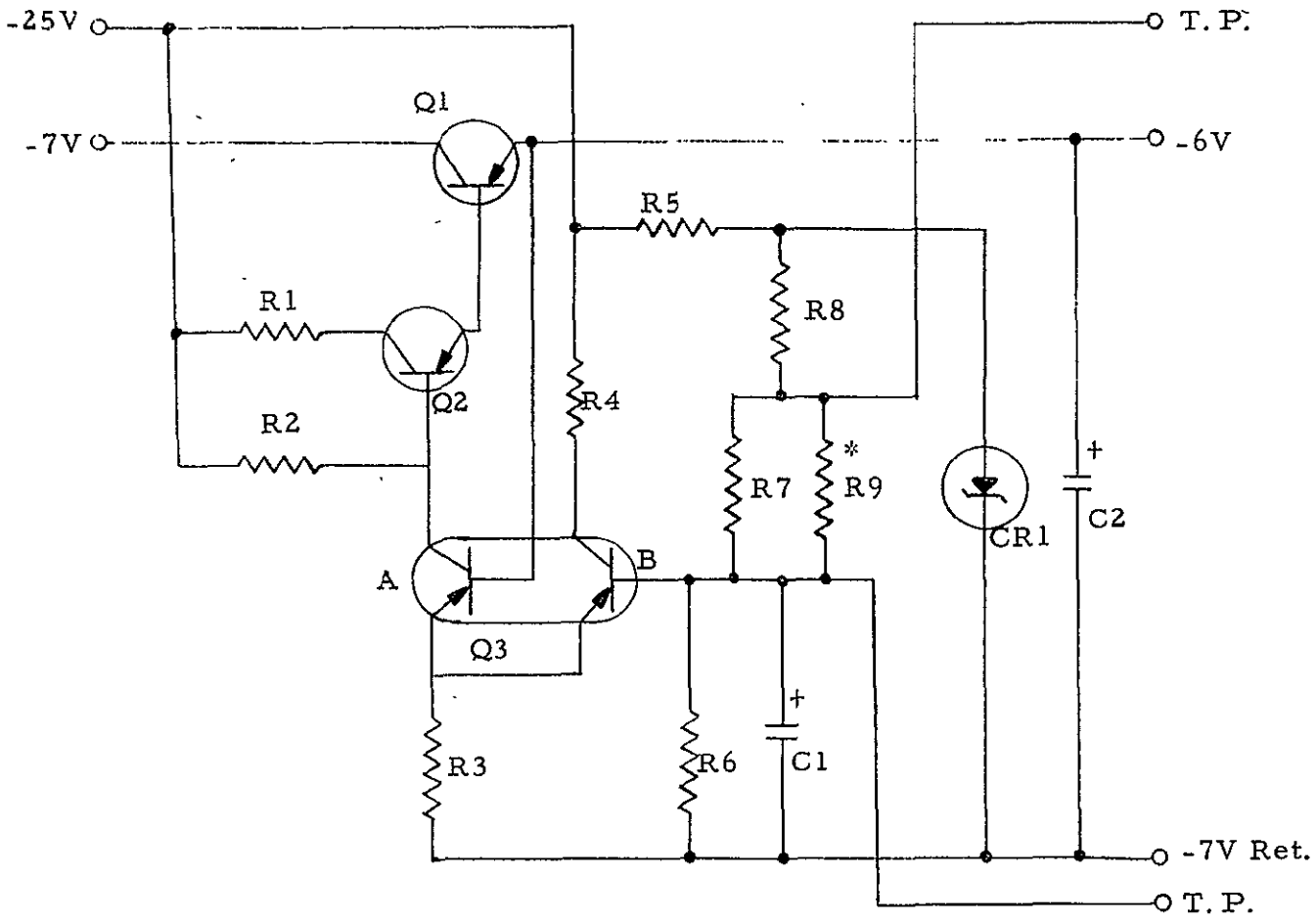
4.14.4 Filament Power Supply

The input to the Filament Power Supply is the 3.3 VAC generated by the Low Voltage Power Supply. See Figure 4.14.4-1 for the schematic diagram.



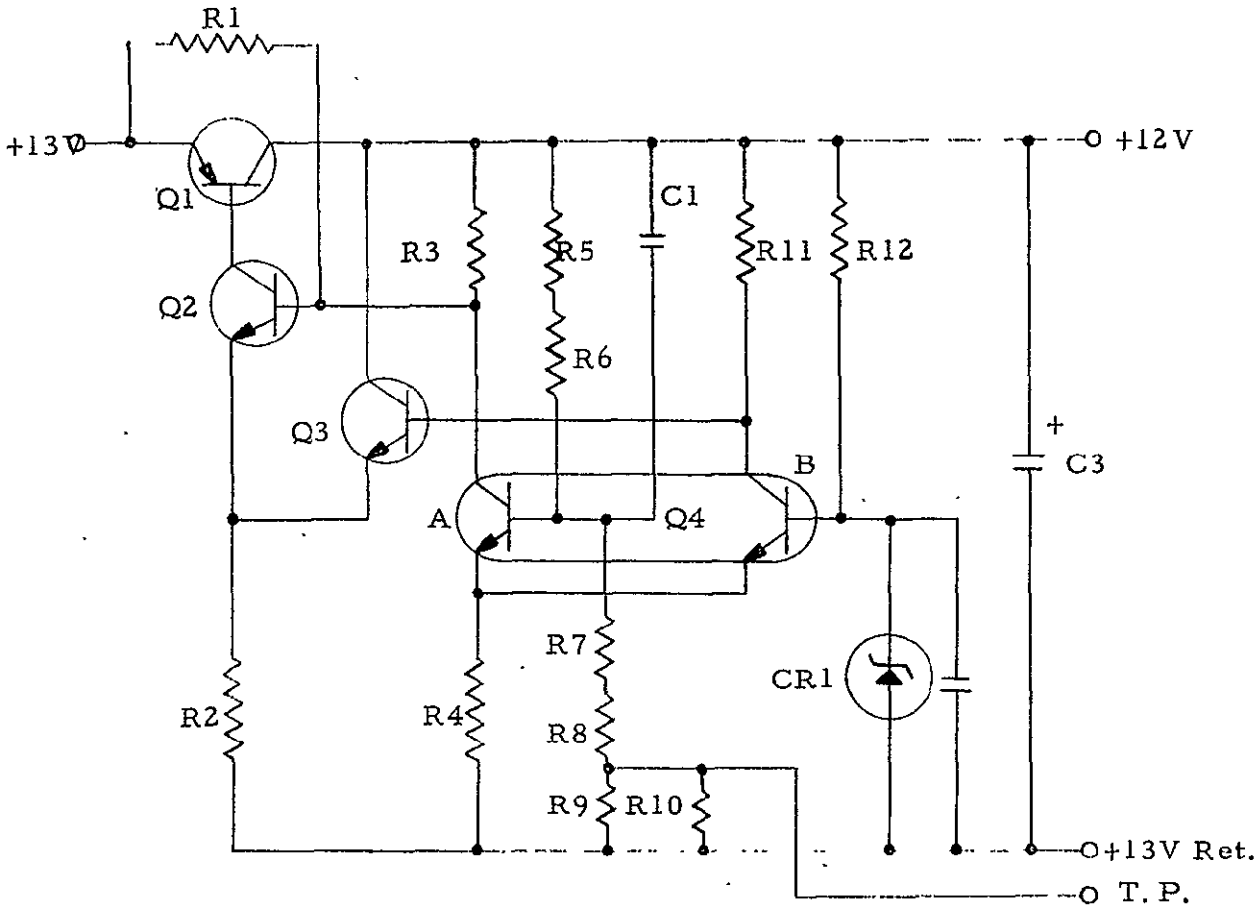
$Q_1 = Q_2$ = ML002
Q_3 = 2N4042
R_1 = 27K
R_2 = 160K
R_3 = 54.9K
R_4 = 91K
R_5 = 51.1K
R_6 = 100K
R_7 = 11K
R_8 = 6,.19K
R_9 = Select
CR1 = FCT1121
C_1 = 1μfd
C_2 = 22μfd

+6v Post-regulator
Figure 4.14.3-1



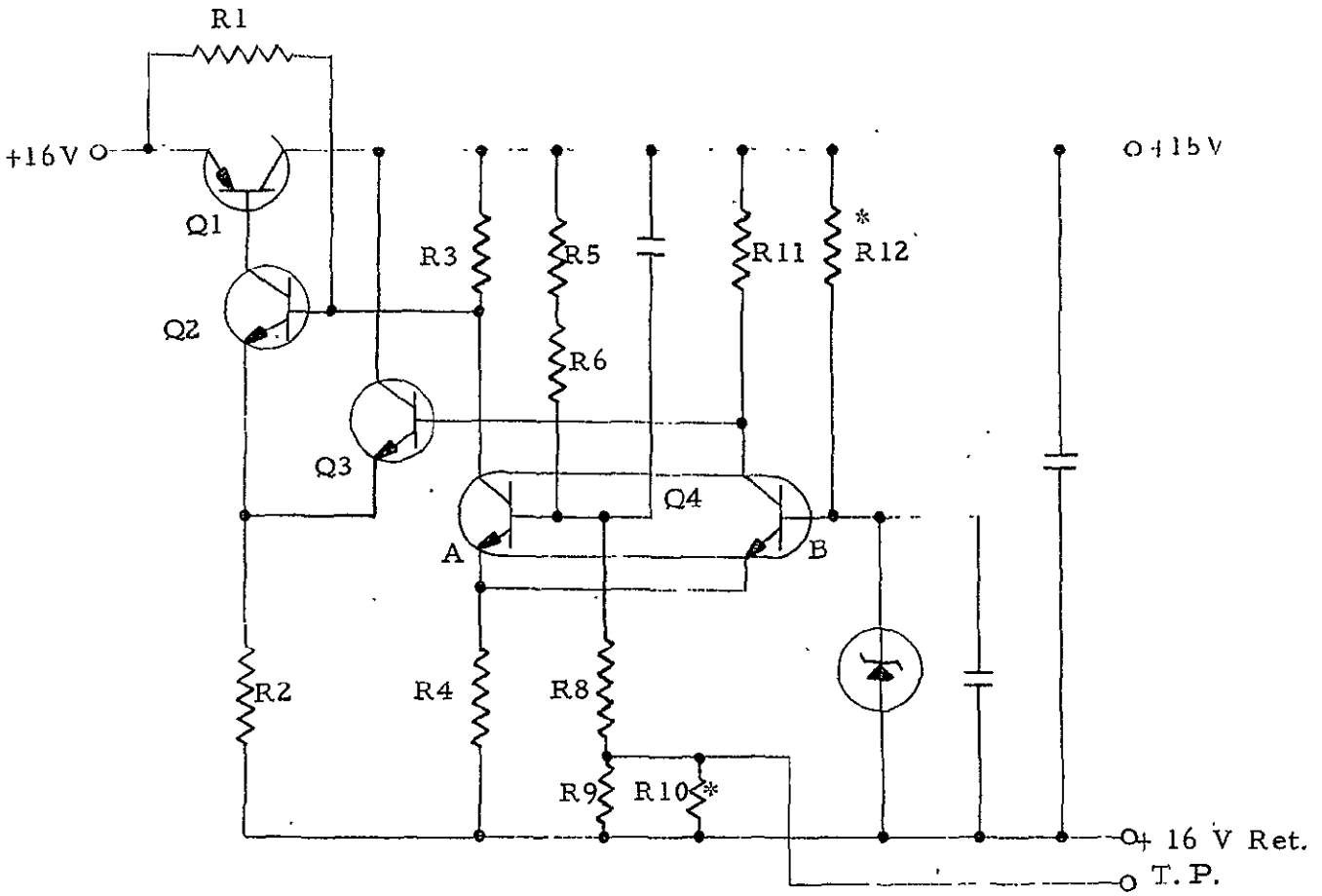
$Q_1 = Q_2$ = ML001
Q_3 = 2N4024
CR1 = FCT1121
R_1 = 62K 5%
R_2 = 360K 5%
R_3 = 54.9K 1%
R_4 = 200K 5%
R_5 = 100K 1%
R_6 = 75K 1%
R_7 = 8.25K 1%
R_8 = 4.75K 1%
R_9 = Select
C_1 = 1 μfd/50V
C_2 = 22 μfd/50V

-6v Post-regulator
Figure 4.14.3-2



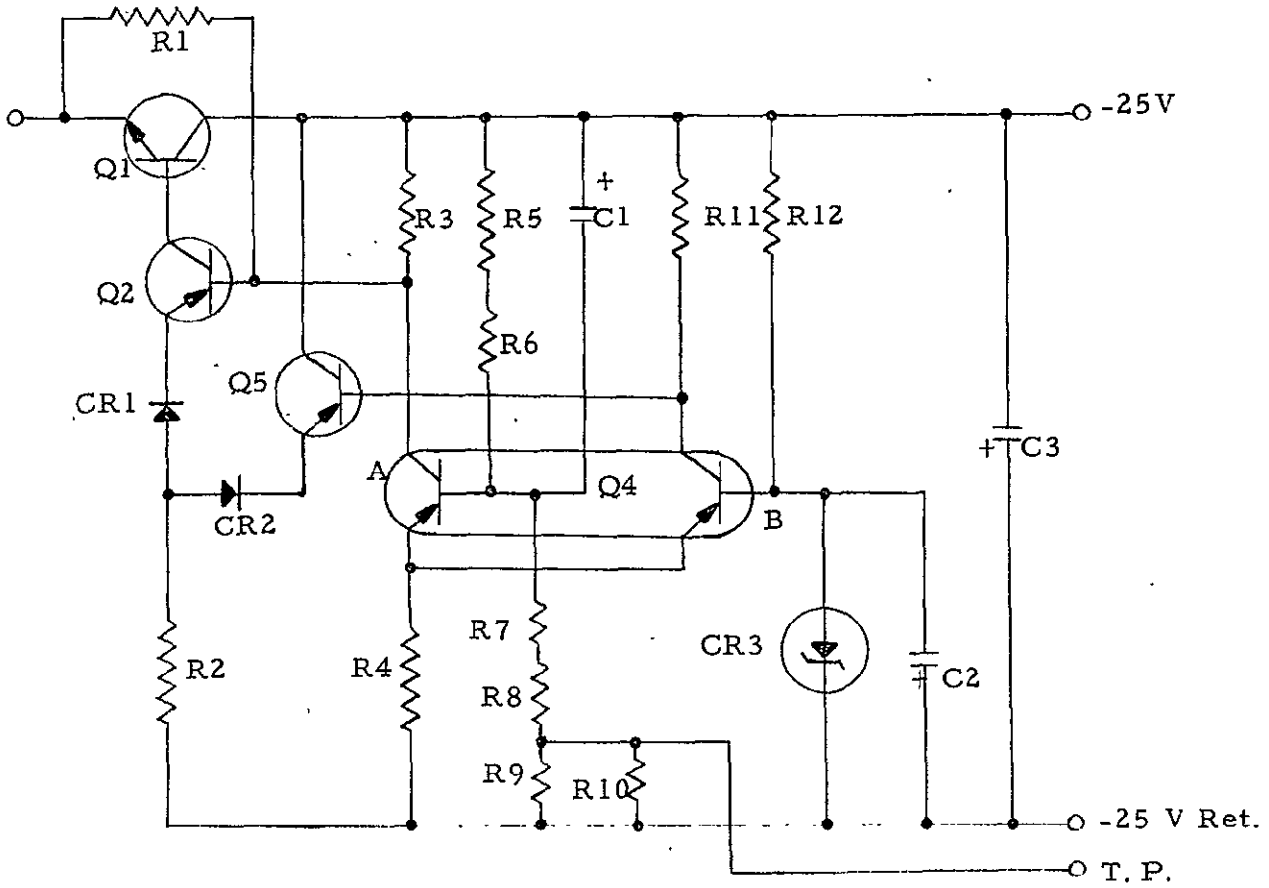
Q_1 = ML001
$Q_2 = Q_3$ = ML002
Q_4 = 2N4042
CR_1 = FCT 1121
R_1 = 820K 5%
R_2 = 30K 5%
R_3 = 120K 5%
$R_4 = R_{11}$ = 100K 5%
$R_5 = R_7$ = 100K 5%
R_8 = 110K 1%
R_9 = 21K 1%
R_{12} = 51K 5%
R_{10} = Select
R_6 = 6.81K 1%
C_1 = 1 μfd/50V
C_2 = 2.2 μfd/50
C_3 = 6.8 μfd/35

+12v Post-regulator
Figure 4.14.3-3



Q_1 = ML001	R_4 = 82K 5%	R_{12} = Select
$Q_2 = Q_3$ = ML002	R_5 = 100K 1%	C_1 = 1 μfd/50V
Q_4 = 2N4042	R_6 = 200K 1%	C_2 = 3.3 μfd/15V
CR1 = 1N752A	R_8 = 82.5K 1%	C_3 = 6.8 μfd/35V
R_1 = 1M 5%	R_9 = 18.2K 1%	
R_2 = 47K 5%	R_{10} = Select	
R_3 = 200K 5%	R_{11} = 160K 5%	

+15v Post-regulator
Figure 4.14.3-4



Q_1 = ML000

$Q_2 = Q_3$ = ML001

Q_4 = 2N4024

CR2 - CR1 = SP30265

CR3 = FCT1121

R_1 = 2M 5%

$R_2 = R_{11}$ = 300K 5%

R_3 = 360K 5%

R_4 = 100K 5%

R_5 = 301K 1%

R_6 = 200K 1%

R_7 = 100K 1%

R_8 = 78.7K 1%

R_9 = 17.8K 1%

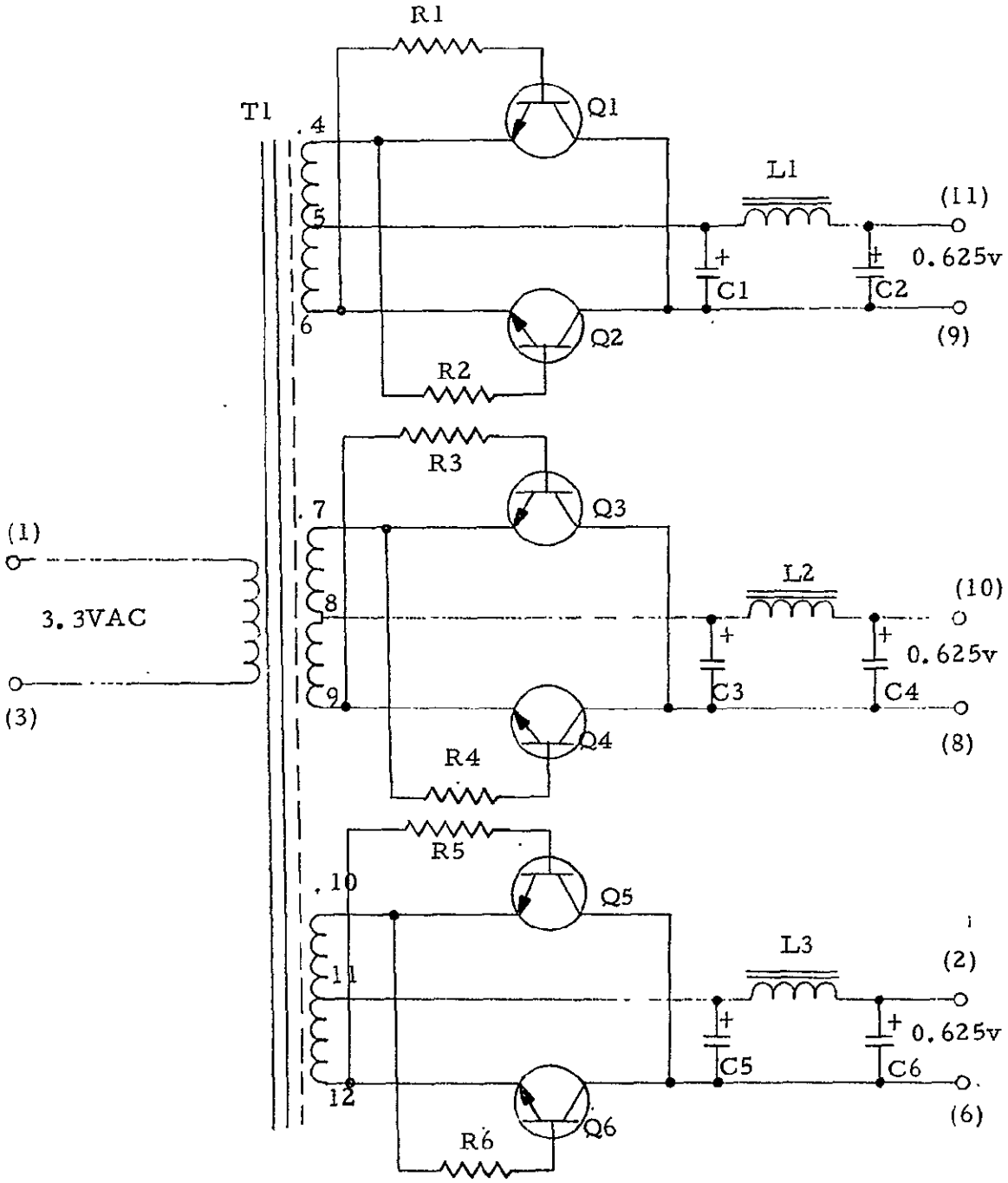
R_{10} = Select

C_1 = 1 μfd/50V

C_2 = 2.2 μfd/20V

C_3 = 4.7 μfd/15V

-25v Post-regulator
Figure 4.14.3-5



Filament Power Supply Schematic
Figure 4.14.4-1

Synchronous rectifiers are used for greater efficiency and lower power dissipation. The three outputs are each 0.625 volts.

The operation of the Synchronous Rectifier is as follows:

When 3.3 VAC is present at pin 1 of T_1, pin 4 goes negative and pin 6 goes positive. This in effect makes the base of Q_1 positive with respect to its emitter; therefore, Q_1 saturates. Q_2 is kept OFF because its emitter is positive with respect to its base. Current flows from pin 5 of T_1 through the filter and back to pin 4 through Q_1. In the next cycle, the reverse occurs and current flows from pin 5 of T_1 through the filter and up to pin 6 through Q_2. The operation is similar for the other two rectifier sections.

4.15 Reliability Analysis

A Reliability Analysis report for the ARC Plasma Probe can be found in Appendix F.

5.0 NEW TECHNOLOGY

5.1 Reporting Organization: Time-Zero Corporation, 3530 Torrance Boulevard, Torrance, California 90503.

5.2 Contract Number NAS 2-3374.

A "Reportable Item" is any innovation, invention, improvement or discovery conceived or first reduced to practice in performing work under the above identified NASA contract and includes (but is not limited to) any new or improved product, device, material, process or method and should be promptly reported to the Contractor's New Technology Representative.

The questions below are not intended to limit information regarding the Reportable Items; however, it must be complete enough for others to fully understand the disclosures and its implications and possible applications.

5.3 Title of Disclosure: Wide Dynamic Range Logarithmic Pulse Width Modulator for an Electrometer Amplifier Application.

5.4 Brief (Abstract) Description: A low power Logarithmic Pulse Width Modulator, (LPWM) was developed into flight hardware for the Pioneer 8 and 9 Plasma Probe instruments. This LPWM converted the analog output of an electrometer amplifier whose output ranged from 3.3 mv to 22 volts. An additional complexity was required to compensate for the piecewise linear compression of the electrometer amplifier which was necessitated by its dynamic range of 5 orders of magnitude (10^{-14} to 10^{-9} amps). This amplifier was reported as a New Technology item in NASA TECH Brief 67-10199.

5.5 Description (Attach sheets as required)

A. Give complete information in the following order:

(1) General purpose of the item.
(2) Improvement and/or advantages over prior methods, materials, or devices.
(3) Detailed description including as applicable the explanation of the principle of operation: details of the preparation of the process and/or materials; technical data, drawings, and sketches. These should be included as required to fully describe the Item. Include reference drawings, specifications, technical reports, test reports, and other technical information which will be useful in the evaluation of the Disclosure. (If a document containing excerpts of the requested description exists, it may be attached to meet this requirement).
(4) Features of the Item believed to be new.
(5) Additional information to more fully describe Item.
(6) Does the contractor intend to file a patent application?

_____ Yes _X_ No _____ TBD

B. Identify any previous publication of the Disclosure.

None ___X___ See attached sheet _____

C. List publications pertaining to this Item and where they may be obtained.

None _____ Final Engr. Report for NAS 2-3374.

5. 6. Applications: Include possible industrial and other non-aerospace uses. Identify specific industries, processes, or products in which the Reportable Item might find application or to which it might be related.

The LPWM could find application where A/D conversion of wide range analog signals is required for data-logging or transmission particularly where power is at a premium, e.g. in unattended oceanography instrumentation.

5. 7. What are possible extensions of this Item: This design could be extended to operate over wider input dynamic ranges and could also be extended to reliable conversions of greater than seven bits.

5. 8. Degree of Development. Check applicable stage:

_____ Concept only _____ Development complete[illegible] available

___X___ Limited production _____ Other-Remarks _____

5. 9. Technological significance: In relation to the present state of technology, this Reportable Item is considered to be a:

_____ Major improvement _____ Substantial advance in the art _____

Design improvement ___X___

5.10. Optional-Publication of Reportable Items

It appears at this time that publication of this reportable item:

a. ___X___ would be of value to the Aerospace Industry

b. ___X___ would be of value outside the Aerospace Industry. If so, one or more of the following are recommended:

(1) _____ a multiple-page Contractor Report

(2) _____ a brief draft of a scientific Journal Announcement

(3) ___X___ a brief announcement (NASA Tech Brief) for republication on a technical or trade publication

c. _____ publication is not warranted at this stage of development.

5.11. Innovator's Name(s)

Signature Dean Aalami Norman Katz Date 2/11/70

Type or print name Norm Katz Dean Aalami

5.12. Technical Supervisor of Innovator(s)

Signature Robert Kobayashi Date 2/11/70

Type or print name Robert Kobayashi

5.13. Contractor's Technology Utilization Representative

Signature William Sandstrom Date 2/11/70

Type or print name W. Sandstrom

5.5.A.(1) The purpose of the LPWM is to convert current impinging upon a target of a Solar Plasma measuring instrument into a digital signal suitable for data processing and transmission over the Pioneer spacecraft telemetry system. Only seven bits of data were available for this measurement which necessitated the logarithmic conversion since the input current had a dynamic range of five orders of magnitude (10^{-14} to 10^{-9} amps). In addition, the LPWM was designed for both positive and negative inputs since both the ions and electrons in the Solar Plasma were analyzed by the instrument.

5.5.A.(2) The system described was an improvement over previously developed systems since it enabled (together with the associated electrometer amplifier) accurate measurements of both positive and negative currents over a wider dynamic range than previously practical. This was accomplished with a minimal cost in power and weight.

5.5.A.(3) (See page following)

5.5.A.(4) The features believed to be new include the low power, the wide dynamic range and the capability of unfolding the compression of the input analog signal.

5.5.A.(5) None.

5.5.A.(3)

A simplified block diagram of the system, incorporating the LPWM, is shown in Fig 5.5-1. A quadrispherical electrostatic analyzer performs an energy analysis of the Solar Plasma with the accepted particles being focused upon a target. The current on the target is detected by an electrometer amplifier which is capable of measuring ion currents from 10^{-14}a to 10^{-9}a and electron currents from 10^{-14}a to 10^{-10}a. The gain of this amplifier is piecewise linear by allowing the feedback factor to change at an output level determined by precision zener diodes. This gain is:

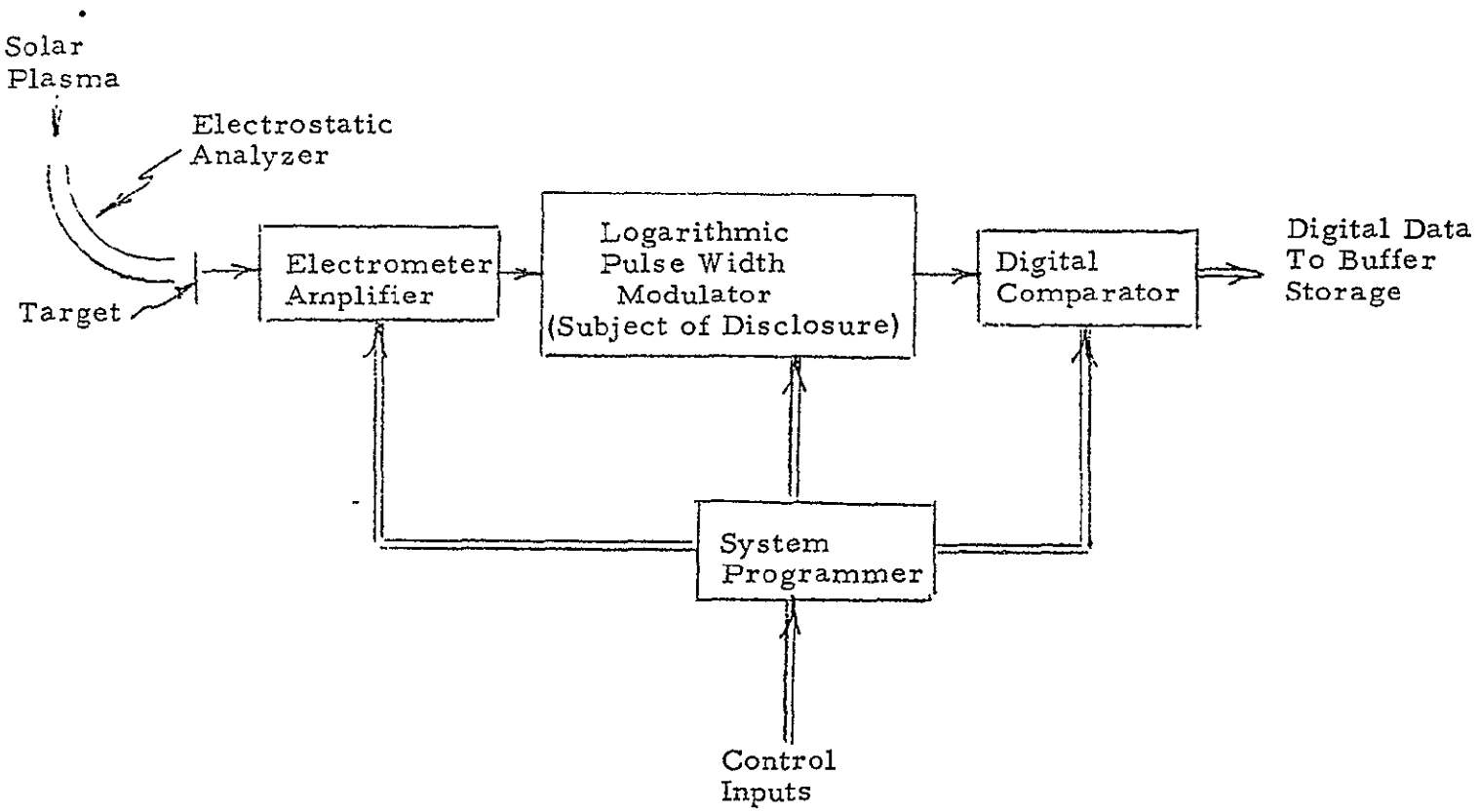
$$(1a) \quad -eo = 33 \times 10^{10}\, i_i \quad \text{for} \quad i_i < 2.1 \times 10^{-11}\text{a}$$

$$(1b) \quad -eo = 6.9 + 1.5 \times 10^{10}\,(i_i - 2.1 \times 10^{-11}) \quad \text{for} \quad i_i > 2.1 \times 10^{-11}\text{a}$$

The useful output of the electrometer, therefore, varies from about 3×10^{-3} volts to 22 volts.

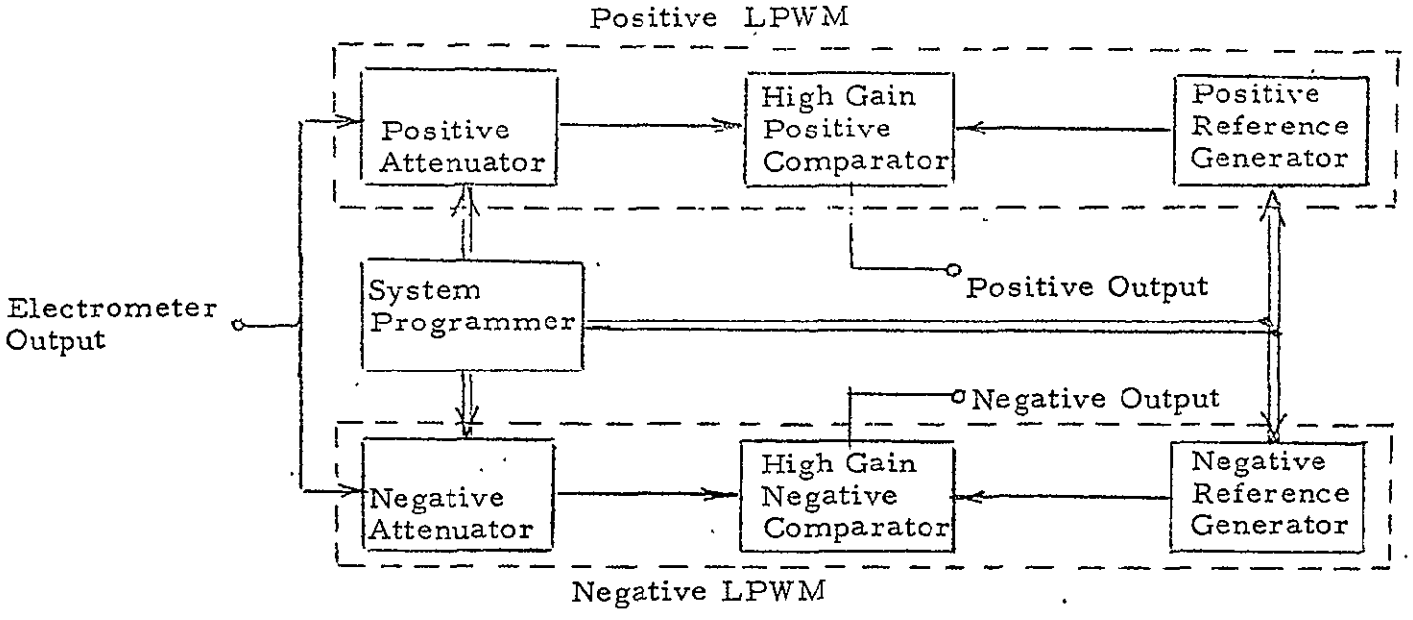
The output from the LPWM gates 82 KHz clock signals in the Digital Comparator to enable peak measurements to be performed. The output of the comparator, which is a relatively straightforward logic design, is a seven bit digital word which is transferred into an intermediate buffer storage with selected data finally shifted to a magnetic core memory for subsequent transmission over the spacecraft telemetry link.

Fig 5.5-2 shows a simplified block diagram of the LPWM. It consists of a three stage attenuator, a high gain stable comparator, a three-step logarithmic reference voltage generator, and a programmer which provides the required control and clock signals. As indicated, separate LPWM's are incorporated for negative and positive input signals.



SIMPLIFIED BLOCK DIAGRAM, LPWM SYSTEM

Figure 5.5-1



SIMPLIFIED BLOCK DIAGRAM OF LPWM

Figure 5.5-2

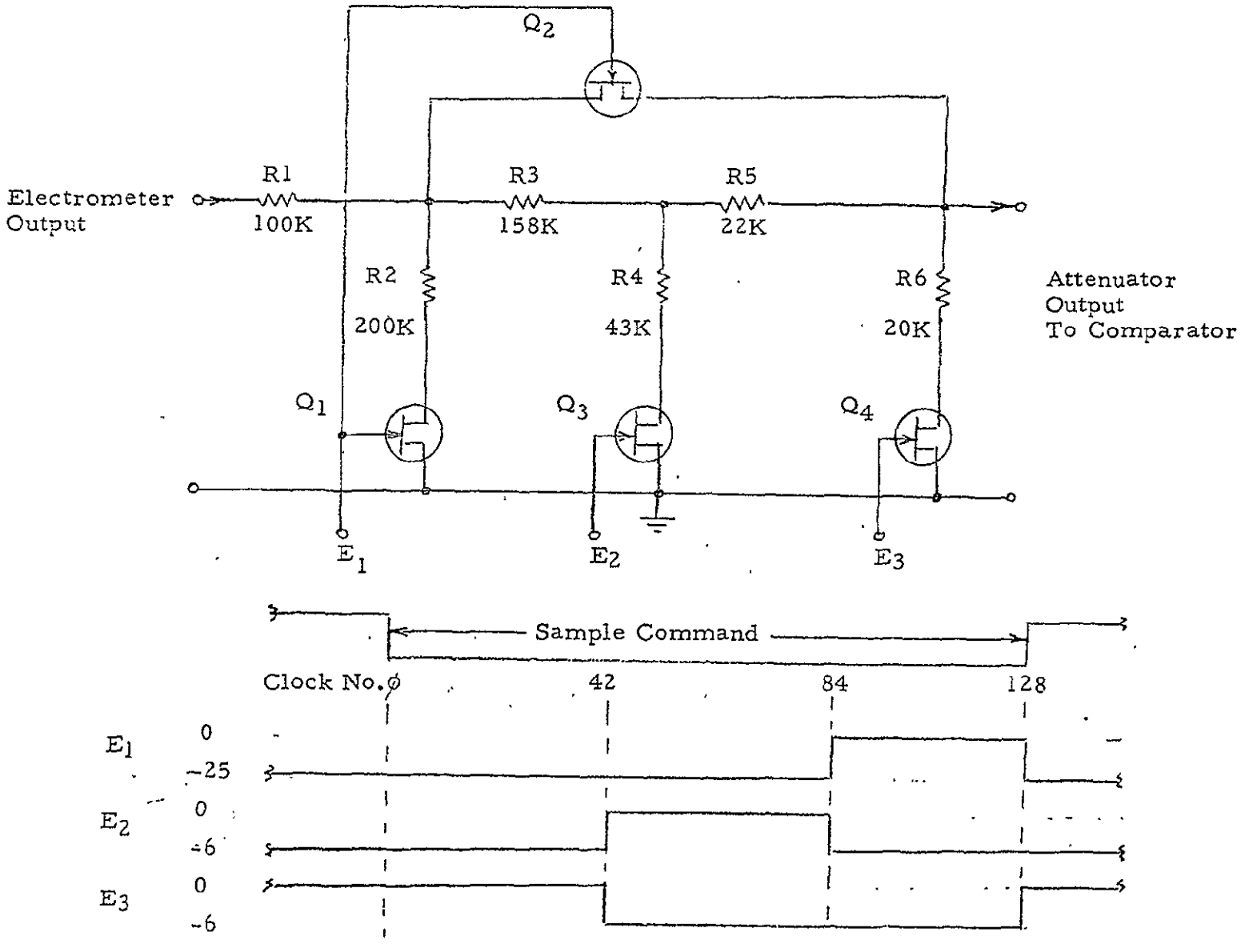
5. A. (3) (continued)

These are virtually identical in operation so further discussions will only refer to the positive LPWM.

Fig 5.5-3 shows a simplified schematic of the attenuator together with the input control signals. Prior to the start of a sample command (each 4 milliseconds) the control signal, E_3, is zero which causes Q_4 to conduct. E_1 and E_2 keep Q_1, Q_2, and Q_3 off generating a maximum attenuation of 15. This protects the comparator at all times between samples. During the first 42 of the total of 128 clock periods of the sample command, the attenuator remains in this state.

From clock pulses 43 through 84, E_2 causes Q_3 to conduct while Q_1, Q_2, and Q_4 are off. The attenuation factor during this period is 7. During clock pulses 84 through 128, Q_1 and Q_2 conduct while Q_3 and Q_4 are off for a minimum attenuation of 1.5. The function of Q_2 is to increase the accuracy when minimum input signals are being converted.

Simultaneous with the different attenuator states, the Reference Generator shown in Figure 4 generates three consecutive exponential reference levels. During the first state, Q_1, operated in the inverted mode, is turned off, allowing the +6 volts from E_1 to generate a pedestal across R_6. This pedestal compensates for the breakpoint voltage from the electrometer and has a value of approximately $6.8/15 = 0.45$ v. At the same time, C_2 causes the E_1 input to be differentiated generating a waveform shown in Fig 5. 5-4. During the second and third states, no DC pedestal is generated since Q_1 is on, therefore only the proper level of exponential reference exists at the output. The output waveform shown is drawn approximately to scale.



ATTENUATOR SCHEMATIC & TIMING

Figure 5.5-3

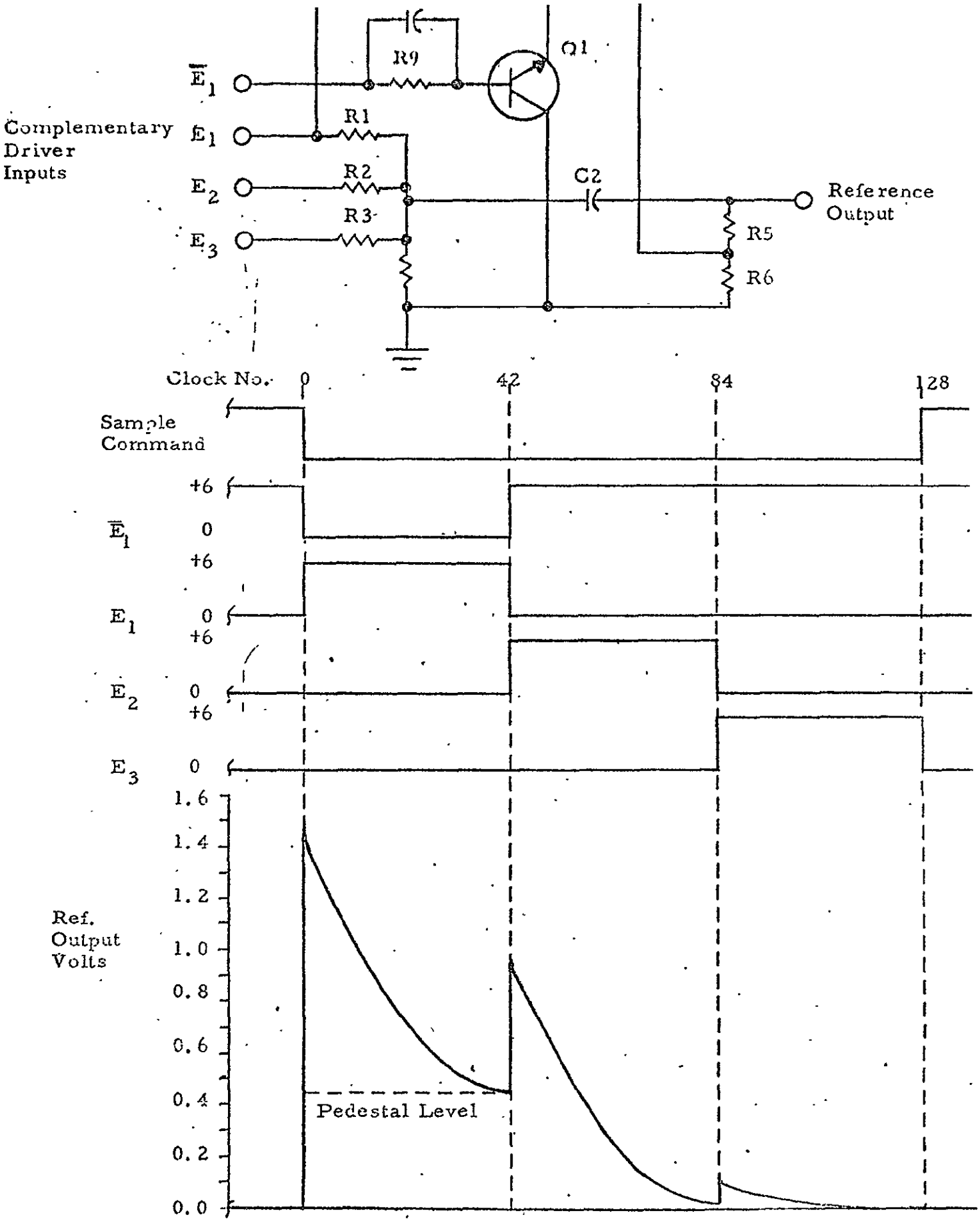


FIGURE 5.5-4
REFERENCE GENERATOR
SCHEMATIC AND TIMING

5.A.(3) (continued)

The attenuator and reference outputs are applied to the comparator shown in Fig 5.5-5. This comparator has a nominal gain of 10^5 and will not be explained in detail since it is very straightforward in design.

The LPWM described in the above was successfully flown as part of the Plasma instrument on Pioneers 8 and 9 and has proved to be very accurate and reliable.

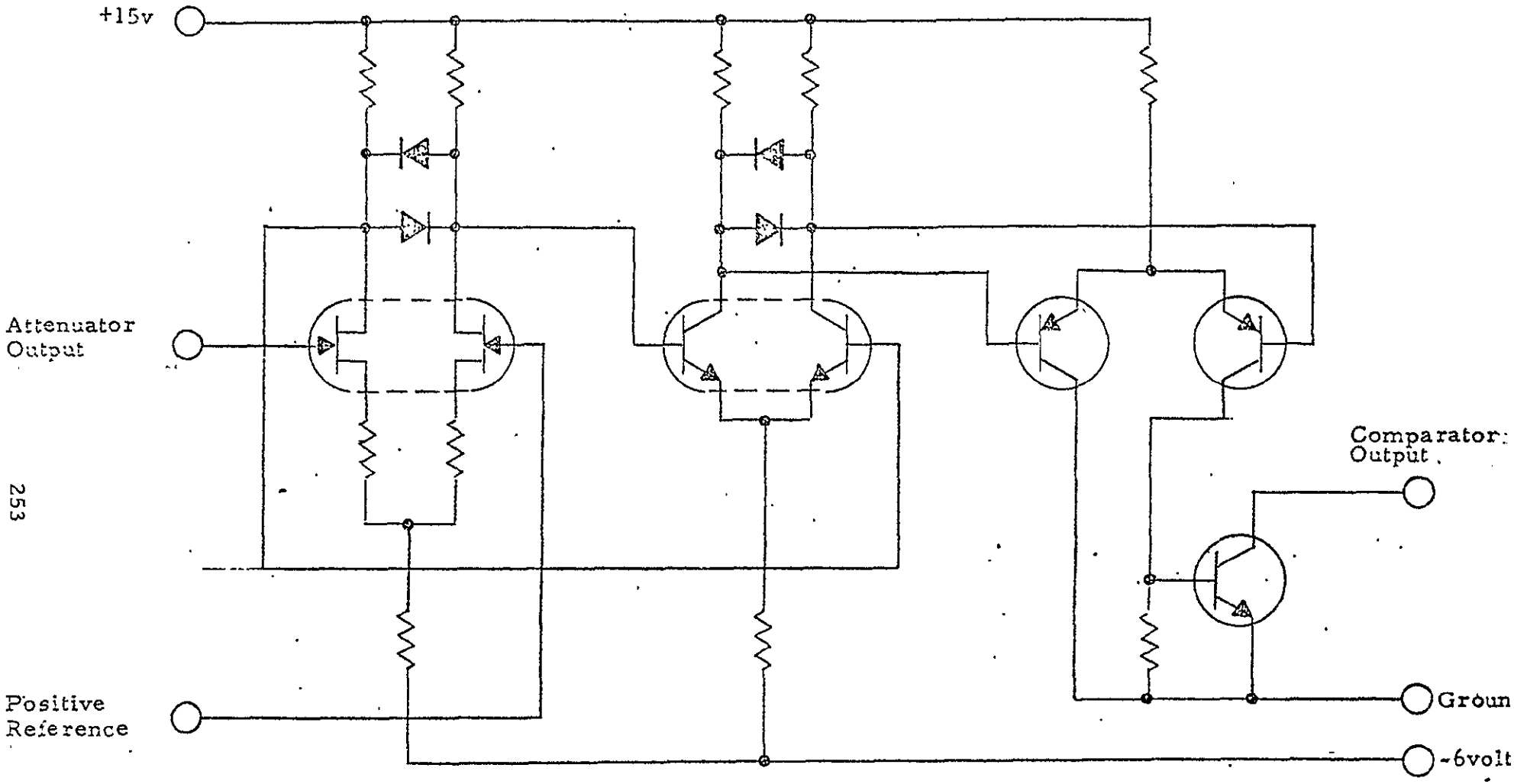


FIGURE 5.5-5
POSITIVE COMPARATOR SCHEMATIC, SIMPLIFIED

6.0 MECHANICAL AND THERMAL DESIGN

The Pioneer C, D & E Plasma Probe experiment instrument, specified and monitored by Ames Research Center, was designed and manufactured by Marshall Laboratories (now Time-Zero Corp.) in conformance with Ames' procurement specification A10202. Mechanical aspects of the instrument's analysis, design, fabrication and testing are discussed in the following paragraphs.

6.1 Optics Assembly Design

The Plasma Probe is an electrostatic, mass per unit charge, particle spectrometer.

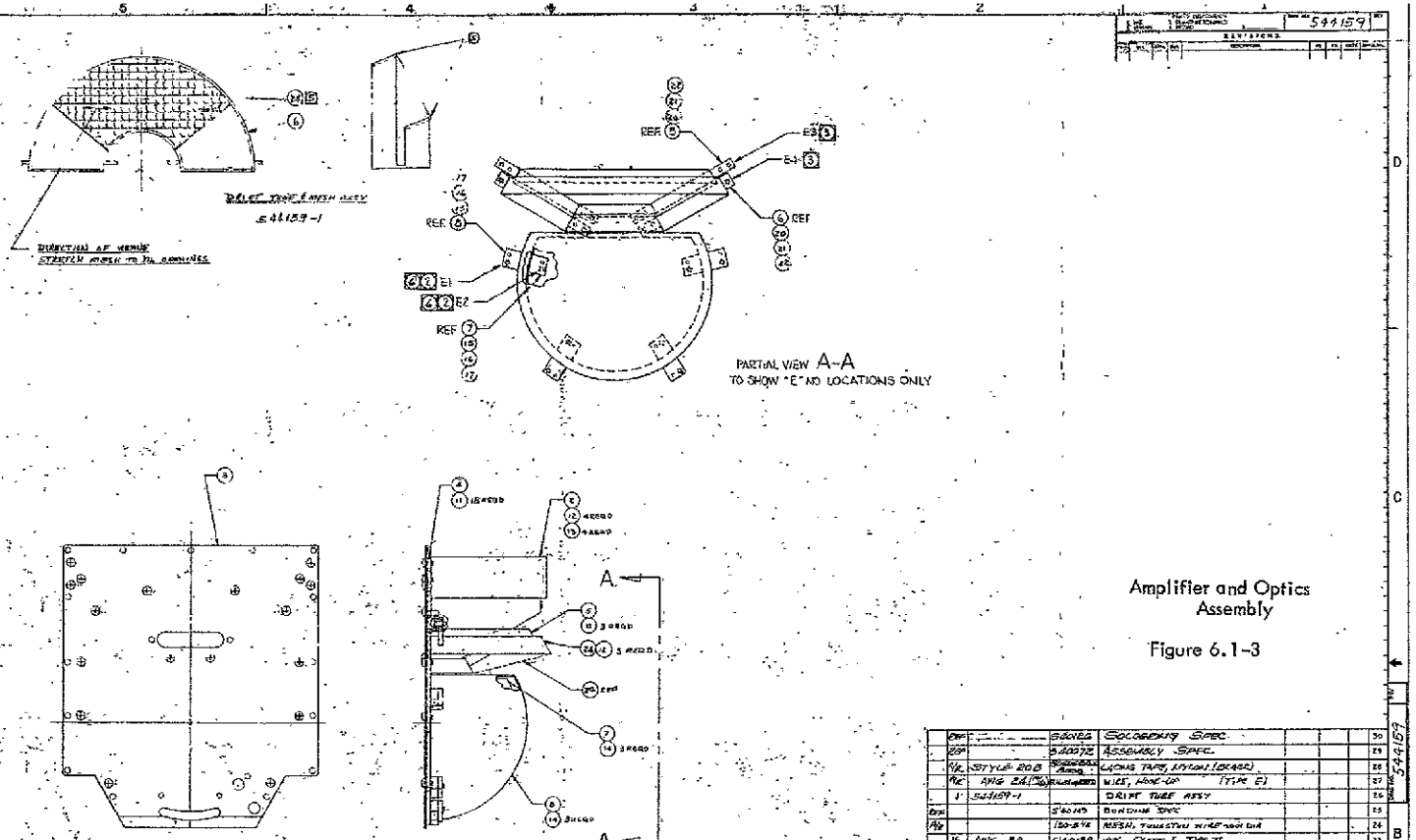
The Plasma Probe assembly drawing is shown in Figure 6.1-1, Instrument, Final Assembly, ARC Plasma Probe. The Master drawing list is presented in Appendix B.

Mechanically the instrument consists of:

- Amplifier and Optics Assembly
- Power Supply Assembly
- Logic Assembly
- Buffer Storage Assembly
- Housing and Covers
- Connectors and Associated Wiring
- Miscellaneous Hardware, Terminal Boards, and Modules

The instrument is supplied with a custom carrying case.

The amplifier and optics photo is shown in Figure 6.1-2, assembly drawing is shown in Figure 6.1-3. This figure shows the optics elements attached to a lexan face plate which in turn attaches to a metallic face plate.



Amplifier and Optics Assembly

Figure 6.1-3

			S-60163	SOLDERING SPEC			30
			S-60072	ASSEMBLY SPEC.			29
	½	STYLE 20B	REFERENCE	CLOTH TAPE, ANTISTATIC (BLACK)			28
	AR	AWG 24	REFERENCE	WIRE, HOOK-UP TYPE E1			27
	1	544159-1		DRIFT TUBE ASSY			26
			S-60145	BONDING SPEC			25
	AR		150-5%	RESIN, TUNGSTEN WIRE WOUND			24
	½	AWG 20	S-60158	WIRE, CLASS I, TYPE II			23
	8	KR43	THOMAS & BETTS	TERMINAL LUG	66,68		22
	2	MS2104	ELASTIC	LOCKNUT, 4-40			21
	2	LP35235-10	LOUISLOC	SCREW 4-40 x ⅝			20
	REF	544101		INTERCONNECT SCHEMATIC			19
	TREF		64001	IDENTIFICATION SPEC			18
	2	KR29	THOMAS & BETTS	TERMINAL LUG	65,66		17
	2	MS2102	ELASTIC	LOCKNUT 2-56			16
	2	LP35235-7	LOUISLOC	SCREW 2-56 x ⅜			15
	3	LP35235-5		SCREW, 2-56 x ¼			14
	4	LP35235-10		" 4-40 x ⅝			13
	10	LP35235-5		" 4-40 x ¼			12
	18	LP35235-3	LOUISLOC	SCREW, 4-40 x 3/16			11
							10
							9
	1	544604-2		ANALYZER PLATE, OUTER			8
	1	544604-1		ANALYZER PLATE, INNER			7
	1	544101-1		DRIFT TUBE			6
	1	544150-101		GROUND LEAD			5
	1	544121-1		LEXAN FACE PLATE			4
	1	544120-1		METALLIC FACE PLATE			3
	1	544150-101		AMPLIFIER ASSY			2
	-1	-101	PART NO.	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	USED ON NEXT ASSY	QUAN PER ASSY

6. SOLDER PER MIL SPEC. S-60163.
7. ASSEMBLE PER MIL SPEC S-60072.
6. PREWIRE ITEMS 17 & 22 WITH 18 LONG WIRE LEADS - ITEM 27.
5. BOND ITEM 24 TO 6 PER S-60109, ACCELERATED CURE.
4. CORRELATE "E" NO'S TO INTERCONNECT SCHEMATIC 544101.
3. ITEMS 10 & 21 ARE THE NECESSARY MTG HARDWARE IN THIS LOCATION. ITEM 22 SHOULD BE INSTALLED UNDER ITEM 21.
2. ITEMS 15 & 16 ARE THE NECESSARY MTG HARDWARE IN THIS LOCATION. ITEM 17 SHOULD BE INSTALLED UNDER ITEM 16.
1. LOCTITE PER MIL SPEC. S-60111, CLASS III, TYPE III.

NOTES: UNLESS OTHERWISE SPECIFIED

MARSHALL LABORATORIES
ANALYZER & OPTICS ASSY
ARC PLASMA PROBE, PIONEER C & D
E 13126 544159

FOLDOUT FRAME

FOLDOUT FRAME

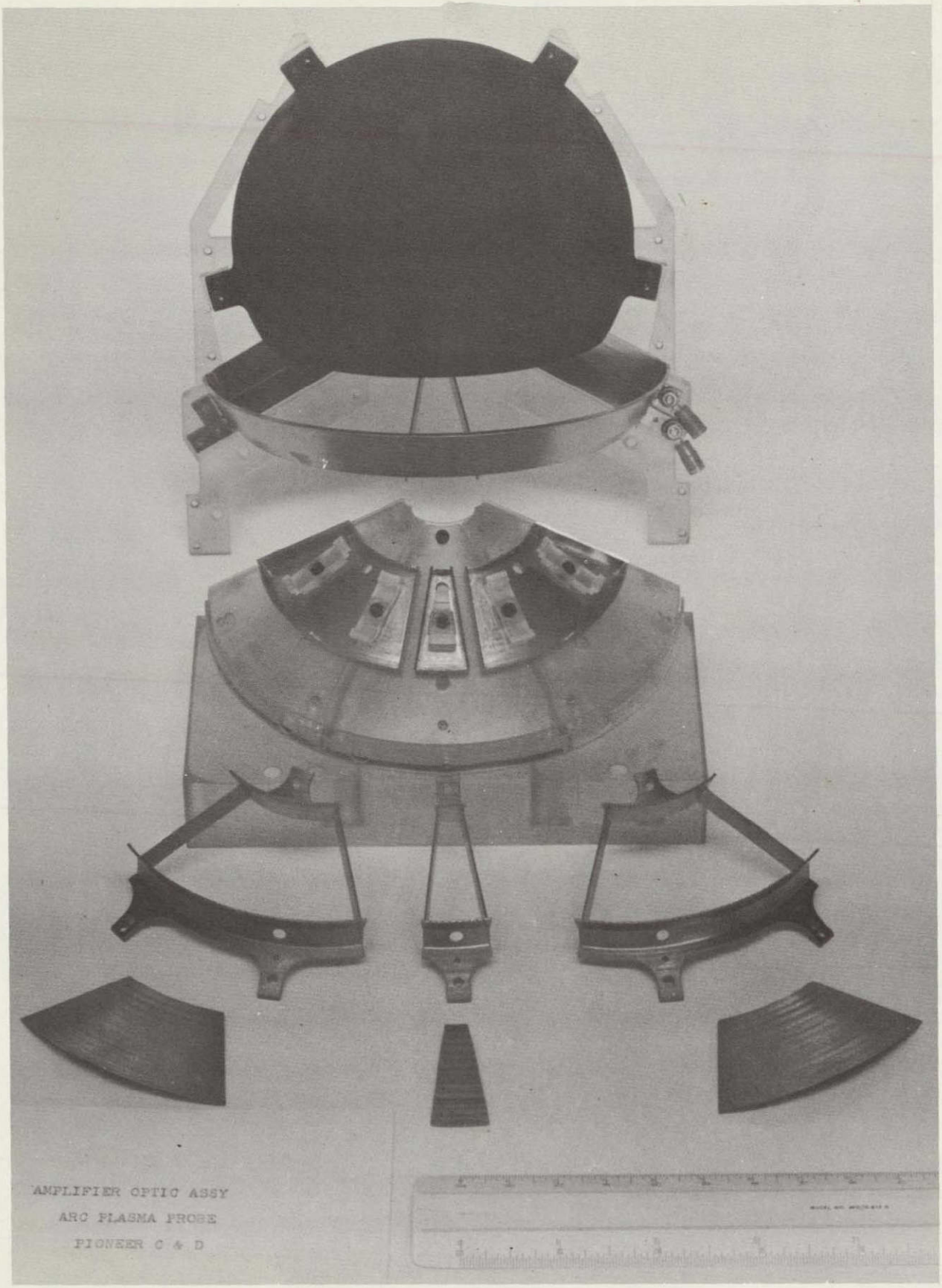


Figure 6.1-2. Amplifier and Optics Assembly

The amplifier attaches to the metallic face plate. The amplifier and optics assembly is screwed to the instrument housing by fifteen 4-40 screws through the metallic faceplate.

In operation, only those particles whose mass to energy ratio corresponds to the analyzer plate spacing and curvature and to the applied voltage will be admitted to the electrometer amplifier input target. The trajectory of the accepted particles passes through the entrance aperture in the metallic face plate, then between the concentric, spherical analyzer plates, through the drift tube grid, and suppression grid to the amplifier input target. Three targets correlate the direction of particle approach.

The targets are shown in Figure 6.1-4 as items 11, 12 and 13. They are mounted on lexan target supports, items 17, 18 and 19 and enclosed on the sides and bottom by the target insulator guard items 14, 15 and 16 in the figure.

Extreme care was required in the preparation of the target supports. Only a minute charge leakage from the target could be tolerated. The target support had to be extremely clean and free from contamination.

Item 15 of the Figure 6.1-4, the target insulator guard, was kept at a potential which minimized capacitive effect of the target to any ground point.

The three driven shield assemblies items 38, 39 and 40 each consist of a frame member item 19 or 20 supporting a tungsten wire knit mesh item 37 in Figure 6.1-4. The wire mesh is bonded to the frame with conductive epoxy. The edges of the mesh are laced with a single wire to prevent unraveling.

WIRE LIST			
WIRE NO.	FROM	TO	REMARKS
1	FE 1-E1	544161-E6	28 AWG
2			
3	-E1	544157-E9	
4	-E2	544161-E21	
5	-E3	544161-E22	
6	-E4	544161-E23	
7	-E5	544161-E29	
8	-E6	544161-E25	
9	-E7	544161-E32	
10	-E8	544161-E27	
11	FE -E9	544161-E26	
12			
13	FE 2-E1	544161-E6	
14			
15	-E1	544157-E6	
16	-E2	544157-E10	
17	-E3	544161-E6	
18	-E4	544161 E12	
19	-E5	544161 E13	
20	-E6	544161-E16	
21	-E7	544161-E11	
22	-E8	544161-E17	
23	FE 2-E9	544161-E15	
24			
25	FE 3-E1	544161-E17	
26			
27	-E1	544157-E16	
28	-E2	544157-E8	
29	-E3	544161-E7	
30	-E4	544161-E19	
31	-E5	544161-E18	
32	-E6	544161-E24	
33	-E7	544161-E30	
34	-E8	544161-E35	
35	FE 3-E9	544161-E36	
36			
37	544157-E5	E8	4
38	E2	FE 3-J1-E1	4
39	544161-E5,	E5	4
40	E3	FE NO 2-E1	4
41	544152-E11	E4	4
42	E4	FE NO 3-E1	28 AWG
43	544161-E4	TP1	(COMMON)
44	TP1	FE NO 1-E10	BRASS WIRE
45	544161-E9	TP2	(COMMON)
46	TP2	FE NO 3-E10	BRASS WIRE
47	544161-E8	TP3	(COMMON)
48	TP3	FE NO 2-E10	BRASS WIRE
49			
50			
51			
52			
53			
54			
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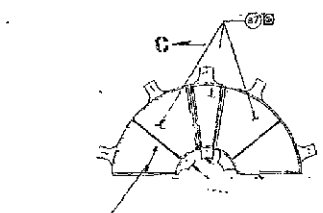
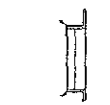
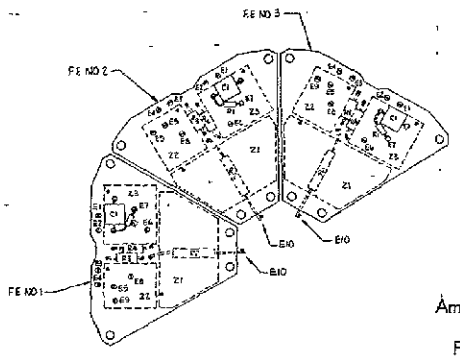
4 AFTER F.E ASSY IS MTD

5 AFTER F.E ASSY IS MTD

4 AFTER F.E ASSY IS MTD



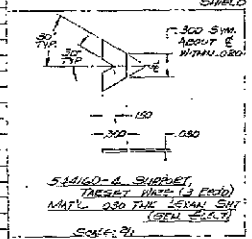




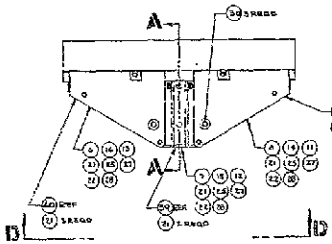
Amplifier Assembly

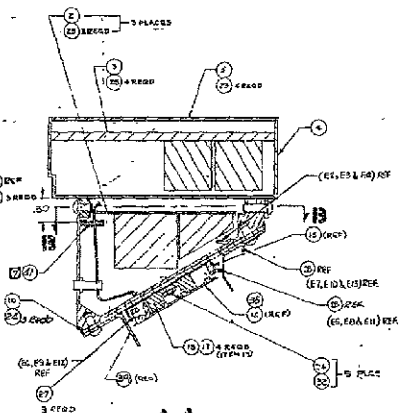
Figure 6.1-4

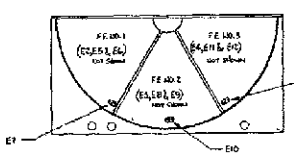
PARTIAL SECTION B-B (SCALE: NONE)
THIS VIEW SHOWN FOR "E" NO. LOCATIONS & AMPLIFIER ORIENTATION



544160-4 SHROUD, TARGET WIRE (3 REQD) MATL .030 THK INCONEL 600 (OR EQUIV)
SCALE: 2/1







THIS VIEW SHOWN FOR "FE" NO LOCATIONS

9. SOLDER PER MIL SPEC. 5401EG.
5. ASSEMBLE PER MIL SPEC. 5400T2E.
7. BOND ITEM 41 IN PLACE AS SHOWN PER MIL SPEC. 5400A9, TYPE II TYPICAL INSTALLATION FOR FROM AMPLIFIER.
6. BIND ITEM 37 TO ITEMS 3, 13, & 25 PER MIL SPEC. 5400F, ACCELERATED CURE.

5 WIRE SECOND.
4 WIRE FIRST.

S CORRELATE "E" NO'S TO INTERCONNECT SCHEMATIC 544101.

6 BONDING IN IS 4 IN TO 11 IN TO PER MIL SPEC 5400A9, TYPE II.
7 IDENTIFY PER MIL SPEC 5400H, CLASS 2.

NOTES: UNLESS OTHERWISE SPECIFIED

ITEM	QTY	PART NO.	SPECIFICATION	NOMENCLATURE OR DESCRIPTION	SIZE	COAT PER ASSY	ZONE
				SOLDERING SPEC.			
				ASSEMBLY SPEC.			
	1/2	STYLE 208		TACKING TAPE NYLON (BLACK)			
	3	544160-4		SHROUD, TARGET WIRE			
	1	544160-3		DRIVEN SHIELD ASSY			
	1	544160-2		DRIVEN SHIELD ASSY			
	1	544160-1		DRIVEN SHIELD ASSY			
	1/2		130-5½	TITANIUM SHEET MESH .001 DIA			
	REF		540103	BONDING SPEC (Supersedes 5401)			
	REF		540149	BONDING SPEC. (Replaces 5401)			
	REF	544139		SCHEMATIC DIAGRAM			
	REF		5401H	IDENTIFICATION SPEC			
	5	MS27602	BASSUNE	NUT 2-56			
	1/2		20-AWG-S	WIRE, BRASS .057 DIA S.S			
	3	1700	MASCOD	SOCKET	TH-TP2		
	1/2	26 AWG	540153	WIRE - CLASS I, TYPE III			
	6	R265	MASCOD	TERMINAL LUG			
	8	LP4KB3224-2	Consult-LOC	SOCKET HEAD SET SCREW, 2-56 x 1/8			
	5	LP3522-10	Consult-LOC	SCREW, 2-56 x 5/16 FLAT HD			
	15	LP3522-1	Consult-LOC	2-56 x 1/16			
	5	LP3521-10	Consult-LOC	2-56 x 1/4 FLAT HEAD			
	4	LP3522-7	Consult-LOC	2-56 x 1/2			
	3	LP3521-3	Consult-LOC	2-56 x 3/16			
	11	LP3522-2	Consult-LOC	SCREW, 2-56 x 3/16			
		544158-102		DRIVEN SHIELD			
	1	544104-101		DRIVEN SHIELD			
	1	544117-2		TARGET SUPPORT			
	4	544117-1		TARGET SUPPORT			
	1	544157-3		TARGET INSULATOR GUARD			
	1	544157-2		TARGET INSULATOR GUARD			
	1	544157-1		TARGET INSULATOR GUARD			
	1	544155-1		TARGET			
	1	544155-2		TARGET			
	1	544155-3		TARGET			
	1	544158-1		DRIVEN SHIELD SUPPORT			
	1	544154-2		DRIVEN SHIELD			
	1	544116-3		AMPLIFIER HOUSING			
	1	544116-4		AMPLIFIER HOUSING			
	1	544116-5		AMPLIFIER HOUSING			
	1	544116-2		AMPLIFIER HOUSING COVER			
	1	544116-1		AMPLIFIER HOUSING			
	1	544141-101		C.S. PWB ASSY			
	3	544140-101		ELECTROMETER F.E ASSY			

MARSHALL LABORATORIES
BALDWIN PARK, CALIFORNIA

AMPLIFIER ASSY - ARC PLASMA PROBE PIONEER C & D

E 13126 544160

FOLDOUT FRAME

The driven shield assembly supports the high transmission tungsten wire mesh grid approximately one centimeter above each target. Voltage is applied to the driven shields to minimize secondary electron emission.

The ground vane, item 5 of Figure 6.1-3, consists of a magnesium frame which is maintained at ground potential. The frame is configured so that it surrounds the sides of the driven shields and target assemblies. By interposing the frame elements at ground potential, the individual detectors are isolated from each other.

The drift tube assembly, item 26 of Figure 6.1-3 consists of a frame supporting a tungsten wire mesh and is attached to the lexan face plate. The open wire mesh is thus interposted between the exit of the analyzer plates and the driven shield mesh above the targets. The drift tube is biased to +40 volts to shield the target area from stray particles.

The analyzer plates, items 7 and 8 of Figure 6.1-3 are also shown in the photos, Figures 6.1-5 and 6.1-6. The plates are mounted concentrically to the lexan face plate. The mean radius of the plates is about 9.5 centimeters; the spacing is about 0.5 centimeters. The plates are .020 ±.005 inches thick. The particle path length is 120° of arc. The plate length perpendicular to particle path is 180° of arc. Platinum Black surface finish prevents passage of photons to the target area.

Wall thicknesses are: drift tube assembly, .025 inches; driven shield and target insulator guard .020 inches; metallic faceplate .040 inches; Lexan faceplate .100 inches.

Drift tube, target insulator guard, and faying surfaces of the metallic face plate and the area around the entrance aperture are gold plated. They are made of AZ31B Magnesium alloy.

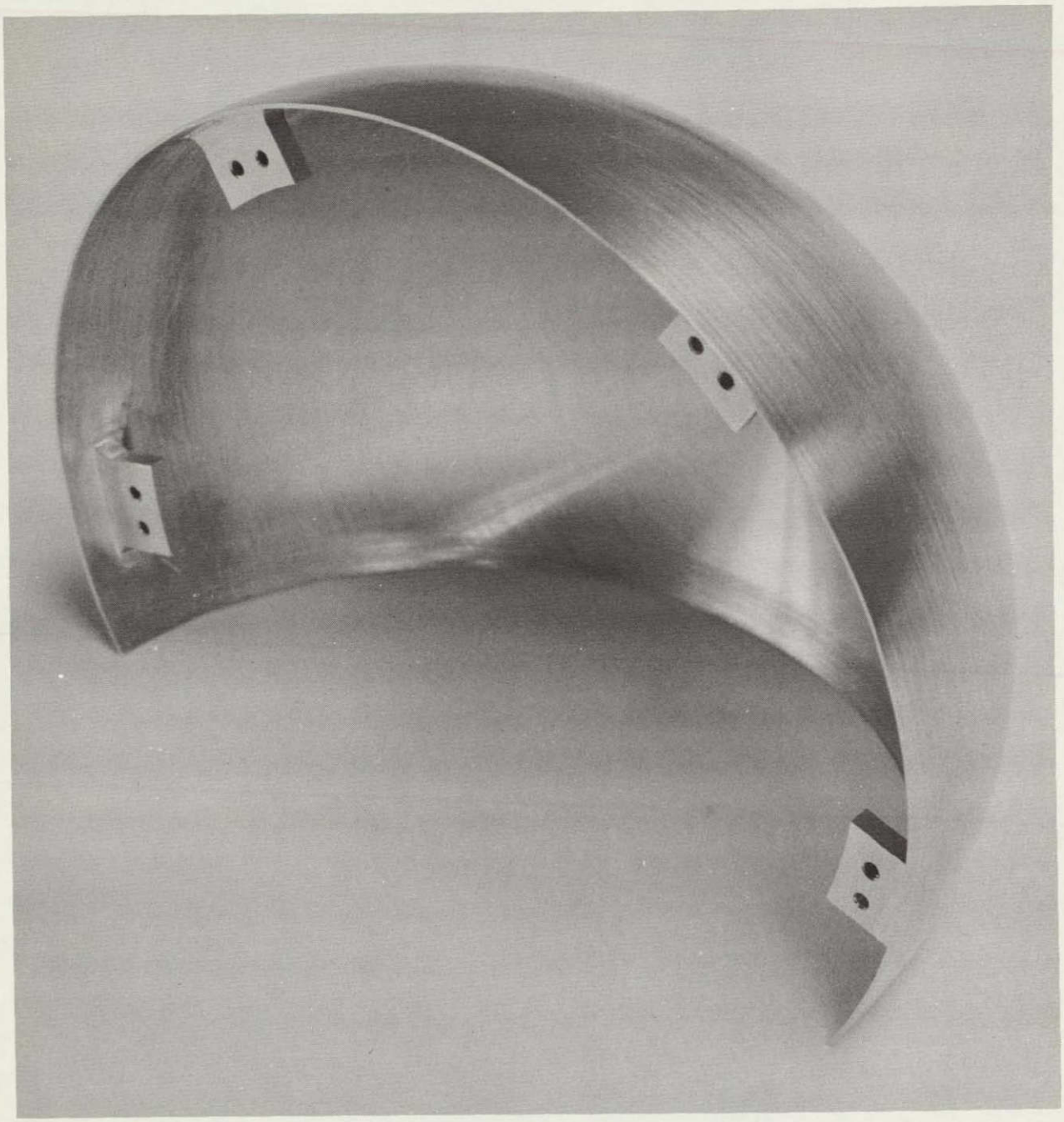


Figure 6.1-5. Analyzer Plate, 544804-1

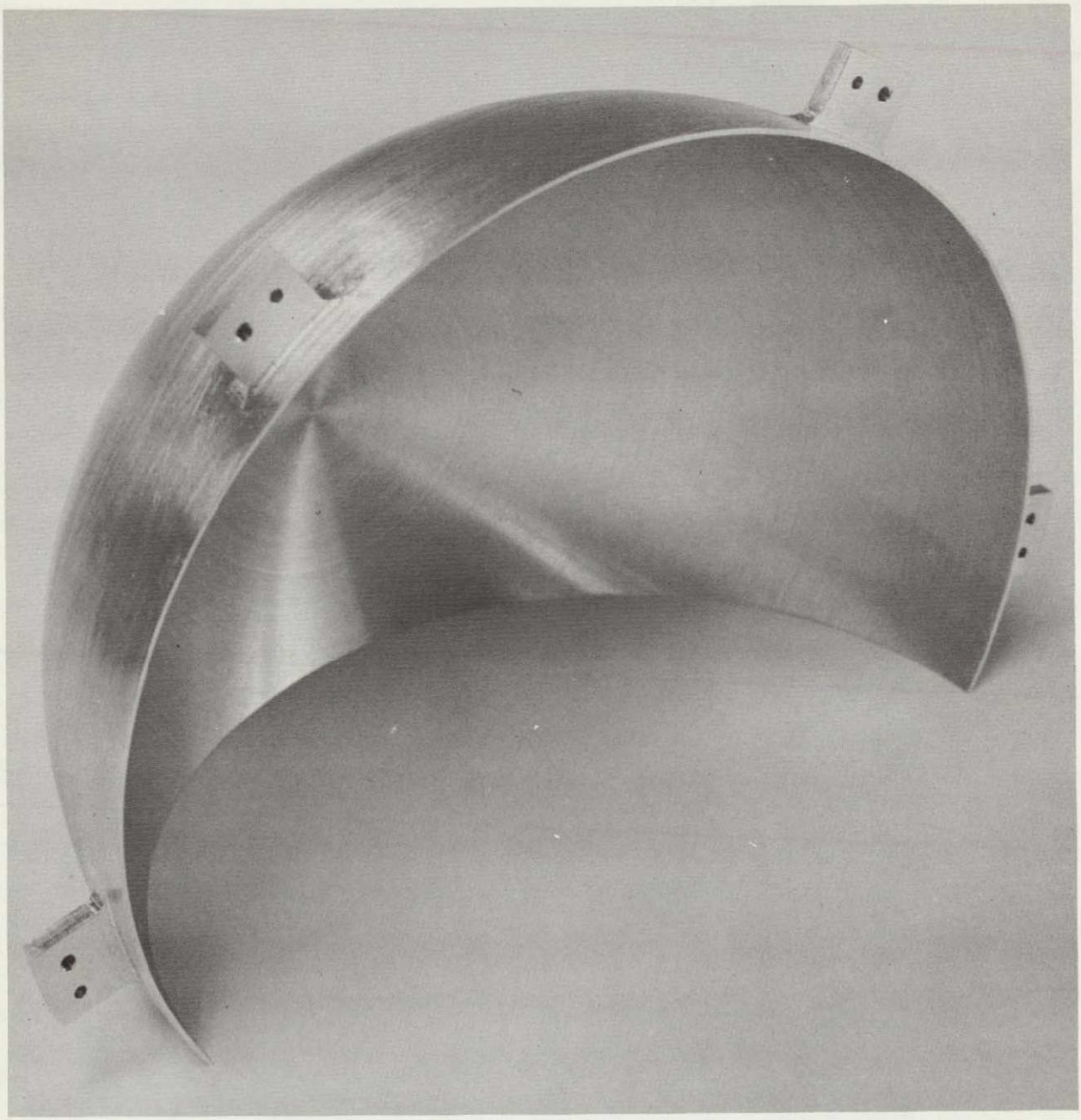


Figure 6.1-6. Analyzer Plate, 544804-2

The magnesium housing with the metallic face plate installed is shown in Figure 6.1-7. Each housing was machined from a 170 pound magnesium alloy forging, ZK60. Typical wall consists of .020 panels with .040 stiffener sections. Finish machining included electrical discharge operation.

The mounting surface and surfaces under the covers are gold plated. The rest of the housing was covered with a flat black epoxy base paint.

6.2 Electronic Packaging

The basic mechanical and packaging design objectives of this program were to provide the following:

1. Components of the highest mechanical and electrical integrity.
2. Units which are mechanically suitable for the expected environment.
3. Equipment with a high degree of built-in reliability and quality.
4. A packaging concept which allows for easy replacement of subsystem elements.

In fulfilling these basic requirements, Marshall Laboratories programmed the project with the philosophy of achieving maximum reliability with minimum weight and size by applying an extensive background and experience in designing and fabricating flight worthy aerospace instrumentation.

The mechanical packages were constructed in such a manner that final checkout and calibration were accomplished with minimum effort. The most versatile packaging approach was a separate assembly for each subsystem thus allowing parallel efforts to be made during assembly, module test, final calibration and checkout.

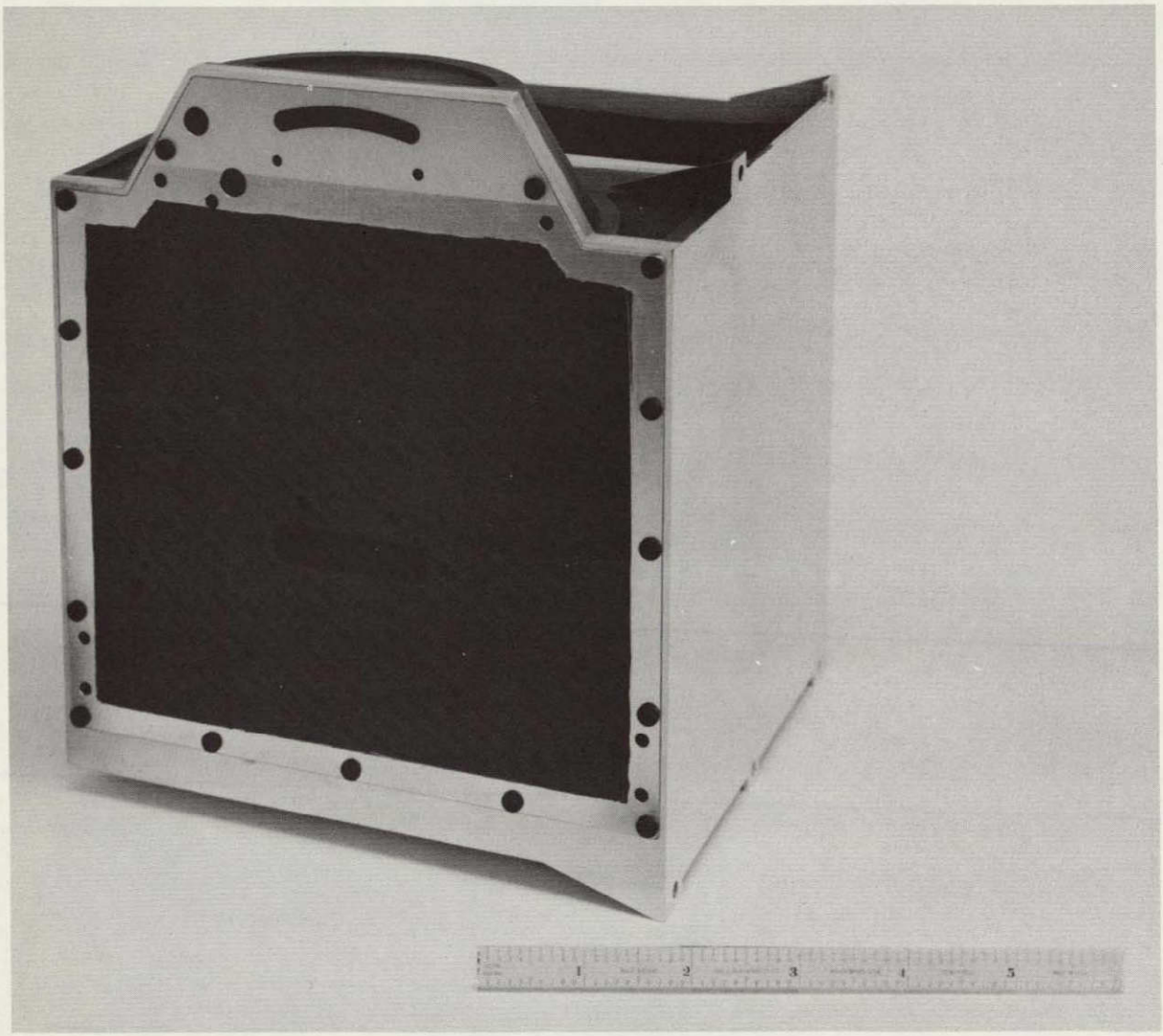


Figure 6.1-7. Instrument Housing

The system is such that it inherently subdivides into natural subsystem groupings thus allowing for this packaging approach.

Analysis of the preliminary schematics indicated that the best method of module construction to be employed for the system was discrete component welded cordwood modules mounted and interconnected on a welded ribbon matrix. This packaging technique contributed to the reliability of the system as well as to the high packaging density and resulted in weight saving.

Point-to-point discrete component welded modules utilize thin mylar wafers with components sandwiched between the layers of mylar. Interconnection of the components was made with welded non-magnetic Alloy 180 ribbon. The philosophy at Time-Zero Corporation (Marshall Laboratories) is to use standard size modules for the program. This allows the program, based upon the circuit logic requirements, to establish a size of module which gives ease of fabrication and a size adaptable to the program requirements for reworkability and component replacement.

To provide ease of fabrication the module is designed as an art work. This art work provides all interconnection requirements of the components contained within the module. Upon completion, the art work is photographically reduced 10:1. Copies provide the mylar wafers used in the fabrication process.

These modules usually contain from two to six transistors plus associated components which are sandwiched between two to four mylar wafers and interconnected by welding with aforementioned ribbon. These modules may be either digital or analog type circuits.

The module may be designed one of two ways. One type sandwiches the components between the mylar wafers with the mylar wafers parallel to the exit pins. When this module is fabricated an epoxy board header is used to position the module exit pins. See Figure 6.2-1.

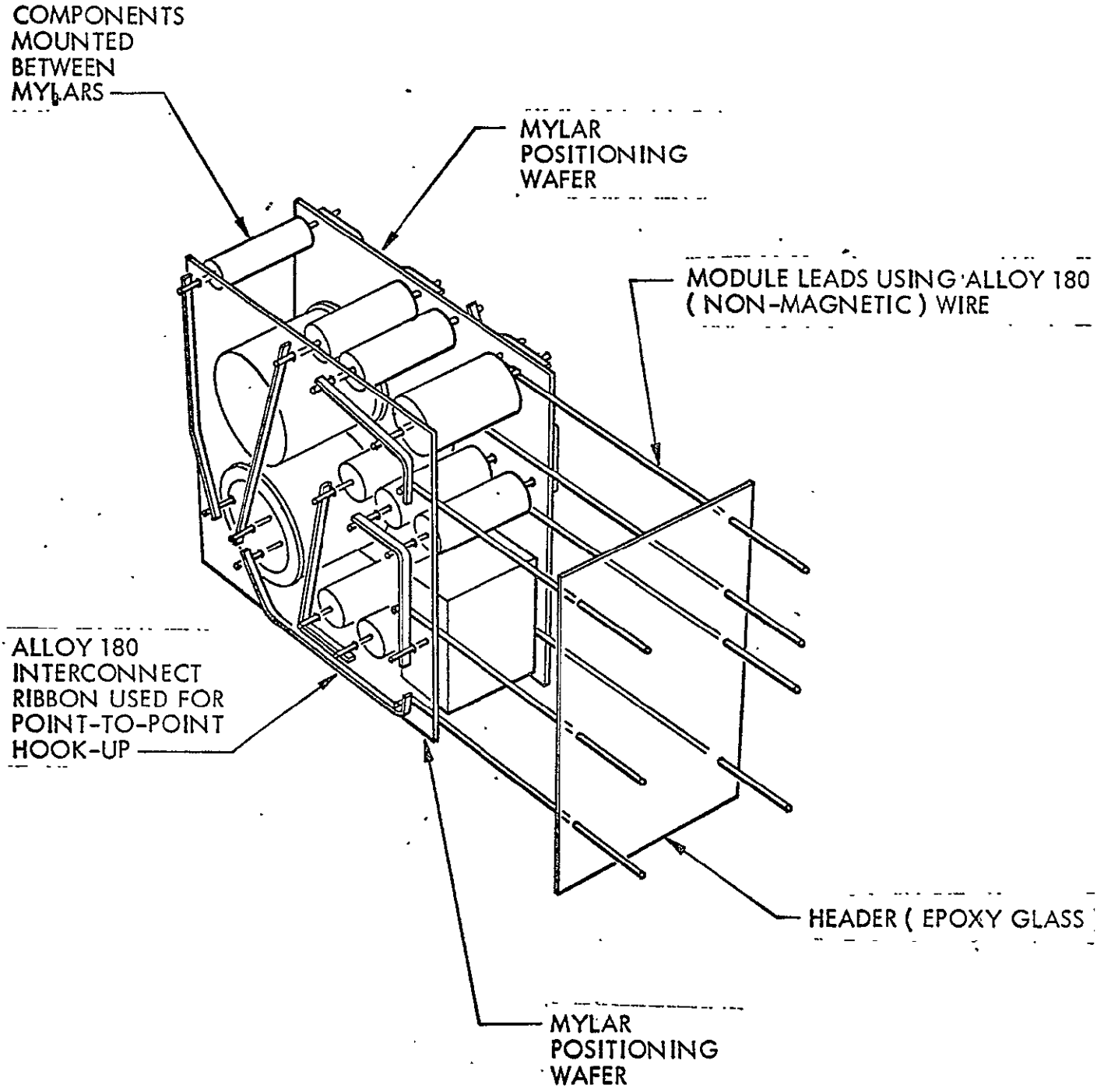
The second type of welded module positions the exit pins perpendicular to the mylar wafer. This method of discrete component module packaging does not require a header for pin alignment as the positioning mylar serves that function. See Figure 6.2-2.

The module's exit pins are designed such that the same pin of every module is used for "power" (B+). The same principle is used for "ground". This provides quick orientation of the module and allows ease of the matrix mother board interconnection. Signal pins of the module are isolated with input signals positioned as far away as possible from output pins, subject only to the interconnection requirements and the module size.

Wire (as opposed to ribbon) is used for module exit pins and feed-thrus required for circuit interconnection. Thin walled Teflon tubing is used to sleeve the feed-thrus to prevent internal short circuits.

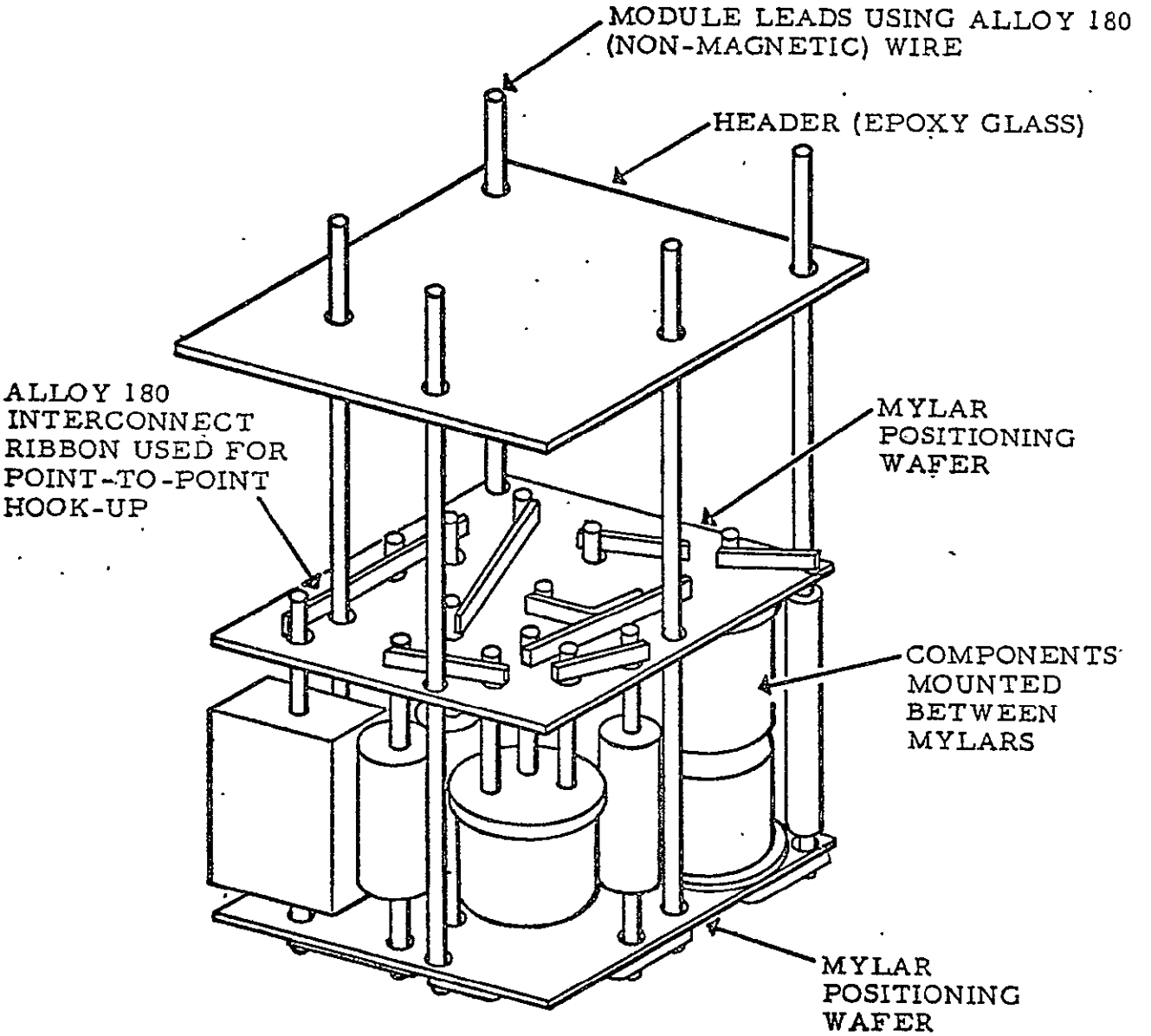
After fabrication and subsequent to electrical checkout, the module is conformally coated with a low viscosity epoxy material to supply the module with rigidity and moisture protection. The close proximity of the interconnect layers adds to the rigidity of the module enabling it to withstand all expected environmental conditions.

The module interconnect matrix is a family of interrelated elements utilized in the interconnection of modules and other individual electrical components comprising the electrical assembly.



TYPICAL WELDED MODULE

Figure 6.2-1



WELDED MODULE

Figure 6.2-2

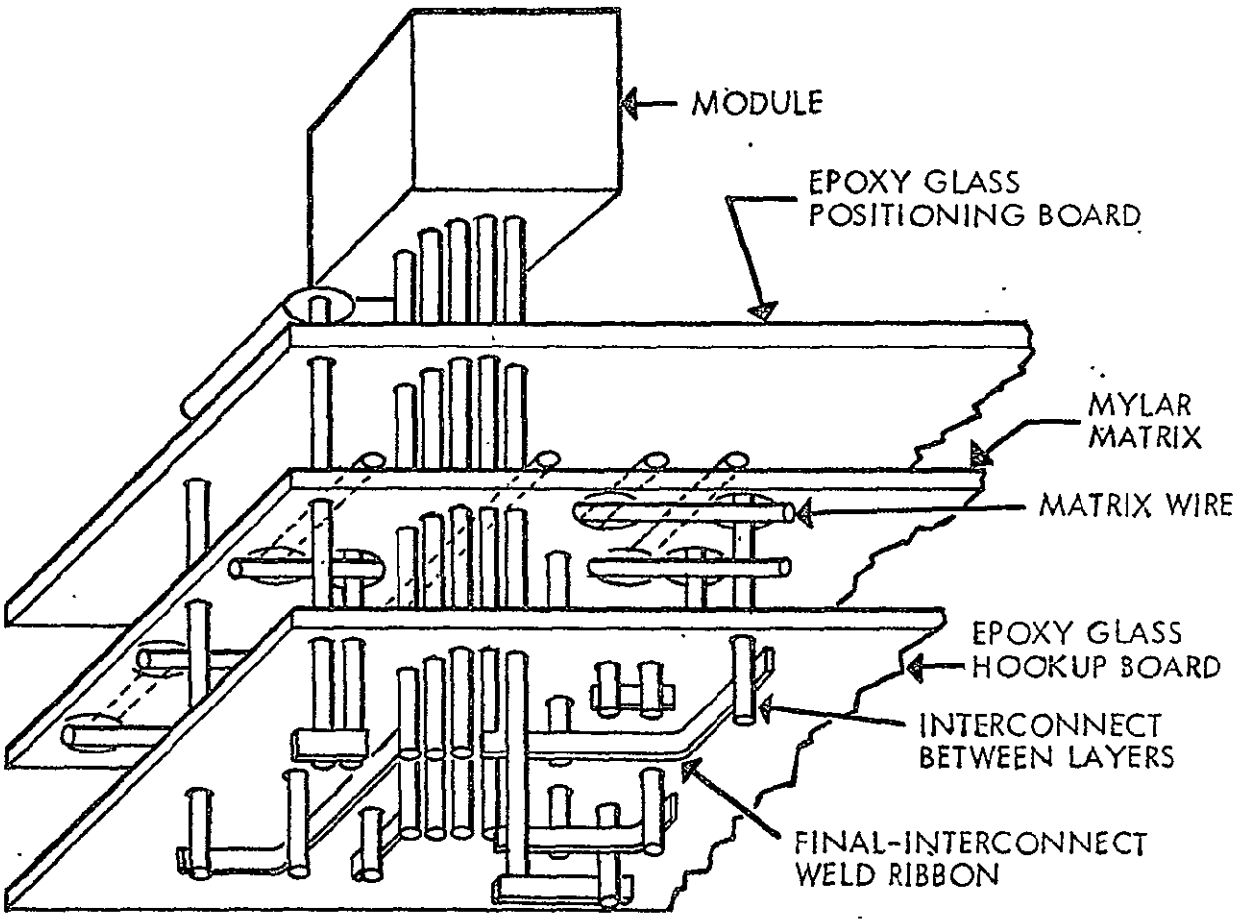
The assembly consists of a hookup board, a positioning/support board, a matrix, and spacers. Upon assembly, the matrix consists of a two-sided mylar interconnect sandwiched between the hookup and positioning/support board separated by spacers. All module interconnections are accomplished on a hookup board as shown in Figure 6.2-3.

The matrix assembly is built using a 0.007 inch thick mylar upon which alloy 180 wire is used to form the interconnection of the electrical subunits. All modules and circuit elements are connected to the matrix as required by wires protruding through the matrix and welding upon the hookup board level. Interconnection of the subunits in this fashion allows the accessibility required for repair and troubleshooting of the assembly.

Epoxy glass spacers, the thickness of the matrix wire, are bonded around the edge and each side of the mylar. A 0.016 inch thick positioning/support board and a hookup board are then bonded to the matrix. The positioning/support board artwork shows the electronic elements' positions upon the matrix assembly and also supports them. The hookup board becomes the prime interconnect layer serving as the guide for the alloy 180 ribbon interconnection of the circuit assembly elements.

All circuit elements are interconnected on the hookup layer as a point-to-point welded module. If a circuit element requires replacement, the point-to-point interconnecting ribbon can be cut, the old element removed and replaced by a new element, and rewelded into the circuit on the interconnecting wafer.

The matrix provides the means to buss voltage, ground and signal circuits. This results in dense circuit packaging and good volume efficiency. The matrix can be fabricated easily because all welding is accomplished before the circuit elements are installed.



MODULE INTERCONNECT MATRIX

Figure 6.2-3

The positioning board, matrix and hookup board are then assembled. The modules as circuit elements are then installed in the assembly and welded as one large point-to-point module. All welds are open for complete accessibility even after being attached to a structural housing assembly.

To provide electrical inputs as well as outputs, terminals are installed upon the positioning and/or hookup board as required. The required electrical signals are provided by free wiring from a connector installed upon the matrix housing. This interconnection of the signals to the matrix assembly is accomplished after the matrix has been bonded to the housing.

The completed electronic matrix assembly is then conformally coated to provide insulation, moisture protection and rigidity. The matrix assembly as fabricated at Time-Zero Corporation (Marshall Laboratories) becomes a structural load-carrying member in addition to being a mounting board for modules and a device for making their interconnection. This is accomplished when the assembly is bonded into the machined support housing for the matrix assembly.

Blivet housing frames on this experiment were designed as mechanical structures machined from solid blocks of magnesium (Alloy AZ31B-H24 per QQ-M-44A) to provide a high strength to weight ratio. All areas of the housings not contributing to the structural integrity of the completed instrument are either relieved or removed as applicable, based upon the particular requirements. The relieved areas are designed as thin (.025 inch to .030 inch) webbed stress coupling membranes. These thin webs are capable of carrying loads after the matrices are installed in the housings.

The major portion of the electronics assembly consists of three blivet assemblies and the amplifier. A photo of the power supply blivet is shown in Figure 6.2-4, the logic blivet in Figure 6.2-5, and the buffer storage blivet in Figure 6.2-6. A drawing of the amplifier assembly is shown in Figure 6.1-3. The Photo, Figure 6.1-2 shows the amplifier housings.

The Amplifier assemblies are enclosed in lexan housings. Shielding is provided by conductive epoxy coatings applied to both inside and outside. The inside coating is isolated from the outside. The wall thickness of the amplifier housings is .040 inches.

6.3 Environmental Testing

Qualification tests were conducted to demonstate the ability of the design to meet all performance requirements for space flight.

Results of the qualification tests performed on the ARC Plasma Probe Instrument verified that the experiment is capable of meeting these requirements.

One significant problem arose as a result of qualification level vibration test and resulted in a minor redesign of the electrometer amplifier module. The problem consisted of the electrometer tubes' (Raytheon 8520) ability to withstand the amplified vibration at qualification levels. This was expressed in failures Nos 003, 004 and 005 as a direct result of the electrometer tubes. Structural integrity analysis and empirical testing of the problem areas resulted in the addition of soldering soft wires from the electrometer tubes and shock mounting them within a soft foam collar. These modifications proved satisfactory and were incorporated in the flight units.

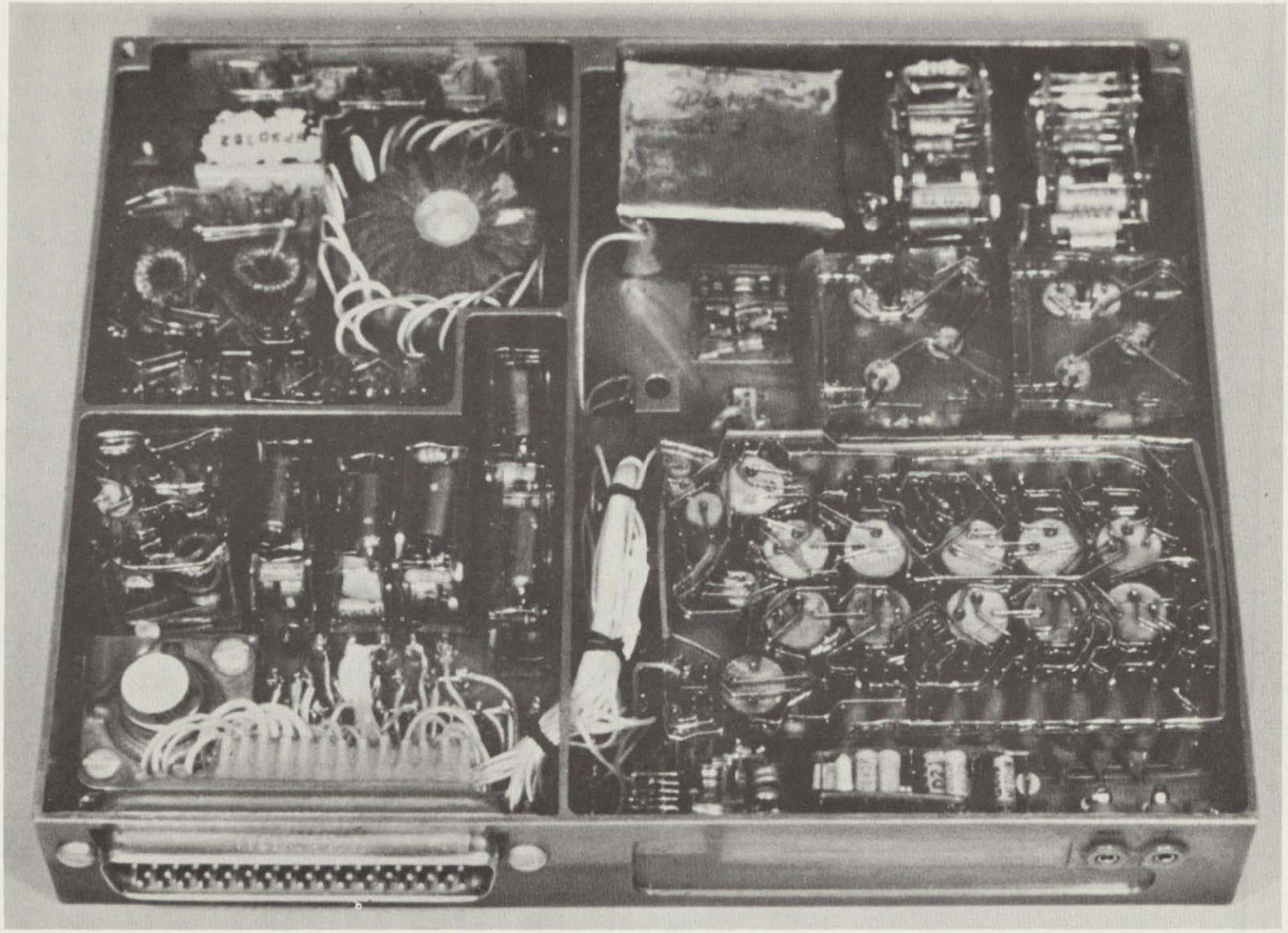


Figure 6.2-4. Power Supply Blivet

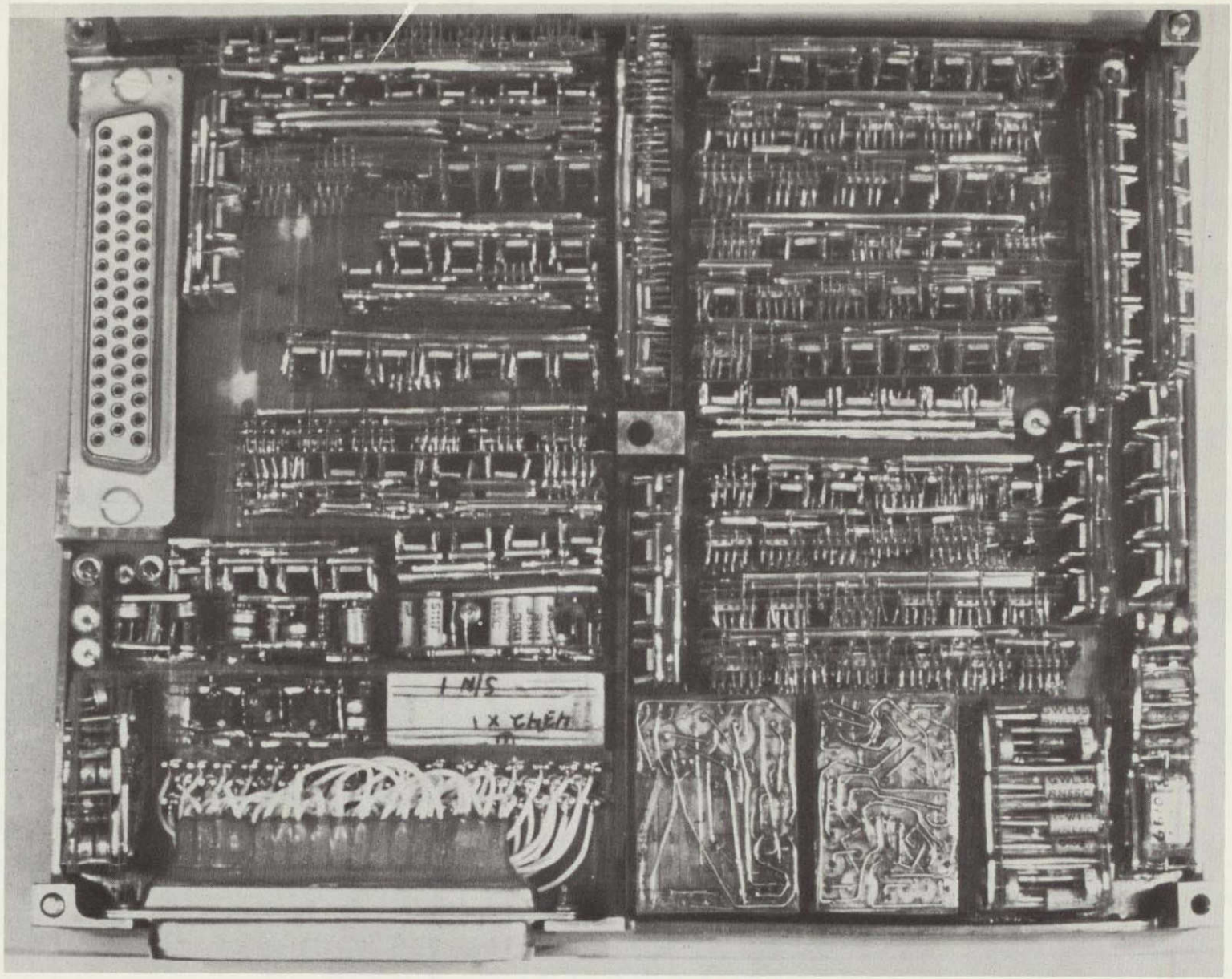


Figure 6.2-5. Logic Blivet

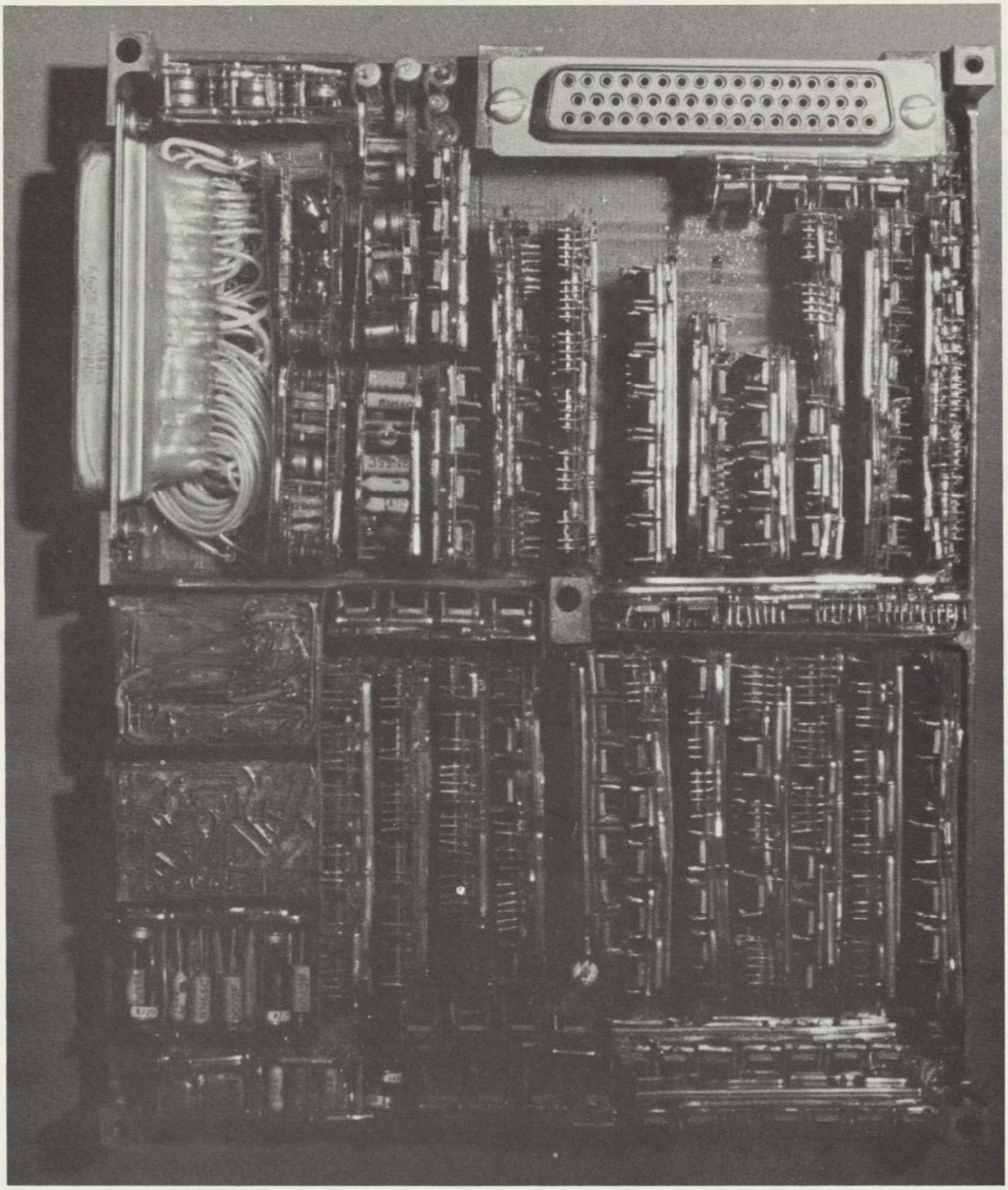


Figure 6.2-6. Buffer Storage Blivet

Flight Acceptance tests were conducted to assure that the instruments were equivalent to the qualified instrument and to provide a debugging burn-in which reduced possibility of infant mortality failures. These tests were designed to disclose undetected defects.

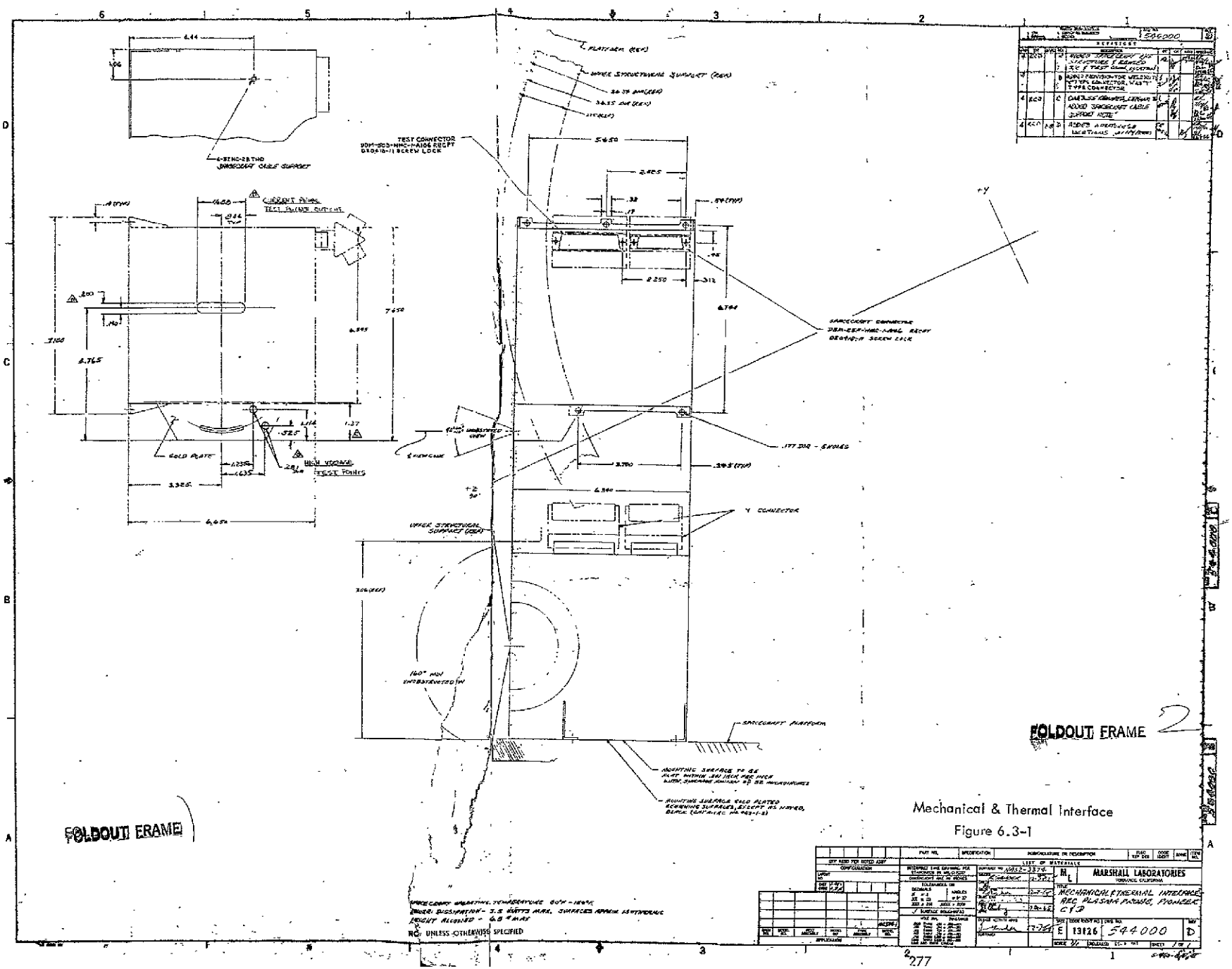
A typical Flight Acceptance test is included in Appendix B and C.

Results of the flight acceptance tests performed on the ARC Plasma Probe Instrument verified the experiment as being capable of meeting the flight requirements.

Thermal and Structural analyses were made that apply to this program. Documentation of Shroud heating effects and structural analysis is contained in Appendix G and H. Environmental tests verified the analyses.

6.4 Mechanical and Thermal Interface

The mechanical and thermal interface requirements are shown in the Mechanical and Thermal Interface drawing, Figure 6.3-1.


FOLDOUT FRAME
FOLDOUT FRAME 2
Mechanical & Thermal Interface
Figure 6.3-1
MARSHALL LABORATORIES
MECHANICAL/THERMAL INTERFACE
REC. PLASMA PROBE, IONOSPHERIC C.V.D.
544000
D
SPACECRAFT PLATFORM
HIGH VOLTAGE TEST POINTS
GOLD PLATE
TEST CONNECTOR
SPACECRAFT CONNECTOR
Y CONNECTOR
UPPER STRUCTURAL SUPPORT (REF)
SPACECRAFT RADIATIVE TEMPERATURE 60°F - 100°F
POWER DISSIPATION - 3.5 WATTS MAX. SURFACES FACING SPACECRAFT
WEIGHT ALLOWED - 6.0 # MAX
UNLESS OTHERWISE SPECIFIED

7.0 GROUND SUPPORT EQUIPMENT (GSE)

7.1 Function

The primary function of the GSE is to

(a) provide all stimulus, timing signals, and power supply potentials necessary to operate the flight hardware over its entire range of operation and for all modes of operation.

(b) provide a readout capability which is synchronized to the stimulation of the sensor for measuring and recording system inputs, outputs, and performance parameters

(c) provide means for simulating that portion of the spacecraft electronics normally seen by the scientific instrument

7.2 Environmental Range of Operation

The GSE is designed to operate continuously over a temperature range of 50^{o}F to 100^{o}F, and a humidity range of 20% to 95%.

7.3 Delivered Items

(a) Each GSE set consists of:

1. Simulator Unit/Demodulator Unit
2. Monitor and Control Unit
3. Meter Unit
4. Printer Unit
5. Current Probe Unit
6. Isobox

(b) One (1) breadboard GSE with one (1) set of 30 foot cables (delivered prior to start of prototype)

(c) Two (2) GSE sets delivered as follows:

1. GSE set number 1 delivered with one (1) set of 30 foot cables and one (1) set of 6 foot cables.

2. GSE set number 2 delivered with one (1) set of 30 foot cables.

(d) Drawings

1. Functional block diagram
2. Circuit schematics
3. Wiring diagrams
4. Logic diagrams

(e) Test Procedures

1. Compatibility Test
2. Functional Test
3. Checkout Procedure
4. Operating Procedure
5. Calibration Procedure

7.4 Performance Features

The GSE has an operating life of 20,000 hours with reasonable servicing and parts replacement and an overall possible lifetime of 10 years.

The GSE is capable of continuous operation for 1,000 hours within the anticipated ground environment, allowing for battery charging only.

Like GSE components are interchangeable. The GSE is mounted in containers provided by NASA/ARC.

Detailed design requirements are the same as for the Plasma Probe instrument with the following exceptions:

(a) Non-magnetic parts not required except for cable connectors at S/C end.

(b) Part screening not required.

(c) Use of preferred parts not mandatory.

(d) Electrical parts review not required.

Breadboard GSE utilizes rack-mounting construction with plug-in circuit cards.

Electromagnetic Inteference requirements are observed per paragraph 3.2. of MIL-I-26600 (Class 1B). For purposes of Plasma Probe this requirement is interpreted that all normal RFI precautions be taken in the design and the signature of the final equipment shall be obtained. Where possible interference occurs between GSE and other instruments or spacecraft, an appropriate fix is installed to eliminate the interference.

The equipment is designed for simplicity of operation with a minimum of panel controls.

System chassis grounds, signal return, and power return lines are tied to GSE chassis ground at a single point within the GSE.

Digital data is decoded for readout on a NIXIE tube display and on a high speed printer. Controls permit selection of individual words or sequences of words in addition to all words printed out.

7.5 Interface

7.5.1 System Inputs Provided by GSE

Nomenclature	Signal Description	Amplitude On (+Volts DC)	Amplitude Off (+Volts DC)	Duration (50-50%) μs	Risetime (10-90%) μs	Z Source	Z Load
16.384 KHz Clock	Pulse train 16.384 KHz	11±2	0±1	2± $^{1.0}_{0.5}$	<1	6.8K//.001 uf	3K
Bit Shift Pulse	Pulse generated at bit rate in groups of 6 pulses followed by a missing pulse	11±2	0±1	10±3.5	<1	6.8K//.001 uf	3K
16 Hz Clock	Pulse train w/16 pps repetition rate	11±2	0±1	10±3.5	<1	6.8K//.001 uf	3K
Word Gate	Gate to instrument up for DTU words 8 thru 16 for each frame	9 $\pm\frac{1}{2}$	0±1	Bit Rate Depend.	<50	6.8K//.001 uf	3K
DTU (Digital Telemetry Unit) Status	BR 512 BR 256 Separate BR 64 Lines DCSM	9 $\pm\frac{1}{2}$	0±1	Duration of Cond.	<10	10K	20 K
Command Pulse	In-Flight Calib.	10±2	0±1	10±2	<1	6.8K//.001 uf	3K
	Suppress Cmd	10±2	0±1	10±2	<1		3K

Nomenclature	Signal Description	Amplitude On (+ Volts DC)	Amplitude Off (+ Volts DC)	Duration (50-50%) μs	Risetime (10-90%) μs	Z Source	Z Load
Sun Pulse	One pulse/sc rev. Range 40-80 ppm.	10.5±2	0±1	12.5±6	1	6.8K//001 uf	3K
Input Power	+ 28V DC Nom 3.5 watts cap. Range 25-35 V DC I limit @ 200 ma.						
Probe Stimulus	0-24V DC ramp pulse input 57m sec duration, variable and selectable over sun pulse cycle.	0-24±1	0±5	57ms ± 6			

7.5.2 System Outputs Processed by GSE

Instrument interface circuits drive a 30 foot cable.
(Specs listed not required for 30 foot cable)

(a)	Digital Data -	Series of pulses synched to within 10 μs of shift pulses	+10±1 V DC 3-13μs across 3.9K duration ≤1μs ≤1μs
(b)	Analog Data -	Sub-Com 2(temp)	0 to 3V DC

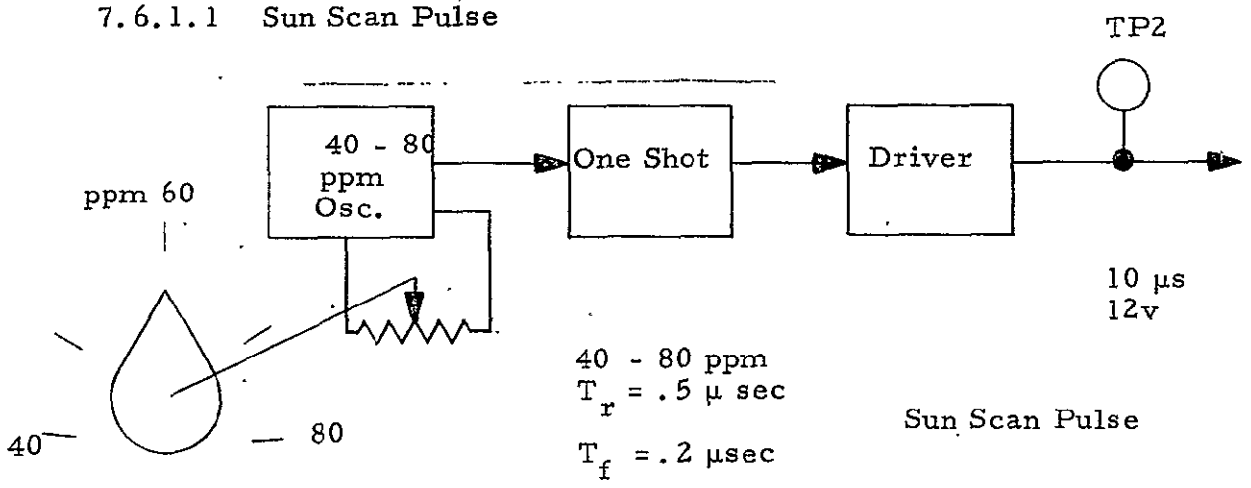
(c) All voltages measured to within ±0.1% by Data Monitor Meter.

(d) Test points provided for monitoring all spacecraft and test connector pins.

7.6 Functional Description

7.6.1 Simulator Unit (Figure 7.6.1-1)

7.6.1.1 Sun Scan Pulse



The oscillator employs NPN-PNP transistor compensation in order to minimize drift due to junction temperature variations. The front panel frequency control dial is calibrated and accurate to ±1.0 pulse per minute at any setting. Output pulses are shaped and amplified by a one shot M.V. and driver combination.

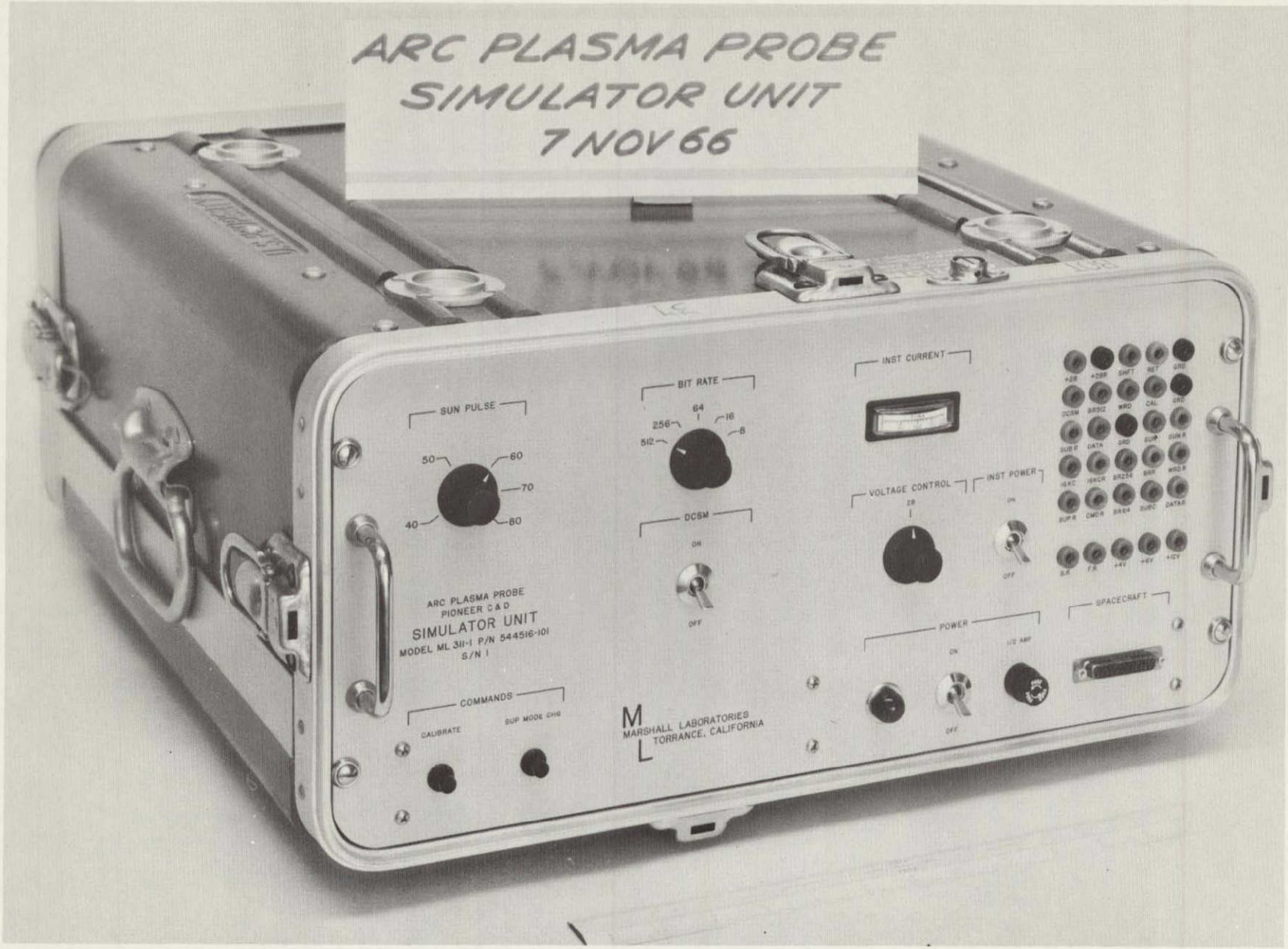


Figure 7.6.1-1. Simulator Unit

7.6.1.2 Commands

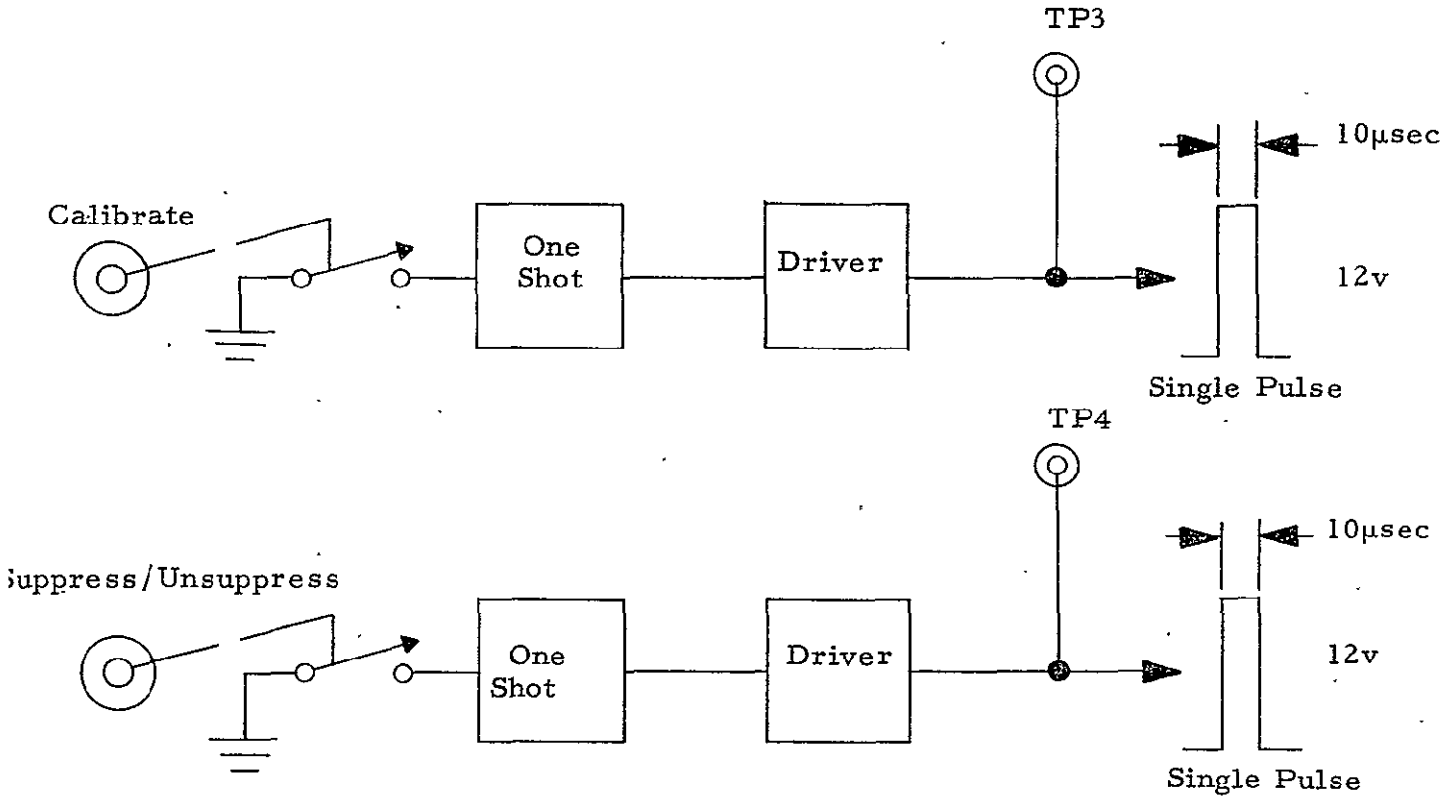


Figure 7.6.1-2 Ground Commands

Each front panel push switch activates a one shot M. V. for a single pulse output each time the button is depressed. Drivers are used to amplify the output pulse as illustrated.

7.6.1.3 Mode Select

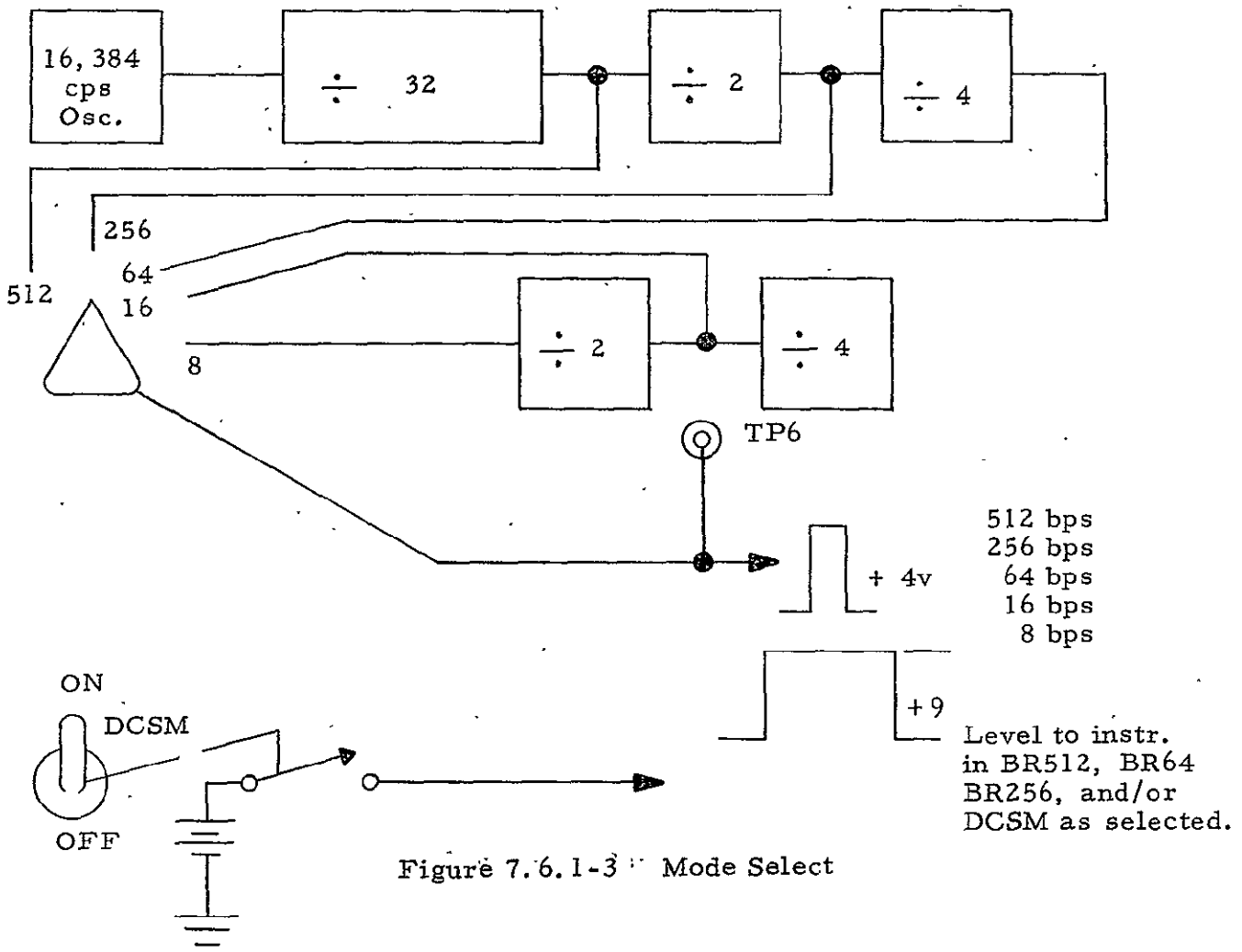


Figure 7.6.1-3 Mode Select

A temperature-compensated oscillator provides an output of 16,384 Hz ± 30 Hz. This output is counted down in a flip-flop counter chain to achieve the required 512, 256, 64, 16 and 8 bits per second operating modes. The pulses are used internally within the GSE to drive other interface signals and gated levels are sent to the instrument as commands for the 512, 256, 64 or Duty Cycle Storage modes.

7.6.1.4 Word Gate Logic

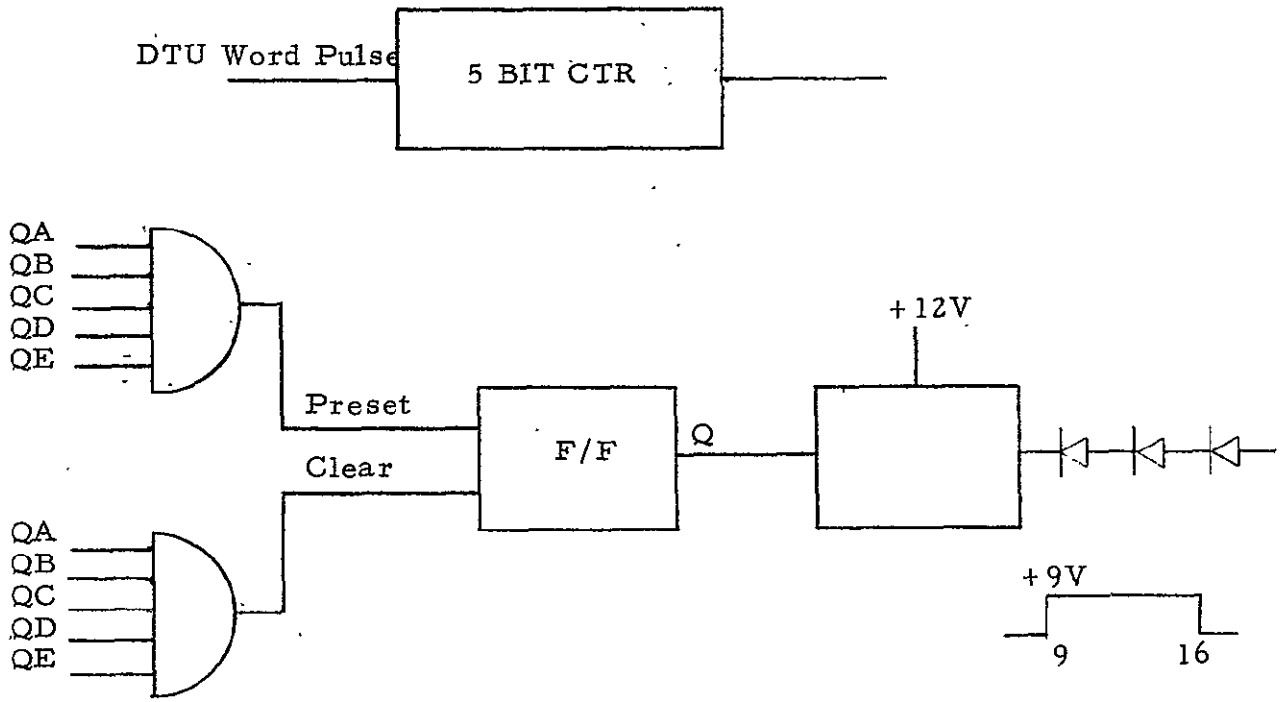


Figure 7.6.1-4 GSE Word Gate Logic

E	D	C	B	A	X
0	0	0	0	1	1
0	0	0	1	0	2
0	0	0	1	1	3
0	0	1	0	0	4
0	0	1	0	1	5
0	0	1	1	0	6
0	0	1	1	1	7
0	1	0	0	0	8
0	1	0	0	1	9
0	1	0	1	0	10
0	1	0	1	1	11
0	1	1	0	0	12
0	1	1	0	1	13
0	1	1	1	0	14
0	1	1	1	1	15
1	0	0	0	0	16

The Word Gate logic circuitry provides a gate pulse to the instrument which starts at DTU word 9 and ends following DTU word 16. Bit rate pulses are counted down to achieve a word count (Bit rate ÷ 7). The words are counted down and decoded by the logic shown above. A driver is used to amplify the pulse to the required level.

7.6.1.5 Power

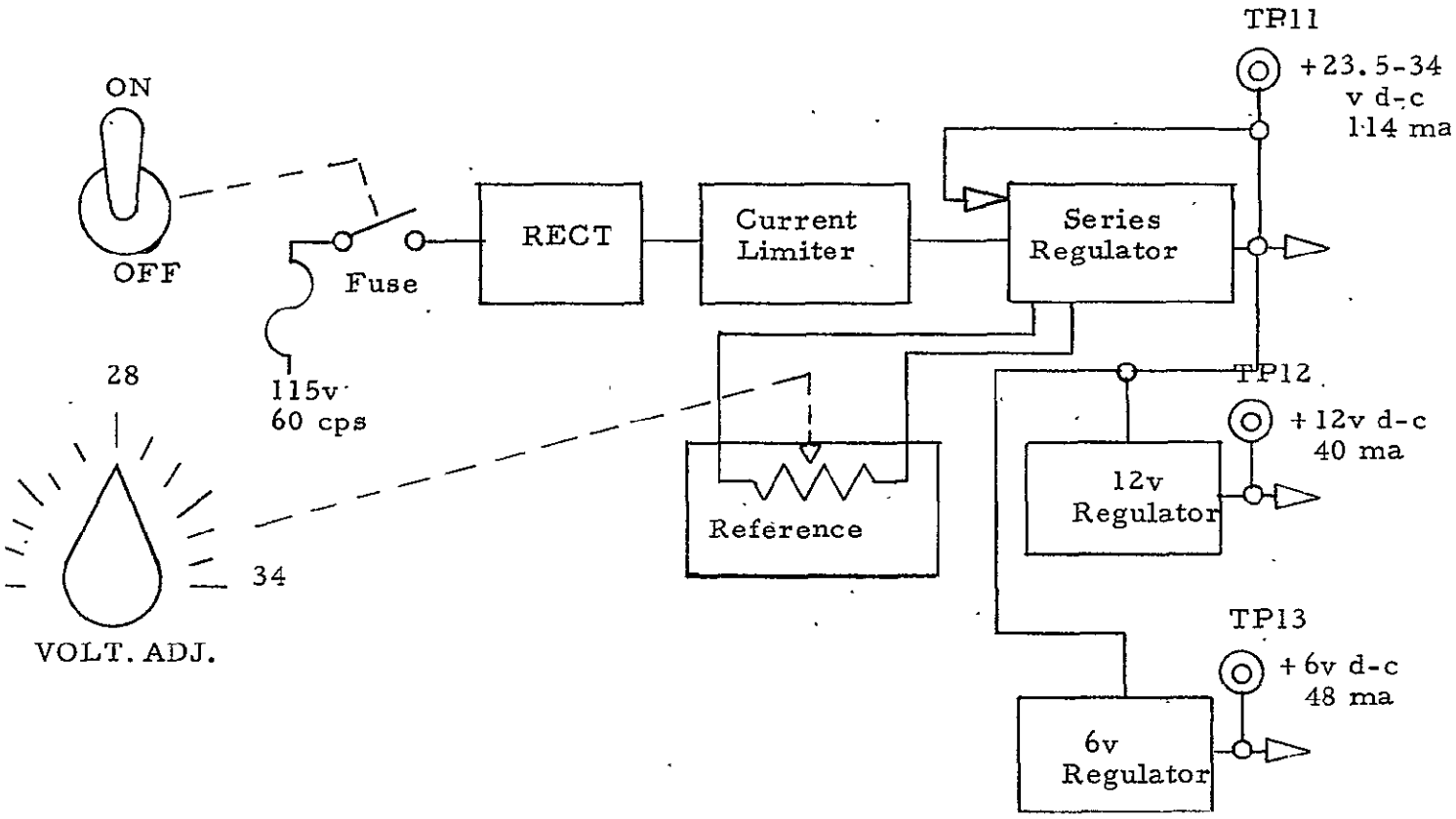


Figure 7.6.1-5 GSE Power Supply

Three regulated voltages are produced within the simulator:

+28v d-c ± .2v, 114 ma, adjustable from 23.5 to 34v
+12v d-c ± .3v, 40ma
+ 6v d-c ± .1v, 48 ma

The regulated +28v d-c is used as the instrument input power source and the +12v and +6v are used to power GSE circuitry.

The voltage control potentiometer is factory calibrated and all settings are accurate to ± 0.1 volts.

7.6.1.6 Miscellaneous Outputs

The following signals and pulses are generated within the simulator but do not have individual front panel controls or adjustments.

16,384 Hz Clock

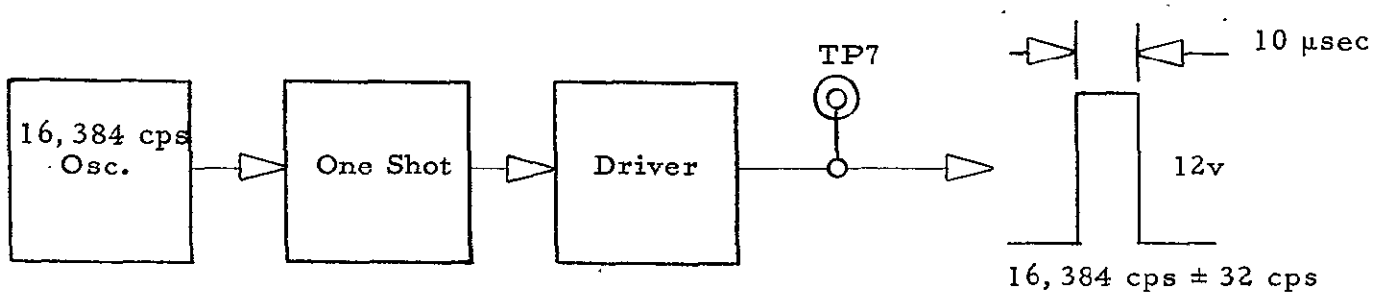


Figure 7.6.1-6 GSE Pulse Generator

Shift Pulses

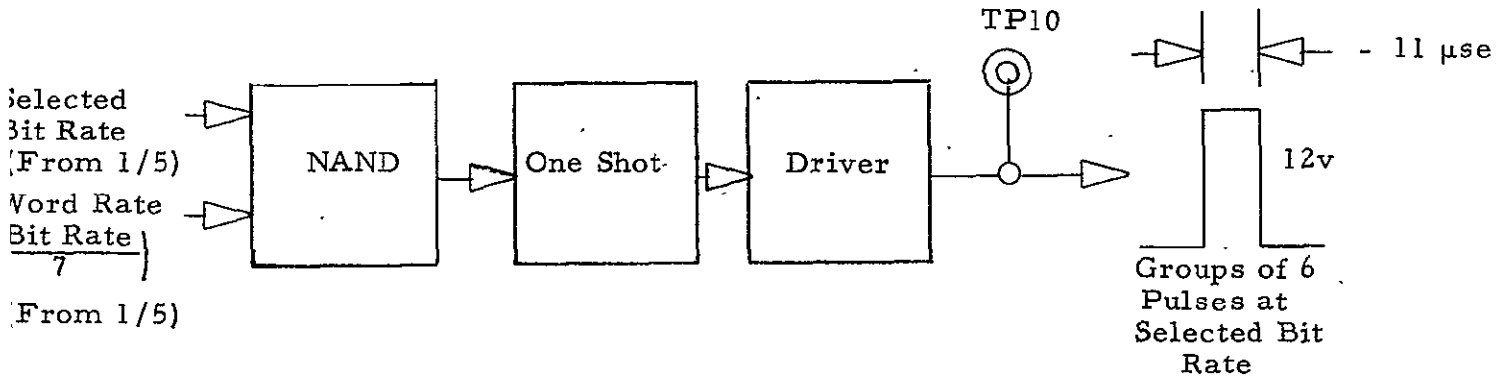


Figure 7.6.1-7 GSE Shift Pulse Generator

INSTRUMENT READOUT FORMAT.

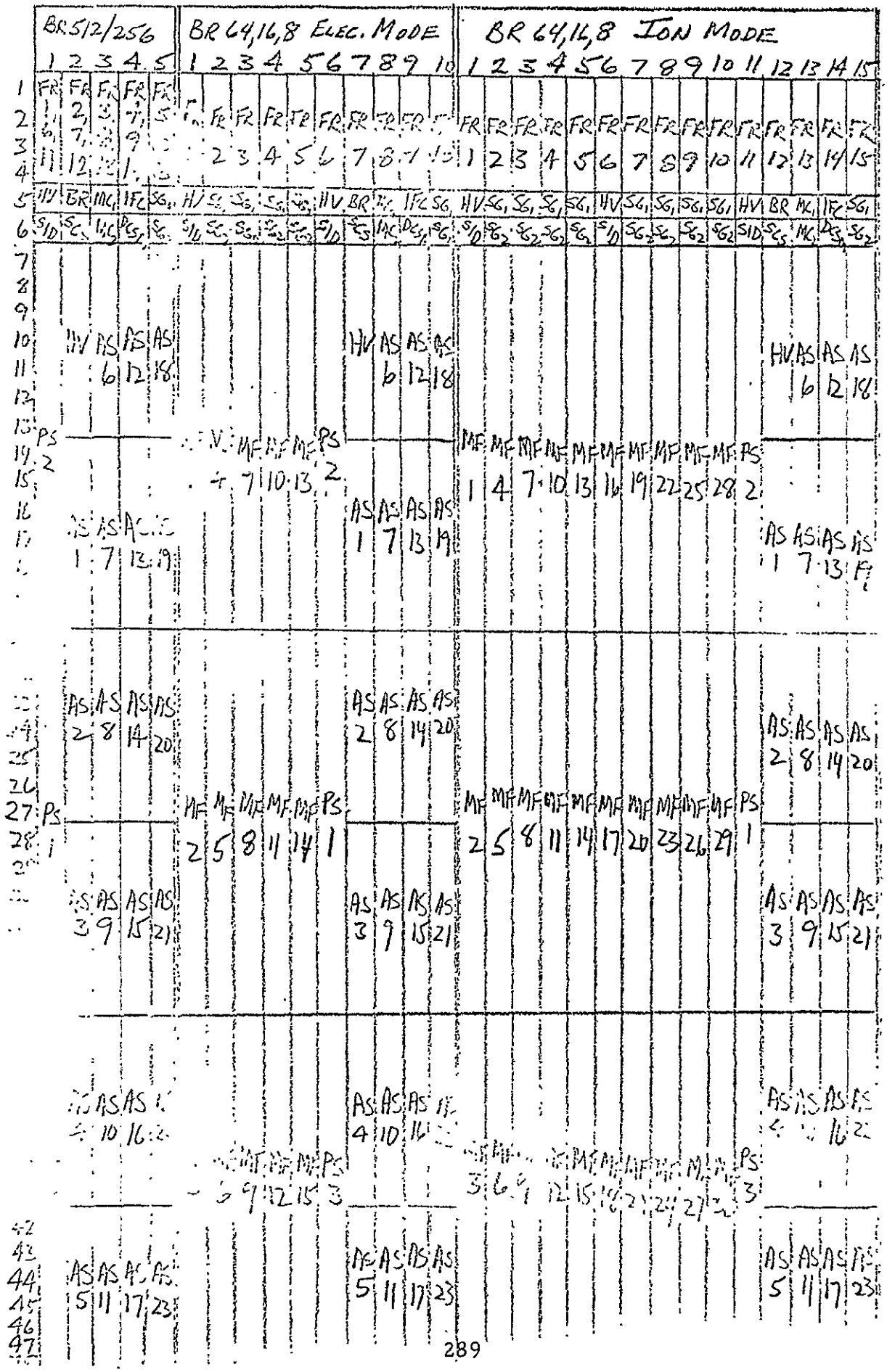


TABLE 7.6.1 A

7.6.2. Print Cycle Calculations

$$\frac{1 \text{ sec}}{512 \text{ bits}} \times \frac{7 \text{ bits}}{\text{DTU Word}} \times \frac{32 \text{ DTU Words}}{\text{Frame}} = .436 \text{ Sec/Frame} = 2.3$$

= 2.3 Frames/

$$\frac{512 \text{ bits}}{\text{sec}} = 1.96 \text{ ms/bit}$$

$$\frac{1 \text{ sec}}{512 \text{ bits}} \times \frac{7 \text{ bits}}{\text{DTU Word}} \times \frac{8 \text{ DTU Words}}{\text{Word Gate}} = .109 \text{ sec/Word Gate}$$

Print line =	Frame			Flux/HV		Flux/Sector
	X X	- X	-	X X X	-	X X X
	4 bits	2 bits		7 bits		7 bits

20 data bits/print line or 23 bit spaces/printline

23 bits x 1.96 ms/bit = 45 ms/print line

Print Cycle is 50 ms [17 ms data acceptance + 33 ms ID]

Print Sequence/Frame

X X - X - X X X - X X X
X X X - X X X
X X X - X X X
} 48 data bits

1st line = 20 bits
2nd line = 14 bits
3rd line = 14 bits
48 bits = 56 bit spaces = 109 m sec

Dwell time between frames = 24 DTU Words x 7 bit/DTU Word

$$\times \frac{1 \text{ sec}}{512 \text{ bit}} = 342$$

Storage Requirements: (From Timing Chart)
1st line = 18 m sec
2nd line = 36 m sec
3rd line = 54 m sec

Minimum time for decode to BCD = 6 ms

Figure 7.6.3-1. Monitor and Control Unit

7.6.3 Monitor and Control Unit

7.6.3.1 Input Data Encoding

Figure 7.6.3-1 shows a pho[illegible]nitor and Control Unit

The heart of the monitor and control unit is the circuitry for encoding the input digital data words into the correct formats for Nixie tube display and printing. As illustrated by the data format described in the preceeding sections, the data words consist of varying length and format according to the frame ID and mode of operation. This data must be segregated according to content and encoded from a binary code to the BCD code required for the printer and Nixie display.

Although the Franklin Printer selected for the application has a basic printing speed of 20 lines per second, it requires that data to be printed be held at the input for 17 milliseconds of the 50 millisecond cycle. Since data enters the GSE at a approximately 2 millisecond per bit at 512 BPS, some storage is required to avoid loss of data.

The monitor decode section accepts data as received and provides storage only as required to prevent loss of data. It utilizes the fact that the data for the greater portion of the instrument operation is seperable into 7 bit blocks and the fact that 14 bits of storage are required to complete sequential printing operations. The internal clock is derived from the instrument 16 KC clock to insure synch under all conditions and modes of operation. BCD encoding is accomplished by weighting the clock pulses and turning them on or off to the BCD counters according to the data.

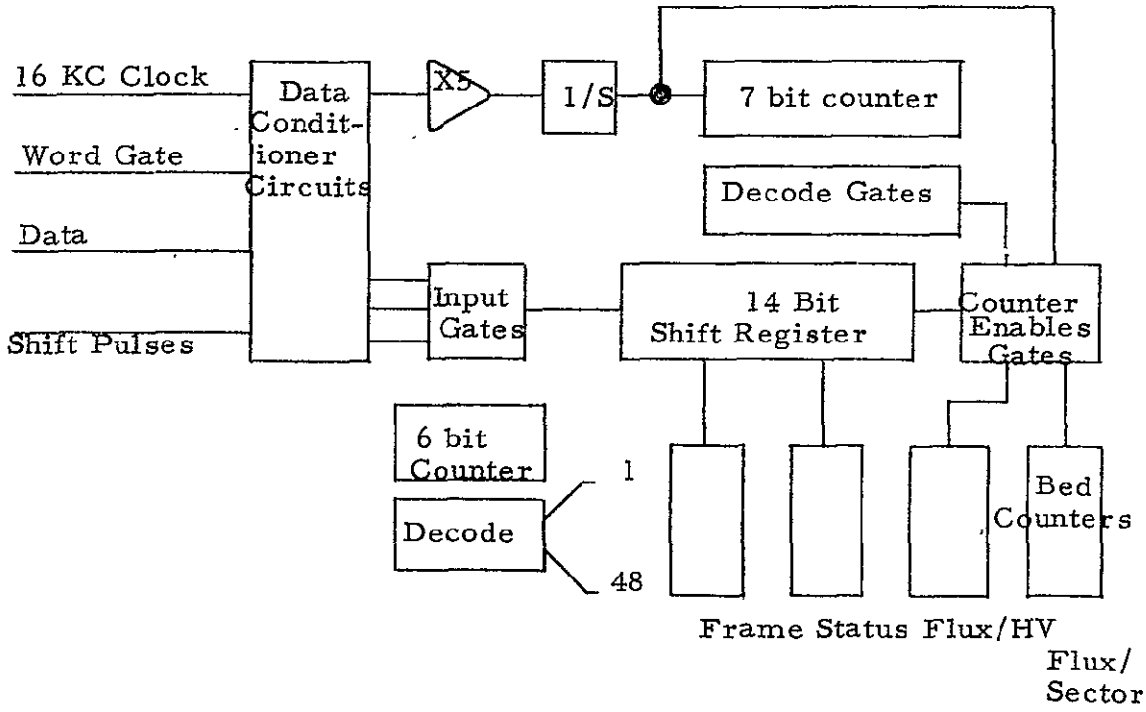


Figure 7.6.3-2 Input Data Encoding Circuit

For control of the NIXIE display, a circuit is used which encodes the Frame Identification No. (4 bits) and selects a given Frame number in combination with a 14 bit word identification selection. In this manner, it will be possible to select out any given word in any frame for display to permit instantaneous monitoring of given data words. This will simplify monitoring the instrument output at the high bit rates when reams of printer tape must be analyzed for observing proper operation. The NIXIE display also serves as a back-up for the printer if for any reason the printer is down.

The probe stimulus circuitry generates a ramp pulse which is variable in amplitude and can be selectively applied to coincide with any selected sector of the sweep. A third variable is the capability of being able to apply the stimulus during a particular selected High Voltage step to permit complete instrument check-out under polar scan conditions. Circuitry for accomplishing these results is indicated as follows:

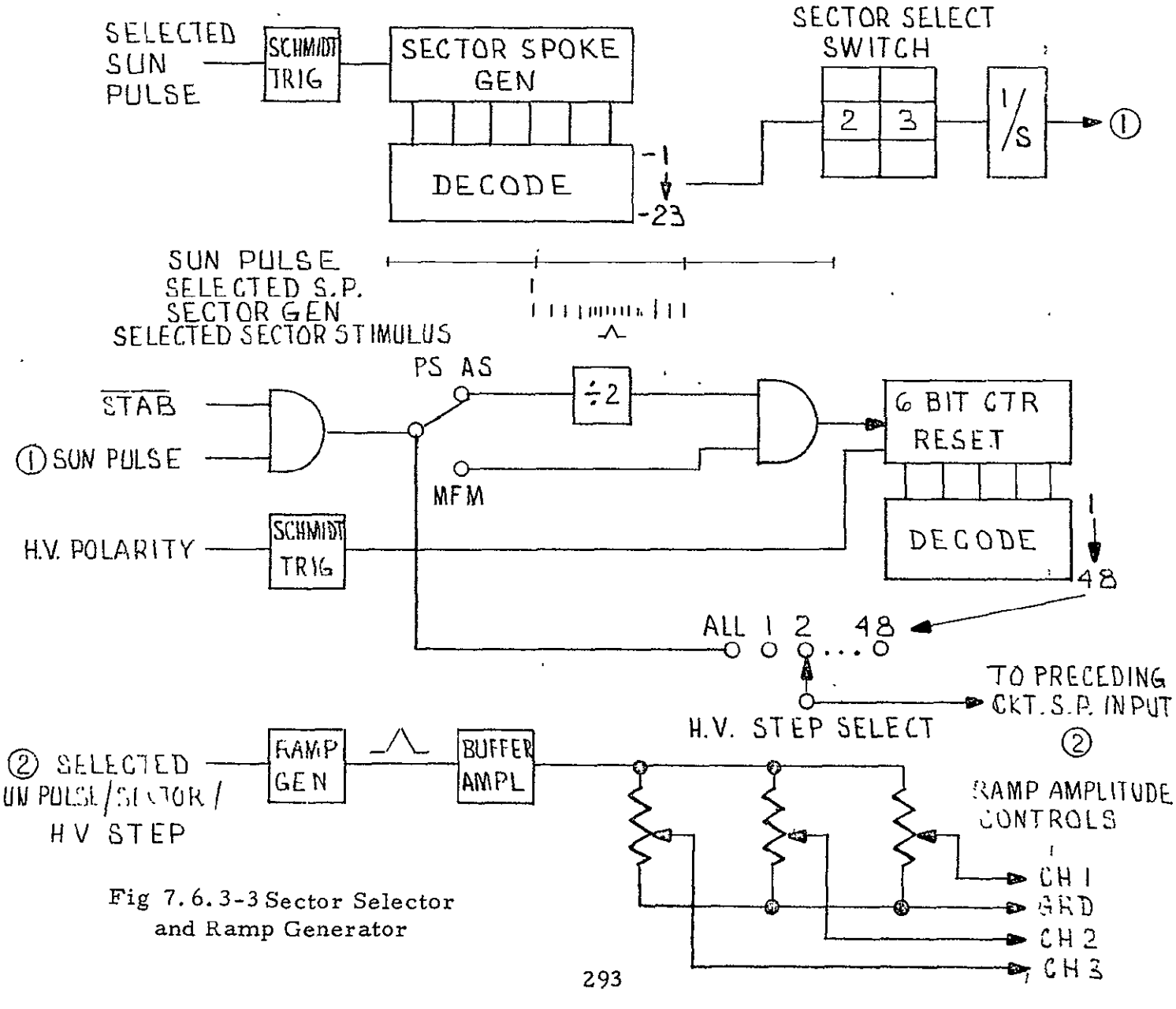


Fig 7.6.3-3 Sector Selector and Ramp Generator

7.6.3.2 High Voltage Programmer Control

In order to facillitate instrument test and calibration operations, it is desireable to permit rapid selection of a particular voltage step for instrument operation. The following GSE control circuit permits selection of the signal to the HV programmer in the instrument to cause it to step to and halt at the desired step number. Pulses are counted down at a 16 KC rate in a 6 bit counter which has a decoder and select switch to cause the pulse to halt stepping operations where the count reaches the number selected.

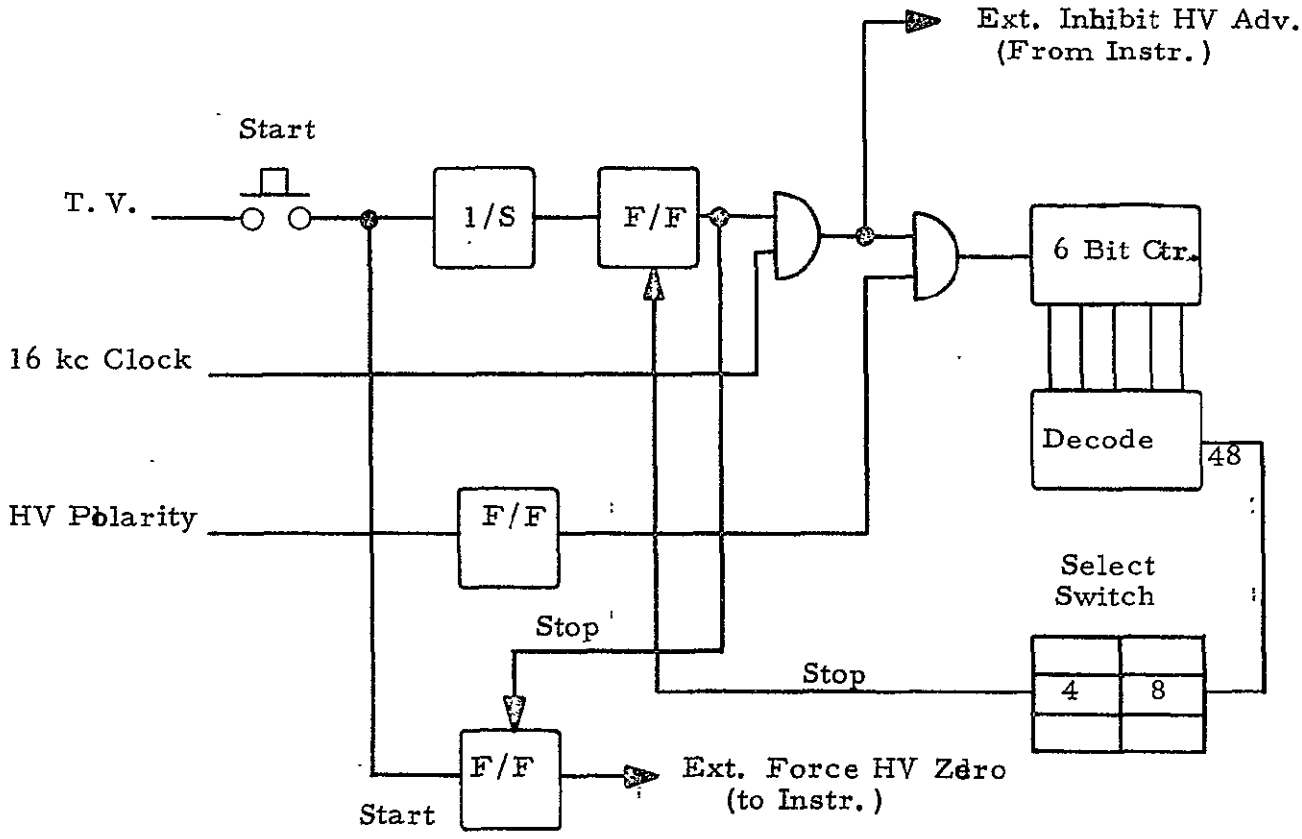


Figure 7.6.3-4 High Voltage Programmer Control

7.6.4 Meter Unit

A separate meter unit has been provided with the GSE for the purpose of monitoring all DC voltages. The basic meter is an Electro Instrument Model 620 Digital Voltmeter which is capable of measuring voltages from 0 to ± 750 volts to an accuracy of ± 0.5% of reading. The measured voltage is displayed on a 5 digit numeric readout. Auto ranging is included and the unit is capable of measuring a desired voltage inserted into the input jacks available at the front panel. The unit is adapted for Plasma Probe use by installation of the assembly into the standard GFE suitcase. In normal operations the accompanying selector switch is operated to present any one of the voltages available on the instrument test connector to the meter. For reading external voltages, the switch is set at the "EXTERNAL" position. The meter unit also contains 50 test points for monitoring all signals and voltages available from the instrument test converter. See Figure 7.6.4-1 for a photo of the Meter Unit.

7.6.5 Printer Unit (Figure 7.6.5-1)

The printer provided with the GSE is a Franklin Model 1200 Printer which has a basic printing speed of 20 lines per second. Ten print positions are provided with a format selected to conform to the Plasma Probe output data configuration.

7.6.6 Current Probe Unit (Figure 7.6.6-1)

The Current Probe Unit provides a means of calibration of the electrometer amplifiers by the insertion of known precision input currents. The generated current is continuously variable over five (5) decades from 10^{-9} to 10^{-14} amperes. The desired current may be set to three (3) significant digits by a front panel dial. The accuracy of the current level is primarily determined by the quality of the standard used to calibrate the current source. A Cary type 31 Electrometer is used as the primary standard and is certified to ±1%. A periodic check of a test voltage provides a means of calibrating the current source with the exception of the probe resistor. The large ohmic value probe resistor exhibits stabilities of better than one (1) percent per year.

A panel control provides for the selection of either a pulse or minus current. The current may be interrupted by the stabilize signal from the instrument or by the exterior stabilize panel control. The Current Probe exterior stabilize signal is also available for control of the instrument stabilize command.

The unit operates from power supplied by clip-in mercury batteries. Operational life on the original set of batteries is in excess of 2000 hours with a shelf life of several years.

The batteries are connected to the decade voltage divider through the polarity switch. The decade voltage divider sets the voltage on the potentiometer to either 20, 2, .2, or .02 volts. The ten-

Figure 7.6.4-1. Meter Unit

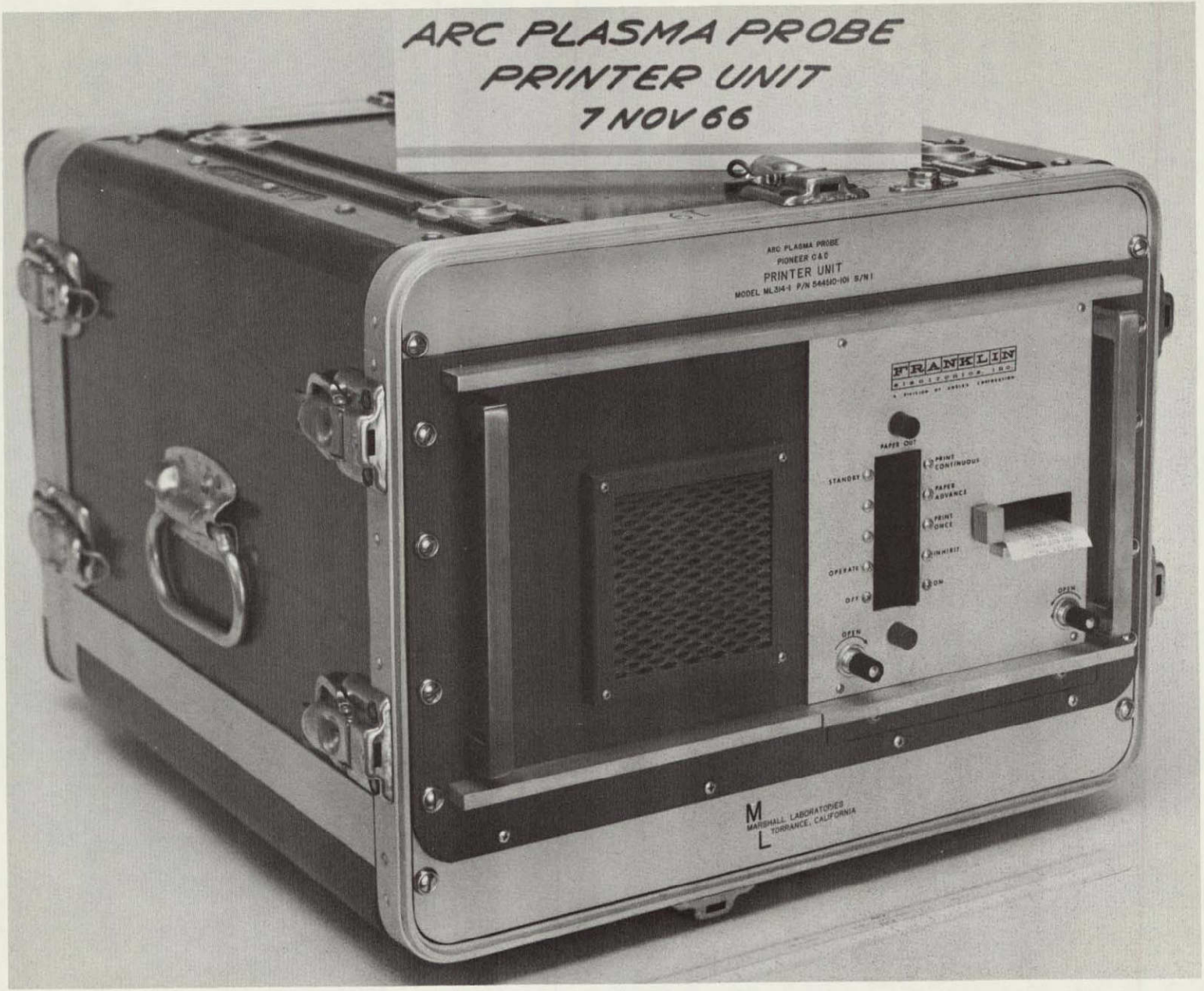


Figure 7.6.5-1. Printer Unit

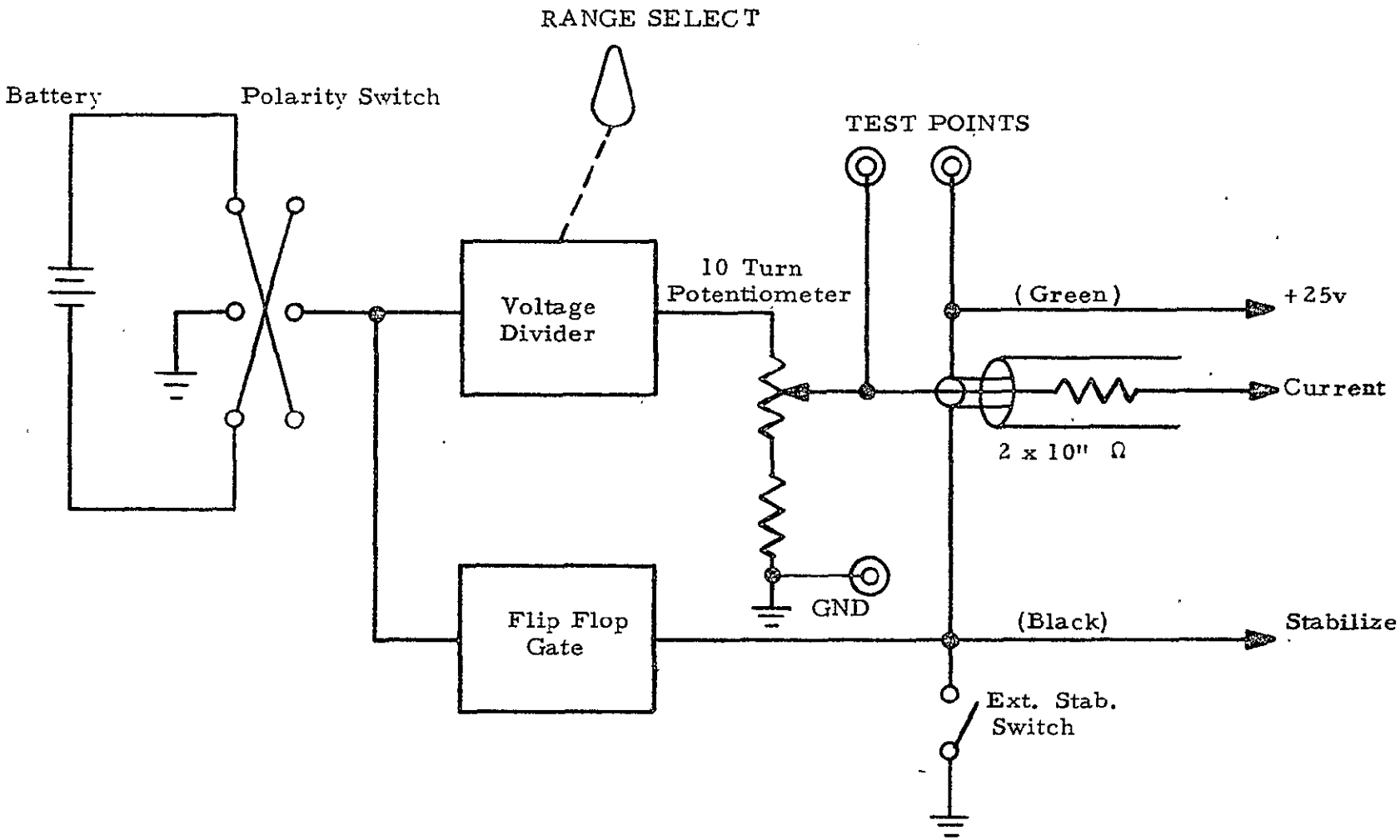


Figure 7.6.6-1 Current Probe

turn potentiometer sets the voltage into the probe to a fraction of the decade divider voltage. The current obtained is the potentiometer voltage divided by the probe resistance, 2×10^{10} (i.e., $20v/2 \times 10^{10}\Omega = 10^{-9}A$) or 2×10^{12} ohms external pulse or the pulse generated by the exterior stabilization pushbutton, causes the current to be interrupted by an electronic switch.

7.6.7 Demodulator

The function of the demodulator is to convert the pulse width flux data from the instrument into a high accuracy real time proportional d-c signal.

The schematic in Figure 7.6.7-1 shows five buffers, an A/D clock, one 7-bit ripple counter, four 7-bit storage registers, four each of ladder driver and ladder adder blocks. Each block has seven drivers driving seven ladder inputs and having one output. Figure 7.6.7-2 shows the ladder adder schematic; Figure 7.6.7-3 shows the A/D clock schematic.

The sample command signal starts the A/D clock and resets the ripple counter with its leading edge. The clock puts out the first pulse 8 microseconds after the leading edge of the sample command. The pulse width modulator signal begins 3 microseconds after the sample command. The trailing edge of this signal is used to transfer the contents of the ripple counter to the storage register. These outputs are fed through the ladder drivers and finally summed up in the ladder adders.

The analog d-c output is calculated to be 33mv/bit. This output is a minimum when the maximum flux. Thus when there are 127 bits in the counter the output is nearly 0V d-c. As the count down to 0 begins, the voltage will increase by 33 mv ± 1 mv. Thus at 0 bits the output will be:

$$\frac{127}{128} \times E_s \quad \text{where } E_s = 4.267 \text{ volts}$$

$$\text{Therefore} \qquad E_o = \frac{127}{128} \times 4.267 = 4.224 \text{ volts}$$

The instrument uses CLC JK-31 flip flops in the ripple counter and storage registers. It provides all its power requirements by Con Avionics HT15-0.45A and HT5-2.0A power supplies. The HT5-2.0A is adjustable to give 4V to 5V with ± 0.5 regulation.

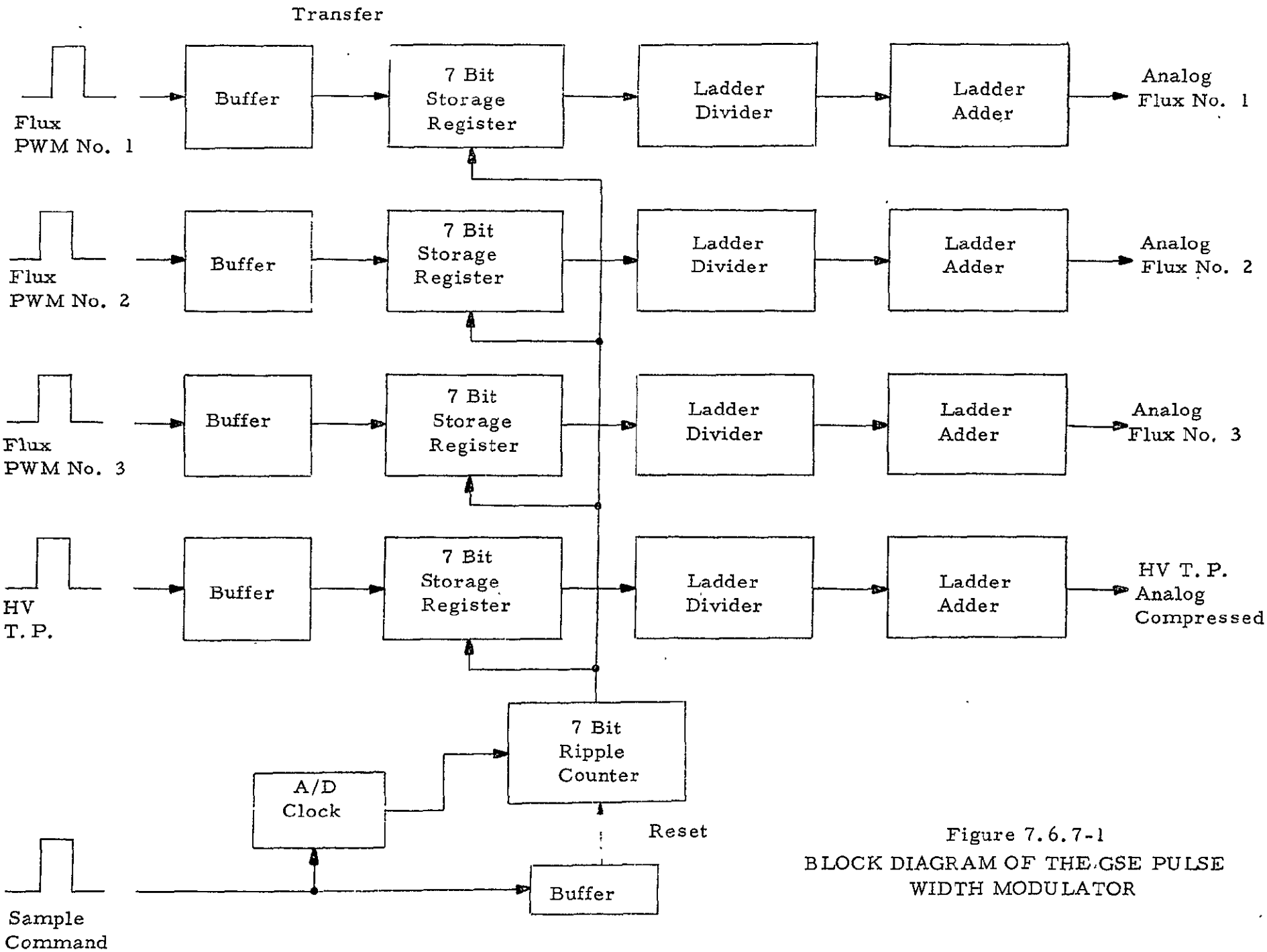


Figure 7.6.7-1
BLOCK DIAGRAM OF THE GSE PULSE WIDTH MODULATOR

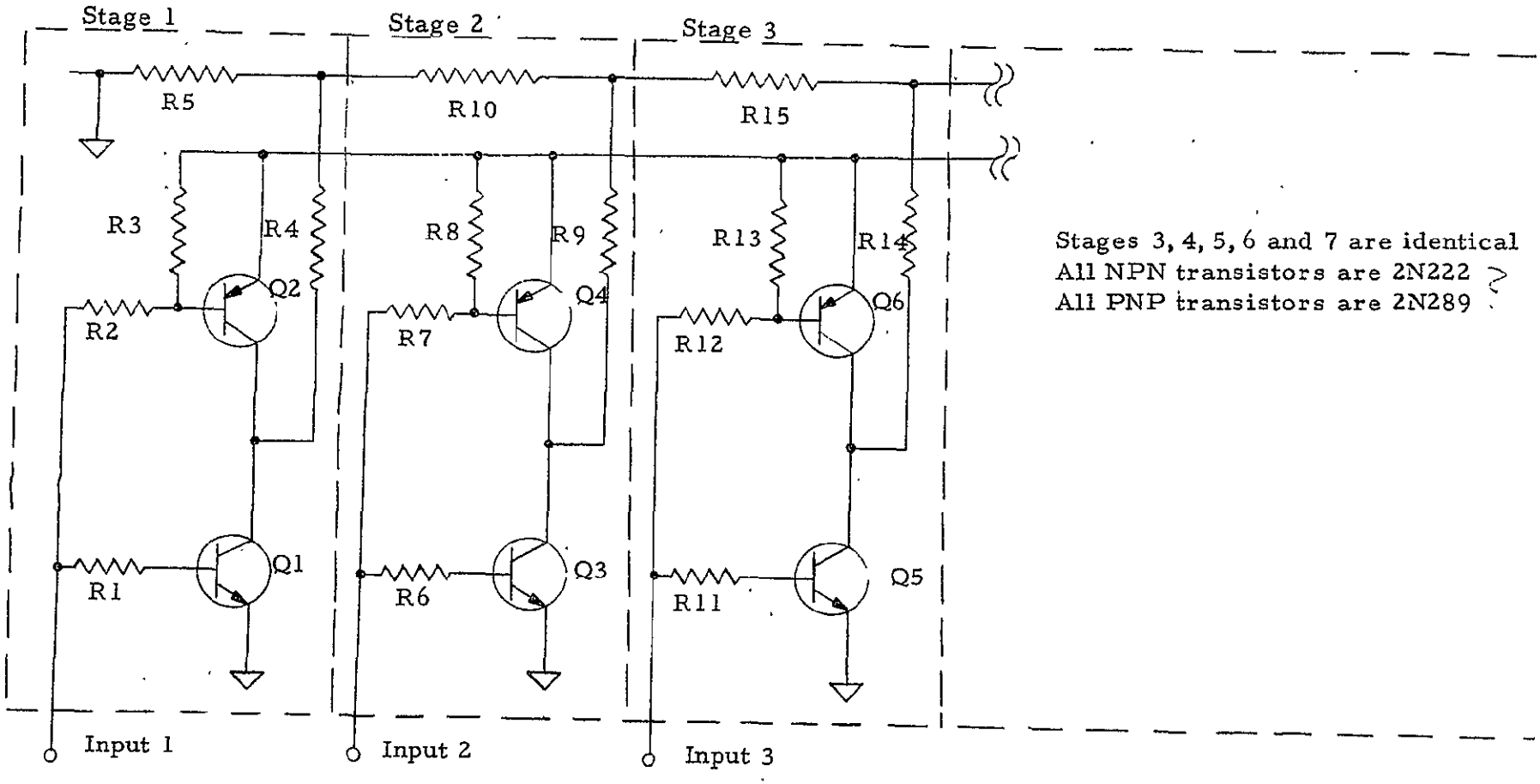


Figure 7.6.7-2 Ladder Adder Schematic

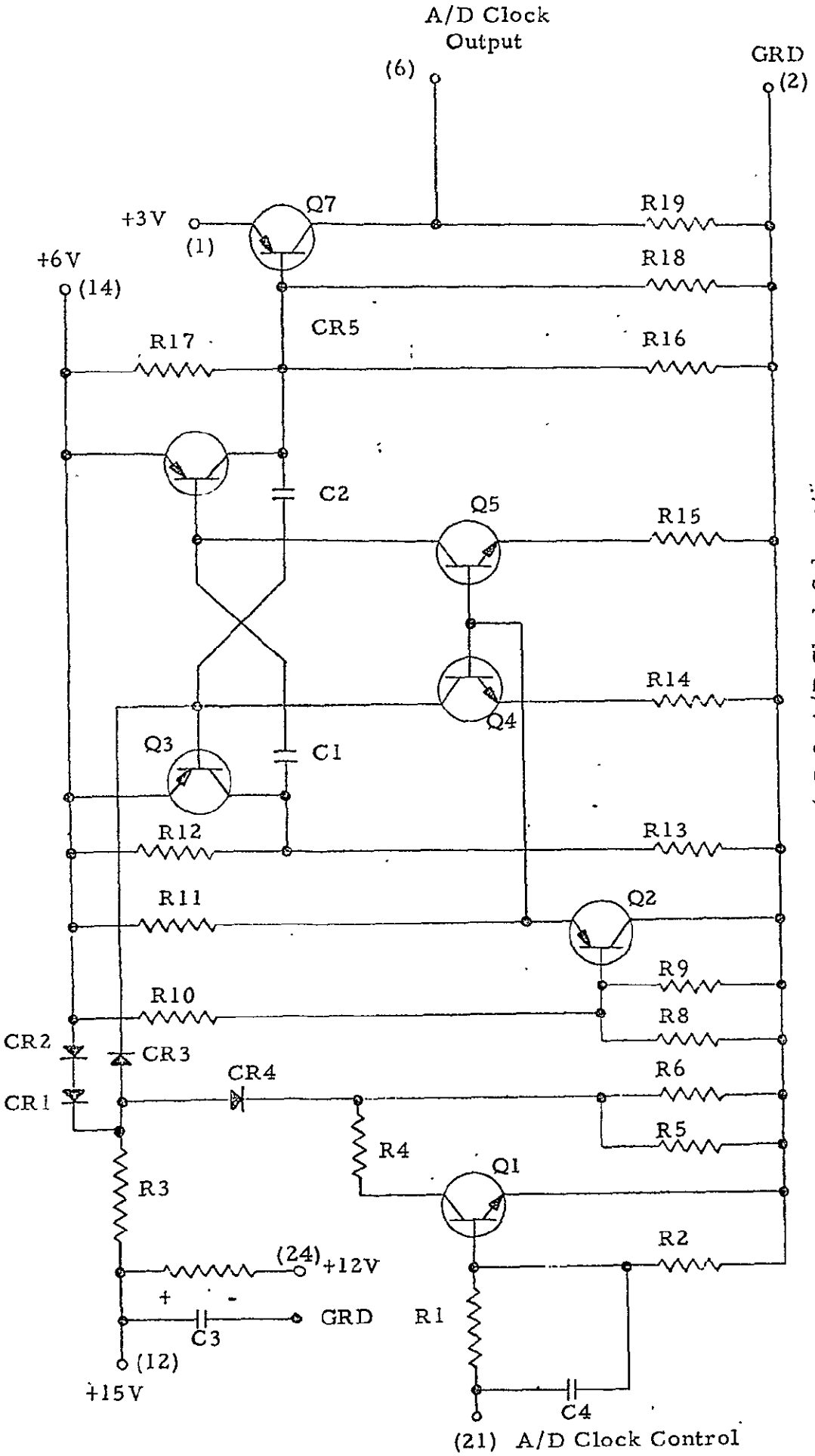


Figure 7.6.7-3 A/D Clock Schematic

8.0 PROBLEM AREAS AND SOLUTIONS

Three problem areas encountered during the program and their solutions are discussed in the following paragraphs.

8.1 Electrometer Tube

Plasma Probe instrument 8C05-1 experienced amplifier drift during retest sinusoidal vibration for qualification level tests. Excessive time for stabilization of a target amplifier was noted, along with amplifier drift. Investigation revealed the inability of the electrometer tube, 8520, to withstand the amplified vibration levels it was subjected to. Sinusoidal vibration maximum had been about 20g, with an estimated amplification in excess of 5.

A structural integrity analysis of the Analyzer and Optics assembly was performed with the intention of damping the assembly to reduce the amplified "g" levels seen by the electrometer tube. Nine low-level sinusoidal exposures were used to analyze and determine a solution to the vibration problem. Both a foam collar mount around the tube and soft wiring to the tube pins for isolation of the vibration stimulus were the answers for successful performance. It is recommended that good mechanical isolation be provided in subsequent designs.

8.2 Suppression Voltage Noise

Random and system noise was noticed on the output when the instrument was fabricated. This noise was being introduced through the suppression grid by the suppression voltage power supply.

An RC filter on the suppression grid power supply output reduced the noise read out errors from the order of 18-25 bits to 7-12 bits.

A quieter suppression voltage power supply with adequate filtering is recommended for the design of the next instrument.

8.2 High Voltage Corona

The analyzer plate stepping high voltage power supply exhibited corona problems during the first flight. Corona appeared during the higher energy steps.

It was determined that the corona was due to outgassing of the instrument during the early phase of flight. The instrument was turned off for approximately two weeks to allow sufficient outgassing, and was then turned back on with no problems re-appearing thereafter.

The subsequent units were installed with the capability, by command, to suppress the last four high voltage steps. It is recommended that the above solution be employed on subsequent systems; it is also recommended that low outgassing materials be used.

An additional high voltage problem occurred in the analyzer plate stepping HVPS during checkout of this subassembly. Due to tight weight and voltage constraints on the instrument, optimum clearances could not be achieved in all areas. This resulted in some corona effects within the doubler module. Proper potting of this sub-assembly eliminated this problem. We recommend that more attention be given for adequate clearances to high voltage points and that good potting and packaging techniques be employed.