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DEVELOPMENT OF GaAs AND $GaAs_{1-x}P_x$ THIN-FILM BIPOLAR TRANSISTORS

BY
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16. Abstract

A study of several parameters which limit the current gain of GaAs bipolar transistors has led to the development of vapor-grown n-p-n GaAs transistors with reproducible stable current gains as high as 30 at room-temperature and 15 at 300°C. These transistors have nearly flat I-V characteristics to voltages greater than 50 V. The technology by which such transistors have been fabricated utilizes a chemical etch of $NaOH:H_2O_2$ to expose portions of the middle (base) layer of a three-layered vapor-grown structure for contacting. With a post-fabrication HCl surface treatment transistor gains have been increased to values as high as 90, although these exceptionally high gains degrade to their pre-treated values in about an hour due to the reversion of the GaAs surface to its pre-treated condition.

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SUMMARY

The objective of this research program has been to develop a vapor-grown bipolar transistor of GaAs capable of operation at an ambient temperature of 300°C. As a direct result of research efforts under this program, GaAs bipolar transistors with stable current gains up to 30 at room-temperature and 15 at 300°C can now be reproducibly fabricated from vapor-grown n-p-n structures. In addition, a reduction in the voltage dependence of the current gain has resulted in reasonably flat transistor I-V characteristics to voltages greater than 50 V.

Recognition of the fact that sputter etching produces a region of high surface recombination in GaAs played a key role in obtaining the results above. The fact that our initial sputter-etched transistors yielded current gains significantly less than expected (15 at 25°C, 8 at 300°C) led to an examination of alternate fabrication techniques. A chemical etch of $NaOH:H_2O_2$ has been found to provide significant increases in transistor current gain and yield, resulting in the gains of 30 at room-temperature and 15 at 300°C mentioned above. In addition, the gain of transistors prepared by chemical etching can be increased still further with a post-fabrication surface treatment to values as large as 90 at 25°C. However, the increased gains brought about by the surface treatment are found to degrade back to their as-fabricated values over a period of time on the order of an hour.

In order to prepare more complex geometries suitable for practical GaAs transistors, efforts during this investigation also have been directed to the development of a photolithographic technology for vapor-grown GaAs structures. With this technology, transistors have been prepared with a resolution of less than 3 μm, and they have been found to be capable of operation to temperatures of 300°C with a gain of about 5.

Finally, the excessive leakage currents for n^+-p junctions prepared in a two-step vapor-growth sequence through an SiO_2 mask have been shown to originate at the semiconductor-epitaxy interface, but have not been eliminated. To the contrary, p^+-n junctions prepared similarly display low leakage currents, presumably due to a slight displacement of the junction during growth.

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I. INTRODUCTION

Although it has long been recognized that GaAs has significant potential for use in high-temperature transistors, this potential has never been fully realized. Until recently, the major obstacle to the fabrication of high-temperature GaAs transistors has been the difficulty in preparing three-layer structures with a necessarily thin base region while maintaining good p-n junction characteristics and minority-carrier lifetimes at elevated temperatures.

Approximately 18 months ago RCA Laboratories embarked on a transistor research program for the National Aeronautics and Space Administration. This program centered around the use of vapor-grown epitaxial layers of GaAs and $GaAs_{1-x}P_x$ for transistor preparation. The primary objective of this research was to examine the potential of the vapor-grown structures for bipolar transistor operation at temperatures up to 300°C.

During the first portion of this program (ref. 1), the potential of vapor-grown three-layered transistor structures was well established. Minority-carrier lifetime measurements on vapor-grown p-n junctions revealed that the electron lifetime and diffusion length in p-type material were nearly temperature independent between 25° and 300°C. More importantly, GaAs transistors, fabricated for the first time from structures prepared entirely from vapor-growth, were found to possess current gains which were also nearly independent of temperature to 300°C. For GaAs n-p-n transistors with base widths between 1 and 2 μm, current gains up to 10 were obtained at room-temperature and up to 5 at 300°C. In addition, the leakage currents of the base-emitter and base-collector junctions for vapor-grown transistor structures were found to be acceptably small ($J \lesssim 10^{-2}$ A/cm^2) at 300°C. Previous transistors prepared by high-temperature diffusion techniques were found to degrade catastrophically at high temperatures, with current gains dropping by orders of magnitude between 25° and 300°C. Such transistors were also plagued by leakage currents about an order of magnitude higher than those for the vapor-grown junctions (ref. 2), thereby seriously hampering high-temperature operation.

The primary objective of this second portion of our research program has been to optimize and develop improved transistor structures and fabrication procedures for GaAs n-p-n transistors in order to provide higher current gains at room-temperature and at 300°C. In this regard, efforts have been directed to those areas which most strongly affect transistor current gain, and include consideration of the emitter injection efficiency, the base transport factor, and surface recombination. Special emphasis has been placed on efforts to develop a technique for exposing portions of the middle (base) layer

for contacting; three different techniques have been extensively investigated: sputter etching, chemical etching, and vapor-growth through SiO_2 masks. Of these, chemical etching has been found to provide significantly increased current gains, with values as high as 90 obtained at room-temperature and 15 at 300°C. Details of the fabrication techniques and their effects on GaAs transistor current gain are treated in the sections below.

II. TECHNICAL DISCUSSION

A. PARAMETERS AFFECTING CURRENT GAIN IN GaAs TRANSISTORS

In the Final Report covering the first part of our research (ref. 1), we described GaAs sputter-etched transistors with room-temperature current gains up to 10. These devices had base widths of 1.5 μm, base acceptor concentrations of 2×10^{17} cm^{-3}, and emitter donor concentrations of 2×10^{18} cm^{-3}. In order to increase the current gain in the GaAs transistors still further, it is essential to examine each of the parameters which can limit the current gain, namely, the emitter injection efficiency, base transport factor, and surface recombination. In the sections below, these are examined in regard to their effects on transistor gain. It will be shown that optimization in each of these areas is required to improve the current gain of our GaAs vapor-grown transistors.

1. Emitter Injection Efficiency

The emitter injection efficiency, γ, of an n-p-n transistor is defined as the fraction of the total current which passes through the emitter-base junction in the form of electrons injected into the p-type base layer. An expression for the emitter injection efficiency can be readily derived*, assuming ideal diffusion currents across the emitter-base junction. Such an expression is

$$\gamma = \left[1 + \frac{N_b}{N_e} \sqrt{\frac{\mu_n \tau_n}{\mu_p \tau_p}} \tanh \left(\frac{W_b}{L_n} \right) \exp \frac{E_{gb} - E_{ge}}{kT} \right]^{-1} \qquad (1)$$

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*An expression for the ratio of hole-to-electron currents for a homojunction can be found in: J. Lindmayer and C. Y. Wrigley, "Fundamentals of Semiconductor Devices," Van Nostrand Co., New York (1965), p. 71, eq. (3-9). Here, $\tanh (W/L_p)$ is assumed to approach unity for the short diffusion lengths expected in our heavily-doped emitter.

The relationship for the ratio of hole-to-electron current for a homojunction and a heterojunction is given by H. Kroemer, Proc. IRE 45, 1535 (1957). The effective masses are assumed to be the same in the base and emitter.

Here, N_b and N_e are the *majority* carrier concentrations in the base and emitter, respectively. μ and τ are the minority carrier mobility and recombination lifetime, W_b is the base width, and L_n is the diffusion length of minority carrier electrons in the base. E_{gb} and E_{ge} are the energy gap for the base and emitter, respectively. The factor $\exp(E_{gb} - E_{ge}/kT)$ accounts for the possibility of a heterojunction occurring due to small differences in the GaAs energy gap in the heavily doped emitter and base regions.

In order to improve the emitter injection efficiency in an n-p-n GaAs transistor, one can theoretically:

(a) increase the emitter doping, thereby increasing N_e
(b) decrease the base doping, thereby decreasing N_b
(c) decrease the base width, W_b
(d) increase the emitter energy gap, E_{ge}
(e) decrease the base energy gap, E_{gb}.

Increasing the emitter concentration significantly above the present concentration of 2×10^{18} cm^{-3} has two disadvantages. First, at larger Se concentrations, Ga_2Se_3 precipitates (ref. 3) and gallium vacancy complexes (ref. 4) are known to occur, which almost certainly would reduce τ_p in Eq. (1), and thereby tend to reduce the emitter injection efficiency. Second, an increase in the donor concentration would reduce the effective energy gap, E_{ge}, of the GaAs emitter due to smearing of the conduction band edge with a broadened impurity band (ref. 5). The heterojunction caused by this energy gap shrinkage would also tend to reduce the emitter injection efficiency given in Eq. (1).

Since the acceptor concentration in the base is relatively low, impurity banding is small, and E_{gb} is not significantly altered. It therefore becomes desirable to reduce the acceptor doping below 2×10^{17} cm^{-3}, so as to increase the emitter injection efficiency directly, according to Eq. (1). Although the actual value of γ is difficult to estimate because of the uncertainty in the minority hole lifetime, τ_p, Eq. (1) clearly shows that the injection efficiency, and hence the current gain, should increase with a reduction in the base acceptor doping.

In order to enhance the emitter injection efficiency, efforts were made during this contract period to reduce the Zn concentration in the base by reducing the vapor-pressure of the Zn during vapor-phase growth.* In this way Zn concentrations as low as 7×10^{16} cm^{-3} were obtained in the base layer. Such values were determined by C-V measurements on n^+-p junctions prepared under growth conditions identical to those for the preparation of the transistors.

* See the Appendix of ref. 1 for the relation between Zn concentration and the temperature of the Zn source during vapor-growth.

The I-V characteristics of a sputter-etched GaAs n-p-n transistor prepared with the lighter base doping are shown in Figure 1 at temperatures of 112°, 227°, and 300°C. Here, the current gain is shown to increase somewhat with increasing temperature from a value of 3 at room-temperature and at 112°C to a value of about 8 at 300°C. This was the highest gain obtained at 300°C for *sputter-etched* transistors. For this particular material, room-temperature gains greater than 5 were consistently obtained, with values as high as 10 observed occasionally. Because of these reasonably encouraging results, Zn concentrations in the range of 7×10^{16} to 1×10^{17} cm^{-3} were employed in most of the transistors prepared during the remainder of this contract period.

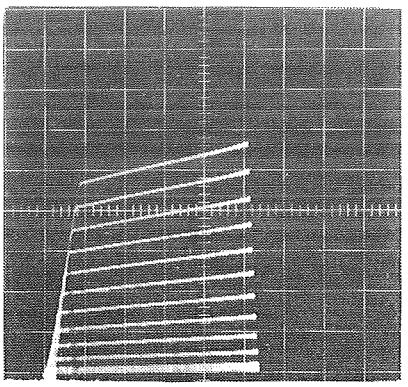
2. Base Transport Factor

The base transport factor, δ, for an n-p-n transistor is the fraction of electrons injected from the emitter which reach the collector without recombining in the base. The transport factor is expressed by the equation (ref. 6)

$$\delta = \operatorname{sech}\left(\frac{W_b}{L_n}\right) . \qquad (2)$$

To increase the transport factor, and hence the current gain, Eq. (2) simply requires decreasing the base width W_b. Such a decrease would also have the added benefit of increasing the emitter injection efficiency described by Eq. (1) in the previous section.

For the most part, previous sputter-etched GaAs transistors prepared by vapor-phase growth had base widths of 1.5 to 2 μm. However, the relatively slow growth rate of 0.5 μm/min (ref. 7) actually allows the preparation of somewhat thinner layers, perhaps ultimately as thin as 0.5 μm. To determine the extent to which the base width could be reduced, one n-p-n transistor structure was prepared with a base width only slightly greater than 0.5 μm. Transistors were successfully fabricated from this structure by sputter etching, and the gains of the resulting units were in excess of 15 at room-temperature, as shown in Figure 2. These gains were the highest obtained with sputter-etched transistors, consistent with the predictions of Eqs. (1) and (2), however the I-V characteristics of these transistors were highly non-linear with a large saturation resistance, and were not reproducible from unit to unit. In view of these problems, a width approaching 0.5 μm was considered to be too small for the technologies presently available. Hence, most of the GaAs transistors prepared during this contract investigation were confined to base thicknesses of about 1 μm, which did in fact reduce the problems associated with the transistor in Figure 2.

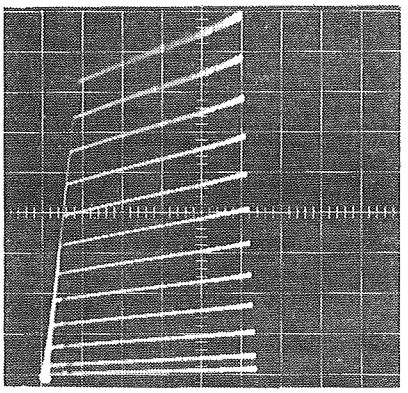


112°C

I_C = 0.5 mA/div

I_B = 0.1 mA/step

V_{CE} = 5 V/div

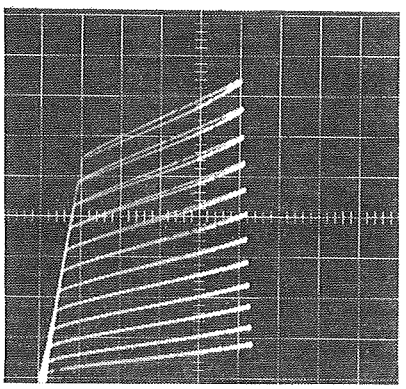


227°C

I_C = 0.5 mA/div

I_B = 0.1 mA/step

V_{CE} = 5 V/div



300°C

I_C = 1.0mA/div

I_B = 0.1 mA/div

V_{CE} = 5 V/div

Figure 1. I-V characteristics at 112°, 227°, and 300°C for a sputter-etched GaAs transistor with reduced base acceptor doping.

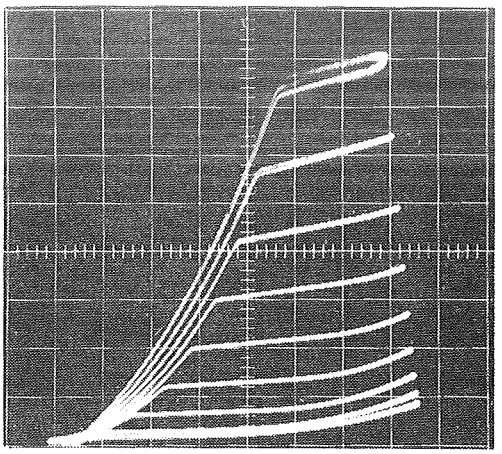


Figure 2. I-V characteristics at 25°C for sputter-etched GaAs transistor with a 1-μm base width.

In subsequent sections of this report, we will show that our best GaAs transistors were obtained with base widths of 1 μm.

3. Fabrication Damage and Surface Recombination

The first GaAs transistors fabricated from material grown entirely from the vapor-phase, and in fact most of the GaAs transistors fabricated prior to the start of this second portion of our research program, utilized a sputter-etching technique for exposing selected portions of the base for contacting. However, one question which remained unanswered during the initial phase of our research was the existence and extent of any possible damage in the GaAs caused by the sputter etching and the effects of such damage on current gain. Efforts to clarify this issue

were undertaken during the present contract period, as discussed below and in a subsequent section.

In our earlier research, a series of lifetime and diffusion length measurements was carried out on vapor-grown n^+-p GaAs junctions (ref. 1). These measurements indicated that minority carrier lifetimes for electrons in p-type GaAs were on the order of 5 to 10 nsec, with corresponding diffusion lengths of about 7 μm. From such measurements, and from Eqs. (1) and (2), the relationship between the theoretical current gain and the ratio of L_n/W_b was calculated for GaAs and $Ga_{1-x}P_x$ transistors (ref. 1). This graph was presented in our previous Final Report (ref. 1), but is included in the present report as Figure 3.

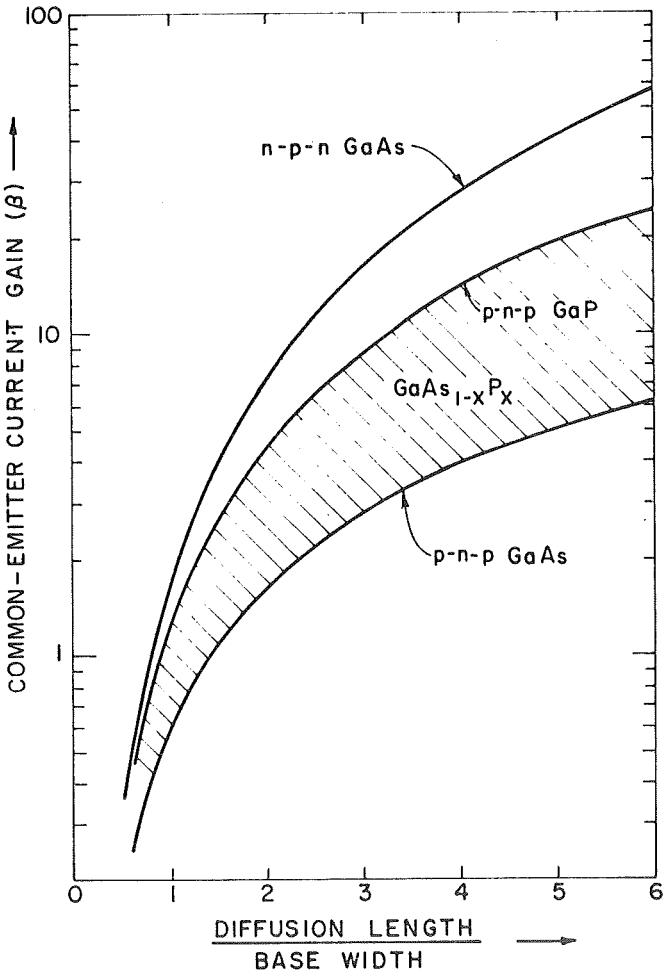


Figure 3. Current gain as a function of the ratio of diffusion length to base width for GaAs and $GaAs_{1-x}P_x$ transistors.

From this figure, we concluded that current gains on the order of 60 could be obtained with GaAs n-p-n transistors with 1-μm base widths. However, for GaAs transistors fabricated with the sputter-etch technique, the maximum current gain obtained has been 15, as previously discussed and illustrated in Figure 2.

The fact that current gains for transistors prepared by sputter etching are significantly less than theoretically predicted does suggest that sputtering may introduce damage leading to high surface recombination, which could clearly shunt the injected minority carriers and thereby reduce the current gain. For this reason alternate techniques for exposing the base layer for contacting were investigated. A chemical-etching technique, described in detail in the next section, was found to provide significant improvements in the current gain, presumably by reducing the surface recombination during transistor fabrication.

B. CHEMICAL ETCHING FOR GaAs TRANSISTOR FABRICATION

In the early stages of our GaAs transistor program, we briefly evaluated several chemical etches for penetrating the emitter layer of an n-p-n transistor. Two problems with chemical etches became apparent at that time: erratic etching rates and nonflatness over the etched regions of the wafer. In particular, "Caro's etch" (5 H_2SO_4:1 H_2O_2:1 H_2O) consistently produced deep "moats" about the edges of an etched pattern, thereby punching through the thin base layer in these regions. A variety of other commonly used semiconductor etches gave similar results.

In contrast, a NaOH:H_2O_2 etch (ref. 8) has been found to provide flatness to about 0.1 μm across the entirety of the etched regions, as determined by interferometric examination of several etched wafers. This result has also been confirmed by its successful use in fabricating several GaAs transistor structures without punching through base layers 1 μm thick. In addition, an etching rate of about 0.13 μm/min has been determined by a series of etches on a single GaAs wafer, as shown in Figure 4. This etching rate has been found to be reasonably reproducible from wafer to wafer. Particularly important for transistor fabrication is the fact that current gains of transistors fabricated with the NaOH:H_2O_2 etch are significantly higher than those previously obtained with sputter-etched GaAs transistors. The fabrication and evaluation of the chemically-etched GaAs transistors are described below.

1. Fabrication Procedure

GaAs vapor-grown n-p-n transistors have been prepared by depositing a thin (5000 Å) layer of SiO_2 over the emitter, photolithographically

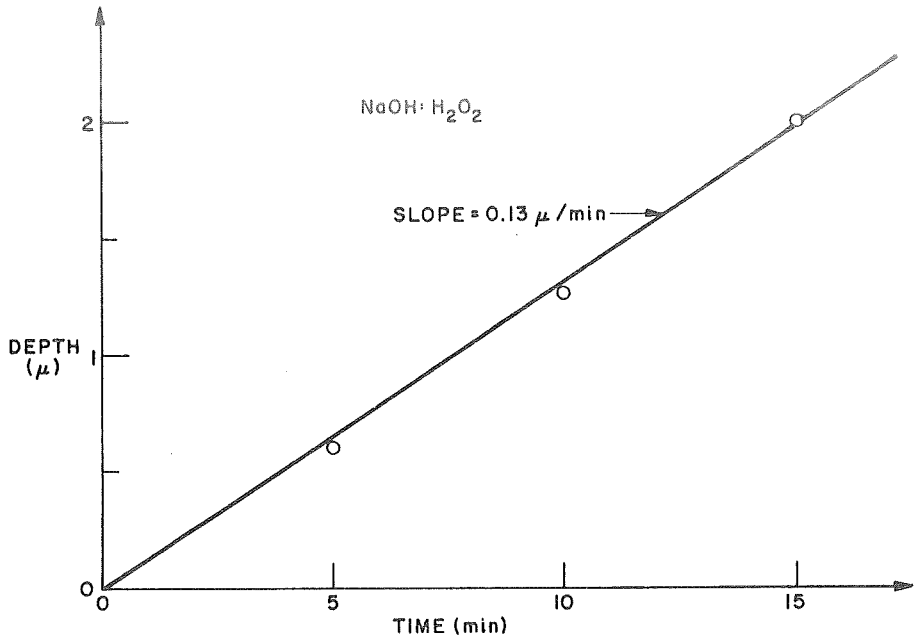


Figure 4. Depth of etching vs. etching time for NaOH:H_2O_2 on <100> GaAs.

etching a simple pattern through the SiO_2, and etching through the emitter and into the base with the NaOH:H_2O_2 etch. After evaporating Ag-Mn (ref. 9) onto the exposed base layer and Ag-Te (or Ag) onto the emitter, transistors are mounted on TO-5 headers with Au-Sn, ultrasonically wire-bonded, and evaluated electrically. It should be mentioned here that, in clear distinction to the sophisticated photolithographic patterns discussed in Section II.C on page 15, the work in this section utilizes a relatively simple transistor stripe geometry (ref. 1, Figures 3 and 4) contacted by visual alignment of eveporation masks onto relatively large area (10 by 20 mils) base and emitter patterns.

2. Current Gain and Yield

Since beginning the use of the NaOH:H_2O_2 etch, a large number of chemically-etched GaAs n-p-n transistors have been prepared, with current gains as high as 28 at room-temperature, as illustrated in Figure 5. Here the base width has been reduced to 1 μm in order to enhance the emitter injection efficiency and the base transport factor. A gain of 28 represents an improvement by a factor of 2 over the best sputter-etched transistor with a 1-μm base width (Figure 2). In addition, the transistors fabricated with the chemical-etching technique were susceptible to a post-fabrication treatment which resulted in further increases

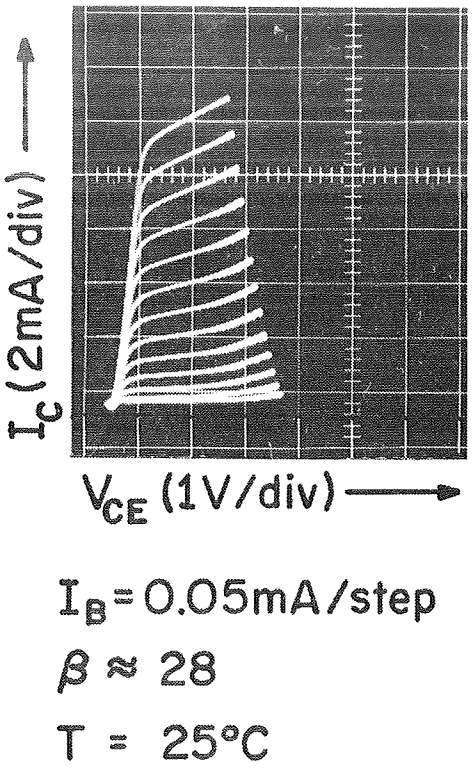


Figure 5. I-V characteristics at 25°C for chemically-etched, as-fabricated GaAs transistor.

in the room-temperature current gain, as discussed in Section II.B.3 on pages 14 and 15.

Several GaAs n-p-n transistors with room-temperature current gains between 8 and 28 in their as-fabricated condition were examined at elevated temperatures. These results are shown in Figure 6. Here, the gains are shown to be only weakly temperature-dependent between 25° and 300°C, with the most severe degradation being by a factor of 2. This result is in agreement with earlier conclusions concerning the relative temperature independence of low-gain transistors ($\approx$ 5) prepared by sputter etching. Note in Figure 6 the existence of two transistors with current gains approaching 15 at 300°C. Current gains on the order of 15 are the highest we have obtained at 300°C with our vapor-grown GaAs transistors, and are almost certainly directly attributable to the improved (chemical-etching) fabrication procedure. The I-V characteristics of one such transistor with a gain of about 12 at 300°C are shown in Figure 7.

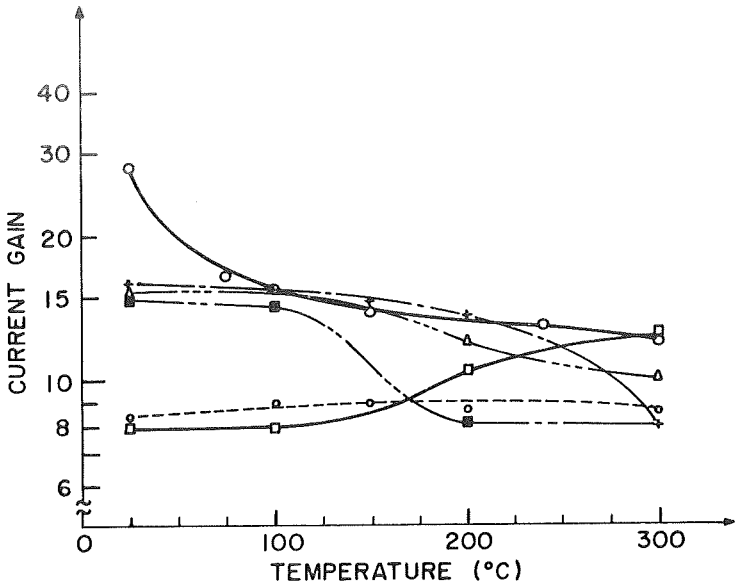


Figure 6. Current gain vs. ambient temperature for chemically-etched n-p-n GaAs transistors in as-fabricated condition.

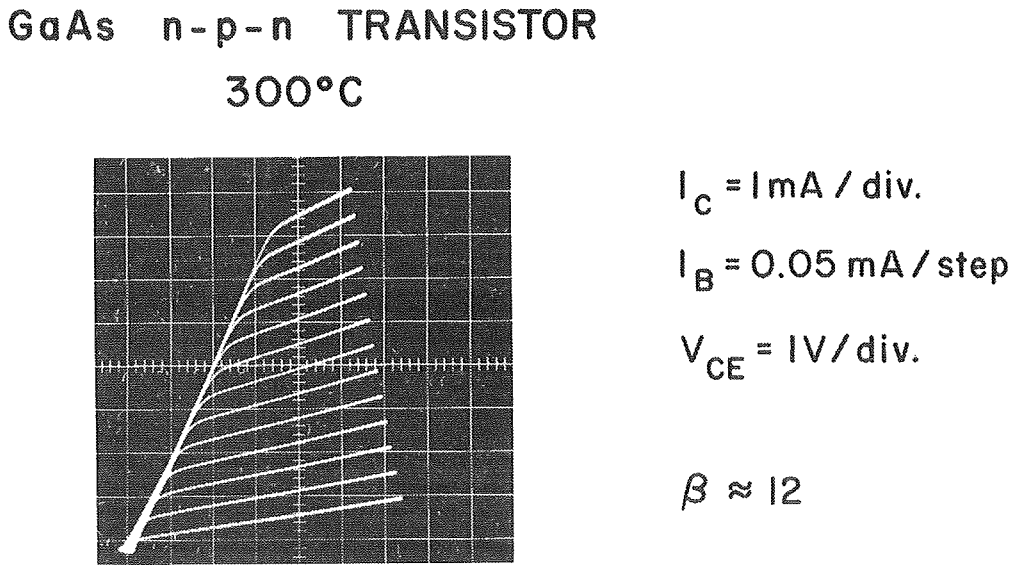


Figure 7. I-V characteristics at 300°C for chemically-etched, as-fabricated GaAs transistor.

In addition to the improvements in current gain brought about by the chemical-etching process, a similar improvement in the *yield* of transistors has been observed. This is apparent from the list of ten transistor structures in Table I which have yielded room-temperature

TABLE I

GaAs n-p-n Transistors Prepared by Chemical Etching

Growth No.	Base Width (μm)	Room-Temperature As Fabricated	Current Gain After HCl
2-26-70:1	1	28	90
5-8-70:1	1.5	11	--
5-8-70:2	1.5	25	40
5-13-70:2	1.5	9	13
5-13-70:3	1.5	10	20+
6-9-70:1	1	15	42
7-21-70:1	1	20	40
R684	1	32	40
R687	1	14	35
R703	< 1	22	30

current gains greater than 10 since the initiation of the chemical-etching process. The yield of individual transistors from any given three-layered vapor-grown transistor structure also has been increased substantially by the recent etching technology. The improvements in both current gain and transistor yield brought about by the chemical etching strongly suggest that the sputter-etched fabrication procedure produces surface damage in the GaAs wafer, resulting in additional recombination centers in the base, reduced minority carrier lifetime, and therefore reduced current gain.

Finally, we have found that thermal probing can generally be used after each $NaOH:H_2O_2$ etch to confirm our reaching the p-type base layer by the etching process. In this way, successive light etches have been used to gradually approach the proper base depth, thereby increasing the probability of reaching, but not penetrating, the thin base layer. The present yield of this process is estimated to be about 80%.

3. Post-Fabrication Surface Treatment

Since beginning the use of the $NaOH:H_2O_2$ chemical etch, current gains in the range of 10 to 30 have been obtained in several "as-fabricated" GaAs transistors. As mentioned briefly in the previous section, the gains of the transistors fabricated by the chemical-etching technique can be significantly increased by a post-fabrication surface treatment, namely a brief (5 to 10 sec) immersion in HCl or HF followed by a water and ethanol rinse. A typical improvement in the transistor gain at 25°C, before and after HCl immersion, is illustrated in Figure 8. Here, the gain was found to increase from a value of 9 before treatment to a value of 20 after.

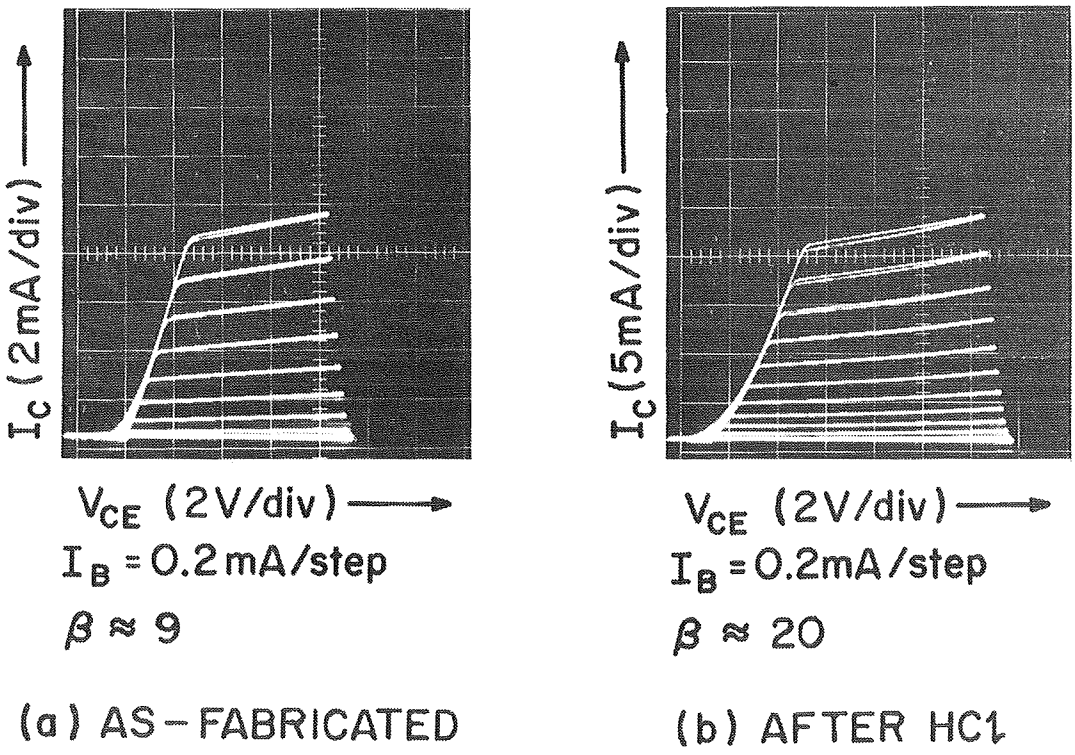


Figure 8. I-V characteristics at 25°C for chemically-etched GaAs transistor, before and after HCl surface treatment.

In this way, several GaAs transistors with current gains in excess of 40 at room-temperature have been obtained, as listed in Table I and shown in Figure 9. The characteristics in this figure are from four transistors fabricated from four different vapor-grown structures, each with a base width of 1 μm (except for the upper right characteristics, where the base width was 1.5 μm). As shown here, current gains as high as 90 have been attained with chemically-etched transistors followed by the post-fabrication surface treatment. A gain of 90 is the highest we have achieved during this investigation, and represents an improvement by about a factor of 9 over the highest gains available at the start of the second portion of our research. Interestingly, the previous vapor-grown GaAs transistors prepared by sputter etching could not be further increased by any known post-fabrication treatment, again, presumably due to the existence of a high-recombination damage layer which extends significantly into the base of the transistor. The existence of such a layer could not only limit the initial gain of a transistor, but could also shunt any further surface improvements. To the contrary, the lack of any significant damage layer in the chemically-etched transistors probably accounts for their initially higher gain, as well as their further improvement when the surface condition is enhanced with the HCl treatment. A current gain of 90 for a chemically-etched transistor with a 1-μm thick base layer is even somewhat higher than that predicted in Figure 3, confirming the absence of any undesirable shunting mechanisms.

One problem with the HCl or HF post-fabrication treatment described above is that the increased current gains degrade rapidly to their pre-treated as-fabricated values after a short period of time ($\sim$ 1 hour), as shown in Figure 10. However, after such degradation, the higher current gains can generally be restored by a repeated surface treatment. Since neither HCl nor HF perceptibly etches GaAs, the strong dependence of gain on such treatments indicates the importance of *surface* effects, and points to the need for future surface passivation studies on our present GaAs transistors. In this regard, layers of Al_2O_3 have been deposited on the fabricated transistors at 400° to 500°C in an atmosphere of HCl, however these depositions have not yet resulted in stabilization of gains higher than the as-fabricated values.

C. IMPROVED TRANSISTOR CHARACTERISTICS

The high-gain transistors presented in Figure 9 illustrate the quality of properly-fabricated vapor-grown transistor structures. However, each of the I-V characteristics in Figure 9 show two undesirable characteristics. First, the collector current begins to increase significantly at voltages in the range of 10 to 20 V due to a softening of the base-collector reverse bias characteristics in this voltage range.

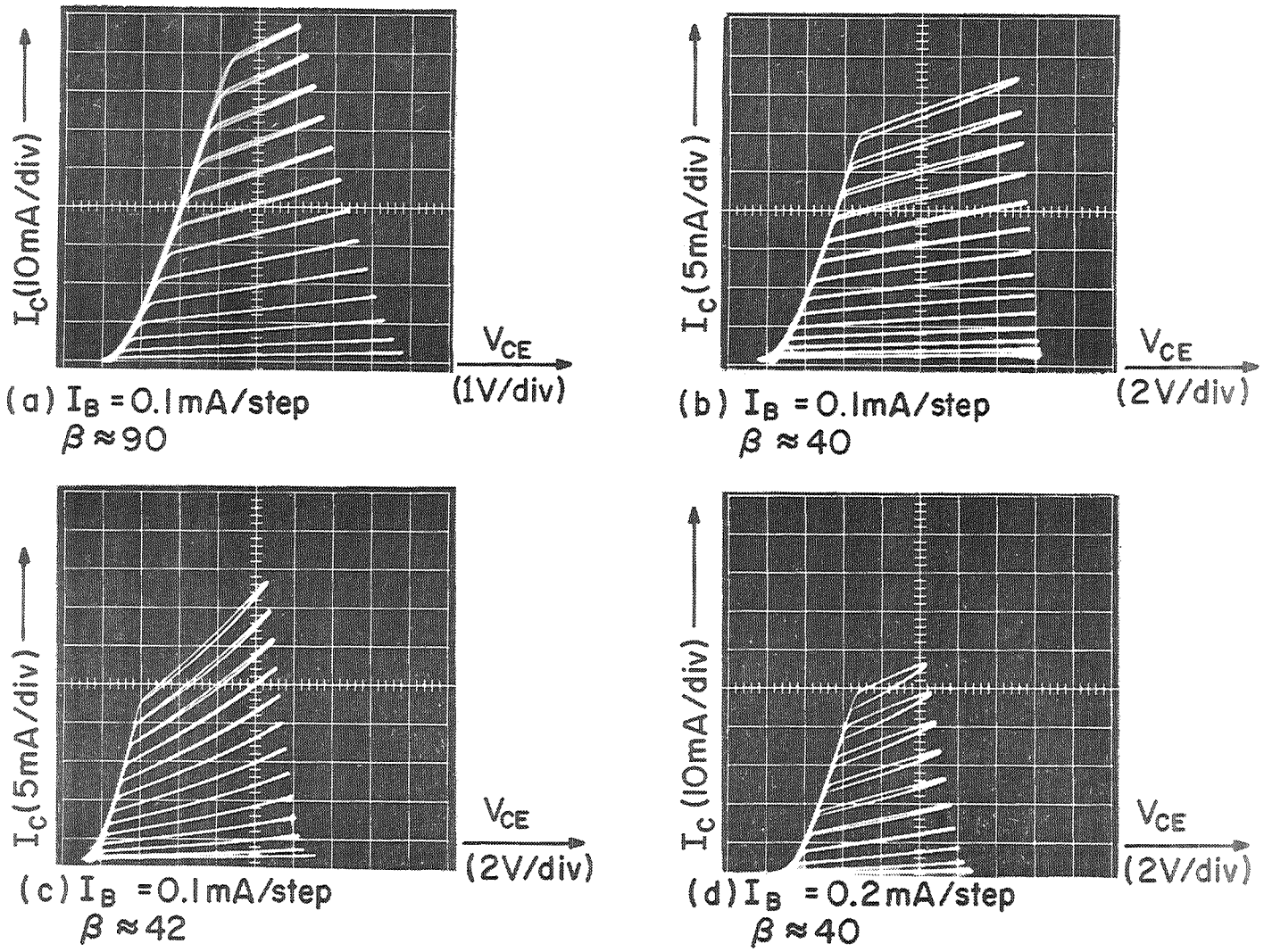


Figure 9. I-V characteristics at 25°C for several chemically-etched high-gain GaAs transistors after HCl surface treatment.

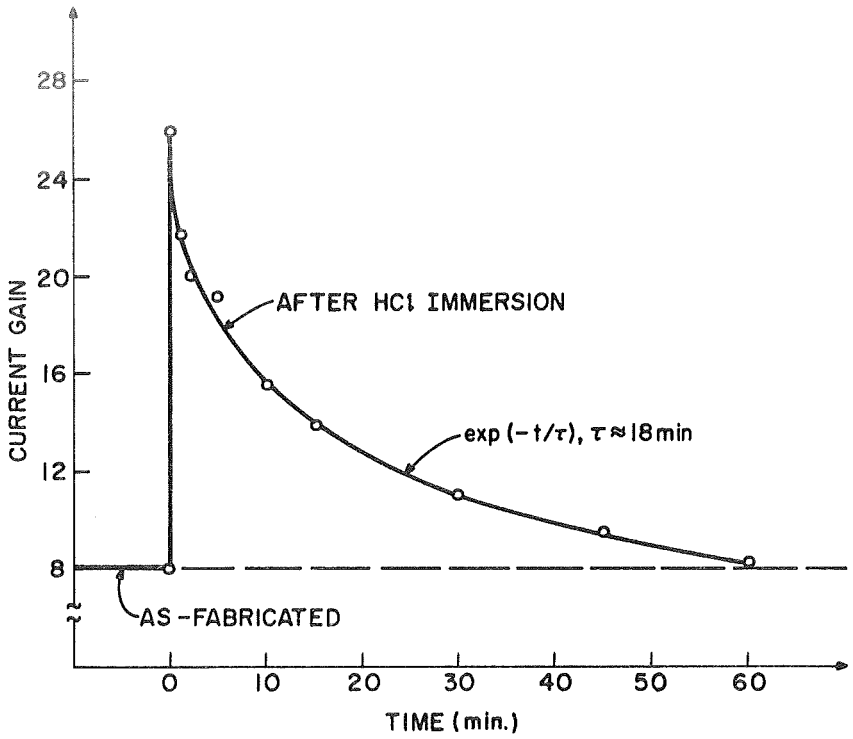


Figure 10. Gradual reversion of current gains to as-fabricated values after HC1 surface treatment.

Secondly, at any given base current, the collector current gain tends to increase slightly with increasing voltage, which is indicated by the gradual increase in the spacing of two adjoining I-V characteristics separated by a unit step in base current. This effect is due to a widening of the base-collector depletion layer into the narrow base region, which reduces the effective width of the base and thereby increases the current gain (ref. 10).

Each of the above problems can be reduced by reducing the donor concentration in the collector. At lower collector doping, the reverse breakdown voltage of the base-collector junction increases (ref. 11), thereby extending the soft region of the pre-breakdown characteristics to significantly higher voltages. In addition, at reduced collector-doping concentrations (relative to that of the base) an increased fraction of the depletion layer extends into the collector, thereby reducing the magnitude of depletion layer widening in the critical base layer.

The collector donor concentration for all our vapor-grown GaAs transistors is determined by the background contamination of the vapor-phase system; no intentional dopants are added. For all the GaAs transistors discussed up to now, including those in Figure 9, a vapor-growth system had been used which typically provided n-type "undoped" donor concentrations of about 1 x 10^{16} electrons/cm^3. In order to decrease the collector doping of a GaAs transistor, a vapor-growth system was used which had been especially designed for high-purity crystal growth. In this system, typical donor concentrations of "undoped" layers are in the range of 5 x 10^{14} cm^{-3}.

The I-V characteristics for the base-emitter junction of a GaAs transistor prepared in the high-purity vapor-growth system are presented in the upper photograph of Figure 11. Note here the small reverse current to voltages as large as 70 to 80 V.

N-p-n GaAs transistor structures prepared in the higher purity vapor-growth system have also demonstrated improved characteristics, as illustrated in the lower photograph of Figure 11. Here, the I-V characteristics are nearly ideally horizontal over the extended voltage range of about 50 V, as expected for the lower collector doping.

The transistor characteristics shown in Figure 11 represent a significant improvement in flatness and voltage range over all previously-prepared vapor-grown transistors. Current gains as high as 30 have been obtained for such transistors, as illustrated in Figure 12.

D. PHOTOLITHOGRAPHIC TRANSISTOR FABRICATION

All of the work described in the previous sections involves a relatively simple stripe geometry (ref. 1, Figures 3 and 4) contacted by visual alignment of evaporation masks onto relatively large area (10 by 20 mils) base and emitter patterns. However, for maximum usefulness of GaAs transistors, their fabrication should be consistent, as much as possible, with standard (silicon) technologies and configurations. In fact, specific transistor geometries will almost certainly be required for particular applications, e.g., high-frequency, switching, power applications, etc. For such geometries, a photolithographic masking technology is essential.

A second advantage of a photolithographic masking technique is that it allows a series of etchings to be consecutively executed without realignment. By etching a wafer in several steps and monitoring the depth after each step, one can compensate for the small variations which occur in chemical- or sputter-etch rates from run to run. In addition, transistors with appreciably smaller dimensions than those

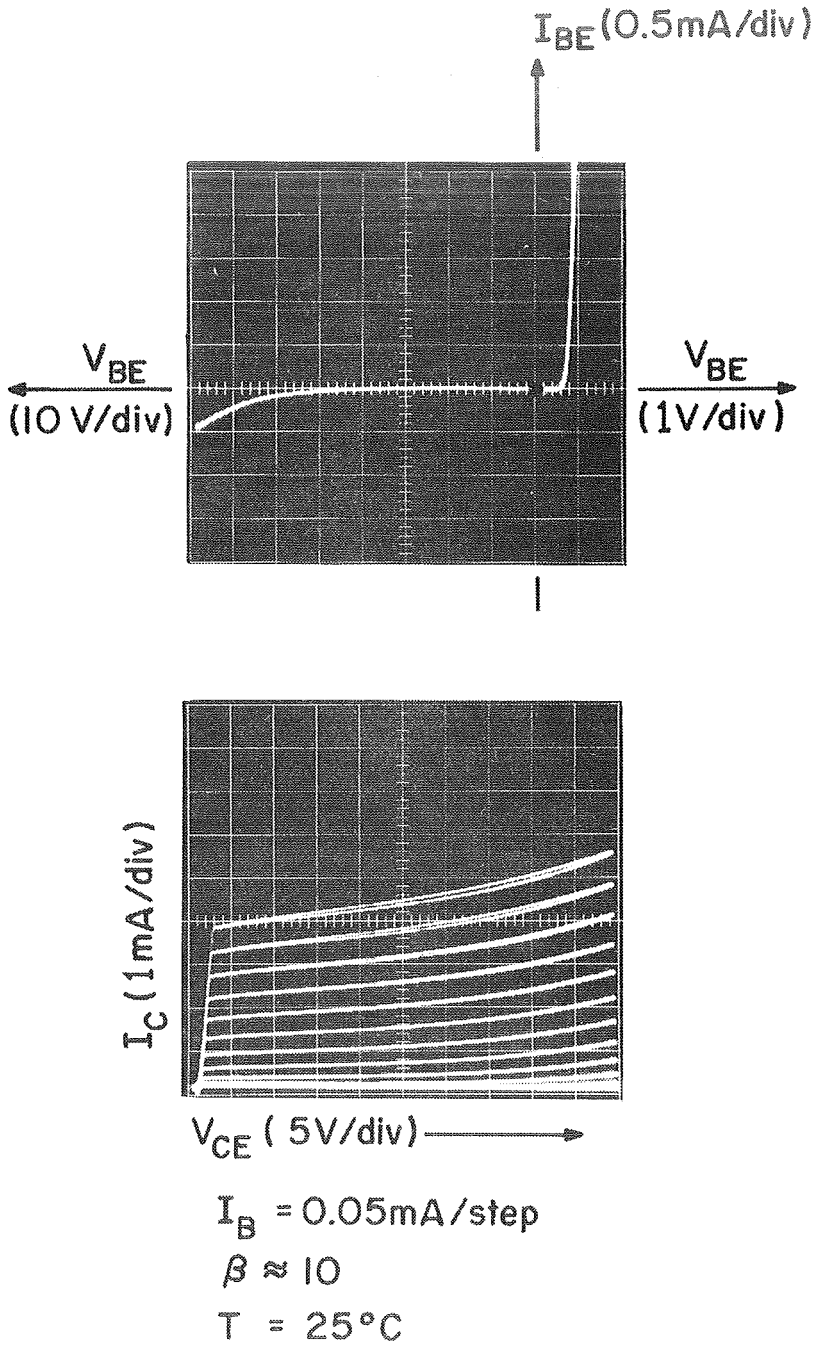


Figure 11. Improved base-emitter junction characteristics and transistor characteristics for chemically-etched GaAs structures vapor-grown with lower collector doping.

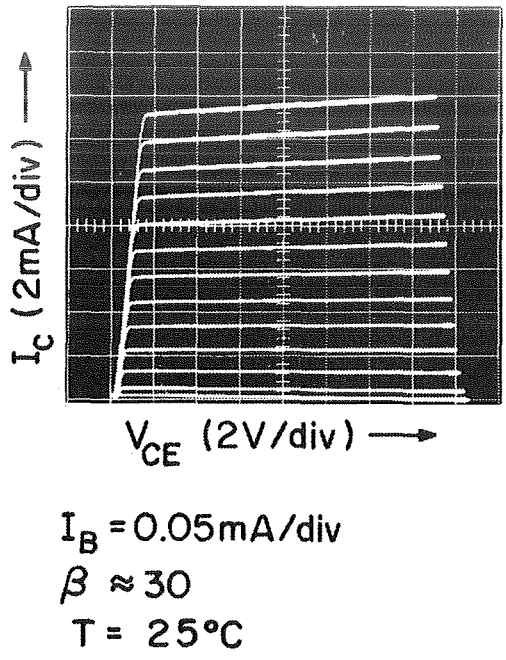


Figure 12. I-V characteristics at 25°C for chemically-etched GaAs transistor vapor-grown with lower collector doping.

previously fabricated can be readily obtained by a photoresist technique. Since the probability, P, of including no randomly distributed defects in an emitter of area A is given by (ref. 12)

$$P = \exp(-nA), \tag{3}$$

where n is the surface defect density, the *yield* increases *exponentially* as the area is decreased.

For all of the reasons given above, efforts during this contract investigation have also been extended to the development of a photolithographic technology involving SiO_2 deposition, photolithographic masking, and either sputter- or chemical-etching, as described in the subsequent two subsections.

1. Sputter-Etching Technology

The sputter-etch technique described in our previous Final Report (ref. 1) required the use of a 2 mil-thick molybdenum mask. Although

this masking procedure was adequate for preliminary evaluation of vapor-grown transistor structures, it suffered from several disadvantages. First, the masking procedure is somewhat crude, since opaque molybdenum handicaps optical alignment. Secondly, the resolution of the array etched through a 2-mil thick mask is about 1 mil, which therefore prevents the use of emitter or base patterns with dimensions less than about 10 mils. Finally, since the mask must be a single, continuous piece, typical concentric transistor patterns cannot be conveniently used. To circumvent these problems, we have initiated the use of an RCA photoresist as a mask against sputtering. The RCA photoresist was selected because it had previously been found to be particularly resistant to sputter etching.

Our photolithographic procedure begins with the deposition of a thin (5000 Å) layer of SiO_2 followed by a thick (3 to 4 μm) layer of RCA photoresist. A transistor pattern is then chemically etched through the photoresist and the SiO_2 by standard photolithographic techniques. The wafer is exposed to sputter etching, and is protected in selected areas by the combination of SiO_2 and photoresist. The SiO_2 alone is not adequate for this purpose, since it is etched itself. The photoresist alone is also not adequate since the mechanical action of the sputtering process is transmitted through it and will disturb a GaAs surface which is not also covered by the harder SiO_2.

Figure 13(a) illustrates an array of GaAs emitter structures which has been sputter etched to dimensions of 1 mil square and 4 mils square. Transistors prepared with these smaller emitter dimensions should have a reasonably good frequency response as well as a wide temperature range. In addition, the emitter crowding which has been observed in some transistors, and which has been reported previously (ref. 1), should be smaller with the photoresist technology, since the peripheral area of each emitter will form a larger fraction of the total area. Figure 13(b) illustrates a practice transistor-type pattern obtained from the sputter-etched mesa pattern of Figure 13(a).

Although the photolithographic technology for sputter etching appears to be satisfactory, it has not been used for actual transistor fabrication during this contract investigation because of the improvements brought about by the use of chemical etching for GaAs transistor fabrication. A similar photolithographic technology, which is appropriate for chemical etching, and which has been used for GaAs transistor fabrication is presented below.

2. Chemical-Etching Technology

Because of the success achieved by the use of chemical etching for exposing selected portions of the base region, a photoresist technique

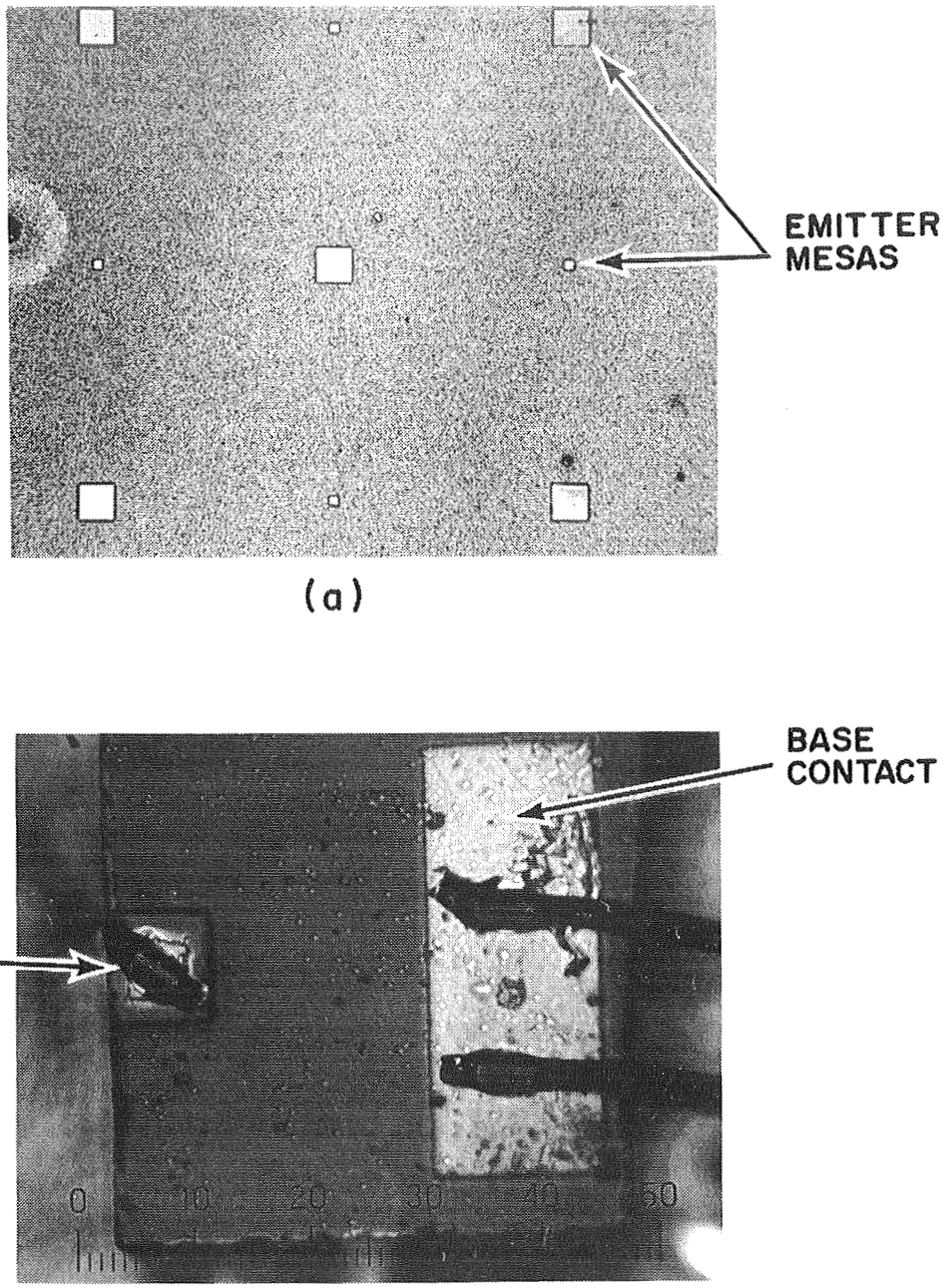
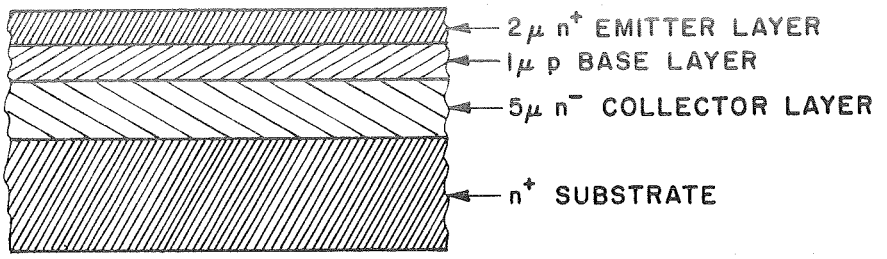
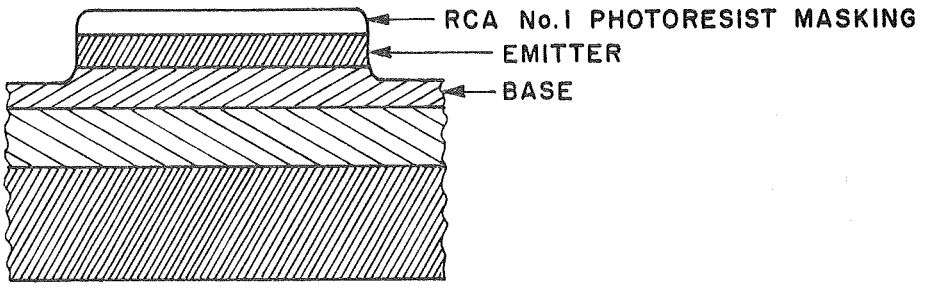


Figure 13. Base and emitter arrays formed by photolithographic masking and sputter etching.

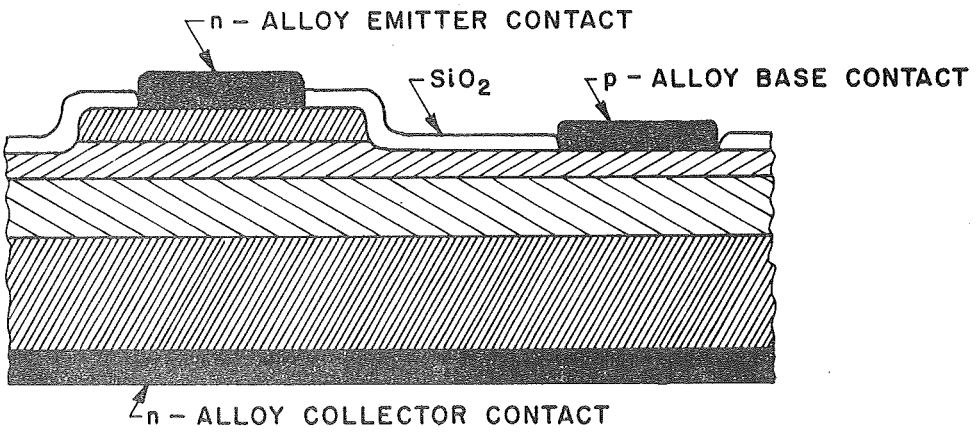
has been developed which incorporates our NaOH:H_2O_2 chemical etch. This procedure is shown schematically in Figure 14, and is described below.



(a) ORIGINAL STRUCTURE



(b) EMITTER MESA FORMATION



(c) CONTACTING

Figure 14. Fabrication procedure for photolithographic masking and chemical etching of GaAs transistors.

A typical collector, base, and emitter three-layered structure is epitaxially vapor-deposited onto an n^+ GaAs substrate, as shown in Figure 14(a). The emitter areas are then masked with RCA No. 1 photoresist, which has also been used here because of its exceptional ability to withstand the hydrogen peroxide in the $NaOH:H_2O_2$ etch. This etchant is employed to etch through the emitter layer, forming isolated emitter mesas and exposing the base layer, as shown in Figure 14(b).

After removal of the photoresist, SiO_2 is deposited over the wafer surface, and successive photoresist patterns are laid down to define the areas for the emitter and base contacts. The appropriate alloys (Au-Ge for the emitter and Au-Zn for the base) are then evaporated and sintered to form the contacts to the emitter and base, followed by the evaporation of Sn to the collector. To provide sufficient strength for bonding, electroless Ni and Au are plated to all contacts, after which the wafer is cleaved into individual transistors [Figure 14(c)].

A typical base-emitter pattern obtained by this photolithographic technique is shown in Figure 15. Here, the stripe down the center is

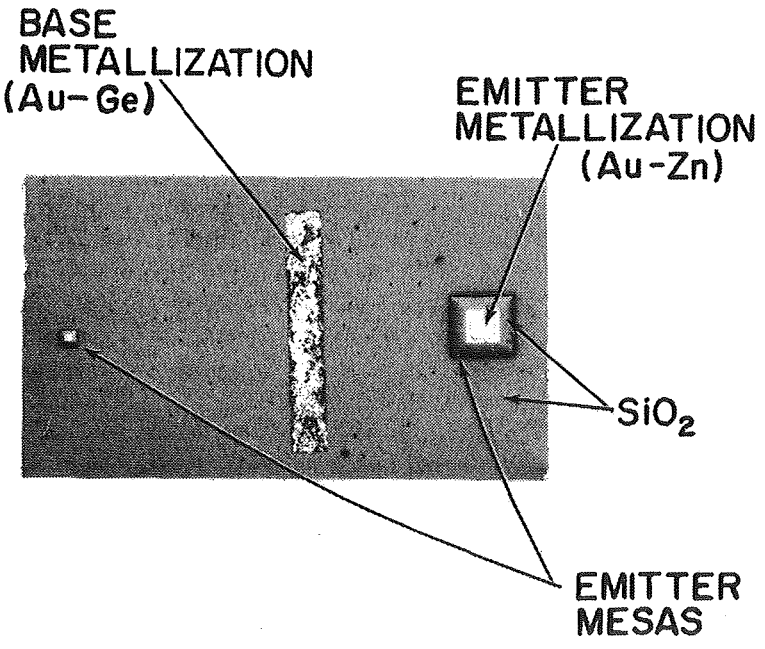


Figure 15. Base-emitter photolithographic pattern formed by chemical etching.

a base contact, whereas the larger square on the right is a 0.004 x 0.004 in emitter mesa with a 0.002 x 0.002 in contact in the center. The smaller square on the left is a 0.001 x 0.001 in emitter mesa with a 0.0005 x 0.0005 in contact in the center. Except for the metalized areas, the entire surface is covered with SiO_2, which in particular protects the edges of the emitter-base junctions. From an examination of the small emitter of Figure 15 at higher magnification, the resolution of this photolithographic technique is estimated to be on the order of 3 μm.

The room-temperature transistor characteristics for the 0.004 x 0.004 in emitter unit shown in Figure 15 are presented in Figure 16.

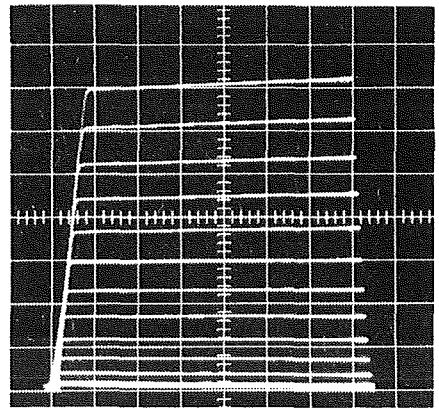


Figure 16. I-V characteristics at 25°C for GaAs transistors prepared photolithographically with chemical etching.

The characteristics in Figure 16 are shown to be well-behaved and exhibit a current gain of about 5. This transistor, and others prepared from the same wafer, retained their current gain and proper I-V characteristics over the entire temperature range between 25° and 300°C. Particularly significant is the fact that cycling between 300° and 25°C did not noticeably alter the characteristics or gain of these transistors, presumably due to the protection of the base-emitter junction by the SiO_2. Future efforts with such transistors should examine the nature and extent of this protection.

E. TWO-STEP VAPOR-GROWTH THROUGH SiO_2 MASKS

In our previous report (ref. 1), we described the formation of two-step vapor-grown junctions, which were consistently found to result in diodes with large reverse currents, particularly at 300°C. Despite this problem, the regrown transistor structure shown in Figure 17 has

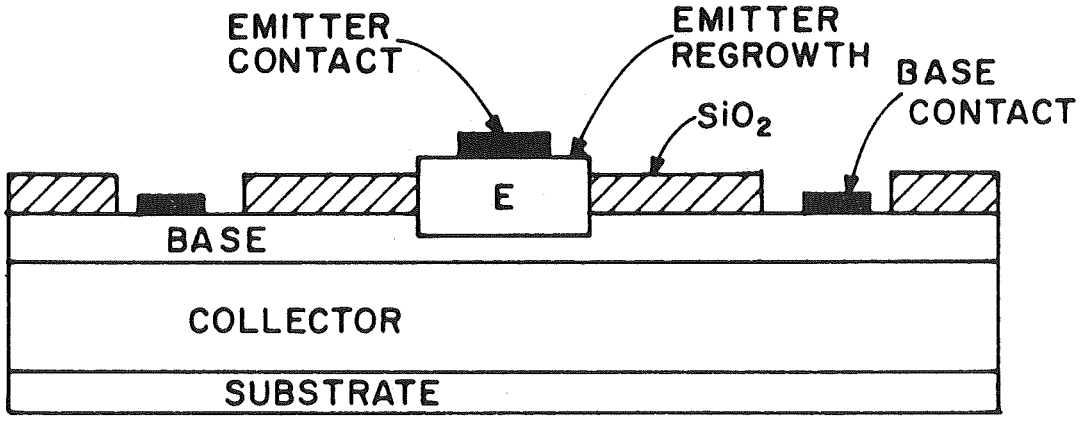


Figure 17. Transistor structure possible with high-quality emitter-base junctions vapor-deposited through SiO_2 masks.

two strong advantages which merit further attention. First, the structure simplifies contacting the base. Second, by combining the regrowth with a short but controlled chemical etch, the effective base width may possibly be reduced. Such a reduction need not affect the series resistance of the base, since the thickness away from the emitter junction could be somewhat larger, as shown in Figure 17.

To investigate the possibility that the previous leakage currents result from SiO_2 masking rather than from the two-step regrowth itself,

we have examined two vapor-grown n^+-p junctions prepared in a two-step regrowth sequence *without SiO_2 masking*. The reverse current densities obtained in these junctions at room-temperature and at 300°C are presented in Table II along with previous results for n^+-p junctions regrown through an SiO_2 mask. The important result of this experiment is that the regrown junctions prepared *without* SiO_2 masking are significantly better than the junctions prepared through an SiO_2 mask, and in fact, are comparable to junctions prepared in a single continuous growth.

Since regrown junctions can thus be prepared with good reverse leakage characteristics, it then becomes important to determine the source of the leakage for regrowths through SiO_2. For this purpose, SiO_2 was deposited on one half of a GaAs wafer and an array of two differently sized holes, 10 and 50 mils in diameter, was etched through the SiO_2. No SiO_2 was deposited on the other half of the wafer. The two halves were placed side-by-side in the growth chamber and an n^+ GaAs layer was epitaxially deposited onto the p-type GaAs. The reverse-bias voltage at a current density of about 10^{-2} A/cm^2 is presented in Table III for the variety of diodes examined in this experiment.

It becomes immediately apparent that the p-n junctions are significantly more leaky (have smaller voltages at a given current density) for the small-area junctions grown through the SiO_2 than for the large-area junctions similarly grown, and that both such junctions are more leaky than those grown over the large-area wafer of GaAs *without SiO_2 masking*. In addition, Table III shows that diodes which were cleaved from the innermost portion of the regrown areas (i.e., the periphery of the diodes were cleaved away) are of comparable quality to those regrown without SiO_2 masking. These results strongly indicate that the leakage is almost entirely confined to the periphery of the regrown areas, which necessarily accounts for a larger fraction of the total area for the 10-mil diameter diodes than for the 50-mil diameter diodes.

Interestingly, the n^+-p diodes are not easily cleaned up by simple chemical treatments, suggesting that the low-quality material extends inward from the crystal surface along the junction plane. This material is definitely confined to the general periphery of the regrown area, since the leakage is removed upon cleaving away the edges of the regrowth. It remains undetermined whether the leakage is due to the specific use of *SiO_2* as a mask, or to the use of *any* foreign material interfacing with the epitaxial GaAs surface. This question will necessarily have to be solved before such a two-step vapor-deposition technique will become practical for n-p-n transistor fabrication.

Interestingly, for the fabrication of p-n-p transistors of GaAs or $GaAs_{1-x}P_x$, a two-step regrowth may be presently feasible. Similar to the technique described above, an n-type (undoped) GaAs vapor-grown

TABLE II

Reverse Current Densities in GaAs
Vapor-Grown n^+-p Junctions

Material No.	Growth Time (Min)	J(A/cm^2) at 300°C	J(A/cm^2) at 25°C
Regrowth Through SiO_2 Masks			
1-26-70:3	6	9	1.4×10^{-2}
1-9-70:1	8	2.3	1.4×10^{-3}
6-9-69:2	5	2	1.1×10^{-1}
6-11-69:2	10	1.3	6.5×10^{-2}
Regrowth Without SiO_2			
1-26-70:2A	6	2.7×10^{-2}	3.1×10^{-4}
1-26-70:2B	6	9.2×10^{-2}	1.1×10^{-3}
Continuously Grown Junctions			
10-9-69:2		2.1×10^{-2}	2.9×10^{-5}
10-9-69:3		5.6×10^{-2}	6.3×10^{-3}
11-10-69		4.9×10^{-2}	4.4×10^{-4}

TABLE III

Leakage in Two-Step Vapor-Grown n^+-p Junctions at Room-Temperature

Diode Configuration	Avg. Voltage at $J \approx 10^{-2}$ A/cm^2
No. SiO_2 masking	13.2
Growth through .010 in dia. holes in SiO_2	1.4
Growth through .050 in dia. holes in SiO_2	4.2
Center of .010 in dia. diodes	9.1
Center of .050 in dia. diodes	10^+

layer was deposited on an n^+ GaAs substrate, after which the wafer was removed from the growth chamber, deposited with SiO_2, and photolithographically etched to form an array of 10-mil diameter holes in the SiO_2. A p-type layer of GaAs was then deposited in the holes by a second vapor-phase growth. The I-V characteristics of the p^+-n junction formed in this sequence are illustrated in Figure 18. Here, the absence of leakage and the sharp reverse-bias breakdown are comparable to that for p^+-n junctions formed in a conventional single growth. The reason for the high-quality junction in Figure 18 is thought to be due to a slight displacement of the p-n junction into the n-type layer by the diffusion of Zn during the 5-to 10-minute growth at 750°C used here. Such a diffusion process would be enhanced by the high concentration of Zn in the p^+ layer and the strong dependence of the diffusion coefficient on concentration for Zn in GaAs (ref. 13). Although p-n-p transistors of GaAs are not particularly useful due to the low gains expected for the small ratio of μ_p/μ_n, the somewhat higher ratio of μ_p/μ_n in $GaAs_{1-x}P_x$ and the trend toward longer diffusion lengths in P-rich alloys of $GaAs_{1-x}P_x$ may allow this technique to find future use here.

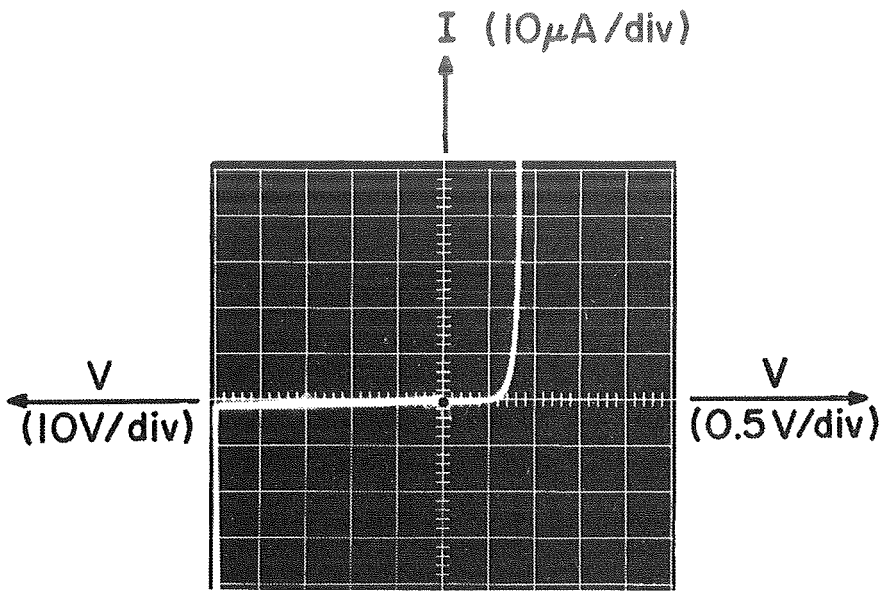


Figure 18. I-V characteristics of GaAs p^+-n^- junction vapor-grown through an SiO_2 mask.

III. CONCLUSIONS AND RECOMMENDATIONS

A study of several parameters which limit the current gain of GaAs bipolar transistors has led to the development of an n-p-n transistor with emitter, base, and collector impurity concentrations of 2×10^{18}, 1×10^{17}, and 5×10^{14} cm^{-3}, respectively, and with a base width of 1 μm. Using such a structure and proper fabrication techniques, current gains in the range of 10 to 30 can be reproducibly obtained at room-temperature for GaAs transistors with nearly ideally flat I-V characteristics to voltages greater than 50 V. In addition, with an HCl surface treatment, transistor gains can be increased to values as high as 90, although these exceptionally high gains degrade to their as-fabricated values in about an hour due to the reversion of the GaAs surface to its as-fabricated condition.

A photolithographic fabrication technology with a resolution of about 3 μm has been developed for use with chemically- or sputter-etched vapor-grown GaAs transistors. Chemically-etched transistors with relatively temperature-independent current gains of about 5 have been prepared in this fashion.

The excessive leakage which prevails for n^+-p junctions prepared in a two-step vapor-growth sequence through an SiO_2 mask has been found to arise primarily at the SiO_2-epitaxy interface. This leakage is drastically reduced in the interior of the vapor-growth pattern and in junctions prepared in two-steps without SiO_2 masking. P^+-n junctions, similarly prepared, are well-behaved with low-leakage currents, presumably due to a slight displacement of the junction away from the SiO_2 interface by the rapid diffusion of Zn during growth.

In order to provide current gains higher than 30 which are stable with time and temperature, future efforts will be required in the area of surface and passivation studies. With such efforts, it may be possible to permanently maintain the GaAs transistor gains of 90 that can now be attained only for relatively short periods of time. Alternately, further research in examining transistor structures or geometries with base widths significantly less than 1 μm could possibly provide as-fabricated current gains sufficiently high to eliminate the need for post-fabrication surface treatments.

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V. NEW TECHNOLOGY APPENDIX

A Chemical-Etch Technique for Exposing Selected Regions of the Base Layer of a GaAs Transistor for Subsequent Contacting

Research under the present contract investigation has resulted in one item of new technology: A Chemical-Etch Technique for Exposing Selected Regions of the Base Layer for Subsequent Contacting. This technology and its results for GaAs n-p-n transistors are described on pages 9 through 26 of this report, and are summarized below.

GaAs vapor-grown n-p-n transistors had previously been fabricated by a sputter-etch technique (ref. 1), resulting in bipolar transistors with current gains as large as 15 at room-temperature and 8 at 300°C.

During the present contract investigation, a room-temperature chemical etch consisting of 1 M sodium hydroxide-0.7 M hydrogen peroxide has been used to etch through selected portions of the emitter and into the thin base layer, thereby exposing regions of the base for subsequent contacting. In this way, current gains of GaAs n-p-n transistors have been increased to values as high as 90 at room-temperature and 15 at 300°C. A similar improvement in the transistor yield has also resulted from the chemical etching.

The features of this etch which are particularly important for the present transistor application are its flatness when etching through a mask, and its reproducible etching rate, which we measure to be about 0.13 μm/min. As compared to that for the sputter-etch technique, surface recombination in the base layer is almost certainly reduced with the $NaOH:H_2O_2$ chemical etch.

VI. ACKNOWLEDGEMENTS

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