A STUDY OF MASS MEMORY APPLICATIONS

by

DAVID A. CURTIS

AUGUST 1970

prepared under

CONTRACT NO. NAS5-21531
(PREVIOUSLY NO. NAS12-2185)

by

ARTHUR D. LITTLE, INC.
CAMBRIDGE, MASSACHUSETTS

GODDARD SPACE FLIGHT CENTER
GREENBELT, MARYLAND

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

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for

Goddard Space Flight Center
National Aeronautics and Space Administration
Greenbelt, Maryland

Mr. F. Kiepert

Technical Monitor

NAS5-21531

(Previously NAS12-2185)

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Greenbelt, Maryland

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CAMBRIDGE,
MASSACHUSETTS

CHICAGO
NEW YORK
SAN FRANCISCO
WASHINGTON
ATHENS
BRUSSELS
CARACAS
LONDON
MEXICO CITY
PARIS
RIO DE JANEIRO
TORONTO
ZURICH

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Cambridge, Massachusetts

SUMMARY

An extensive and detailed review of mass memory storage technologies has been made. Detailed information on the present status of the technologies listed below was obtained from the literature and from technical discussions with leading workers in the various technologies. This information was analyzed to give (1) predictions of the status of mass memory technologies by 1975, and (2) to recommend a technology to replace tape recorders in spaceborne applications.

In 1975, several solid-state technologies will be available for mass memories (about 10^8 bit capacity). They include various optical and electron beam systems, moving magnetic domain systems, and the sonic block organized random access memory (BORAM) system. The major development thrust in the United States today is toward systems suitable for ground-based commercial data processing. There are optical systems under development at the moment which use write-once storage media, such as photographic film, thermoplastic or photoplastic materials, and ablative materials. Because of the difficulties involved with non-mechanical, optical beam deflection schemes, the present optical memory systems use electro-mechanical devices to deflect the light beam or, alternatively, they move the storage medium. This can be done by making the medium in the form of a tape, a disc, a drum, or as a set of storage cards. Systems of this general type will be available within one or two years; some preliminary sales have already been made.

For a spaceborne system, the concept of moving media which can only be used once is unacceptable. Thus, the development of all solid-state systems with reuseable storage media is of interest. Both magneto-optical and photochromic media offer the rewrite capability. The thermoplastic and photoplastic materials can also be rewritten, but only after a special material preparation step. With the current state of the art of materials science, the magneto-optical materials show the most promise. They can be used with either

simple digital writing techniques or as the storage medium for holograms. In each case, the development work is continuing rapidly, but commercial systems are not likely to be available for 2 or 3 years. Optical memories are not recommended because of the size, weight, low efficiency, and poor reliability of the subsystems which comprise an optical memory. The laser, the beam modulator, and the beam deflector with their respective power supplies represent the greatest problems.

There is presently a lot of activity in electron beam memory systems. They offer many of the advantages of optical systems, but they also have disadvantages which make them unattractive in this application. For instance, a suitable reuseable storage medium is not yet available; the lifetime of the system is limited by the lifetime of the cathode, and the system is large and heavy when all the associated electronics and power supplies are included.

There are several different formats in the moving magnetic domain technology. The magnetic material can be either metallic or non-metallic; the material can be a continuous, two-dimensional plane, a series of strips of magnetic material, or a wire (the latter in the metallic case only). These units are basically shift registers. They can be arranged in blocks, each block being one or more shift registers, with random access possible between the blocks. The metallic shift registers are at a more advanced stage of development than the non-metallic units. However, the latter offer certain advantages in size, weight, and power which make them more attractive for spaceborne applications. The present difficulty with the non-metallic magnetic shift registers is obtaining reasonable quantities of good quality material. In this report the magnetic shift registers based on planar metallic storage media are called domain tip propagation logic memories (DTPL), while those based on non-metallic storage media are called "bubble" memories.

The sonic BORAM system is another block-organized sequential memory. The important difference is that the data do not move through the memory. Each block consists of one or more films of magnetostrictive material placed on substrates. A sound pulse passed down the substrate modifies the magnetic properties of the film in the immediate vicinity of the sound wave, and it is thus possible to enter information in the locally disturbed region by passing a pulse of current along a wire adjacent to the magnetic film. The readout occurs by disturbing the magnetic properties of the thin film with a second sonic pulse and monitoring the flux change by recording the voltages induced on the wire. This system has a very low noise level associated with the signal because current drive pulses are not required to perform the readout. Development work on this technology has reached a stage where small capacity memories have been built and operated. There are several areas where improvements can be made, notably an increase in the number of bits per unit length of the substrate, and an increase in the length of the substrate which can be used without distorting the acoustical pulse beyond useable limits. A commercial unit will use a glass substrate, but better performance can be obtained by using a quartz substrate.

An analysis of these systems shows that the magnetic shift registers are most suitable for replacing tape recorders in space applications. They are the smallest, lightest systems with a reasonable power consumption, non-destructive readout (NDRO) is possible, and they are non-volatile, can work asynchronously, and are capable of withstanding the space environment. The magnetic wire shift registers do not qualify because of their size; it is estimated that a 10^8 bit memory using this technology would occupy 30 cubic feet. DTPL shift registers have a better bit packing density than the wire units. As many as 10^8 bits can be packaged in less than 4 cubic feet. The bubble memory has a much better packing density than the DTPL memories and a 10^8 bit memory should pack into 0.5 cubic foot. The sonic BORAM system has disadvantages associated with the basic block size and the number of drive circuits needed. It is also large; a 10^8 bit memory would occupy about 4 cubic feet. The big advantage of the sonic BORAM and metallic magnetic shift register is that they both can be built using current technology. The bubble memory, on the other hand, is not yet at this stage.

The major difficulty at present is in obtaining sufficient quantities of a suitable storage medium. It appears that a medium capable of supporting magnetic domains 0.3 to 0.6 mil in diameter is suitable. If the domains are too large, the memory size is too large; if the domains are too small, there are severe fabrication difficulties associated with the photolithography. Even for those domains in the correct diameter range there are fabrication difficulties associated with the preparation of the thin storage plane. Also there is a complex interrelationship between the thickness of the storage plane, the diameter of the domain, the temperature, and the bias and drive fields. It is the interplay between these parameters which determines the operational margins of a bubble memory.

The commercial development is directed toward a high bit density, greater than 10^6 bits in.$^{-2}$, fast data rate, greater than 1 MHz, and a rapid access time. NASA's needs are different. They can take the technology and make a memory with an adequate bit density, about 500,000 bits in.$^{-2}$, and a data rate between 0 and 1 MHz, by using timing tracks and a bit-parallel organization. There is no need in a buffer memory to stress rapid access to individual characters in the memory.

It does not appear that there are any problems which cannot be overcome if effort is expended on them, so the bubble technology is recommended as being a potential successor to tape recorders in spaceborne data processing systems after 1975. The DTPL shift registers and the sonic BORAM are recommended as second and third choice technologies. The DTPL memories are smaller than the sonic BORAM and for this reason are regarded as the second choice technology. However, in two or three years the DTPL registers may have a further advantage over the sonic BORAM system because the industry appears to see more chance of commercial success with the shift registers and more development effort will be expended there. The DTPL technology is in an advanced stage of development and will be available commercially within the next year. The first units sold will be small memories with perhaps 8k or 16k bits. Larger memories, up to 10 million bits capacity, will appear after that but the extension of the technology to mass memories will require an improvement in the bit packing density from the present 1000 bits in.$^{-2}$ to 50,000 bits in.$^{-2}$ or better. The limitations on the bit packing density are the high resolution photolithography needed to define narrow data channels, the more severe alignment problems associated with the drive conductor patterns and the higher drive fields needed for the narrower domains. It is unlikely that the drive margins will be increased significantly by further development work. One problem which has not yet been answered is the possibility of aging in the magnetic film. However, the first evidence is that aging is not a major problem.

The technologies reviewed during the course of the contract and discussed in this report are:

Ferrite core	
Plated wire	
Integrated circuits --	bipolar, fixed threshold MOS, variable threshold MOS, charge-coupled devices and amorphous devices
Optical memories --	magneto-optic, photochromic, thermoplastic, photoplastic, photographic, tape punching, and holographic
Electron beam memories --	photographic and storage tubes
Thin film --	coupled films, mated films, and etched permalloy
Planar ferrite memories --	laminated ferrite, post and film, and apertured ferrite
Magnetic domain shift registers	
Travelling domain wall memories	
Sonic BORAM	
Cryogenic systems	
Ferroelectric memories --	optical and semi-conductor
Acoustical delay lines	
Opto-electronic memories	

I. INTRODUCTION

Background

This document is the final technical report under NASA contract NAS 5-21531 (formerly NAS 12-2185). The main aim of the work supported by this contract was to survey those memory technologies believed capable of being developed and configured in such a manner that they can act as a replacement for tape recorders used in space missions. This reports details the evidence, analysis, and conclusions of the extensive review undertaken. Chapter I gives the background to the problem by reviewing the characteristics and functions of tape recorders used in space missions, defining the space environment and listing the technologies reviewed. Chapter II discusses the general characteristics which a replacement technology must demonstrate and reviews the influence of commercial trends on the development of memory technology. It is possible in this way to establish a generalized specification for the replacement equipment. The recommendation that the magnetic domain shift register, based on non-metallic material (the well known example is the Bell Telephone Laboratories "bubble" memory) is the best technology is given in Chapter III. In the same chapter, a detailed comparison of this technology with the closest competitors, metallic magnetic shift registers and sonic BORAM, is given. Chapter IV describes in detail the other technologies reviewed, offering reasons why they were not recommended.

Many of the details given in Chapters I, II, and IV were reported in the quarterly technical reports submitted during this contract. As far as possible this survey has covered memory technologies, and not memory systems as produced or developed by different organizations. In some cases, one organization has dominated the field in a particular technology. In these cases, particularly, recommendation or rejection as a suitable technology has been based as carefully as possible upon the merits or difficulties of the technology rather than on the specific system under development. This has been made easier by the fact that no one has been working to develop a technology specifically for the replacement of spaceborne tape recorders, so the criteria used to judge the technologies have been different from those used by the organizations developing equipment for a commercial market. For this reason, it was absolutely essential to review the technologies rather than the products. It must be clearly understood that those technologies not recommended were rejected solely because they were regarded as unsuitable for use as a replacement for tape recorders used in space missions. No criticism is to be implied as to the use of these technologies in any other situation.

Visits to leading companies and laboratories in the various memory technologies constituted a major activity under the contract. A complete list of organizations visited is included in the report as Appendix B.

On June 16, 1970 contract responsibility for the program was transferred from the NASA Electronics Research Center, Cambridge, Massachusetts, where Mr. Neil G. Patt acted as Technical Monitor, to the Goddard Space Flight Center, Maryland.

Objective

The main aim of the study was the definition of a data storage technology potentially capable of replacing tape recorders in existing and future spaceborne data processing systems. The time frame of interest is for a flight in the mid 1970's. The following sections describe the approach adopted, typical missions which NASA undertakes, the present status of tape recorders, generalized data storage systems, and a semi-quantitative approach to reducing the number of technologies to a few.

Approach

The approach adopted was to collect data through an extensive literature survey, make visits to key personnel in many companies, attend several lectures, conferences and symposia, and review information made available by NASA. Another useful source of information was the pool of knowledge possessed by professional staff members at Arthur D. Little, Inc., and the company's non-confidential data files. These data were analyzed and trade-off studies were conducted to define qualitatively those technologies best suited to performing the desired functions in space missions. Care was taken to consider the impact of the technologies on system and subsystem design and to assess the performance advantages to be gained. The commercial potential for the technology recommended was also evaluated.

The first step in the approach to the project was to review the existing tape recorder technology and the space environment so that a standard for comparison could be established. The technologies were reviewed in terms of these standards and some rejected immediately. As a safeguard, the probable future development of these technologies was checked to ascertain that the decision was reasonable. The remaining technologies were ranked in terms of suitability as a replacement for tape recorders today. It became quickly apparent that none of today's technologies was immediately adaptable. The ordering process required extensive trade-off studies.

The top technologies were singled out for further detailed study. Once again, those technologies which were omitted were reviewed for future prospects. Then the candidates were reviewed again in more detail. The natural limits of each technology were established, predictions were made about the future developments in each technology (bearing in mind the levels of effort and the commercial interest involved, as well as purely technical factors), and the production, whether actual or hypothetical, of memory systems based on each technology was reviewed step by step. As a result some technologies were removed, with others rearranged to reflect the expected rank order of the technologies in the mid 1970's. In this way a firm recommendation was reached -- the moving magnetic-domain shift register based on non-metallic storage media. The obvious extension to metallic media for these shift registers was also found to be acceptable and so was the sonic BORAM technology. However, both these technologies have disadvantages in comparison with the recommended technology.

Missions

NASA's satellite missions are designed to make observations of the Earth, its atmosphere and ionosphere, and interplanetary space. There are three possible ways of handling the data collected; it can either be transmitted immediately to Earth in real-time; it can be stored and brought back to Earth in a re-entry vehicle, or it can be stored and then transmitted to Earth on demand. The last technique has proven optimum for the great majority of missions. The savings at the ground stations are obvious. In the satellite itself some data handling, such as analog-to-digital conversion, error detection, error correction, data compression, and data rate changing, can be accomplished. These procedures allow for more efficient use of satellite power, telemetry links, and ground station time. From the first satellite missions NASA has used tape recorders to perform the data storage function. These recorders have been developed considerably (Ref. 1) and now contain all their essential functions within one unit. Apart from the data inputs and outputs and the control input, the only requirement is that part of the satellite's power supply be reserved for the recorder.

All the systems flown in the satellite must be capable of withstanding prelaunch handling and testing, the launch itself, and a hostile space environment. If they are to land on an extra-terrestrial body, they must also survive sterilization before launch and the landing phase as well. The systems must operate correctly throughout the useful phase of the mission. This may be continuous operation over a long period, or an intermittent operation with a variable use-cycle. In the latter mode, a long system "shelf" life in the satellite is desirable. Typical environmental parameters (Ref. 2) for the payload during the launch and the flight are given in Tables I and II. The main characteristics of the environment are shock, vibration, and acceleration during the launch, and temperature, pressure, particle radiation, and the electromagnetic environment during the whole flight. The peak energy in the payload vibration spectrum usually occurs in

TABLE I

TYPICAL PAYLOAD LAUNCH ENVIRONMENT FOR A SATURN BOOSTER

Vibration Levels:

Sinusoidal

5 to 33 Hz at 0.36 cm DA+ displacement

33 to 140 Hz at 8g peak

140 to 240 Hz at 0.0204 cm DA displacement

240 to 2000 Hz at 24g peak

Random

20 to 200 Hz at 2dB per octave

200 to 700 Hz at $0.64g^2\ Hz^{-1}$

700 to 890 Hz at -18 dB per octave

890 to 2000 Hz at $0.15g^2\ Hz^{-1}$

Overall sound pressure level: 153.5 dB

Temperature in boost flight: $21 \pm 5.5°C$

Acceleration maximum: first cutoff* $6.99\ ms^{-2}$

second cutoff** $15.24\ ms^{-2}$

Altitude maximum: 287 km

\+ Double amplitude

* Launch into Earth orbit

** Injection into Earth-escape path

the 600 to 1000 Hz range and the most sensitive times are immediately on firing and on passing through Mach 1. Maximum values of shock likely are 15g to 20g, depending on the structure. The shocks have a duration of about 10 ms. The sound pressure level is that outside the payload.

The environmental parameters listed in Table II are those phenomena which may affect the operation of systems in the payload. In free space the spacecraft is subjected to the full impact of the primary radiation from solar, interstellar, and intergalactic sources. Electrons, protons, and α-particles predominate. On interacting with the structure of the spacecraft, the primary radiation gives rise to a flux of secondary gamma rays and bremsstrahlung much smaller than that of primary radiation. Micrometeorites, the asteroid belt between Mars and Jupiter, and the rings of Saturn obviously present further hazards to the whole spacecraft, but nothing specific to its electronic systems. Another potential hazard is the radioisotope thermoelectric generator which it is envisaged the deep space probes will carry.

With adequate thermal design the temperature of the various subsystems inside the payload should be in the range of 0 to 50°C. For those missions designed to explore the outer planets it may be more appropriate to allow the probe and its subsystems to operate more closely to their equilibrium temperatures in the immediate environment; this would imply temperatures down to -40°C with present technology. The pressure in the payload is that of the surroundings, about 10^{-13} atmosphere.

There is a distinction between the operational environment and the non-operational environment. It is not necessary for the memory system to operate under the severe stresses of launch, but it must certainly survive these and be capable of operation in the zero gravity space environment. During the course of the work most attention was paid to those environmental parameters which are the most restrictive, whether they are for the operational or non-operational conditions.

Tape Recorders

<u>Modes of Operation</u> -- The most frequent function performed by tape recorders is to act as a buffer between the sensors carried by the satellite and the telemetry system. The rate at which data are acquired may differ greatly from the rate at which they must be transmitted to Earth. For Earth-orbital satellites, the transmission to Earth is usually done on demand by a ground station and only 2 or 3 minutes are required to dump all the information gathered by the sensors in one orbit of about 90 minutes. The time taken to dump the information is determined by the desire to have the sensors operating usefully for as much of each orbit as possible, and by the time window available for communication between the ground station and the satellite passing overhead. In this case

TABLE II

TYPICAL PAYLOAD MISSION ENVIRONMENT

<u>Primary Radiation Belts</u>

<u>Inner Zone</u> ($\sim$1000 to $\sim$8000 km)

Composition: mainly electrons and protons ($\lesssim 10^{10}$ particles cm^{-2} s^{-1} $ster^{-1}$, $\lesssim$ 40 MeV)

Slight variations with solar activity.

<u>Outer Zone</u> ($\sim$13000 to $\sim$80000 km)

Composition: mainly electrons and protons ($\lesssim 5 \times 10^8$ particles cm^{-2} s^{-1} $ster^{-1}$, $\lesssim$ 5 MeV)

Extreme variation with solar activity.

<u>Solar High Energy Particle Radiation</u>

Composition: protons with 1-2% alpha particles

Once every few years ($\sim$4.5 years) an extremely high energy ($\sim$15 GeV) flux occurs.

<u>Galactic Cosmic Radiation</u>

Isotropic distribution of particles with intensity variations during the solar cycle. High energies ($\lesssim$ 20 GeV) and about 2.5 particles cm^{-2} s^{-1}

<u>Solar Wind Particles</u>

Small numbers ($\lesssim 10^4$ cm^{-3}) of low energy ($\lesssim$ 40 keV) electrons and protons.

<u>Solar X-Radiation</u>

$\lesssim$ 1 μW cm^{-2} of soft X-rays during periods of solar activity.

the tape deck acts as a buffer between the sensors accumulating information at a low rate over a long period and a wide bandwidth down-link to Earth which transmits the information in a short time. This time compression is accomplished by writing on the tape at a slow speed and reading from the tape at a high speed.

For interplanetary missions the tape recorders also perform a buffer function, collecting information at a high rate, most likely during the short planetary encounter stage, and transmitting it to Earth at a low rate. This has to happen because of signal to noise problems over the long interplanetary communications link.

The on-board data acquisition system must accept data simultaneously from a variety of instruments. A payload group may possess the following characteristics:

1. A wide range of data rates,
2. A binary data rate which is necessarily asynchronous with a spacecraft clock,
3. Intermittent data (in bursts with lengthy quiescent intervals),
4. Data identification requirements,
5. Production of data at a rate which exceeds the telecommunications channel capacity for various intervals of time.

Typical instruments involve the use of devices such as particle counters characterized by: a) a very large dynamic range (1 count per hour to 100,000 counts per second), b) asynchronous operation both in time and in data output characteristics, and c) a relatively low instantaneous digital output rate (the maximum rate is about 20 $bits^{-1}$). Such a science data system may have interfaces with a telecommunication system which has the following characteristics:

1. Provides a single binary channel,
2. Transmits at a synchronous rate under the control of a stable clock (oscillator),
3. Requires rate changes as a function of distance, trajectory, power availability, or other factors,
4. Requires time-sharing of channel capacity with spacecraft performance information, and for two-way doppler and ranging information.

The main emphasis of this report is on the buffering mode of operation of tape recorders, but they do have other uses. They have been used for storage of computer programs, and highly specialized systems have been used to monitor the launch phase of a mission. The tape recorders used as buffer stores are not operated during these phases, but they must be constructed to survive these phases.

<u>Present Status of Tape Recorders</u> -- This discussion is restricted to tape recorders used as data storage buffers. Table III lists the physical and operational parameters of several models of tape recorders which have been used in space missions. The figures for weight, volume and power refer to the total system which includes tape, motors, motor control, reels, write and read heads, information buffers, and parity checking electronics. The power supply is not included.

Tape recorders have some special features which can be utilized to advantage. For example, they can record information in both analog and digital form so, in some cases, there is no need to have analog-to-digital converters for each transducer. The transducers can be partly identified by the track on the tape which they use; this reduces the multiplexing needs. The information is recorded on the tape bit serially and is also read out bit serially from each track. There is no possibility of random access to all the words stored, but if the necessary block identifiers are supplied, then rapid access to any specified block can be made and the data then read serially from the block. Replay of data is possible.

The parameters shown in Table IV are typical of tape recorders designed to satisfy, as far as possible, the following essential requirements: 1) long, unattended life; 2) low weight; 3) small size; 4) low power consumption; 5) multi-speed operation; 6) ability to withstand environmental extremes; and 7) extreme reliability of operation. These characteristics are, of course, of varying importance, depending on the type and the life of the mission.

High information density recorded on the tape reduces size, weight, and power consumption, and would normally be chosen. However, the requirement for long, unattended life rules out high packing densities because such considerations as head fouling, separation due to dust and dirt, changes in the head characteristics due to temperature fluctuations and head wear, etc., all contribute to the upper limit of packing density. Low tape tensions, which are common to in-flight recorders, help minimize the problem of head wear. These low tape tensions, however, aggravate the problem of maintaining intimate contact between tape and head and further limit the resolution which can be considered in an in-flight recorder. Thus, packing densities of 2000 to 3000 flux changes per inch are typical. Tape life of over 10,000 passes (the equivalent of 5000 Earth orbits) has been achieved. To perform the time-compression or time-expansion functions, the recorders require multispeed operation. This can be achieved in a number of ways, but only a few are acceptable for spacecraft operation. The most reliable approach consists of changing the frequency and voltage of the power source

TABLE III

PERFORMANCE CHARACTERISTICS OF SPACE TAPE RECORDERS

Type	Mission	Weight (lb)	Volume (in.^{3})	Speed (in. s^{-1}) Record	Speed (in. s^{-1}) Reproduce	Power (W) Record	Power (W) Reprod.	Tape Length (ft)	Track Bit Density (bits in.$^{-1}$)	Life (h)	Data Type
Borg-Warner Controls R-103	Surveyor	7.5	370	60	60	12 Transp. only	12	37.5 21 tracks	---	---	FM
Kinelogic LS-1	---	12	567	2.4	19.2	16	22	1093 5 tracks	400	10^4	Digital
Kinelogic LS-2	---	12	567	3.6	19.2	16	22	1093 5 tracks	400	10^4	Digital
Leach series 2000	---	15	290	0.5	100	5	25	3000 2 tracks	2000	1.4×10^4	Digital, Analog FM
Precision Instrument PS-303-T	Discoverer	8	347	2	16	8	10	740 2 tracks	---	---	FM
RCA Astro-Electronics	Nimbus D	30.8	---	1.33	43	8	14.9	950 5 tracks	3000	10^4	Digital
Raymond Engineering Laboratory	Mariner IV	16.8	481	12.84	0.01	4	4	330 2 tracks	833	$> 5 \times 10^3$	Digital

TABLE IV

ENVIRONMENTAL SPECIFICATIONS ON VARIOUS SPACE TAPE RECORDERS

Type	Mission	Vibrations Random	Sinusoidal	Accel.	Shock	Temperature Range(°C)	Pressure	Flutter (P-P)
Borg-Warner Controls R-103	Surveyor		3-20 Hz, p-p 0.45 in. 20-100 Hz, 9g 100-1500 Hz, 2g	100g 25g transverse	25g	-20 to 70		0.1° RMS DC - 5 kHz
Kinelogic[1] LS-1 and LS-2	-	15-2000 Hz[2] White gaussian noise 14g RMS, 30 s	1-4.4 Hz 1.5 in. DA[4] 4.4-15 Hz 2.1g RMS 3 minutes, all axes	-	200g, 0.5-1.5 ms any axis	-35 to 70	2 years operation in hard vacuum	-
Leach[3] Series 2000	-	20-400 Hz $0.07g^2$ Hz^{-1} 400-2000 Hz $0.13g^2$ Hz^{-1}	14-40 Hz 3g 40-400 Hz 7.5g, 400-3000 Hz, 15g	11.6g	40g, 6 ms	-20 to 55 (Operational) -35 to 75 (survival)	1 year operation in hard vacuum	-
Precision Instruments PS-303-T	-	White gaussian $0.05g^2 Hz^{-1}$, all axes	5-12 Hz 1 in. DA 12-250 Hz, 4g, 250-400 Hz, 9g, 400-2000 Hz, 15g	-	30g, 6 ms	-35 to 75	-	∿ 3%
RCA Astro-electronics	Numbus D	20-2000 Hz $0.2g^2$ Hz^{-1} 20g RMS	5-2000 Hz 20g	20g	-	-5 to 40	-	1%
Raymond Engineering Laboratory	Mariner IV	20g RMS			200g	-10 to 70		

(1) Survives 100% relative humidity.

(2) Also, 10 minutes of 5g RMS (15 to 2000 Hz) white gaussian and 2g (15 to 40 Hz) and 9g (40 Hz to 2000 Hz) sinusoid together.

(3) Survives 10^{13} neutrons cm^{-2} and 10^{8} C rads

(4) Double amplitude

for the synchronous motor, using logic circuitry. This system has limitations at the high and low speed ends of the range. At low speeds a "cogging effect" is exhibited by the motor, and at high speeds there is a bearing-speed limitation. Windage losses also become severe as motor speeds increase. When compression or expansion ratios exceed 18:1, it becomes necessary to provide two motors, one for high speed and one for low speed operation. Each motor can be matched to the load and operated at its peak efficiency.

Endless-loop machines have been used extensively in Earth-orbiting spacecraft, where all tape motion is in one direction, and two motors can be conveniently coupled to the capstans through self-energizing, overrunning clutches. The control system is simple, consisting merely of energizing one motor (and its associated signal electronics), or the other motor and its signal electronics. In reel-to-reel recorders, devices such as electrically operated clutches, planetary devices, and other, more exotic switching means are necessary for high ratios. The Mariner IV endless-loop recorder has a record/playback speed range of 1284/1. This was achieved with two motors and a pair of overrunning clutches.

The housing for the transport must protect it from dirt, dust, moisture, and the vacuum environment in outer space. A seal is required which will maintain a reasonable pressure for a period of one year or more while being subjected to the thermal changes which all spacecraft experience, and, while being exposed to the hard vacuum of space -- a pressure of 10^{-12} atmosphere or less. Table IV lists the environmental specifications of various tape recorders.

Disadvantages of Tape Recorders

The main disadvantage of tape recorders is that they are electromechanical devices built to very tight specifications. The bearing wear induced by shocks and vibrations is considerable and this causes errors in record and playback. The wear becomes inordinate if resonance occurs. Low vapor pressure lubricants are necessary and, if the system is to be sterilized, they must be applied in large quantities. Timing errors can be eliminated by utilizing one channel on the tape for timing markers or by using an asynchronous output buffer. The effects of dropouts are reduced by the parity checking electronics with error rates of 10^{-5} attainable. Tape and head wear is embarrassing since the readout depends critically on the head gap with wear of a few millionths of an inch reducing the signal considerably. The transfer of tape coating to the head and head material to the tape aggravates the problems of wear and dropouts. Other problems associated with the use of tape are:

1. Excessive shrinkage of the tape at the required test temperature causing the reels to become tight and to jam,

2. Variations in magnetic properties between tape samples causing problems in electronic circuit design for the record and playback amplifiers,

3. Variations in oxide wear between samples causing an unpredictable decay rate of tape performance,

4. Variations in coefficient of friction of the tape surfaces sufficient to cause variations in internal power dissipation,

5. Unsupported tape whips,

6. Tape passing through nips may have variable tensions owing to the mechanical motion of the nips with respect to each other.

Programmed tape recorders which need widely differing tape speeds and perform start-stop functions add to the difficulties of operation. Just as with Earth-bound instrumentation recorders, the tape on a reel that has been standing idle for some time may compact and require a large jolt to start unreeling. Exposure to a large magnetic field or a high temperature will destroy the information on the tape, but these situations are unusual in spacecraft.

The reliability of the system increases as the number of components decreases. This fact has led to the development of tape recorders with only three moving parts, a motor and two reels. However, more flexible performance can be obtained by using more than one motor and several guide rollers. A motor life of 25,000 hours is attainable, but part of this life, of course, is expended in ground testing. Mission experience has shown that the mechanical problems limit the lifetimes. Although lifetimes of 10,000 to 20,000 hours are attainable, shorter lifetimes are of sufficient frequency to raise questions concerning the use of tape recorders. Certainly, their use in deep space probes with a required life of 50,000 to 100,000 hours would seriously compromise the successful outcome of the mission.

Developments -- Considerable effort is still being expended to further the development of tape recorders. Just recently, recording heads with positive aerodynamic control of the head on the recording medium were developed. Although originally suggested for discs, they could be adopted for tapes. Liquid seals for bearings using ferromagnetic liquids were also announced recently. Head life is being improved by introducing new alloys, and tape wear is being improved through the development of new surface lubricants which remain on the tape rather than being shed onto the head.

Another major feature in the use of tape recorder systems is that there is now considerable experience in debugging tape systems. Motors with adequate torques for worst case situations are now used; this reduces oxide shed. The tape is always preconditioned to remove debris from the slitting and the original sloughing, and the tape is specially chosen from a single batch. By careful system design, the programming of a tape recorder can be eliminated. A unit which runs continuously at one speed is more reliable than a programmed unit, so current designs for data systems for space use have a solid-state buffer memory with the tape. The information is stored on the tape, but the solid-state memory acts as the data rate changer between the sensors and the tape, and the tape and the telemetry.

No detailed investigation of the future developments of tape recorders was performed. Therefore, the all solid-state memory recommended as a replacement for tape recorders was recommended after trade-off studies between the competing technologies as they will rank in 1975 and comparison with today's state of the art in tape recorders.

Competing Technologies

A previous report (Ref. 3) by Arthur D. Little, Inc., emphasized the many advantages to be gained by using solid-state devices, particularly integrated circuit components, in space systems. The main advantages noted were improvements in reliability, power consumption, weight, performance, assembly, and testing of subsystems and also lower demands on boosters or, conversely, a better satellite flight plan from the same booster. With each reduction in weight and size there is a multiplier since less cable, harnesses, and mechanical supports, and also less power are required. A conclusion of the report was that a 25-35% weight and volume reduction could be made in spacecraft, such as Explorer, IMP, Syncom, etc., but at that time the transmitters, receivers, and tape recorders were fixed since considerable redesign was needed to obtain further reductions. This report recommends an all solid-state replacement for tape recorders, so that further improvements in the reliability, weight, volume, performance and power consumption of spacecraft can be made.

A large variety of schemes have been developed to store information. Some have received considerable attention over a long period and are now sophisticated systems, while others are still at a development stage or remain just concepts. Table V lists possible candidate technologies which form the basis of the considerations of this report. In contrast to tape recorders which can be used for digital, analog, or FM storage, most of these technologies are digital only.

Figure 1 is a block diagram of a generalized random access memory system. Those parts of the system which are essential to its successful operation will be discussed briefly. The information comes from the various transducers and must first be digitized. If there are many transducers, the buffer outputs must be multiplexed, under the central controller, before reaching the information buffer. Some transducers which have a high data rate will

TABLE V

MEMORY TECHNOLOGIES

Ferrite core	
Plated wire	
Thin film	- coupled films, multi-layer films, etched permalloy
Planar ferrite memories	- laminated ferrite, post and film, apertured ferrite
Moving magnetic domain shift registers	- metallic, non-metallic (Bell Telephone Laboratories "bubble")
Travelling domain wall memories	
Sonic BORAM	
Integrated circuits	- bipolar, fixed threshold MOS, variable threshold MOS, charge-coupled devices, amorphous devices
Optical memories	- magneto-optic, photochromic, thermoplastic, photoplastic, photographic, tape punching, holographic
Electron beam memories	- photographic, storage tubes
Ferroelectric memories	- optical, semiconductor
Acoustical delay lines	- magnetostrictive, piezoelectric
Opto-electronic memories	
Cryogenic memories	

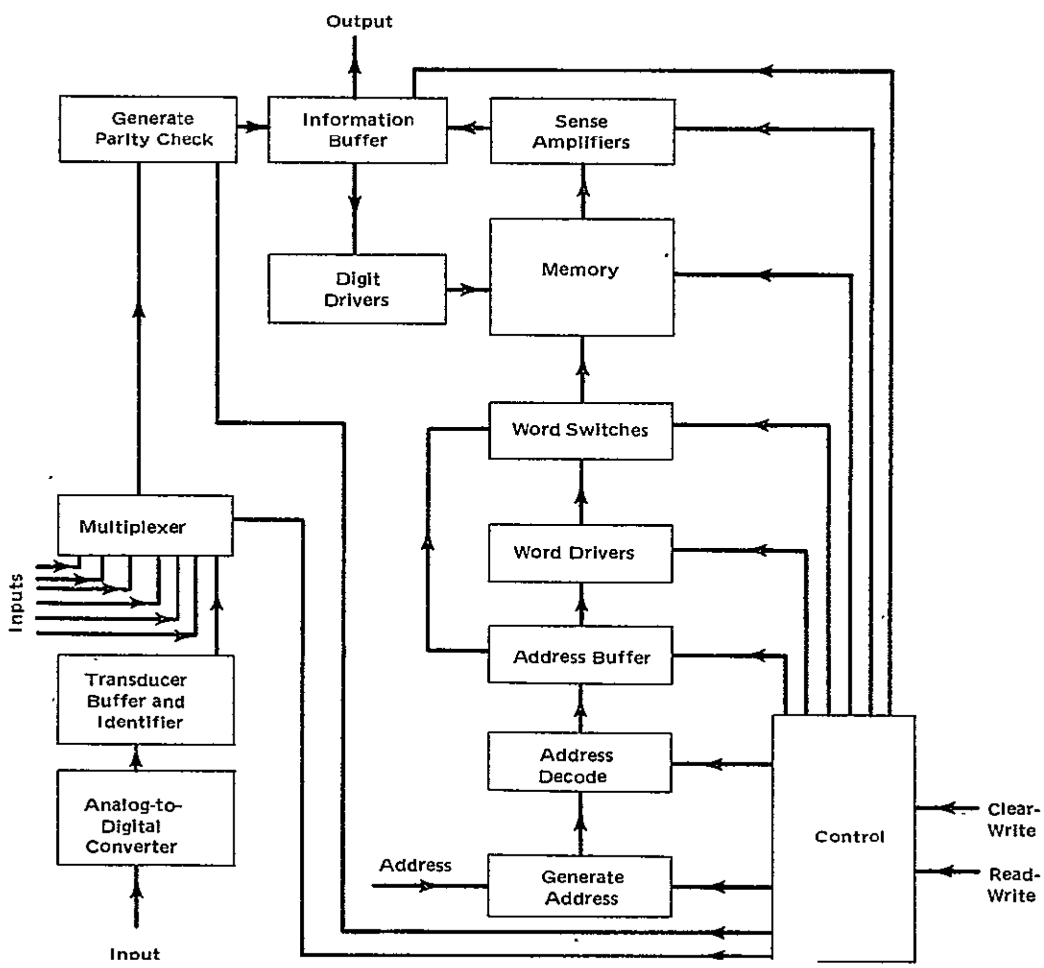


FIGURE 1 BLOCK DIAGRAM OF MEMORY SYSTEM

require interleaved buffers, so that the information in the full buffer may wait its turn for entry into the memory, while the others are storing new information. When the buffer is full, the block of information is read into the memory, along with the information identifier and parity checking symbols generated by the input data. The readout is performed on command by addressing the required words, storing them in an output buffer, and then transmitting them to Earth. Associated with the memory cells are clear, read, and write circuits and address circuits.

A serial memory system has an apparent advantage over a random access memory, since in the latter it is necessary to provide an input and output to every bit within the system, whereas in the former it is only necessary to provide one input and one output. However, in this case it is necessary to wait a definite time after a demand for information while the required bits reach the output. It is usually more convenient to arrange a serial memory in blocks with random access to each block rather than operate it as one continuous string of information. This reduces the average access time to any one bit, but it increases the associated electronics since each block must have input and output facilities and random access to the blocks is desirable in some applications. If the storage medium is non-volatile, power switching between blocks is possible and the overall power consumption is then equivalent to that required by one block. Also, if random access to the blocks is not required the control electronics can be simplified. Figure 1 also applies to a memory arranged in blocks with random access between blocks if the identifiers "word drivers" and "word switches" are replaced by "block drivers" and "block switches." An extra unit must be added to the system diagram to operate the memory media in each block. This is a small additional complication in view of the large reduction in components associated with the change from addressing individual bits to addressing blocks of several thousand bits. Within each block there is usually some flexibility. One block may consist of several serial strings of bits in parallel, so that when it is accessed, the output is a series of words bit-parallel.

Each memory system must have suitable power supplies and adequate mechanical support. The different technologies will need different sizes and layouts of subsystems supplied by standard electronic circuits. The mechanical structure will vary from system to system.

Performance Parameters -- To pursue the trade-off studies in a meaningful manner, a set of operational parameters which describe each system is necessary. Table VI lists a matrix of numerical parameters based on the system's size and weight, its data capacity, and its rate of operation. Table VII is a check list of parameters describing the system's response to the mission environment. In many cases this can only be a qualitative allocation to good, indifferent, or bad categories. The parameters are derived from the total memory system and not just the memory cells

TABLE VI

MATRIX OF OPERATIONAL PARAMETERS

Performance Value		Capacity (bits)	Data Transfer Rate (bits sec^{-1}) Write	Read
		A	B	C
Weight (lb)	V	A/V	B/V	C/V
Volume ($in.^3$)	W	A/W	B/W	C/W
Quiescent Power (W)	X	A/X	-	-
Write energy/bit (J)	Y	A/Y	B/Y	-
Read energy/bit (J)	Z	A/Z	-	C/Z

TABLE VII

CHECK LIST OF RESPONSE TO ENVIRONMENTAL INFLUENCES

Response to temperature changes

Response to shock

Response to vibration

Response to radiation

Mean time between failures

themselves to get a clearer picture of the trade-offs which are possible.

During the trade-off studies not all the parameters in the performance matrix carry equal importance. Each situation has to be assessed on its merits, but the performance matrix gives a numerical basis for intercomparisons. The precise definition of the data transfer rate will depend on the individual circumstance also. If the memory system has destructive readout and it is desired to keep the information, then time must be allowed for a rewrite process. In a non-destructive readout system there is only need for an access time which is composed of different parts, depending on the nature of the system. For example; in a magneto-optical memory the access time consists of the address decoding time plus the beam deflection time, while in a plated wire system the access time consists of the address decode time, the switching time, the pulse delay along the wire, and the magnetic domain switching time. In this work the data transfer rate is taken as the reciprocal of the time required to present the information at the output after an address has been called out, multiplied by the number of bits at each address which appear in parallel.

The environmental check list refers to those characteristics most likely to be troublesome, whether they occur during the operational or non-operational times of the mission. Although these are the chief operational parameters, the production and cost-benefit parameters have not been neglected. Questions of yield and expense are important, and the best use of the payload throughout the mission is also a definite requirement. If it is possible to dedicate part of the memory to computational uses during the mission, thus reducing the size of computer memory required, then this is a desirable feature of the system. There is a trend in very complex missions to provide time-sharing facilities for those parts of the various subsystems which are common, rather than make each subsystem self-contained.

Table VIII presenting the performance matrix and environment check list for state-of-the-art tape recorders, gives an indication of the targets for competing technologies. The figures for bits per pound and bits per cubic inch are impressive, especially when it is noted that they include the weight and size of all the associated mechanics and electronics. There is no doubt that tape recorders are an excellent solution to the buffer store problem, except for the performance deterioration and life-time difficulties.

TABLE VIII

PERFORMANCE MATRICES AND ENVIRONMENTAL CHECK LIST

(a) Performance matrix for the Nimbus D tape recorder.

Performance Value		Capacity (bits)	Data Transfer (bits s^{-1}) Write	Read
		1.7×10^8	2.0×10^4	6.5×10^5
Weight (lb)	30.8	5.5×10^6	6.5×10^2	2.1×10^4
Volume (in.^{3})	-	-	-	-
Write energy/bit (J)	4×10^{-4}	4.3×10^{11}	5×10^7	-
Read energy/bit (J)	2.3×10^{-5}	7.4×10^{12}	-	2.8×10^9

(b) Performance matrix for the Leach 2000 series tape recorders.

Performance Value		Capacity (bits)	Data Transfer (bits s^{-1}) Write	Read
		1.4×10^8	2×10^3	4×10^5
Weight (lb)	15	9.3×10^6	1.3×10^2	2.7×10^4
Volume (in.^{3})	290	4.8×10^5	6.9	1.4×10^3
Write energy/bit (J)	2.5×10^{-3}	5.6×10^{10}	$.8 \times 10^5$	-
Read energy/bit (J)	6.3×10^{-5}	2.2×10^{12}	-	6.4×10^9

(c) Performance matrix for the Mariner IV tape recorder.

Performance Value		Capacity (bits)	Data Transfer (bits s^{-1}) Write	Read
		6.5×10^6	2.1×10^4	16.7
Weight (lb)	16.8	3.9×10^5	1.3×10^3	1
Volume (in.^{3})	481	1.4×10^4	4.4×10	3.5×10^{-2}
Write energy/bit (J)	1.9×10^{-4}	3.5×10^{10}	1.1×10^8	-
Read energy/bit (J)	2.4×10^{-1}	2.8×10^7	-	7.0×10

(d) Environmental checklist for the tape recorders.

Response to temperature changes	Adequate at ambient temperatures
Response to shock	Poor
Response to vibration	Poor
Response to radiation	Good
Mean-time between failures	$\sim 10^4$ hours

II. DISCUSSION OF MEMORY SYSTEMS

This chapter reviews the different functions essential to operation of a memory system and describes the different approaches which can be taken to perform these functions. The trade-offs possible between selected examples of the different approaches are detailed and their influence on the system parameters indicated. The last part of the chapter covers the commercial aspects of the development of a mass memory technology.

Capacity

The capacity of the memory is defined in the contract. It is essential to be able to store up to 10^8 bits, using a system based on all solid-state technology. This is approximately the storage capacity of the tape recorders presently used in space missions. It also falls in a range which causes difficulty in the choice of technologies. This choice is made more critical by NASA's desire to utilize this technology in the mid to late 1970's. Several technologies will be available to provide memories of capacity between 5 and 10 x 10^6 bits in the mid 1970's (see Table IX). It is the increase in capacity by an order of magnitude in that time scale which causes difficulties. For memories of 10^{10} bits, or more, the only obvious candidates are the electron beam and optical memories. However, in each case, it is unlikely that commercial read-write memories using these technologies will be available until the mid 1970's.

Weight

The memory should weigh as little as possible. Tape recorders weigh a few tens of pounds and this is obviously the target weight for a replacement. Of the systems considered in this report, only the electron storage tube can store data in analog form so the replacement of a tape recorder by a solid-state system means that analog-to-digital (A-to-D) converters must be supplied between the sensors and the memory. The number and arrangement of A-to-D converters will be discussed further when data rates are examined. However, their weight must be included in a memory system which, as far as the user is concerned, must have similar interfaces to a tape recorder.

The different types of memory technology will have different weights for a 10^8 bit memory. Each system has contributions to its total weight from the storage medium, the electronic circuitry used for interfacing with the storage medium, the supports for these parts, the protection for these parts, and the main frame on

TABLE IX

CLASSIFICATION OF TECHNOLOGIES BY CAPACITY AND AVAILABILITY

Technology	Typical Capacities (bits)	Time Available (present and fugure)
Ferrite Core	10^3 to 20×10^6	To late 1970's
Plated Wire	10^3 to 10^7	To late 1970's
Integrated Circuits	10^2 to 10^7	Throughout 1970's*
Bell Bubble Memory	10^5 to 10^9	Doubtful
Optical	$\geqslant 10^8$	After 1970
Electron Beam	$\geqslant 10^8$	After 1971
Sonic BORAM	4×10^6 to 10^8	After 1971+
Travelling Domain (Magnetic Shift Registers)	10^3 to 10^7	Throughout 1970's

* The larger systems will be available during 1971.

\+ The commercial future of this technology is still in doubt.

which the whole unit is mounted. A convenient classification of the technologies is in terms of the physical configuration of the storage medium (see Table X). Some technologies appear more than once in the table. Thin film memories can be made either as discrete systems with one element per bit, as planar memories with many hundreds of thousand bits per plane, or as strip systems with several hundred bits per inch. The distinction between the two types of planar memory listed lies in the number of bits per plane. Integrated circuits and some types of travelling domain systems only have a few hundred to a few thousand bits per plane, so a large memory must consist of several thousand planes. The other types of planar memory are all capable of storing up to several million bits per plane, so only a few planes are needed to form a large memory. "Beam access" describes all the memories which utilize optics and electron beams.

Discrete Element Memories -- The weights of a ferrite core memory and a discrete element film memory are minimized if the size and weight of each core or element are reduced. This weight reduction is principally associated with the change in size of the substrate forming the support for the bit elements, since each element is of microscopic weight, for example, 25 μg per core. By reducing the element size, less substrate is required to carry the total memory. However, the substrate cannot be made too thin or the elements too small. A skimpy substrate would be too fragile, and there are wiring difficulties associated with both technologies if the elements are too small.

There are restrictions placed upon the size of each substrate by the need to make connections. Random access memories require two or more wires at each element and these wires have to be taken to terminals at the edge of the substrate. Current commercial practice puts terminals at spacings between 0.125 and 0.05 in. Smaller spacings are possible and by using staggered rows of terminals, several hundred lines per inch can be achieved. However, at this point the wiring problems become more difficult and questions of cost and yield become important.

Associated with these memories are address registers and decoders, low level switches, information registers, drivers and sense amplifiers. For a 2D-2W random access memory there must be $2\sqrt{N}$ word drivers, N word switches, m bit drivers, m sense amplifiers, one m-bit information buffer and one 2^k-bit address buffer, where $2^k = N$ is the number of m-bit words in the memory (Figure 2). This is the minimum electronics required, since parity generation circuits and multiplexers are needed in many applications. The memory controller, the sensors, and the power supply are not included as parts of the memory system in this description. The overall weight of the system is reduced if the size of the components is minimized or integrated circuits are used. In both cases these limits are set by current practice, power dissipation, the basic laws of Physics and the materials available. As far as possible,

TABLE X

CLASSIFICATION OF MEMORIES
BY PHYSICAL CONFIGURATION OF STORAGE MEDIUM

Class		Examples
Discrete		Ferrite core, Thin film
Wire		Plated wire, Delay line, Sonic BORAM, Travelling Domain
Plane	(a)	IC, Travelling Domain
	(b)	Thin film, Laminated Ferrite, Etched permalloy, Travelling Domain, Beam access
Strip		Thin film, Delay line, Sonic BORAM, Travelling Domain

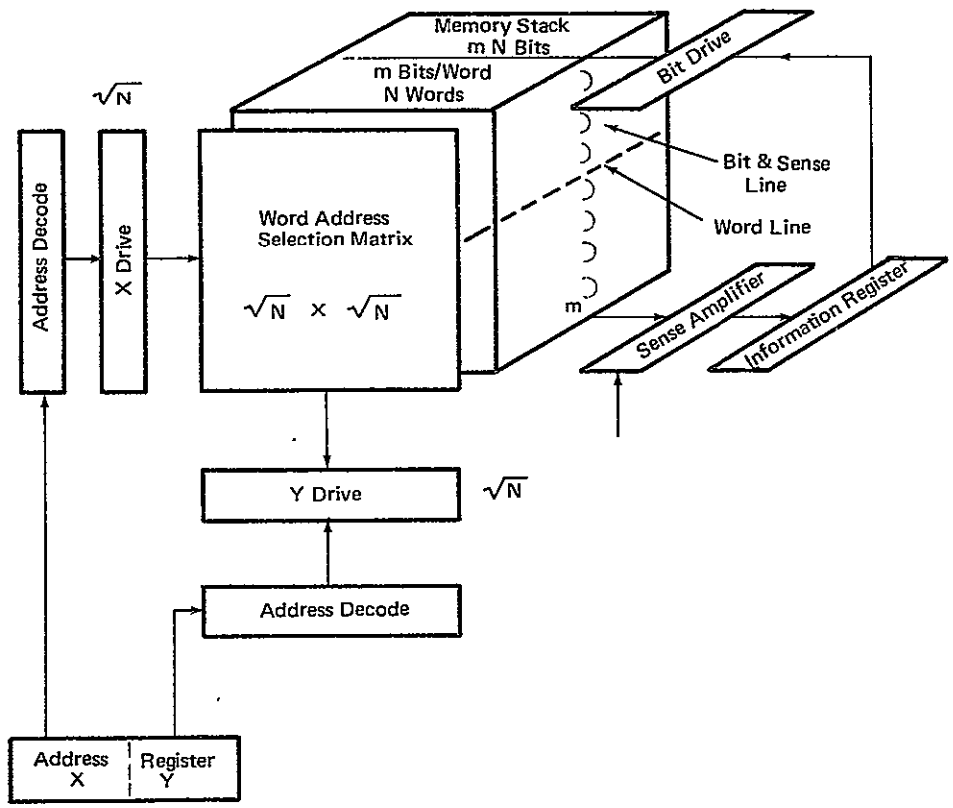


FIGURE 2 2D-2W MEMORY WITH ADDRESS SELECTION MATRIX

the associated circuits should be made using IC's to reduce the weight. One of the more difficult circuits to make as an integrated circuit is the driver for a ferrite core memory. This circuit has to produce current pulses with several hundred milliamps amplitude and rise times of perhaps 50 ns in a load with an inductive component. To generate these pulses, the drivers require voltage sources four to five times larger than those used to power ordinary integrated circuits. However, once the pulse is established, all that power is no longer required. Less than half the power generated in conventional core drivers actually gets delivered to the load; the wasted power heats up the transistors in the current source which adversely affects the circuit's reliability. Considerable improvement can be made by using two power sources, one at a high voltage to establish the current level in the pulse and the other at a low voltage to maintain the current level until the pulse must be turned off. This type of system can be made using hybrid thin film techniques.

There are many ways of arranging the circuits with respect to each other and the memory cells. There are trade-offs here between the various arrangements and parasitics, signal delays, etc. The three major approaches are to put all the circuits on the same substrate as the memory elements, to put part of the circuits on the same substrate, or to put none of them on the substrate. The optimum technique is that which reduces the number, length, and complexity of the interconnections. Each discrete interconnection point requires either a pad, a pin, a soldered joint, or a wire wrap connection. They all require space, have weight, and reduce the reliability. A soldered joint uses about 5 mg of solder, and about 0.1 in. of wire is dedicated to it, as well as the connector pin, pc board eyelet, etc. So the total interconnection weighs about 10 mg. In a 10^8 bit memory, where there might be 10^6 interconnections depending on the technology, they weigh 10 kg. Conventional pin-connector arrays weigh about 500 mg per pin so it is necessary to reduce the number of pins to a minimum also. Wire wrap connectors need a firm, solid pin and use more wire per connector than a soldered joint.

It is not feasible to make a 10^8 bit memory with these technologies as a single module. Each module requires interconnects and supports also. Obviously, these are reduced if the number of modules is minimized, which means that the number of bits per module must be maximized. This occurs when the modules are made with the maximum number of bits per sense and drive line that the electronics can handle. In fact, this is the most critical factor in the design of a large capacity unit since it determines both the number of modules and the amount of electronics required, and these are major weight factors.

Wire Memories -- The storage medium in the various wire memories contains more than one bit per wire. The best condition is to have the maximum number of bits per unit length. However, this is limited by other factors, such as domain wall creep and the accurate placing of the other wires in the system with respect to the bit locations. Therefore, there is an optimum number of bits per unit length, which determines the length of wire needed to supply the total number of bits. Assuming 5 mil diameter wire and a linear bit density of 40 bits $in.^{-1}$, the total weight of plated wire required for a 10^8 bit memory is 5 kg. This contrasts with the 2.5 kg of ferrite needed in a 10^8 bit core memory. There has to be a support structure for the storage wires and the other wires needed. The plated wire array is a 2D-2W memory, and the total unit is minimized by having a small number of modules interconnected in the simplest manner. Each module should have the largest number of words, the bit count of which is equal to the number of words. This squaring of a 2D-2W module reduces the amount of electronics. Again, the maximum size is determined by the number of bits which a line can handle without disturbing the signals. For a plated wire this is about 500 to 1000 bits.

The other wire systems are all bit-serial in organization. The travelling domain and delay line structures usually have the storage wire wrapped in a spiral around a cylindrical former. Here, a significant decrease in the amount of associated circuitry can be achieved if the block length has a large number of bits. The critical parameter in the acoustical systems is the acoustical loss per unit length. Thus it is important to have the best linear bit packing density in a low loss material to give the maximum number of bits per dB loss, and thus the smallest number of input and output circuits. The acoustical systems have an advantage over the travelling domain systems since they do not require extra power to keep the data flowing once it is launched. The travelling domain systems require the provision of a wire driving system which increases the weight, complexity, and power required in the system.

Similar arguments apply to the minimization of the weight of most of the planar random access memories and serial systems. The bits/circuit ratio must be maximized without jeopardizing the successful operation of the memory by loading the lines, causing a deterioration in the signal-to-noise ratio, or requiring increased power. Also the bit density has to be increased to a maximum without causing adjacent bit interference, reducing the signal-to-noise ratio, or imposing too stringent mechanical constraints. Unfortunately, most serial memories have rather a poor linear bit density so they are unable to take full advantage of the improved bits/circuit ratio which many show; therefore, they do not necessarily have a great advantage over random access memories in terms of weight or volume.

Planar Memories -- The beam access systems are a special case of planar memories because the bit density is usually so high that the actual amount of storage material is minimized. The real weight lies with the associated equipment, the beam source, modulators, deflectors, and detectors. Also, because of the high alignment accuracy required, they need very rigid mechanical supports. Frequently, displacements in length are not so important as any change in angles. Mechanical distortions usually lead to a rapid deterioration in the operation.

The IC memory and some types of travelling domain memories are another special category from a construction viewpoint. Currently they are built from many small modules, each containing about 1024 bits. The presently available travelling domain memories are larger than IC memories and there is little likelihood of this situation altering in the immediate future. Therefore, the IC memory is taken as the best example of this type.

Current MOS technology can make a RAM with 1024 bits on a chip about 0.1 by 0.1 in. This is a very good packing density, but it will be improved when the variable threshold MOS (MNOS) comes along as a product (see Table XI). Although no one has achieved 8k bits on one chip using MNOS technology, this does not appear to be beyond the bounds of possibility in the future, since manufacturers are already putting several thousand transistors on a chip for read only memories. However, regardless of the number of bits on a chip, the package in which it is mounted to supply mechanical protection and support for the leads has a size determined mainly by the number of leads and their spacings. For this reason, and the fact that a large number of leads means a decrease in reliability, it is important to organize the overall system with the minimum number of leads per IC. This is determined to a great extent by the circuit design and the technology used to produce the circuits. The weight and size of the package completely dominates the weight and size of the IC in the package. At the next stage the packages have to be mounted onto printed circuit boards. These are then mounted on mother-boards, etc., and at each step the weight and size are determined by the larger component rather than the smaller components used at the lower steps. So, the problem becomes one of establishing the weight and size of the frame, wire harness, and large boards necessary to provide 10^8 bit capability. The most convenient way to reduce this, and simultaneously increase the reliability, is to put as many bits on each chip as possible. The limits here are determined by the bit cell size, which is smallest for variable threshold transistors, and photolithography, which determines the largest circuit with the finest dimensions which can be made. Beyond this, the question of yield and cost is important for large area chips. Although MNOS appears attractive in terms of the area per bit, the questions of yield have not as yet been resolved.

Of course, there is no need to package each chip individually. Some form of hybrid circuitry can be adopted which puts several chips on one ceramic substrate and then package the substrate. The ceramic substrate usually weighs far more than the chips, but its weight and size are lost with respect to the printed circuit boards and higher level packaging. The main difficulty with this

TABLE XI

TYPICAL BIT AREAS ON INTEGRATED CIRCUITS

Technology	Area per bit+ (mil^2)	
	1970	1972-73
Bipolar	100-250	75-200
Static MOS	25-30	15-20
Dynamic MOS	10-15	8-10
CMOS	75-100	45-50
Self-aligned MOS*	15	10
MNOS	1	0.5

---

* Either Si - gate or ion-implanted alignment.

\+ These areas are for random access read/write memories and include the area of the associated circuits also on the chip. Cell sizes for read only memories based on MOS are about one-quarter those given for static MOS.

approach is the reliability of the bonds attaching the components to the substrate. Since rework is certainly forbidden for high-reliability systems, unless redundant bonding positions are supplied, and the success of placing and bonding chips is low, it is not possible to put many chips on a substrate, five being about the maximum. This is probably worthwhile from the point of view of weight and size if the bonds can be demonstrated as reliable, but the introduction of redundant bonding pads on the substrate means a reduction in the bit-packing density.

If the bits on the IC chips have an area of 1 mil^2, the weight of silicon involved in a 10^8 bit memory is only about 0.3 oz. If the chips forming this memory are bonded to a substantial ceramic substrate, the weight of substrate required is about 7 oz. Suitable flat packs capable of taking three to five IC's weight about 0.1 oz each; thus the total weight of flat packs for a 10^8 bit memory is about 17 lb. These figures are approximately correct for an MNOS memory with 8k bits per chip and 5 chips per flat pack, each flat pack carrying 24 leads. Feth and Smith (Ref. 4) discuss IC packaging techniques using flat packs. It does not appear to matter which technique is used to interconnect IC's; the weight and volume of the memory are determined mainly by the package size and the interconnect pattern used for the packages. The real need is to get as many bits as possible into the basic package which means both the smallest bit cell possible and the largest number of chips per package which is reasonable. The discretionary wiring techniques offer alternate ways of increasing the number of bits at the lowest level. Here multilayer metallization is used to interconnect good circuits on an IC wafer. The good circuits must first be identified by electrical testing and the metallization pattern established using a computer-aided design algorithm. Texas Instruments have pioneered in this area (Ref. 5).

Strip Memories -- The memory systems based on strips of material have many characteristics similar to those of RAM and serial memories based on discrete, wire and planar storage elements. The highest linear bit density compatible with satisfactory operation of the memory and the maximum number of bits per drive/sense circuit are required. The spacing of the strips of storage medium and the positioning of the orthogonal circuits performing either sense or drive functions are mainly determined by the type and size of the interconnections used.

Discussion -- The arguments presented above point toward a system with serial operation, a large number of bits per input/output circuit, the maximum possible bit density, and no need for local drivers at every bit location as having the least weight. Table XII gives bit densities per unit area for some technologies, and Table XIII gives typical values of the number of bits per line that various technologies can handle.

There is an interesting contrast between the limiting bit

TABLE XII

STORAGE AREA BIT DENSITY OF SEVERAL TECHNOLOGIES

Technology	Bits in.$^{-2}$
Ferrite Core	500-2000
Plated Wire	500-2500
Thin Film	$10^3 - 10^4$
Bubble *	$10^4 - 10^6$
Sonic BORAM	1000-3000
Beam Access Memories *	$10^7 - 10^9$
Metallic Magnetic Shift Registers	1000-2500

* Predictions

TABLE XIII

TYPICAL VALUES OF THE NUMBER OF BITS PER LINE
DETERMINED BY ELECTRICAL CHARACTERISTICS

Technology	Number of Bits
Ferrite Core	256 - 4096
Plated Wire	512 - 1024
Thin Film	256 - 1024
Delay Line *	2000 - 60,000
Sonic BORAM **	128 - 512
Bell Bubble Memory +	$10^3 - 10^5$

* Depends on type, e.g., quartz, glass, or magnetostrictive wire

** Principal limitation is the acoustic absorption in the substrate

\+ Estimate

densities of MOS, MNOS and the Bell bubble system. In each case, photolithography limits the smallest size component possible. For a dynamic MOS device, which needs at least three components per bit, this means a lower ultimate packing density than in a bubble memory (based on a T-bar structure) which needs two components per bit or an MNOS memory which only needs one component per bit.

Volume

Most of the comments on the weight trade-offs among the technologies apply to the volume as well. The lightest memory system is likely to be the smallest. Typically, the density of electronics equipment is about 50 to 100 lb ft^{-3} so the target weight of 50 pounds is roughly equivalent to a volume in the range of 1000 to 2000 $in.^3$ Obviously, the technology which gives minimum weight and highest density is desirable.

The density is limited by many of the factors which limit the weight. The main ones are the bit packing density, the ratio of the number of drive-to-memory elements, the number of connections, and the need for substantial mechnnical support and protection. However, another important factor, one which influences the weight also, is the allowable power dissipation within the unit.

It is an important design objective to reduce the power to a minimum, but this minimum may still be too large for adequate cooling of a densely packed memory. The sources of heat will be distributed within the memory, and heat will pass by conduction to the outside of the unit where it will be radiated into the surrounding volume. This radiation rate will limit the outflow of heat and, together with the thermal resistances in the memory, fix the rise of temperature. This must not exceed the upper operating limit of the circuits in the memory. Therefore, the packing density of the components and the related increase in power dissipation per unit volume are very important parameters. It is not desirable to let the unit operate at its rated maximum since this reduces the operating margins considerably. Also, it is not desirable to introduce fluids and allow natural or forced convection. It may be necessary to introduce special materials and components into the system to reduce the thermal resistivities. The largest possible area of radiating surface should be supplied. If the memory is made in modular form, each module will have to have adequate cooling, and this means that they should not radiate directly at each other or at any other radiating surface.

Most of the technologies examined dissipate power at a rate between 5 mW $in.^{-3}$ and 250 mW $in.^{-3}$ The most important exception is the CMOS memory which may have to dissipate over 1 W $in.^{-3}$ As far as individual IC packages are concerned, this is reasonable since they can usually dissipate about 1 W per package without special precautions being taken. This is an unrealistic figure for larger systems since the heat transmission paths to the outside world are much longer. For this reason the more conservative figure of 100 mW $in.^{-3}$ is suggested as the limit. It matches well with the experience gained from tape recorders and the likely power dissipation of most of the solid-state technologies investigated. The power dissipated depends on the data rate in most technologies. For this reason it is more useful to discuss the energy requirements to read or write one bit than the power dissipation. Table XIV lists typical energy requirements for several technologies.

Power

Power dissipation is the most important parameter of the memory system. The influence of power on the allowable packing density of electronics was discussed above. The other important aspect is that each extra watt required means a larger power supply must be carried in the satellite. The tape recorders used at present use up to 30 watts of power, depending on the type and the data rates involved. As far as possible this figure should not be exceeded in the replacement system.

The question of the best type of power supply to use for a particular mission is quite complex (Ref. 6), (see Figure 3). The choice depends on the mission duration, the flight path (whether it enters the shadow of the Earth or not), and the peak and average power demands. For any one power supply technology, there is a non-linear relationship between the weight of the supply and the power produced. For example, a 50 watt thermal generator weighs about 10 pounds while a 250 watt unit, using the same technology, weighs 218 pounds. Therefore, there is the possibility of making trade-offs between the weight and power consumption of various memories and the overall satellite weight. It may be advantageous to choose the heavier technology with the smaller power consumption. In this case, a smaller power supply may be capable of supplying the power and the decrease in the weight of the supply may offset the increase in weight due to choosing the larger memory system.

There are several contributions to the power dissipation. The main ones are:

1. The energy required to write and read the data;
2. The energy needed to keep the data moving in a serial system;
3. The power dissipation in the associated address decoders, switches, drivers, and sense circuits.

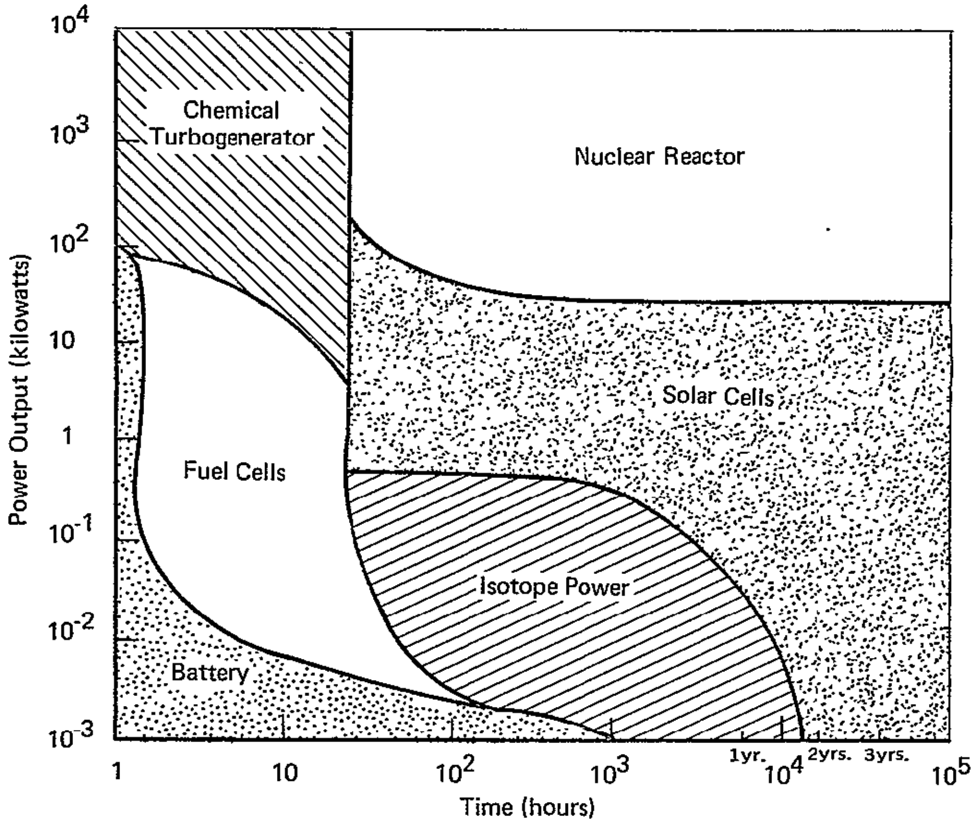
The technology with the lowest power dissipation is the one which needs the least energy to write and read data, has a low data rate, does not need power to move or maintain the data once stored, and has very few address, drive, or sense circuits. The serial memories show up well in this comparison. One sense amplifier can serve many thousands of bits; addressing is elementary between bit

TABLE XIV

TYPICAL ENERGY* REQUIREMENTS TO OPERATE ON ONE BIT

Technology	Energy (J)
Ferrite Core	6×10^{-10}
Plated Wire	1.3×10^{-11}
Thin Film	10^{-11}
Sonic BORAM	4×10^{-13}
Bipolar IC	3×10^{-10}
MOS	4×10^{-9}
CMOS	10^{-10}
Bell Bubble Memory	10^{-13}

* The energies given include the dissipation in the associated circuits, the dissipation in the lines, and the energy to change the bit.



Source: NASA SP-154, Aerospace Electronic Systems Technology: A Briefing for Industry, p 161, May 1967.

FIGURE 3 POWER OUTPUT AND LIFETIME FOR VARIOUS TYPES OF POWER SUPPLY

streams and depends on timing within the bit stream.

Acoustical delay lines are very attractive for low power dissipation, except that it is a continuous demand. Once switched off, they lose data. This volatility is not shared by the sonic BORAM or the various magnetic shift registers. Once the acoustical pulse is launched in the sonic BORAM no more acoustic driver power is needed. In contrast, the magnetic shift registers need driving power to move the bits. Here the Bell bubble has a big advantage in circuit simplicity, since it does not need individual drivers at each bit location. Apart from MNOS, all the IC circuits are volatile and need drive power at each bit when operated as a shift register. It makes little sense to use MNOS in a shift register, since that requires several transistors per bit and spoils the bit packing density.

In random access system there are several ways to reduce the power requirements. These mainly involve operating at a slow data rate so that the read and write energy dissipated per second are reduced and the power required to drive fast rise-time pulses at a high repetition rate down long lines is minimized. Also, switching between sense amplifiers is possible. Of all the circuits in a typical memory the ones which take the most power are the sense amplifiers. Therefore, they must be well designed and their number kept to a minimum. The number required depends partly on the data rate and the data paths provided. Parallel writing and reading requires more electronics than serial processing of the data. If there are likely to be many delays between uses of the system, on-off switches either at the individual circuit, module, or system level are mandatory. This helps reduce the standby power. However, care must be taken to avoid loss of data when switching transients occur. Also, if the storage medium is volatile, switching the power supply off is not feasible.

In every technology there have been continuing attempts to reduce the energy required to write and read bits in the storage medium. For instance, a lot of attention has been directed to producing new ferrite core materials which need less current to produce switching of the magnetization.

Integrated circuits do not show very well in these trade-offs because of their high operational power requirements and their volatility which makes the supply of standby power essential. This explains the interest in CMOS, which has a low standby power, and MNOS which, in fact, is not volatile. The use of CMOS circuits for the electronics of other technologies may help improve their power performance. In an all CMOS memory system, it is not clear how the total standby power required would be related to the standby power of a single bit since there are many metallization paths offering chances for extra leakage. As far as possible, a volatile memory should be avoided.

The data rate and the way that the data flows through the system also influence the total power dissipation. An important factor is the number of A-to-D converters required. A single 8-bit A-to-D converter digitizing at 10^6 bits per second requires several watts (discussed below under "data rate"). There is a saving in power if non-destructive readout is possible, since there is then no need to rewrite the information using more energy in the process.

A memory technology with non-volatile storage, capable of operating in the serial mode and associated with efficiently designed electronics organized to allow power switching, seems to be the best system for power consumption.

Data Rate

The primary functions of the buffer memory in a space vehicle are to store the information until the appropriate telemetry channel is ready and to change the data rates so that the telemetry channel is used most efficiently and with a low error rate. Tape recorders perform the data rate change in analog form by changing tape speed. In other memories the change can be performed in one of several ways. However, there is a more important problem which influences the data rate, power, size, and weight of the memory, namely, the need for A-to-D converters. With one exception (the storage tube) all the systems discussed store digital data only. Therefore, the analog data from the sensors must be digitized before storage. A second problem is whether the data rate has to be increased or decreased through the buffer.

For an Earth orbital satellite, the normal requirement is to dump the data back to Earth at a far faster rate than it is collected. Typically, tape recorders involved in these missions are required to collect data at rates between 1 and 100 kHz and dump it to Earth at rates between 100 kHz and 1 MHz. Most of the solid-state memories considered in this contract can handle the write data rates without any difficulty. Even the electrically alterable read only memory based on MNOS can operate at a few kHz write rate. (For the other technologies, see Table XV.) Comparison of the typical performance demands made by the sensors and performance of several technologies indicates that the memory system could be operated in word-serial-bit-serial mode and still cope with the data. This means that only one A-to-D converter, capable of digitizing at a sample rate between a few kHz and hundreds of kHz with adequate accuracy for the experiment, say 6 to 10 bits per sample, would be required.

This simple configuration offers advantages in size, weight, and power. A-to-D converters typically are 10 cubic inches in volume and require 4 watts to operate at about 50 kHz. However, the serial configuration fails to utilize fully the capabilities of those memory technologies which can accept data at a faster rate. In this case, if the weight and power restraints allow, it is possible to increase the data rate by adding more sensors or by giving

TABLE XV

TYPICAL READ AND WRITE DATA RATES *

Technology	Data Rate (bits s^{-1})	
	Write	Read
Ferrite Core	$10^5 - 2 \times 10^6$	$10^5 - 2 \times 10^6$
Plated Wire	$10^6 - 8 \times 10^6$	$10^6 - 8 \times 10^6$
Thin Film	$10^6 - 2 \times 10^7$	$10^6 - 2 \times 10^7$
Bipolar IC	$5 \times 10^6 - 3 \times 10^7$	$5 \times 10^6 - 3 \times 10^7$
MOS	$5 \times 10^5 - 2 \times 10^6$	$5 \times 10^5 - 2 \times 10^6$
MNOS **	$10^3 - 10^6$	$5 \times 10^5 - 5 \times 10^6$
Bubble	$10^5 - 3 \times 10^6$	$10^5 - 3 \times 10^6$
Sonic BORAM	$8 \times 10^6 - 10^8$	$8 \times 10^6 - 10^8$

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* It is assumed that the memories are operated in the word-serial-bit-serial mode.

** Figures for an electrically alterable read only memory based on technology currently under development.

more complete coverage of the existing sensors. However, there is a limit set by the shortest reasonable cycle time of the memory system. At this point, the way to match the data rate to the memory cycle time is to arrange the memory so that it accepts data as serial-characters-parallel-bits. This requires several interleaved serial-to-parallel shift registers which are loaded in serial mode, while the data in one is being read into the memory bit-parallel. The arrangement requires extra control electronics and, either a digital multiplexer between the A-to-D converter and the shift registers, or several A-to-D converters between an analog multiplexer and the shift registers. In this way, the signals from one sensor are always fed at the appropriate moment to one A-to-D converter and shift register. The limit to the rate at which data can be written into the memory is set by the hardware limitations since, in principle, it is possible to deal with data in bytes of several thousand bits in parallel. Writing 7, 8 or 9 bit bytes in parallel is a much simpler job requiring less electronics.

All these comments are appropriate to both random access and serial memories. However, they do require asynchronous operation of the memory, that is, the memory can write in data at any time on command as long as it is not already writing in or reading out data. In contrast to this, some of the shift register technologies, such as the sonic BORAM, can only be operated synchronously, that is, they can only accept data at precisely defined intervals. This is no difficulty, in general, since the memory cycle time acts as the controller and selects the data at the correct rate from the information buffers and controls the switching between the buffers. There is difficulty if the synchronous rate is much faster than the data rate. The solution here is to interleave the data so that neighboring bits in a character or a data stream do not occupy neighboring sites in the memory. This requires the recycling of the data and precise control of the timing so that eventually the memory is filled with data. Alternatively, a small buffer can be used to match the data rates by handling the data in blocks.

The data rate conversion can occur either by operating the memory at a different cycle rate on the readout, or by using a larger number of parallel channels on readout, or by multiplexing on readout. It is important at this stage to distinguish between Earth-orbital and deep-space missions. The former require an increase in data rate on readout, while the latter require a decrease. The input data rate is similar for both types of satellites so the description given above applies to both types of missions.

In asynchronous memories the decrease in data rate is easily made by making demands on the memory at the right intervals. If the data were read in bit-parallel, it would be best that it be read out bit-parallel. These data can be fed to several parallel telemetry channels, or they can be fed to a parallel-serial shift register and directed into one telemetry channel. The decrease in readout data rate usually is accompanied by a decrease in power consumption since a lower repetition rate and slower rise time pulses are now feasible.

If the memory is synchronous, then an extra buffer is required into which data are fed on demand and read out at the correct rate. This second small buffer must be capable of operating asynchronously. If necessary, the data can be interleaved into the telemetry channel on readout to get the correct rate, but this requires a recirculating memory system. If the data are interleaved, the timing information has to be conserved to allow sorting of the data back into the right stream of bits.

The simplest way to increase the data rate is to increase the readout rate of the memory to the required level. Otherwise, the memory has to be arrayed in blocks and the telemetry channel directed to the output information buffer of each block when the data are ready. If the telemetry channel is multiplexed between the buffers and the cycles of the blocks are staggered, then it visits other buffers while the first is being refilled with data. Parallel readout into parallel telemetry channels is the best idea for a high data rate.

The telemetry data rate from a deep space probe is fixed mainly by signal-to-noise and error rate problems, while from an Earth orbital satellite it is fixed by the desire to make full use of the measuring equipment and to reduce the time during which the memory is occupied by readout.

As far as possible, an asynchronous memory, the data rate of which are compatible with both the sensor and telemetry rates, is required. This system uses the least auxiliary electronics. A synchronous, recirculating shift register memory causes the most difficulties, especially if it is a high speed system. The synchronous serial memories which can be operated intermittently are somewhat more convenient. On the memory input side, a data rate mismatch between sensors and memory of an order of magnitude can be easily handled with a minimum of electronics. On the output side it is more difficult, and extra electronics and precise control sequences are needed. Tables XVI and XVII summarize the system arrangements possible on the input and output sides of the memory.

Reliability

As already discussed in Chapter I, the main environmental hazards are temperature, shock, vibration, radiation, and exposure to vacuum. Apart from the electron beam technologies, where there may be a need to protect the system from the ultra high vacuum of space, none of the solid-state technology systems is degraded by operation in a vacuum once it has been properly outgassed. However, the other environmental parameters are of definite interest. Table XVIII lists the probable response of the various technologies to the different parameters in a qualitative way. It is well known

TABLE XVI

TYPICAL SYSTEM ARRANGEMENTS ON THE INPUT SIDE OF THE MEMORY

Data Rates	Arrangements Summarized	
	Asynchronous Memory (RAM)	Synchronous Memory (serial)
$D_s < D_i$	Straightforward	Interleave data, requires re-circulation
$D_s << D_i$	Straightforward	Asynchronous buffer and intermittent synchronous operation
$D_s > D_i$	Serial-to-parallel conversion	Serial-to-parallel conversion
$D_s >> D_i$	A modular memory with many A-to-D converters or a digital multiplexer	A modular memory with many A-to-D converters or a digital multiplexer

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D_s is digitized data rate from sensors after analog multiplexing.

D_i is input data rate to memory.

TABLE XVII

TYPICAL SYSTEM ARRANGEMENTS ON THE OUTPUT SIDE OF THE MEMORY

Data Rates	Arrangements Summarized
$D_t > D_o$	Memory modules with staggered cycle times and multiplexing between modules
$D_t = D_o$	Straightforward
$D_t < D_o$	Asynchronous memory, straightforward. Synchronous memory, either read blocks on demand into an asynchronous buffer or interleave data into telemetry using data recirculation in the memory

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D_o is memory output data rate

D_t is telemetry data rate which can be varied within limits.

TABLE XVIII

RESPONSE TO ENVIRONMENTAL EXTREMES

Technology	Vibration	Shock	Temperature	Radiation
Ferrite Core	A	A	A	G
Plated Wire	A	A	A	G
Thin Film	A	A	G	G
Bipolar IC*	G	G	A	A ?
MOS	G	G	A	P
MNOS	G	G	A	P
Sonic BORAM	A	A	A	G
Bubble	G ?	G ?	P	G

G System has good ability to withstand extremes of the environment mentioned.

A System has acceptable ability to withstand extremes of the environment mentioned.

P System has poor ability to withstand extremes of the environment mentioned.

? Modifies the description towards a less acceptable class.

* Radiation hardened circuits.

that integrated circuits need special protection against radiation. Every technology will have some IC's associated with it to make a complete system, but in Table XVIII the influence of the various environmental parameters on these associated circuits is neglected.

Extensive work has gone into making integrated circuits resistant to radiation. This can now be done quite successfully, but it means that the bit density is drastically reduced. However, the circuits associated with other technologies can be hardened with no significant penalty. Fortunately, the average space environment is not as harsh as the military environments which might occur. The main influence on each technology are temperature and radiation.

The other aspect of reliability is the mean-time-between-failure (MTBF) of a system, even if it falls within the "good" category of Table XVIII for all parameters. The first factor is to reduce the component count as much as possible, since the MTBF decreases quickly as the number of components in the system increases. Those technologies which do not have discrete bit elements obviously have the advantage here. However, since ferrite cores and discrete thin films are really passive components, the decrease in reliability caused by employing them is significantly less than the decrease associated with an array of discrete active components. Harold (Ref. 7) quotes the failure rate for cores as about 2×10^{-7} % per 1000 hours. Active components can undergo an aging effect which leads to failure or to a reduced operating margin. Of the purely magnetic memories, plated wire has shown the most susceptibility to aging, but now the major manufacturers believe that they have this under control and report predicted operational lifetimes at elevated temperatures of many years.

Considerable data has been amassed over the years referring to the reliability of active components such as transistors and integrated circuits. Current experience points to a failure rate between 10^{-3} and 10^{-2} % per 1000 hours for integrated circuits. It is expected that there will be further reductions in the failure rates as IC technology matures still further.

After the active components, the next factor influencing reliability is the occurrence of interconnections, soldered joints, wire wraps, etc. It is essential to keep these down to a minimum also. For this reason massive plated wire, thin film, and ferrite core memories must be regarded with suspicion. It also emphasizes the need in mass core to use only two wires per core rather than more, even though the other organizations can reduce the count of the electronic components.

For ball bonds IBM claims a reliability of 0.00004 % per 1000 hours and they predict a 10^{-7} % per 1000 hours failure rate for their non-ball bonds on hybrid circuits. Normal soldered joints are predicted to fail at 0.0001 % per 1000 hours when the extra stress of space operation is included. Other bonding mechanisms which can be used for IC's are flip chips, beam leads, inverted beam leads, and spiders. The beam lead connection is very difficult to make on MOS devices because the rf sputtering involved destroys the dielectric layers. The spider or beam lead laminate bonding mechanism puts the lead on the printed circuit board and allows face-up bonding. This has several advantages. The process can be more carefully controlled and the chips subsequently inspected. Also, the chips are bonded onto a metallized alumina substrate which acts as an excellent heat sink. This technique has been developed by Motorola (Ref. 8).

The type of package used for the circuits is also important. Poor seals, weak leads, and a large number of leads can be troublesome. As far as integrated circuits are concerned, it is important to integrate as much as possible onto one circuit while at the same time maintaining a minimum lead count.

With the figures given above for reliability of IC's and bonds, it is estimated that a system must have less than 1000 IC's and 100,000 bonds to have an MTBF of 10,000 hours.

Discussion

It would appear that the most desirable technology for the smallest, lightest mass memory which uses the least power, has zero standby power, is non-volatile, and has the appropriate data rates and good reliability is a magnetic serial shift register memory, which has:

(a) a large number of bits per input/output pair,
(b) has a good linear bit density,
(c) is composed of light material,
(d) has very little interference between adjacent lines even when closely packed,
(e) is already integrated,
(f) has few interconnections, and
(g) can be operated asynchronously at a reasonable data rate.

The Bell Telephone Laboratories' bubble memory immediately comes to mind, but there are several other aspects to consider such as availability, cost, reliability, and commercial feasibility.

Commercial Aspects of Memory Development

It is believed that the overall market for computers and associated equipment will reach $7 to $10 billion within five years. There is a continuing trend toward the memory system being the major cost factor in a data processing system, perhaps 40% of the total. Therefore, there is a definite incentive to manufacturers to develop new and improved memory equipment.

In the commercial world, cost is the most important item in deciding between competing technologies which have approximately equivalent functions. In fact, offering more sophistication at a higher cost does not necessarily generate more sales (Ref. 9). Since cost is the overriding factor in many decisions, it also influences strongly which technology will be backed during the development stages. This information is of prime importance in deciding what will be available in the mid 1970's. NASA is also interested in the availability of reasonable systems at competitive prices which are developed by industry as a result of commercial pressures and modified to NASA's requirements at a minimum cost. In fact, the technologies available to NASA are those which interest the data processing industry also. It is most unlikely that NASA will wish to develop through R & D grants and hardware and equipment procurements a mass memory technology totally unrelated to industry's needs. It will be necessary to support the development and modification of a commercial technology to make a flight-tested and space-proven memory suitable for the particular requirements of the mission involved.

The memory markets today are dominated by ferrite core, moving media systems, small high speed integrated circuit systems, and, to a lesser extent, plated wire. Apart from some specific applications, industry appears to have discarded planar, thin film memories because the promise offered by this technology was not achieved rapidly enough and it was overtaken by developments in other technologies. The moving media systems are not appropriate in this contract, leaving core, plated wire, and integrated circuits as the technologies which are appropriate and available today to commercial users at reasonable cost. The three technologies which appear to have the most attractive commercial futures in the long term, are the integrated circuit memories, beam access memories, both optical and electron beam, and travelling domain systems, in particular the bubble memory. It is most unlikely that one technology will dominate over the whole range of capacities and functions of memories used in computing systems. Also, they are not all at the same stage of development, so even in the commercial environment the choice is by no means clear cut. Table IX classifies the technologies in this way.

The limits of capacity given in the table are not to be regarded as completely restrictive. NASA may well need to go beyond the bounds set by commercial practice for a particular technology. Also, they may wish to accelerate the development of a technology which has commercial promise and offers to satisfy their system requirements.

Normally, there is a mismatch between the components, subsystems, and technologies available at any one time and the systems designed at that time. When a company wishes to design and produce a new system, they wish to produce the least expensive, most reliable system using well known and well tried subsystems and technology. This means that they are unlikely to use those components and subsystems which have been recently developed and are probably based on new technology. These new developments are not likely to be inexpensive, their reliability is uncertain and unknown, and their utilization in a system is untried. There is no pool of design experience and talent to draw upon to avoid many of the mistakes made in utilizing new technology. Also, by waiting a while and using these new developments in later systems, the system designer can take advantages of price reductions in the new components as the manufacturers learn more about the production techniques and the mechanisms which reduce yield are detected, analyzed, and corrected. At this stage in the development of the new component or subsystem, there is a pool of data on the reliability and the design procedures are better understood. Both these factors make its utilization in a system easier.

As far as the data processing industry is concerned, the memory is really a subsystem of a complete data processing system. So the utilization of new developments in memory technology is governed by the arguments given above. Obviously untried memory systems are available before their well tried versions appear, but this lag will not be short circuited by an experienced commercial systems house. Therefore, if NASA decides to adopt one technology at an early stage of development, they are likely to have to support the further development to turn it into a mature technology, as well as the specialized development to adapt the technology to space systems use. This is true, unless NASA's program schedule allows them to wait for continued development under normal commerical pressures.

Another factor which influences the speed with which commercial products are developed, especially from a new technology, is the ease with which the program is divided into steps and short-term targets are set. This makes financing of the program easier since less risk is associated with one decision. Also, if the end result of each step is in its turn a marketable item, then there is considerable incentive to pursue the overall objective through a sequence of limited goals. An example of this distinction is a comparison between the development programs for the bubble and the MNOS systems. The bubble development program can certainly be divided into a series of limited goals, but they are of varying importance, and each, individually, of little value. The major goal is to find a useable storage material. The MNOS development program offers financial return at the completion of each step. The small capacity, electrically alterable, read only memories being developed now will be of commercial value and are one step on the way towards achieving a large random access memory using large capacity IC's.

This contract was aimed at making recommendations for an all solid-state replacement of spaceborne tape recorders in the mid 1970's. Therefore, it is of interest to consider briefly the typical time schedule of a program prior to launch of the space vehicle. The first stages are the definition of the mission and its objectives. Then it is necessary to define the technologies available to the system designers (the stage of this contract). Having defined the goals and the available technologies, the hardware can be specified, developed, procured, tested, assembled, and further tested before launch. It may be necessary at several stages, especially in the early parts of the program, to define specific technological objectives to be achieved by definite target dates. To achieve these objectives, specific development programs may have to be supported. If the tape recorder is to be replaced in missions after 1975, then the technology which will replace it has to be definitely established by the end of 1973. By then, someone somewhere, must be capable of limited production of units and must be able to base their capability on more than a single laboratory example of a partially populated memory. This is not to say that the laboratory unit could not be developed into a useable system, but rather that the chances of successfully completing the job within the time available are less than for the better established technology.

For a 10^8 bit memory, prices below $0.01 per bit are almost mandatory. Predictions have been made that the bubble system and the beam access memories will be less expensive in the long term than other technologies. Sonic BORAM should also be an inexpensive technology, but here there is a possible trade-off since NASA may well have to fund the whole of the development work on this technology as there appears to be little commercial pressure to develop them. A spaceborne tape recorder costs about $50,000 today. This is after years of extensive development work.

Another possible trade-off is between the purchase cost of the equipment on a dollars per pound basis and the cost of the launch, which can also be reckoned on a dollars per pound basis. This trade-off is only useful if the cost per bit is below a certain level. Otherwise, it will tend to dominate regardless of changes in system weight.

III. RECOMMENDATIONS

The technology recommended as the most suitable for the replacement of spaceborne tape recorders in the mid 1970's is the moving magnetic domain shift register using "non-metallic" storage media. The first announcement of this technology was made by the Bell Telephone Laboratories. Memories based on this technology are frequently called "bubble" memories, a name coined by Bell workers to describe the appearance of the magnetic domains when viewed through a microscope. This chapter gives the evidence backing up the recommendation, along with comments on the likely development of the technology and its probable impact on commercial markets.

The moving magnetic domain shift registers based on "metallic" media are closely related to the bubble memories and also deserve consideration. They are discussed in this chapter as the main competing technology to the "bubble" technology. Another technology which deserves mention is the sonic BORAM memory. It has disadvantages compared to the magnetic shift registers but it could be developed into an all solid-state replacement of a spaceborne tape recorder if desired. The discussion of this technology is also included in this chapter.

The Bubble Technology

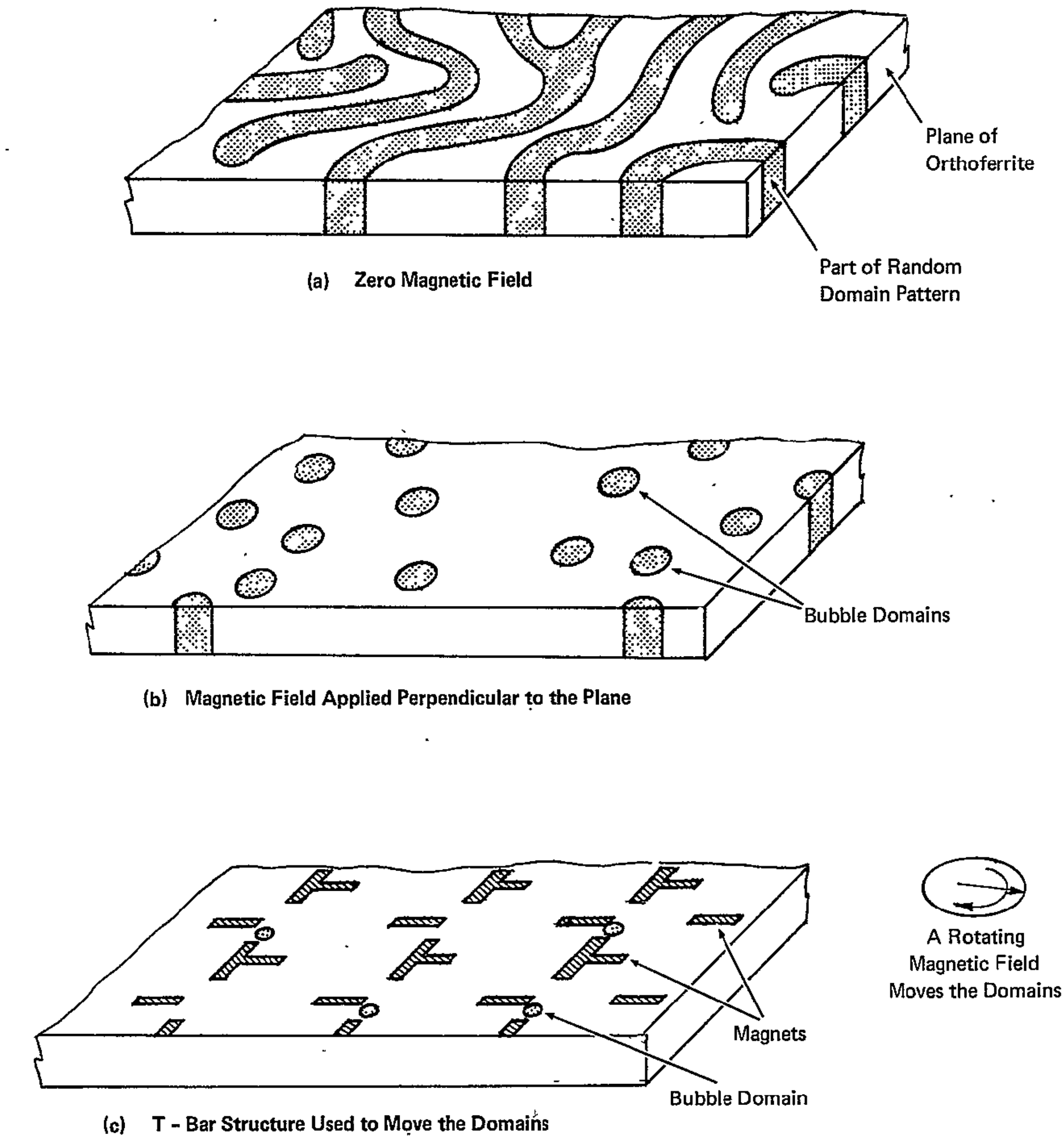
The trade-offs discussed in Chapter II led to the conclusion that a serial access memory which is non-volatile, has non-destructive readout capability, and can be arranged in blocks is the most attractive contender as a replacement for a spaceborne tape recorder. The magnetic shift registers have all these properties. When compared with the performance and characteristics of a tape recorder it became obvious that the shift registers compare favorably and can reasonably be recommended as a replacement for the tape recorders. During this comparison it also became obvious that the bubble shift registers have advantages over the metallic units, particularly those based on wire storage media, so the bubble technology is preferable over the other technologies.

Description of Bubble Technology -- Every magnetic material has a complex and, in general, unpredictable magnetic substructure. The substructure consists of an array of localized volumes of the material. Each volume acts like a small magnet pointing in a different direction from that of its neighbors. These discrete volumes within the bulk material are called domains. The size, shape, and magnetization of a domain depend on many physical, chemical, and mechanical factors, but in the case of certain garnets (general chemical formula RFe_5O_{12}, R is a rare-earth element) and orthoferrites (general formula $RFeO_3$) the domains can be produced in a reproducible manner and moved about the material in a controlled way. This is the basis for the bubble shift register.

Figure 4 shows schematically how the desired control is achieved. The domain structure of a thin plane of rare-earth orthoferrite in a zero applied magnetic field is shown in Figure 4a. The domains typically follow a snake-like pattern. The uniaxial anisotropy of the material keeps the magnetic moment perpendicular to the plane. By applying a magnetic field perpendicular to the plane, (Figure 4b), the domain structure can be modified. Increasing the field causes those domains with magnetization in an unfavorable direction to shrink. Eventually they collapse to cylinders before a further increase in field causes them to collapse entirely. The useful region occurs when the cylindrical domains are formed. These domains act like small magnets and can be moved about the surface of the material by the application of localized magnetic fields in the plane of the material. It is these domains which are called "bubbles" since, when observed through a microscope using polarized light, they look like bubbles moving around on the surface of the material. Information storage is based on the association of a "one" and a "zero" with the presence or the absence of a domain at any particular point. It is necessary to define the positions which must be sensed for the data and provide a driving mechanism. Figure 4c shows one solution to these problems which is described in more detail below. Figure 5 shows another drive mechanism which was considered.

The driving fields may come from a wire array carrying currents, or a magnetic array with the polarity of each magnet changed under the influence of a macroscopic (with respect to the array) magnetic field. The wires and magnets also specify the data positions. There are two interactions between the storage domains and the driving fields used to move the domains. One scheme, demonstrated most clearly in the orthoferrites, is to treat the domains as small permanent magnets of fixed size (the size is maintained by a bias field) and move them around by altering the local magnetic field distribution. To avoid domains coalescing, buffer positions are placed between the storage positions. The T-bar structure with an in-plane rotating magnetic field to drive the domains and a DC bias field to maintain them at a constant diameter is a convenient system (see Figure 4). It offers a good density of bits per unit area and avoids the problems associated with establishing a wire drive system for a large number of bits.

The other system, used mainly in metals but demonstrated in orthoferrites also (see Figure 5), induces the domain to grow so that it will occupy the neighboring site as well as its own site, and then reduces its size so that it only occupies the neighboring site. This requires directional control which can be achieved by a second wire array or a magnet array. The domain growth drive mechanism is more difficult to perform with orthoferrites than with



(a) Zero Magnetic Field

(b) Magnetic Field Applied Perpendicular to the Plane

(c) T - Bar Structure Used to Move the Domains

FIGURE 4 CONCEPTS IN A BUBBLE MEMORY

metals, because the domains do not grow equally in all directions in the plane. For this reason, the data tracks have to be bounded by magnetic walls to confine the bubbles (Figure 5). The triangularly shaped magnets (angel fish) in these tracks force the domains to move in one direction only. The data in a T-bar structure can be moved in both directions along the data track just by reversing the direction of rotation of the in-plane rotating field. It is not so simple to perform switching and logic functions in the angel fish structure as it is in the T-bar and wire systems.

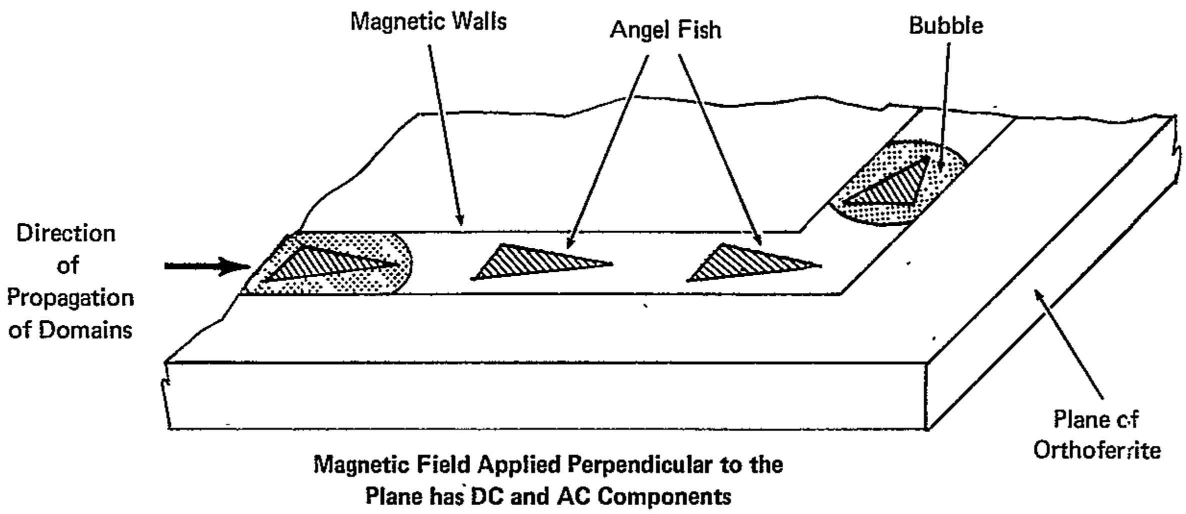


FIGURE 5 ANGEL-FISH DRIVE STRUCTURE

In practice, not every bit location is examined on readout. This would be possible but it represents a very inefficient use of the system. Certainly, for a tape recorder replacement, the serial arrangement where the data are stored in a block with only one input and one output is the best arrangement. There are two techniques for writing data. Both of them rely upon the division of a parent domain to write a "1" into the first storage cell. They differ only in the way that the parent domain is stored. In one technique, the parent domain rotates round a disk of permalloy under the influence of a rotating magnetic field in the plane, and the domains representing the data are torn off the parent domain by localized control fields. In the other technique, the parent domain is moved by currents in a wire array between a temporary storage location and a location where it is halved by a localized control field; the parent domain goes back to the temporary storage location, while the new domain goes to the first storage location and signifies a "1."

The readout can be done using magnetic induction techniques, a Hall effect detector, or an optical system. The two electronic techniques give small output signals, a few hundred microvolts; the optical scheme is bulky and inconvenient to apply.

If necessary, the domains can be removed from the material by a simple process which is the inverse of the rotating domain generator briefly described above. The bubble in the last storage cell is moved into the sphere of influence of a rotating domain and absorbed by that domain. Because the domain size is fixed by the magnitude of the DC bias field, the addition of new domains does not increase the size of the rotating domain.

Theory -- The theoretical description of the operation of bubble systems has been treated by Bobeck et al (Ref. 10) and Gianola et al (Ref. 11), among others. An examination of the theory points out the limitations on the bit density and defines the magnetic fields required. The theory defines a parameter ℓ as the ratio between the energy per unit area of a domain wall and the energy per unit volume of the domain. This parameter has the dimensions of length. The preferred thickness of the magnetic plate is 4ℓ, and at that thickness the domains are stable with a diameter of about 8ℓ. In fact, circular domains occur over a range of fields between H_1 (the first appearance of a circular domain) and H_2 (the field at which the domains collapse). The ratio H_2:H_1 is about 3:2. Put another way, the domain diameter is only stable over a field range equal to about 10% of the saturation magnetization, $4\pi M_s$. The bias field to maintain an 8ℓ diameter domain in a 4ℓ thick wafer is about $1.2\pi M_s$. In order to get a large bit packing density small diameter bubbles are needed. The bubble diameter is a function of the material chosen. Another factor which affects the bit packing density is the interaction between neighboring bubbles. The closest reasonable spacing is equal to three or four domain diameters.

The coercive force (H_c) for wall motion should be small, less than 0.5 oe, in order to allow small drive fields to move the domains through the material. If the drive fields are too large, then the domain size and shape are altered too much from their equilibrium values. Too much variation in the drive field may lose domains since one or more domains may not move forward because of the unwanted variation in the drive fields. To avoid this, the drive fields must be controlled to better than $\pm$ 7%. It is essential that the bias and drive fields do not induce the nucleation of unwanted domains or destroy wanted domains, but by keeping these fields down to a few oersteds these dangers are averted. In an ideal uniaxial crystal the nucleation field is equal to the anisotropy field, so, to avoid nucleation, the anisotropy field must be greater than $4\pi M_s$. If the inequality is just a few gauss, then the wall mobility is also optimized, which is desirable for a high data rate. The optimum value for $4\pi M_s$ is in the low hundreds of gauss. Table XIX summarizes the general materials parameters

TABLE XIX

GENERAL PROPERTIES OF ORTHOFERRITES

Formula $RFeO_3$, R is a rare-earth element

Orthorhombic crystal structure

Easy axis is the C-axis except in $SmFeO_3$

Saturation magnetization, $4\pi M_s$: 62 to 143 gauss

Domain wall energy, σ_w: $\sim$ 2 erg cm^{-2}

Coercive force, H_c: $\sim$ 0.1 oe

Domain nucleation threshold: $\sim$ 1000 oe

Neel temperature: $\sim$ 400°C

Domain wall velocity, v: $\sim$ 1000 cm s^{-1}

Domain wall mobility, μ: 150-800 cm s^{-1} oe^{-1}

$\ell = \sigma_w / 4\pi M_s^2$ $(3\ \mu m \lesssim \ell \lesssim 30\ \mu m)$

Ideal plate thickness, h: 4ℓ

Ideal bubble diameter, d: 8ℓ

Bias field: $\sim 0.3 \times 4\pi M_s$

Drive field gradient across domain $\Delta H > \frac{8H_c}{\pi}$

Domain wall velocity, $v = (1/2)\mu\Delta H$

Minimum stable domain spacing: 3d to 4d

for the orthoferrite class of materials.

Drive Structures -- The T-bar drive structure offers substantial advantages over the wire drive structure. The principal advantage is the improved reliability from not having to make numerous wiring connections. Other advantages are: (1) one drive circuit drives all the bits on a substrate simultaneously by means of the in-plane rotating field, and (2) there is no need to make a wiring pattern with very fine wires, about 0.1 mil in width, capable of carrying several hundred milliamps of drive current. There are disadvantages too. The T-bar structure is inherently slower than the wire structure. Data rates of over 10^6 bits per second have been achieved in $YFeO_3$ with a wire drive, but the best data rates, in a straight line, using a T-bar structure have been about 3×10^5 bits per second. The photolithographic techniques associated with making T-bar structures, with elements about 0.5 mil in dimension and spaced about 0.5 mil apart, for use with small diameter bubbles, are at the state of the art. The permalloy used to make the T-bar magnets is close to the zero magnetostrictive composition and is isotropic. The magnets are deposited in layers in a few thousand angstrom units thick. It is essential to get the permalloy in intimate contact with the surface of the storage material to reduce the reluctance in the path of the flux. This is facilitated by a well polished surface which is essential anyway to keep the walls from being trapped on surface defects. The polishing has to be done very carefully, or it will introduce defects and influence the domain wall coercivity through strains in the surface. The Syton polishing procedure used to prepare silicon wafers can be adapted for this purpose. The T-bars can be deposited on the material or on Mylar. The drive fields used are large enough to saturate the permalloy. The motion of the domain along the T-bar structure is not smooth. There are several places where the domain moves more quickly. Most notably, this occurs when the bubble is moving under the center of a cross-bar and when the trailing edge of a domain follows the leading edge across a gap. This irregular motion can cause trouble when the domain must turn a corner in the data path. In fact, the bubble may get trapped at the corner and move in a small circular path. Currently, 5×10^4 bits per second is the best speed attained for motion of data round a right angle bend in a T-bar data path. Part of the trouble is due to the changing magnetomotive forces along the track of the bubbles and part is due to the eddy currents generated in the permalloy magnets.

The in-plane drive field is created by two Helmholtz coil pairs placed orthogonally to each other. These coils are the main power drain in a memory system of this type. The magnetic field must be closely uniform over the storage medium and there must be no component perpendicular to the plane of the storage medium. To reduce the power requirements, it is attractive to use a drive frequency which causes a resonance between the coils and the supply. However, this means that only one narrow band of frequencies can be used for driving and the data rate is therefore synchronous. It is desirable to use asynchronous operation over a wide range of data rates so the extra power must be supplied to operate away from the resonant frequency of the coils. Fortunately, this is not a serious disadvantage at the relatively low data rates presently available in a T-bar structure. If it is desired to operate at data rates about 1 MHz and higher, then serious consideration must be given to the advantages of the resonant drive scheme.

The angel fish drive structure has not received the attention that the wire and T-bar structures have received. This is because of the inability to perform logic, the slow data rate, and the higher power consumption compared to the other drive system. However, the lack of logic capability is no difficulty for a simple buffer memory where a long average access time to data within a block is acceptable. By using multiple parallel channels, the data rate can be made higher. The higher power consumption is a drawback which more sophisticated drive circuit designs may overcome. More evidence is needed to establish the precise power consumption for this type of domain drive systems.

<u>Input</u> -- Current experience has not produced evidence to distinguish between the wire bubble generator and the rotating magnetic domain generator, A 500 mA pulse applied for 100 ns is required to divide the bubbles. The wire structure used will have to be very fine to deal with the fine bubbles, 0.1 mil to 0.3 mil diameter, needed for the highest bit densities. The rotating domain generator works in a straightforward manner. It requires a localized switching field to induce or prevent the bubble from being split off the rotating generator. This must be provided by a current in a properly placed wire loop. The timing of the pulse to generate data has quite wide tolerances since the rotating parent bubble need only be positioned to $\pm$ 50° degrees to produce the data bubble.

<u>Output</u> -- Of the various output techniques, the Hall effect sensor is the most compact. The Bell Telephone Laboratories have made a sensor using silicon which detects 5000 μV•μs pulses with a signal to noise ratio of 10:1 when measuring data at 57.3 kHz. Silicon was used for the detector because of the advanced state of the art in the manufacture of silicon devices. It offers the possibility of integrating a pre-amplifier with the Hall effect device to improve the signal to noise ratio. The device must be in close contact with the surface, carefully placed, and oriented with respect to the drive fields as modified by the T-bar structure so that the induced signals in the leads are minimized. One drawback of the Hall effect sensor is the occurrence of an offset voltage which may drift with time.

<u>Magnetic Fields</u> -- The magnetic fields required to operate the unit in the T-bar mode are a bias field, two pairs of Helmholtz coils driven in quadrature, the T-bar magnets placed on the surface

of the storage material, and localized fields at the input, output, and any switching positions. All these fields have to be precisely controlled in magnitude, homogeneity, and direction. To conserve power it is best to provide the DC bias field by means of a permanent magnet. The design of this magnet has to be carefully carried out because a homogeneous field is required over a volume of 1 to 2 cubic inches to make a module with a reasonable memory capacity. This implies large pole pieces since the ratio between the pole face diameter and their spacing has to be at least 3:1 to establish a homogeneous field. With a very high coercivity permanent magnet material, it should be possible to use a series of disc magnets stacked in a column with the planes of storage material placed between them so that several modules can be made in one compact unit. However, to increase the efficiency of the magnets and to reduce the stray fields (a disadvantage of the system is that it is not magnetically clean) it will be necessary to consider the provision of a closed flux path through a soft iron yoke. An alternative arrangement for a group of modules would be to arrange them around the yoke with pole pieces on radial arms at the top and bottom. This is not such an attractive arrangement because of the difficulties associated with the suitable placement of the Helmholtz pairs for the drive fields. A memory with 10 modules, each module having about 1 cubic inch of storage medium will require 11 disc magnets with a volume of about 1 cubic inch for each disc. The flux return path will be about 10 inches long. Therefore, the permanent magnet structure requires about 20 cubic inches of material and weighs about 6 pounds. These figures depend on the precise nature of the materials chosen for the magnet structure. The whole design can be integrated so that the various members of the permanent magnet structure also act as support structures for other elements in the system. It may be possible to combine the return flux path with the magnetic shielding which is necessary for the system. This could be done in the most elementary fashion by making the yoke like a cylinder with the modules inside.

The drive coils must provide fields which are accurately in the plane of the storage medium. They must also be homogeneous over this plane. For any one module, the radius and spacing of the coils will have to be about 3 inches to achieve the desired homogeneity. The provision of suitable coils in a convenient arrangement for a set of modules is a more difficult problem. It may well be that the best approach is to make each module in a package independent of the others. In this case the volume of each package is fixed by the area and spacing of the Helmholtz coils. The weight of each package is determined by the amount of magnetic material it contains. The number of turns in each coil and the current flowing through it must be determined with reference to the design of the power supply.

The permalloy T-bar magnets must be accurately located and in intimate contact with the storage medium. To avoid possible damage the permalloy must have zero magnetostriction, and to respond uniformly to the fields in each direction it should be isotropic. By making the permalloy in thin layers the eddy currents are reduced but, at the same time, the reluctance is increased. There is, therefore, an optimum thickness for the permalloy.

To reduce the difficulties associated with the photolithography of very fine wires, it is essential to design the input and output circuits and the switching circuits, so that the location, length, and tolerances required are all optimized. This implies keeping all the wiring to one small area; for example, down one side of the storage plane.

Performance Matrix -- In this section, two performance matrices are given, one for a $Sm_{0.55}Tb_{0.45}FeO_3$ system and one for a garnet system, such as $TbEr_2Al_{1.1}Fe_{3.9}O_{12}$. As far as possible the performance matrices are based on performance figures already achieved, not on future predictions. The major assumption made is that sufficient magnetic material is available to make the system. Apart from this problem, the two main production difficulties are obtaining the right thickness of magnetic material and making the drive pattern using photolithographic techniques.

Table XX gives the predicted performance matrix for the orthoferrite assuming a plate thickness of 0.5 mil and a bubble diameter of 1 mil. It is best to attempt epitaxial growth techniques to achieve this thickness. The bubble diameter means that the T-bar structure must repeat at 3 mil intervals, which is feasible to make, using photolithographic techniques. The bit density along the direction of the data flow is 330 bits $in.^{-1}$, while at right angles to the direction of data flow it is about one-half that. This is because experimental work shows that the bar magnet structure has to be lengthened somewhat to prevent bubbles escaping from the track. As a result, the bit density is about 5×10^4 bits $in.^{-2}$ This base figure, together with an estimate that 20 planes per inch can be stacked, allows estimates to be made about the volume and weight of the system and so the performance matrix can be established.

It is assumed that the data rate per channel is less than 5×10^4 bits s^{-1}. A series-to-parallel shift register is needed at the input and output to accommodate the parallel storage mode of the memory. The power consumption is a function of frequency. The energy dissipated in the storage medium is about 10^{-13} J per bit per step. For a 10^8 bit memory, with 5×10^7 "1's" stored, operating at 5×10^4 steps per second, there is a dissipation in the storage medium of 250 mW. The major component of the power dissipation in the system is in the Helmholtz coils used to drive the data through the memory. The write mechanism requires pulses of several hundred mA's, but at a low duty cycle. The memory can be divided into blocks 50,000 bits long, so that a plane of storage material 1 by 1 inch contains one block. A module with 10 blocks capable of operating in parallel can be made by stacking 10 storage

TABLE XX

PERFORMANCE MATRIX OF A BUBBLE MEMORY USING $Sm_{0.55}Tb_{0.45}FeO_3$

Performance		Capacity (bits) 10^8	Data Transfer Rate (bits s^{-1}) 5×10^5
Weight (lb)	200	5×10^5	2.5×10^3
Volume (in.^{3})	3000	3.3×10^4	1.7×10^2
Energy/bit (J)	5×10^{-5}	2×10^{12}	10^{10}

planes one above the other. Each module has 10 input/output pairs, one pair per plane, so there are 2000 input/output pairs in the whole memory. Although arrangements could be made to operate all 200 modules simultaneously, this is unlikely to be needed. In fact, it is assumed here that only one module at a time is used, with power switching between modules. The extension to pairs or larger groups of modules is obvious. The output, if it is a Hall effect device, requires only a few mW power. The shift registers at the input and output use less than 1 watt each. The total power consumption is approximately 25 watts.

Table XXI is a performance matrix for the garnet. In this case the minimum domain diameter is much less than that for the orthoferrite, about 0.1 mil. This implies that stable operation can be achieved with a plate thickness of 0.1 mil and a bubble diameter close to 0.2 mil. In this case, the use of epitaxially grown material is essential because the effort, cost, and low yield associated with the grinding and polishing of plates that thin are prohibitive. A 0.2 mil diameter bubble requires T-bar magnets placed on 0.6 mil centers. The photolithography for this size structure is at the peak of the art. Increasing the thickness of the plate does increase the useable bubble size, but only very slowly, and there are severe limits. Doubling the plate thickness to 0.2 mil (it is still necessary to prepare the plate using epitaxial processes) increases the stable bubble diameter to between 0.25 and 0.3 mil. This changes the T-bar spacing to 0.75 to 0.9 mil which is a slight easing of the photolithography problems. Unfortunately, the larger sized bubble is stable over a more restricted range of bias fields. Even if this is allowed for in the design of the electronics, further increases in plate thickness impose even tighter constraints on the bias. Eventually, a plate thickness is reached at which major deviations from the cylindrical domain structure occur.

The figures in Table XXI are based on 0.3 mil diameter bubbles in a 0.2 mil thick plate. The bias field will be in the range 55 to 75 oersted, and a drive field of about 30 oersted will be required. The bit density for bubbles of this size is close to 6×10^5 bits in^{-2}. Therefore, one module containing 10 planes will have a capacity of 6×10^6 bits and 16 modules will supply a 96×10^6 bit memory. In this case it is better to make each block 6×10^4 bits long so that one plane with 10 input/output pairs can handle 10 bit characters in parallel. The data rate and power consumption are approximately the same as in the orthoferrite case. On the other hand, the volume and weight are considerably reduced. The sixteen modules can be stacked in 2 units instead of 20 as in the orthoferrite case. It is clear that the order of magnitude increase in bit packing density has made a significant difference in the approximate size and weight of the memory.

<u>Environmental Check List</u> -- This type of memory has excellent resistance to vibration, shock, and radiation. The mean time between

TABLE XXI

PERFORMANCE MATRIX OF A BUBBLE MEMORY USING $TbEr_2Al_{1.1}Fe_{3.9}O_{12}$

Performance Value		Capacity (bits) 9.6×10^7	Data Transfer Rate (bits s^{-1}) 5×10^5
Weight (lb)	20	4.8×10^6	2.5×10^4
Volume (in.^{3})	300	3.2×10^5	1.7×10^2
Energy/bit (J)	5×10^{-5}	1.9×10^{12}	10^{10}

failure (MTBF) estimated from a preliminary component count is about two years. The limiting factor is the number of components in the circuits associated with the memory.

The bubble memory is an all solid-state system and so has good reliability because of the few interconnections and the integrated structure. Shock and vibration do not affect the operation of the shift register as long as the magnetic material has zero, or almost zero, magnetostriction. However, the mechanical structure supporting the permanent magnets, Helmholtz coils, and magnetic storage planes must be quite rigid or vibrations will cause variations in the magnetic field strengths which may go outside the stability range locally.

Although the storage medium is not affected by radiation until very high radiation levels are reached, the circuits are much more sensitive to radiation. Because it is possible to have a large block length and to operate in a serial mode, there are less electronic components needed for this memory than for a random access memory or a serial memory with shorter blocks. This means that the probability of surviving irradiation is improved for the auxiliary circuits associated with the bubble memory.

The response of this type of memory to temperature changes is poor. The $Sm_{0.55}Tb_{0.45}FeO_3$ material, in particular, is very poor in this respect. Some of the garnets are reported to be better because of their higher transition temperatures. Even so, it appears that the temperature must be limited to a 20°C range to ensure successful operation and that it must not be allowed above a certain critical value during storage because the bubbles then collapse. For the samarium terbium ferrite this limiting temperature is about 40°C. There are no data currently available for the garnets. Table XXII summarizes the response of the bubble memory to the environment.

Problems — There are at present several problem areas which require detailed consideration and satisfactory solutions before the technology can demonstrate its real potential. The most pressing problem is the provision of a suitable storage medium. None of the materials which demonstrate bubble domains has been produced in large quantities of good quality. In fact, the largest areas of orthoferrite suitable for this memory have been only a few tenths of an inch on a side. This, combined with the fact that the obtainable bit packing density in an orthoferrite is only about 50,000 bits $in.^{-2}$, makes it essential to search for other materials if a large economical unit is required.

At present, the orthoferrites are grown from a lead salt flux, and the resulting single crystals are small and have flux inclusions in them. Attempts to grow larger crystals using other techniques have been hindered by the morphology of the crystals grown. It is possible to grow quite large crystals in one dimension,

TABLE XXII

ENVIRONMENTAL CHECK LIST

Bubble Memories

Response to temperature changes	Poor
Response to shock	Good
Response to vibration	Good
Response to radiation	Good
Mean time between failures (predicted)	$\sim$ 15,000 hours

but unfortunately the crystal orientation is such that the small dimension is the one which determines the size of plate which can be cut from the crystal. A possible improvement is to use a thermal etch at regular intervals during the growth. This etch sequence removes some of the material grown in the previous growth sequence. This is done in an attempt to keep the major dimensions of the growing crystal approximately equal. The by-product of this technique is the lengthy growth period required to produce a sizeable crystal.

Extensive efforts are being expended to overcome this problem. The search for reasonable materials has moved to other families, for example the garnets. These also have preparation problems, but there is considerable experience in the growth of garnets for other applications. Since garnets are basically cubic in structure, great care has to be taken to cut the crystal correctly to get planes of material showing a suitable uniaxial magnetic anisotropy over the plane. The garnets have some definite advantages over the orthoferrites, notably a smaller stable domain size, combined with a reasonable mobility, and a better response to cutting and polishing, probably because the magnetostrictive effects can be reduced to a minimum.

It is unlikely that one magnetic material will sweep the field for bubble devices in the manner that silicon has done in the integrated circuit industry. There will be materials which have high data rates, materials which have a high bit density, and materials intermediate between the two. The search is still on, but sufficient information is available today about the existing materials to allow reasonable system predictions to be made.

At the present state of technology it is essential to use a plate of single crystal material because the constant direction of the uniaxial anisotropy demonstrated in single crystal material is essential to the formation of regular arrays of bubble domains. It also is essential to have a new perfect single crystal which does not have low angle grain boundaries, twin boundaries, and cracks. All these features prevent the motion of the domains. The adverse influence of surface strains and other local features on the coercive force has already been mentioned.

Considerable efforts are being expended to grow suitable storage materials by epitaxial processes. This technique has been used to grow films of garnet for some years. There are severe requirements on the substrate because it must be at an elevated temperature in a very corrosive atmosphere. It must be chemically inert, have a crystal structure, lattice constant, and coefficient of expansion compatible with the material to be grown. The epitaxial layer must be very uniform in its properties to make a good magnetic storage medium. It is important to minimize the coercive force. Spinel ferrites grown on a magnesia substrate can have $H_c < 0.25$ oersted. The early experiments with garnets, particularly yttrium iron garnet, produced films with a coercive force less than 1 oersted. A big advantage of epitaxy is the ease with which thin films can be formed; thicknesses between a fraction of a micron and 50 microns are readily made. These dimensions are appropriate for the small diameter bubbles needed for large bit densities. They are also more conveniently achieved using epitaxy than by cutting and polishing a crystal. The present state of the art in the epitaxial growth of bubble domain materials is not so advanced as the state of the art in the growth of single crystals. One other possible advantage of epitaxial materials over single crystals, which apparently has not been investigated as yet, is the ability to deposit epitaxial films in patterns so that tracks for the bubbles may be defined by the geometry of the film.

A second serious problem associated with the bubble technology is the temperature sensitivity of the systems. The whole operation of the memory depends on a known and fixed ratio between the diamete of the domain and the spacing of the bit storage cells. The domain diameter depends on the applied magnetic fields, the local arrangement of imperfections, and the temperature. The bias field and the drive field must be constant, both in magnitude and direction, to within a few percent. By careful mechanical and electrical design this can be achieved. The local arrangement of imperfections around each storage cell is not within the control of the system manufacturer, except insofar as he is able to use a perfect material The temperature effects are quite serious in some of the materials examined. The domain diameter can change by 2-3% $degC^{-1}$ in some orthoferrites, e.g., $Sm_{0.55}Tb_{0.45}FeO_3$. Other materials are somewhat better and a claim has been made that YIG (yttrium iron garnet) is very good from this point of view.

There are three possible solutions to this problem. They are: 1) find a material which has a much higher magnetic transition temperature and therefore less sensitivity to temperature changes; 2) operate the unit in a constant temperature environment; and 3) provide temperature compensation circuits. Successfully achieving the first alternative is obviously not to be relied upon. The second alternative is certainly feasible, but it requires space and weight. The third alternative could be partially achieved by having a compensation field applied parallel to the DC bias field. The compensation field can be derived from a pair of Helmholtz coils fed by a current from a temperature controlled feedback loop. The application of a temperature correction to the bias field may also cause other problems. The range of stable domain diameters also changes with temperature, so maintaining a fixed domain diameter as the temperature changes may move it out of the range of stability. Whichever technique is adopted, it is important to use the material least sensitive to temperature changes. There is an upper limit to the temperature at which a bubble memory can be stored because all the bubbles collapse and disappear at that temperature. This means that the data stored are lost since there is no guarantee that new bubble domains will appear where the old ones were.

The domain wall mobility also varies with temperature, by about 0.5% $degC^{-1}$ in some orthoferrites. This is more readily coped with, since all that the designer need do is maintain a minimum drive field level capable of providing the proper operation for the lowest mobility value within the range of temperatures expected. The upper limit to the drive field is set by the tendency of the drive field to distort and destroy the bubbles. There is no need to worry about possible canting of the domain magnetization away from the vertical because, in most materials suitable for bubble memories, the in-plane field needed is several thousand oersteds. The temperature range for storage of the device is not limited by mobility changes.

The data rate is determined mainly by the mobility μ of the domains in the material and the magnitude of the drive field. The mobility is inversely proportional to the anisotropy coefficient of the material, so a low anisotropy coefficient is desirable. It cannot be too small, because then the uniaxial anisotropy is weakened. The domains move under the influence of a gradient in the field and their velocity is given by:

$$V = (1/2)\mu\Delta H,$$

where ΔH is the decrease in the field across the domain. To move the domain, ΔH must be larger than $8 H_c/\pi$, where H_c is the domain wall coercivity. This is the reason for requiring a very low coercivity material. The lower the value of H_c, the smaller the drive fields required and the more readily they are produced. Drive fields of about 20 oersted are normally used. It is very important to have the T-bar magnets in intimate contact with the surface of the storage medium so that as much as possible of the drive field is concentrated into the critical area containing the domains. Domain velocities up to 2000 cm s^{-1} have been attained in garnets. The data rate is determined by the time taken for the domain to move between two storage cells. The spacing between storage cells depends on the domain diameter, so the data rate is linked closely to the basic material parameters. Increasing the drive fields increases the domain velocity to a certain extent; however, it is not always feasible to increase the drive field because of the domain distortions which occur, or because of limitations on the drive power available. Some materials, notably the barium ferrites, have a fundamental limit on the domain wall velocity of 600 cm s^{-1}. The magnetoplumbites also have limiting velocities in the low hundreds of cm s^{-1}.

The apparent limit on the data rate set by the corners in a T-bar track is not fundamental. A modified geometry for the corner will undoubtedly allow faster data rates around the corners. In any case, the 50 kHz limit mentioned above applies only to the motion of a sequence of bits in one channel. The data rate can be arbitrarily increased to 500 kHz by using 10 parallel channels. In this case, a timing channel, with facilities for clocking against this channel, is essential to aid deskewing on the readout. This timing channel can also be utilized to save data when the power is turned on and off.

A wide range of materials has been studied with stable domain diameters between 0.1 and several mils. Although the smallest diameter domains imply the best bit packing density, the problems associated with manufacturing the drive circuits on the plane must be considered. For a wire drive system the dimension of each wire must be a fraction of the diameter of the bubble. This leads to difficulties from both the photolithography and the limit on allowable drive currents. The present state of the art does not extend to placing 30 μin. lines on 100 μin. centers.

The permalloy T-bar magnets usually have a width about equal to the domain diameter and a length about three times their width. For 0.1 mil diameter bubbles this implies depositing permalloy in 0.1 mil widths. This is closer to today's technology in photolithography. However, it is certainly wise to back away from these limits by a factor of 3 or 4. This still leads to a bit density of several hundred thousand bits $in.^{-2}$ if a suitable material is available.

The signal-to-noise ratio is always an important factor. One of the disadvantages of magnetic shift registers is the poor output they give. The typical magnetic induction output takes an abnormally large area of the substrate and requires very fine wiring if small domains are used. This requires very accurate photolithography. The optical readout systems take up a large volume, compared to the volume of the storage material. They also need very accurate alignment. The Hall effect sensors appear to be the best way to go at present, but they have difficulties associated with sensitivity, induced voltages in the leads, offset voltages and precise location in contact with the output position. The small drive currents, 5 to 10 mA, in the Hall sensor do not affect the drive fields which move the domains.

<u>Discussion</u> -- The bubble memory is very attractive in many respects, but the problem of a suitable material is very important. It should have a bubble diameter in the 0.3 to 0.6 mil range, because these diameters lead to a good bit packing density and the associated drive circuits can be built. It is necessary to be able to get plates of material a few tenths of a mil thick, and also the material must be shielded from temperature changes.

The angel fish domain propagation scheme (Figure 3), deserves more attention. One advantage of this drive mechanism is the elimination of the two pairs of Helmholtz coils which must be accurately aligned to give the in-plane, rotating drive field. In their place is one pair of Helmholtz drive coils which provide a field parallel to the DC bias field. It is the large inductance of these coils which makes the power supply problem more severe.

The most important features of the further development of the bubble memory, as far as NASA is concerned, are the improvement in quality of the storage materials, the introduction of epitaxial growth techniques capable of producing materials with a low coercive force; the announcement of a material with a good temperature range; and continuing developments in photolithography. Epitaxially grown garnets seem attractive at the moment and deserve support. If the temperature problem cannot be solved at the materials end, an analysis of the type of constant temperature chamber needed to control temperatures will be required. Passive thermal control has reached the stage where very accurate temperature regulation can be maintained. For example, the retroflector placed on the moon for the laser experiments is maintained at $\pm$ 0.5°C during the severe diurnal temperature variations found on the lunar surface. Obviously, the constant temperature chamber is going to add to the size and weight of the memory. Table XXIII summarizes the main advantages, disadvantages and engineering problems associated with a bubble memory.

It is important that a detailed design analysis of a bubble domain shift register be performed quickly. This analysis, which can be based on presently available data, will establish the size and weight of the individual system components more precisely, their location within the system, the power consumption, the operational tolerances, including magnitude and direction of magnet fields, plate thickness, resistance to temperature changes, amplitudes of drive fields, range of stable bubble diameters, precision of the photolithography required, design of suitable electronics, the best magnet configuration, and the best way to maintain the unit within a fixed temperature range. During this analysis, a detailed comparison between the T-bar drive scheme and the angel fish drive scheme must be made, so that the final design combines the optimum performance with the most simply attained structure. The preliminary analysis made during the trade-off studies in this contract indicates clearly that there is no need to pursue the development of materials beyond the provision of a supply of adequate material. Increasing the bit density to millions of bits per square inch and the data rate to millions of bits per second adds nothing to the system from NASA's viewpoint. On the contrary, the successful achievement of these aims in a production unit adds unnecessary complexities to the equipment and the production process. A satisfactory system can be based on a data rate of 50 kHz in each channel and a bit density of 500,000 bits in^{-2}.

The further development of this technology will require a large scale effort. There is considerable commercial interest in the technology and the current level of effort in developing this technology is estimated to be equivalent to 200 man-years per year among several firms. Bell Telephone Laboratories, Autonetics, and IBM are known to be working in the area and several other companies are believed to be working in the area. This level of effort must be maintained over the next few years to achieve the goal of a replacement for a spaceborne tape recorder.

TABLE XXIII

SUMMARY OF THE CHARACTERISTICS OF A BUBBLE MEMORY

Advantages	Disadvantages	Specific Engineering Problems
Good bit density	Supply of suitable material	Preparing plates of material
Adequate data rate	Temperature sensitivity	Manufacturing the drive structure
Few wire interconnections		Maintaining thermal equilibrium
Non-volatile		Optimizing signal-to-noise ratio
Non-destructive readout Serial operation		Maximizing the data rate along a complex data channel
Low power consumption Possibility of logic operations		Provision of suitable magnetic fields
Negligible standby power		Packaging the memory
Resistant to radiation		
Resistant to shock and vibration		
Light weight		

The level of effort required to produce a system specifically for space applications is difficult to assess. The next step in the development of a spaceborne memory is to create and analyze a detailed design. This analysis should specify closely the type of material required and in what quantities. This information can then be correlated closely with existing materials and the best chosen for a modified design; the process can be repeated until the optimum, practical solution is achieved. This process will probably require one man-year of effort. The continuation from this stage through prototype and final product will depend to a large extent on the availability of the materials at that stage. If one of the garnets can be used, either with or without a temperature controller, this is an advantage. Otherwise, it will be necessary to finance more materials research. The cost of developing a prototype model, given a material, will be of the order of $300,000; this is about $0.003 per bit. This, of course, is much more expensive than the predicted cost of a production unit. On the basis of cost experience gained from the manufacture of ferrites for microwave devices and the experience of costing in the integrated circuit industry, it appears that a large store can be built at a cost of about $0.00003 per bit. As experience is gained this cost will decrease.

The most obvious commercial use for the system is as a serial memory. Currently used serial memories include discs, drums, and tapes employed as backup stores for data processing systems, data acquisition systems, instrumentation, etc.. The properties of the bubble memory approximate those of the disc and drum more closely than those of tape. Since the bubble memory has no moving parts, the average access time depends only on the length of the shift register and the data rate. Other uses are as a buffer store or a shift register. Since it should be possible to perform logic functions also, devices such as first-in first-out registers and associative memories have been suggested. It will be some time before this technology appears on the commercial market, since suitable materials must be developed before a useful system can be evaluated and its reliability tested. Then a commitment must be made to use this type of system in a data processing unit; the commitment will be followed by the two or three-year time lag associated with product development. We, therefore, believe it will be at least five years before bubble memories enter commercial markets. The competitive techniques facing this memory system toward the end of the 1970's will include disc, drum, and magnetic tape systems, and new systems available by then, such as large MOS shift registers, metallic magnetic shift registers, and large systems based upon optical technology. These all offer a serial or a block organization. The bubble memory will be available with varying data rates and bit capacities and perhaps with a removable storage medium (this is still to be demonstrated). Therefore, this new development will compete more directly with the disc and the drum than with any other system. Although one could consider making this device as a direct replacement for disc and drum stores and attempt to enter a retrofit-type market, this approach is not likely to occur. The bubble memory is much more likely to broaden the range of desirable products than to replace other products. Since the data processing market is still increasing rapidly, there is likely to be room for all the devices for many years.

These memories may also find use with small computers or even desk calculators. Since even the crudest estimates predict that the bubble memory will have a very large number of bits per unit volume, operate at a reasonable data rate, and consume very little power, it should be compatible in size, weight, and power with the overall system. It will give the small computer some of the operating modes of a much larger computer backed up by drums, discs, and tape. It appears that a bubble memory in this application would be cost-competitive with its competitors. The major competitor is likely to be the cassette tape recorder currently being developed for data processing applications. Such recorders have removable storage media, but a removable media bubble memory may be developed. Also, as the bubble memory is all solid-state, it should be more reliable than the tape recorder.

The bubble memory should also find applications in other types of data processing systems such as communication terminals, process control computers, and terminals, process control computers, and terminal points for a time-shared system. The introduction of the bubble memory will revive several old ideas of computer architecture and stimulate many new ideas. The possibility of performing logic and storing data on one substrate is very attractive and will stimulate much thought on new systems.

The Bell System can see several possible applications for the bubble memory in its own network. The electronic switching systems currently used require extensive and bulky storage capacity. Substituting a bubble memory for the memories now used will improve reliability and improve utilization of company real estate. At the other extreme, the high bit density and low power available in a bubble system will allow Bell to develop small memories for use at other points in the telephone system. A store of frequently used telephone numbers for each subscriber is one example.

The main differences between the system recommended for NASA and a commercial system are the bit density, data rate, and system organization. To achieve economies in the production, the maximum bit density is required. The cost of the processing steps on the storage medium is not strongly dependent on the size of the memory, so the more bits processed together the better. There is a slight dependency on area, since the larger the bit density, the more critical the processing steps become and the lower the yield, thus, increasing costs. Many commercial applications will need the fastest data rates available to match the increase in data processing speeds. It is unlikely that many commercial users will find a use for a memory with data in blocks of 50,000 bits or more. Therefore, the system organization will utilize much smaller block lengths. This implies a shorter average access time. However, advantage can be taken of the ease of performing switching of trains of data in a bubble memory and other organizations adopted which reduce the access time still further. One approach, suggested by Bell, is to have one input/output pair connected with several storage loops by means of a communicator loop. In this way, the length of the block is divided by the number of loops without having to increase the number of input/output pairs. This system requires switches between the communicator loop and the storage loops which can be provided by special high permeability magnets activated by localized drive currents. Since the switches will be distributed over the storage plane, this implies an extensive wiring pattern which will be difficult to achieve with small diameter bubbles.

It cannot be emphasized too strongly that the requirements for a replacement for a spaceborne tape recorder and the requirements for a commercial memory are different. In fact, the replacement for a tape recorder is a simpler system and for this reason it is possible to talk of using materials with slow data rates and bit densities of several hundred thousand per square inch. Such materials would not be acceptable in commercial units. Also, it is possible to give serious consideration to features such as the angel fish drive structure for use in a replacement for a tape recorder, even though, it is inadequate for commercial systems.

Metallic Magnetic Shift Registers

There are several types of metallic magnetic shift registers. The two systems which have reached the greatest development are based on: (1) the controlled motion of domains on a plane surface, and (2) the motion of domains along a magnetic wire around a cylinder which carries the drive wires. A third possible configuration is to drive domains along strips of magnetic material, but this has not often been used. The technique where domains are moved on a two-dimensional plane is called domain tip propagation logic (DTPL), while the wire technology is probably best distinguished by the trade name Dynabit given it by Hughes.

DTPL -- Several companies have worked, or are working, on DTPL. Although no products are available yet, it is now quite a mature technology and product announcements can be expected soon. The magnetic shift register based on the wire constrains the domains to move along one track by imposing geometrical boundaries. The magnetic shift register based on a planar thin film requires some other means of controlling the motion of the domains. The simplest way is to etch out a track, but another technique commonly used is to make the planar thin film out of two components, one magnetically hard, one magnetically soft, so that the domains move along a track of magnetically soft material bordered by the hard material. It is still necessary to ensure that the domains move in the correct direction; this is done by using three or four-phase driving fields or by using a two-phase scheme with a "diode" structure built into the track. Typically, this diode structure consists of a neck in the track which allows the domain to grow through more readily in one direction than the other.

The main disadvantages of this unit are poor linear bit density, poor output signal, and the need for acceptable drive and nucleation thresholds. The bubble system has a ratio between the nucleation and drive fields of about 1000:1, but in the DTPL system this ratio is usually only 2 or 3:1, which means that much tighter control must be exercised on the driving fields. The bubble system cannot utilize the whole of the 1000:1 ratio because of the limitations set on domain stability. The DTPL system has the advantage of not needing a permanent bias field like the bubble memory. Also, there is no need for Helmholtz coils to supply high homogeneity in the magnetic field.

The two component magnetic structure has other difficulties. The continuous switching in the soft material eventually demagnetizes the adjacent hard material, especially in places where the hard material is particularly exposed to the surrounding domain tracks.

The power requirements can be reduced by more careful packaging, a better field/current ratio, or a slower data rate. The growth and inhibit fields which help move the domains can be supplied as macroscopic fields over the whole area of the register or as local fields. The latter approach requires a lot of wiring and current switching. However, since it is necessary to have at least one of these fields supplied at the level of individual data positions, some wiring array is needed.

The performance matrix is given in Table XXIV. It is based on a module with an 8 million bit capacity, each module occupying about 600 cubic inches and weighing about 25 pounds. The data are arranged in blocks 1000 bits long, and the data rate in each block is less than 10 kHz. This requires a parallel organization with several bits per character so that data rates up to several hundred kHz can be accommodated. For a 500 kHz operation, 50 bit characters are needed. A series-parallel shift register is required at each input and output.

Alternatively, advantage can be taken of the multiphase drive to multiplex information into the storage registers. This reduces the length of the series-parallel resisters needed. Twelve modules give a 96 million bit memory. Since the memory is non-volatile, power switching between modules can be used. This reduces the power consumption to that of only one module. This is about 5 to 10 W at the 10 kHz data rate in each channel. The output signal is about 1 mV, but by careful positioning of the output loop, the output pulse can be adjusted to occur midway between the noise pulses induced by the drive pulses. This technology responds very

TABLE XXIV

PERFORMANCE MATRIX FOR A DTPL MEMORY

Performance Value		Capacity (bits) 9.6×10^7	Data Transfer Rate (bits s^{-1}) 5×10^5
Weight (lb)	300*	3.2×10^5	1.7×10^3
Volume (in.^{3})	7200*	1.3×10^4	7×10
Energy/bit (J)	2×10^{-5}	4.8×10^{12}	2.5×10^{10}

*Technical advances should reduce these values by 4 x before 1975.

ENVIRONMENTAL CHECK LIST FOR A DTPL MEMORY

Response to temperature changes	Good
Response to shock	Good
Response to vibration	Good
Response to radiation	Good
Mean time between failures (predicted)	$\sim 10^4$ hours

well to changes in environment, including temperature. The coercive force, which is an important parameter determining the drive requirements, varies by about 10^{-2} oe $degC^{-1}$ for typical magnetic thin films. The qualitative response to the environment is also given in Table XXIV.

There are more interconnections in a DTPL unit than in a bubble unit because of (1) the shorter block length, (which means more input/output pairs) and (2) the wire drive system used. For this reason, the predicted mean time between failure of one year for a DTPL memory is shorter than for a bubble memory.

The performance matrix is given in terms of today's technology. The bit density is expected to increase from about 10^4 bits in.$^{-3}$ to 4 x 10^4 bits in.$^{-3}$ in the future, with a consequent reduction in overall volume and weight. Also, the same increase in a bit density will enable a longer block to be made with perhaps 8000 bits per input/output pair. This will help reduce the overall size and weight and also the power requirements. Furthermore, it will increase the MTBF somewhat.

This technology obviously deserves attention. It is closer to attaining the parameters discussed than the bubble, but the bubble has considerable economic incentives to reach its goals, and when attained, the memory will be much closer to the size, weight and power consumption of existing spaceborne tape recorders.

Dynabit

The Dynabit system, as developed by Hughes, uses a 0.3 mil diameter magnetic wire to carry the domains. In principle, this technique is the simplest magnetic shift register. This is a one-dimensional problem and the only requirement is to create, drive, and sense the domains. However, there are many problems. The preparation and mounting of a suitable wire is not easy. The wire must have suitable magnetic properties with a good ratio between the drive threshold and the nucleation threshold for domains. The strains induced during handling must not harm the wire properties. The wire must be wrapped carefully around a former carrying the sense and drive circuitry. Uniform properties must be maintained along the wire. The whole assembly must have a good yield. A small tension along the wire gives the correct easy-axis orientation longitudinally along the wire. Careful annealing has to be performed to make a uniform wire before it is wrapped around a former carrying the drive wires. Typically, currents up to 2 A are needed to drive the domains and relays are required to switch the current. The pulse rise times are about 300 ns and the self-inductance of the drive lines a few μH, so the back emf reaches several tens of volts. This means that integrated circuits cannot be used as drivers. The data rate is controlled by the need to accelerate and brake the domain walls and so it is not likely to exceed a few hundred kHz. The output is taken from a sense winding at one end of the former, while the write is done by a simple ferromagnetic pin with a small winding placed at the other end of the former.

A typical system is organized into blocks of eight storage lines on one former so that one set of drive wires drives eight bits in parallel. A block length of 3000 to 4000 bits requires 20 to 30 feet of wire wrapped round the former since the linear bit density is low. The formers can be arranged into any suitable matrix; 1024 holders in a 32 x 32 matrix gives a memory with a capacity near 30 million bits.

The main disadvantages of the system are the low linear bit density, 10 bits in.$^{-1}$, large driving currents, difficulty of reducing stray couplings, low signal output and the need for an adequate ratio between the nucleation and drive thresholds. This latter is made more important by the difficulty of maintaining close tolerances on the windings, in particular, the storage-winding drive-winding arrangement.

The Dynabit memory is not suitable for spaceborne units because the volume of a 32 million bit unit is about 10 cubic feet and the weight several hundred pounds. There is little hope that these figures can be improved by even a factor of 2 in the near future. Therefore, there is no need to give a performance matrix for this technology. However, it must be commended for the extremely good response to environmental changes. Prototype Dynabit units have been operated under very harsh conditions.

Sonic BORAM

The magnetic shift registers have been recommended as the most likely replacement for spaceborne tape recorders. Among these shift registers the bubble memory will reward continued development work with a small, low-power unit. However, it would be unfair not to mention the sonic BORAM memory which could also be configured as a replacement for tape recorders. This technology has received considerable attention and is at a stage of development similar to the DTPL and Dynabit units; namely, prototype units will soon be available. That is, they will be available if there is a demand for them. The commercial future for sonic BORAM seems doubtful at present.

In the sonic BORAM system an acoustical wave in a glass or quartz substrate distorts a layer of magnetostrictive thin film deposited on it. The acoustical wave is used to scan the memory strips and modify the local magnetic properties for a coincident electric pulse to write in data. Of all the BORAM types examined, this has progressed the most. There are many points of difficulty, but they appear to be yielding to effort. A suitable substrate is required to carry the acoustical wave with low loss and, if possible, in a shear wave in the zero-order guided mode to reduce dispersion.

Also, depositing the magnetic film must not damage the substrate. The transducer must be a wide-band unit so that it can deliver the required fast rise time and narrow pulse, and it must be well bonded to the substrate. A narrow pulse is required for a good bit density. Some sort of dissipative load is required to reduce reflections. The magnetic medium must have a good magnetoelastic constant; too low, then the system has poor operating properties; too high, then stray strains, as well as the acoustical wave, rotate the easy axis away from its desired direction. The film must be deposited in a manner which yields very uniform magnetic properties. Since the linear packing density increases as the film switching time decreases, the film must switch in the rotational mode rather than by domain wall motion. This means that the coercive force must be larger than the anisotropy field, a so-called inverted film. The data rate is high, several MHz, since it is related to the speed of the acoustic waves. Blocks up to 500 bits long are feasible and the obvious operating mode is to scan characters or words in bit parallel.

A number of blocks can be strung together along one wire but with separate transducers for each block. In this way the number of input/outputs reduced since the length of the electrical block is now several times the length of the sonic block. The sonic block length can be increased by using a quartz substrate which combines a low attenuation with great expense. For a spaceborne memory, this trade-off will have to be made since the longest sonic block length possible is required. The electrical block length depends on the resistance per unit length of the line. Table XXV gives the performance matrix and environmental check list of a sonic BORAM system. It is based on a memory with twenty-five four-million bit modules. Power switching between modules is allowed because the memory is non-volatile. It has non-destructive readout. The memory is larger than the DTPL unit. The acoustical substrate has to be more substantial than the supporting substrate for the magnetic thin film in a DTPL memory. Also, the full area of the acoustical substrate cannot be utilized because of edge effects. Therefore, more substrate material is needed. The sonic BORAM requires temperature compensation circuits to maintain the clock rate constant. Because of the sensitivity of the magnetic thin film to stress, the memory needs careful design so that shock and vibration do not affect it. Tests have been performed to check for aging of the substrate and the memory film and the performance has usually been satisfactory. The data rate is very high and the operation is synchronous, so an asynchronous IC buffer register is needed at the input and output to match with the other data rates in the system. For these reasons, this technology was not recommended as a first choice replacement for spaceborne tape recorders. There seems to be little chance of the volume being reduced significantly, or the data rate changed in the future. Both of these features are related to the velocity of sound in the substrate. The volume could be reduced by increasing the linear bit density, but this requires a much narrower pulse associated with faster magnetic switching

TABLE XXV

PERFORMANCE MATRIX FOR A SONIC BORAM MEMORY

Performance Value		Capacity (bits) 10^8	Data Transfer Rate (bits s^{-1}) 1.3×10^7
Weight (lb)	450	2.2×10^5	2.9×10^4
Volume (in.^{3})	7000	1.4×10^4	1.8×10^3
Energy/bit (J)	1.9×10^{-6}	5.3×10^{13}	1.5×10^{12}

ENVIRONMENTAL CHECK LIST FOR A SONIC BORAM MEMORY

Response to temperature changes	Adequate
Response to shock	Adequate
Response to vibration	Adequate
Response to radiation	Good
Mean time between failures (predicted)	$\sim 10^4$ hours

and a more fragile transducer. To reach a bit density of 1000 bits $in.^{-1}$ implies that evaporated transducers are needed. These bit densities are definitely not available at present. The data rate is directly related to the linear bit density and the velocity of sound in the substrate; this again is unlikely to be changed.

This technology could be used in space but it has disadvantages compared to the magnetic domain shift registers, in particular, the size and the high, fixed data rate. The response to the space environment is good, but the expected lifetime is limited by the large number of interconnections necessary to connect the acoustical substrates into a longer electrical block.

Summary

The bubble memory has many development steps to go through before it can be packaged in a suitable manner for space. No claim is made that these steps are elementary or that the problems are simple. However, there is a great drive in industry today to solve these problems and the technology has advanced sufficiently to allow the definition of the materials problems. There is more work to do to analyze the system design and define more closely the system problems. The performance matrix for the bubble memory given in this chapter is based on the present state of the art. It is recommended that the system is not built using material with the extreme values of bit density and data rate commonly predicted for the future.

The metallic magnetic shift register is a good second choice. Because it is attractive commercially, this system will continue to be developed over the next few years. The spin-off from this development may justify a review of its status with respect to spaceborne tape recorders in the future.

IV. OTHER TECHNOLOGIES

This chapter reviews the advantages and disadvantages of the other memory technologies which were examined for suitability as a replacement for spaceborne tape recorders. Since these memory technologies were not recommended, the emphasis in this chapter will be on the disadvantages. The quoted disadvantages do not mean that the technology is regarded as unsuitable for other applications in NASA's data processing systems.

Ferrite Core Memories

It is apparent that a 10^8 bit memory unit based on ferrite cores will not be made in the near future and certainly not for use in space. As far as space missions are concerned, large units, possibly up to 1 million bits, are being considered. Today, 18 mil cores are commonly available, but the trend towards smaller cores is continuing and 14 or 15 mil cores will be available in two or three years time. There is not a direct reduction in the area occupied by the memory stack as the diameter of the cores is reduced since the terminals themselves require a fixed amount of area. The smaller cores do allow for an increase in operational speed which counters, to a certain extent, a possible decrease in output signal since the flux change now occurs in a shorter time. Using the same number of small cores per wire as for the larger cores does not result in greater difficulty stringing the cores since the wire length is considerably reduced. Because of the complexities of the electronics associated with a two wire ferrite core system and the extreme requirements of a space mission, it seems likely that a three wire system will be preferred. This implies that reducing the core diameter much beyond 14 mils is almost impossible because of the increasing difficulty of wiring. By utilizing power switching, single sense amplifiers for a large number of cores, operation in the block mode whereby a large section of the memory must be cleared, written into or read out of at any one time, and a relatively slow word rate, a low power is adequate for the system. Indeed, less than half a watt may well be satisfactory for a 2 million bit memory operated in this way.

An array of 10^8 12/7 cores (12 mil outer diameter, 7 mil inner diameter) each one 2.5 mils thick, placed on 15 mil centers requires 600 cubic inches and weighs 16 pounds. These figures are minimum values and do not include the weight and size of the wiring and supports. Typical industrial arrays, when assembled into planes of cores with wiring and interconnection pins, have a bit density of 4000 in.$^{-3}$, this is about 1/100th of the theoretical density given above. Without doubt improvements can be made so that arrays are assembled with a density of 20,000 to 50,000 $in.^3$ This implies an overall array size of about 3000 cubic inches for 10^8 bits. A trade-off must be made between the number of discrete blocks in the array and the number of driver circuits required. Also, the higher the density, the worse the heating problems. These brief considerations indicate that a 10^8 bit memory may well be 5,000 to 10,000 cubic inches, weigh 100 to 400 pounds and use several hundred watts of power to operate at a data transfer rate of 1 MHz.

A well designed memory stack with the cores embedded in a matrix of resin and epoxied onto planes can withstand shocks of over 1000 times the force of gravity applied in a few milliseconds, and sustained vibration of over 30g. The mechanical structure is very rigid and has no resonant frequency within the range of excitation frequencies encountered during launching. Each core is bonded to the planes in such a way that a pull of several grams - many times the weight of a single core - is required to detach it.

The wire threading the cores is a potential source of mechanical failure. It is subject to fatigue, is weakened by chemical changes that occur when it is soldered, and may be kinked and scratched during stringing. When the memory vibrates, the wires may rub against the cores, causing wear. Careful design and construction are necessary to guard against these vulnerable points.

The memory must also be protected against atmospheric hazards. Humidity and contamination could be responsible for both open-circuit and short-circuit failures in a memory. The weakest points in a large ferrite core memory are the soldered joints and the MTBF for a 10^8 bit ferrite core memory is likely to be less than 5,000 hours. However, extensive use of modern electronic packaging techniques reduces the number of soldered joints considerably.

The main disadvantages of the ferrite core memories are: 1) size, 2) weight, and 3) the amounts of power required. The present technical limitations are the size of ferrite core which can be manufactured, tested and wired; and the energy required to reverse the magnetization in the core.

Plated Wire Memories

Plated wire memories are being developed actively by many companies. The problem of aging which plagued earlier systems seems to have been overcome. Most companies are now studying refinements to produce better systems rather than attempting further major developments. The only major development underway is the work on miniwire, that is 2-1/2 mil diameter plated wire. This small diameter wire halves the bit drive current required, since it reduces the magnetic field pattern considerably. The whole system is compatible with integrated circuits because the word lines only require about 300 mA of drive current through a single turn line. It is possible to get 2500 bits in.$^{-2}$ in a plane and an interplanar spacing of 0.1 inch is possible.

The magnetic properties of the plated wire determine both the electronics required and the size of the memory unit. The easy axis dispersion and skew should be minimized in the film; the anisotropy field must be greater than a few oersteds or the output signal will be negligibly small; and the coercive force must be such that disturbance of bits and creep does not occur. The bit packing density is determined by the need to prevent cross-talk between the lines, creep between adjacent bits, and to maintain uniform electrical parameters along each line. The magnetic influence of the current in each word line spreads along the plated wire for a finite distance on each side, so there must be a finite distance between word lines. There are several reasons for this condition. The plated wire is a continuous magnetic medium and domain wall creep is apt to affect adjacent bit locations. Also, the strong localization of magnetization leads to a large demagnetization field which, during readout, requires a large word current. Since it is desirable to use integrated circuits for the drive circuits, the electrical properties of the lines must be carefully optimized. As a result of all these factors each bit occupies about 50 mils of wire length. This is also the approximate spacing allowable between the plated wires.

The magnetic properties of the plated wire memory can be improved by using a magnetic keeper. There are advantages to using a Ni-Zn ferrite, since it has a good electrical resistivity and its permeability and dielectric constant are such that cross-talk and delay time are not adversely affected. The keeper acts to localize the word current field and to reduce the associated demagnetization field. This makes the plated wire memory system rather insensitive to slight variations in the system parameters.

To provide a uniform electrical environment for each wire, several spare wires have to be provided at the edge of each plane of memory elements. Also, to enhance the signal-to-noise ratio, it is desirable to place extra noise cancelling wires in the array the extreme of this approach is to use two-element-per-bit storage Typically the output signal is a few mV in magnitude.

Plated wire memories behave well under conditions of stress, shock, and acceleration because of their rigid construction and the use of zero magnetostrictive wire. They are also insensitive to nuclear and particle radiation since they are metallic and polycrystalline and the generation of electron-hole pairs and the displacement of nuclei by radiation have little influence on the magnetic and electric properties. Plated wires can be operated over a wide range of temperatures. The mean time between failure for such a system depends to a large extent on the lifetime of the electrical connections.

If a bit packing density of 5×10^4 bits in.$^{-3}$ is realized in the future, then 10^8 memory cells will occupy 2000 cubic inches. This is a minimum because of the need for information and address buffers, address decoders, drivers, switches and a controller. The weight of this memory will be of the order of 300 pounds if a ferrite keeper is used. At a data transfer rate of about 10^5 bits s^{-1}, 100 watts are required.

The main conclusion is that plated wire memories in their present form are not adequate to replace tape recorders. Improvements in technology must be looked for to increase the bit density towards 10^6 bits in.$^{-3}$ without adding too much weight in the form of keeper magnets. The basic physical limitation on bit density is the interference between adjacent bits, so better ways must be found to localize the magnetic fields to reduce this. The 2-1/2 mil diameter mini-wire offers a bit packing density of 40,000 bits in.$^{-3}$ and it has much smaller drive current requirements. The word current is 250 mA, which one transistor can supply, and the digit current is 25 mA. A 5 mil diameter wire memory requires three times the weight, and needs twice the power. Therefore, future developments in the mini-wire technology will certainly open up new uses in spaceborne systems.

The main disadvantages of plated wire memories are similar to those for ferrite core; namely: 1) size, 2) weight, and 3) power requirements. Plated wire memories have several advantages over ferrite core, notably speed and the ability to operate in an NDRO mode. Also their power requirements are lower, but not yet low enough.

Thin Film Memories

Metallic magnetic films for digital memories have been under development since the mid 1950's when the storage mechanism in thin films with uniaxial anisotropy was first demonstrated. Their development has not been spectacular in the intervening years, due, in part, to the success achieved in improving the performance and reducing the fabrication costs of ferrite core memories.

The main difficulty in the operation of thin film magnetic memories is obtaining controlled switching, growth, and movement of the magnetic domains. Switching is possible when the vector sum of the word and bit fields ($H_Y + H_x$) is greater than a switching threshold. Normal operation is to have $H_Y > H_k$ (the anisotropy field), so that only a small bit field is required to cause switching by magnetization rotation.

Once the information is stored, it must remain until it is required to read it out. Unfortunately, during the storage period the memory element is subjected to stray fields from the following sources:

1. A demagnetization field, which is static,
2. Stray fields due to skew and dispersions, static,
3. Stray fields from neighboring bits, static,
4. Bit drive fields at unaddressed locations, transient,
5. Fringing fields from both the word and bit lines at neighboring locations which are being addressed, transient,
6. Fields caused by pulses induced on the bit and word lines by the signals on adjacent lines, transient,
7. Fields caused by neighboring bits switching, transient.

These fields alone will not cause any alteration of the magnetization in a perfect film unless they exceed the switching threshold. Unfortunately, flaws and residual fields abound in thin film memories. The flaws help establish a second switching threshold for unwanted switching which is called the creep threshold. The creep threshold is strongly influenced by the skew and dispersion of the magnetic moment across the film. Both skew and dispersion are effects of the film's polycrystalline nature and the failure of all the crystals to line up perfectly with the magnetic field in which the film is deposited. They have the effect of making the memory device more susceptible to stray fields since they introduce field components at an angle to the easy and hard axes. This brings the resultant field closer to the creep threshold. The digit field required for switching must be increased since there is now a non-zero field component due to skew along the word axis which tends to oppose the switching. Having to use larger digit currents also implies that the creep threshold is approached more closely during write.

Overn (Ref. 12) says that the real difficulty in thin film arrays is neither skew nor dispersion, but magnetostriction. Skew and dispersion, although serious, are under control since techniques have been devised to produce large, thin film arrays with suitably small values of skew and dispersion. Magnetostriction causes the skew to increase greatly when a small mechanical strain appears in the element. Strain is almost impossible to avoid completely and, even if a mounting that completely relieves an array from strain can be devised, the slightest external force or tremor introduces new strains. Thus, magnetostriction is a major factor hindering further progress in planar memories.

To avoid creep, the vector sum of the bit field, plus the stray word fields, must be below the creep threshold as modified by skew and dispersion. This can be achieved by proper design of the word and digit lines and the electronic circuits that drive them. In general, either a sufficiently large word field alone, or a sufficiently large digit field alone, can switch the magnetic state of an element. If both fields are present, their sum can switch the element if it is outside the rotational switching threshold curve. But, if the sum of the two fields is just below the rotational threshold, the element's magnetization will not switch unless the driving pulses are repeated many times. If the sum of the two fields is below the creep region, it has no effect on the element. It is necessary to make sure that a field that should be below the creep region stays below it, even in the presence of small electrical transients. To guarantee full switching, the bit field must exceed a certain minimum value and the word field must exceed the sum of the anisotropy field and the demagnetizing field of the bit when driven into the hard direction.

The important thin film parameters are the switching threshold (related to the anisotropy field), the creep threshold (related to the coercive force), and the demagnetizing field (related to the bit geometry). There are many ways in which these parameters can be modified and it is not possible to discuss them all. Among others, the anisotropy field may be varied by altering the film preparation, additions of Co to NiFe increase the anisotropy field H_k, or by altering the in-field anneal procedures. The coercive force can be altered by alloying the NiFe with Co or other metals; it also depends on the substrate, on the grain size allowed to grow, and it can be altered by depositing multilayer structures or shaped structures. The demagnetizing field can be reduced by using structures which close the magnetic flux path either completely or almost completely, or by using keeper magnets with the same function.

It is essential to grow the magnetic films with the minimum amount of skew and dispersion and with good uniformity of the basic magnetic properties. As far as possible the films should be mounted on stress free mountings and be adequately temperature compensated to reduce expansion problems. Adequate shielding from external fields must be used. The thin film should have as few flaws as reasonably attainable to reduce the number of nucleation centers in the bulk of the film. For those memories based on one continuous plane, it is wise not to utilize the whole area of film so that edge effects, such as edge induced anisotropy and edge nucleation, do not influence the bit pattern. Tight tolerances must be maintained on the wiring to reduce creep and noise. The magnetic properties of the thin film can be altered by using multilayer structures, but the ability to fabricate large, multilayer arrays, characterized by precise control of electrical and magnetic properties, and to test these arrays at low cost is a difficult art. Thin films have been grown by vacuum deposition, sputtering, electroplating, and electroless plating.

To achieve low power consumption and high reliability for spaceborne memories, coincident current addressing, and NDRO operation have significant advantages over other methods. Depending upon the application, either or both features may be useful. Presently, planar thin film memories are operated in the linear select, DRO mode. NDRO operation can be achieved by rotating the bit magnetization towards the hard axis by a driver field and sensing the sign of the voltage induced in the sense lines. This process must be reversible so there is a limit to the drive field which cannot be exceeded. This limit is dependent on skew because some bit elements are closer than others to the limit in the absence of a word field; this situation limits the amplitude of the word current in the NDRO mode.

To achieve coincident current addressing, which reduces considerably the amount of associated electronics, a material with an accurately reproducible square hysteresis loop is needed. Without this, the half selected bits will suffer from the repeated pulsing and creep problems will manifest themselves. The coincident currents together must not exceed the reversible limit or the quality of the data is reduced.

There have been attempts to overcome the readout problems by using the non-linearity of the hysteresis curve to mix rf signals. This tends to give signals independent of half-select noise and more independent of bit volume than other techniques. Another technique suggested to improve signal-to-noise on readout is to supply a burst of rf current on the drive line which modulates the magnetic moment of the selected bit at the rf frequency. The induced voltage appears on the sense line at the same frequency and can be detected with a tuned amplifier.

The original planar thin film memories were just simple planes with a wire array superimposed. These memories were very susceptible to the difficulties summarized above. The trend has been towards constructing more complex memories with sophisticated memory elements and precisely controlled electronics. In this way, memories which exhibit very few of the problems of open planar film memories have been made. However, this has been achieved at great cost in the production and testing stages so the memories have never really been competitive commercially.

Mated film memories are being used in certain avionic applications, but they are not directly applicable to the replacement of tape recorders because of their bulk and power requirements. Etched permalloy memories were regarded with great optimism, but their development has now stopped. Among other problems, they had a very poor signal-to-noise ratio.

Even after considerable efforts, planar thin film memories still have drawbacks. Small capacity, high speed processor memories have been made successfully, but it appears that the extension to mass memory systems is still some distance away. The elementary 2D-2W array, which matches their magnetic properties, is very expensive in electronics, even more so than other random access systems. Coupled and planar films offer the best bit densities at the moment, but the more complex the bit element, the larger it is, and so the less attractive from the point of view of a spaceborne system. Their main advantages are low energy requirements for switching the memory cells and the very short, a few nanoseconds, switching time. There is no fundamental limit which prevents them from being used as mass storage devices but, like ferrite core and plated wire systems, this solution is really a brute force remedy. Figure 6 summarizes the present and future status of planar and plated wire memories.

Optical Memories

There are numerous designs for optical memory systems. Many of these systems require electromechanical subsystems so they are not considered further here. There are three main categories of memory left for consideration as candidates for a spaceborne memory. One class utilizes the coherency properties of lasers to record data in holographic form on a suitable medium. A second class uses the high power density of laser beams to write information bit by bit onto a suitable storage medium. The third class of optical storage is called an opto-electronic store where photodetectors interrogate an array of light emitting diodes (LED) to see if they are on or off. In this system the array of light sources acts as the storage medium.

An opto-electronic memory offers several advantages. The input and output sides are completely isolated and may both be grounded separately. Data can be read out serially, in parallel, or in blocks by selecting the right addresses. Finally, optical transforms of the data can be made simultaneously with the readout process by introducing suitable masks between the storage medium and the detectors. The main disadvantages are the volatility of the storage, the continuous power drain exacted by the LED's, and the provision of LED and detector arrays. Typically, the LED's available today require about 10 to 30 mW to produce an output of sufficient intensity to make it suitable as a display. In the memory application, there is no need to use this much power since the photodetectors can be shielded from the ambient light and can detect much lower light levels. An order of magnitude reduction in input power reduces the light level by about 5 times, which is still satisfactory for system use. Also, there is no need to use visible radiation. Advantage can be taken of the good match between the GaAs infrared emission and the peak of sensitivity of the silicon detector. In this way one can also use the LED in a more efficient mode. Therefore, it is possible

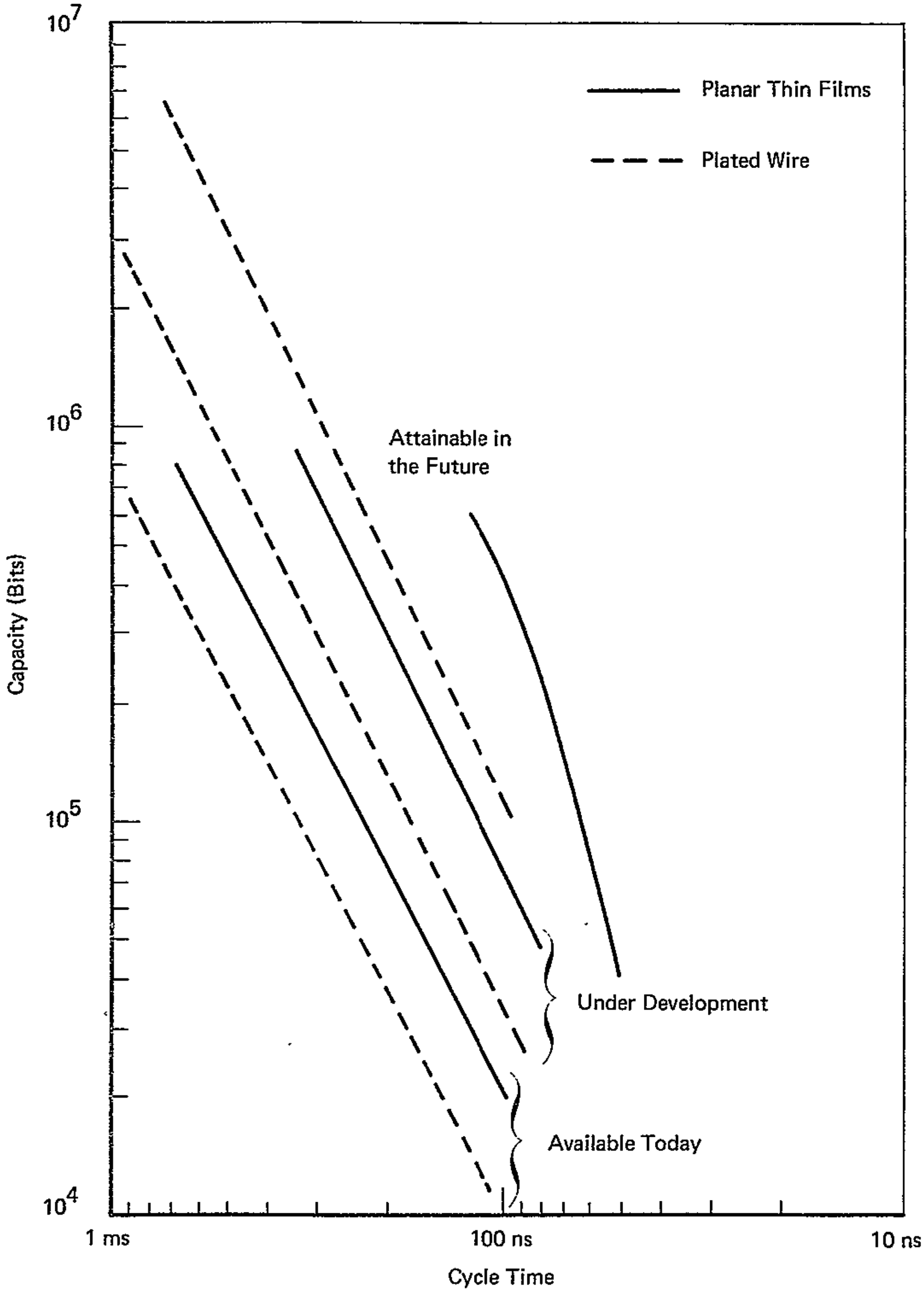


FIGURE 6 PERFORMANCE OF THIN-FILM MEMORIES

to talk of an operating system with perhaps 10 to 100 μW per bit power dissipation. Assuming a 10^8 bit memory with 5×10^7 bits switched on such a system would give a power consumption between 5×10^2 and 5×10^3 watts, which is too large for a space vehicle. The other big snag is that it is not possible, at the moment, to make the large arrays of LED's and photodetectors needed for such a memory. The Texas Instruments vidicon and the Optical Memory Systems units come closest to the sizes needed. The packing problems and suitable techniques for handling stray light inside the system which might cause cross-talk have not even been touched upon yet in the development of this system.

In conclusion, this does not look like a suitable spaceborne memory. Most of the current commercial work is on ROM's which do not need continuous power and are non-volatile so it is not likely that a random access system will be developed in the near future.

Those systems which require lasers for operation are regarded as unsuitable at the present state of laser development. The main disadvantages are: 1) the weight and volume of the lasers, beam deflectors, and power supplies needed to operate them, 2) the poor efficiency of the lasers, 3) the poor match between the laser pulse rates and the data transfer rates, assuming a system with one bit stored per pulse, 4) the short laser lifetimes, and 5) the possible need for mechanical motions in the system. The main advantage of optical techniques is the high bit density, implying that only a small amount of storage material is required.

The auxiliary equipment needed has not received sufficient development to satisfy the overall system requirements of size, weight, power, and lifetime. The only laser which comes close to matching the requirements is the GaAs laser which basically is a low power device. The others are all bulky and need bulky power supplies as well as having short lifetimes. The technical problems of achieving 10^8 resolvable positions with a deflection system are formidable; once more, the GaAs laser, used to form an array, may be the best choice. However, since the usual optical materials used to store the information can store up to 10^8 bits per square inch only a small amount is needed to make a 10^{10} to 10^{11} bit memory and the advantages of having a memory with this capacity for some special application may well outweigh the disadvantages of the associated equipment

Holographic storage has the advantage of a large bit storage density and redundant storage associated with rapid access, so it must still be regarded as a serious contender for memory systems over a period of 8 to 10 years. Photochromics, photoplastics, thermoplastics, and manganese bismuth are being investigated to see if they are suitable eraseable storage media. Certain ferroelectrics form another class of material which could act as an eraseable storage medium. Strontium barium niobate and lithium niobate have both been used in preliminary experiments. One subsystem which is required for a holographic storage system, but not for a discrete bit storage system, is the page former which carries the data to be recorded holographically. Ferroelectric materials and liquid crystals are being examined for this application.

Although beam access systems are the only contenders for really large capacity memories (10^9 bits or more), they will not be available in suitable form for some years. Their present state of development does not justify recommending them as replacements for tape recorders in five years.

Integrated Circuits

Integrated circuit (IC) technology is one of the fastest moving technologies in the U.S.A. There has been a rapid development in the type and complexity of circuits since the first bipolar IC's were made. This is still the major type and is used for nearly all logic functions. The basic memory unit is a flip-flop circuit with set and reset circuits. Typically, one chip is about 100 by 100 mils, and contains 64 bits and address decoders. This type of circuit is used for high-speed computer scratch-pad memories. There is a power-speed trade-off since the faster the switching time of the circuits, the more power is required. But, typically, a bipolar unit requires 10 mW per bit at operating speeds. The information is volatile and is lost if the power is removed.

The next major development was the IC using insulated gate field effect transistors (MOS transistors). These IC's are slower than bipolar circuits because of the drive impedance levels and the capacitive charging and discharging inherent in the MOS transistor structure. To overcome this disadvantage, several types of dynamic approaches have been used, where one or more circuits supply pulses of charge at regular intervals to the transistor so that the operational times are reduced. Alternatively, the voltage swings can be reduced so that less charge has to flow. The latter approach has to be supplemented by higher gain sense amplifiers than those normally used. To maintain the operating speed, it is essential in this technique, and all the other integrated circuit techniques, to put the address decoding on the same chip.

MOS memories have advantages over bipolar memories, except at the higher speeds, since the MOS production process has less steps than the bipolar process and, all other things being equal, correspondingly higher yields. Also MOS transistors do not need the isolation between active areas which is so important in bipolar circuits. Also, they are lower power devices in operation. However, the dynamic operation used in the MOS circuits means that they dissipate more power on standby than the bipolar types since the data are lost if it is not continuously replenished even during standby.

Complementary pairs of MOS transistors consisting of p-channel and n-channel devices on the same chip have recently been developed. These have the advantage of dissipating very little power in the standby mode because no direct path ever exists to ground. Standby power ranges from 10 to 100 nW/bit. There is the disadvantage that complementary memory cells are larger than single polarity cells because of the isolation diffusions required between the devices. In contrast, the static p-channel MOS memory cells dissipate about 1 mW/bit whether in standby or in the operating mode, while the dynamic p-channel MOS memory cells dissipate power which increases as a function of operating frequency. Dynamic p-channel MOS memory cells are smaller than static cells because the ratio of "on" impedance to "off" impedance is not used in this logic and minimum geometry devices which do not emphasize device impedance can be used. Unfortunately, the low power comes at the expense of size in complementary MOS. A reasonable estimate is that the chip area per bit increases by two or three times.

Integrated circuits are capable of withstanding shocks, vibration, and extreme accelerations. There is a need to see that they are carefully mounted and packaged so that they do not shake loose, have wire bonds break, or be injured by parts moving relative to each other. However, they have already been flight tested many times and proved satisfactory. Their response to temperature changes and pressure changes is acceptable over a wide range of values so there is no cause for worry there. In certain situations magnetic fields may cause false signals but these situations are rare. The one environmental situation which may cause worry is exposure to radiation. As this is something which may occur in military environments, it has received considerable attention recently.

Up to the present most emphasis has been placed on the influence of radiation on bipolar transistors, but the other types are affected also. The crystal structure damage can be repaired by annealing processes, but this is impractical in space. The best thing to do in a bipolar transistor is to deliberately shorten the minority carrier lifetime by doping it with gold and design the transistors to operate in this mode; then further damage only represents a small further decrement. The influences of ionizing currents can be reduced by using dielectric isolation and thin film resistors instead of p-n junction isolation and diffused resistors. Alternatively, the system can have a radiation detector built in and the whole system switched off when the detector detects more than a certain threshold of radiation. MOS circuits do not require isolation of the active areas but this is necessary in CMOS. Circuits have been developed which are believed capable of withstanding the savage radiation conditions after a nuclear blast. They have certain difficulties since they require many more processing steps which reduces yield and increases cost. Also, oversized devices with large resistors and wider conductors are better. Included with this are the dielectric isolation barriers, so the basic cell size is almost double the normal cell size.

There is little doubt that bipolar integrated circuits will operate reliably in space, but there may be periods when radiation degrades their operation and, on a long mission, the cumulative effects of radiation may produce a permanent degradation. There is still little information about the performance of MOS's and CMOS's under irradiation.

A more recent development has been the variable threshold MOS transistor, called MNOS in this report. These transistors represent a potential approach to a non-volatile, high density, semiconductor memory. The threshold associated with the current-voltage characteristic of a device can be altered and the new state sensed at a later time without the need for standby power in the interim. Since the storage element is an individual transistor of MOS-like construction, the bit density is very high and the number of bits per chip is also high. In these respects, the MNOS array may eventually approach a complexity equivalent to an MOS read-only memory array.

The variable threshold MOS device is regarded as promising by several companies for an electrically alterable read-only memory. There are problems associated with this particular device which make it unlikely to be available for at least two years. These problems also apply, perhaps to an even greater extent, to a variable threshold MOS device designed specifically for the random access memory. Such a system appears to be some years away, probably at least five. Among the problems associated with this technology needing further attention are:

1. Speed of Write - This depends on the write voltage, the dielectrics, and the geometry chosen; improvements in materials are giving faster write at voltages down to 30 volts;

2. Time of Retention - The variation of the time of retention is related to the write time, geometry, and the dielectrics used; at present $\sim$ 1000 hours are attainable;

3. The Growth of the Necessary Very Thin Oxide Layer and the Nitride Layer - There are variations between the various manufacturers in the thicknesses of these layers, usually this is regarded as proprietary information;

4. The Purity of the Dielectric Layers Grown - Apparently these layers must be grown with greater care than the oxide layer in the standard MOS procedure, and the heat treatments to which they are subjected must also be carefully analyzed;

5. The Asymmetry of the Write Operation - The asymmetry occurs because a different voltage or a different time to write a 1 compared to an 0 is required;

6. The Radiation Hazard - Apparently this hazard is no worse than for standard MOS;

7. The Yield for Large Chips - It would be desirable to have chips carrying at least 8k bits; currently the talk is of chips with 1k bits;

8. Reliability and Aging - The reliability of the system and the possibility of aging has to be checked;

9. Packaging - Packaging is a problem because of the large number of interconnects;

10. Readout - The readout is difficult since, to maintain speed of operation, MOS procedures, such as the use of pre-charged lines, are required; current sensing is apparently faster than voltage sensing;

11. Mixing Devices - It is desirable to mix variable threshold and fixed threshold MOS's on one chip to allow for on-chip decoding; this requires increased care during processing;

12. Clear Process - The clear process to remove data may cause difficulties; these difficulties are associated with the asymmetry of the write process;

13. Addressing - A coincident current addressing scheme is not feasible at the present state of device development, so a linear organization must be used;

14. Electrostatic Damage - MNOS devices are sensitive to damage from electrostatic charges; since they need both positive and negative voltages on the chip, a double zener device is needed to protect the gates, this complicates processing.

There is real doubt whether the MNOS memory can be configured as a 10^8 bit memory by 1975 unless considerable development work is undertaken at the device and system level. It will probably be a good candidate for smaller main memories of 1 to 2 microsecond cycle times within this time period. The unresolved issues represent good technical milestones by which to measure progress.

The IC's under development which use amorphous semiconductors have the advantage of being almost radiation resistant. Their development is still at an early stage and it is difficult to predict how it will progress. Current information is that the first product will be an electrically alterable read-only memory. The clear and write times associated with this technology are rather long and the voltages required are not standard logic levels. The basic memory cell size is larger than in the MNOS IC. It is unlikely that this technology will develop sufficiently in the next few years to make it a real contender to replace tape recorders. There are many similarities between the status of the amorphous IC and the MNOS IC. Both are in early stages of development; both have materials problems; both currently need non-standard supply voltages; and both are being developed as electrically alterable read-only memories. The important difference is that the MNOS technology is supported by a much greater effort, industry-wide, than the amorphous IC's.

Bell Telephone Laboratories recently announced another semiconductor device which they call a charge coupled device (CCD). It is based on MOS technology, but offers the possibility of making shift registers with data rates over 1 MHz at a packing density of 200,000 bits in.^{2} It is the electronic analog of the bubble device. The information is stored as a cloud of minority carriers trapped under an electrode, and it is moved around by altering the potential gradient between neighboring electrodes so that the minority carriers are moved from beneath one electrode to the other. There are materials problems associated with the surface trapping centers at the silicon-silicon oxide interface, and there are also systems problems associated with the volatility and dynamic nature of the operation. Further development is awaited with interest. At present, there is not enough information on the device and possible systems to justify recommending it for use in spaceborne systems.

The main disadvantages of integrated circuits are: 1) volatility as a storage medium, 2) sensitivity to radiation, and 3) power requirements. However, there is hope that some or all of these disadvantages can be overcome in the future. For instance, the radiation problem has received considerable attention and may not be so severe as at first supposed. Also, the MNS technology holds promise for less volatility and perhaps lower powers, as well as considerably smaller volumes and weights.

Planar Ferrite Memories

There have been many attempts to adopt ferrite to the batch fabrication of memory stacks. The ferrite core has proved successful in a variety of applications for many years, but requires so much labor during the stringing operation that a convenient way of making a memory stack in a batch process is very attractive. One immediate economic advantage of such a system, if feasible, is that the overall cost of a large memory system becomes reasonable. For 10^7 to 10^8 bits of core memory the stringing costs are the principal cost, while for the same size batch process memory, the stack costs and the costs of the associated electronics are approximately equal at about this size of memory. Other possible advantages are a more efficient interaction between the ferrite and the drive lines leading to lower drive currents, a higher bit density in a continuous medium than in discrete cores, cycle times between 0.5 and 5 μs, and nondestructive readout.

In the past a lot of attention was paid to laminar ferrite structures. However, no one seems to have succeeded in realizing their promise as a low power, batch fabricated ferrite memory. The main difficulties are associated with the conductor pattern, its placement in the system, the signal to noise ratio, the numerous wire connections, and the loading on the lines by the ferrite. This approach does not seem to offer a suitable solution to the problem of a small, low power, mass storage system.

Other approaches which are based on the batch fabrication of ferrite include the "flute" memory, the "post and film" memory and the "apertured" ferrite system. Of these, the post and film memory is the most practical. The flute memory uses large and unwieldy ferrite structures threaded by one word and several digit lines. The apertured ferrite memory has a poor bit packing density. The post and film memory was recently discussed (Ref. 13) in Electronics magazine. It has several similarities with the somewhat older "waffle iron" memories. This memory has some advantageous points, especially the low drive current, 40 mA for the digit line and 150 mA for the word line, which means that integrated circuits can be used throughout the associated circuitry. The memory consists of two layers of permalloy film bonded to a glass substrate, with a layer of non-magnetic material between them. The permalloy layer next to the glass is a "hard" film, that is, highly anisotropic, and its magnetic hysteresis loop is nearly square in the easy direction and almost linear in the hard direction. The other permalloy layer is "soft"; it is also anisotropic, but the difference in its magnetic properties in the two directions is less pronounced. The easy directions of the two films are parallel to each other and parallel to the word line. In this direction, binary 1's and 0's correspond to magnetization one way or the other. Two sets of grooves are cut into a ferrite block at right angles to each other, leaving a set of posts. Drive conductors are then placed in the grooves, and the glass substrate carrying the films is placed over the ferrite, film side down, to complete the structure. Because the memory elements contain both hard and soft films, readout can be either DRO or NDRO. The posts define the bit positions on the film, which therefore need not be carefully registered on the ferrite array. The posts also provide a complete path through low-reluctance material for the magnetic flux and this reduces the creep problems encountered in planar thin films and reduces the demagnetization field. It has been predicted that an 8000 word unit with 33 bits per word will require 20 watts of power. The bit density is about 1800 bits in^{-2} with the current layout. Therefore, this system is too large and needs too much power for a tape recorder replacement.

Travelling Domain Wall Memory

Some development work on the travelling domain wall memory has been performed. A moving domain wall in one magnetic film scans the storage thin film adjacent to it. The wall position is monitored and the data are written in by applying a suitable field pulse which alters the local magnetization at the point being scanned. To read out, a series of pulses are detected in the sense wire as the domain wall scans over the data positions and modifies them. One travelling domain wall can scan many storage tracks and all the variations of series and parallel data flow are possible. It is usual to place a conducting film between the two magnetic media which acts as part of the shorted secondary of the drive transformer. This has several advantages. It reduces bit disturb problems, and the bias field requirements, and it makes the system less sensitive to changes in the wall velocity. The linear bit density attainable is limited by the spacing between the magnetic films and the resolution of the domain walls. The domain wall can be driven up to 5000 ft s^{-1}, but at the higher fields required for high speeds, there are difficulties with unwanted nucleation centers. Among the disadvantages of this technique are the poor bit density, the difficulties of adjacent bit and adjacent track interference, the jagged nature of the domain wall, the high drive currents required, and the preparation of the structure since the thickness of the film carrying the domain wall must be carefully controlled. It is believed that development work on this technology has ended. There seems little chance of the system being developed into a replacement for a tape recorder.

Cryogenic Memories

Although cryogenic technology has advanced considerably over the past two decades it has, as yet, had little effect on the implementation of electronic systems. Many specialized components have been made in R&D laboratories, including memory units, but only in recent months has anyone marketed a cryogenic electronic component (a sensitive voltmeter by Keithley).

The change from normal to superconductivity exhibited by many materials forms the basis of a memory element. Many configurations have been tried by many people but there seems to be little interest in the technology now.

It is obvious that the main factor in the description of this memory is the ancillary refrigeration gear required to maintain continuous cooling. Any failure in this equipment would lead to the loss of all the data when the bit cells warmed past their critical temperature, unless the data could be dumped during the warming-up time. This volatility is different from the immediate loss of data when the power supplies of an IC memory fail. However, the down-time is likely to be much longer for the refrigerated system since the cool-down time can be significant.

With current technology the only way to produce constant liquid helium temperatures is to use a closed-cycle electro-mechanical refrigerator. Immediately several problems arise. The major ones are reliability and overall efficiency. The main reason for wishing to replace tape recorders as a memory device is their poor reliability due to their mechanical parts. The engineering problems of a cryogenic refrigerator are substantial without having to ask the system to withstand the launch environment. To operate in space a completely sealed unit is required and the maintenance of this sealing is another difficulty also faced by tape recorders. Even in especially cozy environments, a lifetime of three years is unusual for these systems. The overall efficiency of these units is typically $< 1\%$, so to maintain 0.5 watt cooling about 50 watts of driving power is required. This depends to some extent on the speed with which initial cooling is desired. It is obvious that this system cannot reasonably be recommended for a space mission. Cryogenic systems are unlikely to be used on long unmanned missions unless a thermoelectric refrigerator is developed which can use space as a heat sink.

Ferroelectric Memories

The use of ferroelectric materials as a memory, in direct analogy to a ferromagnetic material, has never been really successful. The main problems are related to the properties of the ferroelectric material. The following cause particular difficulty (Ref. 14):

1. There is no real coercive electric field in a ferroelectric,

2. Heating due to hysteresis losses is more severe than in metallic magnetic materials because the ferroelectrics tend to have poor thermal conductivities,

3. The materials show fatigue effects,

4. Some materials, such as $BaTiO_3$, have a shelf-life problem,

5. There is no well defined switching threshold.

Because of these problems, no one produced a ferroelectric core memory which is competitive with other memory devices. Thus the predicted advantages, namely non-volatile operation, low power, good signal-to-noise ratio, and ease of use with integrated circuits, have never been realized.

Work on ferroelectric materials has continued and it now appears that other modes of use as a memory may be possible. Of all these more recent developments, the electro-optical devices have received the most attention. They are based on polycrystalline ferroelectric ceramics which have been poled in an applied electric field. There are two modes of operation, depending on the grain size of the material. For those materials with grains above 2 μm in diameter, the most convenient mode of operation is to utilize the scattering of light by the dipoles. When the dipoles are aligned parallel to the light beam, there is maximum transmission of light; when they are perpendicular to the beam, the scattering reduces the transmission considerably. In this way a light modulator can be made, or, alternatively, a binary digit store using the on-off mode of operation.

The second mode of operation is favored when there are fine grains under 2 μm in diameter. In this case the birefringent properties are utilized and a polarization switch consisting of two polarizers and a piece of ferroelectric ceramic with suitable electrodes forms the element. The switching depends on the light wavelength, the plate thickness, and the voltage applied to the electrodes. In both systems thin, optically polished plates, and a complex array of electrodes which defines the bit size are required. Also, a suitable light source and an array of detectors are needed to read out the data. In principle, bit densities up to 10^6 in.$^{-2}$ are feasible, but in practice only small units with 5000 to 10,000 bits in.$^{-2}$ have been made. However, even assuming that 10^5 bits in.$^{-2}$ are stored in the material, this still implies 1000 in^2 of material which must be packaged so that a light beam can reach every address. This means a large and bulky system if the storage medium has to remain fixed. All in all, the outlook is not good for this technology as a flyable mass memory.

The use of ferroelectrics in conjunction with variable threshold transistors has died since the development of MNOS devices. Piezo-electric devices are not really of direct interest here, and this leaves the photosensitive $BaTiO_3$ Schottkey diodes developed by Sawyer at NASA's Electronics Research Center. These devices are still in the early stages of development and much of the physics of operation and possible performance characteristics is as yet unknown. The main disadvantages seem to be similar to those associated with the electro-optical system, namely, the provision of lots of electrodes and suitable optics, and the heavy capacitative loading presented to the drive electronics.

The main conclusion of the study of ferroelectrics is that they are only in the early stages of development and that, even if developed, they would suffer from the large overhead in the form of optics and electronic circuitry which are required. They do not appear suitable for mass storage in space vehicles.

Delay Lines

Mercury delay lines were among the earliest devices used for computer data storage, but they have since fallen by the wayside. Recent developments in delay line technology and the increase in the market for desk calculators have brought this type of system back into prominence.

There are three main types of delay line memories -- the wire delay line, the bulk delay line, and the surface wave delay line. Each has particular advantages and disadvantages, but they all suffer from the same defect, volatility. It is necessary to keep recirculating the information from the output to the input to retain it. They all have one advantage over other serial memories; namely, they do not require extra power to drive the data down the delay line once it is launched. This advantage is shared by the sonic BORAM system. They do not appear to be realistic contenders for a replacement of moving media systems in space missions. They are volatile, they do not have a good bit packing density, the power consumption per module is significant and they are heavy. Also, their environmental resistance is doubtful.

Electron Beam Technology

It is well understood that optical techniques offer the possibility of very high bit densities and rapid access to the data. The high bit density is associated with the focussing properties. The rapid access is associated with the zero inertia of the photon beam and the almost instantaneous interaction of photons with matter. These advantages are present in electron beam systems also. The main differences are that the electron beam is not coherent and the theoretical limit of the bit density is higher. The bit density goes as λ^{-2} where λ is the beam wavelength. Incoherent light can also be used, but this does not approach the theoretical limits as closely as the coherent beams do.

Electron beam systems require an electron source, modulation, focussing, and deflection systems and a suitable storage material for the target, as well as a vacuum vessel, detection techniques, and information buffers. A major difficulty with electron beam systems is the provision of an intense beam. The brightness of an electron beam is generally less than that of a laser beam. Considerable work is needed to devise a long life cathode capable of emitting several amps/cm^2 over a small area. Deflection and focussing the beam can be achieved by using magnetic, electrostatic, or combined fields, while amplitude modulation is easily attained by modulating the emission currents. In direct analogy with the optical case there is a maximum number of resolvable beam positions in the maximum deflection angle. This figure is between 8000 and 15,000 and depends on the beam current. It is higher for the lower beam currents. The resolution in this type of system is limited more by aberrations than by the Rayleigh resolution criterion.

Because of the limit imposed by the maximum number of resolvable spots and the desire for a high bit packing density, the beam can only be moved over a small area on the target, about 0.04 by 0.04 in., without moving the target. This can be improved on by using a two-step process whereby the beam is deflected to positions on a secondary deflection structure over an area of about 1 by 1 in. This second structure accepts the beam and deflects it over the smaller area. This is known as a "fly's eye" lens. Even if a larger number of resolvable positions were possible, the accuracy required in the power supplies to drive the system would be a limitation.

At the moment there is not really a suitable material for an erasable store using electron beams. It is possible to use a Curie point writing system on a magnetic material using electrons for both write and read, but an intense beam is needed to raise the temperature above the Curie point and the signal-to-noise ratio of the output is very poor. At least two write-once systems have been developed; one uses an electron beam to burn holes in a target, while the other uses a photographic emulsion to record the information.

Although it might be thought that no vacuum chamber would be needed to use an electron beam system in the hard vacuum of space, this is not true. First, the ground check-out procedure requires a vacuum chamber, and second, some vacuum devices do not operate efficiently in a hard vacuum. However, the natural pumping action of space can be used in flight to pump down the chamber against the vapor pressure of a deliberately introduced gas source. In this case pumps and many valves become ground support items only.

Since the bit size is very small, small defects in the storage medium or dust particles on it can cause the loss of a lot of data so that for best use the memory must have extensive error-checking and error-correcting features. A good beam intensity is a help since it leads to a good signal-to-noise ratio and an improved error rate.

Most of the memories suggested involve moving media systems, a lot of electronics to control the beam, and special features to reduce the effects of environmental changes, such as temperature, vibration, and stray electric and magnetic fields. For all these reasons they do not appear to be realistic contenders for a spaceborne memory.

Although plated wire and optical memories can be used to store analog data directly, they have not been considered in that mode here. Electron beam systems can also store analog data; in fact, the storage tube is at an advanced stage of development. The prime feature of such a tube is the storage medium which must accumulate charge from the electron beam and retain it. This requires a good dielectric medium with a high surface resistivity. Typically, present day storage tubes use silicon targets with a SiO_2 glass overlay. The storage locations are formed by photolithography and can be made with such good tolerance that the limiting resolution is set by the properties of the electron beam. The resolution is about 1000 lines, the writing time is about 5 μs per scan, the retention time is 10 minutes while being read and a few hundred hours when not being accessed for information. The output current is of the order of a few hundred nA and a gray scale of five levels can be accommodated. Without the power supplies the whole unit occupies about 6 cubic inches. Even for use in space it would have to be placed in an evacuated enclosure since it is essential to test the unit on the ground. Filament lives of a few thousand hours can be expected. The unit would respond well to vibrations, shock, and temperature, but stray fields and radiation might affect it. Since it stores in terms of a gray scale, one tube could store the equivalent of several million bits.

This is not a realistic contender for a replacement for a tape recorder, even one associated with a TV camera, because of the limited storage time, limited capacity per unit and the poor cathode and filament lifetime.

Summary

Although all the technologies reviewed here have been ruled out as contenders for a spaceborne mass memory in 1975, this does not mean that they are of little interest. It seems unlikely that technologies such as cryogenic or acoustical delay lines will find roles in space, at least not for a long time, but some of the other technologies deserve continued close attention because they may well play a significant role in spaceborne data processing systems in the future. The 2.5 mil diameter plated wire is very close to maturity and should be suitable for space data processing within two or three years. It could quite readily be made into a 10 million bit computer mass memory, but it also can play other roles, down to a non-volatile scratch pad memory, in decreasing capacities.

Both types of beam addressable memories have bright futures for really large, greater than 10^9 bit storage systems. They will not reach maturity for some years yet, maybe as many as 10. Their development will continue steadily because at the moment they offer the only chance of random access read/write memories of that capacity. They will be in direct competition with each other, and today it is difficult to predict the eventual winner. Development work in optical systems has continued steadily for many years but there has been a long gap in the development of electron beam systems. However, suddenly there is great interest in electron beam technology again and work has restarted developing memories of this type.

The other technology which is recommended as worthy of further examination is the variable threshold MOS transistor. Electrically alterable read only memories will be available within 12 months using this technology. Further development of true random access memories with all the advantages of IC technology behind them, and non-volatile operation, will continue and small systems of this type may be available in the mid 1970's.

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APPENDIX A

NEW TECHNOLOGY APPENDIX

After a diligent review of the work performed under this contract, no new innovation, discovery, improvement or invention was made.

APPENDIX B

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TRW

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GLOSSARY OF TERMS

FREQUENTLY USED IN THE REPORT

Angel fish:	triangular shaped magnets, see Figure 5.
Asynchronous:	the ability to operate a memory at different data rates
BORAM:	block organized random access memory
Bubble:	a cylindrical magnetic domain
CMOS:	complimentary metal oxide semiconductor transistors used in integrated circuit with both p-type and n-type transistors
Coercive force:	the ability of a magnet to resist attempts to demagnetize it
Curie temperature:	the temperature above which a ferromagnetic material loses its magnetism
Data rate:	the number of bits per second transmitted through a system
Domain:	a local region in a magnetic material which is magnetized inversely with respect to the surrounding material
DRO:	destructive readout, the information in the memory destroyed when it is readout
DTPL:	domain tip propagation logic, a magnetic shift register using a metallic storage medium
Easy axis:	the preferred magnetization direction in a magnetic material
IC:	integrated circuit
k:	suffix indicating 1024 bits of data
MNOS:	metal nitride oxide semiconductor transistor used in integrated circuits
Mobility:	a measure of the ease with which magnetic domains move through a material

MOS:	metal oxide semiconductor transistor used in integrated circuits, either p-type or n-type
MTBF:	mean time between failures of a system
NDRO:	non-destructive readout, data is not destroyed when read from a memory
Neel temperature:	the temperature above which an antiferromagnetic material loses its magnetism
Non-volatile:	data is not lost when the memory power supplies are switched off
pcb:	printed circuit board
RAM:	random access memory, any stored word can be retrieved in a fixed time no matter what the location in the memory
Saturation magnetization:	the maximum possible strength of a magnet
Shift register:	a memory where the access time to a word depends on its position in the memory
Synchronous:	the operation of a memory at a fixed data rate
T-bar:	two magnets, one shaped like a T, the other like a bar, see Figure 4.
2D-2W:	2 dimensional 2 wire, an arrangement of a memory where each data cell is at the intersection of 2 wires in a 2 dimensional matrix
Uniaxial anisotropy:	description of a magnetic material with one easy axis
Volatile:	data is lost when the memory power supplies are switched off
Wire drive:	magnetic fields produced by currents in a wire array, which are used to drive domains through a magnetic shift register

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