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C-MOS ARRAY DESIGN TECHNIQUES

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by A. Feller

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ABSTRACT

A CMOS standard cell test chip has been fabricated and tested. This chip contains most of the logic circuits of the standard cell family.

The results of the extensive testing and evaluation of the fabricated chip confirms that all the objectives and goals of contract NAS12-2233 were successfully accomplished. These successful accomplishments include modification of the C-MOS automatic Placement, Routing, Folding and Artwork design automation computer programs, the design of the basic C-MOS cell and chip topology, the design and validation of the standard cell circuit family, and the integration of all these capabilities into a tool for low-cost and quick-turnaround generation of LSI C-MOS integrated circuit arrays.

PREFACE

Program Objectives

The objectives of this program are to develop and demonstrate the capability of automatically generating precision artwork for complementary MOS (C-MOS) integrated circuit arrays. The program encompasses the following design objectives:

1. Standard cell family - a basic family of standard circuit cells will be designed. Family members include:
   a. Inverter.
   b. Two-, three- and four-input NOR's.
   c. D-type and set-reset flip-flops.
   d. Two-, three- and four-input NAND's.
   e. Transmission and protective devices.
   f. Special process and mask components.
2. Circuit description:
   a. Static logic.
   b. Single supply.
   c. Logic swing - approximately equal to supply.
   d. Speed - a function of the process and the supply voltages. A realistic objective of nominal stage delays of 13 to 16ns with fan-outs of 2.5 loads appears to be obtainable with factory processes expected to be operational at the time chip fabrication is scheduled. This assumes a supply voltage of 10 volts.
3. Computer programs - Four major computer programs will be implemented for the C-MOS technology:
   a. Placement, routing and folding program - This program will provide for the automatic orientation or cell placement, the cell interconnections, and an acceptable form factor.
   b. Artwork program - This program will generate the instruction for an automatic artwork generator to plot the final mask artwork at some acceptable scale.

c. CalComp check plot - This program permits a composite check plot to be generated on a low-cost plotter for checking and optimization reasons.

d. Manual modification program - This program aids in implementing manual modifications when desired.

4. C-MOS standard cell basic system design including:

   a. Cell orientation.

   b. Power distribution.

   c. Low-leakage isolation.

   d. Variable standard cell heights.

   e. Production design rules.

   f. P-type tunnel.

   g. Standard guard band interface height.

   h. Maximum utilization of P-MOS programs.

5. Design of tests and generation of artwork for test chip encompassing:

   a. Static and dynamic evaluation of representative cells.

   b. Test of C-MOS system.

   c. Evaluation of programs.

   d. Determination of process and device parameters.

   e. Correlation.

6. Design criteria - The selection of the device geometries and therefore the standard cell height will reflect tradeoffs which consider the following:

   a. Design rules that are compatible with factory and production standards. This decision is based on insuring as reliable a device as possible since production standards are based on exhaustive preproduction evaluation and conservative quality control.

   b. Process parameters and characteristics either now in production or soon to be. Introduction of processes having significantly reduced threshold voltages and lower doping levels promise to deliver significant improvements in performance.

   c. Increased gate density.

   d. Chip dimension compatible with good yield.

   e. Compatibility with computer programs.

   f. Low power.

   g. Competitive speeds.

Scope of Work

The scope of this program has combined the various technologies and computer programs required to automatically produce artwork for complex functional C-MOS integrated circuit arrays starting with partitioned logic.

Included in this program scope were the following:

1. The definition of a group of logic cells for the basic standard cell family
2. The circuit design and layout of the standard cells
3. The computer circuit simulation of the performance of the cell family and the correlation of these simulation techniques by experimental verifications
4. The conceptional design and implementation of the CMOS array or chip layout that considers systems, logic, partitioning requirements, electrical packaging considerations, mask generations, processing and fabrication constraints
5. Development of a series of computer programs that includes the automatic Placement, Routing and Folding programs, the Artwork generation program for the Gerber automatic plotter, a Manual Modification program, and Programs to drive local, laboratory plotters
6. The design, fabrication, test and the evaluation of a C-MOS Standard Cell Test Chip which provided experimental validation and evaluation of the computer programs, the circuit design and layouts, and the chip design and layout.

Conclusions

All the objectives and goals of this program have been successfully achieved within the cost budget and time schedule. These measurable results were obtained from the first C-MOS Standard Cell Test Chip designed, fabricated and evaluated as part of this program. The evaluation of this test chip validated the algorithm and coding of the C-MOS Placement, Routing, Folding and the Artwork programs, the design and layout of the standard cell family, and the design and layout of the C-MOS standard cell array.

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INTRODUCTION

As part of a program change of scope, approved by the program technical monitor of MSFC, this quarterly report will serve as a final report. In accordance with the conditions of this approved change of scope, this report will include fourth quarter progress and documentation of the changes and modifications made in the various computer programs. Specifically this report includes:

(1) Detailed description of the additions, changes and modifications made to the Placement, Routing, Folding (PRF) program. The description includes all relevant data and parameter changes that are required to update the PRF programmers and users manuals.

(2) Description of new standard cells. The inclusion of the Set-Reset Flip-Flop into the standard Cell Library completes the Standard Cell Library as required by the terms of the contract. Thus the combined standard cell descriptions found in this final and Quarterly Report No. 2 (period from March 15 to June 15, 1970) provide a complete set of documented standard cell data sheets to aid logic and system designers in applying standard cells to a particular logic design.

(3) Description of the C-MOS Standard Cell Test Chip and details of fabrication, testing, and evaluation of the chip.

(4) Overall Standard Cell circuit performance and system implication.

(5) New application and performance areas of C-MOS standard cell technology.

(6) Conclusions.

Section II

COMPUTER PROGRAM

Modifications, changes, additions, and improvements were made to the P-MOS Placement, Routing, and Folding (PRF) program to adapt it to the C-MOS technology. These changes include:

(1) Extensive changes to the RNMAIN routine to include the restart feature.

(2) Changes to the INPUT subroutine to preset input parameters and enable changes to these preset values. Addition of new parameters for the C-MOS technology.

(3) Modifications to the ARTWRK and POWR subroutines to:

   (a) Automatically generate all standard (non-cell) patterns, such as chip alignment keys, test transistors, and photo alignment keys.

   (b) Automatically generate chip borders for all seven levels.

   (c) Automatically generate "SYMBOL" data for each level of artwork.

   (d) Automatically leave room for input/output pads on the left side of the chip.

(4) Addition of the RIGHT and REED subroutines to write common data on and to read common data from magnetic tape. These subroutines are used in the restart feature.

(5) Addition of the MANMOD subroutine to be used for manual modifications.

Descriptions of these changes, modifications, additions, and improvements are included in this section. Also, the data input requirements are discussed and the data format is itemized to serve to update both the programmers manual and, more specifically, the users manual.

No changes to the ARTWRK program were required.

A. RNMAIN EXECUTIVE ROUTINE

The RNMAIN executive routine controls the execution of the PRF program.

1. Restart Feature

The restart feature is a technique to enable the user to exercise the PRF program in a "serial step" mode. This feature uses the RIGHT and REED subroutines to write and read, respectively, data in common to and from temporary storage on magnetic tape. This magnetic tape has a header which contains two locks. These locks will prevent incorrect use of the common data tape and the PRF program. The restart feature can only be exercised when the proper keys have been specified. At any point specified by the user, the program can be temporarily stopped. The user can then examine the results of the run to that point. The user could then continue the normal execution of the PRF program with or without minor modification to the data in common or he could reexecute previous levels of the program with or without minor modification to the data in common.

2. Restart Parameters

The first step in any run of the PRF program is to read the restart parameters. These parameters control the mode of execution of the PRF program. The restart parameters are JSTART, JMID, JPRINT, KIN, and KOUT.

a. JSTART

JSTART is used to specify which subroutine of the PRF program will be the first to be executed.

JSTART is also used as an error stop switch. After execution of any subroutine, except MANMOD, the program will automatically stop execution if JSTART has been internally set to a value of 6. If JSTART has been read in as a value of 2, 3, 4 or 5, the program will automatically exercise the restart feature by reading in the

data stored on the restart tape. After completion of reading in these data, the program will automatically start execution of the subroutine specified by JSTART.

Whenever the PRF program has been restarted, JSTART is also used as a key to allow acceptance of the data from the restart tape. This key is described in detail in the writeups on the RIGHT and REED subroutines.

When JSTART has been read in as a value of 6, the PRF program will only execute the MANMOD subroutine.

b. JMID

JMID is used to specify the number which has been assigned to the chip being designed. Whenever the PRF program is in the restart mode, JMID is also used as a key to allow acceptance of the data from the restart tape. This key is described in detail in the writeups on the RIGHT and REED subroutines. This chip identification parameter, JMID, will automatically be part of the symbol data generated in artwork instruction output of the PRF program.

c. JEND

JEND is used to specify which subroutine of the PRF program will be the last to be executed.

If JEND has been read in as a value of 1, 2, 3, or 4, the program will automatically exercise the restart feature by writing all common data to the restart tape (after completion of the last subroutine to be executed).

If JEND is read in as a value of 6, the program will print common data, after completion of the ARTWRK subroutine.

Whenever the restart feature has been selected, JEND is also used as a key to prevent incorrect restart of the PRF program. This key is described in detail in the RIGHT and REED subroutine writeups.

JEND is not used when the MANMOD subroutine is exercised.

d. JPRINT

JPRINT is used as a print control for debugging purposes in the RIGHT, REED and MANMOD subroutines. See the detailed descriptions of these subroutines for the explanation of the use of the restart parameter JPRINT.

e. KIN and KOUT

KIN and KOUT are input and output device specifications for the MANMOD subroutine. See the detailed writeup for the MANMOD subroutine for detailed descriptions of these parameters.

B. PRF SUBROUTINES

1. RIGHT

The RIGHT subroutine is part of the restart technique used in the PRF program. This subroutine provides intermediate storage on magnetic tape of all data which are in common in the PRF program. The RIGHT subroutine will be exercised when the restart parameter "JEND" is greater than 0 and less than 6. This subroutine will write a header to the output magnetic tape which will be used as a double lock to prevent incorrect use of the magnetic tape. The first lock is the chip identification number. This number is the restart parameter "JMID". This lock will prevent incorrect use of the magnetic tape. The second lock is the restart parameter "JEND" which will prevent the user from restarting the PRF program at the incorrect point.

The restart parameter "JPRINT" is used as a debug parameter. If JPRINT = 2, or 3, this subroutine will print all PRF common data. These data are very useful for both debugging the PRF program and to aid in the design of the chip.

2. REED

The REED subroutine is also a part of the restart technique used in the PRF program. Its purpose is to recover the data temporarily stored on magnetic tape. The data on the magnetic tape is all data which are in common in the PRF program. The REED subroutine will be exercised when the restart parameter "JSTART" is greater than 1 and less than 6. This subroutine has been provided with a double lock to prevent improper execution of the PRF program. The first lock is the chip identification number, the restart parameter "JMID". This lock will prevent using the wrong restart tape when more than one chip is being designed. The second lock is the stop level of the restart tape. When the restart feature has been previously exercised, the stopping code "JEND" has been written to the header of the restart tape. The present attempt to restart the PRF program will have the restart parameter "JSTART" specified. If JSTART is not exactly one greater than the JEND stored on the restart tape, this subroutine will terminate the restart attempt, thus preventing improper use of the PRF program.

The restart parameter "JPRINT" is used as a debug parameter. If JPRINT = 1 or 2, the subroutine will print all PRF common data. These data can then be used for debugging the PRF program or to aid in the design of the chip.

In this subroutine, the user has the option of changing any of the data contained in any integer arrays. This option is a very powerful aid to the user. It allows the user to exercise a portion of the PRF program. When the PRF has been restarted, the user can modify any data in common and thereby control the final layout of the chip and not have to reexecute the previous sections of the PRF program. For example, it is possible to change one or more of the input parameters so that the chip design can be modified before generation of the artwork instruction data. This could preclude the necessity for extensive manual modifications. Each array has been assigned an index number. In order to exercise the change-of-data option the user must specify the array name or the array index number as well as the variable location index number within the array.

The array index number and the variable location index number (from one to three indices) of the location of the data within that array will specify the storage area to be changed. That data will be changed to the value specified in the modification data. To facilitate the usefulness of this option, the program has been implemented with automatic array index specification. This is accomplished by specification of the array name rather than the array index number. The program will convert the name to the index number.

3. MANMOD

The purpose of the MANMOD subroutine is to enable the user to modify the artwork instructions output of the PRF program. These modifications may be required due to changes in the logic design, desired changes of the physical layout of the chip, or wiring problems on the chip. For instance, the user may wish to relocate the chip input/output bonding pads.

This subroutine will accept either the artwork instructions previously generated by the PRF program or the artwork instructions previously modified by the MANMOD subroutine. These input data may be either from data cards (KIN = 5) or from magnetic tape (KIN = 11). The subroutine will accept the modification data and implement the design changes. For preparation of these modification data, see the detailed description of input data section. After completion of all modifications, the subroutine will generate a new artwork instruction data set. This output can either be to data card (KOUT = 7) or to magnetic tape (KOUT = 12). This subroutine can only be exercised by specifying the restart parameter, JSTART as a value of 6.

The artwork instruction input data will be decoded and stored in the IDATA (I, J) array. The index "I" is used as a sequential index on the input data and will correspond to the sequence number printed with the artwork instructions (see Figure 1). The index "J" is used to locate pertinent data for each sequence number "I". The meanings for the values of index "J" are presented in Table 1.

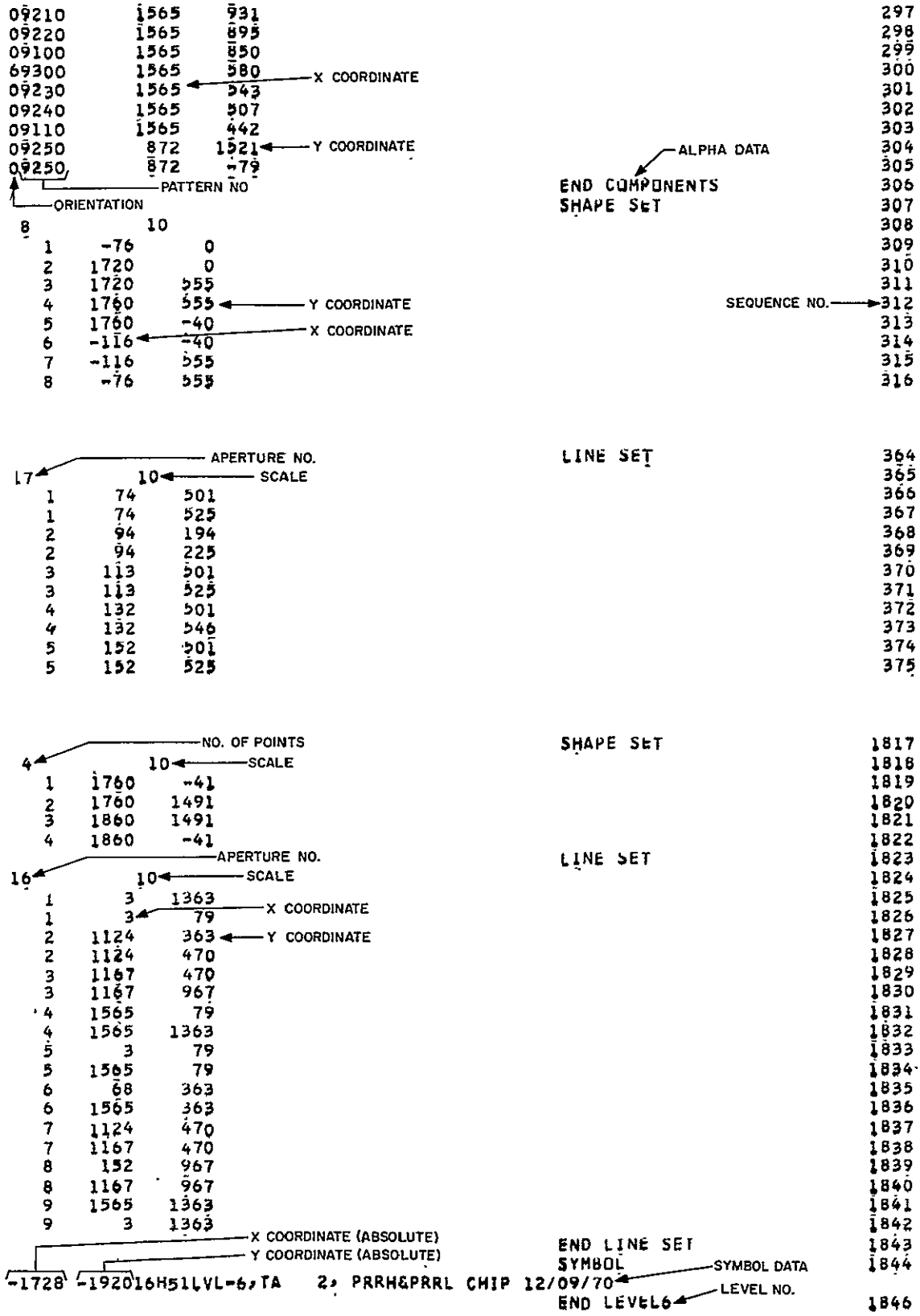


Figure 1. Samples of Artwork Instructions

TABLE 1. MEANINGS ASSIGNED TO INDEX "J"

Value of J	Meaning
1	Forward Index Number. "I" index of next data in artwork instructions.
2	Reverse Index number. "I" index of previous data in artwork instructions.
3	X-coordinate (or the number of points for shape set or the aperture number for line set).
4	Y-coordinate (or the scale factor for shape set or line set).
5	Data code (or pattern number of component).
6	Pattern orientation for components.

The data code stored in J = 5 is used to differentiate each of the various types of data. These data codes are listed in Table 2.

TABLE 2. DATA CODES STORED IN "J = 5"

Name	Value	Meaning
KODE1	1	Component coordinate data*
KODE2	2	Shape Set coordinate data
KODE3	3	Time Set coordinate data
KODE4	4	Symbol coordinate data
KODE5	5	Shape Set number of points and scale
KODE6	6	Line Set Aperture number and scale
KODE11	10	"End components"
KODE12	20	"Shape Set"
KODE13	30	"Line Set"
KODE14	40	"End Line Set"
KODE15	50	"Symbol"
KODE16	60	"End Level"

*The component pattern number is actually stored in memory, rather than this code value. This restricts pattern numbers to be 70 or greater.

After the subroutine has completed reading the input data, the modification portion of the subroutine will automatically be exercised. This section of coding is controlled by the variable "Type" (see detailed description of input data) read in as part of the modification data. When data are changed ("Type" = "C" or "CHG") the user has the option of indicating the data which are being replaced (old data). If so indicated, the program will verify that the old data matches before making the specified changes. If these data do not match, the program will reject the modification. When a Line Set (or Shape Set) is added, it is the users responsibility to specify that this addition is at a point in the data such that all data sets (line sets or shape sets) are complete and correct. The user is also required to correctly specify the correct number of points and scale for Shape Sets and the correct aperture number and scale for Line Sets. When a delete Line Set or a delete Shape Set has been specified, the program will verify that the specified sequence number corresponds to the start of the Line Set or Shape Set. If this test fails, the program will disregard the specified modification command. When the user has specified a Shift command, the program will automatically shift all X and Y coordinate data within the rectangle specified in the shift data by the ΔX and ΔY increment. The user is cautioned to exercise reasonable care when exercising this option.

After the last modification has been implemented, the program will automatically enter the output data section of the subroutine.

The output data generation section will decode the data stored in IDATA (I, 5) matrix and write the properly formatted network artwork instructions to the output media. These data will also be printed. Each line of the data (except symbol data) will contain a sequence number which is required when any additional modifications are to be implemented. The program will automatically check that each Line Set has coordinate data that are paired and that the number of points in each Shape Set corresponds to the specified number of points for that Shape Set.

The restart parameter "JPRINT" is used in this subroutine as a debug printing parameter. If JPRINT = 1, or 2, the IDATA (I, J) array will be printed after the input data has been read into storage. If JPRINT = 2 or 3, the IDATA (I, J) array will be printed after the modifications have been completed.

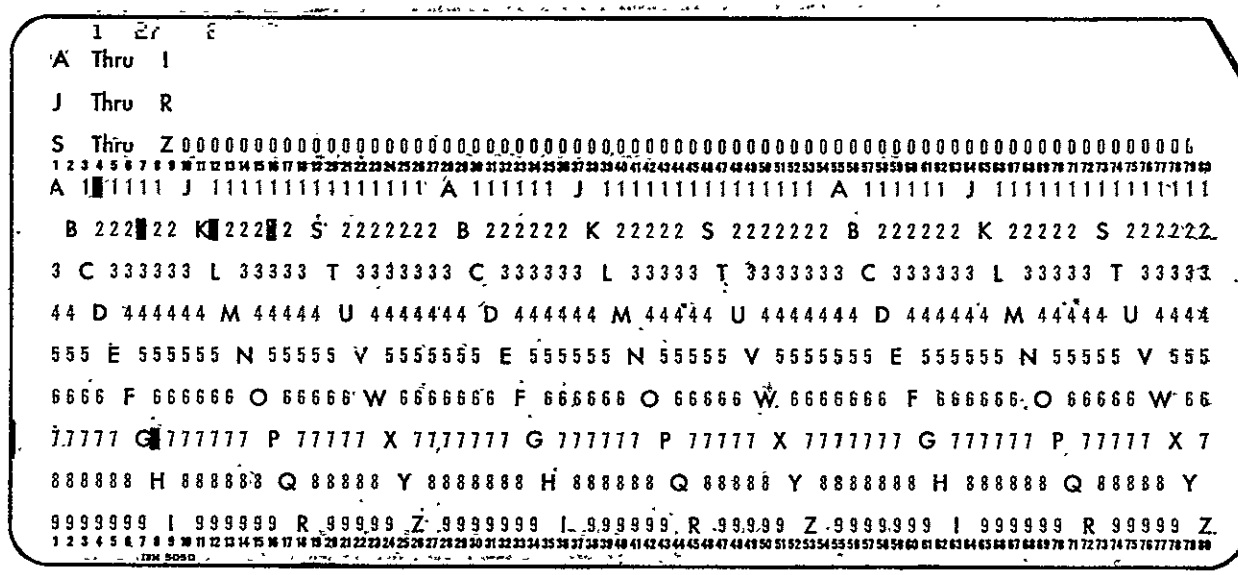
C. DESCRIPTIONS OF INPUT DATA TO PRF PROGRAM

1. Restart Parameters

Purpose: The purpose of the restart parameters is to control the mode of execution of the PRF program.

Card Format: (18I4)

Card as It May Appear:



Coded Breakdown: All fields are right justified integer fields

Field A, Columns 1-4; JSTART

JSTART is used to specify which subroutine of the PRF program will be the first to be executed.

JSTART=	Start Execution at Subroutine
1	INPUT
2	PLACE
3	ROUTE
4	"FOLD"
5	ARTWRK
6	MANMOD

Field B, Columns 5-8, JMD

JMID is the chip identification number. This number will be part of the symbol data written below the chip artwork.

Field C, Columns 9-12, JEND

JEND is used to specify which subroutine of the PRF program will be the last to be executed.

JEND=	Stop Execution After Subroutine
1	INPUT
2	PLACE
3	ROUTE
4	"FOLD"
5	ARTWRK
6	ARTWRK

Field D, Columns 13-16, JPRINT

JPRINT is a debug print control for RIGHT and REED subroutines and also for the MANMOD subroutine.

JPRINT	SUBROUTINE	PRINT OPTION
0	ALL	Do Not Print
=1	MANMOD	Print IDATA (I, J) before manual modifications

JPRINT	SUBROUTINE	PRINT OPTION
=1	REED	Print Common Data
=1	RIGHT	Do Not Print
=2	MANMOD	Print IDATA (I, J) before and after manual modifications
=2	REED	Print Common Data
=2	RIGHT	Print Common Data
=3	MANMOD	Print IDATA (I, J) after manual modifications
=3	REED	Do Not Print
=3	RIGHT	Print Common Data
≥4	ALL	Do Not Print

Field E, Columns 17-20; KIN

KIN is the input data set reference number to read the artwork instructions in the MANMOD subroutine.

KIN	Artwork Instructions
<0	From cards
5	From cards
>0 & ≠5	From magnetic tape (KIN set = 11)

Field F, Columns 21-24; KOUT

KOUT is the output data set reference number to write artwork instructions in the MANMOD subroutine.

KOUT	Artwork Instructions
< 0	To cards
7	To cards
>0 & ≠ 7	To magnetic tape (KOUT Set=12)

Note:

The input subroutine has been programmed to preset each parameter (except M1) to a "Standard" value. The user may accept the standard values by leaving each field of each parameter card (except the first field of the first parameter card) blank (or zero). If the user wishes to change the value preset within the program, he should enter the desired value in the proper location of the proper parameter data card. The program will use the new value in place of the standard value for that parameter.

The preset value of the parameters are:

Parameter	Preset Value
M1	Not Preset
LEN	0
LIMINT	3
IHF	144
IBR	1
IBF	1
IBP	0
IBP1	1
IBPA	1
IDP	4
IDBG	1
NWRK	12
NAR	11
IPAD	9020
ICN (1)	22
ICN (2)	0
ICN (3)	2
ICN (4)	100

Parameter	Preset Value
ICN (5)	670
(6)	32
(7)	64
(8)	1260
(9)	1000
(10)	560
(11)	-560
(12)	-1
(13)	0
(14)	72
(15)	7
(16)	18
(17)	9
(18)	8
(19)	-1
(20)	6
(21)	9500
(22)	17
(23)	16
(24)	0
(25)	0
(26)	0
(27)	0
(28)	10
(29)	0
(30)	0
(31)	0
(32)	16
ICN (33)	70

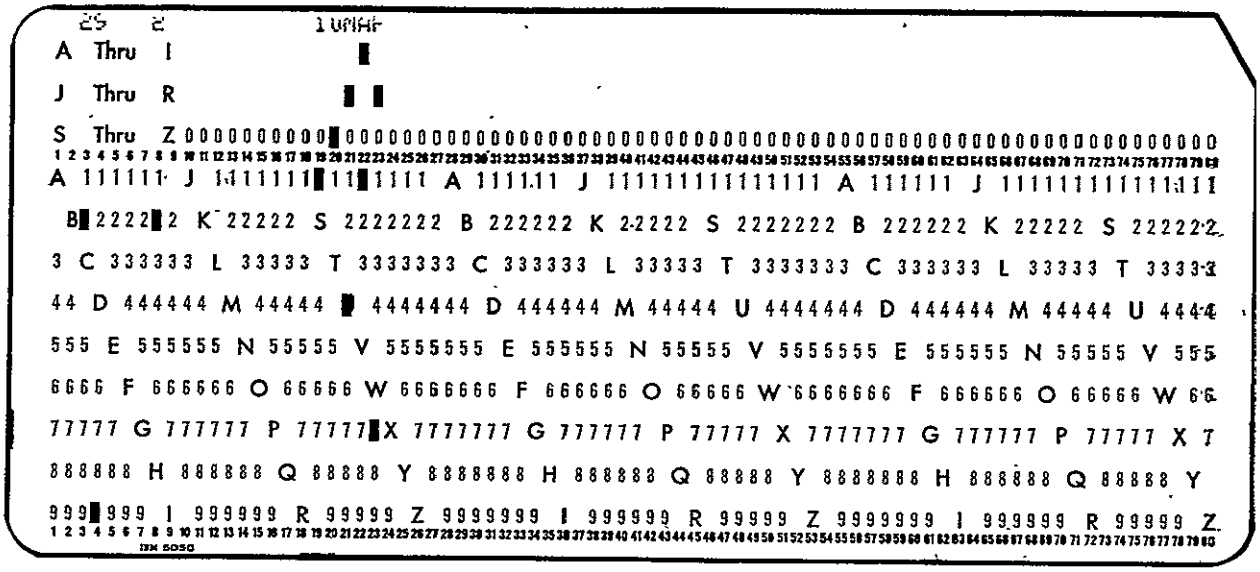
Parameter	Preset Value
ICN (34)	0
(35)	0
(36)	0
(37)	0
(38)	0
(39)	0
(40)	0
(41)	0
(42)	0
(43)	0
(44)	0
(45)	2
(46)	0
(47)	0
(48)	9100
(49)	9110
(50)	61
(51)	0
(52)	0
(53)	0
(54)	0
(55)	4
(56)	0
(57)	0
(58)	3
(59)	0
(60)	0
(61)	9510
ICN (62)	0

Parameter	Preset Value
ICN (63)	0
(64)	0
(65)	39
(66)	39
(67)	4
(68)	100
(69)	40
(70)	0
(71)	4
(72)	7
(73)	19
(74)	56
(75)	140
(76)	0
(77)	0
(78)	0
(79)	9400
(80)	9210
(81)	9300
(82)	0
(83)	9600
(84)	9250
(85)	1300
(86)	76
ICN (87)	80

2. Input Data for Common Data Modifications

Purpose: The purpose of the common data modification data is to selectively change the common data when the restart feature is being exercised. The user should not attempt to change a large portion of these common data. This feature should be used to change a spacing parameter, a pattern assignment, a switch or some other simple variable.

Card as it May Appear:



Format: (5I4, A4)

Coded Breakdown:

Field A, columns 1-4; LL1

LL1 is the first index of the array being changed.

Field B, columns 5-8; LL2.

LL2 is the second index of the array being changed.

Field C, columns 9-12; LL3

LL3 is the third index of the array being changed.

Field D, columns 13-16; LL4

LL4 is the index number assigned to each array in common.

Field E, columns 17-20; LL5

LL5 are data to be entered in place of old data.

Field F, columns 21-24, ALPHA

ALPHA is the first four letters of the array name (left justified).

Notes:

1. LL1, LL2 and LL3 (when required for the specific array being changed) must be greater than zero and less than or equal to the maximum index of the array.

2. Either LL4 or ALPHA is required in order to determine the specific array being changed. If ALPHA is given, the program will automatically determine the correct value of LL4. The following table shows the arrays in common, their assigned index number, the ALPHA variable and the upper limit of all applicable indices.

Array	LL4	ALPHA	LL1	LL2	LL3
IC (I, J)	1	IC	200	10	NA
ICK (I, J, K)	2	ICK	120	10	NA
ICL (I, J)	3	ICL	120	6	NA
ICN (I)	4	ICN	200	NA	NA
IEC (I)	5	IEC	200	NA	NA
IEZ (I)	6	IEZ	200	NA	NA
IF (I, J)	7	IF	10	4	NA
IFA (I, J)	8	IFA	200	200	NA

Array	LL4	ALPHA	LL1	LL2	LL3
INF (I, J)	9	INF	200	4	NA
INL (I)	10	INL	200	NA	NA
INT (I)	11	INT	6	NA	NA
IP (I, J)	12	IP	200	2	NA
IPR (I)	13	IPR	250	NA	NA
IPTRN (I)	14	IPTR	120	NA	NA
IRA (I, J)	15	IRA	800	50	NA
IXW (I)	16	IXW	35	NA	NA
IYW (I)	17	IYW	200	NA	NA
IZ (I)	18	IZ	200	NA	NA
JD (I)	19	JD	2	NA	NA
LIMIT (I)	20	LIMI	50	NA	NA
LNAD (I)	21	LNAD	1,000	NA	NA
MAP (I, J)	22	MAP	200	2	NA
NC (I, J)	23	NC	600	5	NA
NET (I)	24	NET	2,000	NA	NA
NETTOT (I)	25	NETT	200	NA	NA
NOUT (I, J)	26	NOUT	200	3	NA
NX (I, J)	27	NX	200	3	NA

3. Changes to the data in common will automatically stop when no further changes are required.

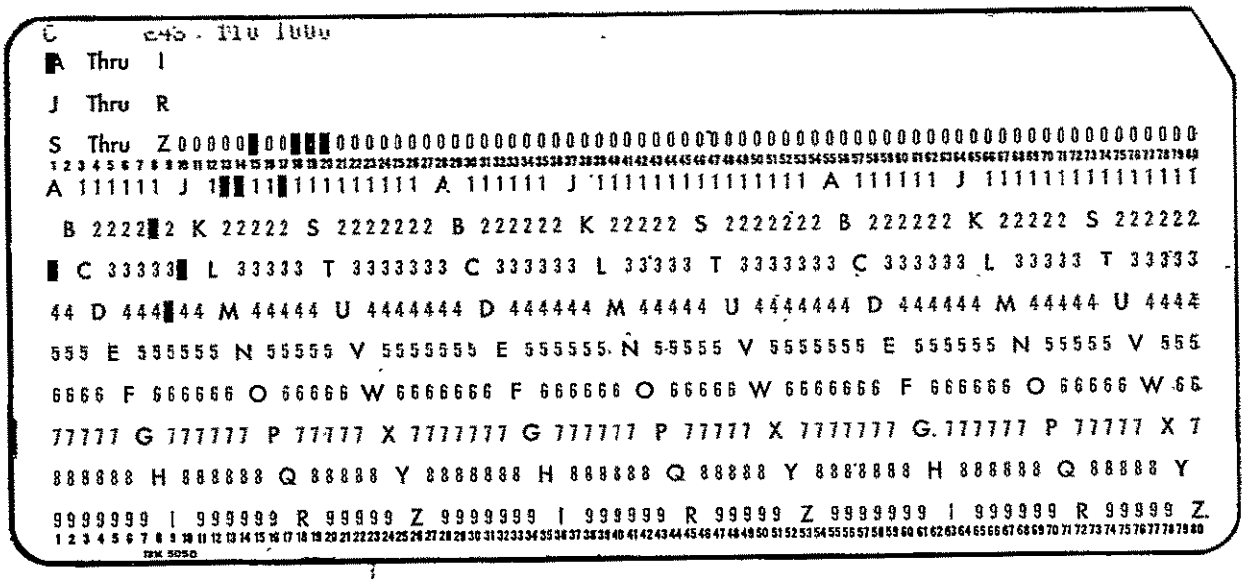
4. If a value of 100 (or greater) is entered for LL4, the program will automatically terminate making changes to the data in common. This feature will enable the user to have data cards for other purposes in the PRF program behind these changes.

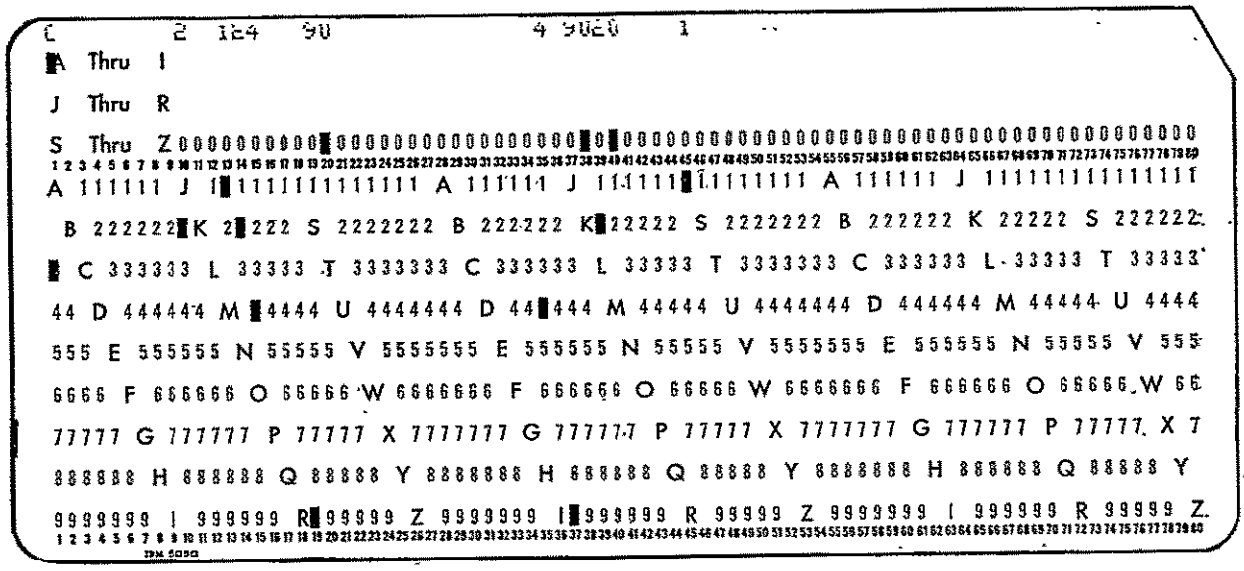
3. MANMOD Input Data

Purpose: The purpose of these data cards is to implement modifications to the artwork instruction data.

Card Format: (A3, 2X, 8I5)

Cards as They May Appear:





Coded Breakdown: Field A is a left justified alpha field. All other fields are right justified integer fields.

Field A, Columns 1-3; TYPE

TYPE is used to specify which type of modification is being made. The variable TYPE can be equal to any one of the following values:

TYPE=	Meaning
A	Add data after specified sequence number.
ADD	Add data after specified sequence number.
ALS	Add Line Set after specified sequence number.
ASS	Add Shape Set after specified sequence number.
ASY	Add symbol command and symbol data after specified sequence number.
C	Change data at specified sequence number.
CHG	Change data at specified sequence number.
CSY	Change symbol data at sequence number.
D	Delete data at specified sequence number.
DEL	Delete data at specified sequence number.
DLS	Delete Line Set starting with specified sequence number.
DSS	Delete Shape Set starting with specified sequence number.
DSY	Delete symbol command and symbol data starting at sequence number.
S	Shift those coordinate data which are within the specified rectangle by the specified X/Y increment.
SHF	Shift those coordinate data which are within the specified rectangle by the specified X/Y increment.

Notes:

A or ADD

If TYPE = "A" or "ADD", the user may add any data at any point in the artwork instructions. It is the user's responsibility to add the correct data type at the correct position. The data added after the specified sequence number will be:

For	IXNEW	IYNEW	IDX	IDY	KODE*
Components	X-Coord.	Y-Coord.	Orientation	Pattern No.	1
Shape Set #Pts. & Scale	No. of Points in Set	Scale	N/A	N/A	5
Line Set Apt. # & Scale	Aperture No.	Scale	N/A	N/A	6
Other Data	X-Coord.	Y-Coord.	N/A	N/A	*

ALS

If TYPE = "ALS", the user must start the add at a sequence number so that all data will remain self consistent. He must not, for example, add a line set in the middle of a shape set or the components, etc. The IXNEW variable must contain the aperture number of this new line set. The IYNEW variable must contain the scale of this new line set and the variable IDX must be the exact number of points in this line set. (IDX = twice number of lines in set). All points in the line set must follow the "ALS" data card. These data cards will contain the X and Y coordinates of the points in the IXNEW and IYNEW data fields.

ASS

If TYPE = "ASS", the user must start the add at a sequence number so that all data will remain self consistent. For example, a shape set must not be added in the middle of a line set of the components, etc.

*See description of KODE for further requirements during an add modification.

The IXNEW variable must contain the exact number of points in the shape set. The variable IYNEW must contain the scale of this new shape set. All points in the shape set must follow the "ASS" data card. These data cards that follow the "ASS" card will contain the X and Y coordinates of the points in the IXNEW and IYNEW data fields.

ASY

If TYPE = "ASY", the user must start the add at a sequence number so that all data will remain self consistent. Symbol data must not be added in the middle of a line set or shape set. Symbol data must be located just before an end level instruction. The variable IDX should contain the artwork level number at which the symbol data are added. If this data are added just before the end level instruction and no data are entered for IDX, the program will extract the level number from the end level instruction. Following the ASY data, the alpha data required for the symbol data must be entered using a format of (17A4). These alpha data must contain the information specified on page 29 of the "User's Manual for the Artwork Program" as well as any alpha data required by the user.

C or CHG

If TYPE= "C" or "CHG", the data may be changed at any point in the artwork instructions. It is the user's responsibility to maintain the artwork instruction in a self consistent arrangement. The data will be changed in the same organization shown for the A or ADD type. If non-zero data has been entered in the IXOLD (or IYOLD) field, the program will validate the IXOLD (or IYOLD) data against the old X-coordinate (or Y-coordinate) data stored in IDATA (I, J) before making any changes. If this test fails, the program will point an error condition and not execute the change of data. See description of KODE for further requirements during a change modification.

CSY

If TYPE="CSY", the user must specify the exact sequence number where these symbol data are stored or the program will abort this modification. The variable IDX may contain the artwork level number at which these symbol data are located. Since the symbol data are located just before the end level instruction and when no data are entered for IDX, the program will extract the level number from the end level instruction.

Following the CSY data, the user must enter the alpha data required for the symbol data using a format (17A4). These alpha data must contain the information specified on page 29 of the "User's manual for the Artwork Program" as well as any alpha data required by the user.

D or DEL

If TYPE="D" or "DEL", the user may delete any data in the artwork instructions as specified by the data sequence number ISEQ. It is the users responsibility to maintain a self consistent set of artwork instructions. When any data other than X/Y coordinates are deleted, the program will print a warning to the user. If the user has entered non-zero data in the IXOLD (or IYOLD) field, the program will validate the IXOLD (or IYOLD) data against the old X-coordinate (or Y-coordinate) data stored in IDATA (I, J) before making any changes. If this test fails, the program will print an error condition and not execute the deletion of data.

DLS

If TYPE="DLS", the user must specify the exact sequence number of the "Line Set" instruction. That is, the deletion of a line set must start at the beginning of the line set. When this type of modification has been specified, the complete line set will be deleted.

DSS

If TYPE="DSS", the user must specify the exact sequence number of the "Shape Set" instruction. That is, the deletion of a shape set must start

at the beginning of the Shape Set. When this type of modification has been specified, the subroutine will delete the "Shape Set" instruction, the number of points and scale and the number of X/Y coordinates specified by the number of points in the shape set. Therefore, the user should make sure that the number of points in the shape set exactly corresponds to the number of points specified in the data.

DSY

If TYPE="DSY" the user must specify the exact sequence number of the "symbol" instruction. That is, the deletion of symbol data must start at the beginning of the symbol instruction. When properly specified the program will delete both the "symbol" instruction and the symbol data.

S or SHF

If TYPE="S" or "SHF" the user may shift any X/Y coordinate data by a specified increment. Only those data within the rectangle specified by IXNEW, IYNEW, IXOLD, and IYOLD (inclusive) will be shifted, where:

IXNEW = Minimum X value of rectangle

IYNEW = Minimum Y value of rectangle

IXOLD = Maximum X value of rectangle

IYOLD = Maximum Y value of rectangle.

If the X and Y coordinates of any data are within the prescribed limits, the program will shift the X coordinate by the increment specified by IDX and the Y coordinate by the increment specified by IDY.

Field B, Columns 6-10, ISEQ

ISEQ is used to specify the sequence number of the artwork instruction data which is to be modified. This sequence number must correspond to the sequence number printed with each artwork instruction. The user must use the correct artwork instructions listing corresponding to the input data to the MANMOD subroutine.

Note: The following sequence number should be used for each specified type of modification.

FOR TYPE=	Use Sequence Number of
A or ADD	Data to add after
ALS	Last data of shape set, line set or components
ASS	Last data of shape set, line set, or components
ASY	Data before end level
C or CHG	Data to be changed
CSY	Symbol alpha data
D or DEL	Data to be deleted
DLS	"Line Set" instruction data
DSS	"Shape Set" instruction data
DSY	"Symbol" instruction data
S or SHF	Not used

For data following ALS (or ASS), which are part of the added line set (shape set), sequence numbers are not required.

Field C, Columns 11-15; IXNEW

IXNEW is used as follows:

For Type	IXNEW is
A or ADD	New X-coordinate data, number of points for shape set or aperture number for line set.
ALS	Aperture number of line set on first data card of modification. Successive data cards are X-coordinates.
ASY	X-coordinate of symbol data
C or CHG	New X-coordinate of data, number of points for shape set or aperture number for line set.
CSY	Not used
D orDEL	Not used

For Type	IXNEW is
DLS	Not used
DSS	Not used
DSY	Not used
S or SHF	Minimum X value of shift rectangle

Field D, Columns 16-20, IYNEW

IYNEW is used as shown in the table in IXNEW making the following changes:

From	To
X-Coordinate	Y-Coordinate
Number of point in shape set	Scale of shape set
Aperture number of line set	Scale of line set
Minimum X	Minimum Y
Maximum X	Maximum Y

Field E, Columns 21-25; IXOLD

IXOLD is used as follows:

For TYPE	IXOLD is
A or ADD	Not used
ALS	Not used
ASS	Not used
ASY	X-coordinate of symbol data
C or CHG	X-coordinate data, number of points in shape set or aperture number in line set before modification. If non zero, program will validate old data equality prior to modifications.
CSY	Not used
D or DEL	Same as for change
DLS	Not used
DSS	Not used
DSY	Not used
S or SHF	Maximum X value of shift rectangle

Field F, Columns 26-30; IYOLD

IYOLD is used as shown in the table for IXOLD with the changes shown in the table for IYNEW.

Field G, Columns 31-35; IDX

IDX and IDY are used as follows:

For TYPE	IDX is	IDY is
A or ADD	Pattern orientation for component modifications	Pattern number for component modifications
ALS	Number of points (cards to follow) in Line Set.	Not used
ASS	Not used	Not used
ASY	Not used	Not used
C or CHG	Same as for A or ADD	Same as for A or ADD
CSY	Level number of symbol data, can be zero for automatic level determination if end level instruction follows.	Not used
D or DEL	Not used	Not used
DLS	Not used	Not used
DSS	Not used	Not used
DSY	Not used	Not used
S or SHF	X increment of shift	Y increment of shift

Field H, Columns 36-40; IDY

See Field G.

Field I, Columns 41-45; KODE

KODE data are only used for A, ADD, C, and CHG and are used as follows:

KODE=	Generated Code in IDATA (I, 5)
0	Use same code as specified in IDATA (ISEQ, 5)
> KODE1(=1)	Use IDATA (I, 5) = KODE
= KODE1(=1)	Generate pattern number and orientation for IDX and IDY card store as required.
<0	Same as KODE = KODE1

Section III

ANDARD CELL FAMILY

The addition of the set-reset flip-flop cell (No. 1420) completes the Standard Cell Family as required. The engineering data sheet for general design purposes is presented in Figure 2. This cell data sheet, plus the data sheets found on pages 5-17 of Quarterly Report No. 2 (for cells Nos. 1110, 1120, 1130, 1140, 1220, 1230, 1240, 1260, 1270, 1280, 1290, and 1310) provide a complete set of engineering data for the working logic cell complement of the Standard Cell Family. The topological layout of the set-reset flip-flop cell is shown in Figure 3.

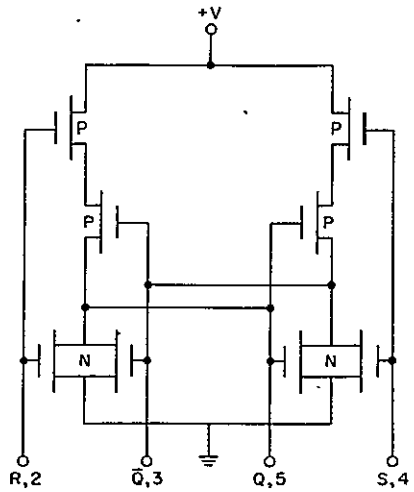
A complete list of the entire cell family, including both the logic and non-logic (functional) cells, is shown in Figure 4.

C-MOS STANDARD CELL

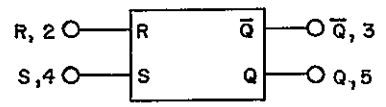
SET-RESET FLIP-FLOP

CELL NO. 1420

SCHEMATIC



LOGIC SYMBOL



LOGIC EQUATION

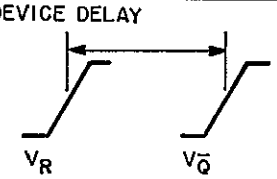
TRUTH TABLE

R	S	Q	$\bar{Q}$
0	0	Q	$\bar{Q}$
0	1	1	0
1	0	0	1
1	1	0	0

CELL I/O CAPACITANCE VALUES

PIN	CAPACITANCE (pF)
2	1.30
3	0.87
4	1.30
5	0.96

DYNAMIC ELECTRICAL CHARACTERISTICS*

CHARACTERISTIC	TIME (ns)
DEVICE DELAY 	50 TO 80
MINIMUM PULSE WIDTH	80

*C_L = 6.0 pF

Figure 2. Data for Set-Reset Flip-Flop Cell No. 1420

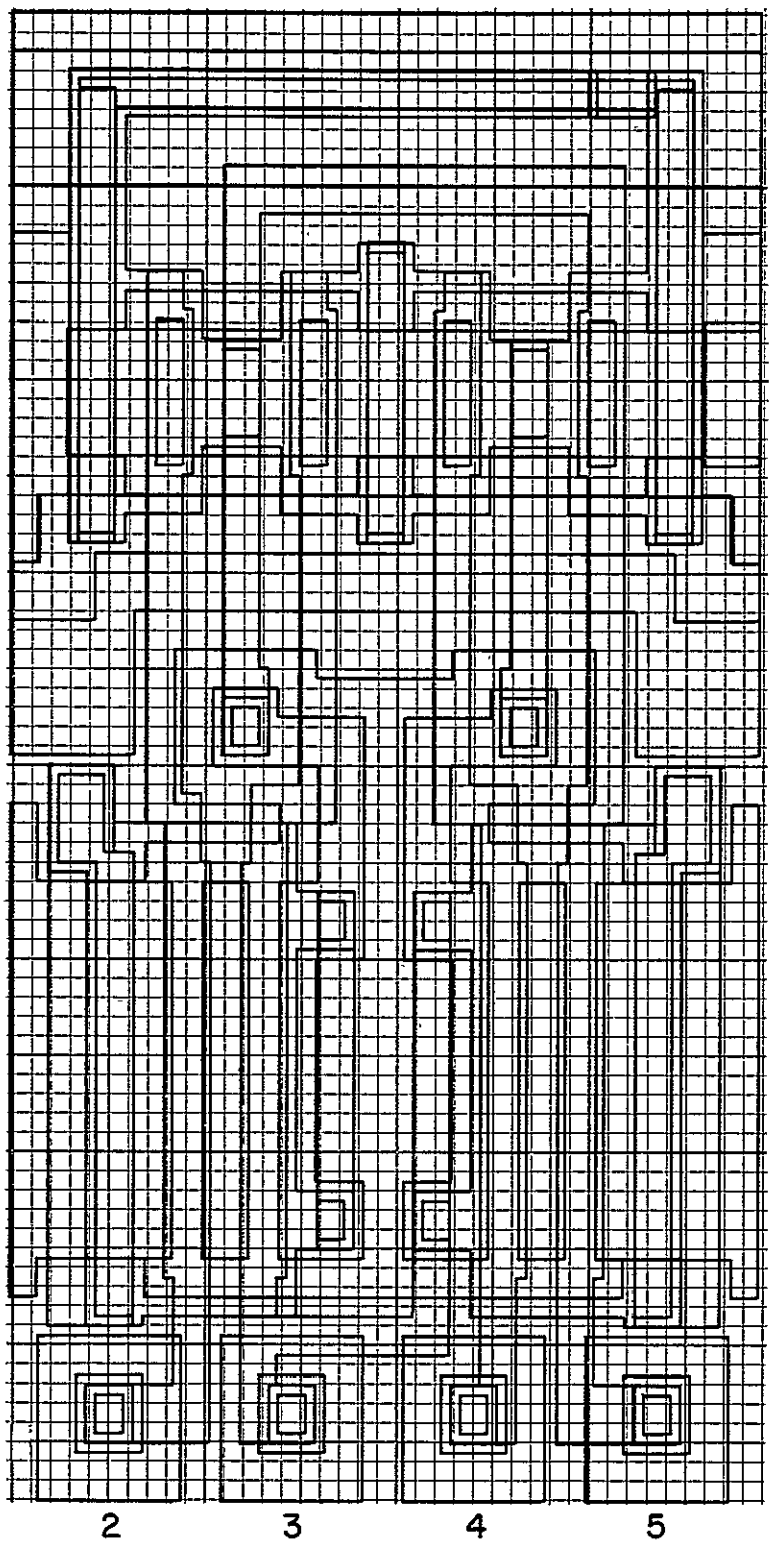


Figure 3. Composite Topology (Levels 1 through 6) for Set-Reset Flip-Flop Cell No. 1420

Cell No.	Cell Name	Configured	Laid Out	Digitized	Checked	Finalized	Verified	Characterized*	Functional and Dynamic Performance Verified on Actual Chip **
9010	Input Pad	→	→	→	→	→	→	N/A	→
9020	Output Pad	→	→	→	→	→	→	N/A	→
9100	Ground Pad	→	→	→	→	→	→	N/A	→
9110	V_D Pad	→	→	→	→	→	→	N/A	N/I
9210	Chip Alignment Key	→	→	→	→	→	→	N/A	N/I
9220	Chip Alignment Key	→	→	→	→	→	→	N/A	N/I
9230	Chip Alignment Key	→	→	→	→	→	→	N/A	N/I
9240	Chip Alignment Key	→	→	→	→	→	→	N/A	N/I
9250	Photo Alignment Key	→	→	→	→	→	→	N/A	N/I
9400	RCA Symbol	→	→	→	→	→	→	N/A	N/I
9410	NASA Symbol	→	→	→	→	→	→	N/A	N/I
9500	Tunnel End	→	→	→	→	→	→	N/A	→
9600	End Cap	→	→	→	→	→	→	N/A	→
9300	Test Transistor	→	→	→	→	→	→	N/A	→
1110	Inverter	→	→	→	→	→	→	→	→
1120	Two-Input NOR	→	→	→	→	→	→	→	→
1130	Three-Input NOR	→	→	→	→	→	→	→	N/I
1140	Four-Input NOR	→	→	→	→	→	→	→	N/I
1210	N & P Transistors	→	→	→	→	→	→	N/A	→
1220	Two-Input NAND	→	→	→	→	→	→	→	→
1230	Three-Input NAND	→	→	→	→	→	→	→	→
1240	Four-Input NAND	→	→	→	→	→	→	→	N/I
1250	Test Resistors	→	→	→	→	→	→	N/A	→
1260	Begin Shift	→	→	→	→	→	→	→	→
1270	Middle Shift	→	→	→	→	→	→	→	→
1280	End Shift	→	→	→	→	→	→	→	→
1290	Free Shift	→	→	→	→	→	→	→	→
1310	Buffer Inverter	→	→	→	→	→	→	→	→
1410	Miller Test	→	→	→	→	→	→	→	→
1420	Set-Reset Flip-Flop	→	→	→	→	→	→	→	N/I

*N/A is not applicable

** N/I is not included on test chip

Figure 4. C-MOS Standard Cell Design Status

Section IV

NASA-RCA C-MOS STANDARD CELL TEST CHIP

A. OBJECTIVES

The NASA-RCA C-MOS Standard Cell Test Chip was produced for several reasons. Since this chip is the first C-MOS array generated using the standard cell design automation techniques, the primary objective was to use the chip to validate the computer programs and the design concepts and techniques developed during the course of this program.

A second objective was to provide a test vehicle from which performance data could be directly measured. The test vehicle provided data which was used to verify the accuracy of the computer circuit simulation techniques that were used in the original design. To achieve these first two objectives at least one circuit type out of each of the basic groups of the standard cell circuit complement was incorporated into the fabricated test chip.

A third objective of the test chip was to provide the test patterns and circuits to verify that the chip design was compatible with the various fabrication and process constraints, and to allow these fabrication and processing parameters to be determined quantitatively, within an acceptable level of accuracy. The availability of this capability is an important asset in establishing and providing for multiple sourcing of chip fabrication at the mask level interface.

A fourth consideration in defining the logic contents of the test chip was to provide a flexible vehicle which could be used to quickly gain experimental evaluation of new technologies and new processes and improvements in current technologies and processes.

B. TEST CHIP LOGIC

The logic contents of the test chip is shown in Figure 5. This illustration has been updated from the one in Quarterly Report No. 2. Each circuit type used has been identified by the cell number so that reference can be made to the data sheets. In addition, the pad (P) designations have been updated to conform to the corresponding pad locations on the metallization level mask artwork shown in Figure 6. The pad designations have been updated to conform to those on the actual chip.

C. TEST CIRCUITS

Although the purpose of many of the test circuits on the test chip are straightforward, there are several tests that have been incorporated into the chip that are not obvious. A brief description of these test circuits follows.

1. Three-Bit Counter and Three-Bit Shift Register

The three-bit counter and the three-bit shift register provide data for at least three specific reasons. The first is to provide experimental evaluation of the master-slave "D" type flip-flop which forms the basis of cells Nos. 1260, 1270, 1280, and 1290. This flip-flop,* for which a patent disclosure has been filed, uses only twelve transistors. Configuring this basic flip-flop into both counter and shift register functions provided data on this device in the two most basic functions in which it will be used.

To implement these functions most efficiently, the 'string cell' concept was developed. The objective of the string cell concept is to provide a means by which interconnection between the bits of a function like a shift register is implemented by connections within the cells themselves. Since these interconnections do not increase the size of the cells and do not use external road bed area, they have practically no

*Described in Quarterly Report No. 2, pp 46 to 50.

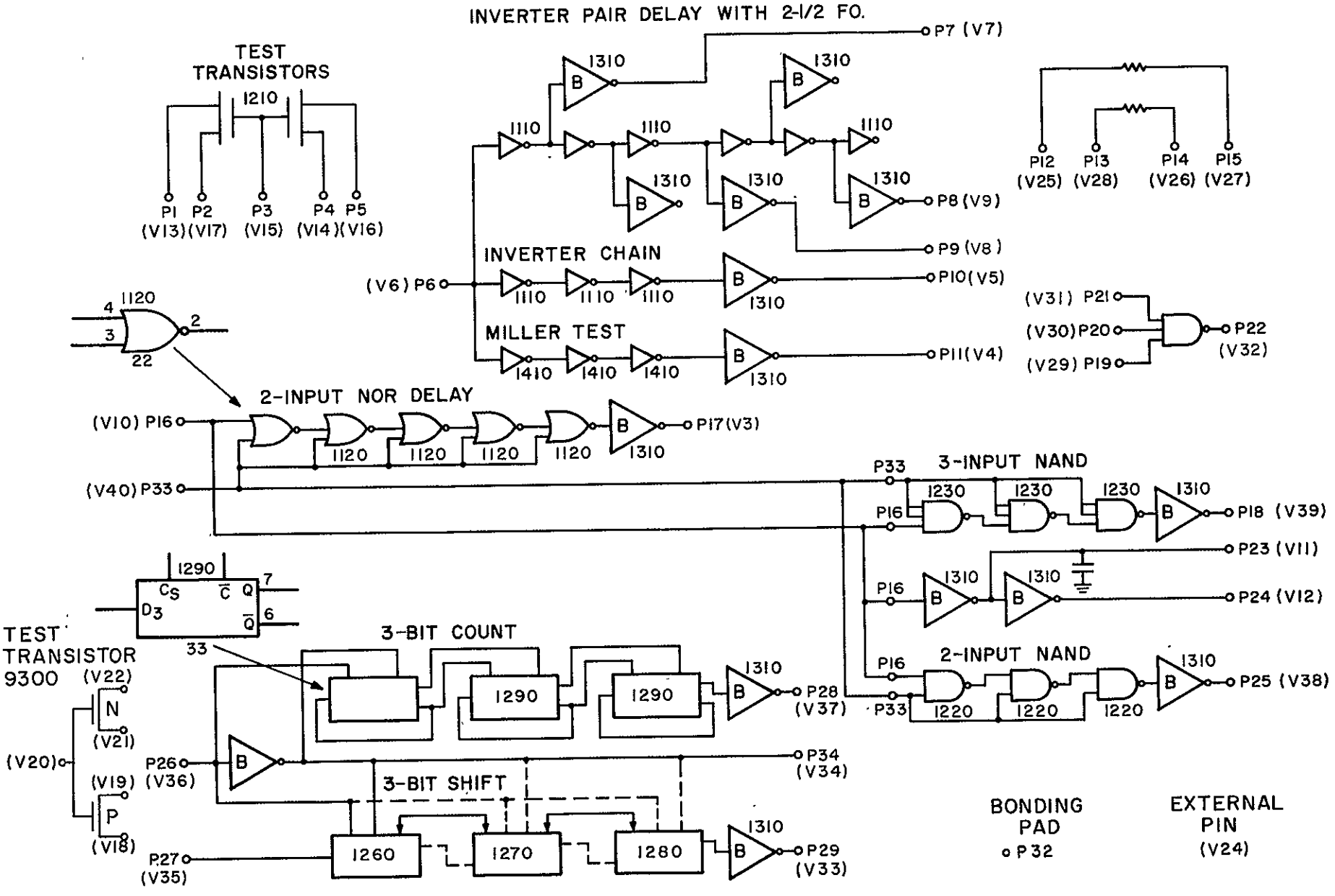


Figure 5. NASA C-MOS Standard Cell Test Chip, Logic Diagram

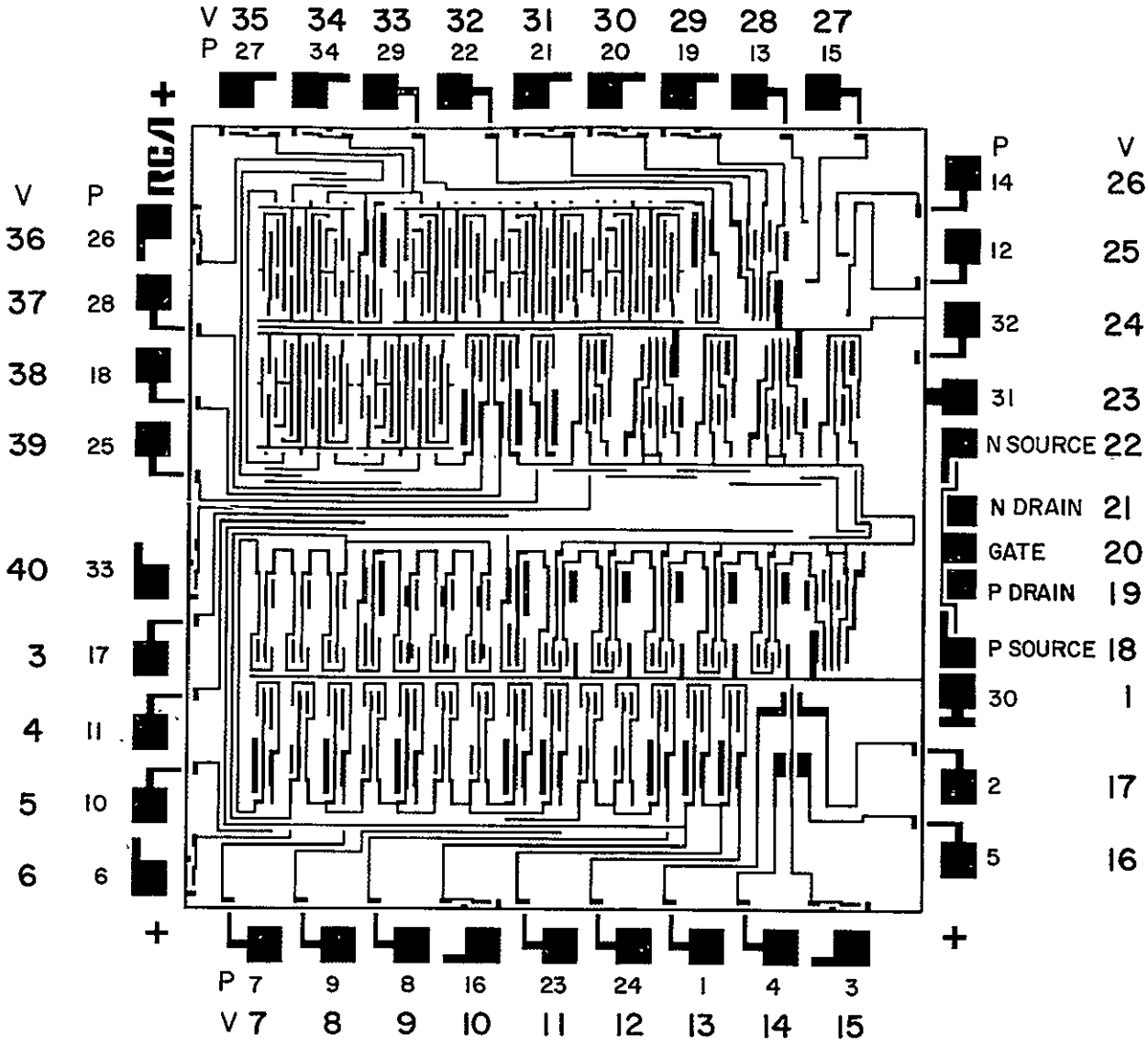


Figure 6. NASA C-MOS Standard Cell Test Chip, Metallization Level Mask Artwork

effect on the size of the chip. This is the significance of the dotted lines in Figure 5. The dotted lines define those interconnections that will be made not by the Routing program, but by placement of cells Nos. 1260, 1270, 1280 in adjacent locations such that a metal overlap between these adjacent cells will make the interconnections. To

provide this capability the begin shift, middle shift, and end shift register cells (Nos. 1260, 1270, and 1280, respectively) were designed into the standard cell library. They represent virtually identical layouts except for slight shifts and modifications that permit intracell interconnections, Cell No. 1290 is another slight modification that optimizes the use of the "D" type flip-flop in counting functions. Examination of the three shift bits on the top row of cells in Figure 6 demonstrates the concept.

The experimental verification of this concept and of the four layouts plus an evaluation of the computer programs in implementing this concept are the other basic aims of the three-bit counter and shift register test.

2. Inverter Pair Delay With 2-1/2 Fanout

This multi-purpose circuit includes all the circuit paths from input pad P6 to the output pads P7, P8, P9, P10 and P11. One of the main purposes of this test is to provide accurate on-chip propagation delay measurements. The circuitry has been designed such that the buffer amplifier and wiring path connected to P7, P8, and P9 are similar. Therefore the propagation delays associated with each of these branches are virtually the same and do not influence the propagation time measured between pads P7 and P8, P7 and P9, and P8 and P9. If the pins attached to these pads are similarly loaded, the propagation time measured between P7 and P9 and between P8 and P9 will yield an accurate on-chip pair delay. Similarly the measured delay between P8 and P7 will yield an accurate two-pair delay or four-stage delay on-chip measurement. With the input capacitance of inverter cell (No. 1110) defined as a unit load, each inverter in these chains is loaded with a 2-1/2 fanout, since buffer amplifier cell No. 1310 is a 1-1/2-unit load.

The Miller Test circuit in the bottom logic chain between P6 and P11 is a special test designed to measure the effect of the drain-gate feedback capacitance. This test involves the Miller Inverter Cell No. 1410 which is essentially an Inverter cell in which the overlap oxide capacitor has been enlarged so that its effect on propagation delay can be measured by comparing the delays between P6 and P10 and P6 and P11.

3. Three-Input NAND Circuit

The three-input NAND circuit appears in two different tests. The test involving the logic chain between pads P16 and P18 serves primarily to yield propagation delay measurements for the three-input NAND circuit as well as the comparative propagation delay between the three- and two-input NAND circuits. This permits an indirect measurement of the additional delay associated with the substrate effect. The three-input NAND circuit connected to P21, P20, P19, and P22 provides the mechanism for direct measurements of the substrate effect both in connection with the propagation time and for the determination of the process parameters required for process evaluation and computer simulation.

4. Test Transistors

To facilitate all steps involved in the production of the C-MOS array, two sets of test transistors have been incorporated into the test chip design. At various phases in the production cycle these devices are examined for various specific reasons.

The street test transistors (cell No. 9300) are the basic test devices that will automatically appear in each C-MOS array using the standard cell approach. Because the cell is located outside the area reserved for the array logic (see Figure 5) there is no loss of active area associated with it. The primary function of the cell is to serve as a test device to be used during initial wafer probing to provide data in order to determine whether or not a particular wafer should continue through the fabrication cycle. To facilitate these measurements the sources of both devices are internally connected to their corresponding substrates so that only three probes are required to obtain stable and reproducible readings.

The other set of test transistors are found in cell No. 1210. This cell is located in the active area and will not, in general, appear on standard cell C-MOS arrays. Among the differences between this cell and cell No. 9300 is that the sources and substrates in Cell No. 1210 are not internally connected as are those in

cell No. 9300. This separation facilitates gain, threshold, and substrate-effect measurements which are necessary to obtain process and device parameters that are needed for circuit characterization and computer circuit simulation. This, in turn, provides another means to verify that satisfactory correlation exist between the measured and computed results further validating the computer simulation technique as an effective design tool.

Section V

ELECTRICAL CHARACTERIZATION AND DESIGN VERIFICATION

A. ELECTRICAL CHARACTERIZATION

The results of the measurements taken on the C-MOS test chip are summarized in this section. The dynamic testing results indicate that all cell and chip designs are functionally correct and that present C-MOS analysis techniques are accurate. This again validates the design procedure and the effectiveness of the computer simulation technique and insures that future standard cell designs and performances will be predictable to a design level of accuracy.

As described in Section IV, these test circuits have been selected such that all standard cell circuit types are represented, and the measured data will serve not only to verify that the goals of the contract have been achieved, but will provide data such as nominal propagation delays, rise and fall times, input and output capacitances, and other data that can serve as nominal design information for systems and equipment.

The nominal values for the various process parameters and mask geometries were used to compute the performance of the various circuits by computer simulation techniques. These fabrication process parameters included substrate doping levels, oxide thickness, diffusion depth, threshold voltages, and mobilities. To determine the level of correlation between the computed and measured performance such as propagation delay, it is necessary to account for the difference between the nominal values assumed for the process parameters and the actual measured or experimentally determined values. These relationships are discussed in evaluating the measured performance for the various test results that follow.

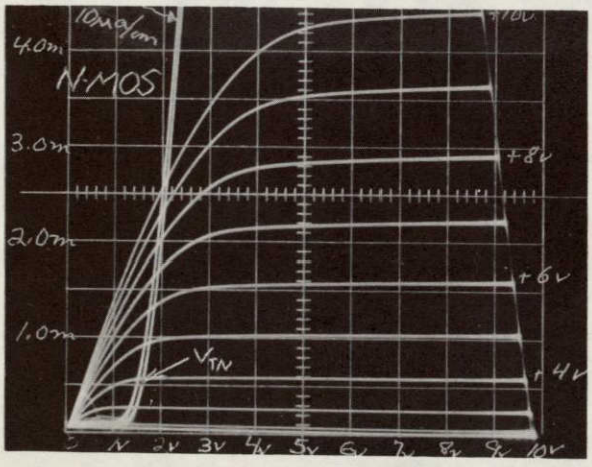
The measurements were made at ambient temperature and at a nominal supply voltage of 10 volts. Most of the delay measurements were made in the form of pair delay, which is the propagation delay measured through two similarly loaded stages at the 50% transition level. Two measurements are taken, positive to positive and negative to negative. The average of these two values constitute the pair delay.

In the experimental results the input and output terminals on the test chip are identified with a P and V numeric indicator. The P designation corresponds to the pad location in Figures 5 and 6. The V designation corresponds to the pin on the 40-pin DIP to which this pad is connected. The inputs and outputs of these circuits on the illustrations of the measured results are, therefore, identified with the V numbers.

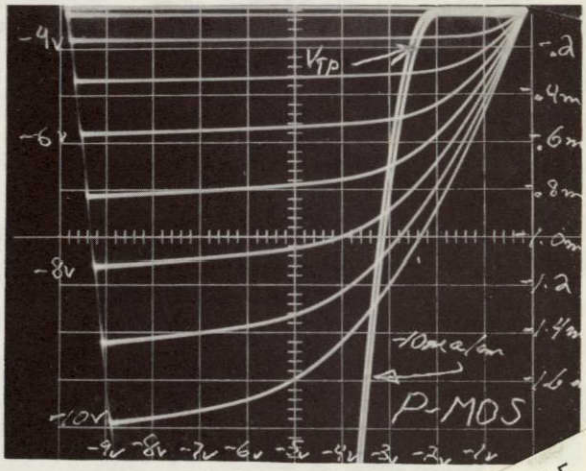
B. TEST RESULTS

1. Test Transistors

The drain characteristics of the N and P transistors shown in Figure 7 are typical of the units measured. As indicated in the diode curves, the threshold voltage for the two devices are approximately 2.5 volts for the P transistor and 1.5 volts for the N transistor. Since the two devices have the same gate geometry, the ratio of the drain currents is indicative of what ratios were employed in the various cell designs in order to maintain uniform charge and discharge times.



N TRANSISTOR



P TRANSISTOR

Figure 7. Characteristics of Test Transistors

2. Inverter Pair Delay with 2-1/2 Fanout

The test circuit shown in Figure 8 provides a most accurate means of measuring "on-chip" pair delays. Each stage in this chain is loaded by a succeeding stage and a Buffer-Inverter (labeled "B"). The loading capacitance at each internal node has been accurately estimated to be 3.25 pF. By observing the waveforms at nodes 7, 8, and 9, it is possible to accurately determine the "on-chip" delays between nodes 7A, 8A, and 9A. All delays associated with the output Buffer-Inverters are essentially balanced out by making relative delay measurements between pins 7, 8 and 9.

The measured delay between P6, P7, P8 and P9 is shown in Figure 9. As can be seen, the internal pair delay from 7A to 8A and 8A to 9A (measured at P7, P8 and P9) is approximately 26 ns or 13 ns per stage for an inverter loaded with 2-1/2 fanout. Of interest also is the delay from the input P6 through 8 stages to P8. As shown in Figure 8, this logic chain contains three buffer amplifiers loaded with 7.3, 15.4, and 9.0 pF in addition to the five inverters each loaded with at least 2-1/2 fanouts. The measured delay (shown in Figure 9) is approximately 84 ns or slightly over 10 ns/loaded stage.

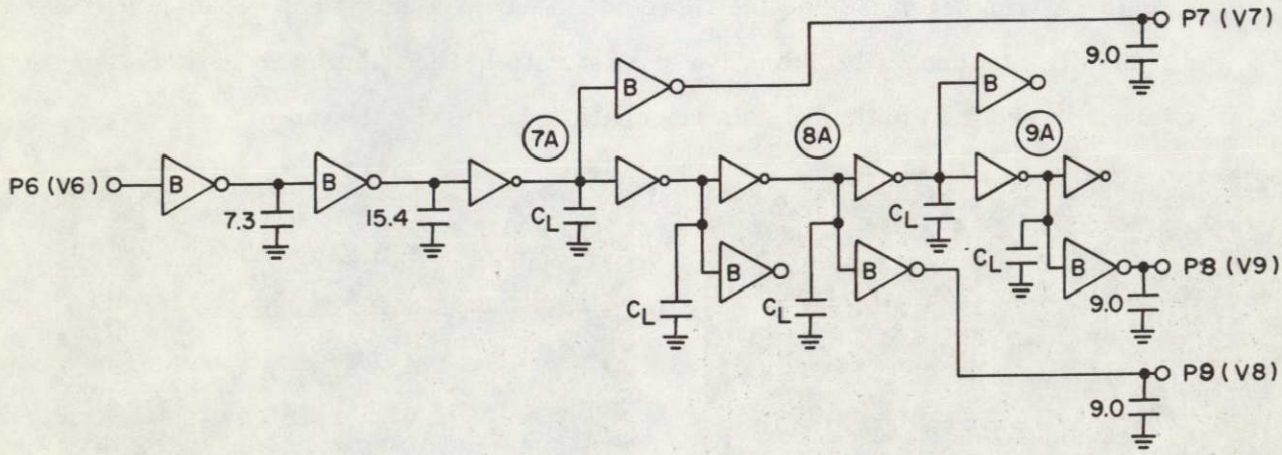


Figure 8. Test Configuration for Inverter Pair Delay with 2-1/2 FO

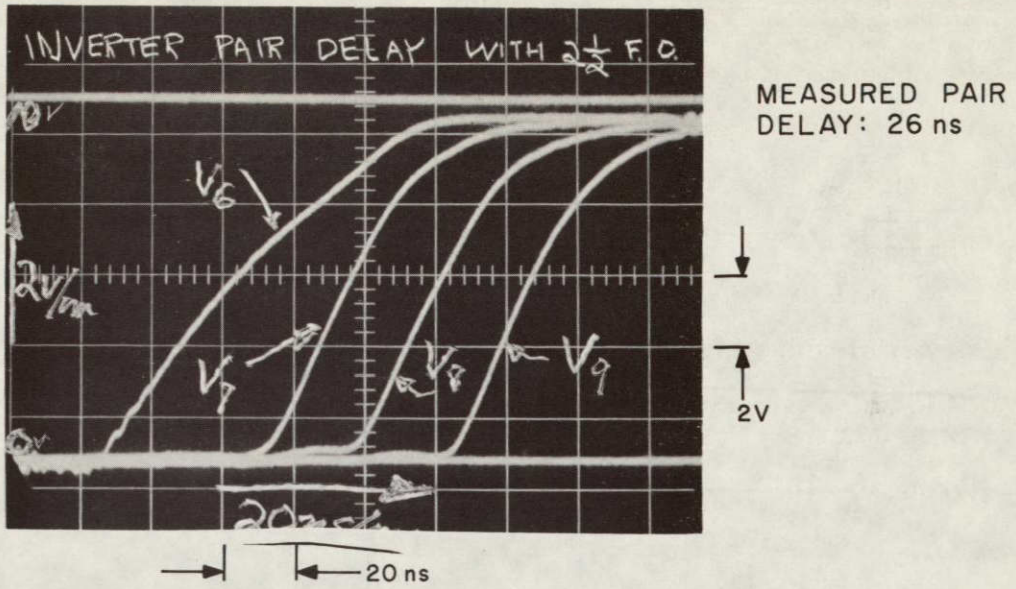


Figure 9. Measured Inverter Pair Delay

A nominal "on-chip" pair delay for cell No. 1110 (Inverter) was estimated to be 19 ns when loaded with 2.0 pF.* Extrapolating this performance figure to that of the 3.2 pF load gives a predicted on-chip pair delay of 30 ns. The difference between the measured 26 ns and the predicted 30 ns is attributable to the slight difference between the assumed nominal parameter values and the actual (measured) parameter values.

3. Two-Input NOR

An on-chip pair delay of 22 ns was predicted for the two-input NOR cell No. 1120. Measurements made on the test chip test circuit, shown in Figure 10, gave a 6-stage delay of 86 ns, as shown in Figure 11. The measured average pair delay over the entire chain of six devices is 29 ns (86/3). Because the measurements of the pair delays of the chains of NOR cells were made with additional input- and output-stage loading, the average delay calculated does not accurately indicate the

*Quarterly Report No. 2, p6

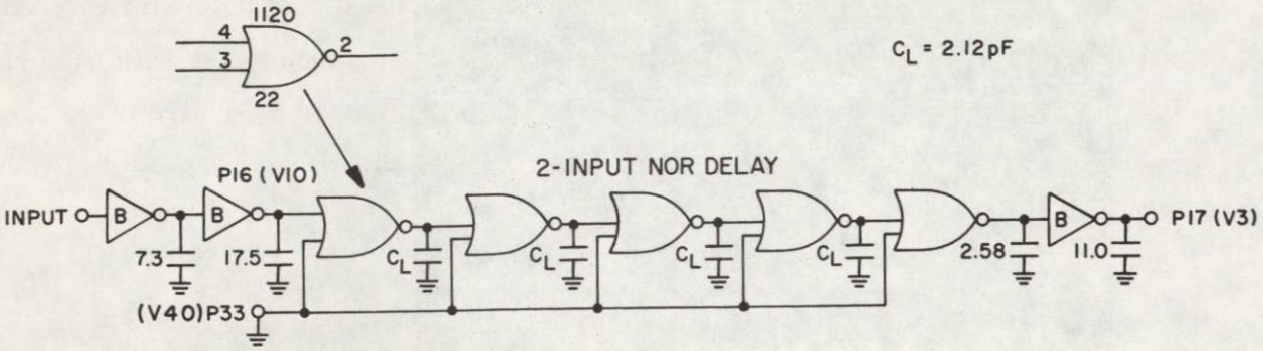


Figure 10. Test Configuration for Two-Input NOR Pair Delay

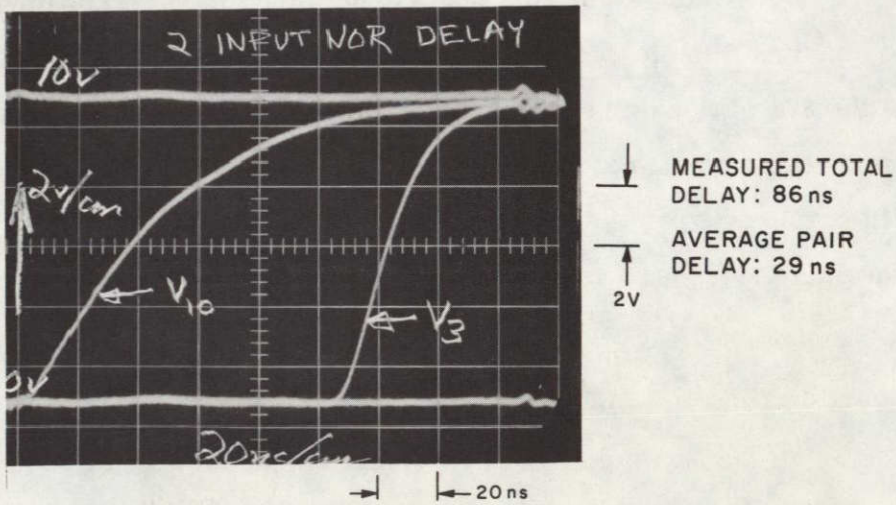


Figure 11. Measured Two-Input NOR Pair Delay

actual delay for the individual cells. The actual pair delay for a chain of two-input NOR cells (with 2.12-pF loading) should be approximately 26 ns.

4. Inverter Chain— Miller Test

The Inverter Chain — Miller Test circuit, shown in Figure 12, permits a direct comparison of circuit delays produced by the intentionally enlarged feedback capacitance of the Miller inverter, with the delays associated with the nominal feedback capacitance of the inverter. The effective capacitive loading associated with each chain is shown on Figure 12. The measured averaged pair delay over the entire chain of four inverter devices is 22 ns (44/2) as shown in Figure 13.

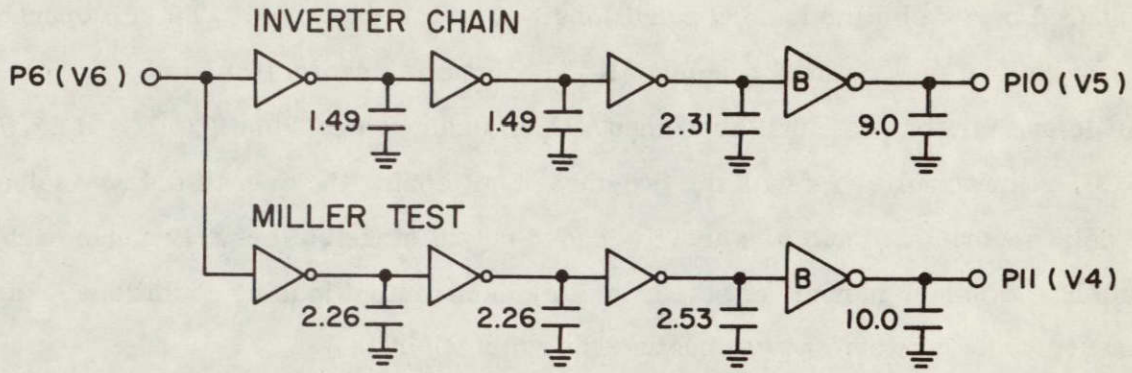


Figure 12. Test Configuration for Inverter Chain — Miller Test Pair Delay

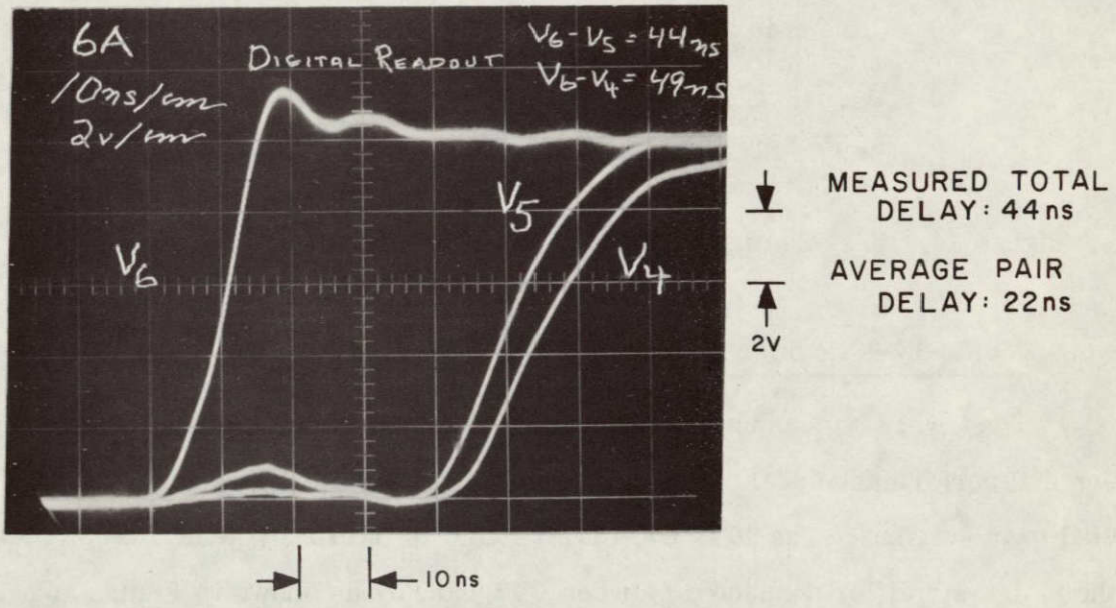


Figure 13. Measured Inverter Chain — Miller Test Pair Delay

A nominal "on-chip" pair delay for this cell was estimated to be 19 ns, when loaded with 2.0 pF.* However, because of the increased effective loading on the output stage the measured average inverter pair delay is 22 ns. Slight differences between the processing parameters assumed for the calculated delays and those of the actual test chip contribute to the observed discrepancy.

5. Two- and Three-Input NAND

Performance of the two- and three-input NAND chains shown in Figure 14 was measured under similar loading conditions. The two-input NAND circuit operates 3 ns/stage faster than the three-input NAND circuit as shown in Figure 15. The average pair delays for the two- and three-input NAND chains were 30 ns (60/2) and 34.5 ns (69/3), respectively. As with the two-input NOR chain, the overall delays include the delays associated with the heavily loaded output stage buffers. Because each chain has the same number of stages and the same output loading conditions, relative measurements between the two chains are quite accurate.

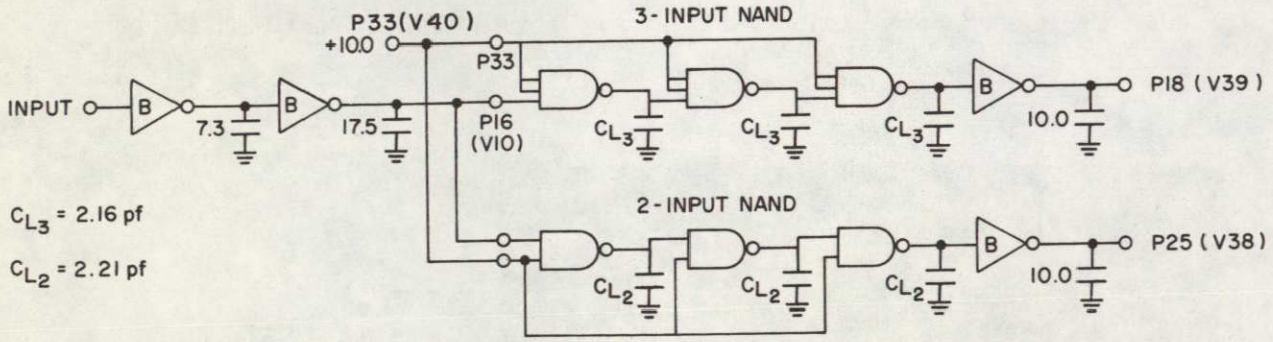


Figure 14. Test Configuration for Two- and Three-Input NAND Pair Delay

6. Divide-by-8 Counter

The three-stage counter, shown in Figure 16, verifies and evaluates the design and performance of the free shift cell No. 1290. Note that only the clock is applied to the circuit. The "CLOCK-NOT" signal is internally generated on the chip by the buffer amplifier connected between P27 and P34 as shown in Figure 16. This buffer has a 13.5-pF load, which introduces a clock skew of approximately 30 ns between "CLOCK" and "CLOCK NOT".

*Quarterly Report No. 2, p6.

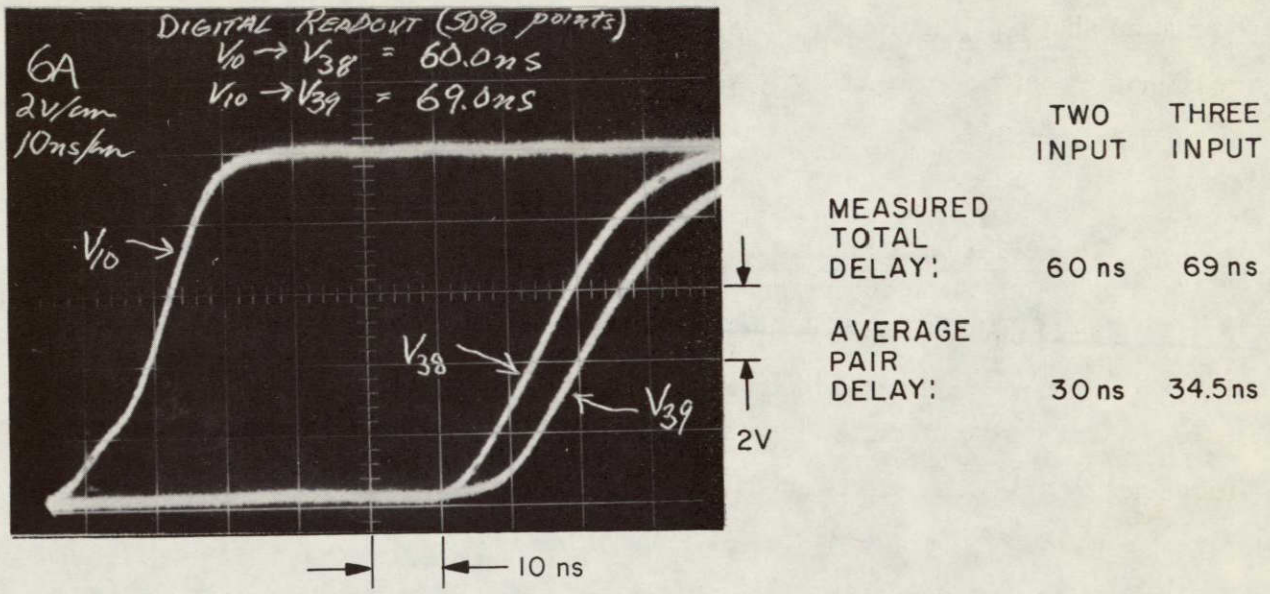


Figure 15. Measured Two- and Three-Input NAND Chain Pair Delay

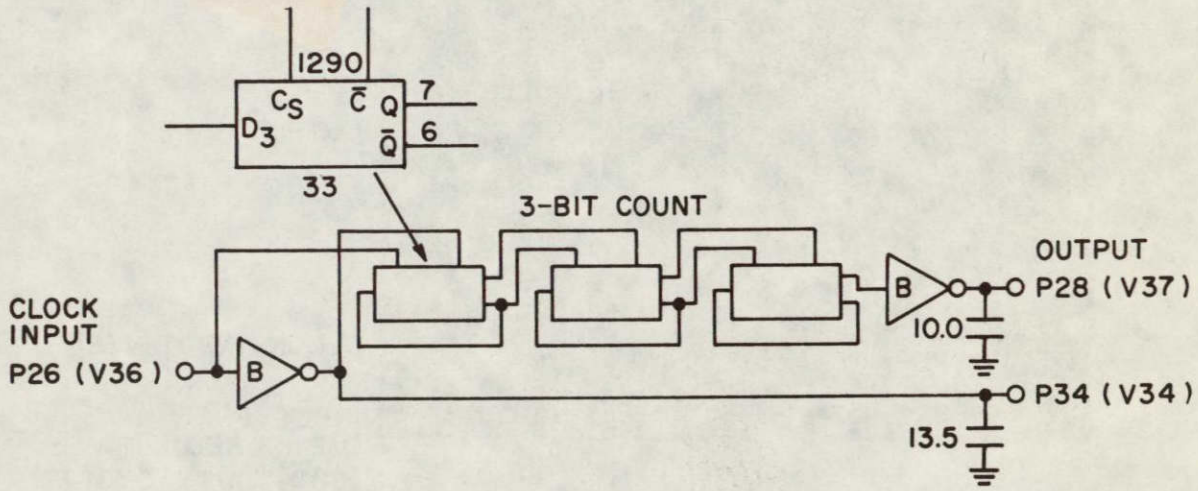


Figure 16. Test Configuration for Divide-by-8 Counter

The circuit functioned properly over the frequency range for which it was tested as shown in Figure 17. The counter operated at a 10-MHz clock rate, the maximum repetition rate of the generator used. The maximum operating rate has yet to be determined.

7. Three-Bit Shift Register

The performance of the three-bit shift register serves to evaluate cells Nos. 1260, 1270, and 1280. The clock and data input for the test circuit, shown in Figure 18, is derived from the circuit on another test chip. For this condition, the dynamic performance at a 2-MHz rate is shown in Figure 19.

8. Leakage

Quiescent chip dissipation is a function of such chip complexities as the number of transistors, the number of tunnels, the size of transistors and the overall chip size. In addition to this, improper mask misalignment can cause further leakage.

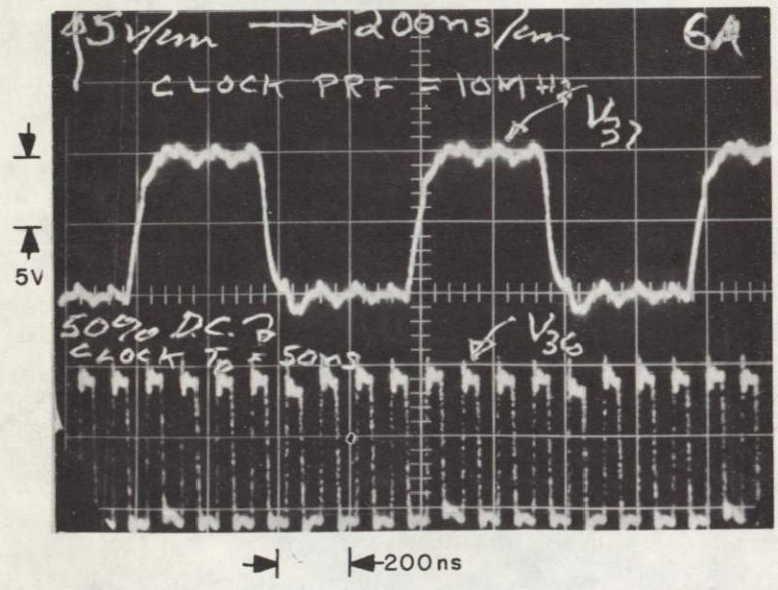


Figure 17. Measured Results of Divide-by-8 Counter Tests

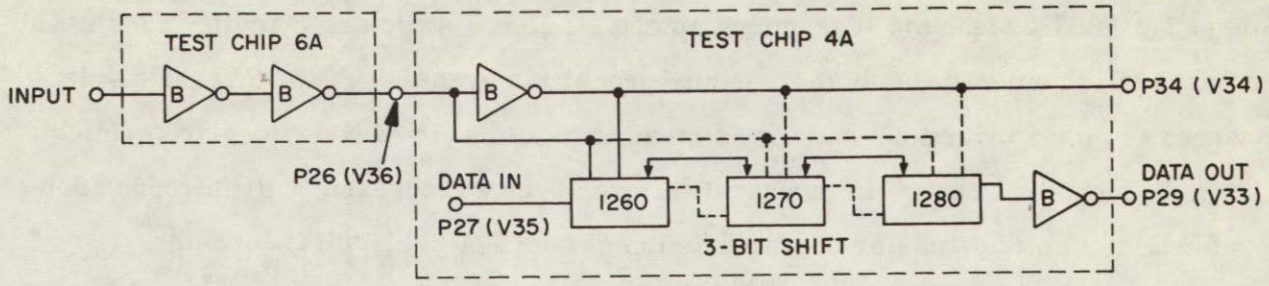


Figure 18. Test Configuration for Three-Bit Shift Register

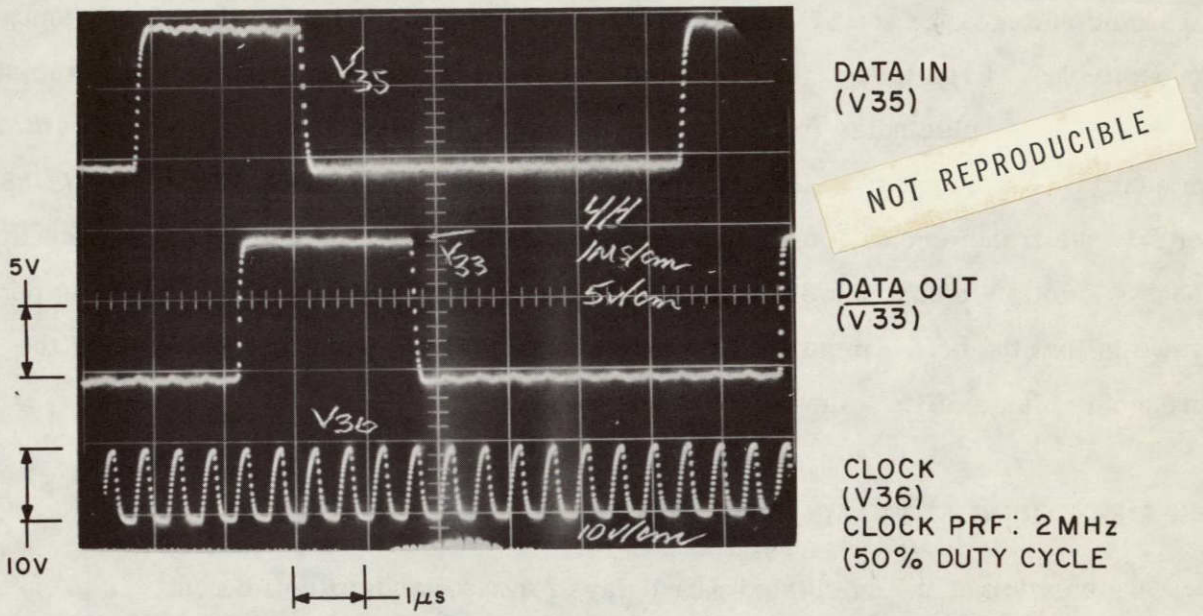


Figure 19. Measured Results of Three-Bit Shift Register Tests

Leakage tests were conducted on the Test Chip. In brief, the procedure was to ground all inputs to the chip. With +10.0V applied to the N-substrate and the P+ guard bands tied to ground, the power supply current was measured. Typical leakage currents were less than 1.0 μA. Leakage currents as low as 0.20 μA were measured. This works out to be less than 5nA per device for the Test Chip.

9. DC Transfer Characteristics - Noise Immunity

One of the most important system advantages of using C-MOS circuitry is its excellent noise immunity characteristics. Not only is its absolute and percentage noise

immunity usually high, but it is unique among all digital switching circuits in being able to essentially maintain its noise immunity properties even though the threshold voltage changes in either direction, as long as the change in the P and N devices are symmetrical. A non-symmetrical change in threshold voltage, even an increase, will introduce non-symmetries into the transfer characteristics of the C-MOS circuits.

The transfer characteristics of transistors from two test chips, 4E and 5E, presented in Figure 20, demonstrate this characteristic. As shown in Figure 20, the threshold voltages for the 5E units are low (1.76 and 1.61 volts for the P and N units, respectively). Even though the threshold voltages are low, the transfer characteristics indicate a wide pulse noise immunity of at least 4 volts for a 10-volt supply - a 40% noise immunity. For the 4E unit, in which the P device has a high threshold voltage (3.88 volts)*, the transfer characteristics indicate that the noise immunity has decreased to about 3.5 volts - a 35% noise immunity. The seemingly surprising conclusion to be drawn is that the noise immunity properties of the 4E unit would be increased if the threshold voltage of its P device were lowered.

C. SUMMARY OF DYNAMIC PERFORMANCE

A tabulation of the calculated pair delays for the standard cell circuits is presented in Table 3 with experimental results for several cells. This data is based on dynamic measurements taken on the C-MOS test chip. The calculated values, identified in Table 3 by the letter "C", are based on an assumed set of nominal process parameters. The measured data is identified by a M suffix. All tabulated delays have been defined as the time between the 50% points of two positive or negative going waveforms. For all cells except 1290 and 1420, the storage cells, the tabulated delays are the pair delays in the conventional sense for nominal conditions.

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*Unit 4E would normally have been a rejected unit had not a rejected wafer been requested in order to get units of widely varying characteristics for evaluation purposes.

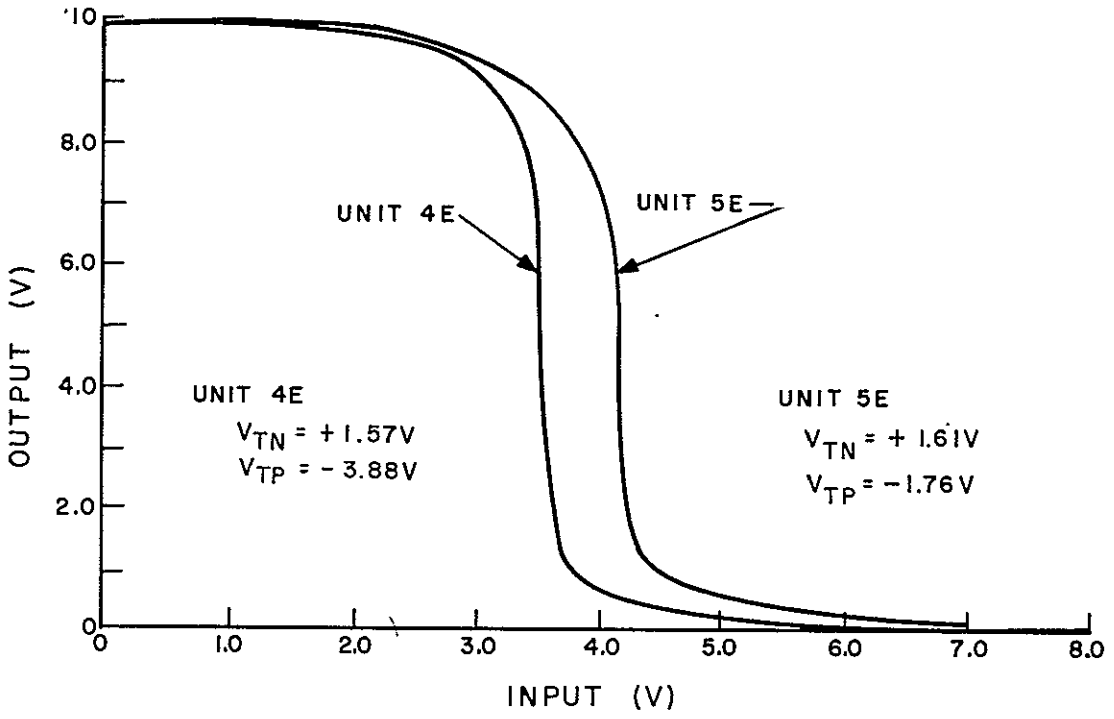

Figure 20. DC Transfer Characteristics of C-MOS Transistors

As shown in Table 3, measured and computed data are listed for cells Nos. 1110, 1120, 1220, 1230, and 1310. Therefore, these results can be used to indicate the level of correlation between predicted and measured performance recognizing that the differences in the load capacitances as listed in the last column must be taken into account. For the first set of data for cell No. 1110, the capacitive load used for the actual and simulated circuit was the same, (3.25 pF). Therefore, for this condition, the measured pair delay of 26 ns and the computed delay of 30 ns can be compared directly. For the other conditions, the effect of different load capacitors must be taken into account.

A tabulation of the 20-80% rise and fall times for each of the standard cells is presented in Table 4. These are computed using nominal process parameters and the capacitance values shown.

The capacitance at each input and output for all the cells is presented in Table 5.

Tables 3, 4, and 5 can be used to update the C-MOS Standard Cell data sheets on pages 5-17 of Quarterly Report No. 2.

TABLE 3. NOMINAL PAIR DELAYS

Cell No.	Function	Pair Delay (ns)*	Load (pF)
1110	Basic Inverter	26-M	3.25
		30-C	3.25
		22-M	1.49
		19-C	2.00
1120	Two-Input NOR	29-M	2.12
		22-C	2.00
1130	Three-Input NOR	27-C	2.00
1140	Four-Input NOR	34-C	2.00
1220	Two-Input NAND	25-M	2.21
		19-C	2.00
1230	Three-Input NAND	27-M	2.16
		33-C	2.00
1240	Four-Input NAND	40-C	2.00
1310	Buffer Inverter	35-M	8.20
		20-C	5.00
1290	Free Shift-Shift Register Bit	$V_C \rightarrow V_Q$ 51 (Worst Case)-C (Device delay)	3.00
1420	Set-Reset Flip-Flop	$V_R \rightarrow V_{\overline{Q}}$ 80 (Worst Case)-C (Device delay)	6.00

*M is Measured on Test Chip;
C is computed characteristic based on nominal process parameters.

TABLE 4. RISE AND FALL TIMES (20-80%) FOR STANDARD CELLS

Cell No.	Name	T_R (ns)*	T_F (ns)*	C_L (pF)
1110	Inverter	8	7	2.0
1120	Two-Input NOR	7	8	2.0
1130	Three-Input NOR	7	10	2.0
1140	Four-Input NOR	8	14	2.0
1220	Two-Input NAND	9	6	2.0
1230	Three-Input NAND	15	21	2.0
1240	Four-Input NAND	18	13	2.0
1260-1290	Shift Cells	21	19	3.0
1310	Buffer Inverter	4	4	2.0
1420	Set-Reset Flip-Flop	30	30	6.0

*Calculated rise and fall times based on nominal process parameters.

TABLE 5. CELL I/O CAPACITANCE VALUES

Cell No.	Name	Pin No.	Capacitance (pF)
1110	Inverter	2	0.55
		3	0.94
1120	Two-Input NOR	2	0.82
		3	1.30
		4	1.30
1130	Three-Input NOR	2	1.18
		3	1.71
		4	1.71
		5	1.71
1140	Four-Input NOR	2	1.39
		3	1.82
		4	1.82
		5	1.82
		6	1.82

TABLE 5. CELL I/O CAPACITANCE VALUES (Continued)

Cell No.	Name	Pin No.	Capacitance (pF)
1220	Two-Input NAND	2	1.04
		3	1.17
		4	1.17
1230	Three-Input NAND	2	0.76
		3	1.40
		4	1.40
		5	1.40
1240	Four-Input NAND	2	0.85
		3	1.54
		4	1.54
		5	1.54
		6	1.54
1260-1290	Shift Cells	3	2.39
		4	0.89
		5	0.97
		6	1.33
		7	2.33
1310	Buffer Inverter	2	1.21
		3	1.76
1420	Set-Reset Flip-Flop	2	1.30
		3	0.87
		4	1.30
		5	0.96

Section VI

NEW TECHNOLOGY

The results of a patent search of the patent disclosure for the C-MOS Static Shift Register (RCA Docket No. 63,427), reported in Quarterly Report No. 2, indicated that a circuit containing similar characteristics had been patented by RCA and made available to NASA under the RCA-NASA contract agreements.

Section VII

CONCLUSIONS

All the objectives and goals of this program have been successfully achieved within the cost budget and time schedule. The validation of the technologies and computer programs developed as part of the contract was based on measured results taken on the C-MOS Standard Cell Test Chip designed for this special purpose. The work accomplished and validated include:

(1) Development of a series of computer programs that includes the automatic Placement, Routing, and Folding Programs for the C-MOS technology, C-MOS Artwork Generation Programs for the Gerber Automatic Plotter, an improved Manual Modification program and programs to drive local, laboratory plotters.

(2) The conceptional design and implementation of the C-MOS array layout.

(3) The definition of a basic C-MOS standard cell circuit family of 13 cells. The circuit design, device specification and topological layout of the standard cells using the standard factory design rules and processes.

(4) The development and specification of the design rules for the topological layout of the standard cell.

(5) The characterization of the circuits for nominal parameter values and loading conditions.

(6) The computer circuit simulation of the performance of the standard cell family.

(7) Verification of these simulation techniques by correlation with experimental results.

(8) The design, fabrication, test, and evaluation of a C-MOS Standard Cell Test Chip which provided the basis for the validation of the above result.

The generation of the C-MOS custom array demonstrates that the standard cell concept can produce low-cost, quick-turn-around, custom C-MOS arrays with the same efficiency as has been demonstrated and confirmed in the earlier P-MOS version. This turn-around time will further deerease as the base of the standard cell family is

increased, although not a very large cell family is required before good flexibility to accommodate a wide variety of custom designs exist.

In order to achieve a reasonable device density on the chip, limited device geometries were used in the design of the various cells. For example, the standard inverter has a 2-mil P device and a 1.3-mil N device. Nevertheless, the overall results show that these circuits have a measured stage delay of from 13 to 15 ns under nominal conditions. This 13- to 15-ns stage delay is for a fanout of about 2-1/2 loads on the chip and about 13 pF load capacitance when going off the chip. The 13- pF capacitance is an estimated load that includes the capacitance of the package, interconnecting wiring, and connectors and is based on a reasonably dense packaging technique.

The decision to use the standard factory, conservative design rules and processes was made to insure the highest reliability in the fabricated arrays even though more advanced design rules and processes were available in RCA. However, these newer processes and design rules had not yet been exhaustively evaluated at the time the design and layout of the present cell family began.

However, since then, a new process has been evaluated that will lower the threshold voltages significantly below those of the current factory low-voltage process. This reduction in threshold voltage should further reduce the stage delay of the present cell family. Within the framework of a denser package that technologies such as beam leads and multi-layer ceramic can provide, the average load capacitance will also be reduced significantly. The results will be a C-MOS standard cell technology than can be expected to provide nominal stage delays in the range from 5 to 8 ns.