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Final Report

MODULAR ENERGY STORAGE and CONDITIONING (MESAC) STUDY

July 1970

TRW SYSTEMS GROUP

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SECTION I

SYSTEMS STUDY

OBJECTIVES AND APPROACHES

The purpose of the MESAC program is to study the concept of a centrally controlled Modular Energy Storage and Conditioning (MESAC) system to provide an understanding of its advantages, disadvantages, and range of applicability.

MESAC was originally conceived at TRW Systems Group as a method of overcoming the unpredictability of the reliability of power systems containing batteries, which is due to the unpredictability of cell and battery failure rates. MESAC consists of a solar array, shunt voltage limiter, and a number of parallel energy storage units (ESU). Each ESU contains a low-voltage battery, a downlink converter (which converts bus voltage to battery charge voltage), and an uplink converter (which converts battery discharge voltage to bus voltage). A central control unit controls the power flow in the central shunt, downlink converter, and uplink converter of each ESU to maintain constant bus voltage and transfer energy from solar array to load with maximum efficiency.

Overall system reliability is enhanced in several ways:

1) Lower voltage batteries are employed, thus reducing the number of series-connected cells and minimizing cell mismatch problems.

2) Redundancy may be added in small increments. If N ESU's are required to supply the rated load power, M units may be installed, and M-N units permitted to fail before a mission or power failure occurs. All units may operate in parallel, including the spares, but provision may be made to switch them OFF line individually either automatically or by ground command.

The study was conducted in two phases, a theoretical phase, in which estimated weight, efficiency and reliability were analyzed and compared with conventional systems, and a breadboard phase, in which a typical three-ESU system was breadboarded.

SUMMARY AND CONCLUSIONS

The results of the study phase showed the following:

- The practicability of high-efficiency direct energy transfer from source to load without intervening loss elements and at a regulated voltage was demonstrated.

- The MESAC system was shown to be extremely flexible in selection of bus voltage and battery voltage independent of one another.

- The practicability of building MESAC power subsystems of varying power levels by addition of identical ESU's to an existing system was demonstrated. However, power subsystems so designed would not necessarily be optimized for the desired application in weight or reliability.

- When compared to a conventional system of equivalent reliability, the MESAC system shows a significant weight advantage over the conventional system for long life systems, the crossover point falling between four and six years.

- The weight advantages of the MESAC system are more pronounced in the longer orbit applications than in shorter orbits.

The results of the breadboard phase are as follows:

- The breadboard performed all of the functions required to demonstrate the MESAC concept, and continued to operate at rated power levels after simulated failure of any one of the ESU's.

- Uplink converter efficiency at nominal load approximated the predicted 83 to 85 percent.

- Downlink converter efficiency was reduced to 70 percent due to the need for a protective zener diode at the output.

- Weight and reliability of the breadboard circuit were not analyzed.

A number of significant problems were exposed during the development phase. Stability problems were encountered due to feedback of ripple from the main bus to the control system of the uplink converters through the high gain central control system, and due to the use of a variable OFF time combined oscillator and modulator. This resulted in excessive filtering at the main bus to stabilize the system. Use of a constant-frequency system should result in a considerable weight savings over the existing breadboard concept.

Variations in gain of the converter control and drive circuitry result in a degradation of the accuracy of load sharing between converters, so that both charge and discharge tend to be partially sequential. Although fine adjustment can alter the current ratios, a revision of control and drive concepts of the converters is necessary before the behavior can approach that of diode-coupled batteries.

Limited base-emitter reverse breakdown voltage ratings of available transistors have limited accordingly the boost ratio to a value slightly too low for adequate boosting. A modification of the drive circuitry is necessary to increase boost ratios.

SYSTEM STUDY GROUND RULES AND ASSUMPTIONS

The MESAC system consists of the following basic components: A single central control unit, internally redundant and therefore highly reliable, is used to sense the system bus voltage and to control the operation of the electronics in each of several energy storage units. The system functions by controlling the up converter, down converter, and shunt limiter so as to maintain bus voltage constant at all times. These energy storage units (ESU), each containing a battery and associated electronics for conditioning both charge and discharge power, are internally nonredundant, and individually are not sufficiently reliable for extended operation. However, by carrying one or more spare ESU's, an overall system reliability approaching the desired reliability may be achieved. A simplified block diagram of the MESAC concept as used for the theoretical study is shown in Figure 1.

The study was bounded by the following considerations:

1) To preserve the modular character of the system, a minimum of 3 ESU's in parallel was considered. Although the maximum number of units is theoretically unbounded, the study was limited to consideration of not more than 15 units in parallel.

2) The number of cells in series in each ESU was varied from a minimum of two to a maximum of 22.

3) Tradeoffs over a large range of missions were limited to the assumption of constant power. However, the parametric data are available for an analysis of the characteristics of variable power missions.

4) Cell capacities were limited to those currently available in nickel-cadmium batteries on an off-the-shelf basis, between one ampere-hour minimum and 20 ampere-hour maximum.

5) Orbit conditions studied varied from the 100 minute orbit (eclipse time 0.667 hours) to the synchronous equatorial orbit (eclipse time 1.2 hours).

6) Weight calculations are based upon the assumption of a common heat sink for batteries and associated electronics.

The analysis was conducted by dividing the energy storage unit into two power handling sections, the uplink (discharge) converter, and the downlink (charge) converter. The remaining parts, including current limiting circuitry, charge controls, and other logic were lumped, both in

weight and power consumption, and assessed as a constant added to the variable weight and power consumption of the power handling components.

Since no specific mission is under consideration, the tradeoffs were done on constant power missions; however, the data can be used for any variable power mission by selection of an energy storage unit, uplink and downlink converter, and a battery of appropriate size.

ANALYSIS OF THE UPLINK CONVERTER SIZING EQUATIONS

For any specific cell size, or capacity, the total ampere-hours which can be delivered to the input of the uplink converter is expressed by:

$$A\text{-}H_{input} = (C_B)\ (DOD)$$

where C_B = Battery capacity

DOD = Maximum allowable cell depth of discharge

The average current to be delivered to the converter is then:

$$I_{input} = (C_B)\ (DOD)/t_e$$

t_e = Eclipse time in hours

For any cell size and DOD, the shorter the eclipse the higher the current. The average input current is independent of the number of series-connected cells. At rated converter power output, the peak switch current is expressed by:

$$I_{sw} = (I_{input})\ (V_{max}/V_{min})\ (K)$$

where K = 1 for double-ended converters

2 for single-ended converters

V_{max}/V_{min} = The ratio of maximum to minimum input voltage

Again, the switch current is independent of the number of series-connected cells since the ratio V_{max}/V_{min} is independent of the number of cells if no cell failures have occurred.

The power output of the unit is not independent of the number of series-connected cells.

$$P_{out} = (P_{input})\ (\eta)$$

where η = Efficiency of the uplink converter

$$P_{out} = (C_B)\ (DOD)\ (N)\ (E_d)\ (\eta)/t_e$$

where N = Number of series cells

E_d = Average cell discharge voltage

DEVELOPMENT OF PARAMETRIC DATA

Based upon these concepts and upon the circuit implementation trade-offs described in Section 2, a set of equations was designed to describe the performance, efficiency, and weight of the uplink converter. These are shown in detail in Section 2.

Similarly, a set of equations describing the performance of the downlink converter was developed, using similar design concepts, and containing compensation for the less-than-unity ampere-hour efficiency of battery cells on charge. See Section 2 for the detailed equations.

In order to allow for increased charge rates when excess solar array capacity is available, the ground rule was adopted that the current limit set for each downlink unit would be twice that required to fully charge the battery from the deepest discharge. The possibility of high rate charge was also considered.

The design equations were implemented in two computer programs, named /UPLINK/ and /DLINK/ respectively. These are programmed in the BASIC language and were run on the TRW SDS 940 remote terminal time-sharing system, varying the frequencies from 1 to 32 kHz, cell size from 1 to 20 ampere-hours, number of cells in series from 2 to 22, and orbit parameters from 100 minute circular to 24 hour circular synchronous. Copies of the source program are shown in the Appendix. The computer-dumped parametric data are too voluminous for presentation in this report. However, complete data sets have been transmitted to the NASA cognizant engineer.

TYPES OF FAILURE RATES AND THEIR DETERMINATION

In large populations of parts operating under reproducible conditions failures are eventually observed. Usable failure rate definitions have been devised in cases where observed failures are neither too few nor too numerous, i.e., if some of the population fail but not an appreciable fraction.

Under the above conditions, the observed failure rate is usually composed of several contributing sub-populations:

1) The classical "random constant" failures. These are usually due to a combination of latent manufacturing defects and occasional abnormal environmental stress. Constant failure rate with time is a good approximation to the occurrence of these failures if they are few compared to the total population and if the observation is made after the system has been operated for long enough to eliminate gross defects.

2) Devices whose principal stress is cyclic have a failure component similar to the above which is approximately constant with the number of cycles of operation. Devices wearing out under cyclic stress will show approximately the above characteristics with number of cycles rather than time.

3) Some devices "wear out" in time, either as a result of electrochemical, thermal, or other physical equilibrium effects or accumulated effects due to environmental stress. Most wearout is characterized by a slow degeneration over the useful life followed by abrupt collapse at a critical threshold.

In the case of high reliability equipment whose design life is shorter than component wearout life, the change of catastrophic wearout failure is small, and a failure rate rising linearly with time is a good approximation, giving the form $R(t) = e^{-kt^2}$.

Since the initial condition of devices is usually distributed over an acceptable range, the time to the threshold varies through a population so that a distribution due to randomness is superimposed upon the deterioration modes. When incomplete knowledge must be used, a workable approximation to complex behavior is to assume the failure rate constant by year (or other time interval) of operation, but variable from year to year. If there is both a time and a cycle-dependent failure contribution, separate estimates may be made of the proportion of each contribution in order to extrapolate from one condition to another.

Typical Battery Failure Rate Models

Although apparently simple in structure, the nickel-cadmium cells used in spacecraft display a complex failure behavior. Several physical failure modes have been qualitatively identified, each proceeding at its own rate, and each dependent upon the environmental and operational stresses imposed upon the cell.

The principal failure modes which have been observed in nickel-cadmium batteries are as follows:

Interplate Short-Circuits may be caused by manufacturing defects, by the successive compression and relaxation of the separator material as the cell is cycled between the discharged and charged states, and as a result of chemical action of the electrolyte and the oxidizing environment upon the separator material. Thus, interplate short-circuiting may have time-dependent, and cycle-dependent components, upon which are superimposed a random distribution resulting from manufacturing variables. In addition, a further dependence upon the integral of voltage and time could result from a dependence of the rate of formation of dendrites upon the voltage of the negative electrode.

Loss of Seal Integrity may result from a randomly distributed manufacturing or handling defect, from the pressure cycling which occurs as the cell is charged or discharged, or from a time-dependent corrosion process. When seal integrity is lost in a vacuum environment eventual cell drying may be expected, resulting in an open-circuit.

Terminal-to-Case Short-Circuits have been observed as a result of a process by which silver, derived from the corrosion of a seal brazing alloy, is deposited across the ceramic insulator of the cell terminal, eventually causing a short-circuit. Extremely high failure rates were observed until a redesign of the terminal sealing process reduced the rate of silver deposition significantly.

Voltage Divergence leads to failure when one or more cells in a battery of series-connected cells deviates sufficiently in performance from the remaining cells of the battery to experience excessive voltage at end of charge, or to reverse in voltage due to overdischarge. This behavior has been observed in laboratory tests simulating actual operation of flight power systems hydrogen generation within the cell, overpressure, and seal failure.

Development of TRW Battery Failure Rates

The battery testing program which has been conducted on nickel-cadmium cells at the Naval Ammunition Depot Testing Laboratories at Crane, Indiana displayed such a large number of failures during the first and second years that to apply these failure rates to flight batteries would have resulted in excessively low reliabilities for batteries and electric

power subsystems containing batteries. The testing conditions under which the batteries were operated in the NAD tests were not representative of the best operational satellite power systems, nor were the test batteries representative of the flight quality batteries which could be assembled from cells which had been extensively tested, and from which all cases of infant mortality had been eliminated.

In addition, the high failure rates resulting from the NAD data were not borne out by either testing experience at the TRW laboratories, or by satellite flight experience. On the other hand, if one eliminates all of the NAD data from consideration, insufficient data remains for an adequate justification of any reasonable failure rates. At the present time, after eliminating all failures due to infant mortality and those representing the terminal short-circuit failure mode which had subsequently been eliminated by redesign of the brazing operation in the header, a total of only 25,000,000 cell-hours of operation have been accumulated on nickel-cadmium cells over a three year period with only one cell failure due to an interplate short-circuit in the third year of operation. No other complete cell failures have been seen.

Occasional leaks, however, have been detected which could, if carried to their logical conclusion, have resulted in drying of the cell and causing an effective open-circuit. Similarly, divergence of cell characteristics has been observed, resulting in high voltage behavior of individual cells which, allowed to progress, could result in failure of the battery due to high pressure operation and rupture of a divergent cell. Finally, although the redesign of the terminals has decreased the rate of silver formation across the insulator, accelerated tests have still detected some silver formation. Unfortunately, none of the testing programs in which these phenomena were observed permitted the continuation of the test to determine the actual time of failure. Consequently, although we know that the failure modes exist, and can either observe or anticipate their dependence upon time and cycles of operation, and upon temperature, we have insufficient data to enable us to compute the failure rates rigorously. We must therefore make a determination on the grounds of the data which are available to us, and upon the basis of the best engineering judgement of which we are capable.

In the case of interplate short-circuits, a computed nominal failure rate of $1/2.5 \times 10^7 = 40$ failures per 10^9 hours was raised to 50 on the basis of engineering judgement, and increased during the fourth through sixth years based upon the thinning and deterioration of the separator observed after dissection of older cells. The remaining failure rate data of Table 1 are similarly based upon our best estimate of the failures which would be experienced with extended operation and a larger number of cells in the test program.

RELIABILITY

Study of the MESAC system reliability was initiated with an analysis of the reliability of a battery as a function of time and of the number of series-connected cells, utilizing as a ground rule the assumption that the effect of divergence upon battery failure rates varies linearly with the number of series-connected cells.

Table 1. Estimated Battery Cell Failure Rates (Time-Varying)

Failure	Cell Failure Rate (Failures/10^9 Hours) Yearly Basis - Six Year Duration					
	1	2	3	4	5	6
Terminal-Case Short (λ_{ss})	3	4	6	8	12	17
Plate-Plate Short (λ_{ps})	50	50	50	100	200	400
*High Voltage Divergence (λ_d)	10	20	50	200	500	1000
Open (λ_o)	10	20	36	54	76	100

*For 22 series connected cells, varying linearly to zero for 2 series connected cells.

The equations upon which the analysis is based are as follows:

Battery Reliability Math Model

Battery Success Equations

$R_{B_1}(t_n)$ = The reliability of one battery for a mission time of t_n.

$$R_{B_1}(t_n) = P_c(t_n)^{22}$$ where P_c = Probability of survival of 1 cell

$R_{B_2}(t_n)$ = The reliability of two redundant batteries for a mission time of t_n.

$$R_{B_2}(t_n) = 1 - \left[1 - P_c(t_n)^{22}\right]^2$$

Cell-Level Success Equations*

The probability that the battery cell will be in a given condition at the end of the nth time interval (i.e., $t = t_n$) can be obtained from the following equations:

$P_c(t_n)$ = The probability that a certain battery cell is unfailed at time t_n.

$$P_c(t_n) = e^{-Z_{n+1}}$$

$Q_{ss}(t_n)$ = The probability that a certain battery cell experiences a terminal-case short at time t_n.

$$Q_{ss}(t_n) = \sum_{i=1}^{n} \left(\frac{\lambda_{ssi}}{\lambda_i}\right) e^{-Z_i} \left[1 - e^{-\lambda_i (t_i - t_{i-1})}\right]$$

$Q_{ps}(t_n)$ = The probability that a certain battery cell experiences a plate-plate short at time t_n.

$$Q_{ps}(t_n) = \sum_{i=1}^{n} \left(\frac{\lambda_{psi}}{\lambda_i}\right) e^{-Z_i} \left[1 - e^{-\lambda_i (t_i - t_{i-1})}\right]$$

$Q_o(t_n)$ = The probability that a certain battery cell opens at time t_n.

$$Q_o(t_n) = \sum_{i=1}^{n} \left(\frac{\lambda o_i}{\lambda_i}\right) e^{-Z_i} \left[1 - e^{-\lambda_i(t_i - t_{i-1})}\right]$$

$Q_d(t_n)$ = The probability that a certain battery cell diverges at time t_n.

$$Q_d(t_n) = \sum_{i=1}^{n} \left(\frac{\lambda d_i}{\lambda_i}\right) e^{-Z_i} \left[1 - e^{-\lambda_i(t_i - t_{i-1})}\right]$$

where, $\lambda_i = \lambda_{ss_i} + \lambda_{ps_i} + \lambda_{o_i} + \lambda_{d_i}$, the total battery cell failure rate for the ith time interval.

λ_{ss_i} = The cell terminal-case short failure rate for the ith time interval.

λ_{ps_i} = The cell plate-plate short failure rate for the ith time interval.

λ_o = The cell open failure rate for the ith time interval.

λ_d = The cell divergence failure rate for the ith time interval.

$$Z_i = \int_0^{t_{i-1}} \lambda(t)dt = \sum_{j=1}^{i-1} \lambda j(t_j - t_{j-1}) \quad \begin{matrix} \text{for } i = 2, 3, 4, \ldots, n \\ \text{for } i = 1 \end{matrix}$$

t_j = The time at which the jth time interval ends, $t_o = 0$

$n = 1, 2, \ldots, 6$

These equations were implemented in a BASIC program named /REL/ for the SDS 940 Time-Sharing Computer, using the short-circuit, open circuit, and terminal-case short-circuit failure rates as a single lumped failure rate, and varying the divergence failure rate from 0 at 2 series-connected cells to the value shown in Table 1 at 22 series-connected cells. The program is shown in the appendix. This program also creates a data file of battery reliabilities for use in later computer programs.

Binomial Redundancy

If enhanced reliability is required, full or partial redundancy of batteries, energy storage units, or circuit elements may be used. The reliability of such a system is calculated as follows:

R_b = Probability of survival of one battery or ESU

$1 - R_b = S_b$ = Probability of nonsurvival

Thus

$$R_b = S_b = 1$$

and where m units are used in parallel:

$$(R_b + S_b)^m = 1$$

Expanding the above expression binomially gives:

$$R_b^m + aR_b^{m-1} S_b + \ldots$$
$$+ zR_b S_b^{m-1} + S_b^m = 1$$

where the coefficient of the rth term is equal to:

$$\frac{m!}{(r!)\ (m - r)!}$$

Now if j units may fail without failing the system, then the reliability is equal to the sum of the first j + 1 terms of the expanded binomial above.

The reliability of the MESAC central control and of the overall system was based upon the reliability block diagram of Figure 2, in which the system is broken up into individual circuit groups which are internally nonredundant, and will fail with the failure of any part in the circuit.

These circuit groups are then combined using binomial, or quad redundancy and the overall reliability of the black box or system calculated by a generalized computer program available at TRW for this purpose.

The resulting section and system reliabilities are then used as an input to the MESAC System Reliability Program, /MESREL/which computes the overall system reliability as a function of the number of cells, the number of units required, the number of units installed, and the required time of survival.

A block diagram of the overall reliability calculation process is shown in Figure 3.

FINAL TRADEOFF STUDIES

The comparison between several MESAC systems and their conventional battery system counterparts was made on the following basis:

1) The weight of the ESU was calculated as the sum of of the weights of the power components, including the packaging weight required to mount and enclose the components, plus a constant weight of 2 pounds for the low level control circuitry such as current limits, charge control, etc.

2) The weight of the central control unit was estimated at 4.1 pounds, regardless of the power of the system, since it consists of low level control circuitry only. All weights include packaging and assume discrete components rather than integrated circuitry.

3) The total system weight is the sum of the weight of the installed ESU's, the central control unit, and a solar array weight penalty due to the inefficiency of the power subsystem in storing and releasing energy.

4) The solar array weight penalty in the case of the 24-hour synchronous orbit was judged to negligible and was neglected. In the case of the 100 minute orbit, it was set equal to the solar array weight at 2 w/lb resulting from the losses due to the product of the efficiencies of the uplink and downlink converter for MESAC, and to the efficiency of the battery charger times an estimated 5 percent solar array mismatch penalty in the case of the conventional circuit.

In order to restrict the tradeoff effort to a reasonable level, a preliminary plot was made of the efficiency of the uplink and downlink converters as a function of the number of series cells in the ESU battery and of efficiency and weight as a function of frequency. These are shown in Figures 4 and 5. It was felt that although the optimum system weight might occur at lower efficiencies, since the solar array weight penalty

resulting from a power processing loss is usually lower than the comparable battery weight penalty, the cost of the solar array is so high that it seems advisable to maintain high efficiency if possible. Consequently, it was decided to maintain the frequency at 8 kHz, and the number of series cells between 6 and 10 in order to take advantage of the relatively high efficiency of the converters under those conditions without incurring excessive weight penalties.

By returning to the data dumps on uplink and downlink converters it was possible to put together several combinations of MESAC systems which would deliver a power equal to, or slightly greater than, a pre-assumed power level. For each of these systems, the weight was calculated and a plot made of the power to weight ratio of the best MESAC system as a function of the number of units installed and the reliability of the system.

As a specific example, Figure 6 shows a comparison between the best two MESAC systems designed for 100 watts, and the best conventional 22-cell battery systems designed for the same power at the same depth of discharge (70 percent in a synchronous equatorial orbit).

The two described MESAC systems are as follows:

1) The total system power is 100 watts in a synchronous orbit. A minimum of 3 ESU's are required having a power level of not less than 33.3 watts each. Each ESU contains a battery of 6 series-connected 9 AH cells. The graph shows the ratio of power required to total system weight (exclusive of solar array) P/w = 100/w as a function of the probability of survival of the system for 6 years as the number of installed units is increased from 3 to 6.

2) The second MESAC system alternative for the same mission employs 2 ESU's each containing 6 series-connected 12 A-hr cells and capable of delivering 100 watts. The graph shows the ratio of power required to total system weight (exclusive of solar array) as a function of reliability as the number of installed units are increased from 2 to 4.

3) The conventional battery is a 22-cell, 6 ampere-hour unit of which one is required to accomplish the mission or two similar 3 A-hr units. The graph shows the ratio of total system weight, exclusive of solar array versus reliability, for the installation of batteries with varying redundancy.

Figures 7 through 13 show the comparative tradeoffs over the range of 1000 watts for synchronous, and 100 to 500 watts for the 100 minute circular orbits. These tradeoffs and other less optimum ones which are not shown display certain consistent features:

1) Fewer numbers of series cells give curves which are more favorable than (i.e., lie above and to the right of) those with larger numbers of series cells.

2) A larger number of low power units will give a relatively flat curve, usually intersecting the steeper curve for a smaller number of large units. This implies that systems that require very high reliability for long times should consist of many small units, whereas, the preferred system of moderate reliability would be fewer units of higher power if the required reliability level falls to the left of the intersection point.

Behavior of the MESAC System as a Function of Required Survival Time

Almost without exception, the conventional battery curves tend to be much steeper than those of the MESAC curves. This leads to an intersection of the MESAC and conventional curves, the intersection point being the tradeoff point.

The 100 watt one-battery conventional system and the three-battery MESAC system of Figure 6 are plotted in Figure 14 to show the tradeoffs as a function of required survival time. The heavy line may be interpreted as the locus of crossover points at which the MESAC system becomes both lighter and more reliable than the corresponding convention 22-cell battery system. It is clear from this figure that as reliability requirements and life time increase the MESAC system shows clearer advantages. Thus, at two years, it would be unprofitable to use the 100 watt MESAC system unless a reliability of 0.9996 or greater is required. However, at 6 years, the MESAC system having a reliability requirement of 0.72 or greater would be lighter in weight than its conventional counterpart.

By measuring the vertical distance between the MESAC curve and the conventional curve as shown in Figure 14, it is possible to compute the power-to-weight ratio improvement resulting from the use of MESAC as compared with the conventional system. A plot of the percent improvement

in power-to-weight ratio as a function of reliability for the 100 watt system of Figure 6 is shown in Figure 15.

Variation of the Tradeoff with Cell and Battery Failure Rate

Failure rates in current use at TRW are not firmly supported by a large mass of test data as in the case of most electronic components. This is due to the complexity of battery testing and of analysis of test data from which it is not always possible to determine the true cause of failure, nor to decide in some cases whether or not a physical failure actually occurred. As a result, the failure rate data of Table 1 are a synthesis based upon TRW testing experience, a study of the NAD Crane data, heavily seasoned with the judgement of battery and reliability engineers.

Because the MESAC system depends upon compensating for the poor reliability of the battery cells by the addition of the more reliable electronics, any change in the relationship between cell failure rates and electronic component failure rates will affect the region of applicability of MESAC when compared with a conventional 22-cell battery.

As an example, Figure 16 shows the same MESAC and conventional battery systems as Figures 6 and 14, except that the reliabilities are computed on the basis of failure rates which have been reduced to half the normal values. MESAC is still useful; however, whereas with normal failure rates, the crossover at a reliability of 0.98 occurs at four years, the same crossover at half-normal failure rates does not occur until 5 years and a reliability of 0.98. Thus, should the cells and batteries improve at a rate exceeding the rate of improvement of the electronic components, the advantages of MESAC will tend to be restricted to missions of increasing length.

In view of the increasing requirements for extended life as the size and number of practical applications satellites grow, the usefulness of the MESAC system remains unimpaired regardless of any assumed increase in battery and cell reliability, provided that the relationship between cell failure rates and electronic component failure rates remains constant. Only a marked decrease in battery cell failure rate without a comparable decrease in electronic component failure rate is likely to affect the conclusions significantly.

Variation of the Applicability of the MESAC System with Orbit

When comparing the systems for the synchronous equatorial orbit with those for a 100 minute circular orbit, it becomes clear that the MESAC system shows less weight advantage for the shorter orbits due to the higher current-carrying requirements of both the uplink and downlink converters for the shorter orbit applications. This results in an increased ESU weight and a depressed power-to-weight ratio. Nevertheless, for the lower powered systems (40 to 200 watts) MESAC has distinct advantages in weight over the conventional system at high reliability requirements. When the high powered systems are studied under the restriction of 20 percent DOD, and no cells larger than 20 A-H, it is necessary to use so many ESU's and to increase the number of cells in each ESU to the point where the electronics weight overshadows any other advantages.

SECTION II

CIRCUIT IMPLEMENTATION STUDY

REQUIREMENTS

MESAC circuit design requirements are divided into system requirements and circuit requirements. System requirements deal with the interface of the power source, battery and electronics, and the interface between the MESAC system and power users. Circuit requirements refer to the detailed implementation of system requirements on the circuit and part level.

The circuits shown in Section II are preliminary designs, conceived for the purpose of conducting the tradeoff studies. As such, they do not represent tested designs as do those of Section III, which show actual breadboard circuits.

SYSTEM REQUIREMENTS

MESAC electronics consist of local electronics for each ESU and a central control unit. The central control unit distributes a common battery charge or discharge signal to local electronics depending upon the excess of source power over load power or the excess power requirements of loads over source capacity. Local electronics provide battery charge (downlink conversion) or discharge (uplink conversion) depending upon the central control signal received, terminate charge in response to state of local battery charge, and provide internal current limiting and fault protection. The MESAC system provides a bus voltage arbitrarily selected to be regulated to 28 vdc ±1 percent. Regulation during discharge is accomplished by the uplink converter. Regulation during initial charge is accomplished by the downlink converter using batteries as shunt bus loads. Regulation following charge is provided by a central shunt regulator which may operate either alone or in parallel with downlink converters.

The central control unit provides positive lockout to prevent simultaneous charge of some batteries and discharge of other batteries. System charge power rating is 200 percent of nominal to permit utilization of

source power variations with orbit angle and time of mission life. System discharge power rating is 100 percent or rated load. Both charge and discharge efficiencies are maximum at 100 percent of rating.

Inequality of battery charge currents is acceptable since charge efficiency improves as charge current increases.

Inequality of battery discharge current should be minimized for the following reasons:

1) Battery internal passes increased with increasing current due to the nonlinear nature of the cell polarization curve.

2) Current unbalance on discharge results in excessive discharge of one battery, and lesser discharge of others, leading to an unbalance in residual capacity.

CIRCUIT REQUIREMENTS

Central Control Unit

The central control unit provides a proportional control signal to local uplink converters when bus voltage is in the range of 27.8 to 27.9 vdc, a proportional signal to downlink converters when bus voltage is in the range of 28.0 to 28.1 vdc, and a proportional signal to the central shunt regulator when bus voltage exceeds 28.2 vdc.

Since the central control unit is an in-line element in the MESAC reliability block diagram, reliability should exceed that of all parallel ESU's. As a design goal, high reliability is achieved by internal redundance in each central function so that performance is not degraded by any single part failure.

Weight is minimized to avoid an excessive cover-charge penalty for low power systems. However, in the interest of system standardization it is also desirable to retain a fixed central control unit configuration for all applications. Both of these design goals are considered capable of implementation by limiting central control unit circuits to low power levels, with the exception of the shunt regulator which can utilize existing power source structure for mounting and thermal control.

Local Control Units

Each local control unit consists of an uplink converter and a downlink converter with individual current limiting and fault protection functions.

The weight design goal is 10 percent of associated battery weight. Structure and thermal control weight may be minimized by using existing battery structure for mounting.

The reliability design goal is to exceed associated battery reliability. This goal is approached by the selection of simple circuit configurations with minimum parts count. Power parts are nonredundant to conserve weight and efficiency but small parts may be made redundant if necessary. Circuit performance may be degraded by a part failure. However the ESU must be capable of removing itself from the bus after any failure causing system degradation.

Uplink Converter

The preliminary uplink converter design converts stored battery energy to regulated bus power. Nominal output rating is total system rating divided by the number of ESU's required for system success. Load range was assumed to be 67 percent to 100 percent of nominal load, except where a low ratio of units required to units carried requires a reduced minumum load under normal operating conditions. No transient overload capability is provided in the basic MESAC system; overload capability is discussed further below. Efficiency is maximum at rated load. Rated input voltage is 1.10 to 1.35 vdc per battery cell.

Downlink Converter

The downlink converter converts the excess of source power over load power to battery charge current at a rate required to maintain bus voltage regulation as determined by the central control unit. Nominal output power corresponds with nominal battery charge current; range was assumed to be 67 percent to 200 percent of nominal with maximum efficiency at nominal load. Charge is terminated in response to a signal from a single third electrode as modified by battery temperature. Charge termination control is sufficiently flexible to accept other types of control inputs. Rated output voltage is 1.28 to 1.46 vdc per battery cell.

BASELINE IMPLEMENTATION TRADEOFFS

Baseline Circuit

Selection of a baseline circuit was required to accomplish the parametric system analysis. This baseline circuit was designed to perform all major functions with sufficient optimization of critical criteria discussed below to guarantee valid system analysis results.

Criteria for Selection

Efficiency. High efficiency was considered a primary goal for 100-minute-orbit downlink converters and for uplink converters for all missions. Since no particular tradeoffs appeared to exist for efficiency versus other goals this was simplified to a goal of high efficiency for all converters. Assuming that major controllable losses resulted from power transistor switching and drive, the selected circuit was required to have either inherently or controllably low switching losses and to be capable of accepting a current drive readily. Current drive was considered mandatory for uplink conversion where base current might be as high as 10 percent of input current (battery discharge current). Such high base current in combination with drive voltages approaching battery voltage would result in excessive losses. Ready implementation of current drive was imposed as a requirement to avoid classical current drive problems associated with saturation of power magnetics by slight drive imbalance.

Reliability. Reliability of local converters was to be kept high by minimizing the number of parts, particularly high-power parts.

Where function location was optional in either the central control unit or local ESU's such as a central versus local oscillators, the central location of a single redundant function was preferred over local situation of several nonredundant elements.

Weight. The minimum ESU part count goal for high reliability also provides minimum weight. A particular weight goal was to combine power functions in a single part where possible.

Part Type. The MESAC study was limited to silicon transistors and excluded comparative system analysis of germanium transistor effects. Silicon transistors were selected because faster switching speeds — 0.25 microseconds versus 10 microseconds — placed a minimum limitation on system bandwidth and allowed use of lighter magnetics and filters at higher frequencies. It was recognized that germanium transistors with a saturation voltage of 0.25 versus 0.5 vdc allowed the option of a potential efficiency increase for a given number of series battery cells, or the opportunity to operate fewer cells in series for a given efficiency, if substantially reduced switching frequencies, longer system response time and increased magnetic and filter weight were acceptable.

Baseline System Design

The block diagram of the baseline system is shown in Figure 17. The requirement for close bus voltage regulation of 28 vdc ± 1 percent and the accomplishment of this requirement by selected discharge, charge, and shunt limiting function dictate that the controlling error signal be provided by a common error amplifier. The common amplifier is designated the central load bus error amplifier (LBEA) in the block diagram. It compares load bus voltage to reference voltage ELB (28 vdc); and provides one or the other of two proportional error outputs; Output 1 when bus voltage is less than reference voltage or Output 2 when bus voltage exceeds reference voltage. Output 1 controls the central uplink error amplifier (ULEA), which in turn controls battery discharge through local uplink converter such that bus voltage error is maintained within the range of E_{LB} to E_{LB} $-\Delta E$. Output 2 controls battery charge and shunt limiting functions. The central downlink error amplifier (DLEA) compares Output 2 against reference voltage E1. Load bus voltage error in the range of ΔE to $2\Delta E$ causes the EALB to produce an Output 2 voltage proportional from E1 to 2E1, causing the DLEA to provide an output proportional from zero to full scale. The DLEA output is applied to local downlink converters and controls charge rate to maintain bus voltage in the range of $E_{LB} + \Delta E$ to $E_{LB} + 2\Delta E$. The central shunt regulator error

amplifier (SREA) is referenced to 3E1. Bus voltage error greater than $3\Delta E$ causes Output 2 voltage to exceed 3E1, which in turn causes the SREA to provide a proportional control signal to the central shunt regulator (CSR). The CSR then shunts sufficient source current to maintain bus voltage in the range of $E_{LB} + 3\Delta E$ to $E_{LB} + 4\Delta E$. A guard band equivalent to a load bus error of ΔE prevents combined discharge and charge. A similar guard band prevents combined charge and shunt regulation until the excess of source power over load power exceeds the combined charge current limit. It may be noted that the end of a typical charge cycle will require combined charge and shunt regulation functions as individual batteries reach full charge sequentially and transmit overriding turn-off signals to associated downlinks.

The typical uplink converter (ULC) shown in the block diagram receives primary control from the ULEA as discussed above. A current function is compared to current reference I_1, equivalent to source excess power rating divided by number of ESU's required for mission success, plus a 10 percent margin. Discharge current in excess of the established current limit produces an error signal which is mixed with the central control signal to reduce converter input signal. Transient loads with coarse power quality requirements, such as squibs, may be energized from an auxiliary load bus which is directly connected to batteries through series-redundant blocking diodes. Assuming that no connected load has a nominal power rating exceeding 10 percent of total MESAC rating then 200 percent of nominal power rating is available for transients required by that load, such as for start-up or fuse-clearing. This is a conservative worst-case estimate based on maximum allowable previous ESU failures. If a connected load requires more than 10 percent of total bus power for fuse clearing, fault removal may be possible at reduced bus voltage assuming a current-limited uplink mode and impedance of the faulted unit much lower than that of other normal loads. If the power rating of a single load constitutes a large percentage of total load power, and if that load is intended to draw occasional large power surges in normal operation without extreme bus voltage degradation, the system design should be subject to careful review. But assuming the need is real, such a load might be accommodated by a MESAC system rated for average power

by means of a conventional battery consisting of series cells with voltage rating perhaps 10 percent below regulated bus voltage. It is assumed that discharge energy requirements would be minute and that charge would be accomplished by a dissipative charger operating at a low fixed current.

Baseline Circuit Design

The circuit design of the central control unit is shown in the schematic of Figure 18. Reliability requirements indicate that functions require part or circuit redundancy. The selected implementation consists of binomial 2 of 3 circuit redundancy for low-level analog circuits, and binomial 3 of 4 (quad) redundancy for high power analog and all digital circuits.

Channel A of the 3-channel central load bus error amplifier (LBEA) is shown in zone 5A. Differential amplifier Q309A/B compares bus voltage divided by R311 and R312, with reference voltage zener VR301. Output 1 (bus voltage $<E_{LB}$) is amplified by complementary pair Q307 and Q308 and applied to the LBEA Output No. 1 majority voting gate (MVG) in zone 6A, together with channel B and channel C outputs. It may be shown that the MVG output is unaffected by any single part failure in channels A-C or the gate itself.

The majority voting gate, consists of three parallel paths each varied in impedance by two series-connected transistors. The six transistors are driven by the three error amplifier circuits so that one transistor in each of two of the three legs of the parallel circuit are controlled by each error amplifier circuit. Should any circuit fail so as to cause a shorted transistor (fully on) the remaining transistor in that leg will limit current. Should any circuit fail so as to open those transistors which it controls, at least one of the three legs will still control. The current through the three legs of the majority voting circuit is summed in three parallel resistors, and the output taken as a voltage drop across the resistors. The accuracy of the circuit depends upon the fact that the majority voting gate is part of a large, high gain control loop so that regardless of the nature or extent of the failure which occurs, the external circuit will adjust the output of the gate to the correct level. The gain of the control loop is so much greater than the gain of the voting

network that changes in the voting network gain have no significant effect upon the final result.

The output of Output No. 1 MVG is then amplified by the central uplink error amplifier (ULEA) in zone 6C, and distributed to local uplink converters. Circuit design and redundancy implementation is similar to that of the LBEA.

Output 2 of the EALB (bus voltage $>E_{LB}$) originates as the opposite polarity error signal of differential amplifier Q309A/B (zone 5A). It is amplified by complementary pair Q310 and Q311 and then connected to the Output 2 majority voting gate (MVG) in zone 4A, together with EALB channel B and channel C outputs.

Channel A of the central downlink error amplifier (DLEA) is shown in zone 3A. Reference voltage at VR501 equals E1. When Output 2 from the LBEA gate exceeds E1, corresponding with bus voltage greater than $E_{LB} + \Delta E$, channel A of the DLEA (zone 3A) amplifies the difference. Outputs of channels A-C are then voted through the downlink majority voting gate (zone 2A) and distributed to control charge rate of local downlink converters.

The central oscillator, zone 1B, is a saturating core design. Its output is a square wave with a frequency of approximately 8 kHz, as determined by core characteristics. Semiconductor redundancy is provided by quad transistors for each of two switching elements. The transformer is nonredundant but has a low failure rate of 15 bits/10^9 hr.

Baseline Energy Storage Circuit

A simplified schematic of the energy storage circuit is shown in Figure 20, together with power waveshapes. During the time T_{ON}, Q1 is turned ON by an external signal (not shown) and energy is taken from the source and stored in inductive transformer T_1 by primary winding NP. Diode CR1 is reverse biased and load power is supplied from energy previously stored in capacitor C1. During the time T_{OFF} the external drive signal is removed from Q1, which turns OFF. Inductive energy is removed from the inductive transformer by secondary winding N_S as current I_S. Part of I_S provides load current I_L, and the balance recharges capacitor C1.

It may be shown that $T_{ON}/T_{OFF} = E_{OUT}/E_{IN}\ \ N_p/N_s$. For a given E_{OUT}/E_{IN} ratio, the selection of T_{ON}/T_{OFF} and N_p/N_s ratio is a design option. If T_{ON}/T_{OFF} is low, then peak collector current is high, requiring several parallel transistor chips with reduced reliability. But if T_{ON}/T_{OFF} is high, then transistor turn-off voltage is high, leading to part selection and derating difficulty. A unity T_{ON}/T_{OFF} ratio is selected for a suitable design compromise for parametric study, together with the minimum inductance value required to maintain I_s above zero during T_{OFF}.

A simplified uplink converter (ULC) schematic and power waveshapes are shown in Figure 21. Time scale is exaggerated during transistor turn-off, to display switching loss components. Similar downlink converter (DLC) information is shown in Figure 22.

Baseline Uplink Converter Design

The schematic of the uplink converter (ULC) is shown in Figure 19. The basic components, comparable to the simplified schematic of Figure 21, are transistor Q1, power transformer T3, rectifying diode CR1, and filter capacitor C1. Magnetic amplifier T4 is selected to mix central and local control signals. Its advantages are capability to mix dc-isolated signals, drift-free operation, and high reliability. Inherent disadvantages requiring design care are magnetizing current output in the OFF state, and output rise time slower than that of a comparable semiconductor mixer. AC excitation is supplied to T4 by the central oscillator. Output is normally OFF as the result of resetting bias ampere-turns through resistor R2. Presence of central downlink control signal at resistor R1 provides net control ampere turns to turn T4 output on near the beginning of each period T. A turn-on pulse is then applied to transistor Q1, and discharge energy is stored in power transformer T3. Diode CR1 is reverse-biased, and load power is supplied from energy previously stored in capacitor C1. Regenerative current feedback from current transformer T2 provides continuous drive current to Q1 as demanded by collector current. A turn-off signal is applied to Q1 at time T/2, from the central oscillator through capacitor C3. Inductive energy is then transferred from the primary to the secondary of T3, and secondary current supplies load current and also recharges capacitor C1.

An output voltage signal proportional to discharge current is produced by current transformer T1. When the magnitude of this signal exceeds the VR1 reference voltage, resetting ampere-turns are applied to magnetic amplifier T4 through resistor R3. The ON time of Q1 is then reduced to limit discharge current to 110 percent of nominal rating.

Fuse F1 clears when discharge current exceeds 200 percent of rating as the result of a low impedance converter fault.

Baseline Downlink Converter Design

The schematic of the downlink converter (DLC) is also shown in Figure 19. Design and operation are similar to that of the ULC, except that an input filter (not shown) is required to attenuate ripple current induced on the bus by converter operation. No output filter capacitor is required and local control is added to terminate charge when the battery is fully charged.

A full state-of-charge signal is provided by a third-electrode on the cell connected to the return bus. The cell pressure-sensitive third-electrode potential, nominally 0.25 vdc across a 10 Ω resistor at full charge, is mixed with a temperature function by Schmitt Trigger Q1 and Q2 to provide a digital signal when the battery is fully charged. This signal is amplified by Q3 and employed to short the output of current drive transformer T1. Charge is then terminated until third electrode potential reduces to a selected level nominally 0.1 volt and Q4 drive is reenabled.

PARAMETRIC ANALYSIS

CENTRAL CONTROL UNIT PARAMETRIC DATA

Only the shunt regulator function of the central control unit requires parametric analysis. The balance of the unit consists of a fixed configuration of small parts with negligible power dissipation and constant weight of 4.1 pounds, based on 410 parts with packaged weight of 0.01 pound per part. The weight of the shunt regulator is determined primarily by thermal control considerations. Thermal control must provide sufficient radiation to maintain transistor junction temperatures below 150°C during maximum power dissipation, and sufficient thermal capacity to maintain junction temperatures above -65°C during eclipse. Based on a typical paddle-mounted solar array* with a 50 percent tap for shunt regulation, shunt weight is 0.02 pound per watt of array power. Shunt power dissipation in the OFF mode is less than 10 milliwatts and may be neglected for system parametric studies. Shunt power dissipation in the ON mode is of no interest for other than shunt weight determination since it corresponds with excess solar array power which cannot be utilized either for load operation or battery charging.

ESU CONVERTER PARAMETRIC DATA

Parametric magnetic and filter weight and power dissipation analysis of ESU converters utilizes data in the TRW study on "Power System Component Limitations," Second Quarterly Report, Contract No NAS 7-546.

The LC Filter with High AC Current is functionally equivalent to the input filter in the downlink converter; adjustments are required for differences in RMS currents as shown in Figure 22. Copper weight is adjusted to maintain losses constant while core weight is held constant. It is assumed that losses are entirely in the inductor and are 50 percent copper and 50 percent core. Weight is assumed to be 25 percent copper, 25 percent core, and 50 percent capacitor.

*Worst case thermal control weight requirement.

The LC Filter with High AC Voltage is functionally similar to the energy storage circuit used in the downlink and uplink converters. Adjustments are required for deletion of the output capacitor in the downlink converter, as well as for differences in RMS currents as shown in Figure 21 and inductance value. Loss and weight distribution assumptions and modeling approach are similar to those for the LC filter with High AC Current.

Semiconductor losses are calculated directly. Semiconductor component weight only is included; thermal control weight is assumed to be part of battery structure weight.

Semiconductor losses are calculated from the waveshapes of Figures 21 and 22. Transistors are assumed to be Solitron 2N3599 units, paralleled as required to provide a typical saturation voltage $V_{ce}(SAT)P$ of 0.5 vdc at peak collector current T_{cp}. Rise time T_R and fall time T_F are assumed to vary linearly from 0.25 microsecond for a single 30A unit to 0.40 microsecond for a multiple unit with a nominal rating of 400A. Base-emitter voltage is assumed to be 1.0 vdc constant. Current gain H_{FE} is assumed to be 10. All of the above presumptions are based on typical room temperature data, except for H_{FE} which is worst-case.

Diodes are assumed to be Motorola 1N3909, with a forward drop of 1.0 vdc typical and a reverse recovery time t_{rr} of 0.2 microsecond typical.

Packaging weights assume that the battery structure provides adequate conducted thermal control. Moderate dynamic and EMC requirements are assumed, similar to typical TRW space project requirements. Packaged weight consists of 0.01 pound per part, 1.5 x magnetic and filter weight for output power less than 100 watts or 1.3 x magnetic and filter weight for output power greater than 100 watts, and minimum semiconductor weights, as derived from the component limitations study. Power transistor weight of 0.0015 pound per watt of input power and power diode weight of 0.0015 pound per output watt provide for mounting brackets installed on the battery structure.

UPLINK CONVERTER PARAMETRIC DATA AND DERIVATION OF UPLINK CONVERTER (ULC) EQUATIONS

The schematic of the ULC is shown in Figure 21; power waveshapes are also shown in Figure 21.

T_{ON} is selected equal to T_{OFF} at 100 percent rated load, and turns ratio NP/NS is designed accordingly for each battery voltage NEB and 28 vdc constant bus voltage. The selection of unity T_{ON}/T_{OFF} ratio is a compromise between excessive peak collector current for low T_{ON}/T_{OFF}, and excessive collector voltage for high T_{ON}/T_{OFF}.

$$\eta_{ULC} = \frac{P_{OUT}}{P_{IN}} \tag{1}$$

$$P_{IN} = NE_B \times I_B \tag{2}$$

$$P_{OUT} = P_{IN} - \left[P_Q + P_D + P_T + P_c\right] \tag{3}$$

$$P_Q = P_{ONQ} + P_{OFFQ} + P_{SATQ} + P_{DRIVE\ Q} \tag{4}$$

$$P_{ONQ} \sim 0 \tag{5}$$

$$P_{OFFQ} = f\int_o^{T_F} 2NE_B \times \frac{4I_B t}{T_F}\, dt = 4fNE_B I_B T_F \tag{6}$$

$$P_{SATQ} = f\int_o^{T/2} \frac{4I_B t}{T/2} \times \frac{0.5}{T/2}\, t\, dt = \frac{I_B}{3} \tag{7}$$

$$P_{DRIVE\ Q} = 1.1_{TRANSFORMER\ LOSS} \times f\int_o^{T/2} \frac{4I_B t}{10} \times 1.0\, dt = 0.11\ I_B \tag{8}$$

$$P_D = P_{OND} + P_{OFFD} + P_{SATD} \tag{9}$$

$$P_{OND} \sim 0, \text{ for } f \leq 64 \text{ kHz} \tag{10}$$

$$P_{OFFD} \sim 0, \text{ for } f \leq 64 \text{ kHz} \tag{11}$$

$$P_{SATD} = f\int_o^{T/2} 41_B \frac{NE_B}{E_{OUT}} \times \frac{1}{T/2}\, t\, V_{Fdt} = \frac{I_B NE_B}{28} \tag{12}$$

$$P_T + P_C = P_{CL} \tag{13}$$

$$W = (W_T + W_C)\, K_1 + W_O + W_D + W_P \tag{14}$$

$$W_T = W_{CORE} + W_{COPPER} \tag{15}$$

$$W_{CORE} = \frac{W_{CL}}{4} \tag{16}$$

$$W_{COPPER} = \frac{W_{CL}}{4} \times \frac{\eta_{ULC}}{CL} \times \frac{I_{RMS\text{-}ULC}^{\,2}}{I_{RMS\text{-}L}} \tag{17}$$

$$\frac{\eta_{ULC}}{\eta_{CL}} = \frac{L_{ULC}}{L_{CL}}^{1/2} \times 2 \tag{18}$$

$$L_{CL} = \frac{E_o T}{6 I_{o\ MIN}} = \frac{0.83 E_o T}{I_o} \tag{19}$$

$$L_{ULC} = \frac{E_o \times T/2}{4 I_o} = 0.125 \frac{E_o T}{I_o} \tag{20}$$

$$I_{RMS\text{-}CL} \sim I_o \tag{21}$$

$$I_{RMS\text{-}ULC} = \frac{2 I_o}{\sqrt{6}} \tag{22}$$

$$W_C = \frac{W_{CL}}{2} \times \frac{C_{ULC}}{C_{CL}} \tag{23}$$

$$C_{CL} = \frac{I_{o\ MIN} T}{2 E_{opp}} = 80 \frac{I_o T}{E_o} \tag{24}$$

$$C_{ULC} = \frac{\int i\,dt}{E_{opp}} \frac{I_o \times T/2 \times I_o/2 \times T/6}{E_{opp}} = 230 \frac{I_o T}{E_o} \tag{25}$$

Summarizing Equations (14) through (25)

$$W_T + W_C = 2.2 \times W_{CL} \tag{26}$$

$$K_1 = 1.5 \text{ for } P_{OUT} < 100 \text{ watts} \quad (27a)$$

$$K_1 = 1.3 \text{ for } P_{OUT} > 100 \text{ watts} \quad (27b)$$

$$W_o = 0.0015\ P_{IN} \quad (28)$$

$$W_D = 0.0015\ P_{OUT} \quad (29)$$

$$W_P = 0.22 \quad (30)$$

Nomenclature

Terms are listed in order of appearance in equation derivation. Orbit variable terms represent average values over an eclipse period.

η_{ULC}	uplink converter efficiency
P_{OUT}	output power to load bus, watts
P_{IN}	input power from battery, watts
N	number of cells
E_B	cell voltage, volts
I_B	current, amperes
P_Q	total transistor loss, watts
P_{ONQ}	transistor turn-on loss, watts
P_{OFFQ}	transistor turn-off loss, watts
P_{SATQ}	transistor saturation loss, watts
P_{DRIVEQ}	transistor drive loss, watts
f	switching frequency, Hertz
T_f	transistor fall time, seconds
P_D	total diode loss, watts
P_{OND}	diode turn-on loss, watts
P_{OFFD}	diode turn-off loss, watts
P_{SATD}	diode forward loss, watts
P_T	power transformer loss, watts
P_C	filter capacitor loss
P_{CL}	equivalent high ac voltage filter loss from Component Limitations study

W	uplink converter weight, pounds
W_T	transformer weight, pounds
W_C	capacitor weight, pounds
W_Q	transistor and bracket weight, pounds
W_D	diode and bracket weight, pounds
W_{Pc}	part count package weight, pounds
W_{core}	transformer core weight, pounds
W_{copper}	transformer copper weight, pounds
W_{CL}	weight of equivalent high ac voltage filter from Component Limitations study
L_{ULC}	transformer inductance, Henries
L_{CL}	high ac voltage filter inductance from Component Limitations study, Henries
E_o	output voltage, watts
I_o	output current, amperes

DOWNLINK CONVERTER PARAMETRIC DATA DERIVATION OF DOWNLINK CONVERTER (DLC) EQUATIONS

The schematic and waveshapes of the downlink converter are shown in Figure 22. Downlink equations differ from uplink equations as follows:

- An input filter is added to attenuate ripple current induced on the bus.
- The energy storage circuit output capacitor is deleted, since high ripple current is acceptable to the battery.
- The energy storage transformer is sized for operation at 200 percent of power rating.
- Alternate calculations are provided for a synchronous rectifier in place of the diode rectifier. The computer program selects the more efficient, subject to voltage limitations corresponding with a maximum of three series cells.

$$\eta_{DLC} = \frac{P_{OUT}}{P_{OUT} + P_L + P_C + P_Q + P_T + P_D} \tag{1}$$

$$P_L = P_{CL} \text{ (LC FILTER WITH HIGH AC CURRENT)} \tag{2}$$

$$P_C \sim 0 \tag{3}$$

$$P_Q = P_{ONQ} + P_{SATQ} + P_{OFFQ} + P_{DRIVEQ} \tag{4}$$

$$P_{ONQ} \sim 0$$

$$P_{SATQ} = f\int_0^{0.36T} \frac{5.6\, I_B \times (NE_B + 0.9)\, t}{28 \times 0.36T} \times \frac{0.5t}{0.36T}\, dt$$

$$= 0.012\, I_B(NE_B + 0.9) \tag{6}$$

$$P_{OFFQ} = f\int_0^{T_F} \frac{5.61_B\, (NE_B + 0.9)\, t}{28 \times T_F} \times 56\, dt$$

$$= 5.6\, fI_B(NE_B + 0.9)\, T_F \tag{7}$$

$$TF = \left[0.25 + 5.6\, I_B \times \frac{(NE_B + 09)}{28} \times 0.05\right] \times 10^{-6} \tag{8}$$

$$P_{DRIVEQ} = f \int_{o}^{0.36T} \frac{5.6\, I_B (NE_B + 0.9)\, t}{28 \times 0.36T \times 10} \times 1.0\, dt \qquad (9)$$

$$= 0.0039\, I_B (NE_B + 0.9)$$

$$P_T = P_{CL} \text{ (LC FILTER WITH HIGH AC VOLTAGE)} \qquad (10)$$

$$P_D = P_{OND} + P_{SATD} + P_{OFFD} \qquad (11a)$$

$$P_{OND} \sim 0 \qquad (12a)$$

$$P_{SATD} = 0.91\, I_B \qquad (13a)$$

$$P_{OFFD} \sim 0 \qquad (14a)$$

$$P_D = P_{SR} = P_{ONSR} + P_{SATSR} + P_{OFFSR} + P_{DRIVESR} \qquad (11b)$$

$$P_{ONSR} = 1.9\, f I_B NE_B T_R \qquad (12b)$$

$$T_R = \left(0.25 + \frac{5.6\, I_B}{100} \times 0.5\right) \times 10^{-6} \qquad (13b)$$

$$P_{SATSR} = 0.34\, I_B \qquad (14b)$$

$$P_{OFFSR} \sim 0 \qquad (15b)$$

$$P_{DRIVERSR} = f \int_{o}^{0.36T} \frac{5.6\, I_B\, t}{10 \times 0.36\, T} \times 1.0 \times 1.1_{\text{DRIVE TRANSFORMER}}\, dt$$

$$= 0.11\, I_B \qquad (16b)$$

$$W = (W_L + W_C + W_T)\, K_1 + W_Q + W_D + W_P \qquad (17)$$

$$W_L + W_C = W_{CL} \text{ (LC FILTER WITH HIGH AC CURRENT)}, \qquad (18)$$

where $P_{CL} = 1.5\, P_{IN}$

$$W_T = 1.1\, W_{CL} \text{ (LC FILTER WITH HIGH AC CURRENT),} \tag{19}$$

$$\text{where } P_{CL} = P_{OUT} \tag{20}$$

$$K_1 = 1.5 \text{ for } P_{IN} < 100 \text{ watts} \tag{20b}$$

$$K_1 = 1.3 \text{ for } P_{IN} > 100 \text{ watts} \tag{21}$$

$$W_Q = 0.0015\, P_{IN} \tag{22a}$$

$$W_D = 0.0015\, P_{OUT} \tag{22b}$$

$$W_D = W_{SR} = 0.0015\, P_{OUT} + 0.13 \times W_T \tag{23}$$

$$W_P = 0.28$$

Nomenclature

DLC	downlink converter efficiency
P_L	power loss in LC high ac current filter, watts
P_Q	total transistor power loss, watts
P_{ONQ}	transistor turn-on loss, watts
P_{SATQ}	transistor saturation loss, watts
P_{OFFQ}	transistor turn-off loss, watts
P_{DRIVEQ}	transistor drive loss, watts
T_F	transistor fall time, seconds
P_T	transformer loss, watts
P_D	total diode loss, watts
P_{SATD}	diode forward loss, watts
P_{SR}	total synchronous rectifier loss
P_{ONSR}	synchronous rectifier turn-on loss, watts
P_{SATSR}	synchronous rectifier saturation loss, watts
P_{OFFSR}	synchronous rectifier turn-off loss, watts
$P_{DRIVESR}$	synchronous rectifier drive loss, watts
W	total downlink converter weight, pounds
W_T	transformer weight, pounds
W_C	capacitor weight, pounds
K_1	magnetic and capacitor packaging factor
W_Q	transistor weight, pounds
W_D	diode weight, pounds
W_{SR}	synchronous rectifier weight, pounds
W_P	part count package weight, pounds

DETAILED CIRCUIT IMPLEMENTATION TRADEOFFS

System Tradeoffs

Independent Versus Interrelated Current Limits. Interrelated current limits refer to a demand selection of local converter current limits based on total charge or discharge power and number of operating ESU's. The advantage of this design is that converter currents would always be equal at any total current; system discharge efficiency would always be optimum, and system thermal gradients would be minimum. The disadvantage of limit interrelation is that transient load capability is reduced and that reliability is reduced to the extent that failures can propagate among ESU's. Conventional current monitor cross-strapping reduces reliability since the current monitor of each ESU would be added in series with the system reliability block diagram. Upgrading the reliability of the ESU monitor with redundancy to minimize this reliability reduction would add substantial ESU weight. A redundant operational amplifier could be installed in the central control unit to sum individual ESU current level signals and return an average reference signal to each ESU for comparison and control. While preferable to conventional cross-strapping, this approach still adds finite cable weight and connection failure probability.

The disadvantage of independent current limit selection is that the limit must be permanently established at the highest required value, corresponding with maximum charge or discharge rate, and minimum allowable surviving ESU's. Under normal operating circumstances moderate to large current divergences are then possible, with resulting system thermal gradients and reduction of discharge efficiency. The advantages of independent limits are simplicity, maximum reliability and constant maximum available transient overload capability. This is the selected design.

Dissipative Shunt Versus Shunt Switch. The dissipative shunt selected for the baseline circuit represents standard TRW technology. Reliability of the power element exceeds 0.9999 for 6 years as a result of series-parallel redundancy. Weight ranges from 4 percent of solar array

weight for a spherical body-mounted solar array to 7 percent for a paddle-mounted array. The additional parts required for redundancy contribute little to the SEA weight, but do add frequency stabilization difficulty owing to large gain variations between normal and failure mode operation. The selection of a tapped shunt regulation point to minimize shunt dissipation and weight also limits the regulation range of the shunt. It is typical design practice to rely on battery clamping action rather than shunt regulation to limit the output voltage of a paddle-mount array immediately after eclipse when the array temperature is minimum and output voltage maximum.

Converter Circuit Design Tradeoffs. Several circuit types were evaluated prior to the selection of the single-ended energy storage circuit for the baseline converter circuit design. These circuits are reexamined below for a specific MESAC configuration, the 24-hour synchronous orbit application of the 20 AH cell, six cells in series with 8 kHz conversion frequency. The configuration of the single-ended energy storage circuit is also varied to consider the effects of increased inductance and a double-ended modification. In general, the weight and efficiency differences between candidate circuits are too small to be of major significance and the decision to implement one circuit over another is partially based on reliability consideration, part count, and ease of implementation.

Pulsewidth Downlink Regulator. A pulsewidth downlink regulator has a slight weight advantage over the energy storage converter since it requires only an output filter inductor rather than an inductive transformer. However this weight advantage is more than offset by the requirement for an input filter capable of attenuating additional induced ripple current corresponding with the ratio of bus to battery voltage, or 3.5. Transistor turnoff loss P_{QOFF} is increased by a factor of

$$\frac{E_{IN} \times 6.9\, I_B}{2E_{IN} \times 4I_B \times \frac{NE_B}{E_{IN}}} = 3.0$$

P_{QSAT} and transistor failure rate are both increased by a factor of 6.0, because peak transistor current equals peak output current, without the benefit of impedance transformation provided by a transformer.

Push-Pull Downlink Converter. The push-pull downlink converter provides efficiency and weight virtually the same as those of the baseline circuit modified to a double-ended configuration, neglecting a slight weight disadvantage resulting from separation of transformer and inductor functions into separate parts. Implementation of current drive requires particular design care to preclude saturation of the ungapped power transformer; this is considered an inherent weakness compared to the baseline circuit.

Boosting Uplink Converter. A boosting auto transformer uplink converter has a slight weight advantage and a theoretical efficiency advantage over the baseline uplink modified to a double-ended configuration. For the selected comparison configuration, transistor turn-off loss is decreased by the ratio of transistor turn-off voltage to comparable baseline voltage, or,

$$\frac{E_B\left(1 + \frac{E_B}{E_{OUT}}\right)}{2E_B} = 0.6$$

But this loss reduction applies only at the battery voltage selected as minimum discharge voltage.

Assuming a reasonable design safety margin is applied, total losses may actually increase at nominal battery discharge voltage, when battery current is conducted during transistor off time through an 1.0 volt bypass diode voltage drop versus an 0.5 volt transistor voltage drop. Transformer weight is decreased 40 percent by the auto-transformer connection; but the weight of a separate inductor holds the total magnetic weight decrease to approximately 20 percent. The boosting uplink converter has the distinct disadvantage of a direct diode connection between the battery and bus which would require special failure mode protection or inefficient series diode redundancy. While this would not normally disqualify the circuit, it was felt that the implementation problems were more severe than those of the energy storage converter.

Push-Pull Uplink Converter. As with push-pull downlink converter considerations, weight and efficiency are virtually the same as those of the baseline circuit modified to a double-ended configuration. Increased difficulty of proper current drive implementation is considered an inherent design weakness compared to the baseline uplink.

Baseline Circuit Modifications. The foregoing review of other circuit approaches indicates that the baseline circuit selection is sound. It is now worthwhile to investigate minor modifications of the selected energy storage circuit while still retaining its tolerance of moderate dc bias.

Selection of Optimum Inductance Value. The value of the baseline inductance was selected to be the minimum value capable of maintaining inductor current above zero when the converter operates into maximum rated load. Rationale was that minimum inductor weight consistent with regulation capability would result in minimum total converter weight. Considering that power transistor failure rate is proportional to the number of parallel chips required to provide the selected 0.5 vdc maximum VDC (SAT) at peak collector current, and that transistor failure rate represents a substantial part of total ESU failure rate for higher rated MESAC systems, the effects of increased inductance and reduced peak currents are investigated.

For an uplink converter inductance increase of 100 percent and core and copper weight held constant, it may be shown that the transistor failure rate is reduced 25 percent, copper losses are decreased 21 percent, and capacitor weight is reduced 10 percent. It is concluded that the inductance selected for the baseline circuit should be increased approximately 100 percent. It may be noted that further inductance increase pays diminishing returns and eventually increases weight or losses; there is undoubtedly an optimum range for each specific MESAC system.

Single Versus Double-Ended Configuration. A double-ended energy storage converter consists of two single-ended units which share a common output filter capacitor. Double-ended reconfiguration of the baseline

uplink circuit, keeping efficiency constant, results in the following major changes:

- Weight of power parts is reduced 25 percent as the result of 50 percent filter capacitance decrease.
- Weight of small parts is increased 0.1 pound since individual drive circuit part count is doubled.
- Failure rate of small parts is increased approximately 30 percent.

The double-ended circuit is clearly a strong candidate for high power MESAC systems. If the weight of the uplink converter exceeds 1.2 pounds, part of the filter weight saving can be used for a redundant drive circuit. The net result would be lower weight and equal or better reliability.

Degree of Control Centralization

The basic control functions which are performed by the central control unit and by the local ESU's are as follows:

Central Control Functions:

1) Measurement of the bus voltage error, and generation of a control signal for distribution to the ESU's.

Local Control Functions:

1) Current limiting
2) Termination of charge upon receipt of a "full charge" signal from the auxiliary electrode
3) Variation of the power output of the up or down converters in response to the control signal.

The nature of the control signals, and the degree of localization of the oscillator(s), modulator(s) are not inherent in the MESAC design and are therefore subject to further tradeoffs.

Maximum Control Centralization

At one extreme, maximum control centralization may be used. In this form, a redundant central oscillator is used to provide the frequency excitation, and a central modulator is used which, in response to the bus voltage error signal from the central control unit, produces

a variable pulsewidth signal which is distributed to all ESU's used to control the switching on-off times of all of the ESU's uniformly.

This control system eliminates or minimizes local differences in control system gain, and produces the greatest degree of inherent current sharing in both charge and discharge, the sole divergent influence being the differences in battery voltage. However, it necessitates the development of internally redundant oscillator and modulator circuitry. In addition, it also requires the addition of a local pulsewidth signal modulator for implementation of the local current limit function and of the charge control function, thus duplicating the redundant central modulator with a nonredundant local one (see Figure 23).

Modulator Decentralization

Since in the system of Figure 23 the local modulator can readily combine the control functions of current limiting, charge control, and bus voltage control, it is possible to reduce the total part count by eliminating the central modulator entirely, distributing an analog dc signal to the local modulators at the penalty of some nonuniformity of bus voltage control gain between the several energy storage units. This will tend to result in poorer sharing of current on both charge and discharge, and in a lessening of a tendency of the battery currents to converge. It does, however, result in a significant reduction in the part count (and therefore the weight) of the central control unit (see Figure 24).

Oscillator Decentralization

A further savings in part count may be achieved by utilization of circuit designs which combine the functions of the oscillator and modulator in a single circuit. By use of a variable-frequency astable oscillator with a constant ON time, and a variable OFF time, the oscillator and modulator functions can be combined, for further part count reduction. The frequency of operation of each of the energy storage units is controlled by the OFF time, decreasing with decreasing current until the converter or regulator is completely turned off when the current reaches 0 (see Figure 25).

SECTION III

MESAC BREADBOARD

SELECTED BASELINE DESIGN

The schematic diagram of the selected baseline design is shown in Figure 18 (CCU) and Figure 19 (ESU). Significant features affecting baseline weight and reliability data are:

- A central CCU oscillator versus local ESU oscillators to minimize ESU weight
- ESU control by a magnetic amplifier, in which CCU and local current limit and charge control inputs are mixed. Magnetic amplifier excitation is supplied by the central oscillator, leading to constant frequency, variable ON/OFF time ratio control of ESU converter.
- Current limit control by means of negative feedback after a preset limit is exceeded
- A transformer-coupled energy-ladle configuration for both uplink and downlink converters. An advantage is flexibility of transformer turns ratio, and hence flexibility in transistor current and voltage ratio. A disadvantage not thoroughly appreciated in December 1958 is the practical difficulty of designing an uplink converter with acceptably close primary-secondary coupling.
- Inductance equal to minimum value capable of maintaining inductor current above zero, during operation into maximum rated load impedance.

EVOLUTION OF SELECTED BASELINE DESIGN INTO FINAL DEVELOPED SYSTEM

Local Timing Core

The central oscillator was changed to a local oscillator or "timing core" in the detail design of April 1969, discussed April 1969 during the trip made to NASA by TRW personnel, and both control and current limit functions were incorporated into this oscillator. Constant frequency operation was changed to a virtually constant ON time, and an OFF time controlled by the central control signal and a local feedback signal.

An advantage over the previous design was improved current limit accuracy, resulting in less oversizing required for the power transformer and power transistor. Another advantage was improved current limit response time. OFF time was maintained until transformer current decayed to a preset level, providing a controlled current level at the beginning of the next ON time.

All-Electronic Control

Making use of tradeoff studies just performed in another TRW design area for another project, the April timing core approach was replaced by a combined Schmitt Trigger astable multivibrator control for uplink and downlink converters in May 1969. The astable provided a fixed OFF time directly, and a variable ON time as determined by a synchronizing signal provided by the Schmitt Trigger. Schmitt Trigger input was the central control signal mixed with a current limit signal.

Advantages of this approach over the timing core design were as follows:

- Electronic control provided faster rise time resulting in more efficient power transistor switching
- Modification of ON time by the current limit signal allowed zero design margin for the power transformer and transistor since ON time was terminated precisely at part rating.

Inductor for Uplink

Lack of unity coupling between primary and secondary windings of the power transformer caused severe switching dissipation in the uplink converter and inability to load output up to power rating. Careful transformer design and manufacture failed to reduce this leakage inductance to an acceptable level. Power conservation circuits were considered in an effort to store and release the above dissipation at appropriate times during the switching cycle. However, considerable complexity was introduced by those conservation circuits, and conservation itself was imperfect in this difficult low-voltage, high-current circuit application.

Since no system considerations precluded battery grounding, a simple expedient was selected. The inductive power transformer of the uplink converter was replaced with a single-winding inductor in the final power circuit configuration, and the leakage inductance problem was circumvented for the uplink.

Fixed ON Time

The ON time was next made fixed and the OFF time variable to provide explicit OFF time control and eliminate spurious OFF time termination by noise.

FUNCTIONAL DESCRIPTION OF FINAL DEVELOPED SYSTEM

A block diagram of the MESAC system is shown in Figure 26.

It consists of the following building blocks:

(1) Load bus error amplifier (LBEA)
(1) Uplink error amplifier (ULEA)
(1) Downlink error amplifier (DLEA)
(1) Central shunt error amplifier (CSEA)
(1) Central shunt regulator (CSR)
(3) Energy storage units (ESU's)

Each ESU includes one battery, one uplink converter (ULC), one downlink converter (DLC), one current limiting circuit for each converter, and one third electrode sensor in conjunction with the DLC.

There are three distinct modes of operation.

In eclipse, the ULC's provide the power to the load. Two of the ULC's are sufficient to deliver 110 w full power. Each converter is current limited in order to avoid excessive unbalance of the batteries due to improper current sharing.

During this period the system is in its first regulation mode, and an error signal $E = A(E_{LB} - E_R)$ appears at the output of the LBEA. Where E_{LB} is the load bus voltage, E_R is the load bus reference voltage and A is the gain of the LBEA. This signal E is compared to an uplink reference voltage E_{R1} and another error voltage $E_1 = A_1 (E - E_{R1})$ appears at the output of the ULEA, controlling the OFF time of the ULC's, and thus the load bus voltage is regulated. A_1 is the gain of the ULEA.

As the solar array (SA) output increases, similarly does the OFF time of the ULC's, and the load current is now shared by both the SA and the ULC's.

Finally the OFF time of the ULC's becomes infinity and the total load power is provided by the SA alone. Under this condition the ULEA is saturated and the load bus is no longer regulated by this loop.

This zone of no regulation occurring between two modes is called the "guard band," and can be specified in voltage: 20 ±10 mv.

Further increase of the SA output power then permits the excess power not required by the load to charge the batteries through the DLC's.

In this second mode of operation the load bus voltage E_{LB} first must reach a new threshold value $E_R + E'_{R2}/A$. Above this value an error signal, $E_2 = A_2 (E_{R2} - E)$, acts on the inputs of the DLC's to create a new regulation loop where E_{R2} is the DLEA reference voltage and A_2 is the gain of the DLEA.

When E_{LB} reaches $E_R + E_{R2/A'}$ at which time the DLEA error signal $E_2 = A_2(E_{R2} - E)$ is zero, the DLC's are operating with the shortest possible OFF time, at maximum charge current and possibly in a current limiting mode.

A further increase of array output causes E_{LB} to exceed the shunt threshold value of $E_R + E_{R3}$, and an error signal $A_3 (E - E_{R3})$ appears at the output of the CSEA, which in turn provides an input current to the CSR, thus completing the feedback loop for the third or shunt mode of operation. A_3 is the CSEA gain, and E_{R3} the CSEA reference voltage.

Overlap of the downlink and shunt regulation is avoided by a second guard band between the two modes which ensures that the DLC is fully on before the SEA begins to turn on.

The three error signals E_1, E_2, and E_3 are shown in Figure 27 in relation to E and the load bus voltage E_{LB}. Only one feedback loop, involving one of the error signals E_1, E_2, or E_3, is in an active mode at one time.

The function of the third electrode sensor associated with each battery is to terminate charging whenever the third electrode voltage reaches 100 ±30 mv.

Uplink Converter

Loop Function

Further details of a typical ULC are shown in Figure 28. It is basically a boost converter with voltage ratio determined by the ON time t_{on} and OFF time t_{off} of the transistor switch S.

Relevant current waveforms are shown in Figure 29 for a steady-state condition in the active region of the uplink feedback loop when the error voltage from the ULEA is E_1. The ULC is delivering an average current I_B from the battery.

During the switch ON time t_{on}, the instantaneous current i_s through the switch is given by:

$$i_s = I_B + \frac{E_B}{L}\left(t - \frac{t_{on}}{2}\right) \tag{1}$$

where

E_B = battery voltage

L = inductance

I_0 = average load current

I_B = average battery current

The basic relation of I_B to I_0 is:

$$\frac{I_B}{I_0} = 1 + \frac{t_{on}}{t_{off}} \tag{2}$$

An equivalent relationship exists between the load bus voltage E_{LB} and the battery voltage E_B:

$$\frac{E_{LB}}{E_B} = 1 + \frac{t_{on}}{t_{off}} \tag{3}$$

Functional Description of a Typical ULC

The detailed circuit of the ULC and its drive circuitry is shown in Figure 30.

Equation (2) gives the required maximum on-off ratio as:

$$\frac{t_{on}}{t_{off}} = \frac{E_{LB}}{E_B} - 1$$

for E_B = 6 v and E_{LB} = 27 (see Section IV, paragraph 3 for the choice of the numbers).

$$\frac{t_{on}}{t_{off}} = \frac{27}{6} - 1 = 4.5 - 1 = 3.5$$

$$t_{off} = 0.286\, t_{on}$$

Since t_{on} is constant and t_{off} is controlled by the feedback loop of the regulator:

$$0.286\, t_{on} \leq t_{off} \leq \infty$$

throughout the operation of the ULC.

The main power switch is Q_1.

To maintain maximum efficiency, current feedback drive is used for Q_1 through transformer T_1. The feedback turns ratio N_2/N_1 must be large enough to keep Q_1 in saturation during t_{on}. A square-loop core material is chosen for T_1 to give minimum leakage inductance, and therefore sharp transitions between the two switch states.

Turn-on is initiated when Q_{10}, the output of the astable oscillator, switches on. This is differentiated by C_2 to provide a turn-on current pulse to Q_3, which saturates, thereby applying the battery voltage E_B across N_3. A positive voltage $E_B(N_1/N_3)$ is then applied to the base of Q_1, which is sufficiently greater than the normal $V_{BE(ON)}$ (base-emitter voltage in the ON condition) to ensure rapid turn-on. As the current drive pulse to Q_3 decays, the positive current feedback from N_2 to N_1 maintains Q_1 on.

Throughout the ON time, Q_2 and Q_4 are off, and $t_{on}\ V_{BE(ON)}/N_1$ volt-seconds per turn are stored in the core of T_1, which must not saturate during t_{on} available from the astable oscillator.

Turn-off of Q_1 is initiated when the Q_9 switches on. This is differentiated by C_3 to provide a turn-on current pulse to Q_4, which saturates, thereby applying the battery voltage E_B across winding N_4. A low-impedance turn-off drive is applied to the base of Q_1 to withdraw the stored base charge and to cause sharp turn-off.

As soon as Q_1 turns off, the (negative) base current falls abruptly to zero, and Q_4 must supply only the reset magnetizing current in N_4.

Since $t_{on}\ V_{BE(ON)}/N_1$ volt-seconds per turn were previously stored, the reset time t_r is given by:

$$\frac{t_r E_B}{N_4} = \frac{t_{on} V_{BE(ON)}}{N_1} \tag{4}$$

or

$$t_r = t_{on} \frac{N_4}{N_1} \frac{V_{BE(ON)}}{E_B} \tag{5}$$

The reset time t_r must be less than the OFF time t_{off}, to ensure that T_1 is indeed reset; otherwise T_1 will eventually saturate in the other direction and will prematurely terminate the ON time. This condition places an upper limit on the turns ratio N_4/N_1:

$$\frac{N_4}{N_1} < \frac{t_{off}}{t_{on}} \frac{E_B}{V_{BE(ON)}} = \frac{E_B^2}{(E_{LB} - E_B) V_{BE(ON)}} \tag{6}$$

During T_1 reset, the reverse voltage applied to the base of Q_1 is $E_B(N_1/N_4)$ and this must be less than the reverse base-emitter breakdown voltage, BV_{BER}. Hence there is also a lower limit on the ratio N_4/N_1:

$$\frac{N_4}{N_1} > \frac{E_B}{BV_{BER}}$$

Consequently, N_4/N_1 must be chosen in the range

$$\frac{E_B}{BV_{BER}} < \frac{N_4}{N_1} < \frac{E_B^2}{(E_{LB} - E_B) V_{BE(ON)}} \tag{7}$$

At the end of the reset time t_r, less than the OFF time t_{off}, the core saturates and the voltage across all windings collapses. Because of the reset magnetizing current previously flowing in N_4, the voltage does not collapse to zero, but tends to overshoot in the opposite direction. The

function of Q_2 is to prevent the resulting premature turn-on Q_1 at the end of the reset time t_r; Q_2 is on throughout the OFF time t_{off}, and the reset overshoot voltage is clamped by CR_2.

Resistor R5A is included to ensure that Q_4 continues to provide the reset current to N_4 while remaining saturated.

The circuit consisting of Q_{11}, Q_{12}, Q_{13}, and Q_{14} is a collector-coupled astable multivibrator. The constant on-time (t_{on}) portion of the cycle is determined by the RC product of R_{23A}, R_{23B}, and C_6: $t_{on} = 0.69 \times (R_{23A} + R_{23B}) C_6$. Adjustment of t_{on} is available by potentiometer R_{23A}.

The controlled OFF time of the cycle is fixed by the product of C_7 and R_{34} in series with the impedance of Q_7.

If there is no voltage input either from the ULEA via CR_8, or from the current limiting via CR_7, the astable runs with the shortest OFF time t_{off} 0.3 t_{on}, due to the biasing arrangement of Q_7 in connection with the circuits of Q_5 and Q_6. The adjustment of the OFF time is done by potentiometer R_{35}.

The error signal from the ULEA provides a reverse bias to the emitter of Q_6, which reduces the base and collector currents of Q_6 and Q_7, thereby causing the increase of the impendance of Q_7 and the OFF time of the astable. The length of the OFF time is proportional to the voltage level from the ULEA.

For an input voltage greater than 4 volts, Q_6 and Q_7 are reverse biased and the astable oscillator is off.

The current limiting circuit consists of current transformer T_2, CR_6, C_4 and "set-in-test" resistor R_{37}.

R_{37} is adjusted so that for a battery current greater than 13.5 A, a reverse bias is applied to the emitter of Q_6 through CR_7, which causes an increase of the OFF time of the astable oscillator and thereby the current limiting of the ULC.

Downlink Converter

Loop Function

Further details of a typical DLC of Figure 26 are shown in Figure 31.

It is basically a buck-converter, with the voltage ratio determined by the relation:

$$\frac{E_B}{E_{LB}} = \frac{N_S}{N_p} \frac{t_{on}}{t_{off}} \tag{8}$$

Relevant waveforms of the currents and voltages are shown in Figure 32 for a steady-state condition in the active region of the downlink feedback loop, when the error voltage from the DLEA is E_2.

Functional Description of a Typical DLC

The detailed circuit of the DLC and its drive circuitry is shown in Figure 33.

A functional description of the circuits in the DLC, identical to that of the ULC, is omitted here and a reference is made to paragraph 2.2 for details.

The downlink is used as a buck converter with a power transformer having a 1:1 turn ratio.

For E_{LB} = 27 v and E_B = 7.5 v, equation (B) gives the required on-off ratio:

$$\frac{t_{on}}{t_{off}} = \frac{E_B}{E_{LB}} = \frac{7.5}{27} = 0.278$$

$$t_{on} = 0.278\, t_{off}$$

The reset time t_r is given by equation:

$$\frac{t_r E_{LB}}{N_4} = \frac{t_{on} V_{BE(ON)}}{N_1}$$

or

$$t_r = t_{on} \frac{N_4}{N_1} \frac{V_{BE(ON)}}{E_{LB}}$$

t_r must be less than the OFF time t_{off} to ensure that T_1 transformer is indeed reset. This condition places an upper limit on the ratio N_4/N_1:

$$\frac{N_4}{N_1} < \frac{t_{off}}{t_{on}} \quad \frac{E_{LB}}{V_{BE(ON)}} = \frac{E_{LB}^2}{E_B V_{BE(ON)}} \tag{9}$$

During T_1 reset, the reverse voltage applied to the base of Q_1 is E_{LB} (N_1/N_4), and this must be less than the reverse base-emitter breakdown voltage BV_{BER}. Hence there is also a lower limit on the ratio N_4/N_1:

$$\frac{N_4}{N_1} > \frac{E_{LB}}{B V_{BER}}$$

Consequently, N_4/N_1 must be chosen in the range:

$$\frac{E_{LB}}{E V_{BER}} < \frac{N_4}{N_1} < \frac{E_{LB}^2}{E_B V_{BE(ON)}} \tag{10}$$

The basic function of the downlink astable multivibrator is the same as that of the uplink, except the OFF time control circuit has an additional input from the third electrode sensor (TES).

The TES, consisting of an operational amplifier, is a level detector which receives an analog input from the third electrode of the battery and provides a digital voltage through VR_2, R_{39}, and C_{R9} to the emitter of Q_6.

R_{40} is a "set-in-test" resistor, which adjusts the threshold voltage. Resistor R_{43} is an adjustment of the hysterisis; resistor R_{41} is a gain adjustment.

The current limit of the DLC is set for a maximum battery current of 9.3 A by resistor R_{37}.

Central Control Unit (CCU)

As it can be seen from the block diagram of Figure 26, the CCU consists of four error amplifiers: load bus error amplifier (LBEA), uplink error amplifier (ULEA), downlink error amplifier (DLEA), and shunt error amplifier (SEA).

The LBEA compares load bus voltage to reference voltage and provides a proportional error output.

To implement reliability requirements, a binomial 2 of 3 circuit redundancy is selected.

In channel A of the three-channel error amplifier (Figure 30), the differential amplifier Q_{201} compares bus voltage, divided down by R_{201}, R_{202}, and R_{203}, with reference voltage VR_{201}. The output is amplified by the complementary pair Q_{202} and Q_{203} and applied to the input of the majority voting gate (MVG) together with channel B and channel C outputs. This arrangement ensures that the output is unaffected by any signal part failure in the circuit.

The MVG consists of three parallel strings of two series-connected transistors. The six transistors are driven by the three error amplifier circuits so that each transistor in a string is controlled by a different channel. Should any circuit fail, so as to open those transistors which it controls, at least one of the three strings will still control. Should any circuit fail so as to cause a shorted transistor, the remaining transistor in that string will limit current. The current through the three strings of the MVG circuit is summed in three parallel resistors, and the output is taken as a voltage drop across the resistors. This output voltage controls all the other three error amplifiers sequentially.

When it exceeds the reference voltage E_{R1}, as shown in the block diagram of Figure 26, the ULEA becomes active. In channel A of the three-channel circuit, Q_{401} compares the input with the reference VR_{401}. Output is amplified and then applied to the input of the majority voting gate (MVG) together with channel B and channel C outputs.

The MVG of the ULEA is basically the same as that of the LBEA; therefore its further discussion is omitted here.

It can be seen from the transfer characteristic of Figure 27 that the positive slope of gain A_1 of the ULEA begins at $E_R + E_{R1}/A$ and ends at the saturation of the amplifier.

The load bus voltage E_{LB} must exceed $E_R + E_{R2}/A$ in order to control the DLEA. This voltage is greater than load bus voltage the ULEA saturates at; therefore a guard band exists where neither amplifier is operational in the feedback loop.

Break point voltage E'_{R2} is provided by a zener-resistor circuit, such as V_{R501} in series with R_{503}, in each channel of the three-channel single ended amplifier. MVG of the downlink, driven by Q_{501}, Q_{502}, and Q_{503}, contains three parallel strings of two series-connected transistors just as in the ULEA.

The negative slope of A_2 of the downlink transfer characteristic is traversed by the decreasing conduction of the transistors corresponding to the increasing voltage from the LBEA. The break in the slope occurs at $E_{LB} = E_R + E_{R2}/A$, when the transistors stop conducting.

The active region of the downlink is followed by another guard band between $E_R + E_{R3}/A$ and $E_R + E_{R2}/A$. E_{R3} is the reference voltage of SEA, which is greater than E_{R2}. When it is exceeded, the positive slope of A_3 is traversed.

The basic circuit arrangement of the SEA is the same as that of the ULEA, having a binomial 2 of 3 circuit redundancy. The output provides a proportional control signal to the central shunt regulator (CSR).

Central Shunt Regulator

The central shunt regulator (CSR), consisting of one power, one driver, and one subdriver stage, draws shunt current to limit the load bus, when the solar array output power is greater than the load and charge power.

The power stage contains three parallel strings of two series-connected transistors. Each string is capable of handling more than 3.5 A of shunt current. The circuit redundancy assures that a component failure in any of the strings does not affect the operation of CSR.

The input current from CSEA is amplified by both the driver and subdriver stages to provide a proportional current signal to the base circuits of the power stage. Both drivers are quad-redundant.

MESAC SYSTEM TEST DATA

MESAC system test data included in this section consist of the following tables and graphs:

1) Load Bus Regulation (Table 1)

   The maximum load bus change ΔE_{LB} (max) under various modes of operation is less than 40 mv.

2) Ripple Amplitude Versus Operation Mode (Table 2)

   The maximum ripple (180 mv) occurs in discharge with two ULC's providing the full load power.

3) Converters Current Limits (Table 3)

   The current limits of the ULC's and DLC's are 13.5 ±0.9 A and 9.1 ±0.2 A, respectively.

4) Efficiency Versus Input Voltage for Uplink Converters (Table 4)

   The efficiency is maximum at nominal load.

5) Efficience Versus Output Current for Downlink Converters (Table 5)

   The maximum also occurs at nominal load.

6) Transient Response (Table 6)

   The data was tabulated from the pictures shown in MESAC Data Sheets. It can be seen that the transient recovery waveforms are underdamped and thereby the system is marginally stable for the designated conditions. The recovery time is defined for measurements in the test as the time required for output voltage recovery to within 0.3 v of the nominal voltage following a step change in load current.

7) Battery 2 Voltage V_{B2} and Battery 2 Current I_{B2} Versus Simulated Orbit Time

   Although test was conducted on all three batteries, only one plot of a typical battery was obtained.

All measurements were taken at room temperature per the MESAC test procedure and the information was first entered into the data sheets and then transfered to the tables above. Data sheets are shown in Appendix II, Data Sheets.

MESAC TEST EQUIPMENT LIST

Equipment used on MESAC:

VLB: Cubic Model V-top-S/N 250PS
SEA Output: Triplet 630NA-S/N 218
Uplink E. A. Output: Triplet 601-S/N 51241
D/L E. A.: Triplet 630NA-S/N 664
VB1: H. P. 3439-S/N 589
VB2: Cimron 7500A-S/N 4112
VB3: Cimron 7200A-S/N 3991
3rd E. S. No. 1: Triplet 630NA-S/N 51308
3rd E. S. No. 2: Triplet 630NA-S/N 047360
3rd E. S. No. 3: Triplet 601-S/N 051242
I_{Bat} No. 1: H. P. 428B-S/N 00911
I_{Bat} No. 2: H. P. 428B-S/N 2003
I_{Bat} No. 3: H. P. 428B-S/N 01-182169

Table 1. Load Bus Regulation (E_{LB} versus I_L)

Operating Mode	Load	E_{LB}(V)	I_L(A)	Comment
Discharge, normal	Heavy	26. 90	4. 2	
Discharge, failure	Heavy	26. 90	4. 2	
Discharge, normal	Light	26. 90	0. 3	
SA = load	Heavy	26. 93	4. 2	No battery currents
Charge normal	Heavy	26. 92	4. 2	
Shunt normal	Heavy	26. 93	4. 2	
Shunt normal	Light	26. 94	0. 27	

Table 2. Ripple Amplitude versus Operation Mode

Operating Mode	Load	I_L (A)	Ripple (mv) (p - p)
Discharge, normal	Normal	4.2	150
Discharge, normal	Light	0.3	100
Discharge, failure	Normal	4.2	200
Charge, normal	Normal	4.2	80
Shunt, normal	Normal	4.2	90
Shunt, normal	Light	0.27	No measured ripple

Table 3. Tabulation of Current Limits of the Converters

Operating Mode	Converter	I_{B1} (A)	I_{B2} (A)	I_{B3} (A)
Discharge	Uplink 1	13.4		
Discharge	Uplink 2		12.6	
Discharge	Uplink 3			14.1
Charge	Downlink 1	9.3		
Charge	Downlink 2		9.1	
Charge	Downlink 3			9.3

Table 4. Efficiency versus Input Voltage for Uplink Converters

Converter	V_{IN} (V)	I_{IN} (A)	I_L (A)	Efficiency (percent)	Load
Uplink 1	6.29	11.4	2	75.0	Maximum
Uplink 1	6.1	11.9	2	74.2	Maximum
Uplink 1	6.0	12.2	2	73.5	Maximum
Uplink 1	5.88	12.7	2	72.0	Maximum
Uplink 1	5.80	12.9	2	72.0	Maximum
Uplink 2	6.34	10.8	2	78.7	Maximum
Uplink 2	6.30	10.9	2	78.3	Maximum
Uplink 2	6.20	11.1	2	78.1	Maximum
Uplink 3	6.39	10.8	2	78.0	Maximum
Uplink 3	6.30	11.0	2	77.7	Maximum
Uplink 3	6.20	11.4	2	76.1	Maximum
Uplink 3	6.10	11.6	2	76.1	Maximum
Uplink 2	6.30	6.8	1.32	83.2	Nominal
Uplink 2	6.20	7.0	1.32	82.2	Nominal
Uplink 2	6.10	7.1	1.32	82.2	Nominal
Uplink 2	6.30	0.96	0.13	58.0	Minimum

Note: V_{IN} = V_{B1}, V_{B2}, V_{B3}

I_{IN} = I_{B1}, I_{B2}, I_{B3}

I_L = I_L are the corresponding symbols in the data sheet.

Table 5. Efficiency versus Output Current for Downlink Converters

Converter	V_{IN}(V)	I_{IN} (A)	I_0 (A)	Efficiency (percent)	Load
Downlink 1	26.93	3.8	9.2	66.6	Maximum
Downlink 2	26.94	3.5	8.7	71.2	Maximum
Downlink 3	26.94	3.75	9.4	69.0	Maximum
Downlink 1	26.93	1.43	4.0	74.9	Nominal
Downlink 2	26.93	1.60	4.0	68.2	Nominal
Downlink 3	26.93	1.60	4.0	66.4	Nominal
Downlink 1	26.93	0.76	2.0	69.2	Minimum
Downlink 2	26.93	0.88	2.0	60.5	Minimum
Downlink 3	26.92	1.10	2.0	47.7	Minimum

Note: $V_{IN} = V_{LB}$,

$I_{IN} = I_{SA}$,

$I_0 = I_{B1}$, I_{B2}, I_{B3} are the corresponding symbols in the data sheet.

Table 6. Table of Transient Response

Operating Mode	Maximum Peak (volts)	Receiving Time (msec)	Load Change (ohms)	Comment
No SA, normal	1.5	30	14 → 6.5	
No SA, normal	1.2	120	6.5 → 14	Marginal stability
No SA, 1 failure	1.2	20	14 → 6.5	
No SA, 1 failure	2.8	40	6.5 → 14	
W/SA, no shunting	0.3	-	14 → 6.5	
W/SA, no shunting	0.4	1	6.5 → 14	
W/SA and shunting	0.5	20	14 → 6.5	
W/SA and shunting	0.75	15	6.5 → 14	

SECTION IV

DISCUSSION OF POSSIBLE IMPROVEMENTS

It seems to be appropriate to point out, before going into the details of possible improvements, that it is TRW's contention that the MESAC concept, as well as its implementation, has useful applications and deserves further attention.

Considering that the major task was to focus on the realization of the basic concept rather than on details, the optimization and worst-case design were beyond the scope of the job.

If the deficiencies are listed in sequential order of importance, the system stability is first.

1. Although for most operating modes the MESAC system is stable or marginally stable, some low-level oscillation may occur. In those few cases where oscillation was observed, the amplitude was low enough not to affect the regulation or ripple.

The stability of the system should be improved if the converters were changed from a constant ON time to a constant frequency operation. The main difficulty with the constant ON time approach is that for good stability, the crossover frequency of the loop gain must be lower than the switching frequency of the converters, which during regulation at low power (corresponding to increasing OFF time) actually approaches zero. With a constant frequency approach, however, the slopes of the gain curve and the crossover would be better controlled. Therefore, both the stability and the transient response of the system should improve.

The change-over would require a complete redesign of the astable multivibrator and its control circuit; no change would be necessary in the converter power stages.

2. The efficiencies of the converters are not optimized. Substantial power is dissipated in the protective zener VR1 of the DLC, which accounts for lowering the efficiency about eight percent.

Use of the zener was required because of switching spikes exceeding the collector-emitter breakdown voltage of Q_1.

This problem could be solved by replacing the power transistors with high voltage ones.

3. The maximum boost ratio E_{LB}/E_B of the ULC is not high enough to ensure regulation voltage E_{LB} = 28 v at E_B = 5 v. The basic limitation is due to the reverse base-emitter breakdown voltage BV_{BER} of Q_1. N_4/N_1 of T_1 must be chosen so that the negative going base voltage does not exceed BV_{BER}. Thus:

$$\frac{N_4}{N_1} > \frac{E_{B(max)}}{EV_{BER}} = 1$$

But N_4/N_1 also has an upper limit determined by the saturation requirement during OFF time:

$$\frac{N_4}{N_1} < \frac{E_B^2}{(E_{LB} - E_B) V_{BE(on)} Q_1} = 0.9$$

with E_B = 5 v and E_{LB} = 28 v.

The two inequalities cannot be satisfied simultaneously; consequently E_{LB} = 28 v is unobtainable at E_B = 5 v.

A possible solution is to use Darlington connected transistors in place of Q_1 which would permit decreasing the ratio of N_4/N_1.

4. The charge control operation is not satisfactory. The third electrode sensor should be complemented by an overvoltage sensor or a voltage limit to protect the battery against over-voltage.

5. Optimization of the magnetics for minimum weight and size is required to obtain the best power-to-weight ratio.

6. Worst-case analysis of the MESAC system should be completed for environmental extremes, including normal and failure mode analysis, stability, and transient analysis.

7. The worst-case analysis should be compared with the test results obtained for the same operating conditions to verify accuracy of the design techniques.

MESAC TEST PROCEDURE

I. Performance Characteristics

A. Discharge

1. Normal Operation, Full Load

a. Initial conditions, batteries fully charged

$R_L = 6.5\Omega$

All converters on

b. Measurements, V_{LB} - DVM

Photo of ripple

V_{LBEA}, V_{ULEA}, V_{DLEA}, V_{CSEA} - VOM

V_{B1}, V_{B2}, V_{B3} - DVM

I_{B1}, I_{B7}, I_{B3}, I_L - meter

$V_{B_{Q1}}$, $V_{C_{Q1}}$ - photo (one unit only)

2. Normal Operation, Light Load

a. Initial conditions

Continue from above except $R_L = 100\Omega$

b. Measurements

Same as above

3. Failure Mode, Full Load

a. Initial conditions

Continue from above but with $R_L = 6.5$ and one converter disabled

b. Measurements

Same as above except no $V_{B_{Q1}}$ and $V_{C_{Q1}}$ photos

4. Current Limit

a. Initial conditions

Continue from above with R_L = variable

b. Measurements

Disable two converters and adjust load so that remaining converter current limits; record

V_{LB}, V_B - DVM

I_L, I_B - meter

Repeat for other two converters

B. Solar Array, Load

1. Normal Operation

a. Initial conditions

All converters on

$R_L = 6.5\Omega$

$I_{SA} = I_L + I_{DL's}; I_{B's} = I_{UL's}$

b. Measurements

V_{LB} - DVM, photo of ripple

V_{LBEA}, V_{ULEA}, V_{DLEA}, V_{CSEA} - VOM

V_{B1}, V_{B2}, V_{B3} - DVM

$I_{DL's}$, I_{CCU}, I_{B1}, I_{B2}, I_L, I_{SA} - meter

Verify all converters off - scope

C. Charge

1. Normal Operation

a. Initial conditions

All converters on

$R_L = 6.5\Omega$

Max I_{SA}

b. Measurements

V_{LB} - DVM, photo

V_{LBEA}, V_{ULEA}, V_{DLEA}, V_{CSEA} - VOM

V_{B1}, V_{B2}, V_{B3} - DVM

I_{B1}, I_{B2}, I_{B3}, I_L, I_{SA}, I_{SH}, $I_{DL's}$ - meter

$V_{B_{Q1}}$, $V_{C_{Q1}}$ - photo (one unit only)

2. Current Limit

a. Initial conditions

Reduce load and/or remove conterters to demonstrate current limit on each DL

b. Measurements

V_{LB}, V_B - DVM

I_B, I_L, I_{SA} - meter

D. Shunt

1. Normal Operation

a. Initial conditions

DL's off as required to give shunting

R_L = 6.5, I_{SA} = maximum

b. Measurements

V_{LB} - DVM, scope photo

I_L, $I_{B's}$, I_{SA}, I_{SH} - meter

$V_{B's}$ - DVM

V_{LBEA}, V_{ULEA}, V_{DLEA}, V_{CSEA}

2. Full Load Operation

a. Initial conditions

All DL's off, R_L = 100

I_{SA} = maximum

b. Measurements

V_{LB} - DVM, photo

I_L, I_{SH}, I_{SA}

V_{LBEA}, V_{ULEA}, V_{DLEA}, V_{CSEA}

E. Charge Control

1. Normal Operation

a. Initial conditions

All batteries discharged as required

b. Measurements

At trip point for each battery:

V_{3E}, V_B, I_B

II. Efficiency

A. Uplinks

1. Full Load

a. Initial conditions

One at a time

R_L = 13Ω

Disconnect downlinks

b. Measurements at three different $V_{B's}$

I_L, V_{LB}, I_B, V_B, I_{CCU}

2. Nominal Load

Same as above but $R_L = 20$

Do for one unit only

3. Light Load

Same as above but $R_L = 300$

Do for same unit as above

B. Downlinks

1. Full Load

a. Initial conditions

One at a time, uplinks off

R_L and I_{SA} as required

$I_B \cong 8.9$ a

b. Measurements

I_L, V_{LB}, I_B, V_B, I_{CCU}

2. Nominal Load

Same as above, but $I_B = 4$ a

3. Light Load

Same as above, but $I_B = 2$ a

III. Time Response

A. With No Solar Array

1. Normal Operation

a. Initial conditions

All converters on

$R_L = 6.5\Omega$

b. Measurements

V_{LB}, I_L, $V_{B's}$, $I_{B's}$ before and after changing

R_L from 6.5 to 14Ω; V_{LB} on scope during - photo

Repeat for $R_L = 14 \rightarrow 6.5$

2. Failure Mode; repeat with two converters only

B. With Solar Array

1. Normal Operation

a. Initial conditions

All converters on, all batteries charging

$R_L = 6.5\Omega$

b. Measurements

V_{LB}, $I_{.}$, $V_{B's}$, $I_{B's}$, I_{SA}, I_{SH} before and after changing R_L from 6.5 to 14Ω; V_{LB} on scope during - photo

Repeat for $R_L = 14 \rightarrow 6.5\Omega$

2. Charge/Shunt

Repeat with DL's off as required to have shunting before and after both

IV. Simulated 100 Minute Orbits

A. Initial Conditions

All batteries fully charged

All converters on

$R_L = 6.5\Omega$

B. Measurements, every 10 minutes

V_{LB}, $I_{.}$, $I_{B's}$, $V_{B's}$, I_{SA}, I_{SH}

C. Timing

t = 0	$I_{SA} = 0$
t = 40 min	I_{SA} = max
t = 100 min	$I_{SA} = 0$
t = 140 min	I_{SA} = max
t = 200 min	I_{SA} = max

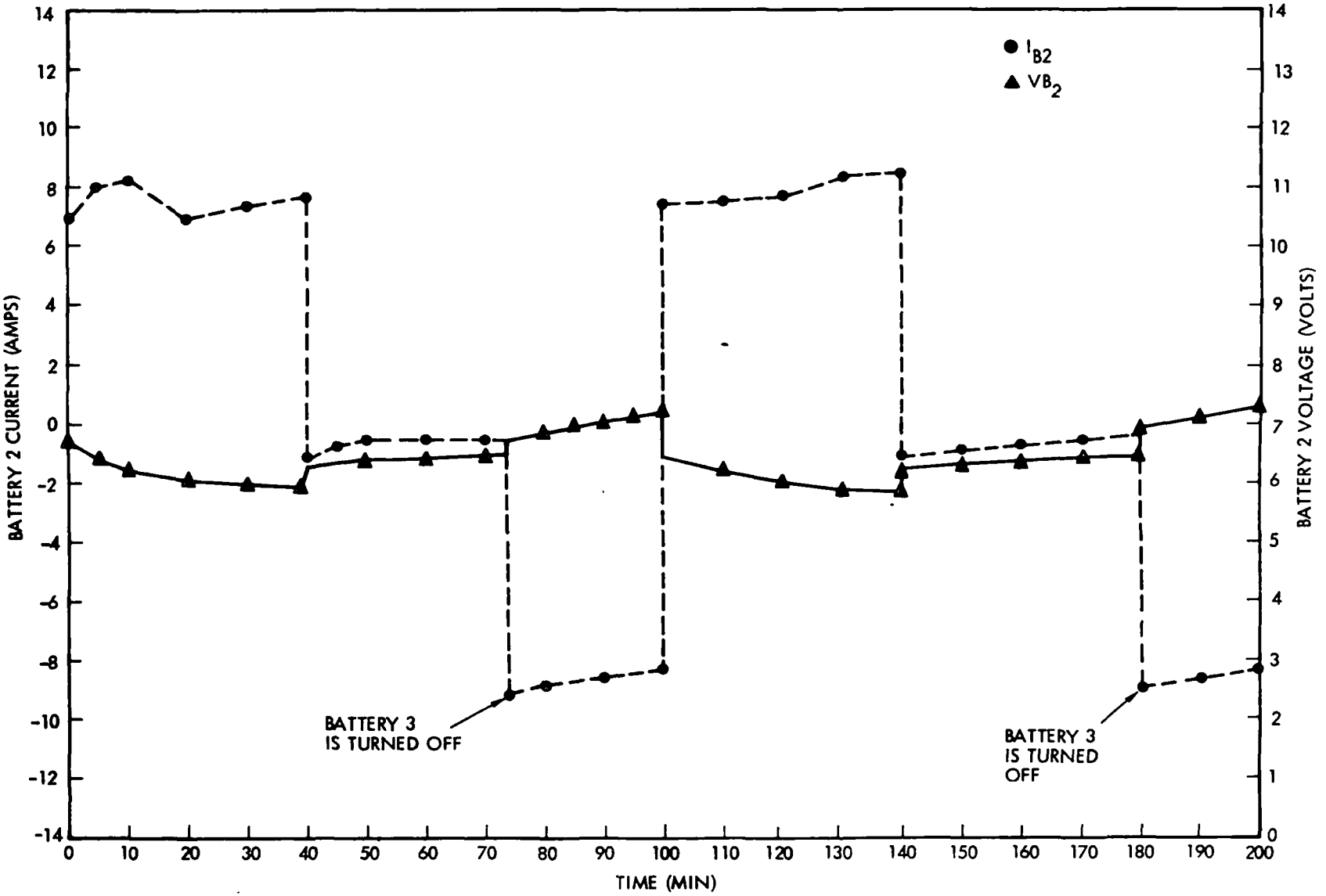


Figure T-1. Final MESAC Breadboard Test Battery 2 Voltage v_{B2}, and Battery Current I_{B2} versus Simulated Orbit Time

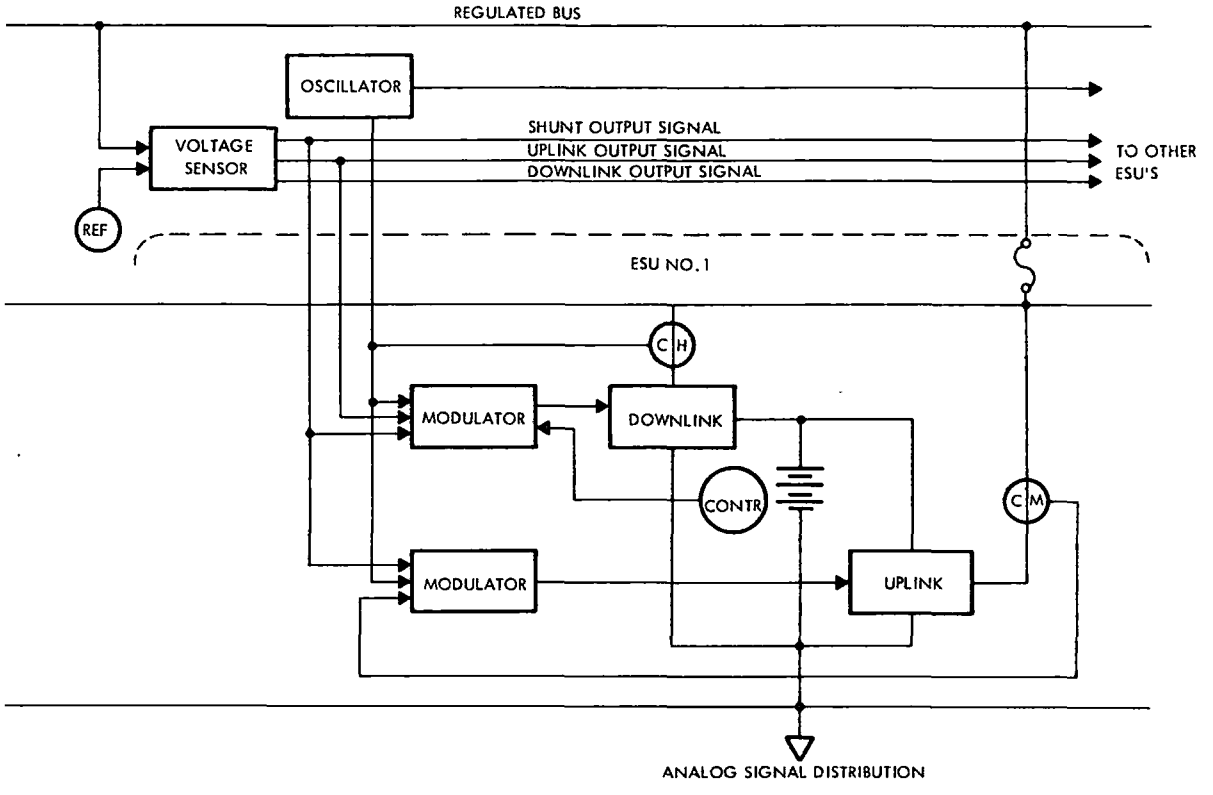


Figure 1. Analog Signal Distribution

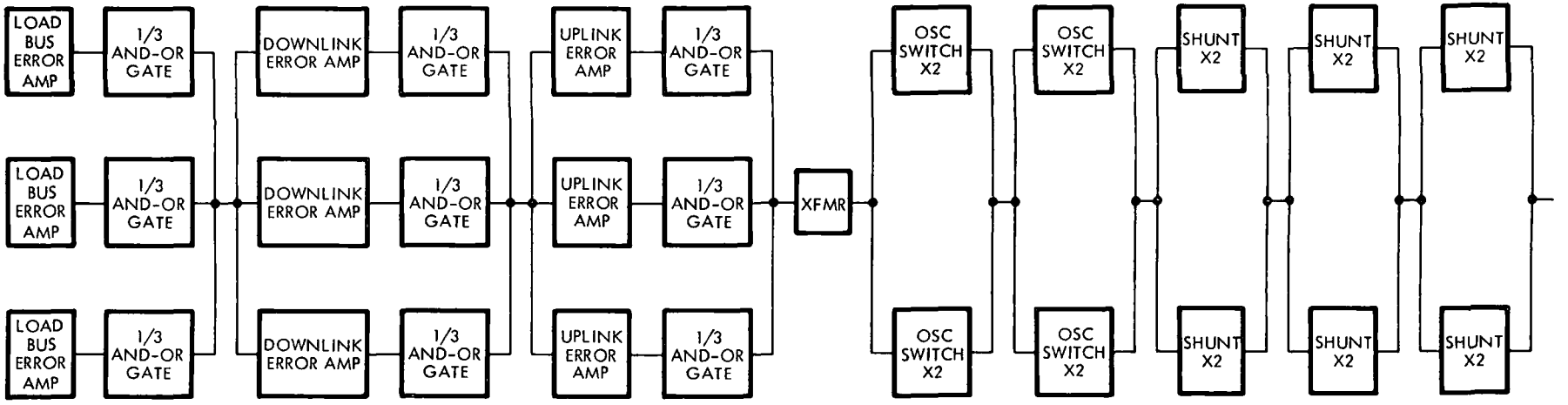


Figure 2. Central Control Unit Reliability Block Diagram

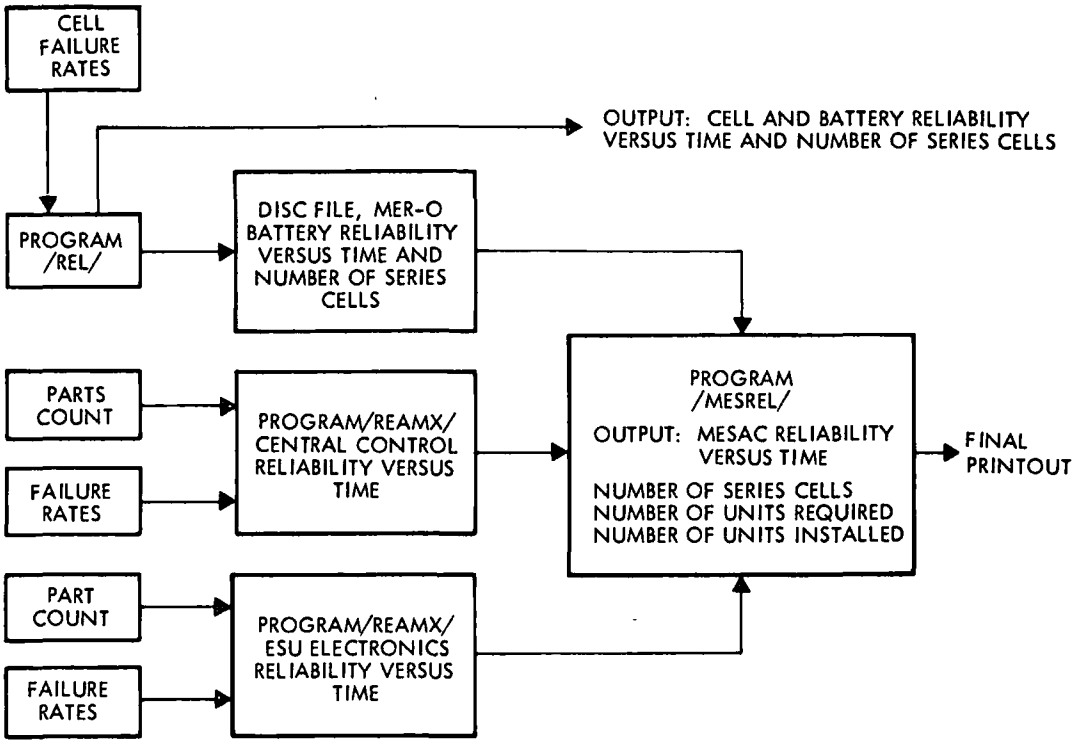


Figure 3. MESAC Reliability Calculation Flow Diagram

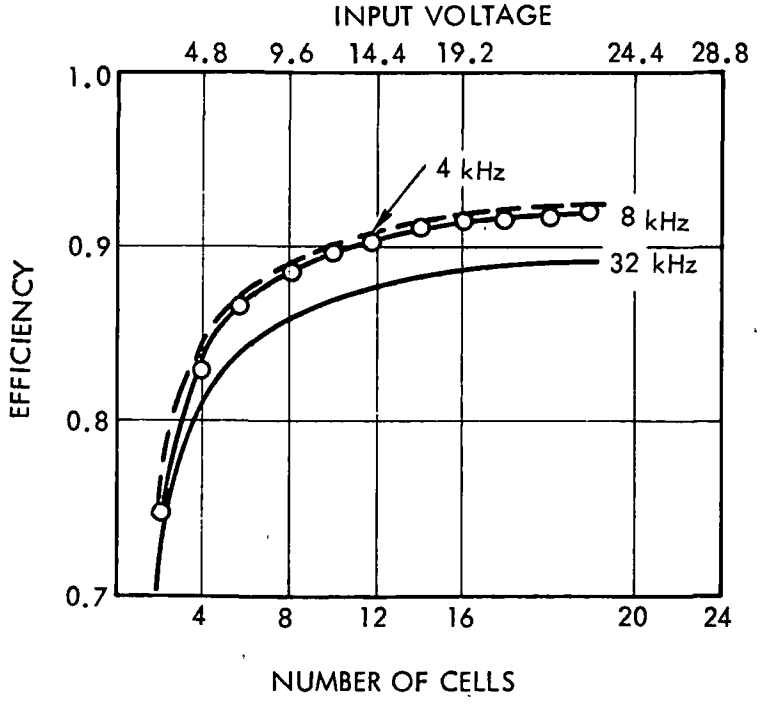


Figure 4. Efficiency of Uplink Versus Number of Series Cells Frequency as Third Variable Synchronous Orbit, 6 A-Hr Cells, 70 % DOD

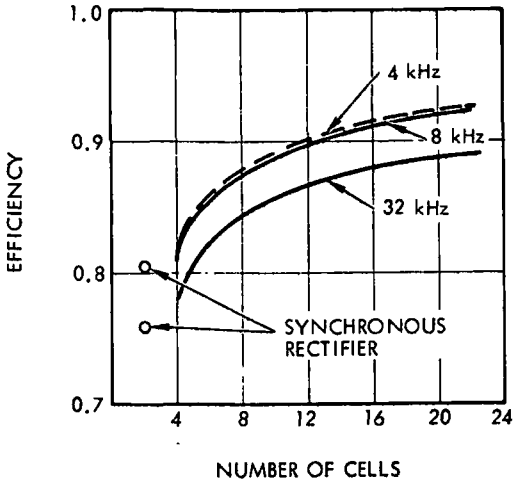


Figure 5. Downlink Efficiency Versus Number of Series Cells, 6 A-Hr, 70% DOD Synchronous Orbit

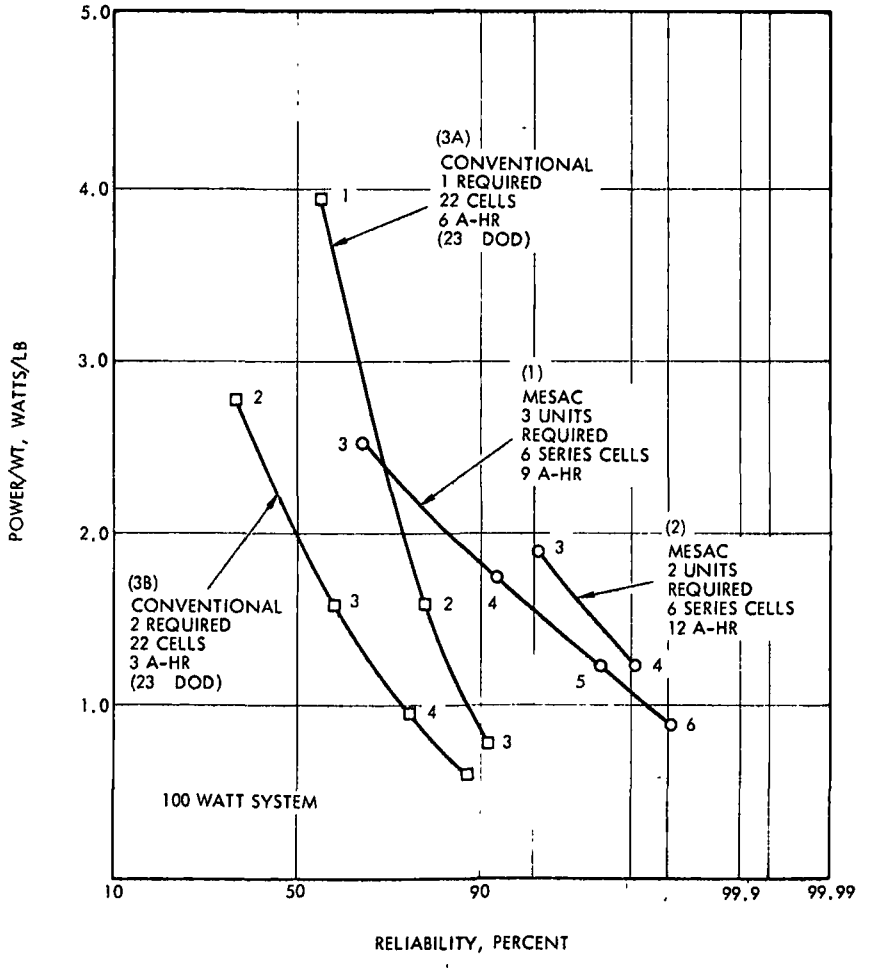


Figure 6. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; Synchronous Equatorial Orbit. Normal Battery Cell Divergence Failure Rates Applied

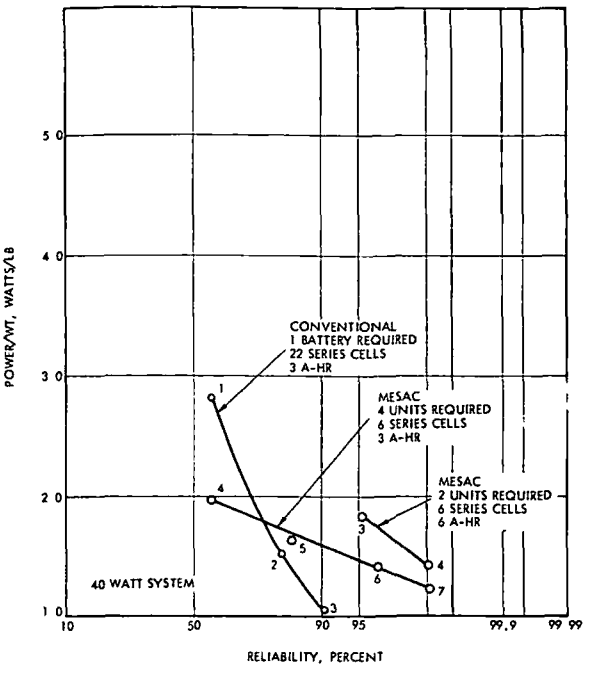


Figure 7. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; Synchronous Equatorial Orbit. Normal Battery Cell Divergence Failure Rates Applied.

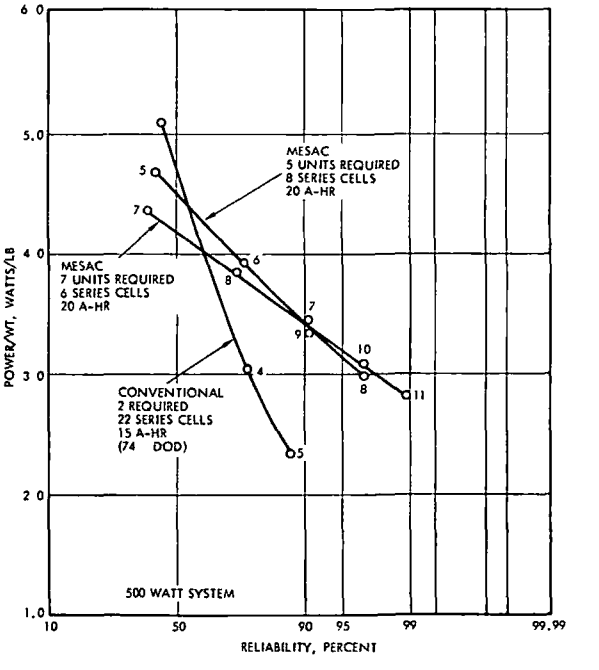


Figure 8. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; Synchronous Equatorial Orbit. Normal Battery Cell Divergence Failure Rates Applied.

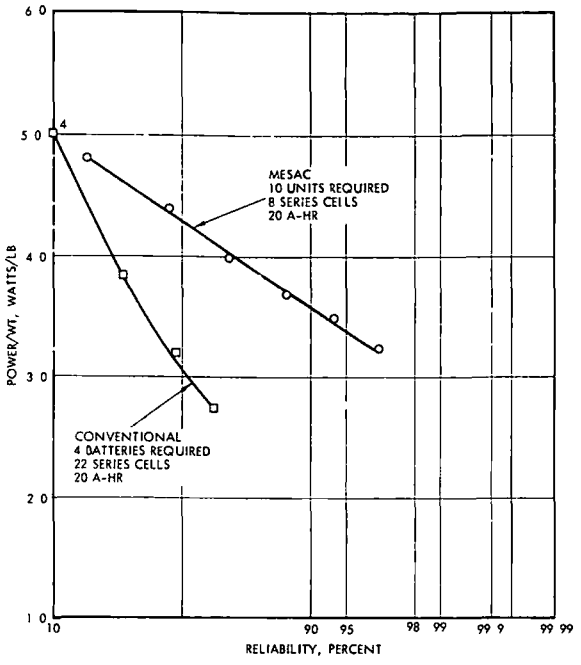


Figure 9. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; Synchronous Equatorial Orbit. Normal Battery Cell Divergence Failure Rates Applied.

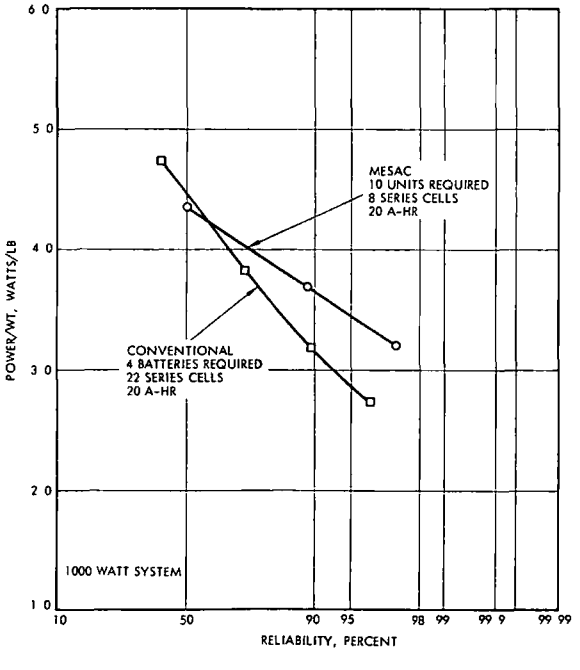


Figure 10. Comparison of Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; Synchronous Equatorial Orbit. Cell Divergence Rates Assumed to be 0.

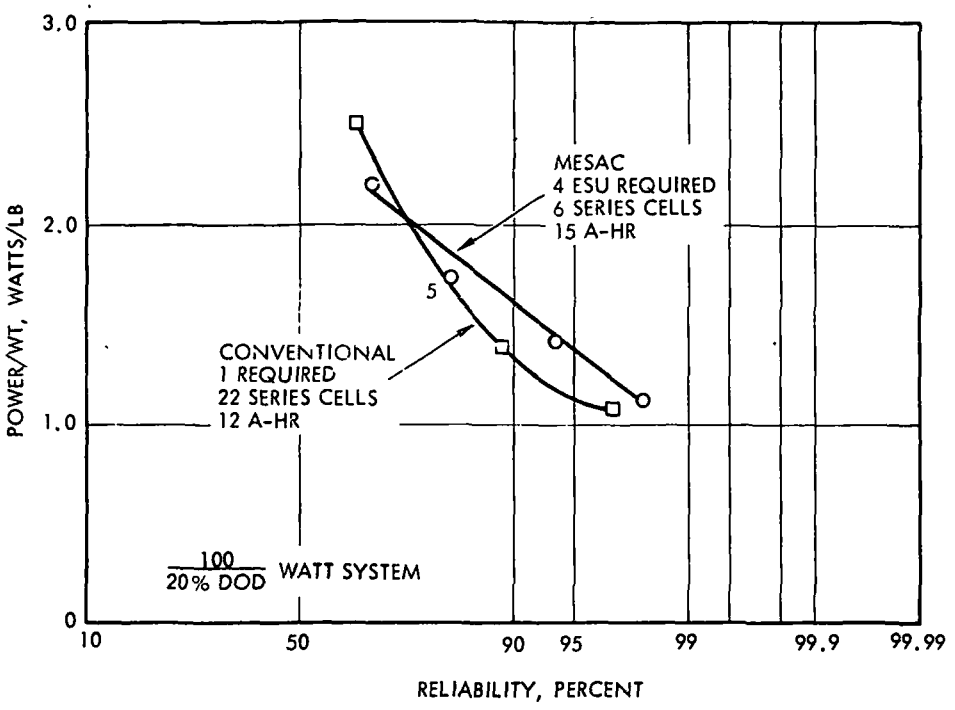


Figure 11. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; 100 Minute Circular Orbit. Normal Battery Cell Divergence Failure Rates Applied.

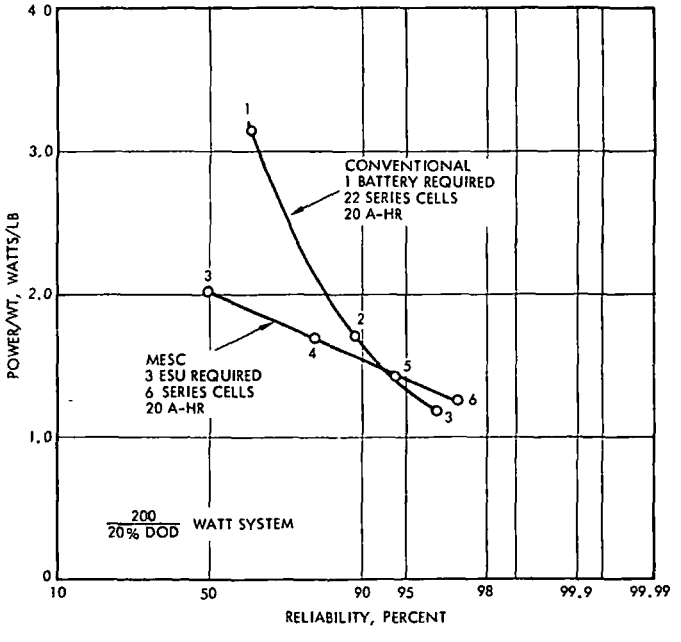


Figure 12. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; 100 Minute Circular Orbit. Normal Battery Cell Divergence Failure Rates Applied.

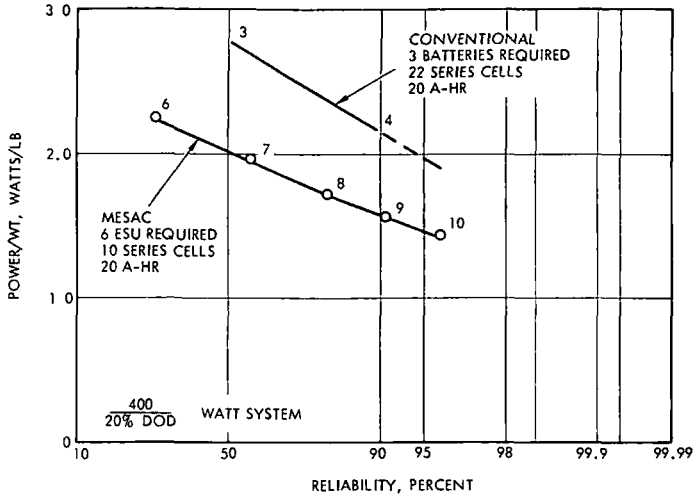


Figure 13. Comparison of the Power-to-Weight Ratios of MESAC and Conventional 22-Cell Battery Systems as a Function of the Reliability at 6 Years; 100 Minute Circular Orbit. Normal Battery Cell Divergence Failure Rates Applied.

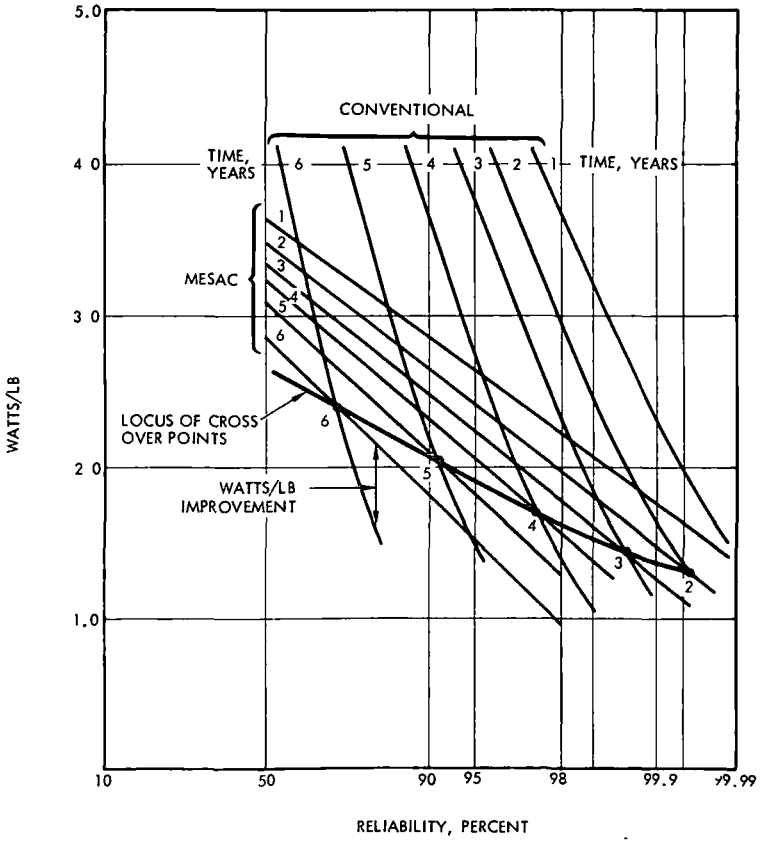


Figure 14. Tradeoff Between MESAC (3 Required) and Conventional (1 Required) Systems for a 100 Watt Synchronous Equatorial Application at 70% DOD. Normal Cell Failure Rates.

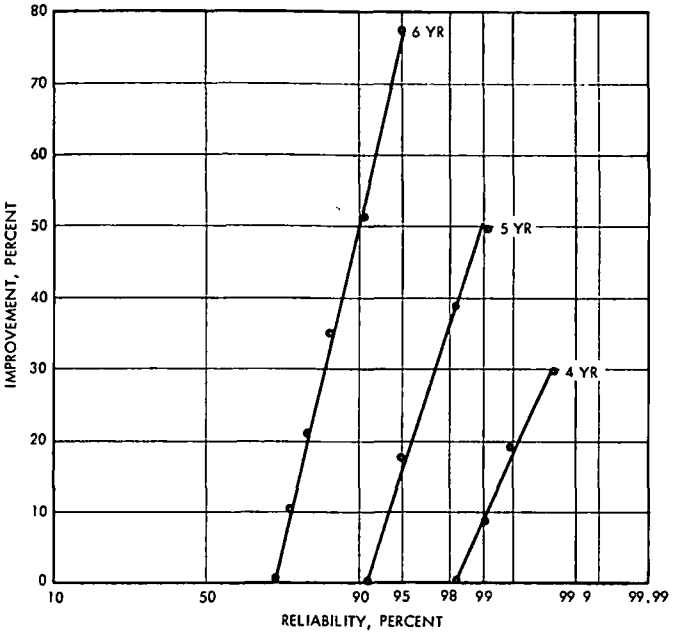


Figure 15. Percent of Power-to-Weight Ratio Improvement Achievable by Substituting MESAC for Conventional Batteries in the 100 Watt, 24 Hour Application.

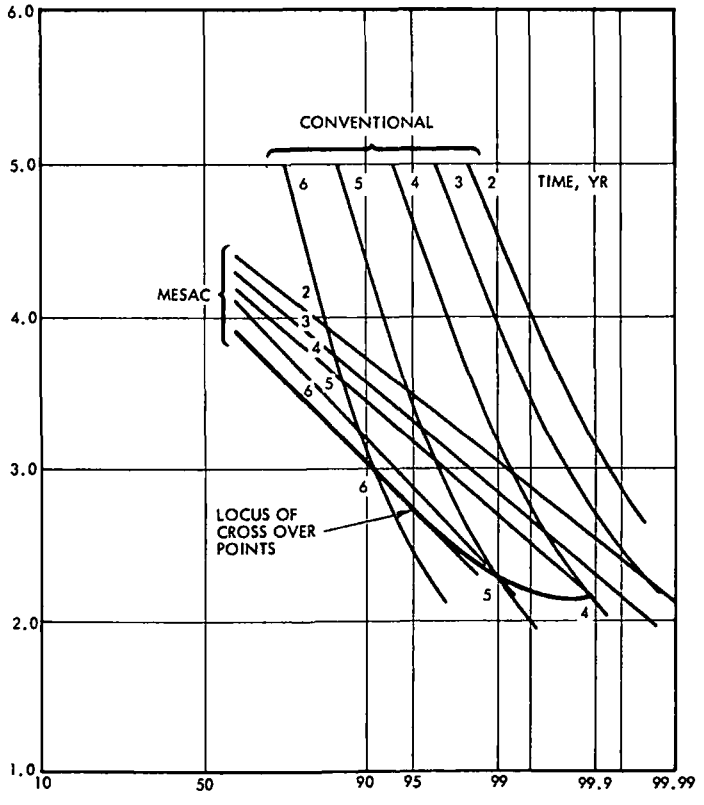


Figure 16. Tradeoff Between MESAC (3 Required) and Conventional (1 Required) Systems for a 100 Watt Synchronous Equatorial Application at 70% DOD. One-Half Normal Cell Failure Rates.

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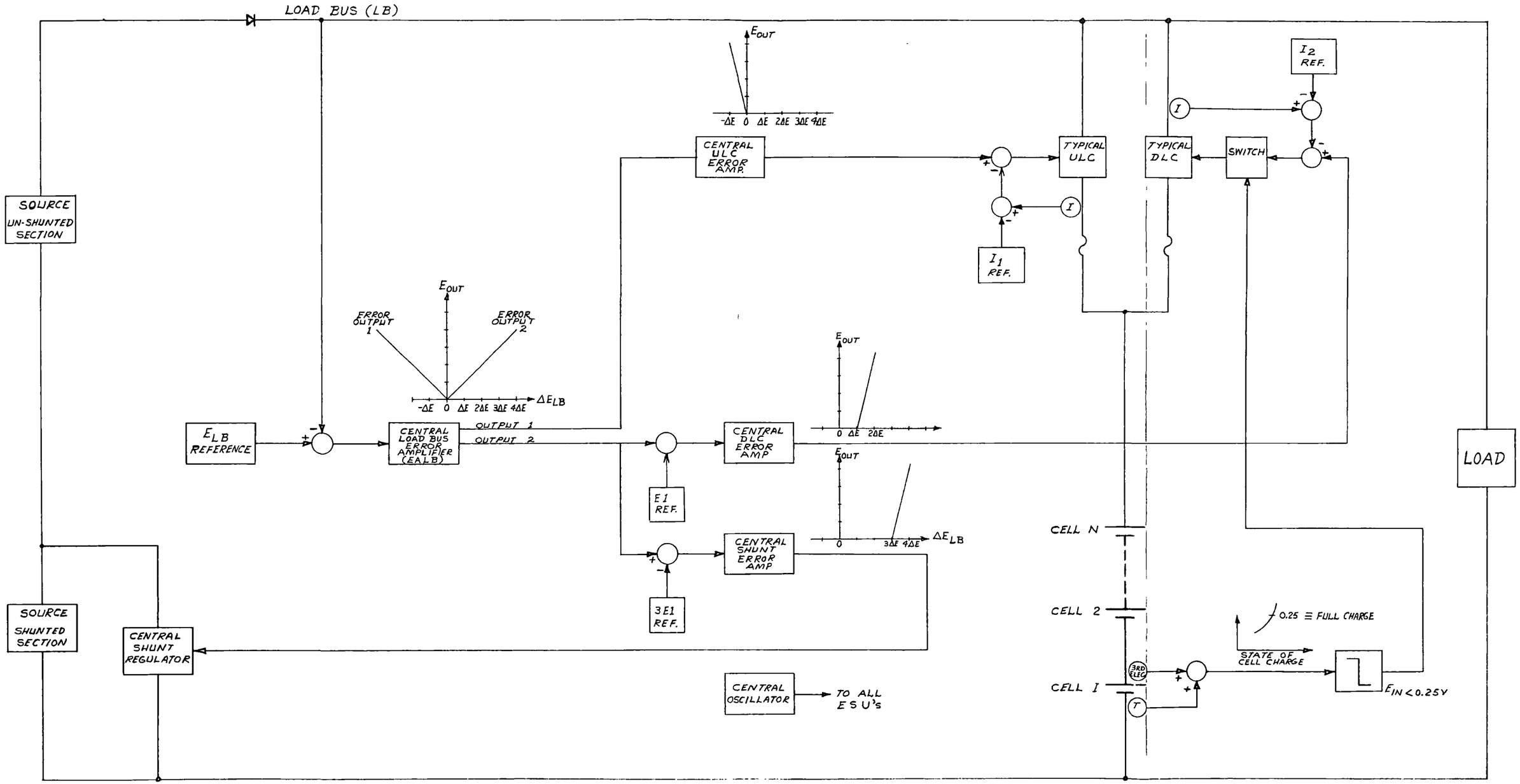


Figure 17. MESAC Block Diagram

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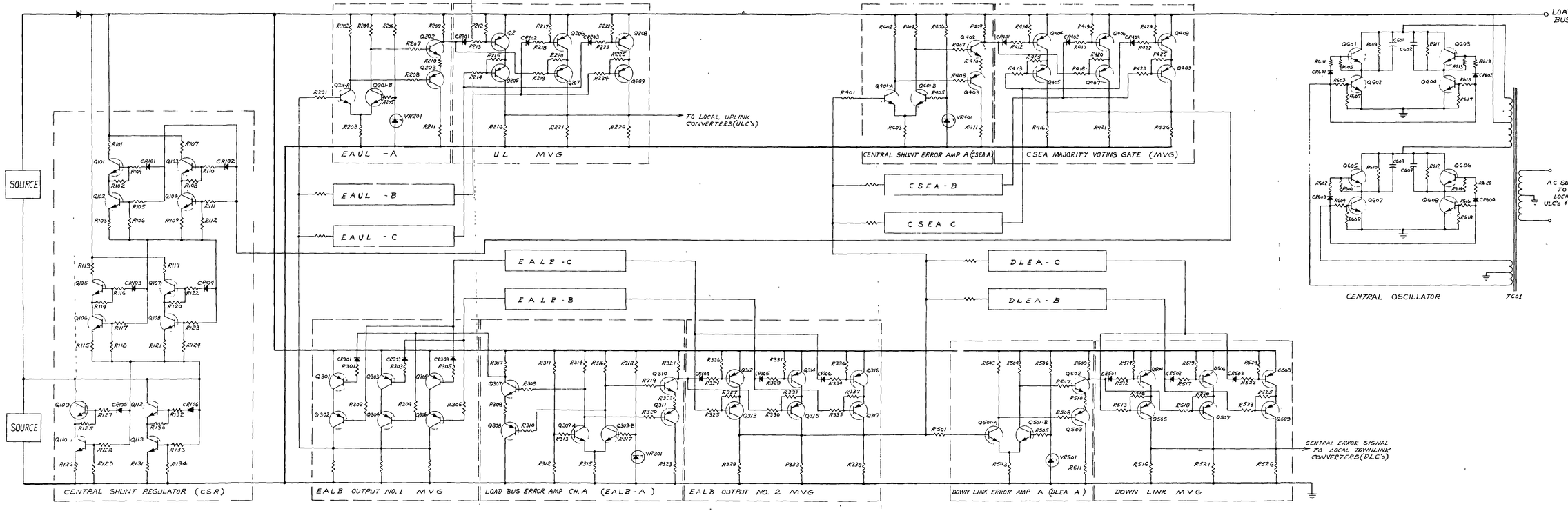


Figure 18. MESAC Central Control Unit (CCU)

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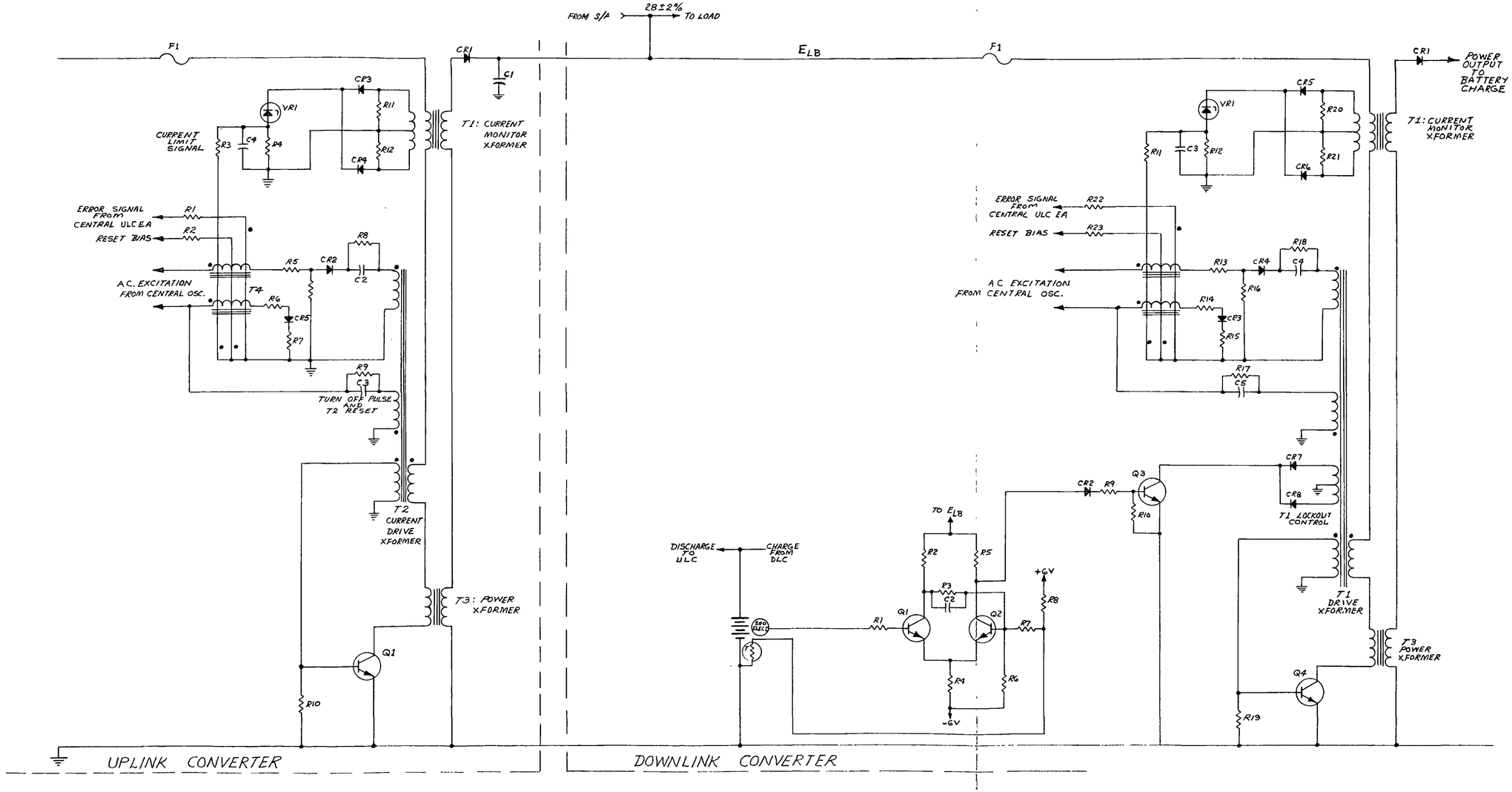


Figure 19. Energy Storage Unit (ESU)

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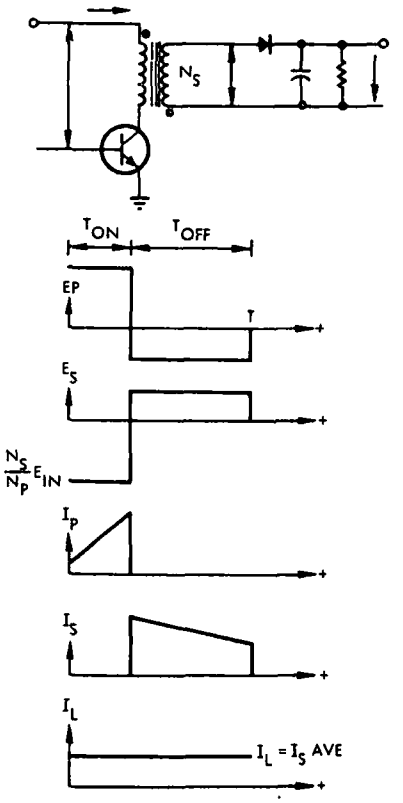


Figure 20. Simplified Energy Storage Circuit Schematic and Waveshapes

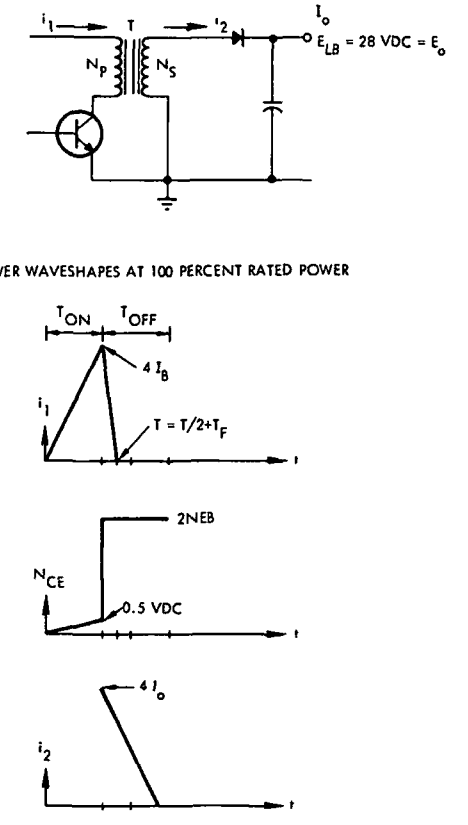


Figure 21. Simplified Uplink Converter Schematic and Waveshapes

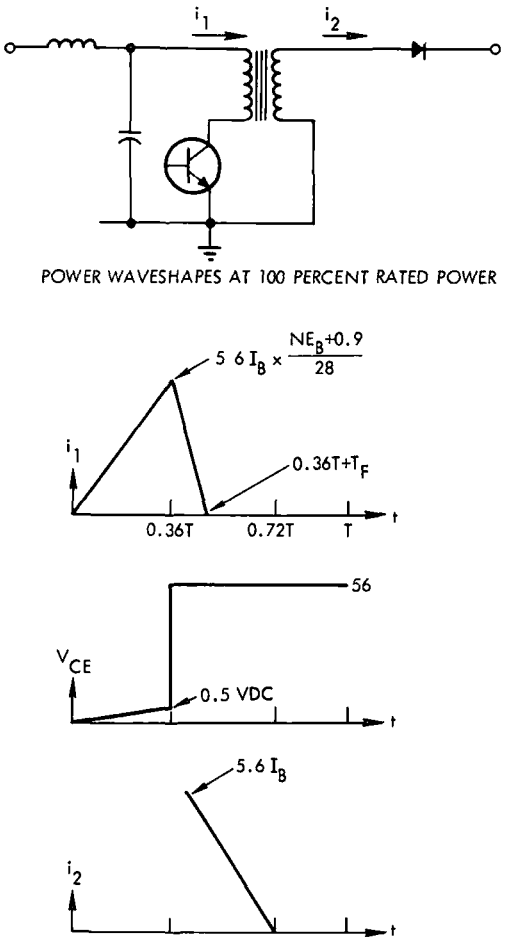


Figure 22. Simplified Downlink Converter Schematic and Waveshapes

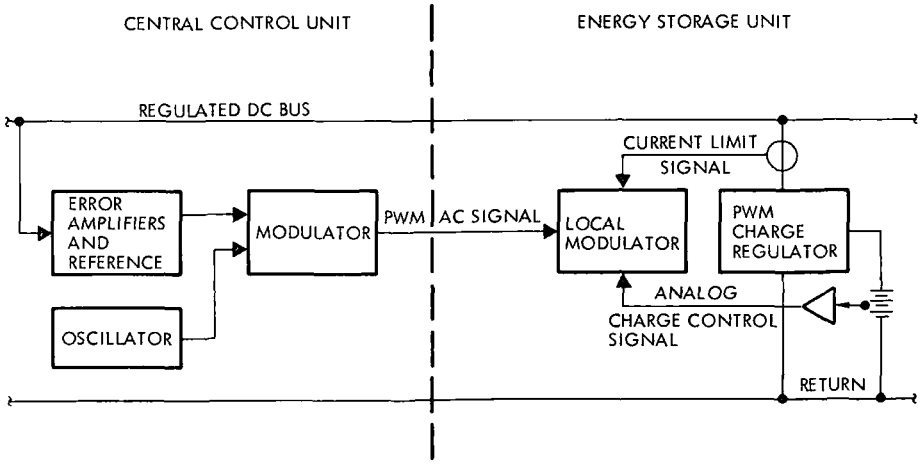


Figure 23. Typical Regulation Control Scheme, Showing Maximum Centralization of Control

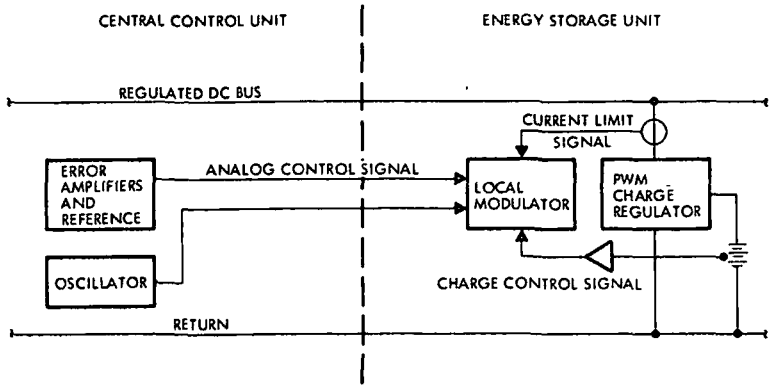


Figure 24. Typical Regulation Control Scheme, Using Analog Signal Distribution, Central Oscillator, and Local Modulator

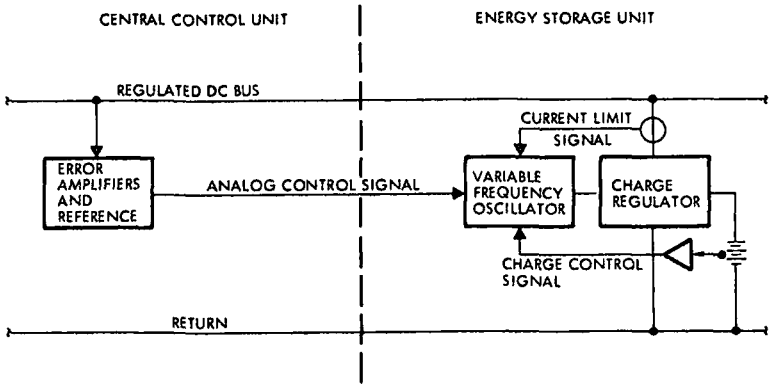


Figure 25. Typical Regulation Control Scheme, Using Analog Signal Distribution and a Variable-Frequency Oscillator

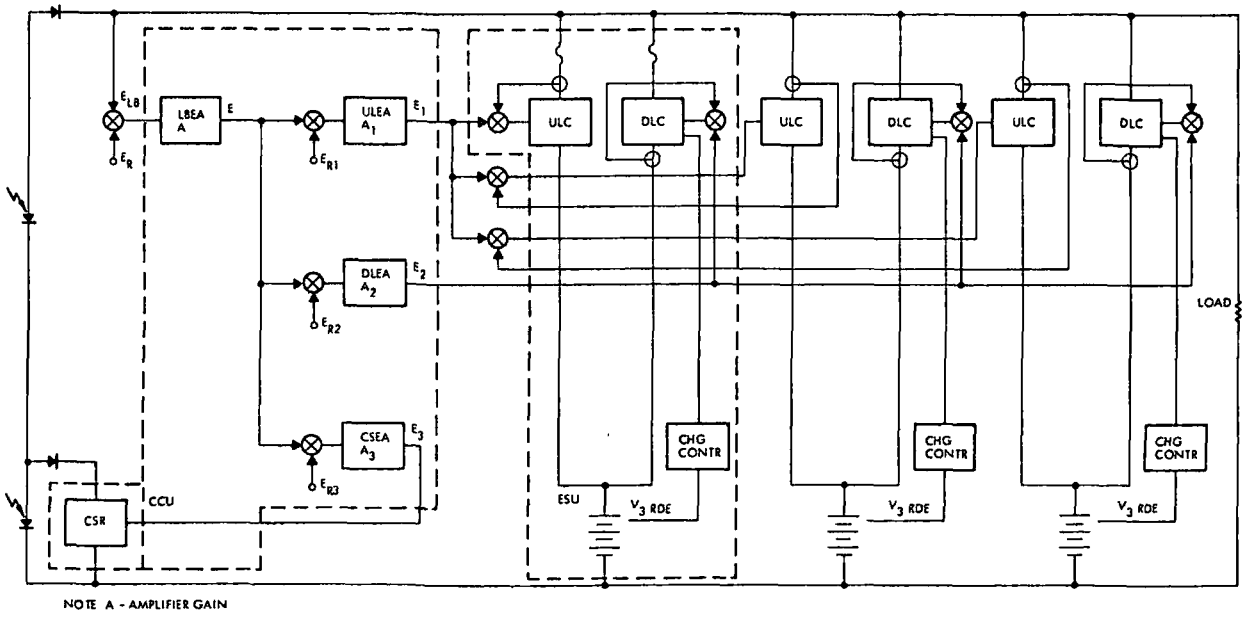


Figure 26. MESAC Block Diagram

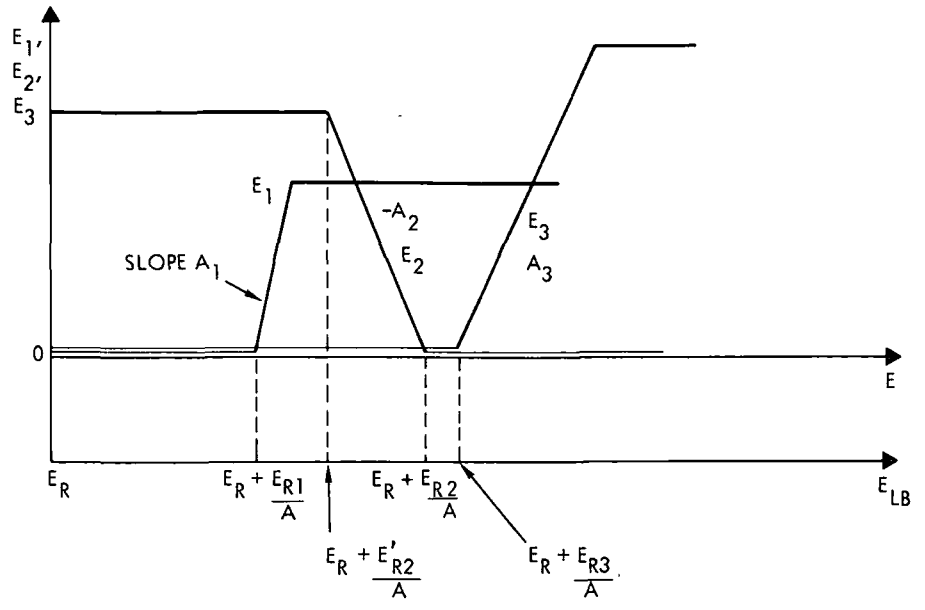


Figure 27. Error Signals E_1, E_2, and E_3 in Relation to the Output of LBEA and the Load Bus Voltage E_{LB}

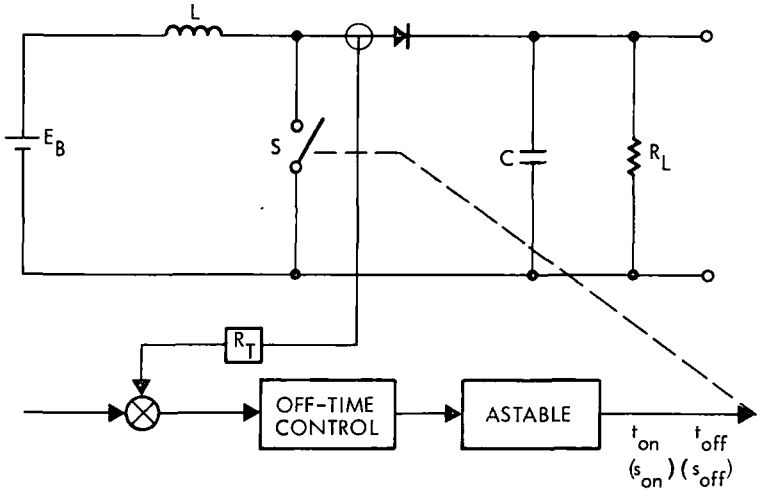


Figure 28. Simplified Block Diagram of ULC

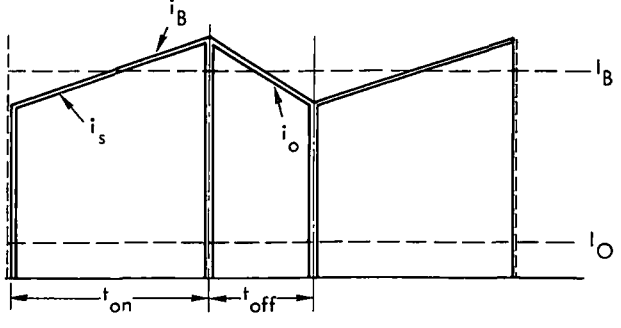
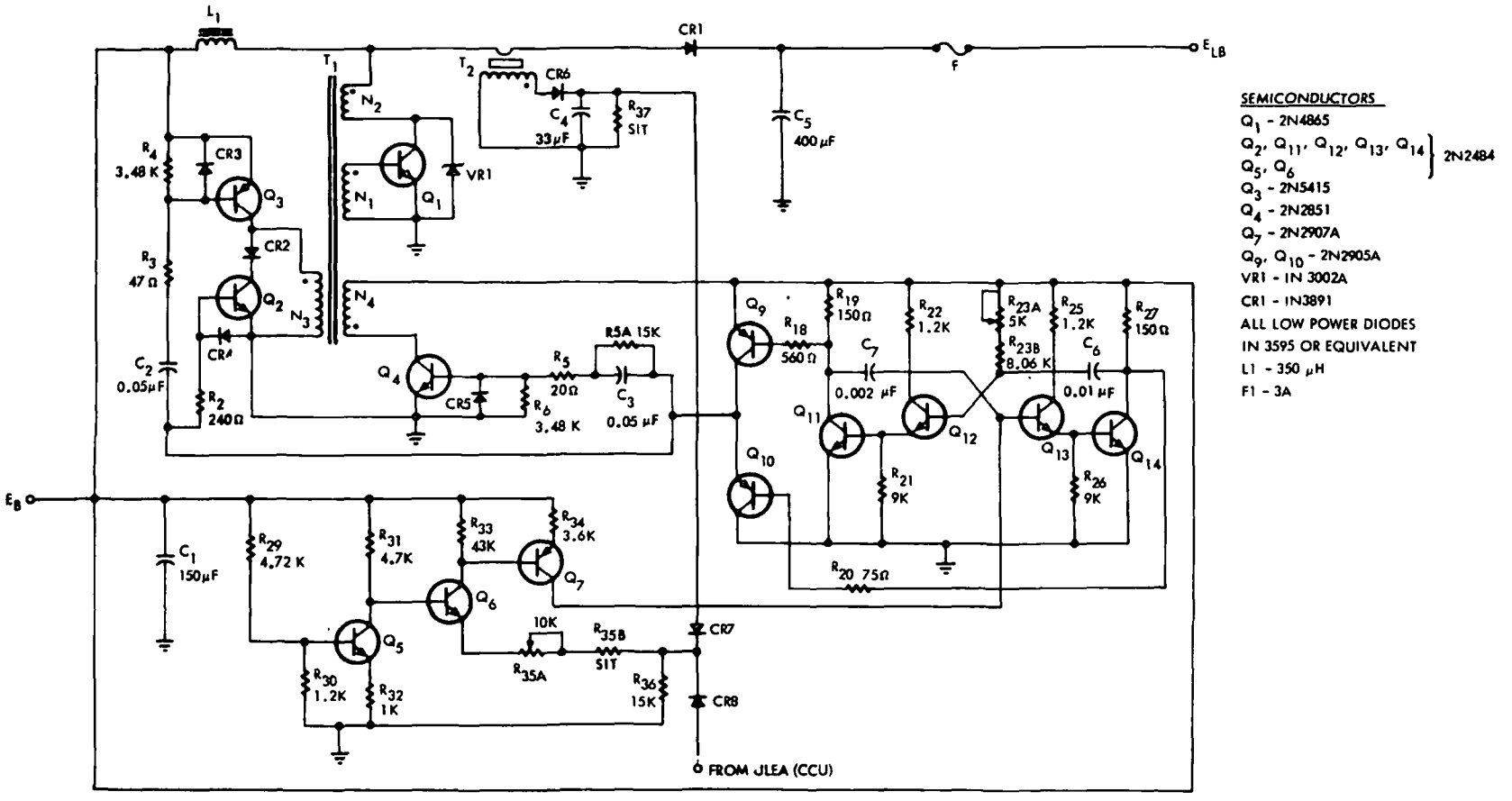


Figure 29. Current Waveform of ULC



SEMICONDUCTORS

Q_1 - 2N4865

Q_2, Q_{11}, Q_{12}, Q_{13}, Q_{14}, Q_5, Q_6 } 2N2484

Q_3 - 2N5415

Q_4 - 2N2851

Q_7 - 2N2907A

Q_9, Q_{10} - 2N2905A

VR1 - IN 3002A

CR1 - IN3891

ALL LOW POWER DIODES IN 3595 OR EQUIVALENT

L1 - 350 μH

F1 - 3A

Figure 30. Uplink Converter

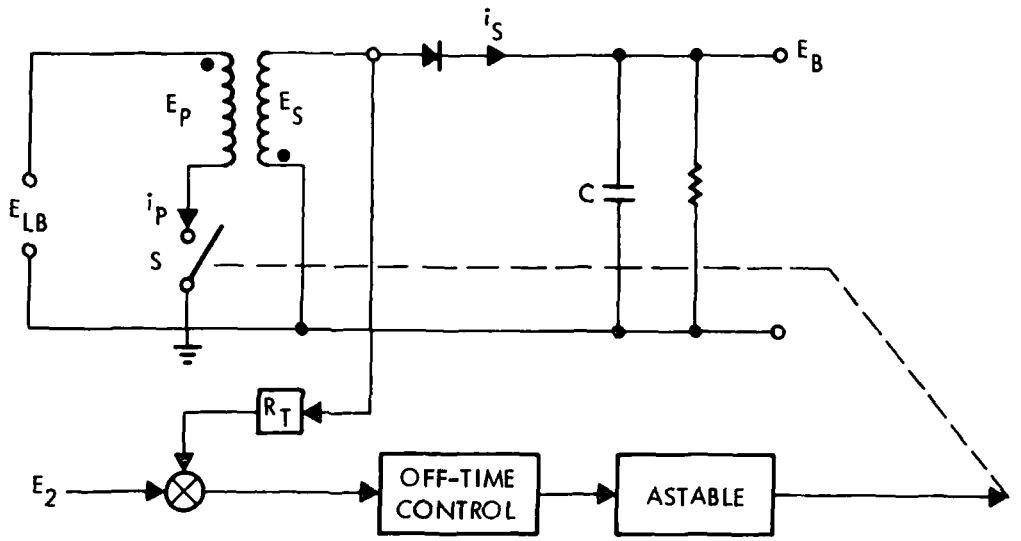


Figure 31. Simplified Block Diagram of DLC

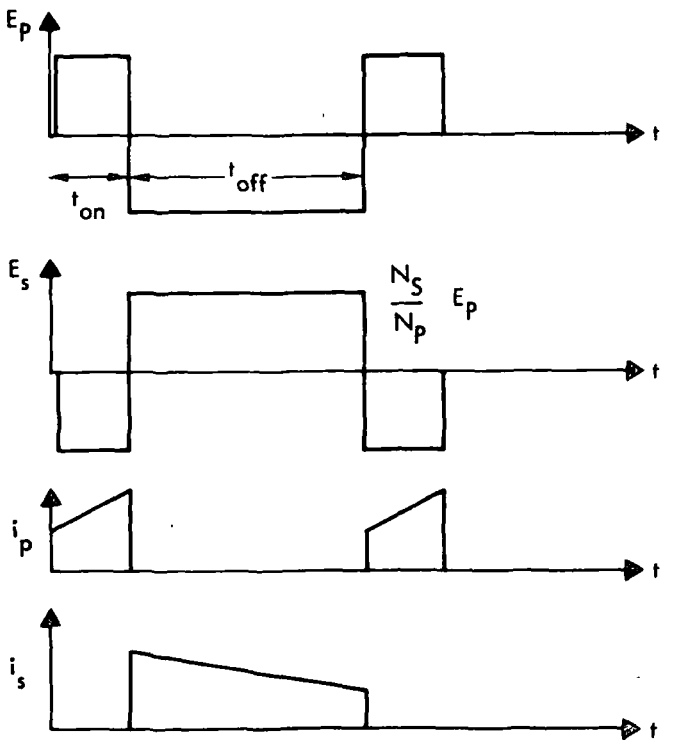


Figure 32. Current Waveforms of DLC

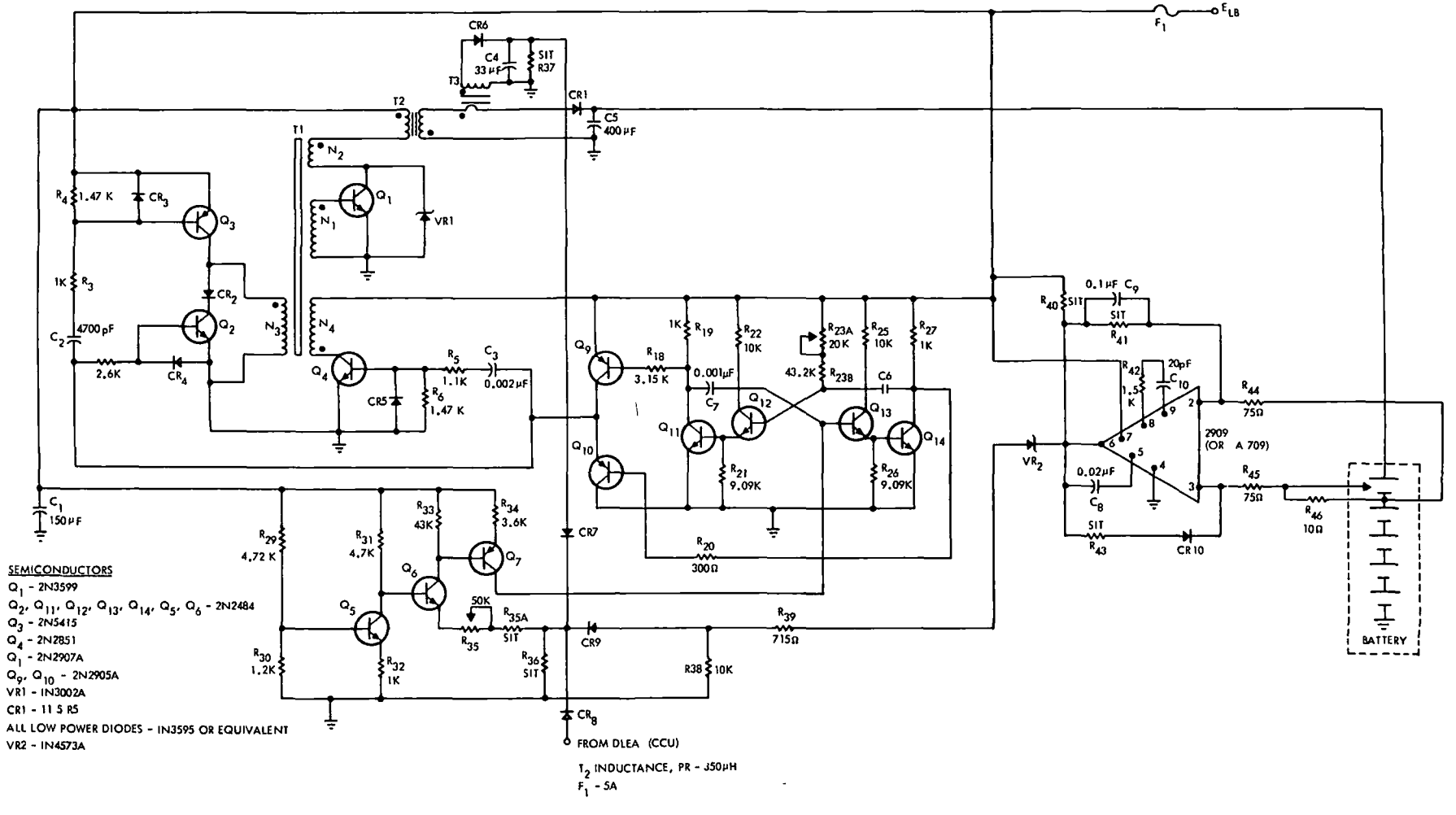


Figure 33. Downlink Converter

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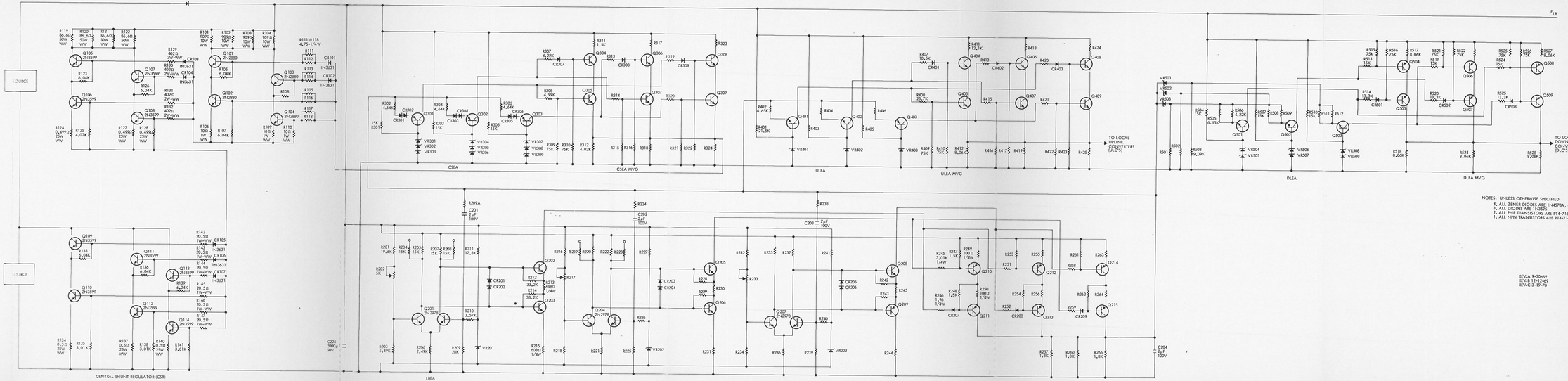
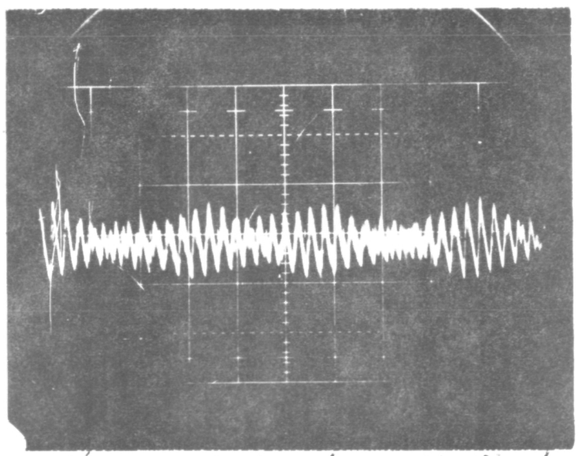


Figure 34. MESAC Central Control Unit and Shunt Regulator

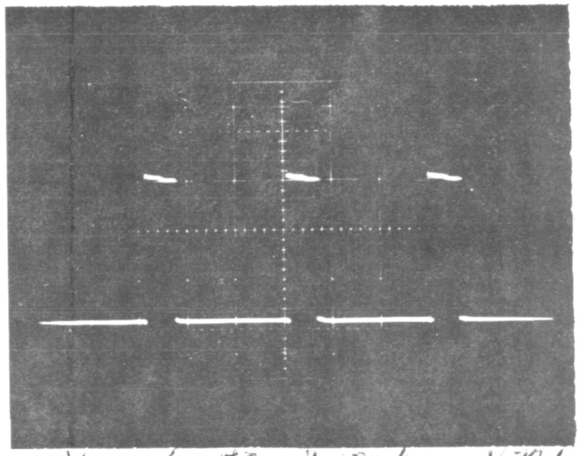
PAGE MISSING FROM AVAILABLE VERSION

MESAC DATA SHEET

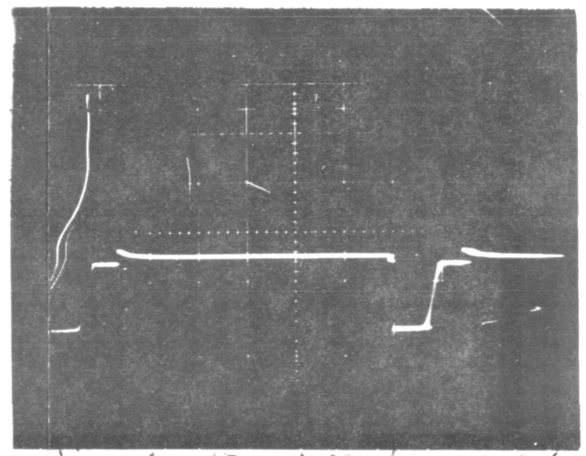
LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																	
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{VLEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}	
1	Discharge - Normal Opr	I-A-1	26.9	4.2	0	0	6.44	6.42	6.24	5.4	5.35	10.3	10.9	2.0	9.3	0	-	-	-	
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V_{LB} H = 0.5 ms/cm V = 1V/cm



V_{B1} Low #2 H = 50 ms/cm V = 10 v/cm



V_{B1} Low #2 H = 20 ms/cm V = 5 v/cm

APPROVALS

PROJECT, WORK PACKAGE, WORK UNIT MANAGER — DATE

FUNCTIONAL MANAGER — DATE

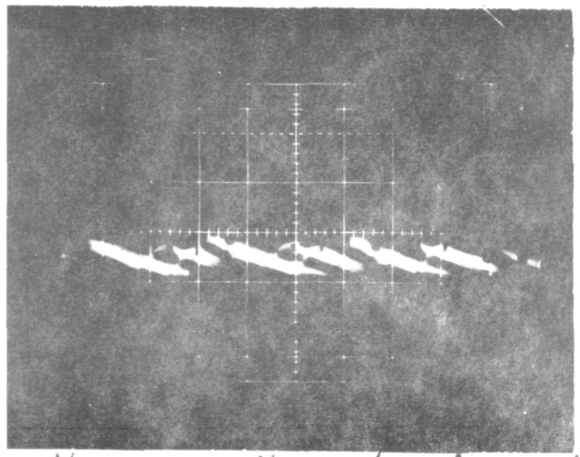
REVIEWING PROJECT AUTHORITY — DATE

SYSTEMS 2450 REV. 12-65

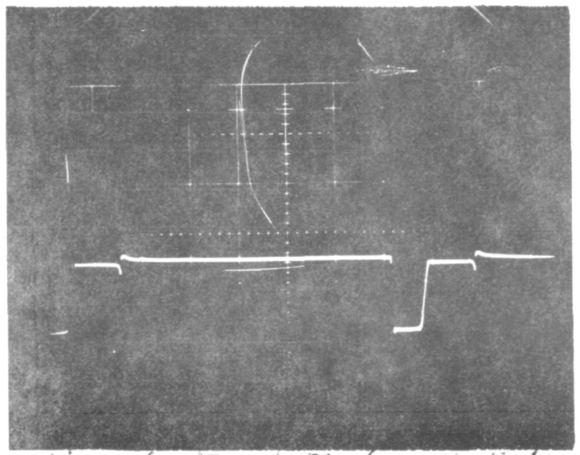
PAGE MISSING FROM AVAILABLE VERSION

MESAC DATA SHEET

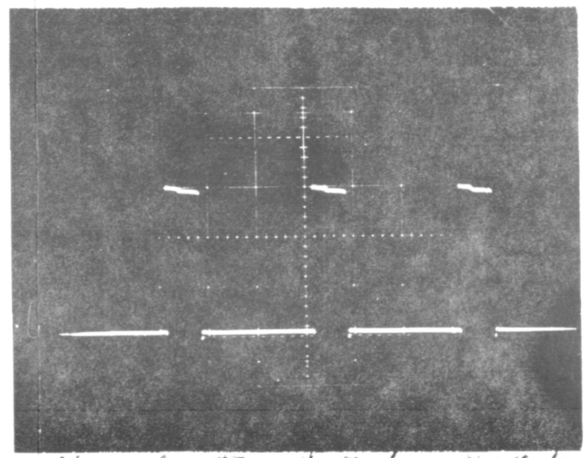
LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{ULEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}
1	Discharge - Light load	I-A-2	26.9	.3			6.43	6.44	6.36	1.2	.85	.4	10.8	2.1	8.3	0			
2																			
3																			
4																			
5																			
6																			
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V_{LB} H = 50 ms/cm V = 20 v/cm



V_{B1} Conv #2 H = 20 ms/cm V = 5 v/cm



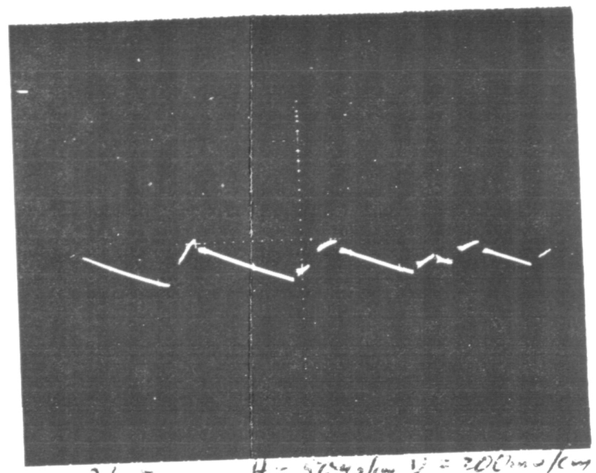
V_{B1} Conv #2 H = 50 ms/cm V = 10 v/cm

APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER — DATE	FUNCTIONAL MANAGER — DATE	REVIEWING PROJECT AUTHORITY — DATE

SYSTEMS 245-1 REV. 12-65

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LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{ULEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}
1	Discharge - Failure Mode	I-A-3	26.9	4.2	–	–	6.1	6.03	6.4	10.9	12.5	–	10.3	1.6	8.3	0			
2																			
3																			
4																			
5																			
6																			
7																			
8																			
9																			
10																			
11																			
12																			
13																			
14	Discharge - Current Limit	I-A-4																	
15	#1		26.2				5.95			13.4									
16	#2		26.7					6.00			12.6								
17	#3		26.8						5.92			14.1							
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V-3 H = 5ms/cm V = 200mv/cm

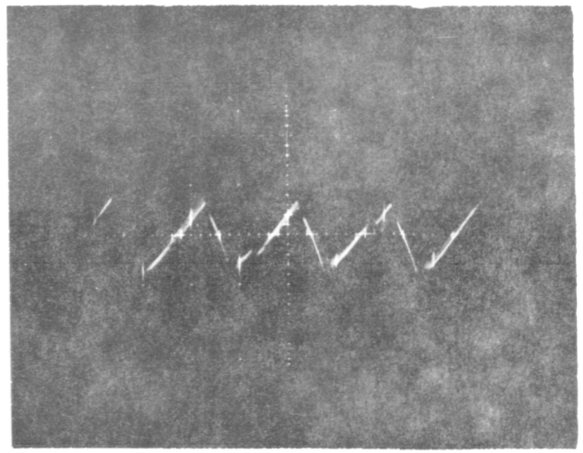
APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER	DATE	FUNCTIONAL MANAGER	DATE	REVIEWING PROJECT AUTHORITY	DATE

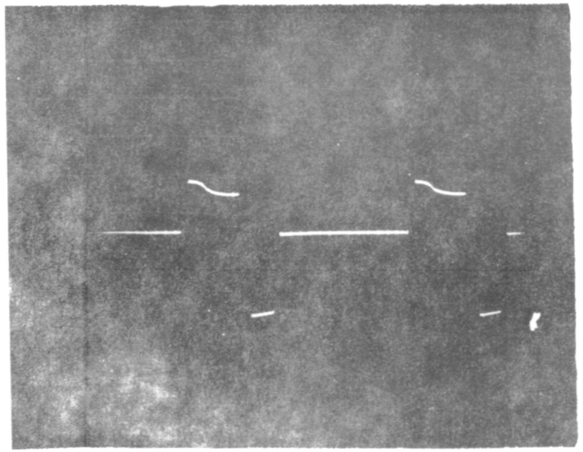
SYSTEMS 2450 REV. 12-65

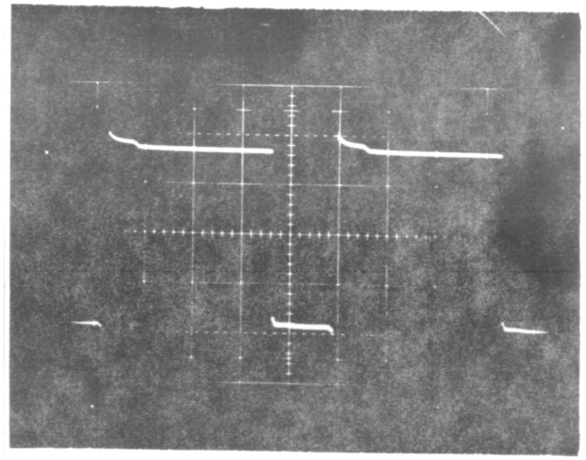
PAGE MISSING FROM AVAILABLE VERSION

MESAC DATA SHEET

LINE No.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																				
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{ULEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}	I_{ECU}	I_{DL1}	I_{DL2}	I_{DL3}	
1	Solar Array = Load	I-B-1	26.93	4.2	4.4	0	6.41	6.44	6.35	.113	.084	.095	19.0	4.2	8.2	0	-	-	-	.064	.092	.072	.062	Verified all converters off. Ripple not measurable
2																							
3																							
4																							
5																							
6																							
7																							
8																							
9																							
10	Charge – Normal	I-C-1	26.92	4.2	8.6	0	6.45	6.57	7.05	0.3	1.45	9.25	19.8	4.1	3.5	0	.01	.007	.05	.065	.045	0.22	2.6	
11																							
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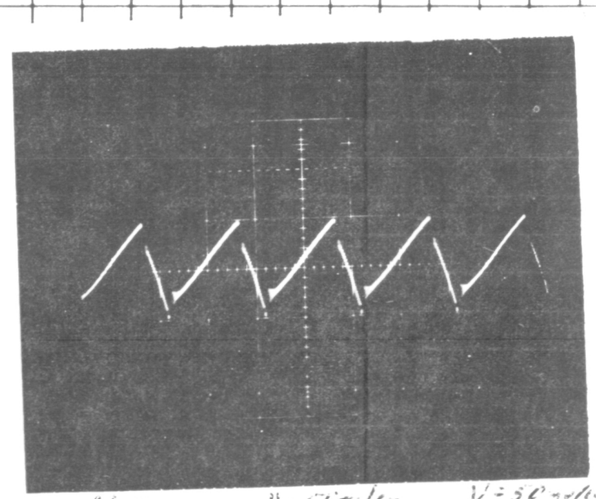
APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER	DATE	FUNCTIONAL MANAGER	DATE	REVIEWING PROJECT AUTHORITY	DATE

SYSTEMS 2453 REV. 12-65

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MESAC DATA SHEET

LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{ULEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}
1	Charge - Current Limit	I-C-2																	
2	# 1		26.94	0	4.3		6.83			9.3									
3	# 2		26.92	0	4.3			6.88			9.1								
4	# 3		26.92	0	4.3				6.72			9.3							
5																			
6																			
7																			
8																			
9																			
10																			
11	Shunt - Normal Oper	I-D-1	26.93	4.2	7.45	1.4	6.53	6.48	6.84	off	off	9.3	23.0	4.2	.2	4.3			
12																			
13																			
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V_{LB} H-5V/div V-5V/div

APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER — DATE	FUNCTIONAL MANAGER — DATE	REVIEWING PROJECT AUTHORITY — DATE

SYSTEMS 2452 REV. 12-65

PAGE MISSING FROM AVAILABLE VERSION

MESAC DATA SHEET

LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																		
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{ULEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}		
1	Shunt - Full load	I-D-2	26.94	.27	.47	8.8	-	-	-	off	off	off	23.9	4.2	0.2	7.2				No measurable ripple.	
2																					
3																					
4																					
5																					
6																					
7																					
8																					
9																					
10	Charge Control	I-E-1																			
11	#1						7.76			8.55							.090			Cycles on and off after once going off	
12	#2							7.84			7.9							.090		Cycles on and off after once going off	
13	#3								7.8			8.7							.135	No cycling	
14																					
15																					
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APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER	DATE	FUNCTIONAL MANAGER	DATE	REVIEWING PROJECT AUTHORITY	DATE

SYSTEMS 2459 REV 12-65

PAGE MISSING FROM AVAILABLE VERSION

MESAC DATA SHEET

LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																						
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBRA}	V_{ULRA}	V_{PLRA}	V_{CSRA}	V_{361}	V_{362}	V_{363}		I_{MON}	P_{IN}	P_O	EFF_L	
1	Efficiency - Uplinks -	II-A-1																							
2	#1		26.9	2.0			6.29			11.4											.04	71.6	53.8	75%	
3			26.9	2.0			6.1			11.9												72.5	53.8	74.2	
4			26.9	2.0			6.0			12.2												73.2	53.8	73.5	
5			26.9	2.0			5.88			12.7												74.6	53.8	72	
6			26.9	2.0			5.8			12.9												74.6	53.8	72	
7																									Starts to become non-linear @ ≈ 5.77
8	#2		26.9	2.0				6.34			10.8											69.5	53.8	78.7	
9			26.9	2.0				6.3			10.9											69.7	53.8	78.5	
10			26.9	2.0				6.2			11.1											68.9	53.8	78.1	
11																									
12																									
13																									
14	#3		26.9	2.0					6.39			10.8										69	53.8	78%	
15			26.9	2.0					6.3			11.0										69.3	53.8	77.7	
16			26.9	2.0					6.2			11.4										70.7	53.8	76.1	
17			26.9	2.0					6.1			11.6										70.7	53.8	76.1	
18																									
19																									
20																									
21	Efficiency - Uplink - nominal	II-A-2																							
22	#2		26.9	1.32				6.3			6.8											42.9	35.6	83.2%	
23			26.9	1.32				6.2			7.0											43.4	35.6	82.2	
24			26.9	1.32				6.1			7.1											43.4	35.6	82.2	
25																									
26																									
27																									
28	Efficiency - Uplink - min.	II-A-3	26.9	.13				6.3			.96											6.05	3.5	58%	
29																									
30																									
31																									
32																									
33																									
34																									

APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER	DATE	FUNCTIONAL MANAGER	DATE	REVIEWING PROJECT AUTHORITY	DATE

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MESAC DATA SHEET

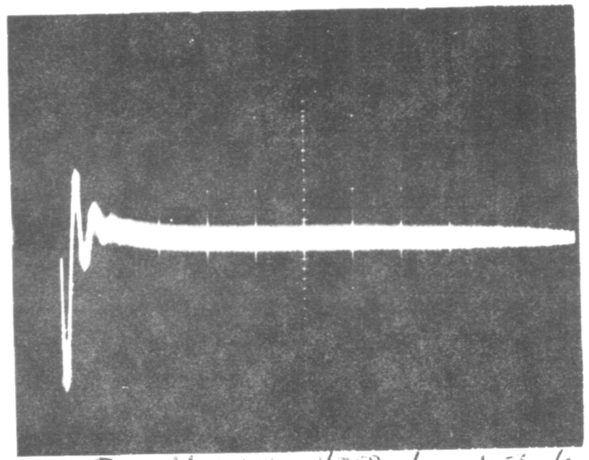
LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																							
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LDRA}	V_{ULRA}	V_{PLRA}	V_{CSRA}	V_{3B1}	V_{3B2}	V_{3B3}		I_{CUM}		P_{in}	P_o	E_{ff}
1	Efficiency - Downlink-Max	II-B-1																								
2	#1		26.93		3.8		7.4			9.2											.05		102.8	69	66.6
3	2		26.94		3.5			7.7			8.7												94.2	67	71.2%
4	3		26.94		3.75				7.4			9.4											101	69.5	69%
5																										
6																										
7																										
8	Nom	II-B-2																								
9	#1		26.93		1.43		7.18			4.0													39.5	28.8	74.9
10	2		26.93		1.6			7.34			4.0												43.1	29.4	68.2
11	3		26.93		1.6				7.15			4.0											43.1	28.6	66.4
12																										
13																										
14	Min	II-B-3																								
15	#1		26.93		.76		7.09			2.0													20.5	14.2	69.2
16	2		26.93		.88			7.19			2.0												23.7	14.4	60.5
17	3		26.93		1.1				7.04			2.0											29.6	14.1	47.7
18																										
19																										
20																										
21																										
22																										
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APPROVALS	PROJECT, WORK PACKAGE, WORK UNIT MANAGER	DATE	FUNCTIONAL MANAGER	DATE	REVIEWING PROJECT AUTHORITY	DATE

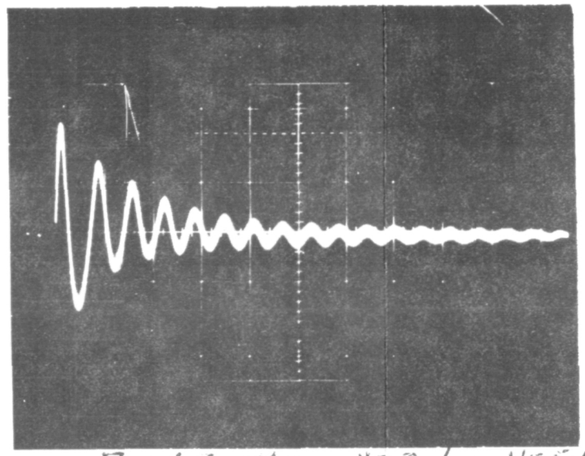
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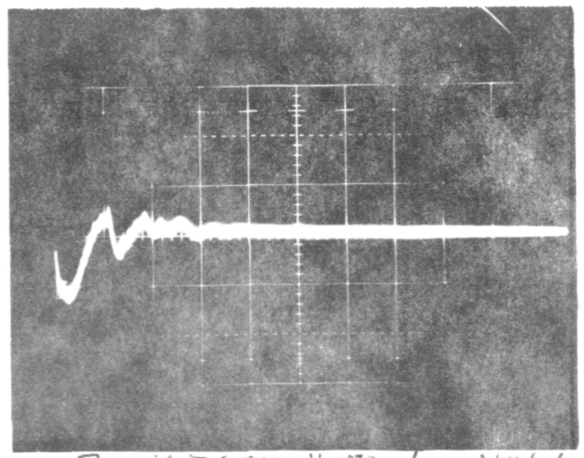
LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{VLEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}
1	Time Response — V_0 SA	III-A-1																	
2																			
3	14 Ω		26.9	2.0			6.58	6.14	6.75	1.5	6.5	2.9							
4	6.5 Ω		26.9	4.1			6.35	6.09	6.17	7.4	8.8	6.2							
5																			
6																			
7																			
8																			
9																			
10																			
11																			
12																			
13																			
14																			
15																			
16																			
17																			
18																			
19	Time Resp - No SA - Failure III-A-2																		
20	14 Ω		26.9	2.0			6.49	—	5.91	.8	—	13.0							
21	Conv 1 & 3 6.5 Ω		26.9	4.0			6.25	—	5.80	9.0	—	13.0							
22																			
23																			
24																			
25																			
26																			
27																			
28																			
29																			
30																			
31																			
32																			
33																			
34																			



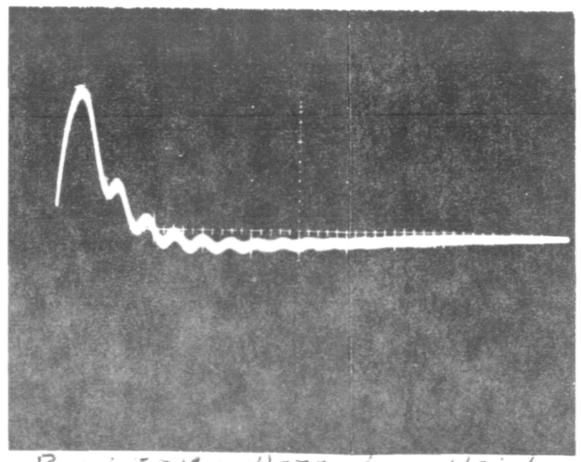
R_L - 14 → 6.5 Ω H = 50 ms/cm V = 5 v/cm



R_L = 6.5 → 14 Ω H = 50 ms/cm V = 5 v/cm



R_L = 14 → 6.5 Ω H = 20 ms/cm V = 1 v/cm



R_L = 6.5 → 14 Ω H = 20 ms/cm V = 1 v/cm

APPROVALS

PROJECT, WORK PACKAGE, WORK UNIT MANAGER — DATE

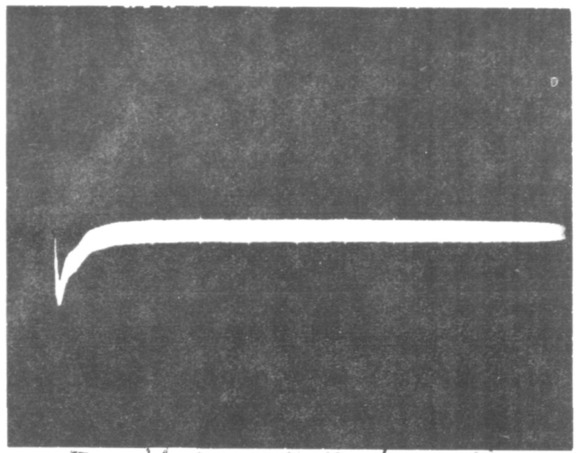
FUNCTIONAL MANAGER — DATE

REVIEWING PROJECT AUTHORITY — DATE

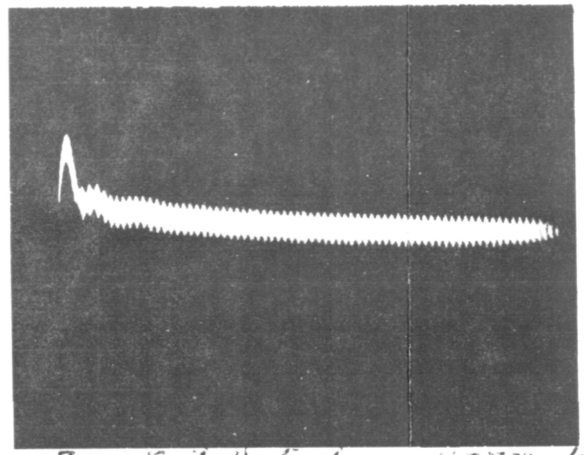
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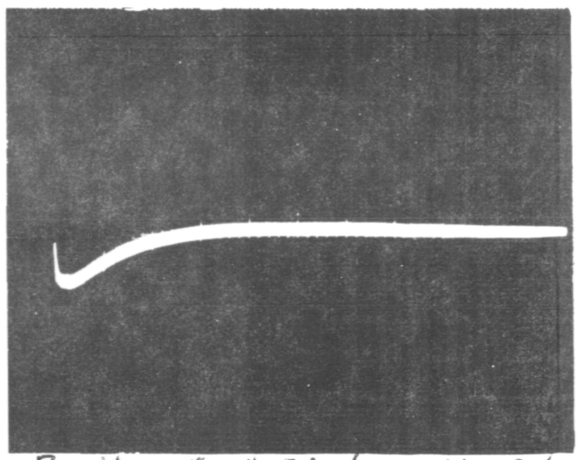
LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	V_{LBEA}	V_{ULEA}	V_{PLEA}	V_{CSEA}	V_{3E1}	V_{3E2}	V_{3E3}
1	Time response with SA - no	III-B-1																	
2	shunting																		
3	14 Ω		26.9	2.0	7.9	–	6.62	6.83	6.99	.3	7.0	9.2							
4	6.5 Ω		26.9	4.1	7.8	–	6.61	6.61	6.92	.1	.6	9.3							
5																			
6																			
7																			
8																			
9																			
10																			
11																			
12																			
13																			
14																			
15																			
16																			
17																			
18																			
19	Time response with SA -	III-B-2																	
20	Shunting (Conv. #2630)																		
21																			
22	14 Ω		26.9	2.0	5.6	3.6	7.30	–	–	9.2	–	–							
23	6.5 Ω		26.9	4.1	7.8	0	7.25	–	–	9.3	–	–							
24																			
25																			
26																			
27																			
28																			
29																			
30																			
31																			
32																			
33																			
34																			



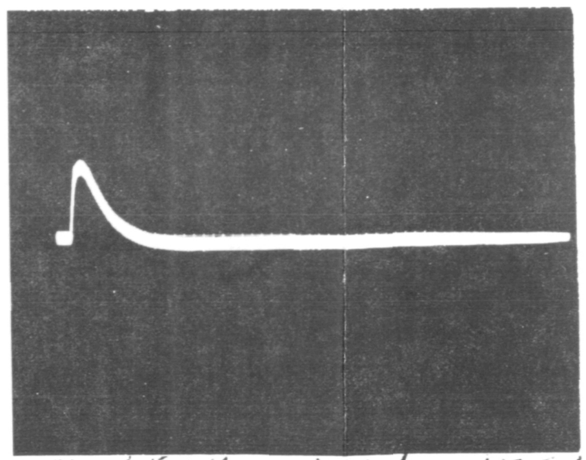
R_L = 14 → 6.5 Ω H = 10 ms/cm V = 200 volts/cm



R_L = 6.5 → 14 Ω H = 5 ms/cm V = 200 volts/cm



R_L = 14 → 6.5 Ω H = 20 ms/cm V = 5 volts/cm



R_L = 6.5 → 14 Ω H = 20 ms/cm V = 5 volts/cm

APPROVALS

PROJECT

FUNCTIONAL MANAGER

QUALITY

DATE

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LINE NO.	WORK DESCRIPTION	SUB ELEMENT NUMBER	Data																		
			V_{LB}	I_L	I_{SA}	I_{SH}	V_{B1}	V_{B2}	V_{B3}	I_{B1}	I_{B2}	I_{B3}	$\bar{V}_{LBRA}$	$\bar{V}_{ULRA}$	$\bar{V}_{PLRA}$	$\bar{V}_{CSRA}$	V_{SE1}	V_{SE2}	V_{SE3}		
1	Simulated Orbits	IV-A															mv	mv	mv		
2	Sun = 60 min, Eclips = 40 min																				
3	0900 3/12/70 t = 0 min		26.98	4.2	–	–	6.64	6.69	6.82	10.0	6.9	4.1					10	42	-20		
4	5		26.90	4.2	–	–	6.41	6.37	6.41	6.55	8.0	7.0					55	55	-20		
5	10		26.90	4.2			6.33	6.24	6.28	6.3	8.2	7.5					60	47	-23		
6	20		26.90	4.2	–	–	6.20	6.08	6.09	7.0	7.9	7.8					60	24	-33		
7	30		26.86	4.2	–	–	6.03	5.97	5.98	8.5	7.4	7.3					42	10	-38		
8	End of Eclips 39		26.84	4.2	–	–	5.95	5.91	5.88	8.0	7.55	7.9					30	0	-38		
9	Start of Sun 40		26.92	4.2	8.1	–	6.23	6.32	6.60	8.1	1.2	9.65						27	+42	3rd electrode sensor didn't reset on Batt #1	
10	45		26.92	4.2	8.1	–	6.31	6.37	6.77	0.18	0.7	9.3					28	26	+42	After manual reset of 3rd electrode on Batt #1	
11	50		26.92	4.2	8.1	–	6.35	6.40	6.90	0.13	0.59	9.3					25	24	+40		
12	60		26.92	4.2	8.1	–	6.37	6.43	7.13	.040	0.50	9.1					18	13	+32		
13	70		26.92	4.2	8.1	–	6.37	6.40	7.46	-.020	0.45	8.8					15	7	+60		
14	74		26.92	4.2	8.1	–	6.45	6.57	7.72	1.6	9.1	0					15	20	+122	Batt. #3 is shut off, begins recycling	
15	80		26.92	4.2	8.1	–	6.50	6.88	7.07	1.6	8.9	0					15	25	+40		
16	90		26.92	4.2	8.1	–	6.56	7.06	7.07	1.6	8.6	0					15	23	+40		
17	End of Sun 99		26.92	4.2	8.1	–	6.61	7.21	7.04	1.8	8.4	0					13	24	+35		
18	Start of Eclips 100		26.88	4.2	–	–	6.10	6.49	6.59	8.6	7.4	5.4					0	-12	+10		
19	110		26.89	4.2	–	–	5.93	6.24	6.35	7.4	7.5	7.6					0	-10	- 2		
20	120		26.93	4.2	–	–	5.98	6.05	6.19	7.3	7.7	7.5					0	-13	-23		
21	130		26.75	4.2	–	–	5.85	5.88	6.06	7.4	8.3	7.5					0	-16	-35		
22	End of Eclips 139		26.76	4.2	–	–	5.84	5.83	5.96	7.4	8.5	7.5					0	-16	-35		
23	Start of Sun 140		26.92	4.2	8.15	–	6.14	6.24	6.61	0.18	1.1	9.45					+10	+ 1	+45		
24	150		26.92	4.2	8.15	–	6.25	6.37	6.96	0.19	0.95	9.20					+12	+10	+40		
25	160		26.92	4.2	8.15	–	6.29	6.41	7.19	0.19	0.7	9.1					+10	+ 7	+40		
26	170		26.92	4.2	8.15	–	6.29	6.43	7.74	0.45	0.5	8.8					+10	+ 5	+125	Batt. # 3 is shut off, begins recycling	
27	180		26.98	4.2	8.15	–	6.46	6.93	6.83	2.0	8.9	0					+10	+22	+40	Batt. # 3 stopped recycling	
28	190		26.92	4.2	8.15	–	6.52	7.09	6.76	2.1	8.6	0					+13	+20	+40		
29	End of Sun 200		26.92	4.2	8.15	–	6.58	7.23	6.72	2.2	8.4	0					+13	+23	+35		
30																					
31																					
32																					
33																					
34																					

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UPLINK

```
20 DIM M(22,2)
40 R1=1
60 DIM P(7),W(7),F(7)
80 FØR L=1 TØ 7
100 READ F(L),P(L),W(L)
120 NEXT L
140 FØR J= 1 TØ 5
160 PRINT
180 NEXT J
200 FØR J= 1 TØ 7
220 READ C(J)
240 NEXT J
260 PRINT , "MESAC"
280 PRINT
300 PRINT"ESU UPLINK CØNVERTER DATA"
320 PRINT
340 PRINT
360 PRINT "MAX.ALLØWABLE DØD";
380 INPUT D1
400 PRINT "ECLIPSE PERIØD,HR.";
420 INPUT T1
440 PRINT
460 FØR J= 1 TØ 7
480 I1=(C(J)/T1)*D1/100
500 P4=.33*I1
520 P5=.11*I1
600 T2=.25+.004*I1
610 FØR L= 3 TØ 7
612 FØR Q= 1 TØ 5
614 PRINT
616 NEXT Q
620 PRINT"RUN NØ.";R1
640 PRINT
660 PRINT "CAPACITY =";C(J);"A-H"
680 PRINT "FREQUENCY =";F(L);"KHZ"
700 PRINT"AVERAGE CURRENT = ";I1;"AMPS"
720 PRINT"T(ØFF)=";T2;"MICRØSEC."
740 PRINT
760 PRINT "NØ. ØF CELLS","EFFICIENCY","P(ØUT)","WEIGHT"
780 PRINT
800 FØR N= 2 TØ 22 STEP 2
820 P1=N*1.23*I1
840 P3=4*F(L)*P1*T2
841 P3=P3/1000
860 P7=.044*P1
880 A2=5.789399
900 B2=-.3077886
920 S2=A2*P1↑B2
940 P8=(P1*P(L)*S2)/100
960 W1=.002*P1
980 A1=.077767E-01
1000 B1=.8525585
1020 S1=A1*P1↑B1
1040 W2 = W(L)*S1*2.2
```

```
1042 W3=W1+W2
1060 M(N,1)=P1
1080 M(N,2)=P8
1120 P0=P1-(P3+P4+P5+P7+P8)
1122 IF P0 > 100 THEN1130
1124 W3=W3*1.5
1126 G0 T0 1140
1130 W3=W3*1.333333
1140 PRINT N,P0*100/P1,P0,W3
1160 NEXT N
1180 PRINT
1200 PRINT,"SUMMARY 0F L0SSES"
1212 PRINT,"% 0F INPUT P0WER"
1215 PRINT
1220 PRINT"DI0DE L0SS = 4.4 %"
1240 PRINT "QSWITCHING L0SS=";4*F(L)*T2*.1
1260 PRINT
1280 PRINT"N0.0F CELLS","QSAT L0SS","QDRIVE L0SS","FILTER L0SS"
1300 PRINT
1310 F0R N= 2 T0 22 STEP 2
1320 PRINT N,P4*100/M(N,1),P5*100/M(N,1),M(N,2)*100/M(N,1)
1340 NEXT N
1350 R1=R1+1
1360 NEXT L
1380 NEXT J
2000 DATA 1,1.71,3.15,2,1.2,1.65,4,.92,.87,8,.80,.465,16,.84,.305
2001 DATA 32,1.02,.211,64,1.42,.15,1,3,6,9,12,15,20
```

DLINK

```
100 REM THIS IS A FILE NAMED D0WNLINK, F0R USE IN MESAC
110 DIM F(7),P(7),W(7),X(7)
120 DIM M(22,5)
130 R1=1
140 F0R L= 1 T0 7
150 READ F(L), P(L),W(L),X(L)
160 NEXT L
170 F0R J= 1 T0 7
180 READ C(J)
190 NEXT J
200 READ A1,B1,A2,B2,A3,B3,E1
210 F0R Q = 1 T0 5
220 PRINT
230 NEXT Q
240 PRINT,"MESAC"
250 PRINT,"ESU D0WNLINK C0NVERTER DATA"
260 PRINT
270 PRINT"AVAILABLE CHARGE TIME,HR.";
280 INPUT T1
290 PRINT"MAXIMUM ALL0WABLE D0D";
300 INPUT D1
310 PRINT
320 F0R J= 1 T0 7
330 N1=1
340 I1=(C(J)*D1)/(T1*N1*100)
350 Y9=I1/C(J)
360 N3=(36.744+46.414*Y9-1363.713*Y9↑2+1352.78*Y9↑3)/100
370 IF ABS (N3-N1) < .01 THEN 400
380 N1=N3-(N3-N1)/4
390 G0 T0 340
400 F0R L= 1 T0 7
410 F0R Q= 1 T0 5
420 PRINT
430 NEXT Q
440 PRINT"RUN N0. ";R1
450 PRINT
460 PRINT"CAPACITY =";C(J);"A-H"
470 PRINT"FREQ. =";F(L);"KHZ"
480 PRINT"CURRENT =" ;I1;"AMPS"
490 PRINT
500 PRINT"N0.0F CELLS","EFFICIENCY","P(0UT","WEIGHT","RECT.TYPE"
510 PRINT
520 F0R N= 2 T0 22 STEP 2
530 P0=I1*N*E1
540P7=.67*.5*I1
550 T3=.25+.004*I1
560 P8=1.9*F(L)*P0*T3*1E-03
570 P9=.11*I1
580P6=.91*I1
590 IF N>2 THEN 630
600IF P6<=P7+P8+P9 THEN 630
610 K1=1
620 G0 T0 640
630 K1=0
```

```
640 P1=A3*F(L)↑B3
650 P1=P1*P0/90
660 P2=.025*I1*(N*E1+.9)*.5
670 T2=.25+(.004*I1*N*E1)/28
680 P3=5.6*F(L)*I1*(N*E1+.9)*T2*1E-03
690 P4=.0039*I1*(N*E1+.9)
700 S2=A2*P0↑B2
710 P5=P(L)*P0*S2/100
720 M(N,1)=P2+P3+P4
730 M(N,2)=P1
740 M(N,3)=P5
750 S1=A1*P0↑B1
760 W2=X(L)*S1*1.1
770 W4=.0015*P0
780 IF K1=0 THEN 860
790 N2=P0/(P0+P1+P2+P3+P4+P5+P7+P8+P9)
800 I9=P0*1.5/N2
810 S1=A1*I9↑B1
820 W1=W(L)*S1
830 M(N,4)=P7+P8+P9
840 W3=.0015*P0+.13*W2
850 GØ TØ 970
860 N2=P0/(P0+P1+P2+P3+P4+P5+P6)
870 I9=P0*1.5/N2
880 S1=A1*I9↑B1
890 W1=W(L)*S1
900 W3=.0015*P0
910 M(N,4)=P6
920 W7= W1+W2+W3+W4
930 IF P0>100 THEN 960
940 W7=W7*1.5
950 GØ TØ 970
960 W7=W7*1.333333
970 PRINT N,N2,P0,W7,
980 M(N,5)=P0/N2
990 IF K1=0THEN 1020
1000 PRINT"SYNCH.RECT"
1010GØ TØ 1030
1020 PRINT"DIØDE"
1030 NEXT N
1040 R1=R1+1
1050 PRINT
1060 PRINT,"SUMMARY ØF LØSSES"
1070 PRINT,"% ØF INPUT PØWER"
1080 PRINT
1090 PRINT"NØ.ØF CELLS","INV.LØSS","FILT.LØSS","XFMR LØSS","RECT.LØSS"
1100 PRINT
1110 FØR N= 2 TØ 22 STEP 2
1120 I8=M(N,5)
1130 PRINTN,M(N,1)*100/I8,M(N,2)*100/I8,M(N,3)*100/I8,M(N,4)*100/I8
1140 NEXT N
1150 NEXT L
1160 NEXT J
1170 DATA 1,1.71,2.2,3.15,2,1.2,1.12,1.65,4,.92,.685,.87,8,.8,.49,.465
```

```
1180 DATA 16,.84,.395,.305,32,1.02,.33,.211,64,1.42,.28,.15
1190 DATA 1,3,6,9,12,15,20
1200 DATA .077767E-01,.8525585,5.789399,-.3077886,.69,-.0626587
1210 DATA 1.41
```

REL

```
10 ØPEN /MER-O/,ØUTPUT
15 FØR J= 1 TØ 13
20 READ K
25 PRINT FILE K,
30 NEXT J
35 DATA 6,.99982925,.99088757,.99958028,.98185818,.99925380,.9729110
40 DATA .99885053,.96404549,.99837120,.95526069,.99781655,.94655595
50 FØR J=1 TØ 5
60 PRINT
70 NEXT J
80 PRINT,"BATTERY RELIABILITY CALCULATIØN"
90 PRINT
120 FØR Y= 1 TØ 6
122 FØR J= 1 TØ 5
124 PRINT
126 NEXT J
130 READ L(Y),M(Y)
140 PRINT Y;"YEARS"
150 PRINT
160 PRINT "NØ. ØF CELLS","CELL REL.","BAT. REL."
170 FØR N= 2 TØ 22 STEP 2
180 Z=L(Y)+M(Y)*(N-2)/20
185 Q=Z*8760*1.OE-9
190 R1=EXP(-Q)
200 R2= R1↑N
210 PRINT N,R1,R2
220 PRINT FILE R2,
230 NEXT N
240 NEXT Y
250 DATA 62,0,137,0,229,0,391,0,689,0,1206,0
```

PROGRAM; MESREL

```
70 FØR J= 1 TØ 7
80 PRINT
90NEXT J
100 DIM C(16,11)
110 FØR I= 0 TØ 15
120 FØR N=0 TØ 11
130 READ A
140 IF A= 0 THEN 170
150 C(I,N)= A
160 NEXT N
170 NEXT I
180 PRINT "MESAC RELIABILITY ANALYSIS"
190 PRINT
200 PRINT "MINIMUM NØ. ØF ESU'S INSTALLED";
210 INPUT I1
220 PRINT "MAXIMUM NØ. ØF ESU'S INSTALLED";
230 INPUT I2
240 PRINT"MAXIMUM ALLØWABLE % FAILURES";
250 INPUT F1
260 ØPEN /MER-0/,INPUT
270 INPUT FILE T1
280 DIM R(2,T1),Q(22,T1)
290FØR T=1 TØ T1
300 INPUT FILE R(1,T),R(2,T)
310 NEXT T
320 FØR T=1 TØ T1
330 FØR S=2 TØ 22 STEP 2
332 INPUT FILE Q(S,T)
334 NEXT S
336 NEXT T
338 FØR T= 1 TØ T1
340 FØR S= 2 TØ 22 STEP 2
342 FØR J= 1 TØ 5
344 PRINT
346 NEXT J
360 PRINT,T;"YEARS"
370 PRINT,S;"CELL BATTERY"
380 PRINT
390 PRINT "NØ.INSTALLED","NØ.FAILED","RELIABILITY","%REDUNDANCY"
400 PRINT
410 R1=R(2,T)*Q(S,T)
420 FØR I=I1 TØ I2
430 FØR F= 0 TØ INT(I*(F1/100)) + 1
440 A=0
450 FØR N= 0 TØ F
460 R2=C(I,N)*(R1↑(I-N)*(1-R1)↑N)
462 R2=R2*R(1,T)
470 A=A+R2
480 NEXT N
490 PRINT I,F,A,100*F/(I-F)
500 NEXT F
510 PRINT
520 NEXT I
530 FØR J= 1 TØ 5
```

```
540 PRINT
550 NEXT J
560 NEXT S
570 NEXT T
1000 DATA 1,0,1,1,0,1,2,1,0,1,3,3,1,0,1,4,6,4,1,0,1,5,10,10,5,1,(
1001 DATA 1,6,15,20,15,6,1,0,1,7,21,35,35,21,7,1,0,1,8,28,56,70,5
1002 DATA 28,8,1,0,1,9,36,84,126,126,84,36,9,1,0,1,10,45,120,210,
1003 DATA 210,120,45,10,1,0,1,11,55,165,330,462,462,330,165,55,11
1004 DATA 1,12,66,220,495,792,924,792,495,220,66,0,1,13,78,286,71
1005 DATA 1287,1716,1716,1287,715,286,0,1,14,91,364,1001,2002,30(
1006 DATA 3432,3003,2002,1001,0,1,15,105,455,1365,3003,5005,6435,
1007 DATA 5005,3003,0
```