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# A SYSTEM FOR MEASURING THE FREQUENCY STABILITY OF AN FM TV TRANSMITTER

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## FOREWORD

This report is a technical summary reporting the progress of studies conducted by the Microwave Research Laboratory of the Electrical Engineering Department, Auburn University, under the auspices of the Engineering Experiment Station toward fulfillment of Contract NAS8-26193. The report describes a sampled system of frequency measurement directed toward Task 1 dealing with systems required to yield high frequency stability in wide-band telemetry transmitters.

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A SYSTEM FOR MEASURING THE FREQUENCY

STABILITY OF AN FM TV TRANSMITTER

M. A. Honnell and J. M. Fontaine

## ABSTRACT

This report is concerned with the design and construction of a system for measuring the frequency stability of an S-band, FM TV transmitter.

The theory of a phaselock loop relevant to the design of the frequency measurement system is discussed with emphasis on the design equations. The design of each unit of the physical system is then presented along with the design considerations involved in the choice of system components.

The tests performed on the system are discussed along with a comparison between test results and calculated performance. Last, but not least, the results of a satisfactory measurement of the frequency of an S-band FM television transmitter is presented.

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# I. INTRODUCTION

One of the major considerations in the design of FM transmitters is frequency stability. The frequency stability requirement is imposed by the Federal Communications Commission in order to utilize the frequency spectrum more efficiently. In the case of transmitters built for space and military applications, the requirements for frequency stability are made even more stringent by the specifications of the Inter-Range Instrumentation Group (IRIG). Naturally, it is necessary to make measurements to insure that the transmitters meet the specifications. Often, making these measurements can be a very complex problem.

There are frequency counters available which can be used to measure the frequency of a transmitter which is not being modulated or of one which is being modulated by some type of symmetrical waveform, such as a sinusoidal wave. All of these devices measure frequency by counting cycles and averaging the count over some time interval, i.e., they measure the average frequency. Unfortunately, these devices cannot be used to measure the frequency of a transmitter which is frequency modulated by a composite video signal (television picture). The reason for this will be made clearer by reference to Fig. 1 and Fig. 2. Fig. 1 shows a general video waveform whose voltage varies from approximately -0.4 volts at the sync tip to about +1.0 volt during the brightest spots in the picture information. The result of modulating a radio-frequency

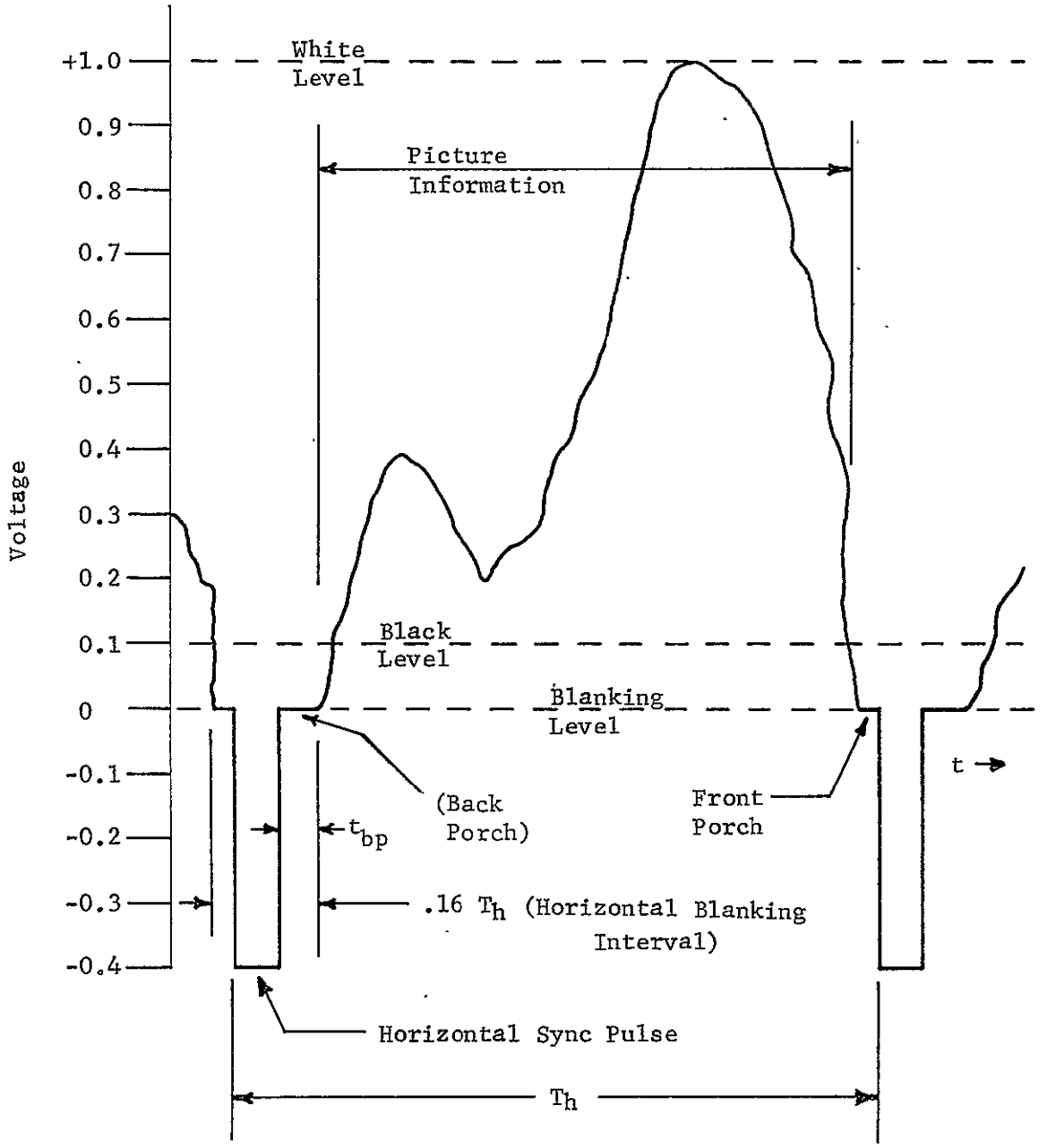


Fig. 1. Illustration of a composite video wave.

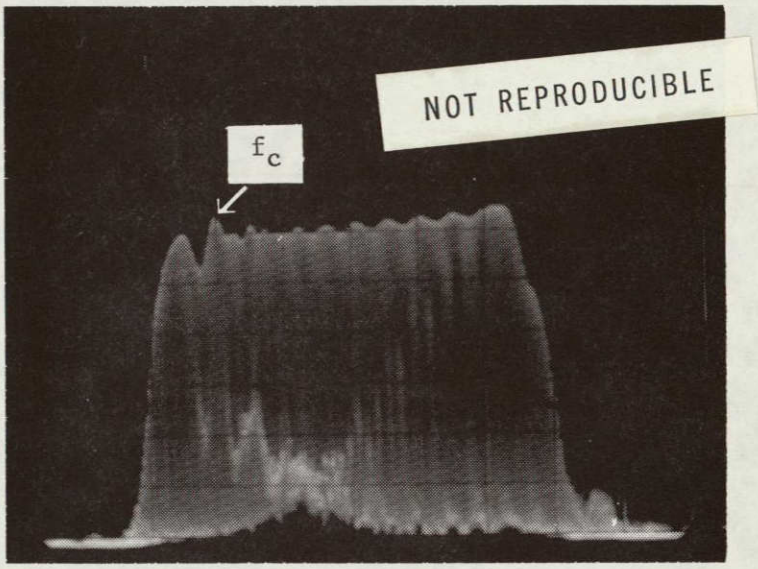


Fig. 2. Frequency spectrum resulting from frequency modulation of a TV radio-frequency carrier with a stair step.

carrier with this video signal is that the carrier is deviated farther in the high-frequency direction than in the low-frequency direction. The average frequency of the transmitter is therefore higher than the unmodulated carrier frequency so that the frequency measured by the counter is ambiguous. This would not be too much of a problem if the video signal were constant so that compensation could be made, but this is not the case. The video signal is dependent on the picture information and, changes from one scan line to the next. Fig. 2 is a representation of the frequency spectrum of an FM TV signal which is modulated by a stair-step composite video signal. The frequency $f_c$ in Fig. 2 is the reference frequency when the video signal is zero volts, corresponding to the back porch. It can be seen that the average frequency is higher than the reference, or back porch frequency. In order to make a measurement of the transmitter's frequency stability some method of sampling the frequency during the back-porch interval must be developed. The purpose of this paper is to present a method of doing this for a specific case.

The measuring system described was developed to measure the frequency of an S-band FM television transmitter which was designed for George C. Marshall Space Flight Center by Auburn University. The frequency of this transmitter is controlled by a Sampled Automatic Frequency Control system (SAFC) [1]. The basic operation of the control system is discussed below.

The output of the transmitter's voltage controlled oscillator is sampled once during each horizontal interval of the picture. The frequency of the VCO is compared to the frequency of a crystal

reference oscillator and a voltage, which is proportional to the frequency difference between the oscillators, is derived. This voltage is applied to the frequency control element of the VCO (a varactor diode), which shifts the VCO frequency in a direction which tends to reduce the frequency difference to zero.

The sampling is done during the back-porch interval of the composite video signal. The back-porch interval is shown in Fig. 1 as $t_{bp}$. There is a great deal of circuitry involved in the sampling operation. The sync pulse is stripped off of the video signal and is used to trigger a multivibrator which develop a sampling pulse occurring during the back porch interval. This pulse drives an RF switch, which gates the VCO output into the discriminator. A second pulse, delayed 30 microseconds, samples the reference frequency which is also gated into the discriminator. A voltage derived from the discriminator output signal is used to bias a varactor in a direction to correct the VCO frequency.

As was mentioned earlier, it is necessary to sample the carrier during the back-porch interval if a meaningful frequency measurement is to be made. One possible approach is to use an RF switch which is on only during the desired interval of time, i.e., during the back-porch interval of the video waveform. The block diagram of a circuit for performing this task is shown in Fig. 3. A time domain representation of the signal at the output of the switch is shown in Fig. 4. The circuit operation is discussed below.

The modulating signal is applied to the input of the sync stripper, where the sync pulse is stripped off and passed to the input of the

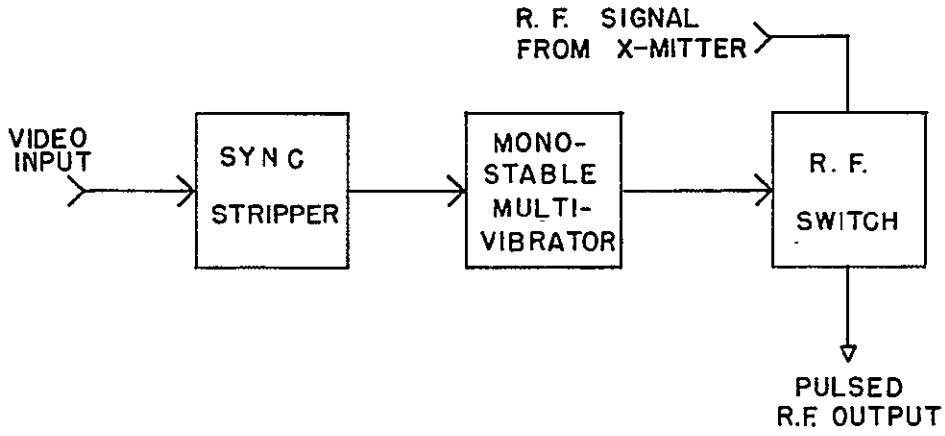


Fig. 3. Block diagram of a possible carrier sampling system.

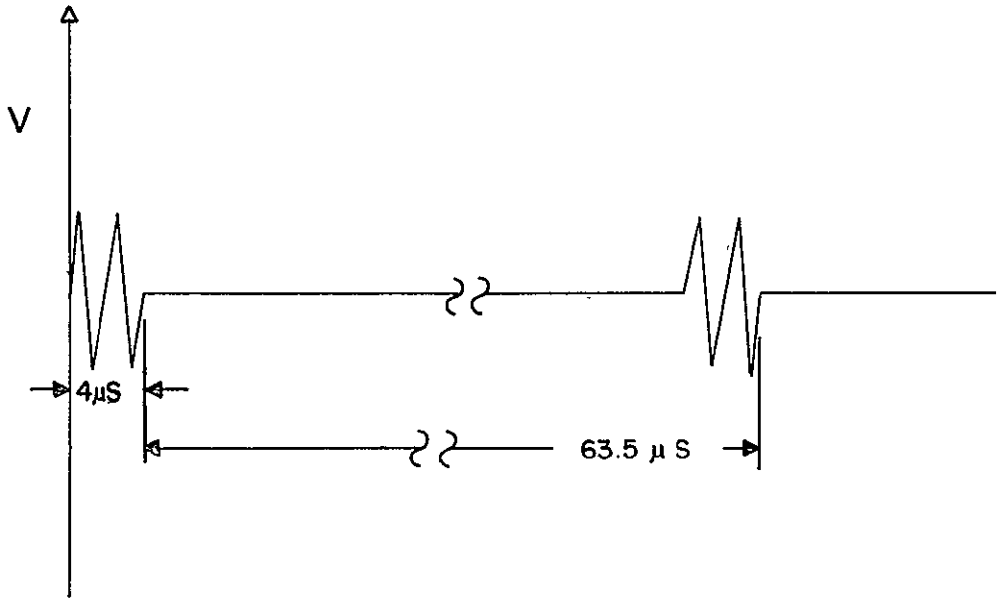


Fig. 4. Representation of the output waveform of the system shown in Fig. 3.

monostable multivibrator. The RC time constants of the multivibrator are such that it produces an output only during the back-porch interval. The output of the multivibrator is applied to the control input of a voltage-controlled RF switch allowing the RF signal from the transmitter to pass through it. The output of the switch is, therefore, a burst of RF energy which occurs during the back-porch interval of the video waveform and is at the frequency of the VCO corresponding to zero video volts.

Since the duration of the pulse burst is not precisely constant, the output of the switch is not suitable for use with a frequency counter. In addition, the digital counter available would not respond to the RF signal, but responded to the pulse repetition rate. The counter counted the rate at which the bursts of energy occur, rather than counting the number of cycles of RF within each burst of energy. These results were determined experimentally and the exact nature of the problem is not fully understood. It is believed that the burst of energy triggers the counter's flip-flop, causing it to count the repetition rate of the pulse burst. Although this approach seemed to offer a simple solution to the problem of determining the frequency of an FM TV transmitter, the problem with the counter meant that another solution had to be found.

The second approach to the problem proved to be feasible and is discussed in detail in the remainder of this paper. This second approach uses a phaselock loop to determine the frequency of the transmitter. The signal from the transmitter is first down converted

and then sampled during the back-porch interval. Then a phaselock loop is used to phaselock a voltage controlled oscillator to the down-converted sampled signal from the transmitter. The frequency of the voltage-controlled oscillator is then counted and used to determine the frequency of the transmitter. A block diagram of the system is shown on page 55.

## II. THEORY OF THE FREQUENCY MEASUREMENT SYSTEM

Phaselock techniques are often used in low-noise telemetry receivers in order to obtain a narrow noise bandwidth. Another important application of phaselock loops is the control of the frequency of an oscillator. The frequency measurement system to be discussed makes use of this second application. In the following paragraphs the theory of phaselock techniques is examined with special attention given to the frequency control aspects. Although the following analysis is for the phaselock characteristics of two continuous wave signals, it presents an insight into the locking characteristics of a VCO with an FM TV signal.

A block diagram of a simple phaselock loop is shown in Fig. 5. The loop consists of a phase detector, a voltage controlled oscillator (VCO), and a loop filter. The phase detector compares the input signal $V_s$ having a frequency $f_s$ and the VCO output signal $V_v$ having a frequency $f_v$ and produces an output voltage which is proportional to the phase difference between the two signals. The output signal is conditioned by the loop filter and is then applied to the frequency control element of the VCO. The result is a change in the phase of the VCO's output signal in a direction which tends to reduce to zero the phase difference between $V_s$ and $V_v$. In order to clarify the operation of the loop a mathematical analysis is given below.

When $f_s$ is equal to $f_v$, the phase detector output can be represented

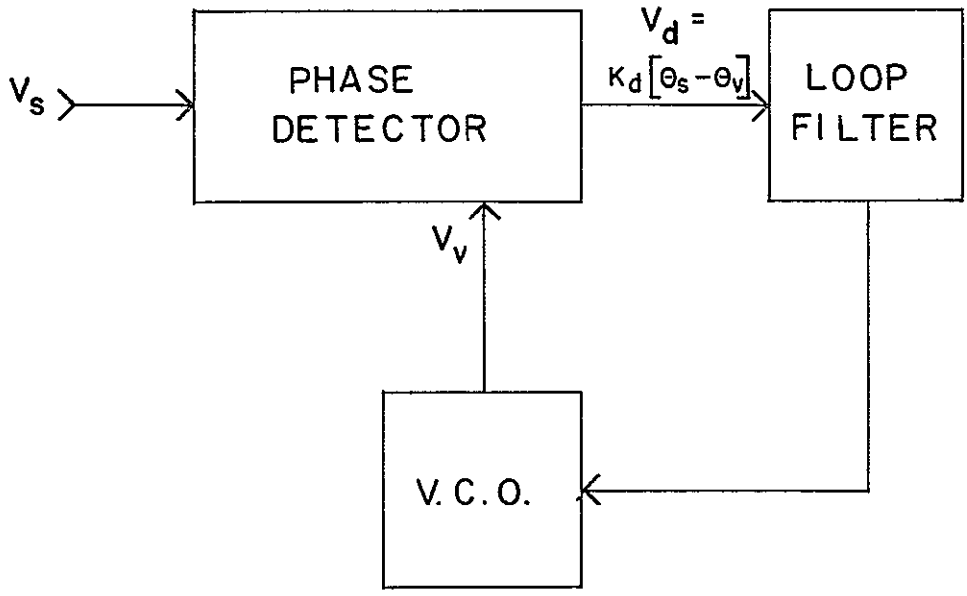


Fig. 5. Block diagram of a simple phaselock loop.

by

$$V_d = K_d(\theta_s - \theta_v) \tag{2-1}$$

where $K_d$ is the phase detector gain constant and $\theta_s$ and $\theta_v$ are the instantaneous phase angles of the input signal and the VCO output signal, respectively. $K_d$ has units of volts per radian and $\theta_s$ and $\theta_v$ have units of radians.

The filter has a transfer function given by

$$F(s) = \frac{V_f(s)}{V_d(s)} \quad . \tag{2-2}$$

The output of the filter is then

$$V_f(s) = V_d(s)F(s) \tag{2-3}$$

or

$$V_f(s) = F(s)K_d[\theta_s(s) - \theta_v(s)], \tag{2-4}$$

where $\theta_s(s)$, $\theta_v(s)$, $V_f(s)$, and $V_d(s)$ are the Laplace transforms of the appropriate terms.

The deviation of the VCO from its original frequency $f_c$ is

$$\Delta\omega = K_v V_f(t) \text{ radians/sec.} \tag{2-5}$$

where $K_v$ is the VCO gain constant. $K_v$ has dimensions of radians per second-volt. Remembering that frequency is the derivative of phase, the deviation of the frequency of the VCO from $f_c$ may be defined in terms of its phase angle deviation, $\theta_v(t)$, from $\omega_c t$ as

$$\Delta\omega = \frac{d\theta_v(t)}{dt} \tag{2-6}$$

where

$$\frac{d\theta_v(t)}{dt} = K_v V_f(t). \tag{2-7}$$

If both sides of the Equation (2-7) are integrated with respect to t, then

$$\theta_v(t) = \int K_v V_f(t)dt$$

or

$$\theta_v(t) = K_v \int V_f(t)dt. \tag{2-8}$$

This shows that the phase angle of the VCO output signal is proportional to the integral of the output of the loop filter. Equation (2-8) may also be expressed as a Laplace transform which will be more convenient to use in later work. When this is done equation (2-8) becomes

$$\theta_v(s) = \frac{K_v V_f(s)}{s}. \tag{2-9}$$

In order to determine the transfer function of the loop it is necessary to define $\theta_v(s)$ in terms of $\theta_s(s)$. Equation (2-9) is used as a starting point for this operation.

$$\theta_v(s) = \frac{K_v V_f(s)}{s}, \tag{2-9}$$

but

$$V_f(s) = F(s)V_d(s); \tag{2-3}$$

therefore

$$\theta_v(s) = \frac{K_v F(s) V_d(s)}{s} \quad . \tag{2-10}$$

$V_d(s)$ is given by Equation (2-4) as

$$V_d(s) = K_d[\theta_s(s) - \theta_v(s)]. \tag{2-4}$$

When Equation (2-4) is substituted into Equation (2-10) the following equation is obtained

$$\theta_v(s) = \frac{K_v K_d F(s)[\theta_s(s) - \theta_v(s)]}{s} \quad . \tag{2-11}$$

When Equation (2-11) is solved for $\theta_v(s)$, the solution is

$$\theta_v(s) = \frac{K_v K_d F(s) \theta_s(s)}{s + K_v K_d F(s)} \quad . \tag{2-12}$$

The transfer function of the loop is given by

$$H(s) = \frac{\theta_v(s)}{\theta_s(s)} = \frac{K_v K_d F(s)}{s + K_v K_d F(s)} \quad . \tag{2-13}$$

In order to completely define the loop transfer function it is necessary to determine the transfer function of the loop filter. Fig. 6

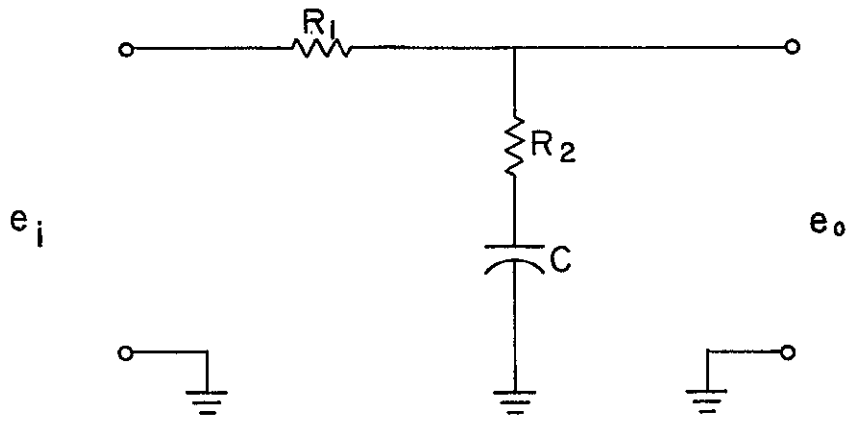


Fig. 6. Schematic diagram of a common loop filter.

is a schematic diagram of a common phaselock loop filter. The filter may be recognized as the lag compensator found in control systems. The transfer function of this filter is given by Gardner [2] as

$$F(s) = \frac{SCR_2 + 1}{SC(R_1 + R_2) + 1} \quad . \tag{2-14}$$

If $R_1C$ is renamed $\tau_1$ and $R_2C$ is renamed $\tau_2$ then Equation (2-14) becomes

$$F(s) = \frac{s\tau_2 + 1}{s(\tau_1+\tau_2) + 1} \quad . \tag{2-15}$$

Equation (2-15) can now be substituted into Equation (2-13) to obtain the transfer function of a phaselock loop which uses the filter shown in Fig. 6.

$$H(s) = \frac{K_v K_d \dfrac{s\tau_2+1}{s(\tau_1+\tau_2)+1}}{s + K_v K_d \dfrac{s\tau_2+1}{s(\tau_1+\tau_2)+1}} \tag{2-16}$$

$$= \frac{K_v K_d (s\tau_2+1)}{s^2(\tau_1+\tau_2)+s+K_v K_d (s\tau_2+1)}$$

$$= \frac{K_v K_d (s\tau_2+1)/(\tau_1+\tau_2)}{s^2 + s/(\tau_1+\tau_2)+K_v K_d s\tau_2/(\tau_1+\tau_2) + K_v K_d/(\tau_1+\tau_2)}$$

$$H(s) = \frac{K_v K_d (s\tau_2+1)/(\tau_1+\tau_2)}{s^2 + s(1+K_v K_d \tau_2)/(\tau_1+\tau_2) + K_v K_d/(\tau_1+\tau_2)} \quad . \tag{2-17}$$

The transfer function can also be found in terms of the damping factor and the natural frequency of the loop. If the natural frequency $\omega_n$ is defined as

$$\omega_n = \left(\frac{K_v K_d}{\tau_1+\tau_2}\right)^{1/2} \tag{2-18}$$

and the damping factor $\zeta$ is defined as

$$\zeta = 1/2\left(\frac{K_v K_d}{\tau_1+\tau_2}\right)^{1/2}\left(\tau_2 + \frac{1}{K_v K_d}\right) \tag{2-19}$$

then, according to Gardner, H(s) becomes

$$H(s) = \frac{s\omega_n(2\zeta - \omega_n/K_v K_d) + \omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2} \quad . \tag{2-20}$$

The transfer function is an important quantity in any type of control system, but there are other quantities involved in a phase-lock loop which give a better indication of the loop's ability to control the frequency of an oscillator. Some of these quantities are the hold-in range, the acquisition range, and the pull-out frequency. These quantities will be discussed in detail, but first it is desirable to briefly describe the operation of the phase detector.

Dishington [3] did much of the preliminary analytical work on four-diode phase detectors of the type shown schematically in Fig. 7. This phase detector is also known as a ring modulator or a doubly balanced mixer. In the normal locked mode of operation of a phaselock loop the frequencies of the input signal $V_s$ and the VCO signal $V_v$ are equal and differ in phase by the angle $\phi$. The output of the phase detector is then given by

$$V_d = K_d[\sin(2\omega_s t+\phi) + \sin\phi]. \tag{2-21}$$

The first term in the brackets is a high-frequency term which is removed by an RF filter at the output of the detector. The phase detector output is then given by

$$V_d = K_d\sin\phi. \tag{2-22}$$

If the phase difference between the two signals is small, $\sin\phi$ may be replaced by $\phi$ and Equation (2-22) becomes

$$V_d = K_d\phi. \tag{2-23}$$

With the information available it is now possible to determine the hold-in range. The hold-in range is the frequency range over which the VCO will track the input signal. The hold-in range is the most important characteristic of the loop when frequency control is the

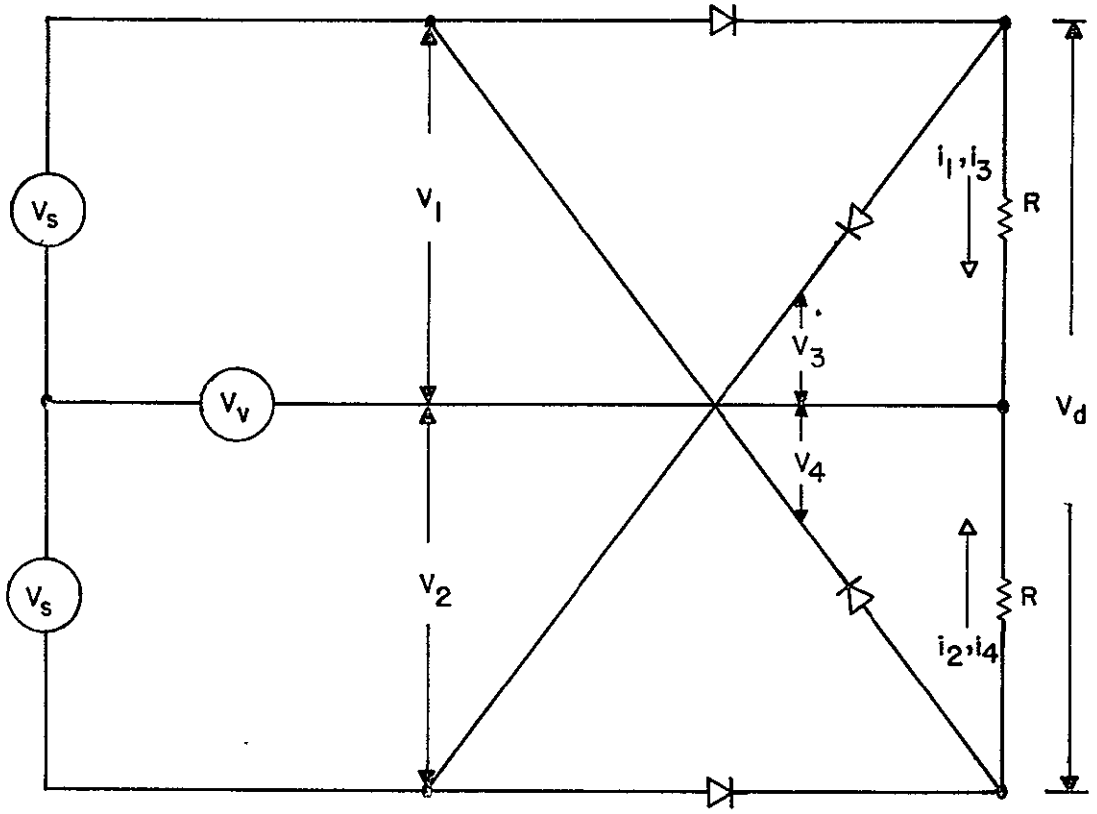


Fig. 7. Simplified schematic diagram of the phase detector.

prime objective.

The frequency deviation of the VCO, according to Equation (2-5), can be written as

$$\Delta\omega = K_v V_f(t) \tag{2-24}$$

where $V_f(t)$ is the output of the filter between the phase detector and the VCO. When the system is in lock the output of the phase detector, input to the filter, is a constant and the steady state output of the filter is

$$V_f(t) = K_d F(0)\phi \tag{2-25}$$

where $\phi = \theta_s - \theta_v$ is a constant. The frequency deviation for this case can then be written as

$$\Delta\omega = K_v K_d F(0)\phi \tag{2-26}$$

or if $K_1$ is defined as

$$K_1 = K_d K_v F(0) \tag{2-27}$$

then

$$\Delta\omega = K_1\phi. \tag{2-28}$$

Equation (2-28) holds only when the loop is locked and during this time $\sin\phi$ must be between $\pm 1$. The hold-in range is

$$\Delta\omega_H = \pm K_1. \tag{2-29}$$

The hold-in range can be seen to be a function of the DC gain of the loop.

Another quantity of interest is the pull-out frequency. This quantity determines the response of the loop to a frequency step. The pull-out frequency has been experimentally determined by Viterbi [5] and an equation has been written which gives the pull-out frequency as

$$\Delta\omega_{po} = 1.8\omega_n(\zeta+1) \quad . \tag{2-30}$$

It is also useful to determine the rate at which the input frequency can be changed without causing the loop to lose lock. This has also been determined by Viterbi and is given by the following equation.

$$\frac{d\Delta\omega}{dt} = \omega_n^2 \tag{2-31}$$

Two other quantities that are of interest are the lock-in frequency $\Delta\omega_L$ and the pull-in frequency $\Delta\omega_p$. The equation for the lock-in frequency is due to Richman [6] and is

$$\Delta\omega_L = 2\zeta\omega_n. \tag{2-32}$$

This equation is a measure of the frequency range within which the loop locks immediately. The pull-in equation is also due to Richman and it is a measure of the frequency range within which the loop will eventually lock. The equation is given by Gardner as

$$\Delta\omega_p = \sqrt{2}\,(2\zeta\omega_n K_1 - \omega_n^2)^{1/2}. \tag{2-33}$$

When $K_1$ is large, Equation (2-33) reduces to

$$\Delta\omega_p = 2\sqrt{\zeta\omega_n K_1}. \tag{2-34}$$

The basic theory upon which the frequency measurement system depends has now been presented. The application of this theory to the measurement system will be examined in the remainder of this section.

It has been shown that the output of the phase detector is dependent only on the phase difference between the two input signals when the loop is locked. When the frequency of one of the inputs changes there is a corresponding change in the phase angle. This causes a correction in the frequency of the VCO so that the two frequencies remain equal as long as they are within the hold-in range of the loop. Therefore, it becomes possible to determine the frequency of the input signal by counting the frequency of the VCO. This is the basis of the frequency measurement system.

If the transfer function of the loop filter is properly adjusted, the system can be made to act as a sample and hold circuit. When this is done, the frequency of the VCO will remain at its value at the sample time until the next sample is taken. If the sampling is done at the proper time, the frequency of the input signal can be measured by merely counting the frequency of the VCO.

There are two possible methods of accomplishing the sampling. Fig. 8a is a block diagram of a system which switches the transmitter output into the phase detector only during the back-porch interval. Fig. 8b is a block diagram of a system which samples the output of the phase detector during the back-porch interval. Either of the systems should perform the required operation, but the system shown in Fig. 8b has been chosen for the following reason. In Fig. 8a the use of the RF switch causes the input to the phase detector to be a pulse train such as that shown in Fig. 4. The frequency spectrum of this waveform is shown in Fig. 9. It can be seen that there are many discrete frequencies in this spectrum and that they appear at intervals which are multiples of the switching rate $f_h$. This means that there are frequencies located at $(f_s \pm nf_h)$ Hz. The system cannot distinguish between these frequencies and it is, therefore, possible for it to lock up on a sideband instead of the carrier. If this happened, there would be an error in the frequency measurement. This error would be a multiple of 15,750 Hz, the horizontal rate. In view of the accuracy requirements on the transmitter, this could be a significant error.

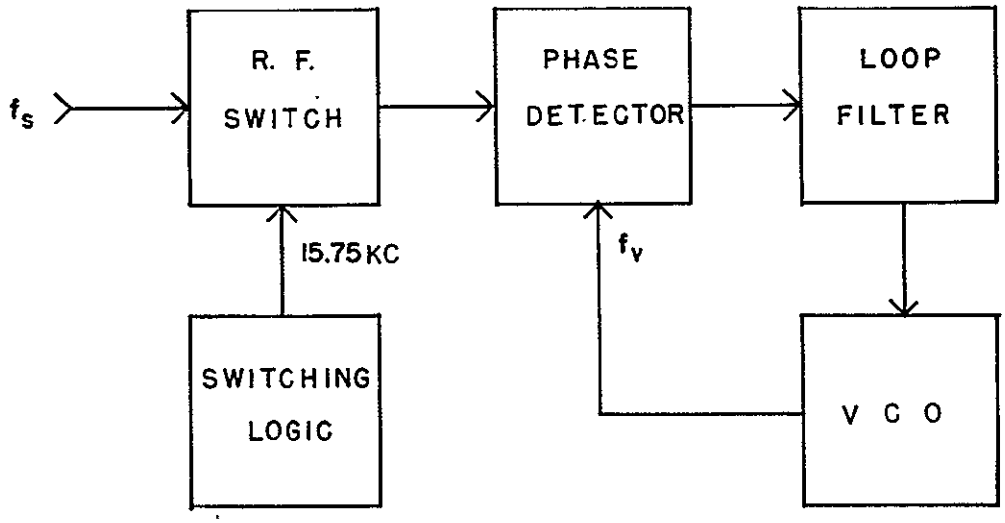


Fig. 8a. Block diagram of a system for sampling at the input to the phase detector.

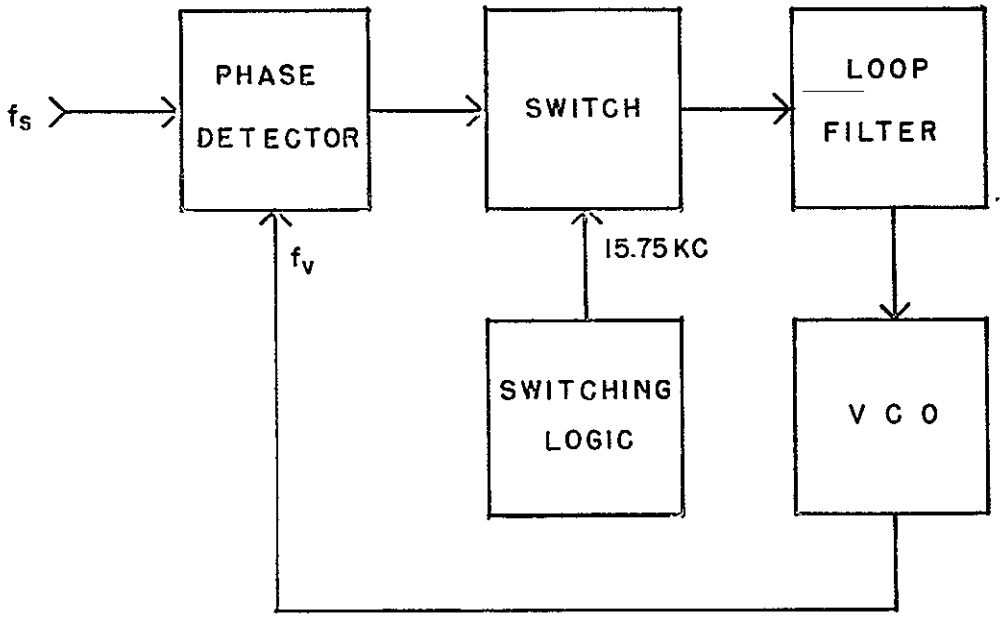


Fig. 8b. Block diagram of a system for sampling at the output of the phase detector.

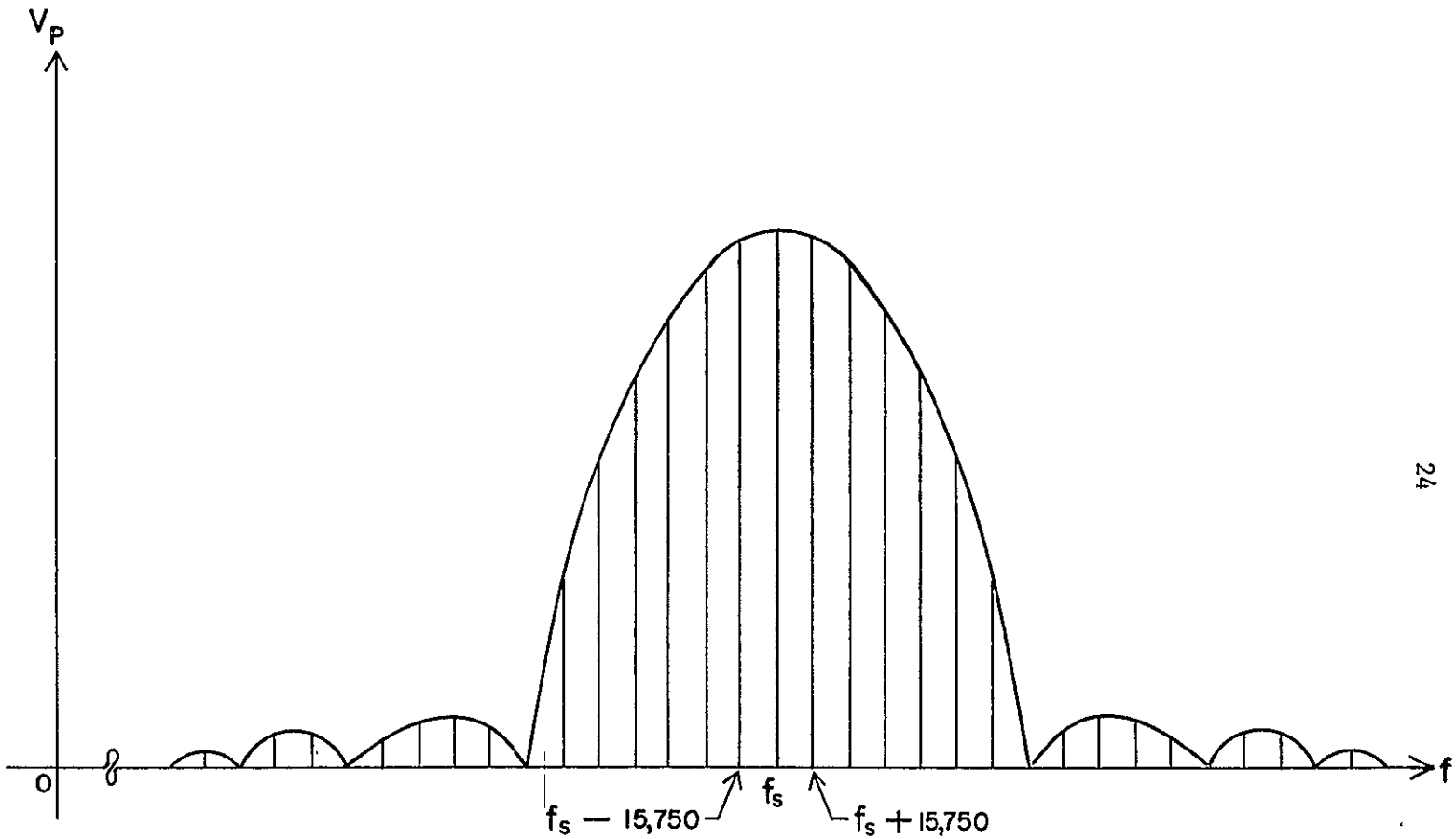




Fig. 9. Spectrum generated by the sampling technique of Fig. 8a.

In the system of Fig. 8b, the transmitter's output signal is applied to the input of the phase detector during the entire horizontal interval. Thus no new RF spectral components are generated by the sampling technique. Since the transmitter's VCO is being held close to the frequency of the crystal reference oscillator during the sample time, there is no deviation of the transmitter's VCO and therefore, there are no sidebands present to cause an erroneous lock condition. The switch used in this system can be an inexpensive solid-state device. These devices are reliable and readily available. The output from the switch will, of course, have a sinx/x spectrum, but this will be centered around zero frequency rather than around $f_s$. The loop filter will not allow any of the spectral components other than the DC value to pass. This means that the sampling can cause no problems such as those mentioned earlier. The system can perform all the tasks necessary for the loop to operate, in conjunction with a standard frequency counter, as a complete frequency measurement system. The design details of the system are discussed in the next chapter.

# III. DESIGN OF THE SYSTEM

In the design of the measurement system, the most important things to be considered are the frequency at which the loop is to operate and the variation that can be expected in the frequency of the input signal. The first is a function of the transmitter's center frequency, but it is limited by practical considerations such as limitations on the operating frequency of the phase detector and the difficulties involved in obtaining frequency stability with a high-frequency VCO. The frequency variation of the input signal from the transmitter determines the hold-in range necessary for the loop to operate properly. Some other considerations are the type of switching logic to be used, the type of device to be used for the switch, whether to use an active or a passive loop filter, the need for an amplifier in the loop, and the type of phase detector to be used.

## A. Operating Frequency of the Loop

A portion of the output of the first RF amplifier of the transmitter is applied to the SAFC system through a microdot cable. The signal at this point is approximately 225 MHz, which is much more convenient to measure than the S-band output. A coaxial tee can be inserted into the line so that part of the signal can be used as the input to the frequency measurement system. This doesn't require any permanent modification of the transmitter and the tee is easily removed when testing of the transmitter is completed.

Most phaselock loops are designed to operate in the 1-MHz to 25-MHz frequency range, but it is possible to design loops that operate up to 60 or 70 MHz. This means that the frequency of the 225-MHz signal from the transmitter is too high to be used directly as the input to the phase detector. There are good mixers commercially available in the 200-MHz frequency range, so that a heterodyne technique can be used to down-convert the transmitter signal to a frequency that can be effectively used in the phaselock loop. The problem of local oscillator frequency stability must still be solved if unnecessary measurement errors are to be avoided.

When the loop is locked, the frequency of the input signal and that of the VCO are equal. If some multiple of the VCO frequency is used as the LO for the mixer, the problem of local oscillator drift is avoided. The frequency of the VCO is given by

$$f_v = f_s - Nf_v, \tag{3-1}$$

where N is the multiplication factor.

The frequency of the input signal is given by

$$f_s = (N+1)f_v. \tag{3-2}$$

The selection of the multiplication factor is fairly arbitrary but it should be low number for two reasons. The first reason is that it is difficult to obtain a high order frequency multiplication in a one stage multiplier and it is undesirable to have more stages than are necessary in any type of electronic system. The second reason is that the number of undesired signals increases as the multiplication factor

is increased. These signals are difficult to get rid of without the use of complicated filtering. If they are not filtered out, they combine with the input signal in the mixer to produce signals that could cause problems in the phase detector. For these reasons, N was chosen to be three. It is now possible to determine the frequency of the VCO by use of Equation (3-2). The frequency of the transmitter during the back porch is actually 224.48 MHz. The required VCO frequency is

$$f_s = (N+1)f_v \tag{3-2}$$

$$f_v = \frac{224.48}{4} \text{ MHz}$$

$$f_v = 56.12 \text{ MHz}.$$

This is a good operating point for the phase detector and it is also a frequency at which the design of the VCO is not difficult.

Once the operating frequency of the loop has been determined, it is convenient to determine the tracking range required and the overall loop bandwidth. The tracking range of the measurement system is a function of the frequency stability of the transmitter. The transmitter specifications require that its frequency be within ±0.01% of the design frequency under all specified environmental conditions. Since the measurement system is required to track any frequency drift that occurs during the back-porch interval, it is necessary to determine the amount of drift, $\Delta f$, that can be expected. Assuming the value of

$\pm$ 0.01 %, $\Delta f$ is calculated below.

$$\Delta f = \pm(1.0X10^{-4})f_{bp}$$

$$= \pm(1.0X10^{-4})(2.2448X10^{8})$$

$$= \pm2.2448X10^{4}$$

$$\Delta f = \pm22.448 \text{ kHz} \tag{3-3}$$

The hold-in range required by this frequency variation can now be found.

$$\Delta\omega_H = \pm2\pi\Delta f$$

$$\Delta\omega_H = \pm2\pi(2.2448X10^{4})$$

$$\Delta\omega_H = \pm1.41X10^{5} \text{ rad/sec.} \tag{3-4}$$

From Equation (2-29), the loop gain constant required for a given hold-in range is

$$\Delta\omega_H = \pm K_1; \tag{2-29}$$

therefore

$$K_1 = 1.41X10^{5} \text{ rad/sec.}$$

This is the value of gain at which the loop would lose lock if the frequencies of the input signal and the VCO were separated by ±22.448 kHz. This is the absolute limit of proper operation of the loop and if the drift should be more than the specified amount it would not be

possible to obtain data on the excess drift. For this reason, the loop is designed to track a frequency variation of ±200 kHz. Equation (2-28) gives the deviation of the VCO as a function of $K_1$ and $\phi$, the phase difference between the input signals to the phase detector. Because $\phi$ is small when the signals are in phaselock, $\sin\phi$ has been replaced by $\phi$. For convenience, equation (2-28) is presented here as equation (3-5).

$$\Delta\omega = K_1\phi. \tag{3-5}$$

Through use of Equation (3-5), it is possible to obtain the value of gain necessary for the loop to track the input signal with some given amount of phase error. If the phase error is set at 0.1 rad. then the gain required to track the input signal over a ±200 kHz range can be found from Equation (3-5).

$$K_1 = \frac{\Delta\omega}{\phi}$$

$$= \frac{2\pi(2.0\text{X}10^5)}{0.1} \tag{3-6}$$

$$K_1 = 1.256\text{X}10^7$$

The values of the phase detector and VCO gain constants must be determined before it can be decided if the above value of $K_1$ is realistic.

In most phaselock loop applications the bandwidth of the loop is

made very narrow in order to reduce the noise power at the input to the VCO, but in this measurement system noise is not a consideration. This means that the choice of loop bandwidth can be made on the basis of such things as spectral component removal and acquisition time. As was mentioned in Chapter II, the sampling produces a sinx/x frequency spectrum in which spectral lines appear at multiples of the sampling rate, in addition to the desired low-frequency component produced by the phase detector. If these components are allowed to pass through the filter to the VCO input, they can cause the measured frequency to be in error. Since the lowest frequency produced by the sampling is 15,750 Hz, the loop bandwidth should be somewhat less than 15,750 Hz. The bandwidth of the loop is selected to be 5.0 kHz. Before any other calculations involving the entire loop are made, it is necessary to examine some of the loop components.

B. Voltage Controlled Oscillator

There are a number of configurations that can be used for the VCO and there is really not much reason, other than designer preference, to select one over the others. The configuration chosen for the measurement system VCO is a modification of a Colpitts oscillator. The VCO is shown in schematic diagram form in Fig. 10. Once an operating point is selected from the transistor's characteristics, all that is required is to design the tuned circuit. The output power of the VCO is set at a fairly low level, about 5 mw, to improve the frequency stability of the oscillator.

The value of $K_v$ can be obtained by measuring the change in frequency of the VCO when the bias on the varactor is changed by one

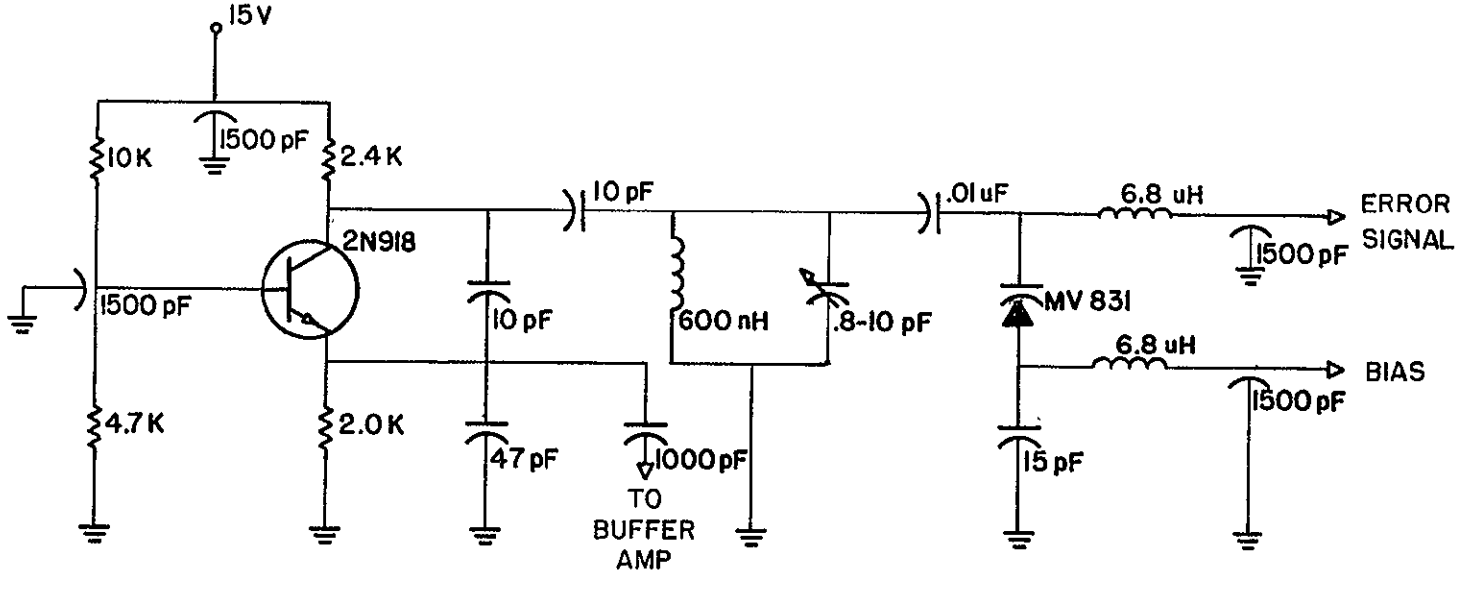


Fig. 10. Schematic diagram of the voltage controlled oscillator.

volt. The value of $K_v$ for the VCO used in the frequency measurement system is 125.5 kHz/volt.

C. Buffer Amplifier

The VCO is followed by a buffer amplifier in order to prevent loading effects from causing unwanted frequency changes. The buffer amplifier is a class-A amplifier with a fairly low power gain. The gain of the buffer is approximately 7 dB. A portion of the output of the buffer is applied to the phase detector and to a frequency counter, and the remainder of the buffer's output is applied to the input of the X3 frequency multiplier. Fig. 11 is a schematic diagram of the buffer amplifier.

D. X3 Frequency Multiplier

The X3 frequency multiplier is a class C amplifier whose output circuit is tuned to the third harmonic of the input signal. The output frequency is, therefore, 168.36 MHz. In order to maintain a high loaded Q in the output circuit of the multiplier, the inductance used in the tuned circuit should be kept as small as possible. The inductor used was approximately 20 nH.

As was mentioned earlier, it is desirable to remove all unwanted signals at the input to the mixer. To help remove these signals, the multiplier is followed by an amplifier which has a double-tuned output circuit. The amplifier provides some power gain at the desired frequency and it also provides attenuation at the frequencies of the unwanted signals. A schematic diagram of the X3 frequency multiplier and the amplifier is shown in Fig. 12.

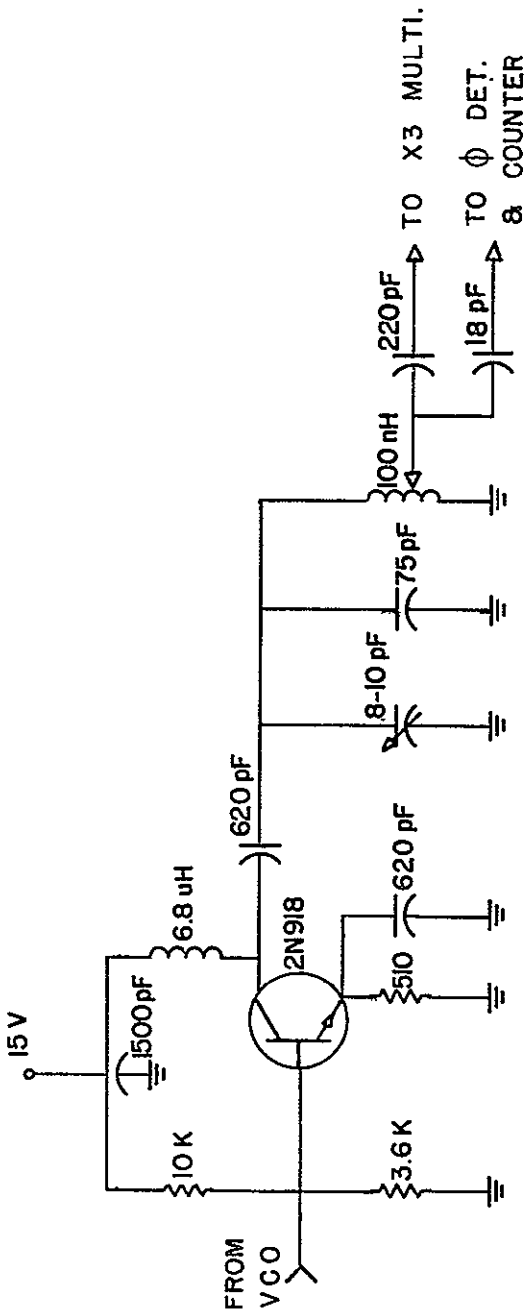


Fig. 11. Schematic diagram of the buffer amplifier.

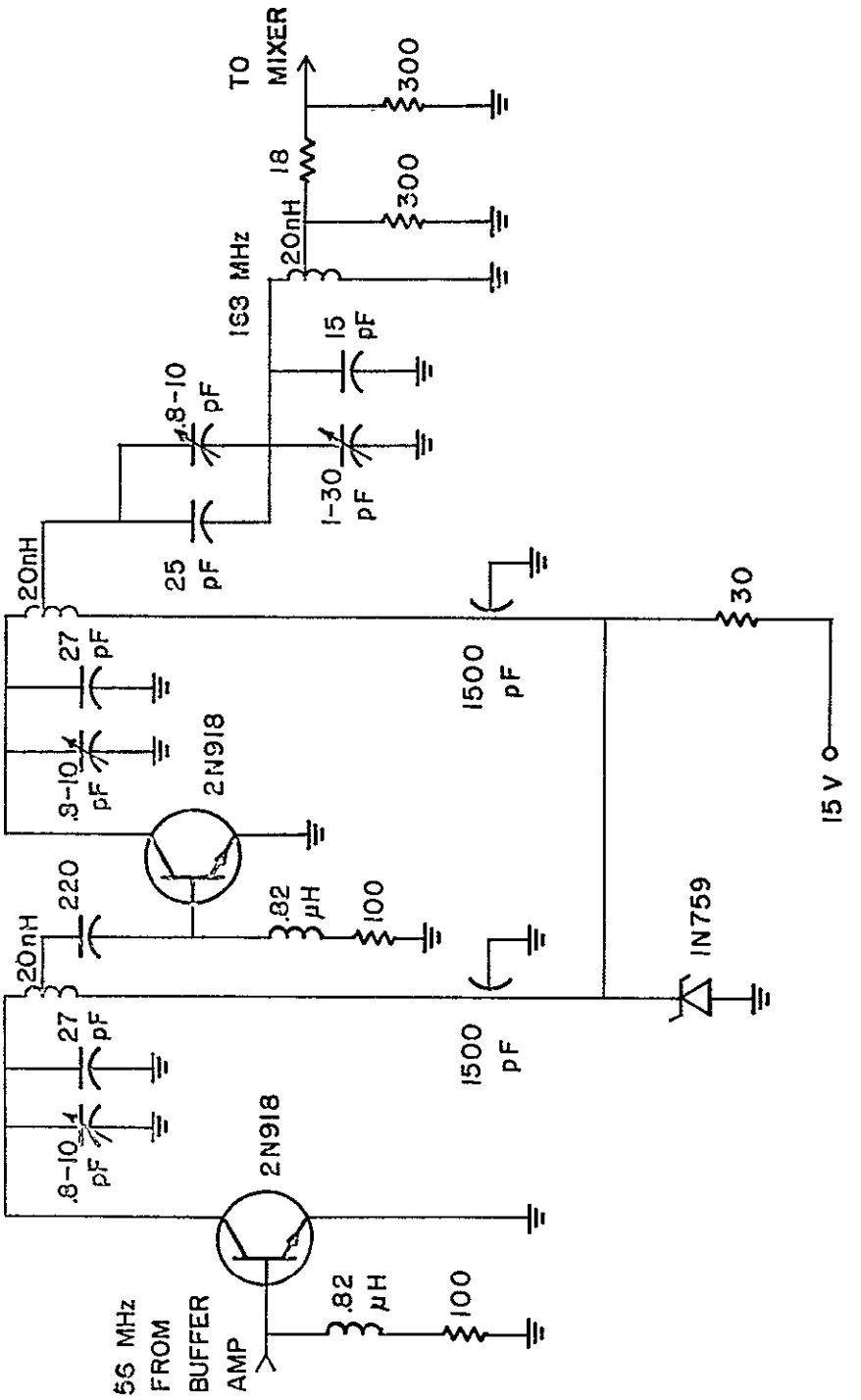


Fig. 12. Schematic diagram of the X3 multiplier and 168-MHz amplifier.

E. Mixer

The mixer used in the measurement system is a Relcom M6E mixer. This mixer is a diode-bridge balanced mixer, which has excellent conversion characteristics. It provides a conversion efficiency of approximately -6.5 dB at the frequencies of interest and it presents an attractive alternative to the design of the mixer for the system. A 3 dB resistive attenuator is provided at the LO input to the mixer, to assure that the input power is at an acceptable level.

F. IF Amplifier

An IF amplifier is provided at the output of the mixer to provide some gain at the intermediate frequency, and to provide rejection of the undesired mixer products. The amplifier is a class A amplifier, with both the input and output tuned to the 56.12 MHz intermediate frequency. A schematic diagram of the IF amplifier and the mixer is shown in Fig. 13.

G. Phase Detector

It is difficult to design a good phase detector at frequencies much above 25 MHz and for this reason phaselock loops are seldom designed to operate above this frequency. The main problems are the sensitivity of the diodes used and the design of the transformer needed for coupling the input signals into the actual detector circuit. During the preliminary research of the measurement system, it was found that the manufacturers of the M6E Relcom mixer discussed earlier, recommended the unit as a possible phase detector. A curve, found on the data sheet for the mixers, which shows the output as a function of phase difference between the input signals is shown in Fig. 14. This is a

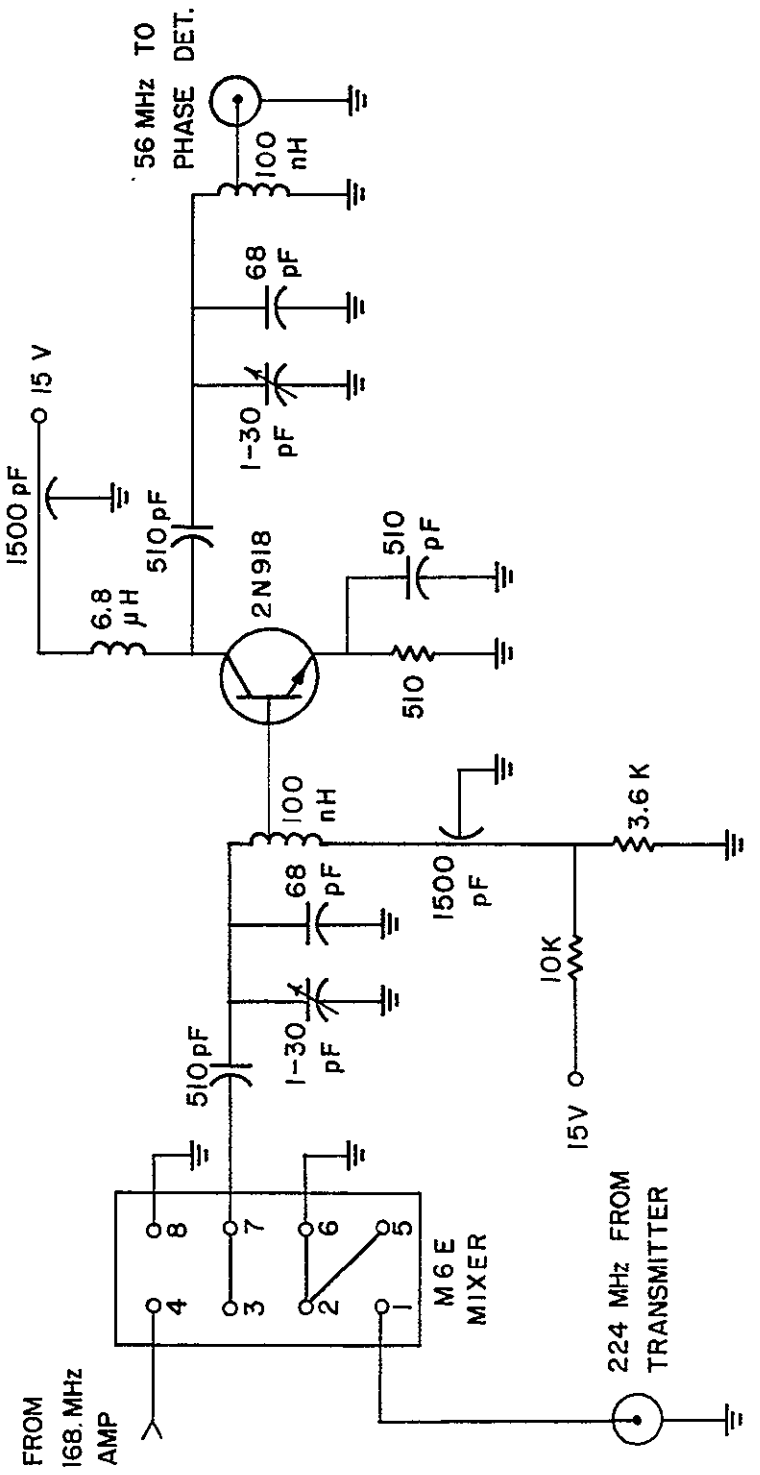


Fig. 13. Schematic diagram of the IF amplifier and the mixer.

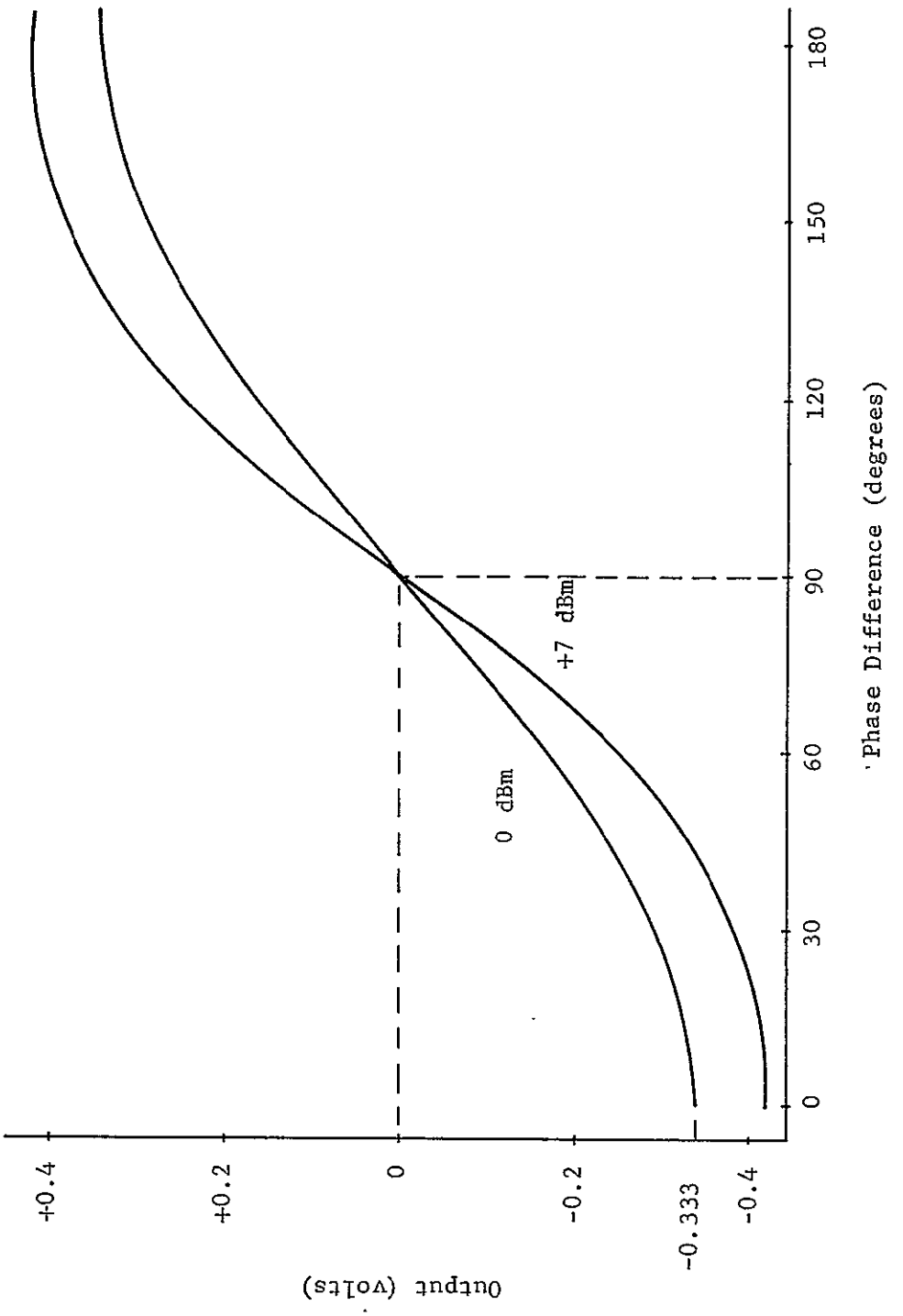


Fig. 14. Phase detector output voltage versus phase difference between the input signals.

general curve, which will vary somewhat at different input frequencies and power levels, but it provides an insight into the mixer's performance when used as a phase detector. Fig. 15 is a schematic diagram of the M6E mixer connected for use as a phase detector. It can be seen that the mixer is essentially the same as the ring modulator discussed in Chapter II. The output of the phase detector is zero when the phase difference between the input signals is 90 degrees. This is accounted for in the equations by considering one of the inputs to be a sine wave and the other to be a cosine wave. The phase detector output can be seen to be more of a sinusoidal function when the power levels of the input signals are high. This means that if linear operation is desired the input levels should be kept fairly low, approximately 1 mw. In the case of the frequency measurement system, this is not a strict requirement and there was no effort made to restrict the inputs to this level.

The value of $K_d$ can be estimated by considering the 0 dBm curve of Fig. 14 to be a linear function of $\phi$.

$$K_d = (V \text{ volts}/1.571 \text{ rad.})$$

$$K_d = 0.333/1.571 \text{ volts/rad.}$$

$$K_d = .212 \text{ volts/rad.} \qquad (3\text{-}7)$$

II. Sampling Circuit

The sampling circuit can be broken down into two parts, the sampling switch and the control circuitry. The design of the control

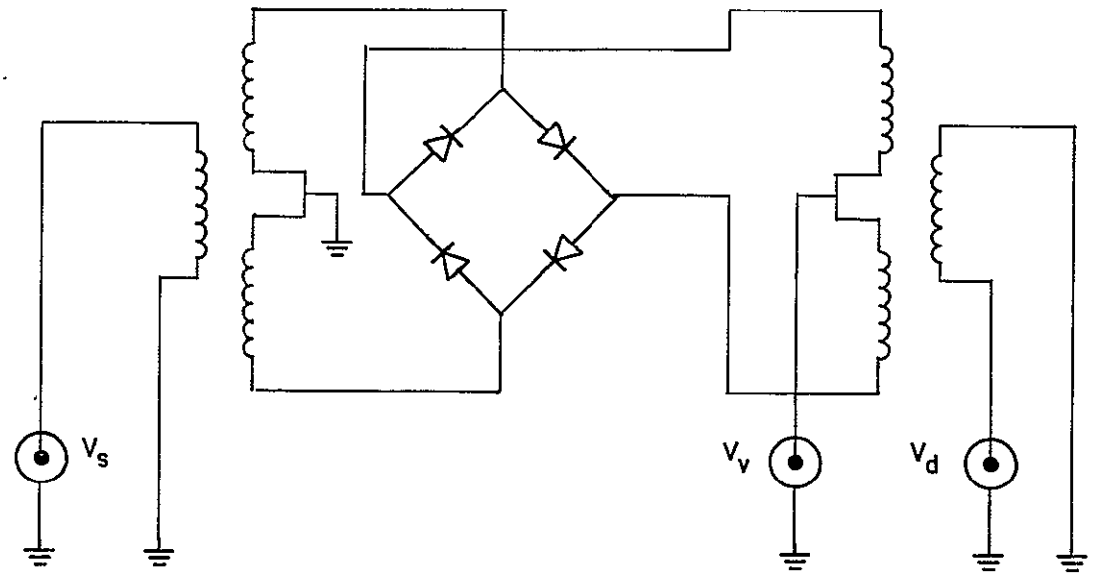


Fig. 15. Schematic diagram of the M6E mixer connected as a phase detector.

circuitry is straight-forward, but the choice of the device to be used as the switch is not so simple. There are several devices that might be used, such as relays or various solid-state devices. Most of the devices have inherent characteristics that make them unsuitable for use in the measurement system.

The device finally selected for the switch is the junction field effect transistor. The characteristics of the FET, when used as a switch, have been described by several authors. Wollesen [7], Neal [8],and Bergersen [9] are three who describe useful circuits as well as theory. The operation of the FET is such that a signal applied to the source will appear at the drain when the device is turned on by a control voltage applied to the gate. The switching time of the device is very fast, a few nanoseconds, and the only loss is a small ohmic drop. The loss is a function of the drain-to-source resistance which can be made small by proper choice of the particular FET to be used. The loss can be further reduced by using a fairly high value of load resistance. The device selected for use in the measurement system is a VCR4N, n-channel FET, manufactured by Siliconix, Inc. The drain-to-source resistance of this device is approximately 200 ohms. Since the load resistance is approximately 50,000 ohms the loss through the switch is insignificant. In addition to its low on resistance, the FET has an extremely high value of off resistance so that the output of the phase detector during the off-time of the switch does not leak through the switch. If leakage occurred, it could introduce errors into the system.

In order to insure that the sampling takes place during the back-porch interval, it is necessary to maintain precise timing between the signal in the measurement system and the TV signal. It is, therefore, necessary to find some readily identifiable characteristic of the transmitter's input or output that can be used as a time reference. The video signal that modulates the transmitter can easily be used as the time reference since it is derived from a test signal generator which is not limited in available output power. The back porch would seem to be the most obvious choice for use as the time reference, but it is not convenient to use because it represents zero signal level. The only point in the video signal that is convenient to use as a time reference is the sync pulse, but before it can be used it must be separated from the remainder of the video waveform by the sync stripper.

The sync stripper used in the measurement system is identical to the circuit used to perform the same function in the TV transmitter. The active element of the sync stripper is a SN52710 differential-voltage comparator. The input circuit is arranged so that only the negative-going portion of the video waveform is applied to the sync stripper. The only negative-going portion of a standard video signal is the sync pulse and thus the sync pulse is separated from the remainder of the video waveform. The output of the sync stripper is a positive-going pulse which occurs during the sync pulse of the video signal.

A monostable multivibrator is used to obtain a pulse that occurs during the back porch of the video signal and that is the required length. The monostable multivibrator is an SN5380 integrated circuit

which triggers when the input changes from a positive voltage to a zero voltage. Through the adjustment of two RC time constants, it is possible to vary the time delay between input and output of the multivibrator and to vary the length of the output pulse. In the case of the measurement system, it is required that the output of the multivibrator occurs during the back-porch interval and, therefore, the delay can be set at zero. In order to assure that the sampling circuit turns off before the end of the back porch, the multivibrator output pulse is made somewhat shorter than the length of the back porch. The length of the back porch is approximately 3.8 μsec. and the length of the pulse is set at 3.5 μsec. A timing diagram which shows the relationship between the sync pulse and the output of the multivibrator is shown in Fig. 16. As can be seen in Fig. 16, the multivibrator's output is 4.0 v except during the pulse interval, when it is zero. This is not compatible with the requirements of the FET switch. An n-channel FET requires a negative voltage on the gate to turn it off, and a zero or slightly positive voltage to turn it on. This means that some kind of level shifting circuit is required due to the operational characteristics of the integrated circuits used for the control circuitry. This problem is discussed in detail below along with a basic circuit arrangement.

The circuit shown in Fig. 17 can be used to shift the output of the multivibrator to the levels required by the FET. The operation of the circuit can be explained as follows: as long as the input to the circuit is positive the transistor is turned on and the output is

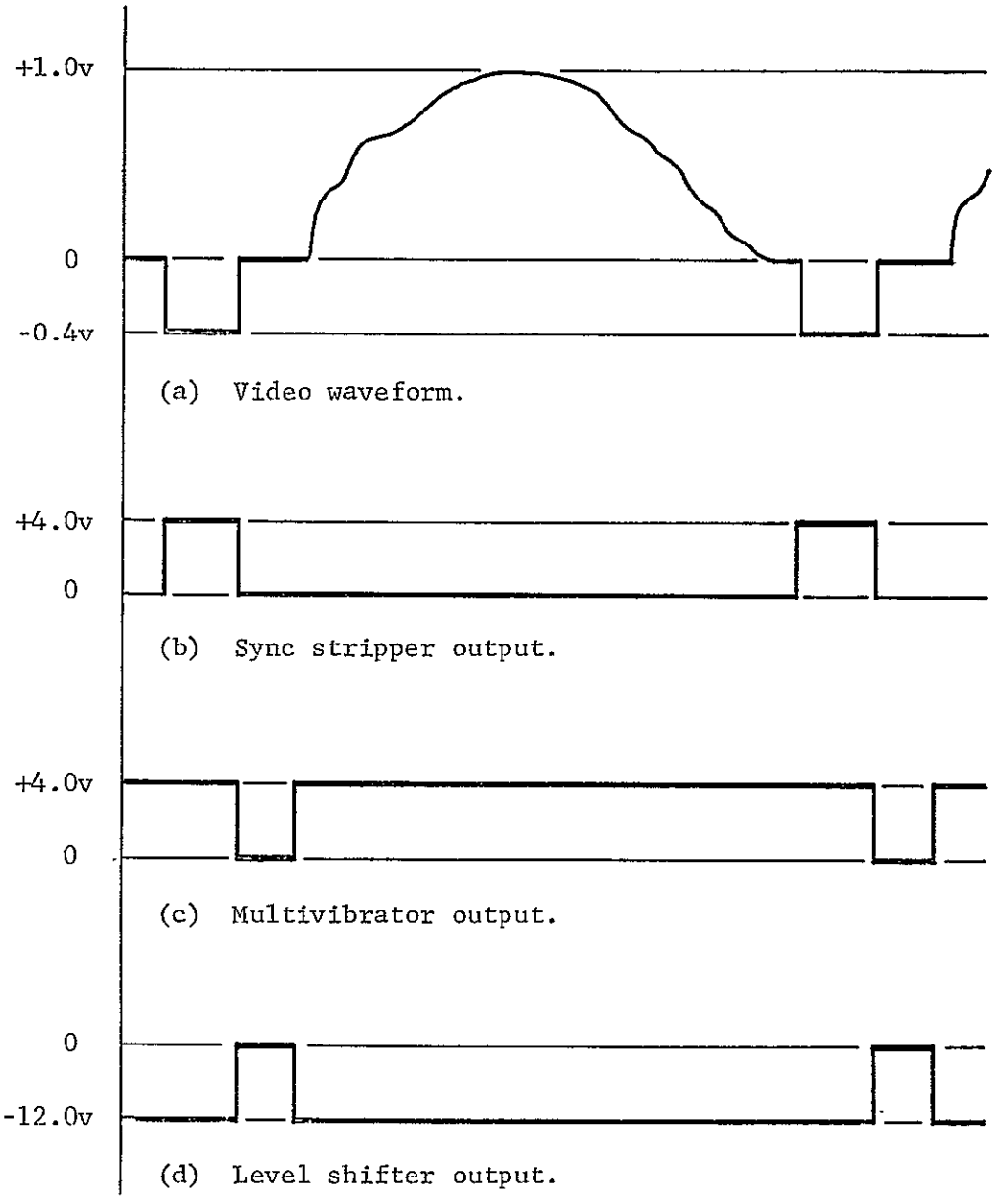


Fig. 16. Timing diagram.

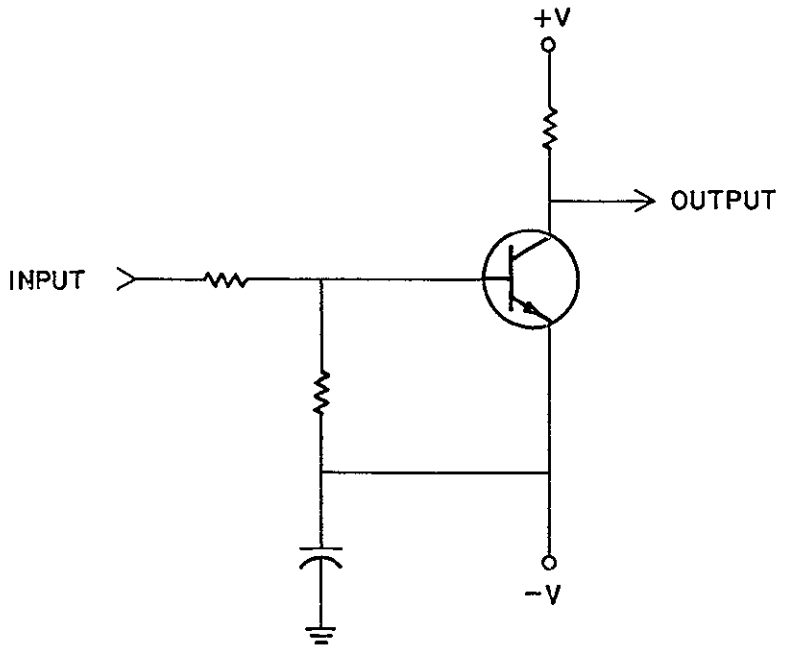


Fig. 17. Simplified schematic diagram of the level shifter.

at -V volts. When the input becomes zero the transistor is turned off and the output is at +V volts. The output of the circuit is shown in the timing diagram of Fig. 16.

A schematic diagram of the complete sampling circuit is shown in Fig. 18. The diodes between the level shifter and the FET are used to prevent the positive portion of the control signal from appearing as a signal at the drain of the FET. It was found experimentally that two diodes in series are required to perform this task properly. If only one diode was used, a slight positive voltage was found to appear at the drain when the input signal at the source was zero. The diodes are selected so that their capacitance characteristics match those of the FET. This helps to improve the switching characteristics of the FET. A more complete discussion of this phenomenon can be found in the literature [7].

I. Loop Filter

The loop filter is the component which is primarily responsible for determining the overall operating characteristics of the loop. It determines such things as the loop bandwidth, response time, tracking range, pull-in frequency, and pull-out frequency. If properly designed, along with an amplifier, it can correct for certain deficiencies in other components of the loop. These include such things as low values of $K_d$ and $K_v$. In the design of the loop filter for the measurement system it is necessary to select a filter that can be used in a sample and hold circuit. The lag filter discussed in Chapter II is essentially an integrator and thus it can be used in a sample and hold circuit. The loop bandwidth has already been chosen to be 5.0 kHz and it is now

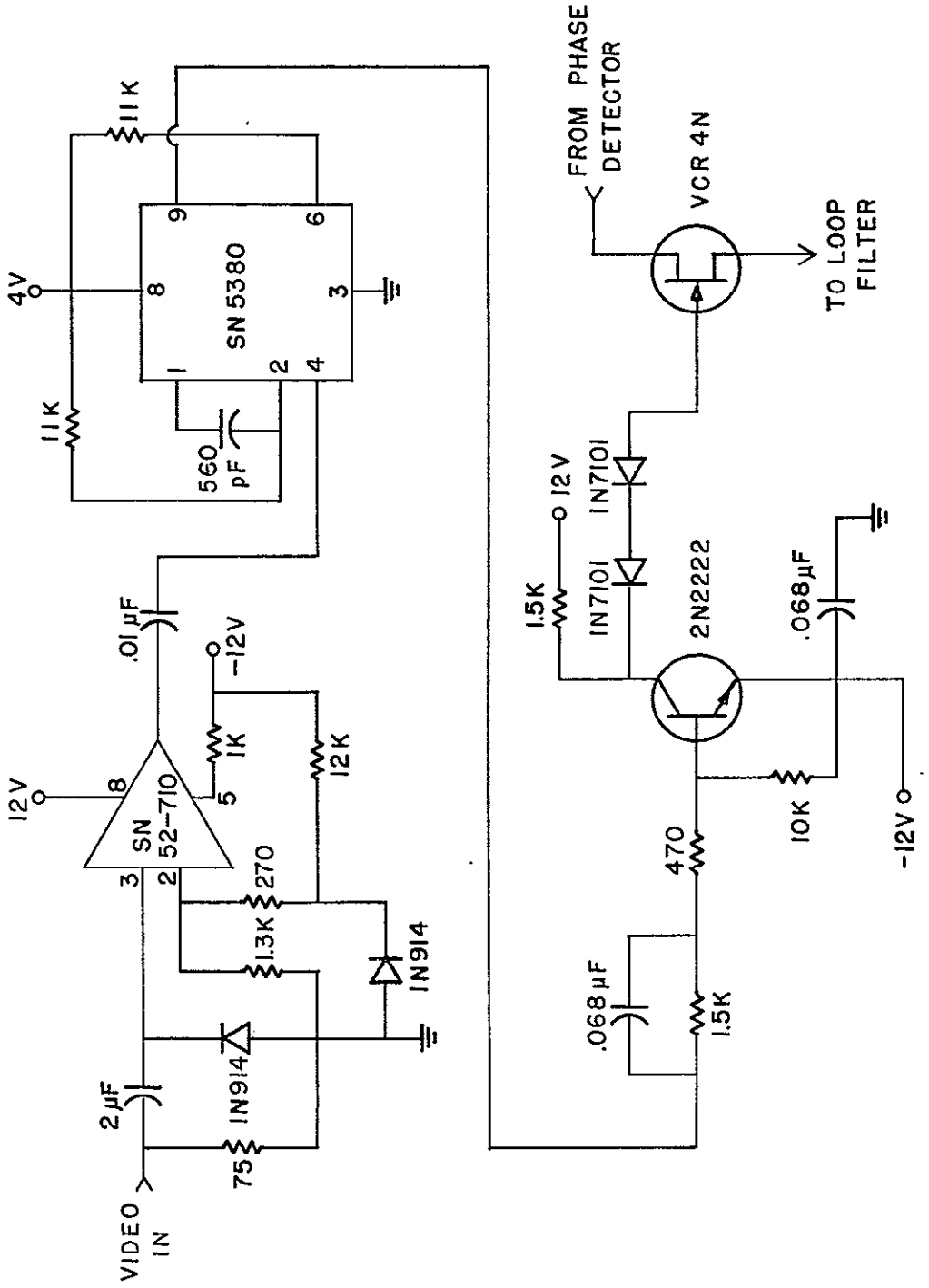


Fig. 18. Schematic diagram of the switching circuit.

possible to design the filter.

Gardner gives an equation for loop bandwidth in terms of the natural frequency and damping factor of the loop.

$$B_L = \frac{\omega_n}{2}\left[\zeta + \frac{1}{4\zeta}\right] \tag{3-8}$$

In Equation (3-8) there are two unknowns, $\omega_n$ and $\zeta$, and it is necessary to select a value of one before the equation can be solved for the other. In many control and phaselock system problems the value of $\zeta$ is chosen to be 0.707. Gardner shows curves which indicate that this will be a reasonable value for the loop damping factor.

$$B_L = \frac{\omega_n}{2}\left[.707 + \frac{1}{(4)(.707)}\right]$$

$$\omega_n = \frac{2\ B_L}{.707 + 1/(4)(.707)}$$

$$\omega_n = \frac{1X10^4}{1.061}$$

$$\omega_n = 9.43X10^3 \text{ rad/sec.}$$

The two time constant, $\tau_1$ and $\tau_2$, of the filter can now be found. $\tau_1$ is given by

$$\tau_1 = \frac{K_1}{\omega_n^2} \tag{3-9}$$

and $\tau_2$ is given by

$$\tau_2 = \frac{2\zeta}{\omega_n} . \qquad (3\text{-}10)$$

Then,

$$\tau_1 = \frac{K_1}{\omega_n^2}$$

$$= \frac{1.256\text{X}10^7}{(9.43\text{X}10^3)^2}$$

$$= \frac{1.256\text{X}10^7}{8.9\text{X}10^7}$$

$$\tau_1 = .141 \text{ sec.}$$

and

$$\tau_2 = \frac{2\zeta}{\omega_n}$$

$$\tau_2 = \frac{2(.707)}{9.43\text{X}10^3}$$

$$= \frac{1.414}{9.43\text{X}10^3}$$

$$\tau_2 = 1.5\text{X}10^{-4} \text{ sec.}$$

Since $\tau_1 = R_1C$ and $\tau_2 = R_2C$ it is necessary to select a value for one of the variables so that the other two can be calculated. Selecting C to be 3.3 μF,

$$\tau_1 = R_1C$$

$$R_1 = \frac{1.41X10^{-1}}{3.3X10^{-6}}$$

$$R_1 = 4.27X10^4 \text{ ohms},$$

and

$$\tau_2 = R_2C$$

$$R_2 = \frac{1.5X10^{-4}}{3.3X10^{-6}}$$

$$R_2 = 4.55X10 \text{ ohms}.$$

A value of 43 kΩ is used for $R_1$ and value of 45Ω is used for $R_2$. The loop filter is shown schematically in Fig. 19.

J. Loop Gain Constant

It is now possible to calculate the value of $K_1$, using the loop parameters that have been measured or calculated. $K_1$ is given by Equation (2-27) as

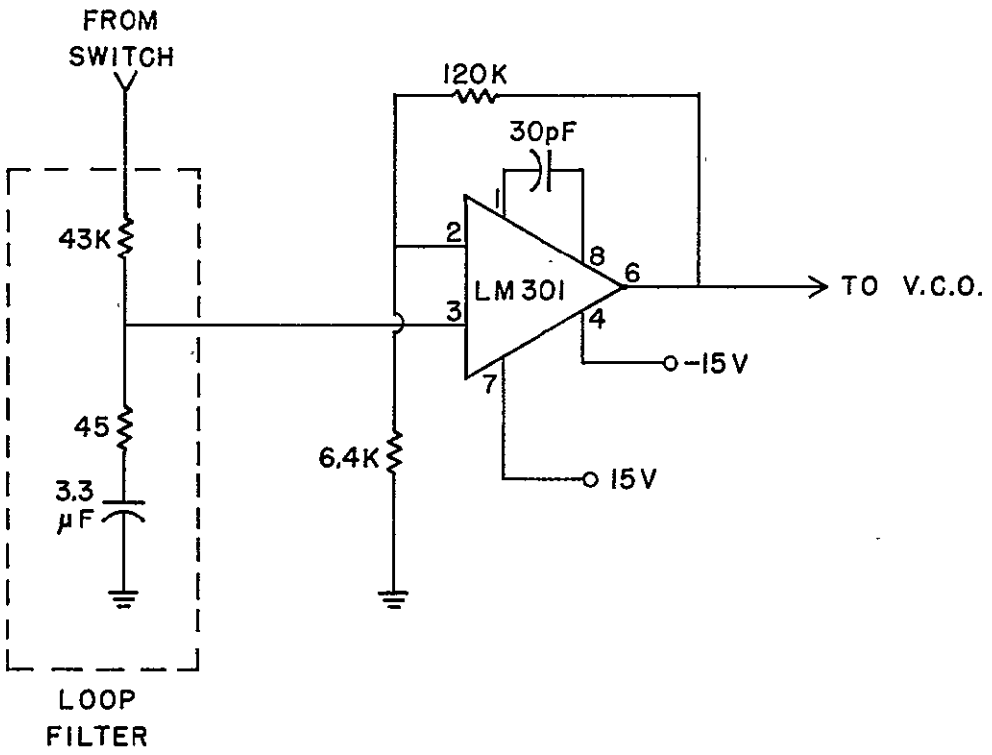


Fig. 19. Schematic diagram of the loop filter and DC amplifier.

$$K_1 = K_v K_d F(0).$$

F(0) is the steady-state DC gain of the loop filter and for the type of filter used, the steady-state DC gain is equal to one. $K_v$ has been measured to be $7.881X10^5$ rad/sec-volt and $K_d$ was found to be 0.212 volt/rad. $K_1$ is then,

$$K_1 = (7.881X10^5)(2.12X10^{-1})(1)$$

$$K_1 = 1.671X10^5 \text{ 1/sec.}$$

The desired value of $K_1$ was found to be $1.256X10^7$ 1/sec. It is obvious that some adjustment must be made if the measurement system is to perform satisfactorily. Is it possible to make the necessary adjustment without redesign of the phase detector and the VCO? Fortunately, the adjustment is quite easy to make.

The deviation of a VCO is increased if there is frequency multiplication at the output of the VCO. The new deviation is $N\Delta F$ where N is the multiplication factor and $\Delta f$ is the original frequency deviation. The output frequency of the VCO is effectively multiplied by a factor of 4 in the measurement system as can be seen from examination of Equation (3-2). With this multiplication, the loop gain constant can now be represented as

$$K_1 = NK_v K_d F(0)$$

$$= (4)(1.671X10^5)$$

2

$$K_1 = 6.684X10^5 \text{ 1/sec.} \tag{3-11}$$

This value is still too low for the measurement system to operate as desired, but there is another adjustment that can be made.

The phase detector gain constant $K_d$ is effectively increased by using a DC amplifier at the output of the phase detector, thus increasing $K_d$ by the gain factor, A, of the amplifier. If the amplifier is placed after the loop filter, it can be used to compensate for any loss that occurs in the filter. If a high gain operational amplifier is used, it will tend to reduce errors that can be caused by loading effects of the filter since the operational amplifier has an extremely high input impedance (several megohms). The required gain of the loop DC amplifier can be calculated from the following equation.

$$K_1 = ANK_vK_dF(0) \tag{3-12}$$

$$A = \frac{K_1}{NK_vK_dF(0)}$$

$$A = \frac{1.256X10^7}{(4)(7.881X10^5)(2.12X10^{-1}}$$

$$A = 18.8 \tag{3-13}$$

A schematic diagram of the amplifier used in the measurement system is shown in Fig. 19. The active device in the amplifier is an LM301

integrated circuit operational amplifier. The design of the circuit is straight-forward once the active device is selected. Care must be taken to assure that the input voltage is not sufficient to saturate the amplifier since this can cause lock-up problems and measurement errors. The gain of the amplifier is given by

$$A = \frac{R_f}{R_i} \tag{3-14}$$

$R_i$ is selected to be 6.2 kΩ and A has been calculated as 18.8, then

$$R_f = AR_i$$

$$= (18.8)(6.2X10^3)$$

$$R_f = 1.167X10^5$$

$$R_f = 116.7\ k\Omega . \tag{3-15}$$

A value of 120 kΩ is used for $R_f$.

K. The Complete System

The design of the frequency measurement system is now complete. A block diagram which shows the interconnection of all the system components is shown in Fig. 20. When the system is used to measure the frequency of a television transmitter it may be necessary, at times, to manually lock the loop by adjusting the bias on the VCO's varactor diode. Provision has been made for this by using a

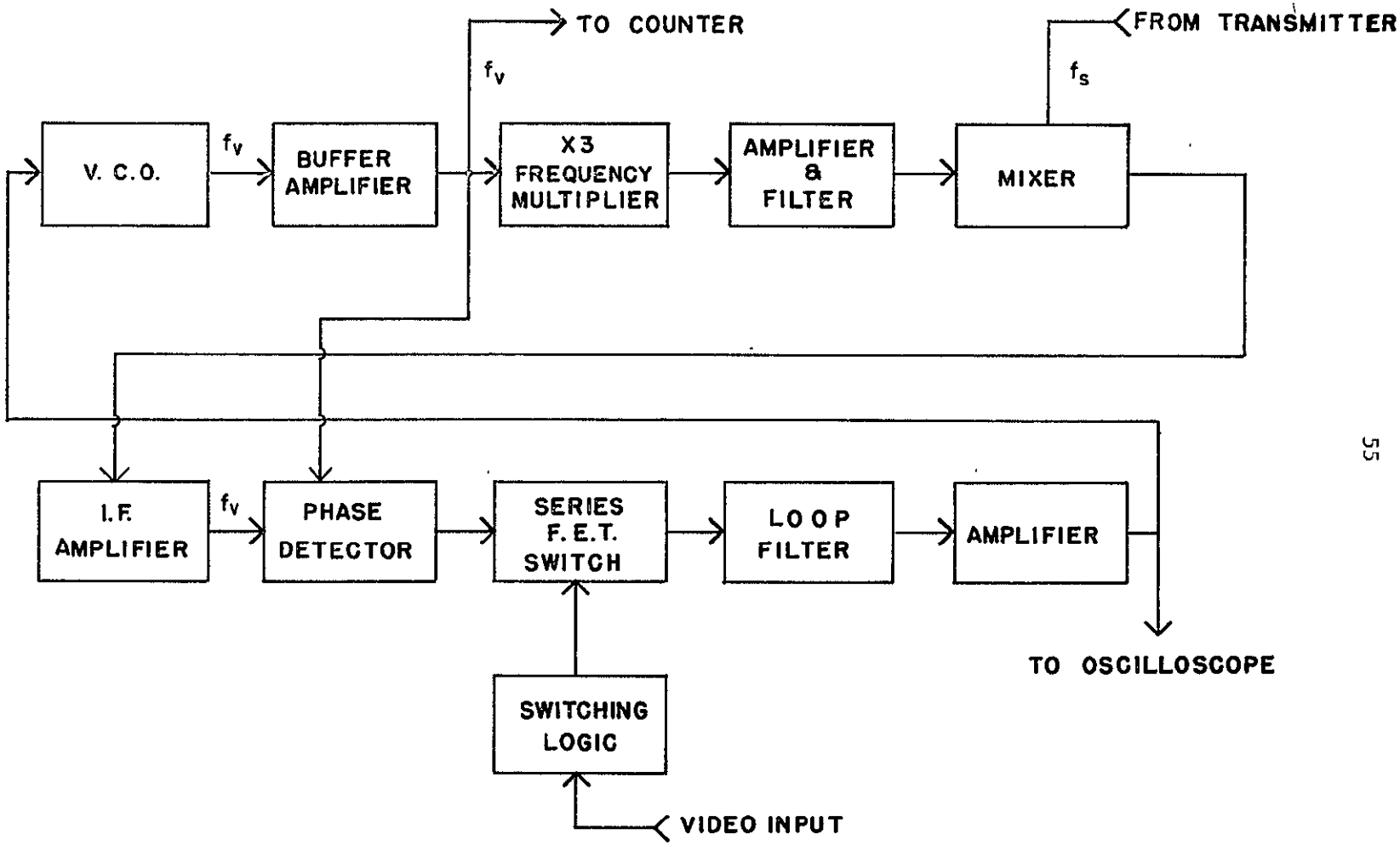


Fig. 20. System block diagram.

potentiometer in the varactor bias circuit. Although it is possible to design a circuit to indicate a locked condition, this was not done. An oscilloscope can be used to determine if lock has occurred, if it is connected to the phase detector output. The loop is locked if the output is a DC signal. If the output is an AC signal the varactor bias should be adjusted in a direction that reduces the frequency of the phase detector's output signal. This will eventually result in a locked condition.

L. Calculated System Parameters

At this time some of the system parameters mentioned earlier will be calculated so that they may be compared to the measured values presented in the next chapter. The hold-in range is given by Equation (2-29) as

$$\Delta\omega_H = \pm K_1. \qquad (2\text{-}29)$$

Substituting in the calculated value of $K_1$ gives

$$\Delta\omega_H = 1.256X10^7 \text{ rad/sec.}$$

The maximum rate of change of input frequency that the system can follow is given by Equation (2-31) as

$$\frac{d\Delta\omega}{dt} = \omega_n^2 \qquad (2\text{-}31)$$

$$= (9.43X10^3)^2$$

$$\frac{d\Delta\omega}{dt} = 8.9X10^7 \text{ rad}^2/\text{sec}^2$$

The pull-out frequency of the loop is a measure of the loop's response to a frequency step. Below the pull-out frequency the loop remains in lock but above the pull-out frequency the loop will lose lock, at least temporarily. The pull-out frequency is given by Equation (2-30) as

$$\Delta\omega_{po} = 1.8\omega_n(\zeta+1) \qquad (2\text{-}30)$$

$$= (1.8)(9.43X10^3)(1.707)$$

$$\Delta\omega_{po} = 2.8X10^4 \text{ rad/sec.}$$

The lock-in frequency is a measure of the maximum difference permissible between the input signals if the loop is to lock immediately. By Equation (2-32) the lock-in frequency is,

$$\Delta\omega_L = 2\zeta\omega_n; \qquad (2\text{-}32)$$

therefore,

$$\Delta\omega_L = 2(.707)(9.43X10^3)$$

$$\Delta\omega_L = 1.33X10^4 \text{ rad/sec.}$$

The last system parameter of interest is the pull-in frequency. This is the maximum frequency separation allowable between the VCO and the input signal if the loop is to eventually lock. The pull-in frequency is given by Equation (2-34) as

$$\Delta\omega_p = 2\sqrt{\zeta\omega_n K_1} \quad . \tag{2-34}$$

Substituting in the required values,

$$\Delta\omega_p = 2\sqrt{(.707)(9.43X10^3)(1.256X10^7}$$

$$\Delta\omega_p = 5.78X10^5 \text{ rad/sec.}$$

This concludes the design of the system. The remaining chapter presents the measured data and makes comparisons between the calculated and measured data.

# IV. MEASURED DATA AND CONCLUSIONS

The measurement system was constructed using the circuits discussed in Chapter III. Initial testing of the system was done using a Hewlett-Packard Model 608 signal generator as the source for $f_s$. This was done so that the actual frequency of the source could be measured using a standard counter. The test set-up is shown in Fig. 21.

The pulse generator is used to provide a trigger signal for the switching circuitry. The oscilloscope is used as a lock indicator. The two counters measure the frequencies of the VCO and of the signal generator.

The first parameter measured was the hold-in range, $\Delta\omega_H$. This test was performed by first increasing the frequency of the generator until the loop lost lock and then decreasing the frequency until lock was again lost. The frequencies at which lock is lost are the limits of the hold-in range. The frequency limits measured are given below:

$$f_{H+} = 226.979 \text{ MHz}$$

$$f_{H-} = 221.013 \text{ MHz}.$$

The center frequency of the generator was 224.480 MHz. The frequency differences are then given by

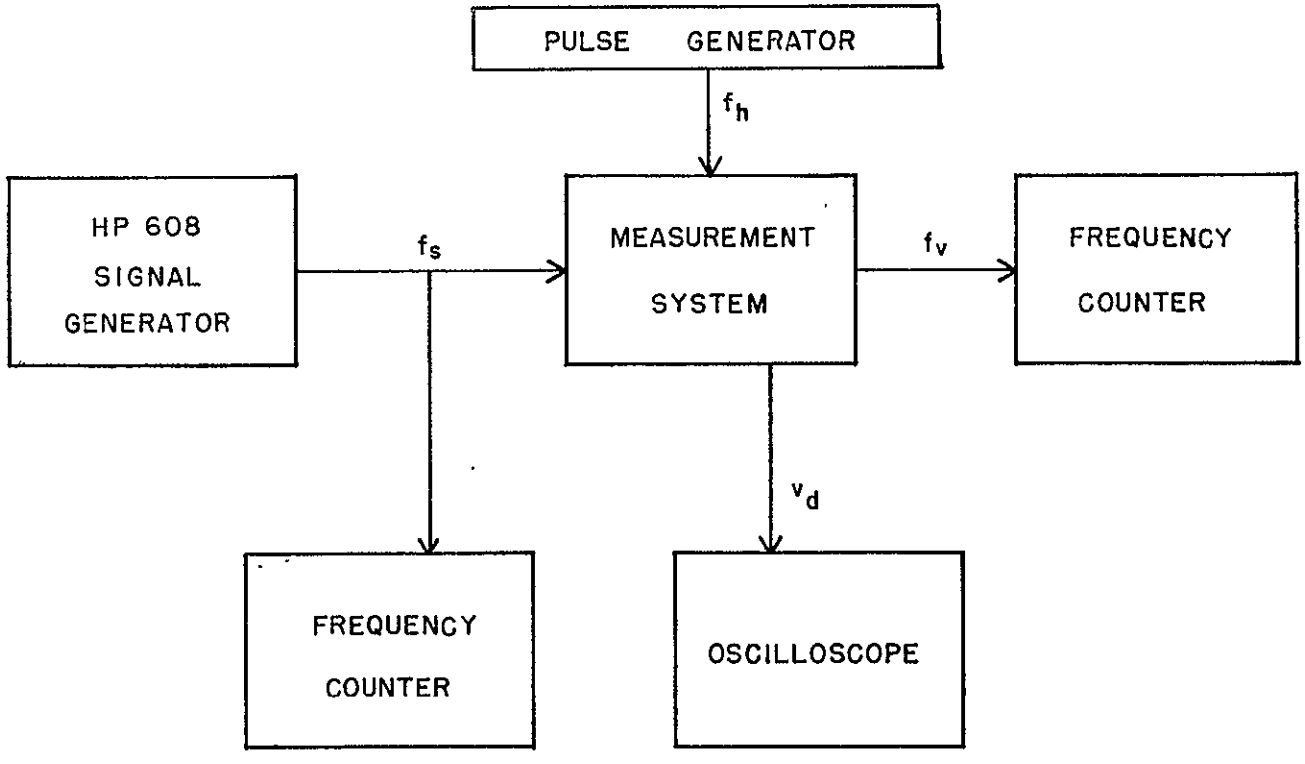


Fig. 21. Block diagram of the measurement system test set-up.

$$\Delta f_{H+} = f_{H+} - f_s$$

$$\Delta f_{H+} = 2.499 \text{ MHz}$$

and

$$\Delta f_{H-} = f_s - f_{H-}$$

$$\Delta f_{H-} = 3.467 \text{ MHz}.$$

The hold-in limits are given in terms of radian frequency by

$$\Delta\omega_{H+} = 2\pi\Delta f_{H+}$$

$$\Delta\omega_{H+} = 1.57 \times 10^7 \text{ rad/sec}$$

and

$$\Delta\omega_{H-} = 2\pi\Delta f_{H-}$$

$$\Delta\omega_{H-} = 2.18 \times 10^7 \text{ rad/sec}.$$

The hold-in range is seen to be wider in the low-frequency direction than in the high-frequency direction. This is accounted for by the fact that the sensitivity of the VCO is greater in the low-frequency direction. This is inherent in the capacitance vs. voltage characteristics of the varactor diode and it is not possible to correct this over a wide frequency range.

The measured value of the hold-in range is seen to be larger than the calculated value. This is accounted for, in part, by the gain of

the amplifier being somewhat higher than the value used in the calculations. The measured value of $K_v$ is also a source of error which could account for some of the difference in the measured and calculated values of $\Delta\omega_H$.

The second parameter of interest is the lock-in range, $\Delta\omega_L$. It was found during testing of the system that it is not practical to measure the lock-in range. Problems arose in trying to set the signal generator frequency so that the difference between the VCO frequency and the frequency of the IF amplifier output signal was within the required ±13 kHz. It is believed that the lock-in range is at least as wide as the calculated value and it appears to be somewhat wider.

In measuring the pull-in range, the beat frequency signal out of the phase detector was used as an indication of the frequency difference between the two phase detector input signals. The loop was first unlocked and then the frequency of the signal generator was adjusted until the beat frequency was close to the calculated value of $\Delta\omega_p$. The frequency of the generator was then adjusted in small increments until the loop pulled into lock. The pull-in range measured in this way was approximately ±60 kHz. This is about 30% less than the calculated pull-in range, but the measured value and the calculated value are not really the same parameter. The calculated value of $\Delta\omega_p$ is the difference frequency at which the loop will eventually pull into lock. This process might take a considerable time. The measured value is the frequency difference at which the

loop will rapidly pull into lock and so it would be expected to be somewhat less than the calculated value.

Another important system variable which was not mentioned before is the power of the input signal. The response of the system to various levels of input power was checked by locking the loop and then reducing the input power until the loop lost lock. It was found that the loop lost lock when the input power to the system reached -26 dBm. The power was then increased until the loop regained lock which occured at an input power level of from -18 dBm to -16 dBm.

The input power was also found to have an effect on the pull-in range of the loop. Varying the input power caused the loop to pull into lock when the frequency difference between the two inputs was greater than the 60 kHz obtained in the measurement of $\Delta\omega_p$. It is believed that this is due primarily to changes in the phase detector output voltage which cause the VCO to begin to change frequency. This has the same effect on the loop as does manually changing the frequency of the signal generator.

A. System Test with the Transmitter

The system test with the transmitter was divided into two phases. The system was first tested with no modulation on the transmitter. This was done by using a pulse generator to simulate the sync pulse input to both the transmitter and the measurement system. The frequency of the VCO, when the loop was locked, was found to be 55.4975 MHz. The modulation on the transmitter's VCO was then shorted to ground and the frequency of the transmitter's VCO was measured and found to be 221.990 MHz. The actual frequency measured by the system can be found from Equation (3-2) as

$$f_s = 4f_v$$

$$f_s = 221.990 \text{ MHz.}$$

Some error was found in the last three digits of the measured frequency, i.e., the digits corresponding to less than 1 kHz variation. This error is due to the response time of the loop and to the fact that the sample and hold circuit is not perfect. An error of 1.0 kHz in the measurement represents a percent frequency error of less than 0.0005% which is insignificant. The frequency of the transmitter was varied from 220 MHz to 229 MHz with results comparable to those above.

In the second phase of system testing, a video test signal (a stair-step) was used to modulate the transmitter. Part of the video signal was applied to the measurement system to provide a trigger for the switching circuitry. The measurement system locked up with no problem and appeared to track the transmitter in the desired manner.

The output of the switch was monitored with an oscilloscope for the lock indication in this phase of the testing. This was done because the output of the phase detector is a beat frequency which is dependent on the deviation of the transmitter except during the back porch interval. It was found to be difficult to separate this beat note from that caused by a normal unlock condition.

It might be useful to remove the vertical blanking on the video signal during testing. The blanking occurs at a 60-Hz rate and causes sidebands

to be present which could cause a false lock condition. This should not cause much measurement error because of the closeness of the sidebands to the carrier, but the possibility of erroneous measurements should be avoided where possible.

The overall performance of the measurement system is well within the requirements discussed in Chapters I and II. It is believed that the system will be very helpful in the testing of any future television transmitters. It is also believed that the system can be used, with slight modifications, in the testing of other types of transmitters where the modulation prevents the use of standard frequency measurement techniques. Radar or PCM transmitters are examples of transmitters where the system could be applied.

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