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WASHINGTON, D.C. 20546

REPLY TO ATTN OF: GP

11-24-70

TO: USI/Scientific & Technical Information Division
Attention: Miss Winnie M. Morgan

FROM: GP/Office of Assistant General Counsel for Patent Matters

SUBJECT: Announcement of NASA-Owned U. S. Patents in STAR

In accordance with the procedures agreed upon by Code GP and Code USI, the attached NASA-owned U. S. Patent is being forwarded for abstracting and announcement in NASA STAR.

The following information is provided:

U. S. Patent No. : 3,533,098

Government or Corporate Employee : U.S. Government

Supplementary Corporate Source (if applicable) : NA

NASA Patent Case No. : XAC-04031

NOTE - If this patent covers an invention made by a corporate employee of a NASA Contractor, the following is applicable:

Yes ☐ No ☒

Pursuant to Section 305(a) of the National Aeronautics and Space Act, the name of the Administrator of NASA appears on the first page of the patent; however, the name of the actual inventor (author) appears at the heading of Column No. 1 of the Specification, following the words ". . . with respect to an invention of . . ."

Elizabeth A. Carter

Enclosure
Copy of Patent cited above

N71-18594

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(PAGES)	(CODE)
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Oct. 6, 1970 R. M. MUNOZ 3,533,098

NONLINEAR ANALOG-TO-DIGITAL CONVERTER

Filed March 25, 1966 2 Sheets-Sheet 1

N71-18594 40%

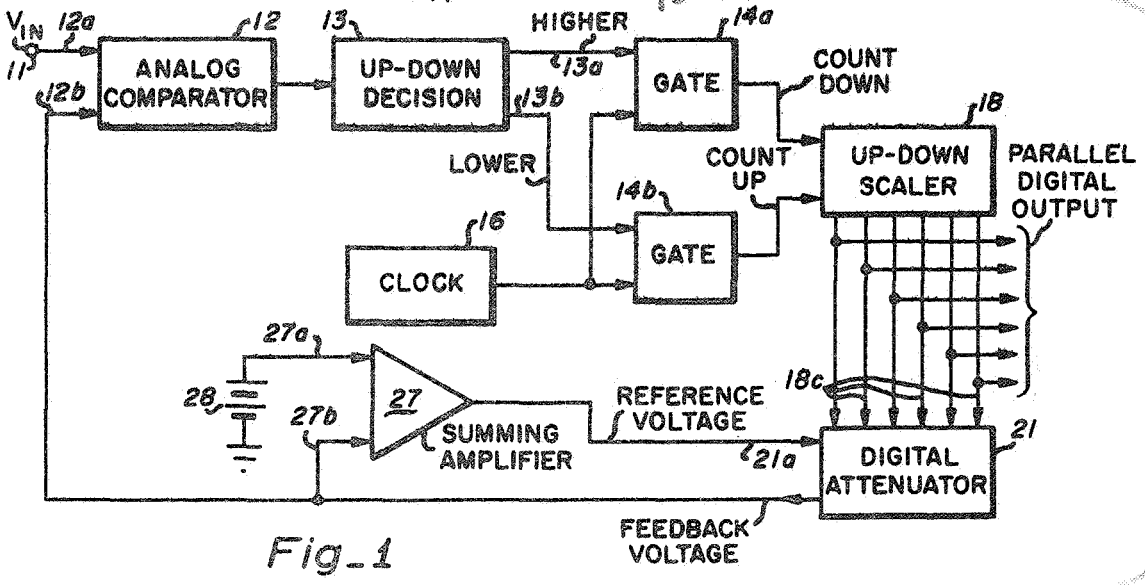

Fig_1

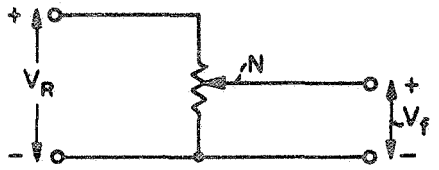

Fig_2

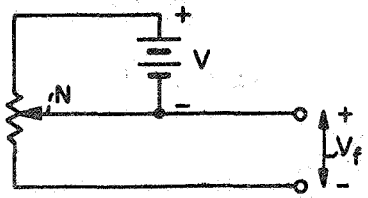

Fig_3

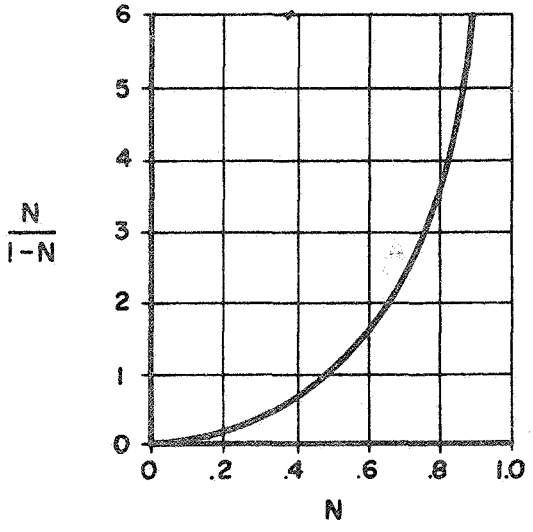

Fig_4

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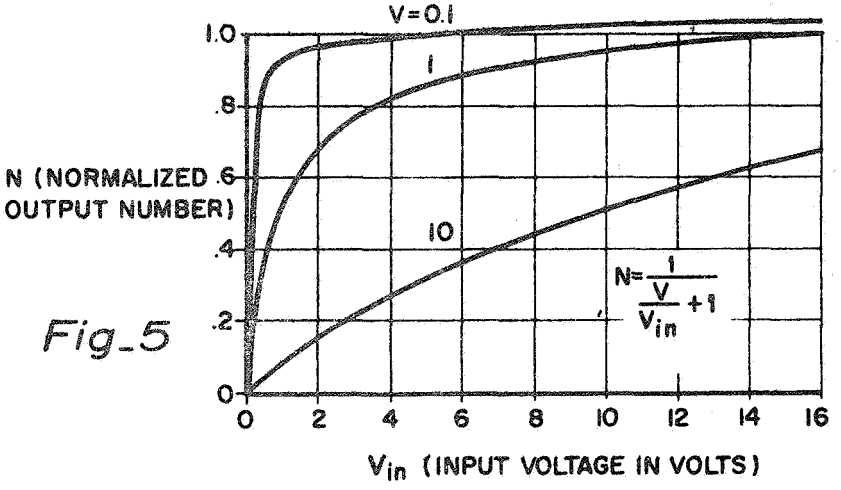

Fig_5

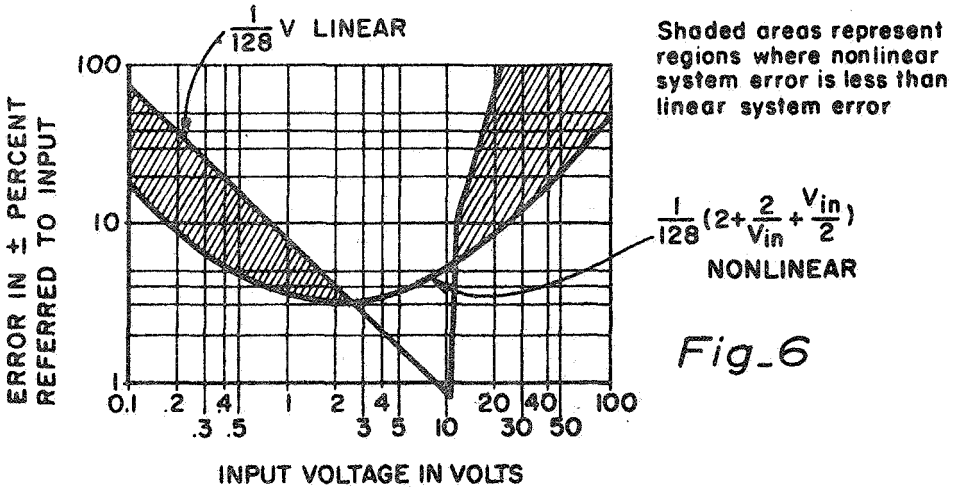

Fig_6

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United States Patent Office

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Patented Oct. 6, 1970

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NONLINEAR ANALOG-TO-DIGITAL CONVERTER

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Filed Mar. 25, 1966, Ser. No. 538,905
Int. Cl. H03k 13/04
U.S. Cl. 340—347 4 Claims

ABSTRACT OF THE DISCLOSURE

A continuous analog-to-digital converter with a parallel digital output that is characterized by improved accuracy, especially in the low end of the scale. Error is reduced by introducing a very accurate nonlinearity in the feedback path. Instead of a linear feedback factor, the feedback voltage is varied in accordance with the function $N/1-N$, wherein N is the ratio of the digital output number to the number that represents full scale. Only two components are needed to produce the nonlinearity.

The invention described herein was made by an employee of the United States Government and may be manufactured and used by or for the Government for governmental purposes without the payment of any royalties thereon or therefor.

This invention relates in general to analog-to-digital converters, and relates more particularly to such converters having nonlinear response characteristics.

In all analog-to-digital converters (hereinafter referred to as ADC), regardless of type, one of the continuing problems is that of error. This error arises as a result of the inability of the ADC to measure input signal levels smaller than the least significant digit in the digital numbering system employed. As an example of this type of error, consider and ADC employing a 6-bit binary code, with a resulting overall accuracy of one bit or one part in 64. This produces an error of 1.6%, or ±0.8%. If the full scale input voltage for such a digital system is 10 volts, this represents a possible error of ± 80 millivolts. However, where the input voltage is a small fraction of full scale, say 1 volt, the total possible error is still ±8% of the reading. Thus, unless it can be guaranteed that the input signal levels will be a substantial part of full scale most of the time, such an ADC will present serious accuracy problems.

In order to provide a system in which the accuracy, expressed as a function of operating level, remains more nearly constant, the present invention provides scale compression in a nonlinear ADC system by introducing a very accurate nonlinearity in the feedback path of a feedback-type ADC. This feedback path includes a conventional digital attenuator, which is employed to convert the digital output signal from the ADC to a corresponding analog signal which is fed back for comparison with the analog input signal to be converted. In the preferred form of this invention, the desired nonlinearity is introduced directly into the digital attenuator circuitry, so that the feedback voltage is modified by the nonlinearity introduced. Thus, the feedback voltage varies nonlinearly with the digital output of the ADC to produce a nonlinear response characteristic for the system. This nonlinear response characteristic produces a scale compression which results in improved error characteristics for the system, since the system error, expressed in percentage of reading, is more linearly constant than with a system having a linear response.

As an additional feature of this invention, the desired nonlinearity is introduced by components which are capable of high accuracy and which are extremely stable with respect to temperature and time. A further feature of the invention is that the desired nonlinearity may be produced by adding only a single component to a conventional feedback-type ADC.

It is therefore an object of this invention to provide an improved analog-to-digital converter having a nonlinear response characteristic.

It is a further object of this invention to provide an analog-to-digital converter of the feedback type in which a very accurate nonlinearity is introduced into the feedback path to produce a nonlinear response for the system.

It is an additional object of this invention to provide an analog-to-digital converter of the feedback type employing a digital attenuator in the feedback path, in which a very accurate nonlinearity is introduced into the digital attenuator circuitry to produce a nonlinear response for the system.

It is a further object of this invention to provide an analog-to-digital converter of the feedback type in which a very accurate nonlinearity is introduced into the feedback path to produce a nonlinear response for the system, the component which produces the nonlinearity being extremely stable with respect to time and temperature.

It is an additional object of the present invention to provide an analog-to-digital converter of the feedback type employing a digital attenuator in the feedback path, in which a very accurate nonlinearity is introduced into the feedback path to provide a nonlinearity response for the system, the nonlinearity being produced by the introduction of only a single component into a conventional feedback-type analog-to-digital converter.

Objects and advantages other than those set forth above will be apparent from the following description when read in connection with the accompanying drawings, in which:

FIG. 1 is a schematic showing, in block diagram form, of one embodiment of the present invention employing a summing amplifier to introduce a nonlinearity into a feedback-type ADC;

FIG. 2 is a functional diagram of the digital attenuator of a linear ADC system of the prior art;

FIG. 3 is a functional diagram of a digital attenuator in accordance with this invention employing a battery to introduce the desired nonlinearity;

FIG. 4 is a graph illustrating the effect of variations in the normalized output number N, of an ADC system on the nonlinear quantity $N/1-N$;

FIG. 5 is a graph illustrating variations of the normalized output number, N, with changes in the analog input signal for different values of the voltage of the battery of FIG. 3; and

FIG. 6 is a graph showing the relative error characteristics of an ADC in accordance with this invention and a linear ADC of the prior art.

Referring to the drawings, FIG. 1 schematically shows, in block diagram form, one embodiment of the invention for converting an analog input signal appearing at an input terminal 11 into a corresponding digital signal. The analog input signal is supplied as one input on a conductor 12*a* to an analog comparator 12 which also receives an analog feedback signal on an input conductor 12*b*. The analog input signal is compared in amplitude in comparator 12 with the feedback voltage appearing on conductor 12*b*, and the output of this comparison is supplied as the input to a device 13 labelled "up-down decision." In the embodiment illustrated in FIG. 1, it is assumed that the ADC described employs an up-down scaler or counter to provide a digital measure of the amplitude of the analog input signal, in a manner well known in the art. In this situation, device 13 determines whether feedback signal is higher or lower than the analog input signal, and provides an output on either a line 13*a* labelled "higher" or a line 13*b* labelled "lower." These output lines are supplied as inputs to associated gates 14*a*, 14*b*, which each also receive a common input from a source of clock pulses 16.

If the feedback signal exceeds the amplitude of the analog input signal, "higher" line 13*a* is energized from element 13 to supply an input to gate 14*a*. This effectively opens gate 14*a* to pass the clock pulses from source 16 to the "count down" input line of an "up-down" scaler 18. As is well known in the art, scaler 18 operates to produce on its plurality of output lines 18*c* a digital measure of the analog input signal, and the digital number produced by scaler 18 may be increased or decreased by energization of the "count up" or "count down" input line.

Thus, where the feedback signal exceeds the amplitude of the input signal, energization of the "count down" line as described above causes scaler 18 to count downwardly from whatever digital number was present therein. Similarly, when the feedback signal is less than the input signal, output line 13*b* of element 13 is energized to open gate 14*b* to pass clock pulses to scaler 18 which operate to increase the count upwardly from whatever digital number is present therein.

The signals on output lines 18*c*, which form a parallel digital representation of the analog input signal, may be supplied to any suitable utilization or storage device as indicated, such as magnetic tape units, etc. These signals are also supplied as inputs to a digital attenuator 21 which functions to convert these digital signals into an analog signal by comparison with a suitable reference voltage supplied on a conductor 21*a*. The analog signal produced by attenuator 21 forms the feedback voltage which is supplied on conductor 12*b* to comparator 12 for comparison with the analog input signal. Attenuator 21 may be of any suitable type which operates as described. In general, such attenuators receive inputs corresponding to either binary ones or zeros from the output lines of scaler 18, and these inputs are operative to control the connection of binarily weighted resistors in the attenuator.

If the reference voltage supplied to attenuator 21 on conductor 21*a* were constant, the circuit of FIG. 1 would operate in a manner well known in the art to convert the analog input signal on conductor 12*a* to a digital representation on conductors 18*c* of scaler 18. This operation would be as follows: Assuming that scaler 18 has been reset to zero, the presence on conductor 12*a* of a signal to be converted produces an output from comparator 12 indicating that the input signal exceeds the feedback signal since there would be no feedback signal with scaler 18 set at zero. This output from comparator 12 causes element 13 to energize gate 14*b* to pass clock pulses to scaler 18 in a direction to increase the count in the scaler.

Scaler 18 thus counts upwardly, producing a corresponding digital output on conductors 18*c* as it does so.

This output on conductors 18*c* is supplied to attenuator 21 to produce an analog feedback signal which increases linearly as the count in scaler 18 increases. The feedback voltage thus increases until it matches the amplitude of the analog input signal, at which time comparator 12 indicates no difference between the compared signals and the supply of clock pulses to scaler 18 is halted. Assuming the analog input remains at this value, the count in scaler 18 stops and the digital number represented on output conductors 18*c* corresponds to the amplitude of the analog input signal.

The above description of the prior art devices and circuits indicates their linear operation, and it will be clear that such operation presents serious problems of accuracy for input signals which are only a fraction of full scale.

In accordance with the present invention, instead of utilizing a linearly operating attenuator to produce a feedback signal which varies linearly with the digital output, the present invention modifies the operation of the attenuator to produce a nonlinear operation which results in improved accuracy. This operation may be understood by reference to FIGS. 2 and 3, which represent functional diagrams of a linear digital attenuator of the prior art and a nonlinear digital attenuator in accordance with the present invention, respectively. In the prior art attenuator of FIG. 2, the feedback voltage V_f is proportional to the product of the reference voltage V_R and the normalized digital output, N, where N is the ratio of the digital output number of the ADC to the number which represents full scale. Thus, with V_R constant, this relationship is a linear one, with the feedback voltage varying linearly with N.

Before discussing the functional diagram of a nonlinear attenuator in accordance with the present invention, the following considerations may be reviewed. In all simple feedback systems, including the feedback ADC systems under discussion here, the following relationship is true

$$\frac{\text{output}}{\text{input}}=\frac{A}{1+A\beta} \tag{1}$$

where A is the forward transfer from input to output (in the present case, the digital output number per volt of analog input), and β, the feedback factor, is the analog voltage output from the digital attenuator per unit digital output from the ADC.

It is convenient to normalize the digital output number to unity for full scale reading, so that one value may represent the output whether the system is a 6-bit, 8-bit, or an *n*-bit system. For such a normalized output, the maximum value of β is unity.

The forward transfer A is usually large for comparators with a low threshold, and Equation 1 then simplifies to:

$$\frac{\text{output}}{\text{input}}=\frac{1}{\beta} \tag{2}$$

This equation shows that the nature of the transfer function is dependent largely on the feedback factor. In the prior art systems as discussed above, β is linear, but in the present invention, is made to vary nonlinearly over the range of operation of the ADC system.

Consider now the functional diagram of FIG. 3, showing a nonlinear digital attenuator in accordance with this invention. In FIG. 3, a battery with a voltage V is connected between output of the attenuator and the reference terminal thereof. The reference voltage V_R is now no longer constant, but is dependent upon the feedback voltage V_f, and the following relationship applies:

$$V_f=N(V_f+V) \tag{3}$$

Solving Equation 3 for V_f:

$$V_f=\frac{NV}{1-N} \tag{4}$$

The term $N/1-N$ in Equation 4 is the desired nonlinear function, and the battery voltage V is a scale factor which can be employed to adjust the range of the system. This nonlinear function is plotted in FIG. 4, which indicates that it is a monotonically increasing function which is asymptotic to the line, $N=+1$.

The transfer function through the digital attenuator is equal to the feedback factor for this system, as shown below in Equation 5.

$$\frac{V_f}{N}=\frac{V}{1-N} \tag{5}$$

Substituting into Equation 2 produces an expression for the overall transfer function of this ADC system:

$$\frac{\text{output}}{\text{input}}=\frac{N}{V_{in}}=\frac{1-N}{V} \tag{6}$$

Solving for N produces:

$$N=\frac{V_{in}}{V+V_{in}}=\frac{1}{\frac{V}{V_{in}}+1} \tag{7}$$

This function is plotted in FIG. 5, with the normalized output number N shown in relation to the voltage V_{in} for three different values of the voltage V of the battery of FIG. 3. It will be seen that this produces a scale which contains all positive values of V_{in} with a relatively constant percentage error, i.e., increasing absolute accuracy as the magnitude of reading decreases. The degree of nonlinearity is easily controlled by adjusting the value of the voltage V.

Thus, a nonlinear ADC system in accordance with the present invention may be built using a battery or other type of floating power supply associated with the digital attenuator as shown in the functional diagram of FIG. 3. As an alternative, such a nonlinear system may be built using a conventional DC summing amplifier as shown in FIG. 1. In that figure, a summing amplifier 27 supplies the reference voltage V_R to digital attenuator 21. Summing amplifier 27 receives one input on a conductor 27*a* from a constant voltage source, such as a battery 28, and receives another input on a conductor 27*b* representing the feedback voltage output from attenuator 21. Amplifier 27 sums these two voltages and supplies the sum to attenuator 21. The attenuator modifies this input voltage from amplifier 27 by N, the normalized digital output number as discussed above, to produce a feedback voltage which varies nonlinearly in a manner similar to that described above for the battery of FIG. 3.

The use of a summing amplifier as shown in FIG. 1 or a floating power supply as shown in FIG. 3 produces a very accurate nonlinearity. This is a significant factor, since any nonlinearity introduced changes the transfer function directly, and any errors in the feedback path will occur in the output without attenuation. The use of an accurate nonlinearity in accordance with the teachings of this invention is much preferable to employing an analog nonlinearity interposed between the digital attenuator and the analog comparator, because some suitable devices, such as semiconductor diodes and thermistors are temperature-sensitive, while others, such as vacuum tube devices, change their operating characteristics as a function of time and are hence not satisfactory for high accuracy system.

As a comparison of the relative error characteristics of the nonlinear ADC of this invention and a linear ADC of the prior art, consider the following. The system error expressed as a function of the reading referred to the input may be computed for the nonlinear ADC by first differentiating Equation 7 above with respect to N:

$$\frac{dV_{in}}{dN}=\frac{V_{in}}{N(1-N)} \tag{8}$$

Solving for the error referred to the input yields:

$$\frac{dV_{in}}{V_{in}}=\frac{dN}{N(1-N)} \tag{9}$$

Substituting, for N, the value obtained from Equation 7 produces:

$$\text{Error}=\frac{dV_{in}}{V_{in}}=\left(2+\frac{V_{in}}{V}+\frac{V}{V_{in}}\right)dN \tag{10}$$

where dV_{in}/V_{in} is the nonlinear ADC system error and dN is the error associated with a one-bit variation in N.

This nonlinear system error is compared graphically with the error produced in a linear ADC system in the curves of FIG. 6. In this figure, the linear system is set to a full scale of 10 volts and a 6-bit binary code is employed. Full scale error is approximately ±0.8%, but the error at 1% of full scale is greater than ±50%. For the same input voltage levels in the nonlinear ADC system of the present invention, where V is set to 2 volts, FIG. 6 shows that the error at 10 volts is approximately ±6%, and this error decreases as the input voltage falls to 2 volts. When the input voltage falls below 2 volts, the error increases slowly, but is still usable (±15%) at 0.1 volt. With inputs between 10 and 100 volts, the nonlinear ADC of this invention provides some information even though the errors are greater than ±6%, thus producing an indication of the order of magnitude of signals beyond the normal range of the system. This is a ten-to-one extension in scale length, even though the error is relatively high (up to ±50% for the worst case where the input is 100 volts) in this example.

At approximately 2.5 volts and 11 volts, FIG. 6 indicates that the errors in both systems are equal, but below 2.5 volts and above 11 volts, the nonlinear ADC is markedly superior. The shaded areas of FIG. 6 represent those regions where the nonlinear ADC system of this invention produces less error than that of the linear system. It will be understood that other error profiles for the system of this invention may be produced by variations in the voltage V, and that the particular case shown illustrates the basic nature of the improvement produced in all cases.

Thus, the present invention produces an ADC system in which the error, expressed as a percentage of reading, is more nearly constant and in which extension of scale length is possible so that certain kinds of data can be digitized with more meaning. The system is further capable of operating over large temperature ranges and long periods of time without materially affecting the system performance. Additionally, the invention has the advantage that it can be implemented with only one additional component (a floating power supply or a summing amplifier) in a conventional linear ADC.

Although specific details of the present invention are shown and described herein, it is to be understood that modifications may be made therein without departing from the spirit and scope of the invention as set forth in the appended claims.

I claim:

1. Apparatus for continuously correcting an analog input signal to a parallel digital representation comprising:

comparator means for comparing an analog input signal to an analog feedback signal and generating an output signal proportional to the difference between said signals;

a source of clock pulses;

counting means coupled to said comparator means and said clock for counting up when said analog input signal exceeds said feedback signal and counting down when said feedback signal exceeds said analog input signal, said counting means having parallel outputs on which digital signals are produced which represent the instantaneous count;

a reference voltage generator comprising a summing amplifier with first and second inputs, and a D-C voltage supply, said voltage supply being coupled to said first input, said reference voltage being generated at the output of said amplifier;

means coupled to said generator and said counting means for comparing said reference voltage and said digital output signals and generating said analog feedback signal; and

means for coupling said feedback signal to said second input of said amplifier and to said comparator means;

said feedback signal being nonlinear and causing a reduction in error over a portion of the voltage range of said apparatus.

2. Apparatus in accordance with claim 1 wherein the feedback signal varies as a function of $N/1-N$, and N is the normalized digital output representing the ratio of the digital output from said counting means to the scale capability of said counting means.

3. Apparatus for continuously converting an analog input signal to a parallel digital output comprising:

comparator means for comparing an analog input signal to a nonlinear analog feedback signal and generating an output signal representing the difference between said signals;

means for generating clock pulses;

an up-down scaler producing parallel digital output signals;

logic means coupled to said comparator means, said clock pulse means and said scaled for enabling said clock pulses to reach said scaler when said comparator means output signal has a magnitude other than zero, said scaler counting up when said analog input signal exceeds said feedback signal and said scaler

counting down when said feedback signal exceeds said analog input signal;

means coupled to said scaler for comprising said scaler digital output signals with a reference voltage and generating said nonlinear analog feedback signal;

a summing amplifier having first and second inputs, said amplifier generating a reference voltage which is coupled to said comparing means;

a D-C voltage source coupled to said first amplifier input; and

means for coupling said feedback signal from said comparing means to said second amplifier input and said comparator means.

4. Apparatus in accordance with claim 3 wherein the feedback signal varies as a function of $N/1-N$, and N is the normalized digital output representing the ratio of the digital output from said scaler to the full scale capability of said scaler.

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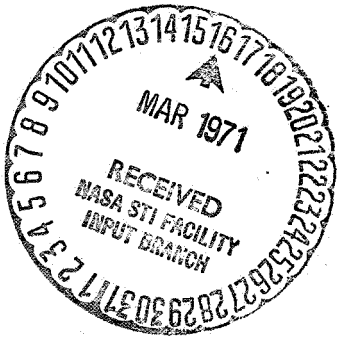
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