MCR-71-82

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LINEAR MODULATOR

TEST PROCEDURE AND REPORT

CONTRACT NAS8-25987

MARCH 1971

Prepared for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama 35812

Martin Marietta Corporation
Denver Division
P. O. Box 179
Denver, Colorado 80201

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Approved by

C. W. Pederson
Program Manager

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FOREWORD

This Test Procedure and Test Report is furnished to show compliance with Paragraph I.2 and as supporting data for the Final Report, MCR-71-81 which was furnished in response to Paragraph II.2 of Exhibit A of Contract NAS8-25987.

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1.0 Introduction

The following report gives the test procedures and results for the Modulator, Demodulator and phase locked loops breadboard. The breadboard successfully passed all tests as outlined in Sections 2.0 to 4.0 and as verified by the data sheets in Section 5.0. Section 6.0 lists the test equipment used during the tests.

The Modulator was tested first according to the procedure outlined in Section 2.0. Some parts of the demodulator were used while testing the modulator such as filters to provide clean signals and a balanced modulator to act as a phase detector. The phase locked loops were tested next; and then the modulator, phase locked loops and demodulator were connected as a system. The modulator and phase locked loops were then used to provide the input signals for testing of the demodulator.

2.0 Modulator Test Procedures and Results

2.1 Distortion Products and Null Voltages

2.1.1 Procedure

A. Use the test circuit shown in Figure 2.1 connected to modulator 1.

B. Set signal generator 1 for 15 volts peak-to-peak (V p-p) at 16 Hz and signal generator for 15 V p-p at 3 kHz, and signal generator 3 for 4 V p-p at 200 kHz.

C. Sweep the wave analyzer from 2 kHz to 450 kHz with the wave analyzer bandwidth at 1 kHz and record output amplitude versus frequency on the X-Y recorder.

D. Set signal generator 1 and 2 for 0 V and signal generator 3 for 4 V p-p at 200 kHz and repeat C.

E. Repeat B through D with signal generator 1 at 3 kHz and 2 at 16 kHz.

F. Repeat A through E at $-20^{o}C$ and at $+85^{o}C$.

G. All output amplitudes from 2 kHz to 216 kHz should be 50 db down from the desired sidebands.

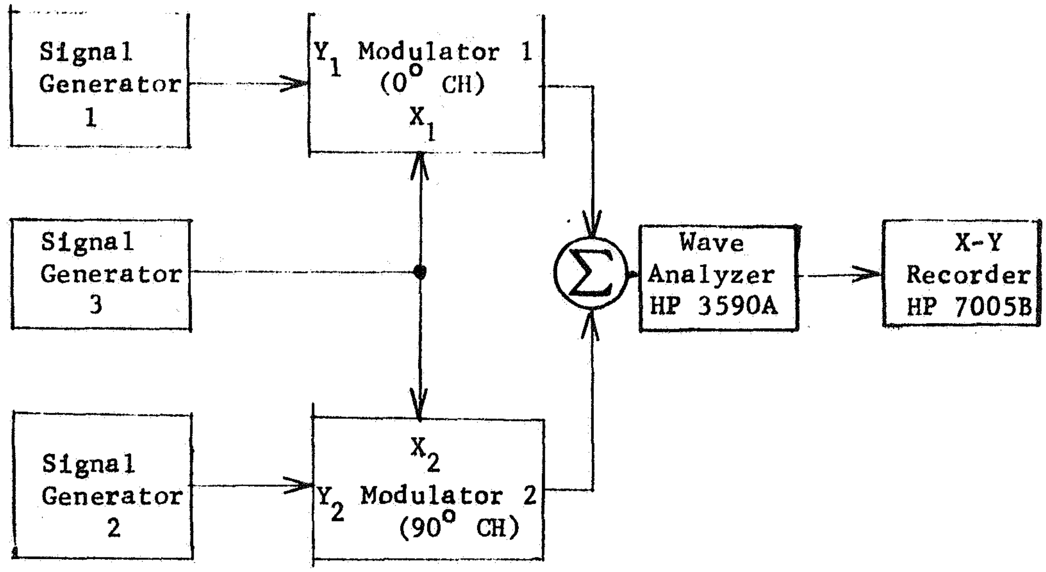

Figure 2.1

Test Circuit for Modulator Distortion Products and Null Voltages

2.1.2 Results

All distortion products and null voltages were attenuated 50 db or more. See Section 5, Figures 5.1 through 5.9.

NOTE: For comparison, the above tests were run with 64 kHz quadrature carriers. These output frequency spectrums are shown in Figures 5.10 and 5.11.

2.2 Amplitude Linearity

2.2.1 Procedure

A. Connect the test circuit shown in Figure 2.2 to modulator 1.

B. Set power supply (X input) to + 4 V dc.

C. Set signal generator to 0, 1, 2, 3, 4, 5, and 5.3 V RMS at 16 kHz. Read and record input and output voltages with Fluke 9500A RMS voltmeter.

D. Repeat C with power supply set to - 4 V dc.

E. Repeat B, C, and D with test circuit connected to modulator 2.

F. Repeat A through E at -20^oC and at $+85^oC$.

G. Maximum deviation from best straight line of modulator output voltage versus input voltage shall be 0.3% of full scale.

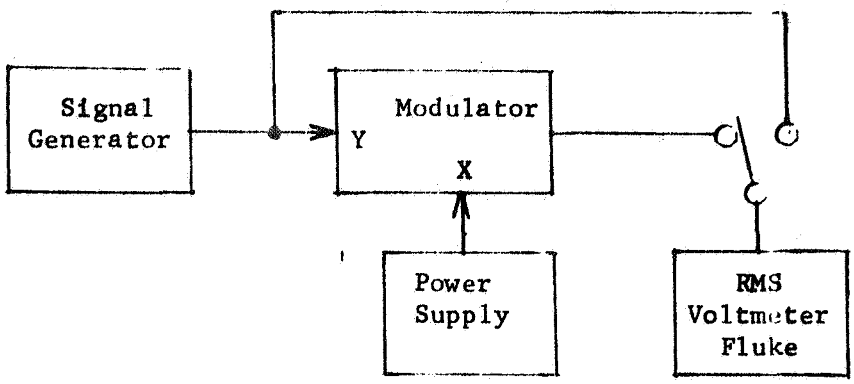

Figure 2.2

Test Circuit for Modulator Amplitude Linearity

2.2.2 Results

The measurements and calculations are shown in Section 5, Tables 5.1 through 5.3. The straight line used for linearity comparison is drawn through the origin (0,0) at a slope calculated from the two maximum readings. The maximum deviation from the straight line is less than 0.3% of full scale.

2.3 Input Impedance

2.3.1 Procedure

A. Connect a 50 ohm signal generator through a 5k 1% resistor to the modulator 1 Y input and set the signal generator for 1 V RMS at 16 kHz.

B. Measure the input voltage at the Y input.

C. Repeat A and B for modulator 2.

D. Repeat A through C for the X input with the signal generator set for 1 V RMS at 200 kHz.

E. The voltage readings for all cases should be 1/2 the generator voltage or greater.

2.3.2 Results

Table 2.1 Input Impedance Data

Channel	Input	Signal Generator Output (V RMS)	Input V RMS	Impedance
0^o	Y	1.007	0.764	15.7K
0^o	X	1.180	0.723	7.9K
90^o	Y	1.007	0.764	15.7V
90^o	X	1.014	0.621	7.8K

Modulator input impedances are greater than 5 K ohms.

2.4 Output Impedance

2.4.1 Procedure

A. Connect a signal generator to the modulator X1 input and set the generator output to 1.5 V RMS, 200 kHz.

B. Apply a dc voltage to the Y1 input and adjust until the modulator summing amplifier output is 400 mV RMS.

C. Connect a 90.9 ohm, 1% resistor between the summing amplifier output and ground and record the new output voltage.

D. The reading in step C shall be 360 mV RMS or greater.

2.4.2 Results

Unloaded output: 0.400 V RMS

Output loaded with 90.9 ohm: 0.399 V RMS

Output impedance is less than 10 ohms.

2.5 Phase Slope

2.5.1 Procedure

A. Use test setup as shown in Figure 2.5 with the signal connected to the input of modulator 1.

B. With switch A in position 1 and switch B in position 2 adjust V_c to 600 mV RMS at 200 kHz and record V_c V_M and filtered dc output V_f.

C. With switch A in position 1 and switch B in position 1 keeping V_c = 600 mV RMS, adjust the dc modulator input until V_M has the same value as in step B. Record filter output V_f.

D. Calculate the modulator phase lag.

$$\text{Phase lag} = \sin^{-1}\left[\frac{V_f \text{ (step C)}}{V_f \text{ (step B)}}\right]$$

E. Repeat steps A through D at 100 kHz and 50 kHz.

F. Repeat steps A through D for modulator 2.

G. Repeat steps A through F at -20° C and at +85°C.

H. Modulator phase slope shall be linear to within ± 1° from 1 to 200 kHz.

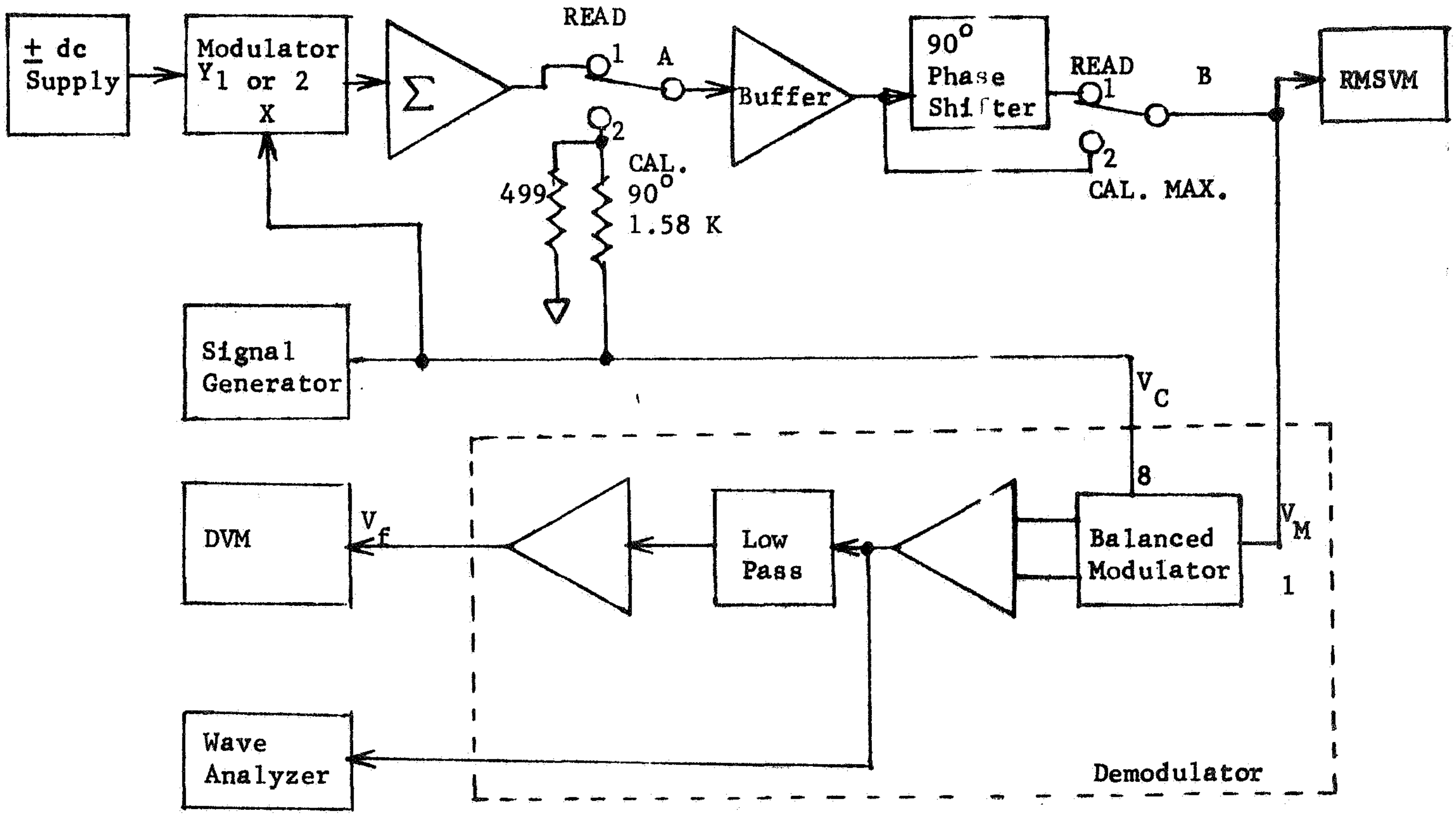

Figure 2.5

Test Circuit for Modulator Phase Slope

NOTE: In this test the test tool is a balanced modulator used as a phase detector. The phase detector output voltage versus phase difference is a sin function and the "in-phase" reading in step B should correspond to the maximum phase detector output (0^o, 0^o); however, this reading includes the phase shift of the modulator and therefore the V_f in step B must be corrected at each test frequency to allow for this. The phase shifter is adjusted for 90^o phase shift with switch A in position 2 at each test frequency. The wave analyzer is used to adjust for minimum carrier feedthrough prior to each reading. Also the dc supply input to the modulator is reversed at each reading, and the average V_f readings are used to compensate for the phase detector and the amplifier offsets.

2.5.2 Results

The phase slope of the modulator is linear to within $\pm 1^o$. See Table 5.4 and Figure 5.12.

2.6 Frequency Response

2.6.1 Procedure

A. Use test setup shown in Figure 2.6 with modulator 1.

B. Set power supply to + 7.5 V dc (Y input).

C. Set wave analyzer output to 4 V p-p and sweep the frequency from 2 kHz to 200 kHz. Record the modulator output on the X-Y recorder set to 1 db/div.

D. Repeat steps A through C with modulator 2.

E. The modulator X input gain shall be flat to within 0.1 db from 2 kHz to 200 kHz.

F. Connect the power supply to the X input of modulator 1 and the wave analyzer output to the Y input. Set the power supply to - 4 V dc and modulator Y input to 15 V p-p.

G. Sweep the frequency from 100 Hz to 16 kHz. Record the modulator output on the X-Y recorder set to 1 db/div.

H. With the setup as in F, set the wave analyzer to 250 Hz and measure the X input and modulator output with a Fluke 9500A RMS digital voltmeter and calculate the modulator gain. Connect a dc power supply to the modulator X input and set to + 7.5 V dc and then - 7.5 V dc. Measure the X input and modulator output and calculate the gain.

I. Repeat F through H for the modulator 2.

J. The modulator Y input gain shall be flat to within 0.1 db from dc to 16 KHz.

K. Repeat A through I at $-20^{\circ}C$ and $+ 85^{\circ}C$.

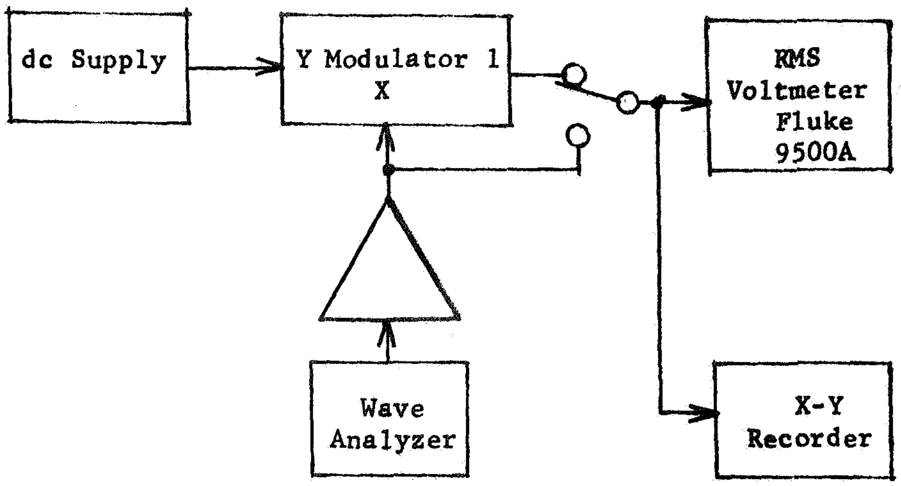

Figure 2.6

Test Setup for Modulator Frequency Response

2.6.2 Results

The frequency response of the modulator X and Y inputs is flat to within 0.1 db. See Table 5.5 and Figures 5.13 and 5.14.

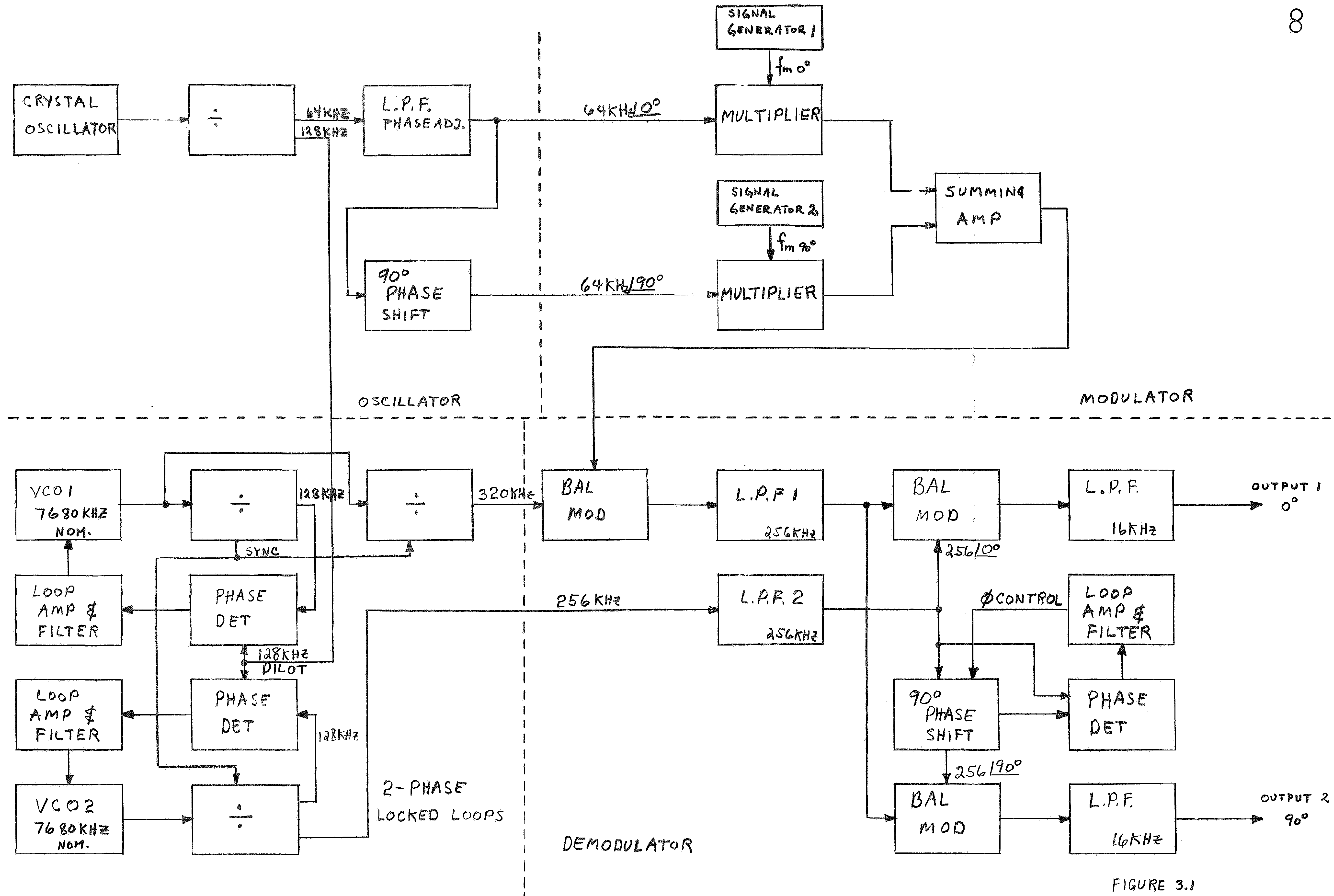

FIGURE 3.1
TEST CIRCUIT FOR DEMODULATOR

3.0 Demodulator - Test Procedures and Results

3.1 Distortion Products and Null Voltages

3.1.1 Procedure

A. Use test circuit shown in Figure 3.1 with channel frequency of 64 kHz and demodulation translation frequency of 256 kHz.

B. Set signal generator 2 to 15 V p-p at 16 kHz.

C. Adjust the phase of the 64 kHz signal for minimum 1 kHz feed-through at demodulator output 1.

D. Adjust the phase of the 90^o phase shifter in the demodulator to minimum 16 kHz feedthrough at demodulator output 2.

E. Sweep wave analyzer at outputs 1 and 2 from 500 Hz to 22 kHz with the wave analyzer bandwidth at 100 Hz and record output voltages versus frequency on the X-Y recorder.

F. Repeat B through E with signal generator 1 at 2.5 kHz and signal generator 2 at 16 kHz.

G. All output amplitudes shall be down 50 db or more from the desired audio signals.

H. Set signal generator 2 to 15 V p-p at 2.5 kHz, and signal generator 1 (wave analyzer) to 15 V p-p at 1 kHz and adjust phase for maximum quadrature suppression of 1 kHz in the demodulator 0^o CH. Sweep frequency of wave analyzer from 500 Hz, and record demodulator 0^o CH output on X-Y recorder.

I. Repeat step H with quadrature suppression adjusted at 4,8 and 16 kHz.

J. Set signal generator 1 to 15 V p-p at 2.5 kHz and signal generator 2 (wave analyzer) to 15 V p-p at 1 kHz and adjust phase for maximum quadrative suppression of 1 kHz in the demodulator 90^o CH. Sweep frequency of wave analyzer from 500 Hz, and record demodulator 90^{o}CH output on X-Y recorder.

K. Repeat step 1 with quadrature suppression adjusted at 4, 8 and 16 kHz.

L. Quadrature suppression at the adjusted frequency shall be 50 db or greater.

3.1.2 Results

Distortion Products and Null Voltages and Quadrature feedthrough are attenuated by 50 db or more. See Figures 5.15 through 5.20.

3.2 Amplitude Linearity

3.2.1 Procedure

A. With test set up as in 3.1, set signal generator 1 to 0, 1, 2, 3, 4, 5 and 5.3 V RMS at 16 kHz. Set signal generator 2 to zero volts.

B. Record output voltages of signal generator 1 and demodulator output 1 with Fluke 9500A RMS voltmeter.

C. With signal generator 1 at zero volts set signal generator 2 to 0, 1, 2, 3, 4, 5 and 5.3 V RMS and record output voltages of signal generator 2 and demodulator output 2 with Fluke 9500A RMS voltmeter.

D. Maximum deviation from best straight line of demodulator output voltage versus signal generator output voltage shall be less than 0.3% of full scale.

3.2.2 Results

Demodulator amplitude linearity is better than 0.3% of full scale.

3.3 Input Impedance

3.3.1 Procedure

A. Connect a 50 ohm signal generator through a 5k ohm, 1% resistor to the demodulator input and set the signal generator for 1 V RMS at 200 kHz.

B. Measure the input voltage at the demodulator input.

C. The voltage reading in B shall be 1/2 the signal generator voltage or greater.

3.3.2 Results

Signal generator output:	1.02 V RMS
Modulator input:	0.579 V RMS
Input impedance =	6.65 K

3.4 Output Impedance

3.4.1 Procedure

A. With test set up as in 3.1 adjust signal generators for 100 mV RMS output voltage at demodulator output 1 and 2 at 16 kHz.

B. Connect a 90.9 ohm, 1% resistor from each of the demodulator outputs to ground and record the new output voltages.

C. The readings in step C shall be greater than 90 mV RMS.

3.4.2 Results

Table 3.1 Output Impedance Data

	0°CH	90°CH
Output unloaded (mV RMS)	100.2	100.3
Output loaded (mV RMS)	94.7	93.7

Output impedances are smaller than 10 ohms.

3.5 Frequency Response

3.5.1 Procedure

A. With test set up as in 3.1 set signal generator 2 to zero volts and signal generator 1 (wave analyzer) to 1 V RMS.

B. Sweep frequency of wave analyzer from 700 hZ to 16 kHz and record demodulator output 1 and signal generator 1 output voltages on X-Y recorder. At 0.7 kHz measure output voltages with Fluke 9500A RMS meter and calculate gain.

C. Set signal generator 1 to zero volts and signal generator 2 (wave analyzer) to 1 V RMS.

D. Sweep frequency of signal generator 2 from 700 Hz to 16 kHz and record demodulator output 2 and signal generator 2 output voltages on X-Y recorder. At 0.7 kHz measure output voltages with Fluke 9500A RMS meter and calculate gain.

E. Replace signal generator 1 with a dc power supply. With signal generator 2 at zero volts set the dc supply to +1.4 V dc and then to -1.4 Vdc, measure dc output at demodulator output 1 and calculate gain.

F. Repeat step E with signal generator 2 replaced by the dc power supply.

G. The frequency response shall be flat to within 0.1 db from dc to 16 kHz. The response shall be down 50 db at 48 kHz.

3.5.2 Results

The demodulator frequency response is flat to within 0.1 db. See Table 5.7 and Figures 5.21 and 5.22.

4.0 VCO (Phase Locked Loops)

4.1 Phase Lock Loop Tracking Response, Linearity and Phase Jitter.

4.1.1 Procedure

A. Use test set up shown in Figure 4.1.

B. Open loop on VCO 2 so that VCO 2 is unlocked. VCO 2 now becomes the FM reference pilot signal for VCO loop 1.

C. With wave analyzer set at 500 Hz, bandwidth at 100 Hz adjust frequency of VCO 2 for a frequency difference of 500 Hz between VCO 1 and VCO2. The output of the calibration amplifier as read by the wave analyzer should now be maximum. (The calibration amplifier now reads phase error with $90^{\circ} = 0$ db). Set the wave analyzer and X-Y recorder for 0 db reference. Readjust the frequency of VCO 2 until loop 1 phase locks in the center of its locking range. Increase the wave analyzer output amplitude until VCO 2 is frequency modulated $\pm$ 1% (measure with oscillioscope).

D. Set the wave analyzer BW to 10 Hz and sweep the frequency from 30 Hz to 1 kHz and record on the X-Y recorder.

E. Repeat steps A through D using loop 2 as the phase locked loop and loop 1 as the pilot FM reference.

F. Phase error from 30 Hz to 500 Hz should be down 50 db or more relative to the 0 db reference from step C.

G. Lock both VCO loops to the reference pilot from the reference oscillator. With the wave analyzer bandwidth set to 1 kHz, record the spectrum of both the 320 kHz and 256 kHz divider chain outputs on the X-Y recorder.

H. All spurious outputs below the desired frequency (320 kHz or 256 kHz) should be down 50 db or more from the desired frequency.

4.1.2 Results

The phase error below 500 Hz is below 50 db. See Figures 5.23 and 5.24. Spurious outputs from the loops are down 50 db or more. See Figures 5.25 and 5.26.

4.2 Frequency Stability (Frequency Pulling Range)

4.2.1 Procedure

A. Use test set up shown in Figure 4.1.

B. Connect a frequency counter to the 128 kHz loop output in LC-VCO_1.

C. Connect a 10 k ohm resistor from pin 2 to ground and then from pin 3 to ground on the loop input amplifier and measure the frequency at the "128 kHz" loop output.

D. Repeat steps B and C for LC-VCO_2.

E. The pulling range shall be 128 kHz $\pm$ 1.003% or greater.

4.2.2 Results

Table 4.1 Frequency Stability Data

	Max. Frequency kHz	Min. Frequency kHz
VCO_1 (320 kHz)	135.43	111.80
VCO_2 (256 kHz)	133.87	111.06

The pulling range is greater than $\pm$ 1.003%.

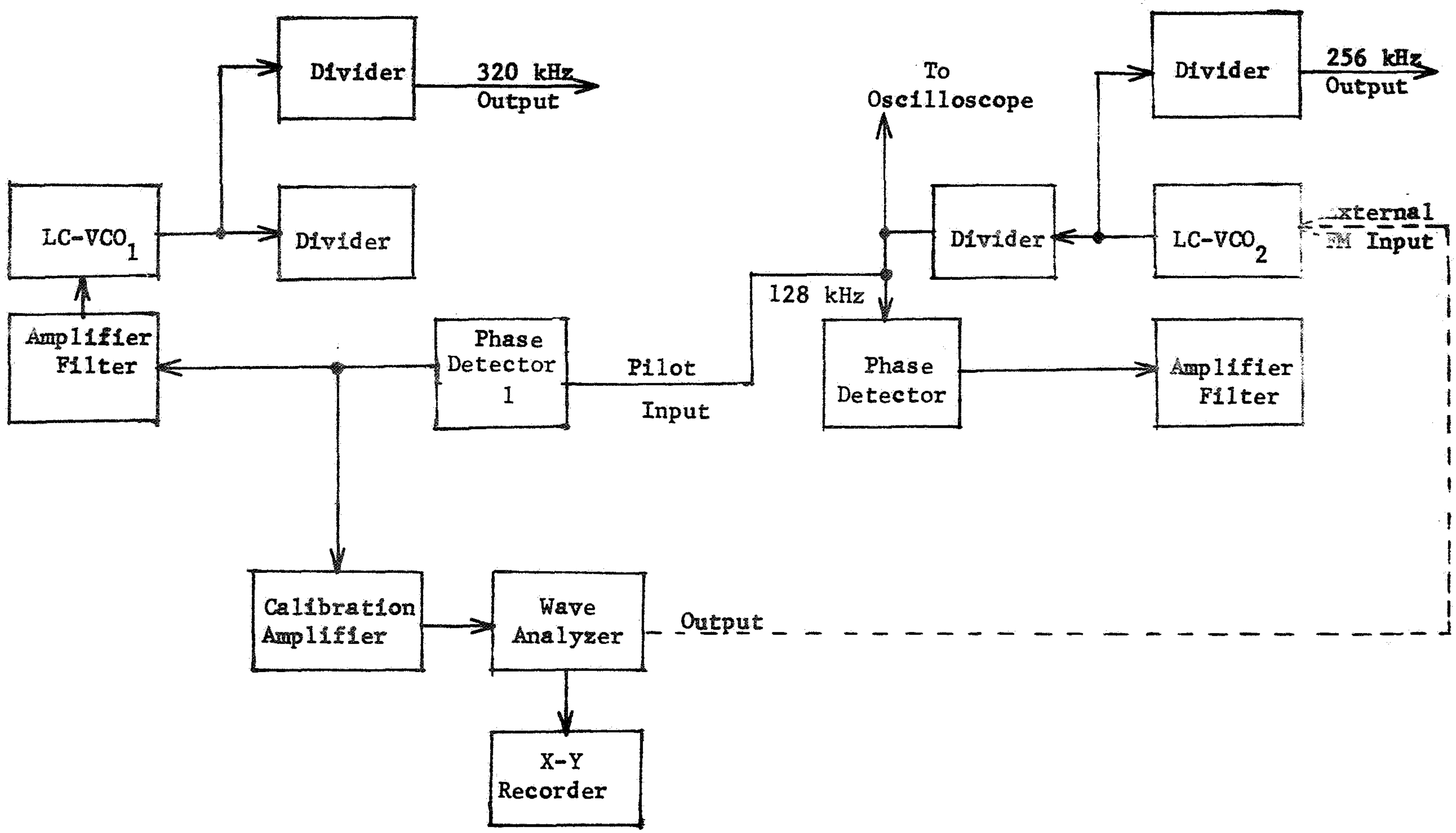

Figure 4.1
Test Circuit for Phase Locked Loops

5.0 TEST DATA

Table 5.1 Modulator Amplitude Linearity, 25°C

CH	Input (V dc)	Input (VRMS)	Output (VRMS)	Calculated Straight Line (VRMS)	0.3% Max. Deviation (VRMS)	Measured Deviation (VRMS)
0°	+4.000	5.307	.8263	.82675	±.00248	-.0005
		4.998	.7782	.77861		-.0004
		4,000	.6236	.62314		+.0005
		2.995	.4672	.46658		+.0006
		1.993	.3108	.31048		+.0005
		1.000	.1560	.15579		+.0002
		0	.000	0		.000
	-4.000	.9995	.1559	.15571		+.0002
		2.006	.3129	.31250		+.0004
		2.998	.4676	.46704		+.0006
		4.000	.6238	.62314		+.0007
		5.007	.7807	.78002		+.0007
0°		5.307	.8272	.82675		+.0004
90°	+4.000	5,300	.8243	.82434	±.00248	.0000
		5.007	.7783	.77877		-.0005
		3.996	.6195	.62153		-.0020
		3,009	.4683	.46801		+.0003
		2.009	.3122	.31247		-.0003
		.9962	.1547	.15495		-.0003
		0	.000	0		00
	-4.000	1.000	.1555	.15554		.0000
		1.994	.3103	.31014		+.0002
		2.996	.4660	.46599		.0000
		4.009	.6239	.62355		+.0004
		5.004	.7777	.77831		-.0006
90°		5.302	.8247	.82466		.0000

Table 5.2 Modulator Amplitude Linearity, +85°C

CH	Input (V dc)	Input (VRMS)	Output (VRMS)	Calculated Straight Line (VRMS)	.3% Max. Deviation (VRMS)	Measured Deviation (VRMS)
0°	+4.000	5.308	.8182	.8188	±.00248	-.0006
		4.995	.7699	.7705		-.0006
		4.006	.6174	.6180		-.0006
		3.000	.4619	.4628		-.0009
		2.007	.3095	.3096		-.0001
		.9967	.1536	.1537		-.0001
		0	.000	0		.000
	-4.000	.997	.1538	.1538		.0000
		1.996	.3080	.3079		+.0001
		2.997	.4625	.4623		+.0002
		4.000	.6174	.6170		+.0004
		4.999	.7717	.7711		+.0006
0°		5.306	.8191	.8185		+.0006
90°	+4.000	5.306	.8163	.81648	±.00248	-.0002
		4.999	.7694	.76924		+.0002
		4.000	.6146	.61552		-.0009
		3.006	.4629	.46256		+.0003
		1.996	.3068	.30714		-.0003
		.9962	.1533	.15329		.0000
		0	.000	0		.000
	-4.000	.999	.1540	.15372		+.0003
		1.996	.3077	.30714		+.0006
		2.996	.4616	.46102		+.0006
		3.996	.6156	.61490		+.0007
		5.006	.7709	.77032		+.0006
90°		5.303	.8162	.81602		+.0002

Table 5.3 Modulator Amplitude Linearity, -20°C

CH	Input	Input (VRMS)	Output (VRMS)	Calculated Straight Line (VRMS)	0.3% Max. Deviation (VRMS)	Measured Deviation (VRMS)
0°	+4.000	5.301	.831	.8300	±.00248	+.001
		4.992	.783	.7816		+.0014
		4.003	.627	.6268		+.0002
		3.000	.470	.4697		+.0003
		2.000	.314	.3131		+.0009
		1.008	.158	.1578		+.0002
		0	.000	0		.000
	-4.000	.998	.156	.1563		-.0003
		2.001	.313	.3133		-.0003
		2.997	.4685	.4693		-.0008
		3.997	.625	.6258		-.0008
		5.000	.782	.7829		-.0009
0°		5.307	.829	.8300		-.001
90°	+4.000	5.296	.830	.8290	±.00248	+.001
		4.992	.783	.7814		+.0016
		4.002	.628	.6265		+.0015
		2.991	.469	.4682		+.0008
		1.992	.313	.3118		+.0012
		1.005	.1575	.1573		+.0002
		0	.000	0		.000
	-4.000	.998	.156	.1562		-.0002
		2.006	.314	.3140		..0000
		3.004	.470	.4702		-.0002
		4.000	.627	.6262		+.0008
		4.993	.781	.7816		-.0006
90°		5.302	.829	.8300		-.001

Table 5.4 Modulator Phase Slope

CH	Frequency (kHz)	Temperature (^oC)	V_c (VRMS)	V_M (VRMS)	V_{fb} (mVdc)	V_{fc} (mVdc)
90°	200	+25	.6013	1.0596	1016.2	104.9
0°	200			1.0596	1016.2	103.2
90°	100			1.0680	1035.5	54.6
0°	100			1.0680	1035.5	54.1
90°	50			1.0215	997.5	25.6
0°	50			1.0215	997.5	25.4
90°	200	+85		1.0257	983.9	108.0
0°	200			1.0257	983.9	104.8
90°	100			1.0215	987.1	52.6
0°	100			1.0215	987.1	51.5
90°	50			1.021	998.0	28.2
0°	50			1.021	998.0	27.6
90°	200	-20		1.0298	989.7	93.1
0°	200			1.0298	989.7	96.2
90°	100			1.0255	992.6	48.2
0°	100			1.0255	992.6	49.6
90°	50			1.020	996.2	25.3
0°	50			1.020	996.2	26.2

NOTE: 1. Max readings V_{fb} are compensated to allow for modulator phase shift per note in 2.5.1.

2. Both V_{fb} amd V_{fc} are averaged for modulator positive and negative DC input voltage per note in 2.5.1.

Table 5.5 Modulator Frequency Response, Y-Inputs

Y-Input AC Gain at 250 hZ

CH	Temperature °C	V_x (Vdc)	V_y (VRMS)	V_{out} (VRMS)	Gain
90°	-20	-3.995	5.246	.820	1.563
	+25			.820	1.563
	+85			.806	1.537
0°	-20		5.280	.827	1.565
	+25			.825	1.560
	+85			.815	1.545

Y-Input DC Gain

CH	Temperature °C	V_x (Vdc)	V_y (Vdc)	V_{out} (Vdc)	Gain
90°	-20	-3.995	+6.211	+.991	1.573
	-20		-6.211	-.965	
	+25		+6.224	+.987	1.563
	+25		-6.224	-.957	
	+85		+6.220	+.976	1.540
	+85		-6.220	-.942	
0°	-20		+6.211	+.990	1.568
	-20		-6.211	-.959	
	+25		+6.224	+.989	1.570
	+25		-6.224	-.968	
	+85		+6.270	+.978	1.554
	+85		-6.220	-.955	

Table 5.6 Demodulator Amplitude Linearity

CH	[illegible] Modulator (VRMS)	[illegible] (VRMS)	Calculated Straight Line (VRMS)	0.3% Deviation (VRMS)	Actual Deviation (VRMS)	Gain
0°	5,308	2,974	2.9738	±.0089	+.0002	.5603
	4.962	2.770	2.7800		-.001	.5582
	3.984	2.228	2.2321		-.0004	.5592
	2.009	1.125	1.1256		-.0006	.5600
	1.002	.5605	.56138		-.0009	.5594
	.4974	.2778	.2787		-.0009	.5595
	.2021	.1128	.1132		-.0004	.5581
	.04810	.02690	.02695		-.0001	.5593
0°	.01419	.00795	.00795		.0000	.5603
90°	5.292	2.970	2.9699		+.0001	.5612
	5.050	2.836	2.8340		-.0004	.5616
	4.039	2.270	2.2667		+.0003	.5620
	3.043	1.708	1.7077		+.0003	.5613
	2.002	1.124	1.1235		-.0001	.5614
	1.018	.5710	.57129		-.0003	.5609
	.5002	.2805	.28071		-.0002	.5608
	.2007	.1125	.11263		-.0001	.5605
	.04825	.02705	.02708		-.0003	.5606
90°	.01418	.00796	.00798		-.0000	.5614

Table 5.7 Demodulator Frequency Response

ac Gain at 700 Hz

Channel	Input (VRMS)	Output (VRMS)	Gain
90°	1.008	.6475	.642
0°	1.008	.6038	.599

dc Gain

Channel	Input (V dc)	Output (V dc)	Gain
90°	+1.409 -1.409	-.903 +.906	.638
0°	+1.409 -1.409	-.841 +.846	.596

6.0 Test Equipment

The test equipment is given in Table 6.1

Table 6.1 Test Equipment

Description	Manufacturer	Model No.	Identification	Calibration Due
Wave Analyzer	Hewlett-Packard	3590A	EQ528777	06/12/71
RMS Digital Voltmeter	Fluke	9500A	EQ526403	04/01/71
Digital Voltmeter	Dana	5400	EQ521647	03/10/71
Wide Range Oscillator	Hewlett-Packard	200CD	ME104466	06/04/71
Low Frequency Oscillator	Hewlett-Packard	202C	EQ500562	08/04/71
X-Y Recorder	Hewlett-Packard	7005B	EQ528778	06/12/71
HF VCG Generator	Wavetek	142	EQ529438	03/03/71

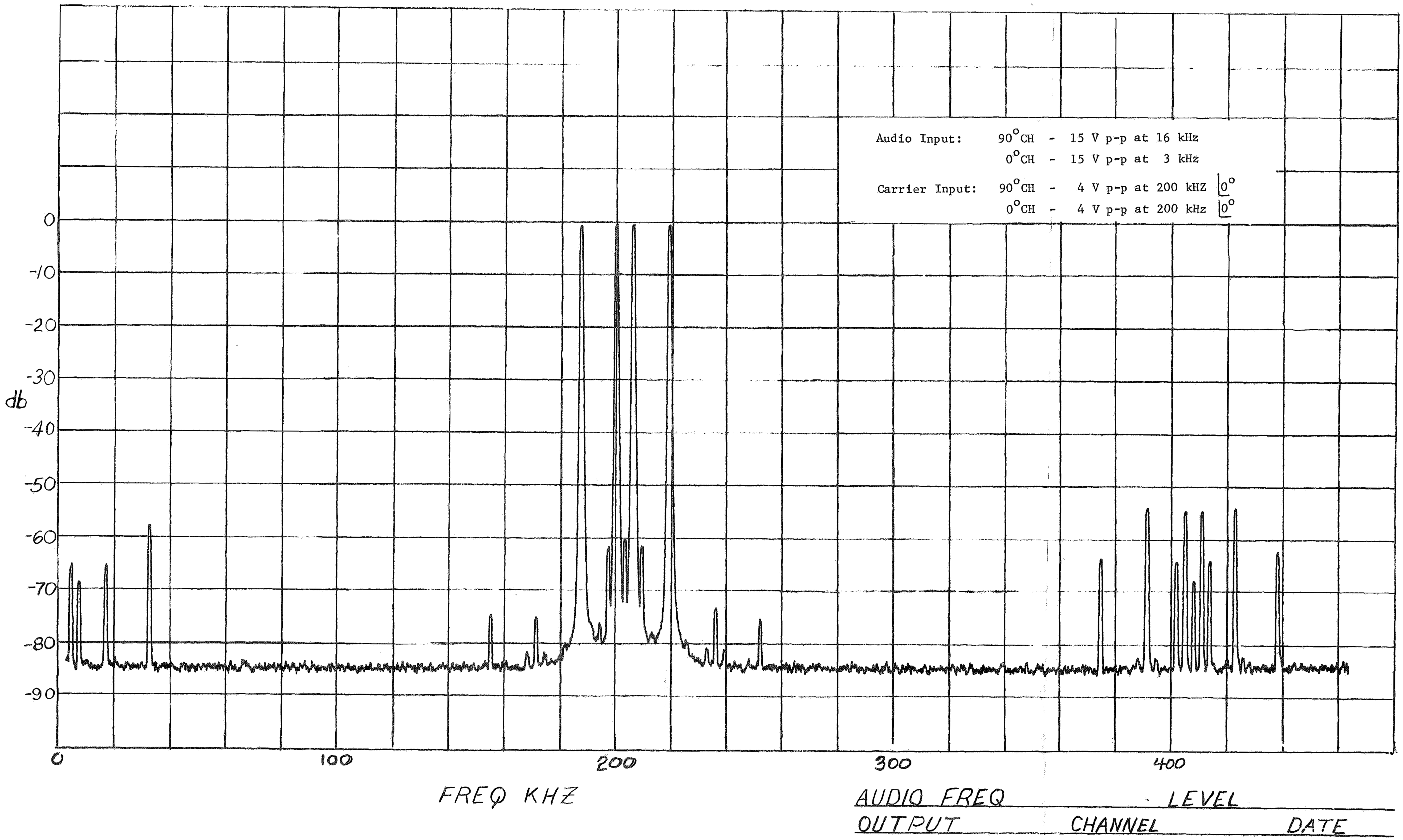

Figure 5.1

Modulator Output Frequency Spectrum, 25°C

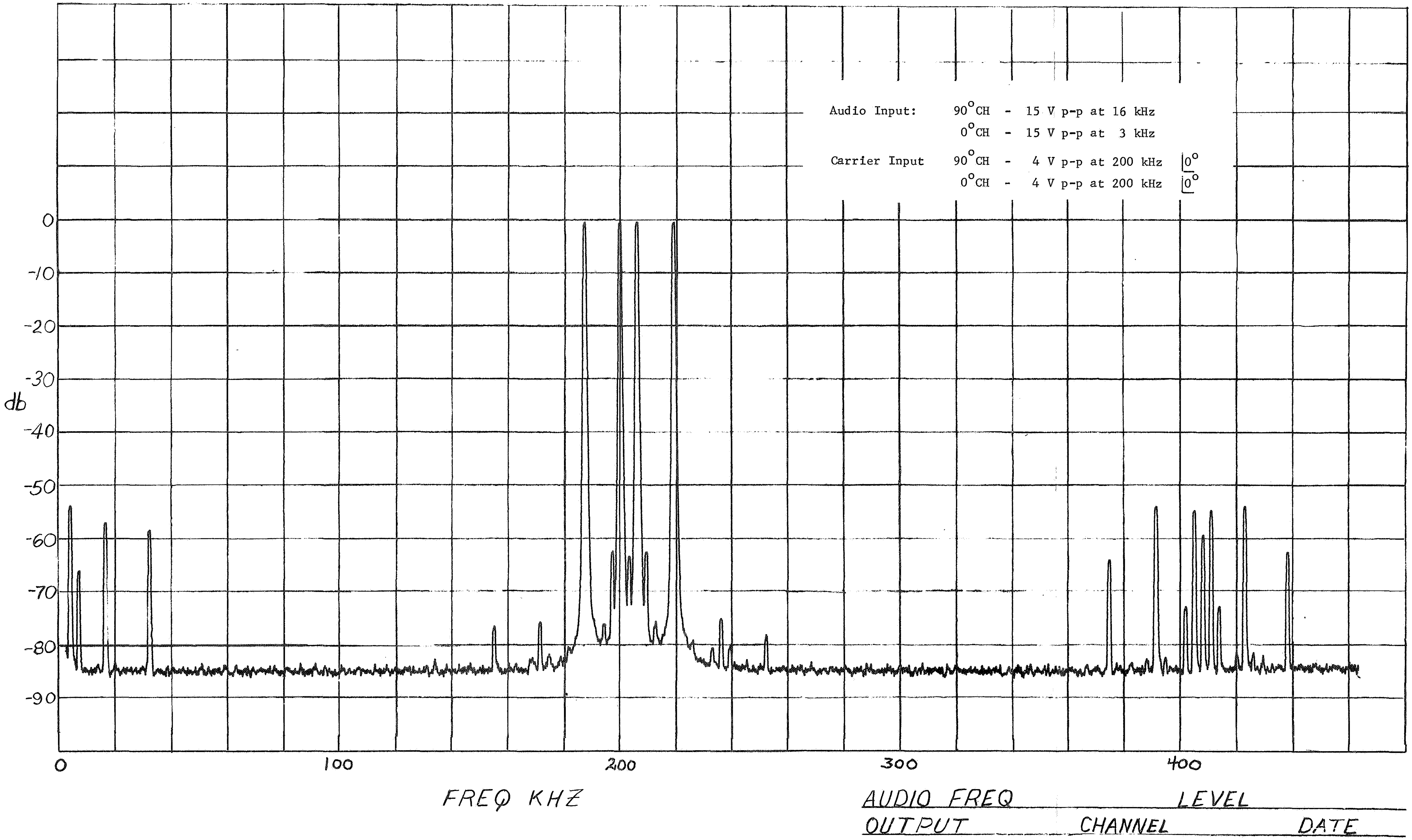

Figure 5.2

Modulator Output Frequency Spectrum, -20°C

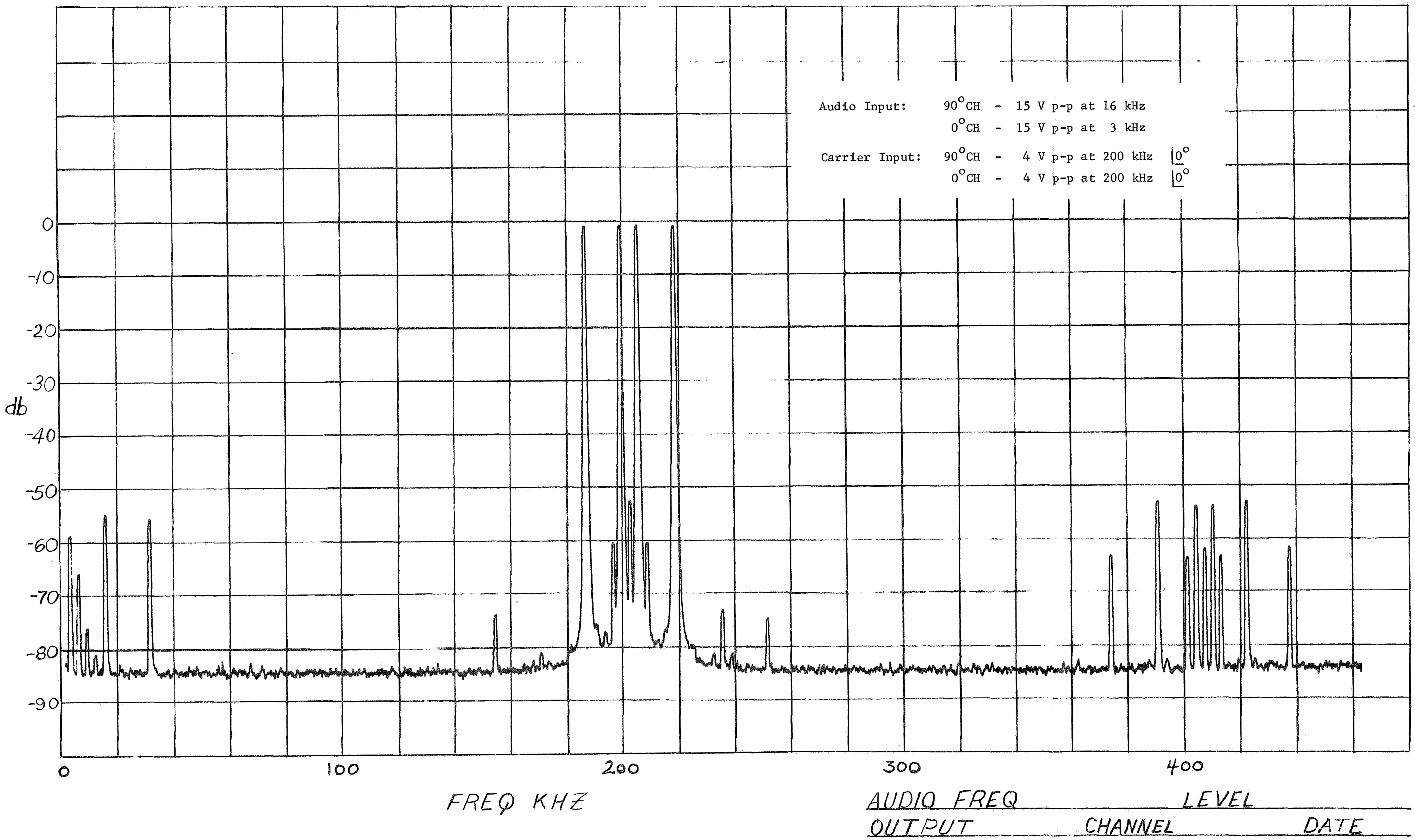

Figure 5.3
Modulator Output Frequency Spectrum, +85°C

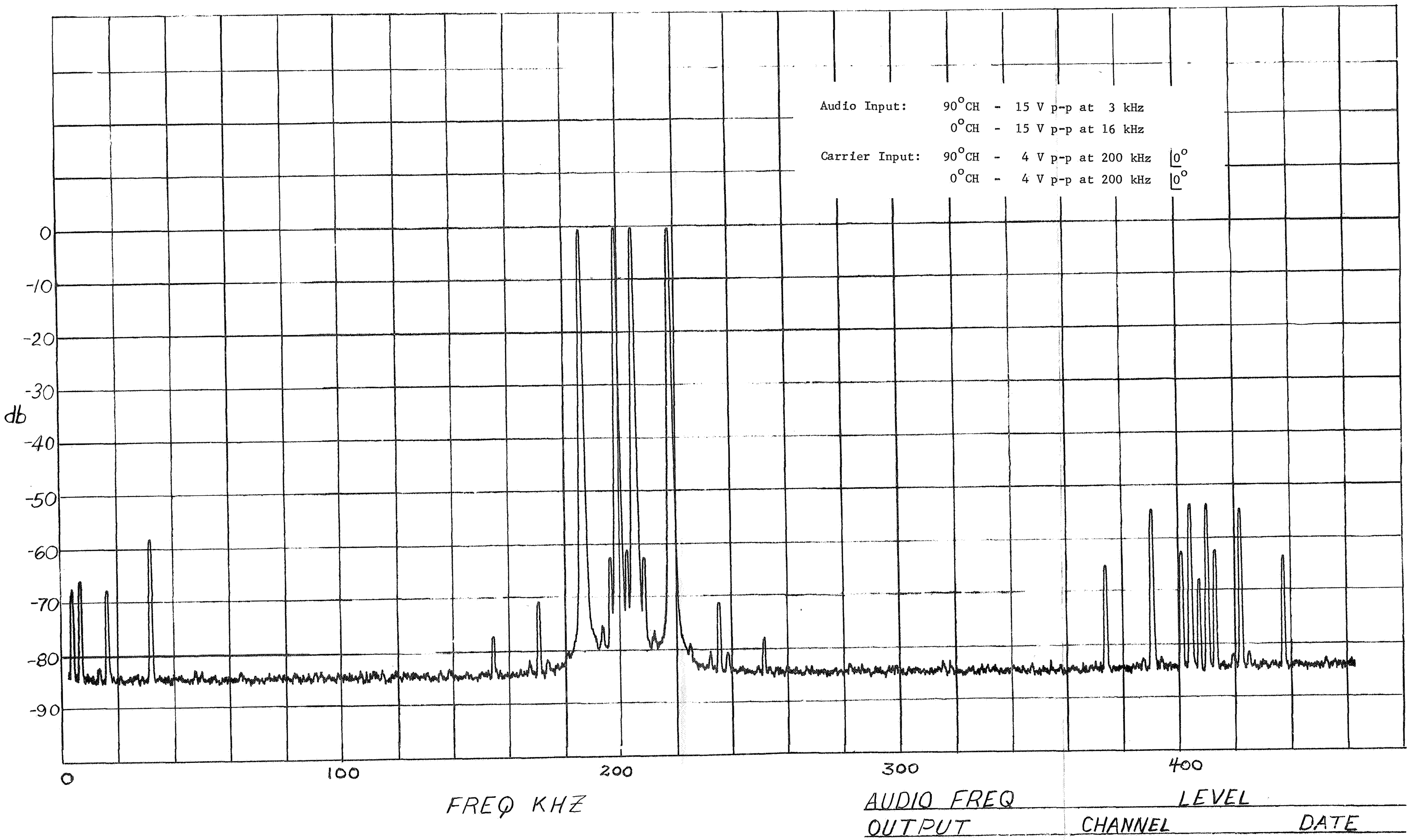

Figure 5.4

Modulator Output Frequency Spectrum, 25°C

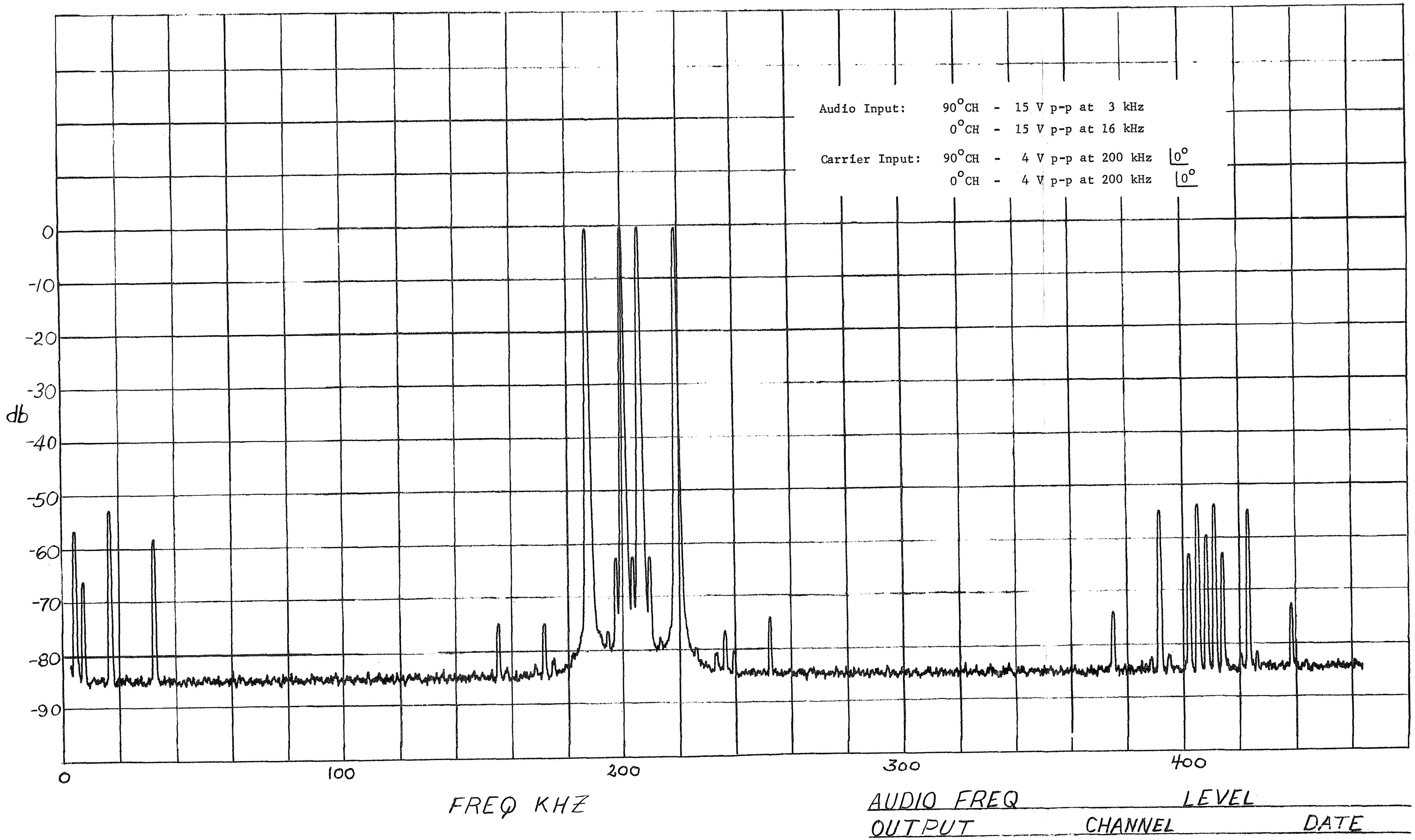

Figure 5.5

Modulator Output Frequency Spectrum, -20°C

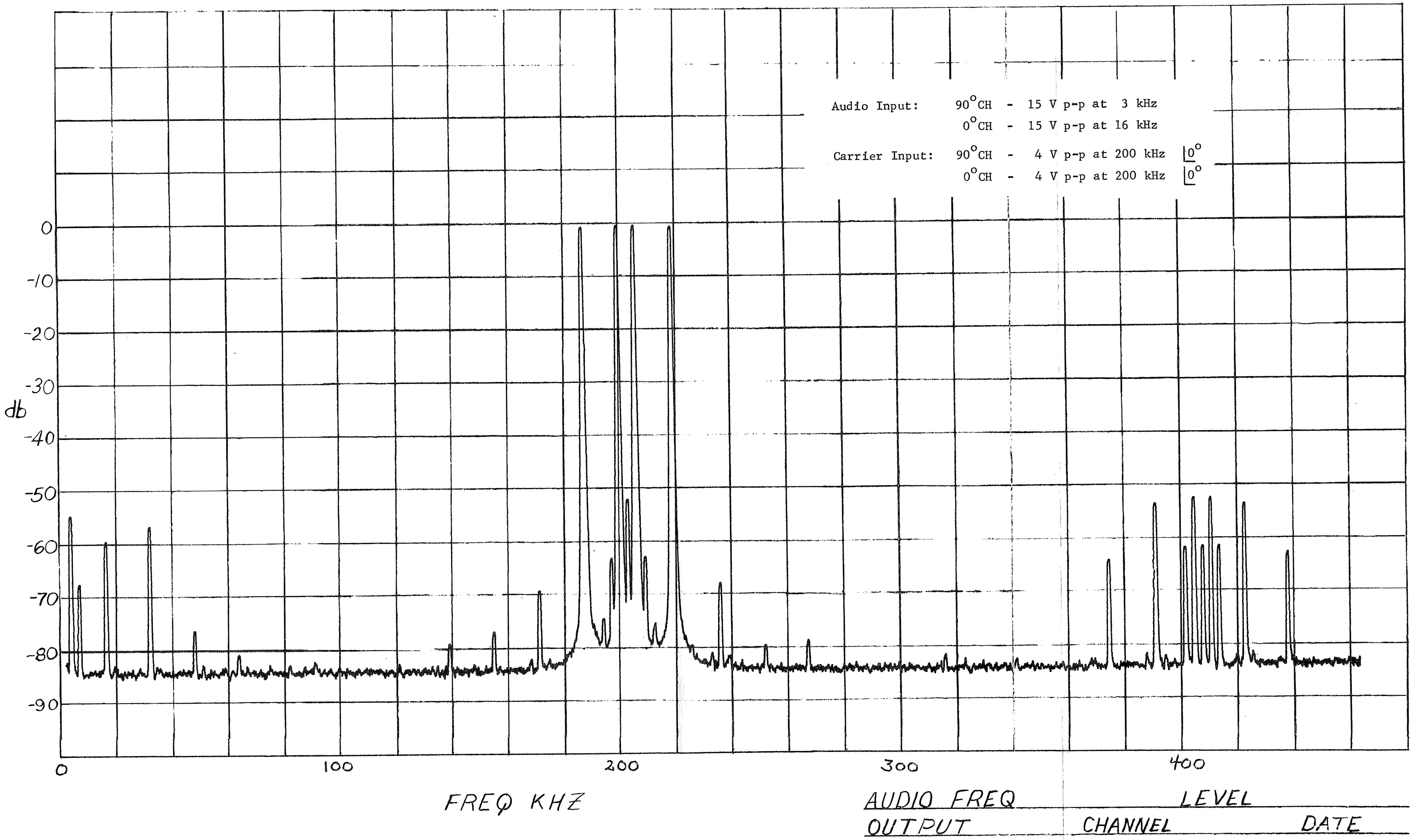

Figure 5.6

Modulator Output Frequency Spectrum, +85°C

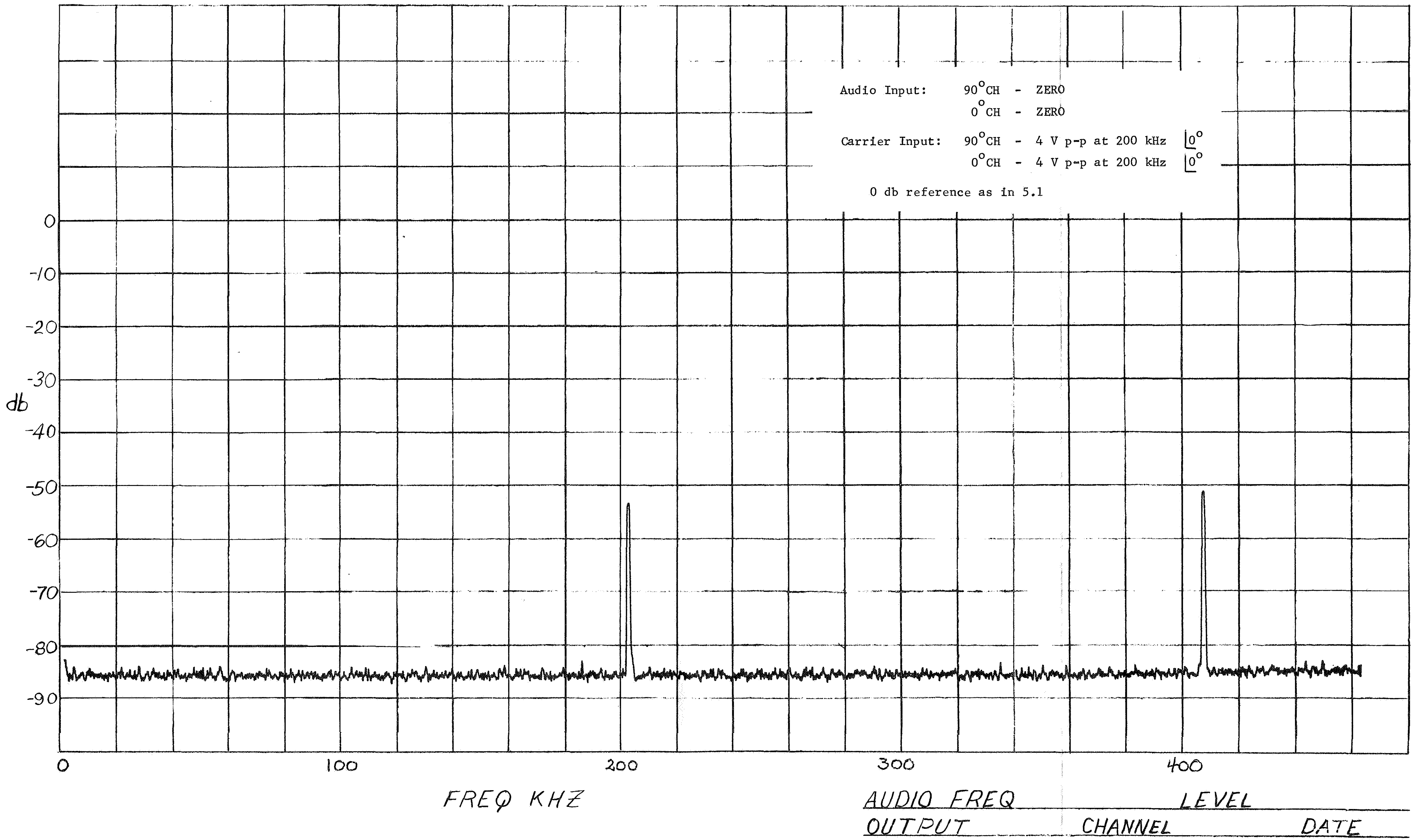

Figure 5.7

Modulator Null Voltages, 25°C

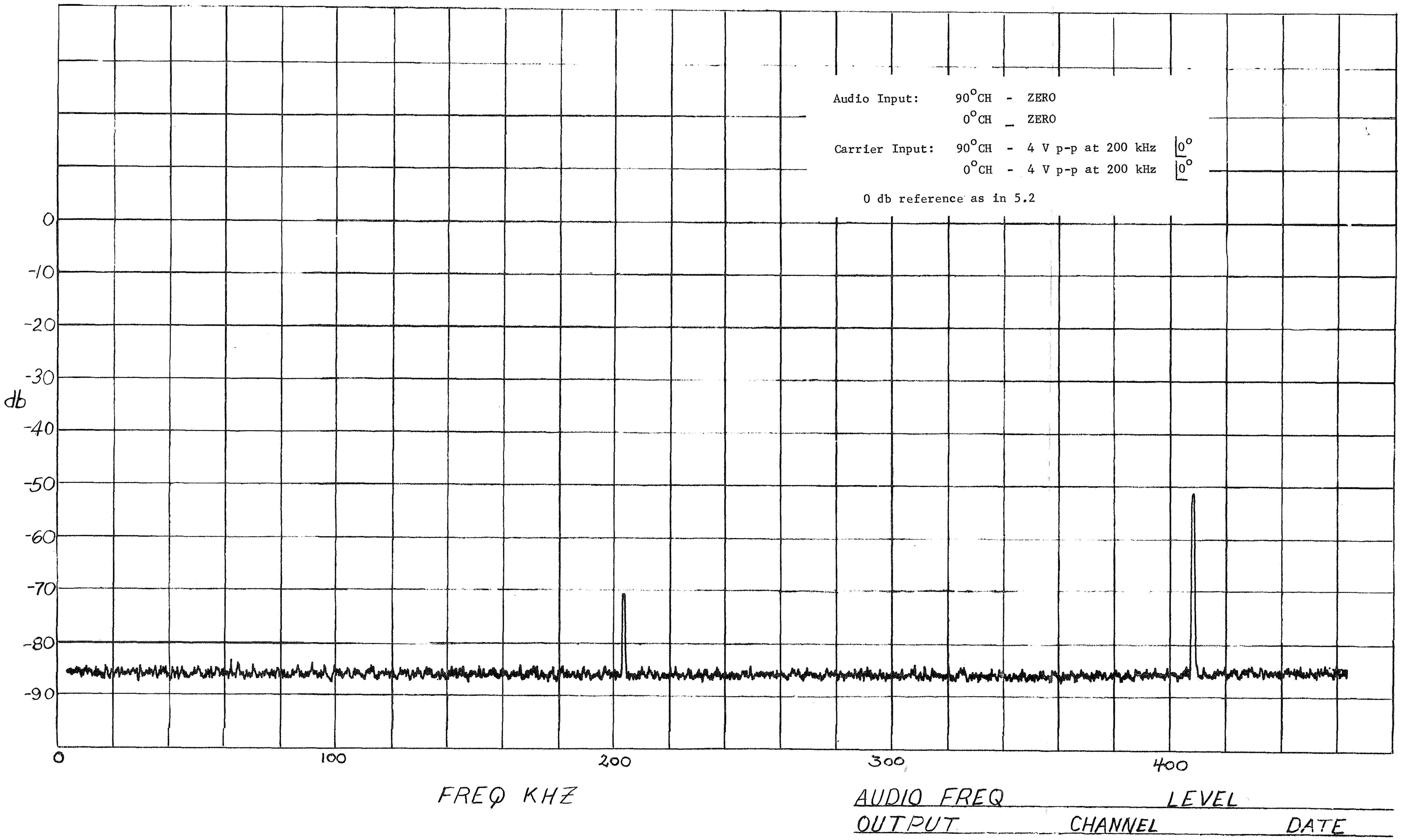

Figure 5.8

Modulator Null Voltages, -20°C

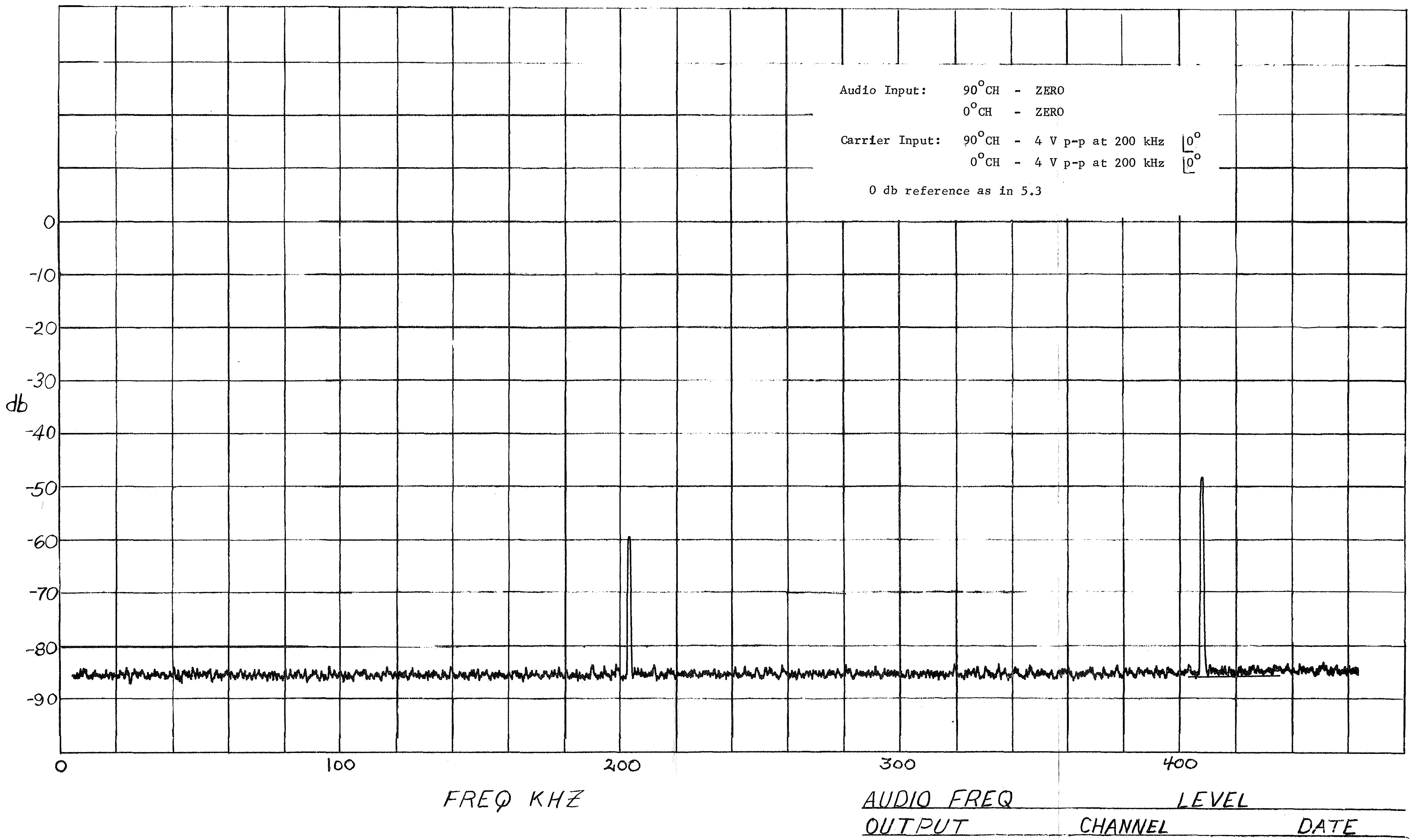

Figure 5.9

Modulator Null Voltages, +85°C

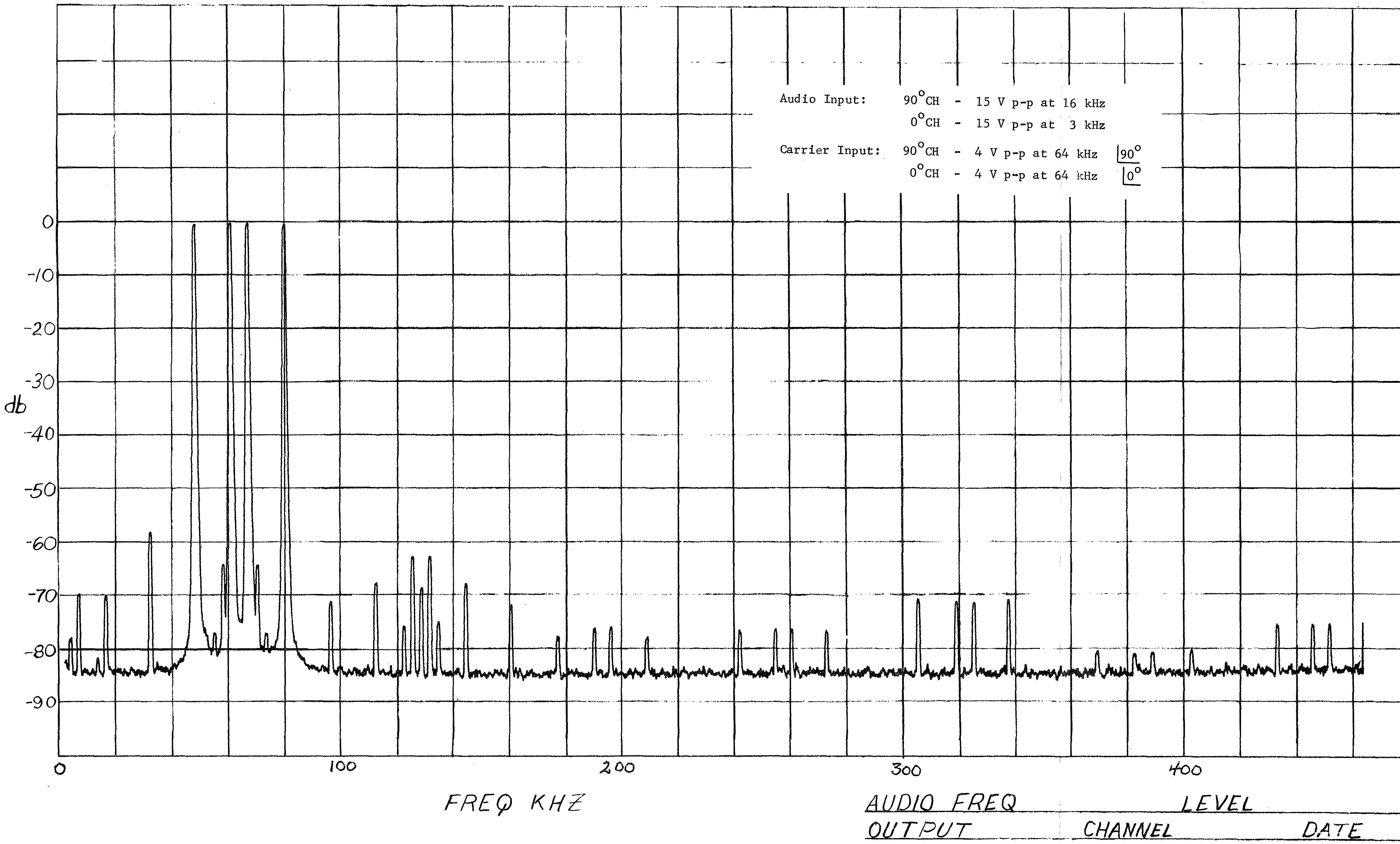

Figure 5.10

Modulator Output Frequency Spectrum, 25°C

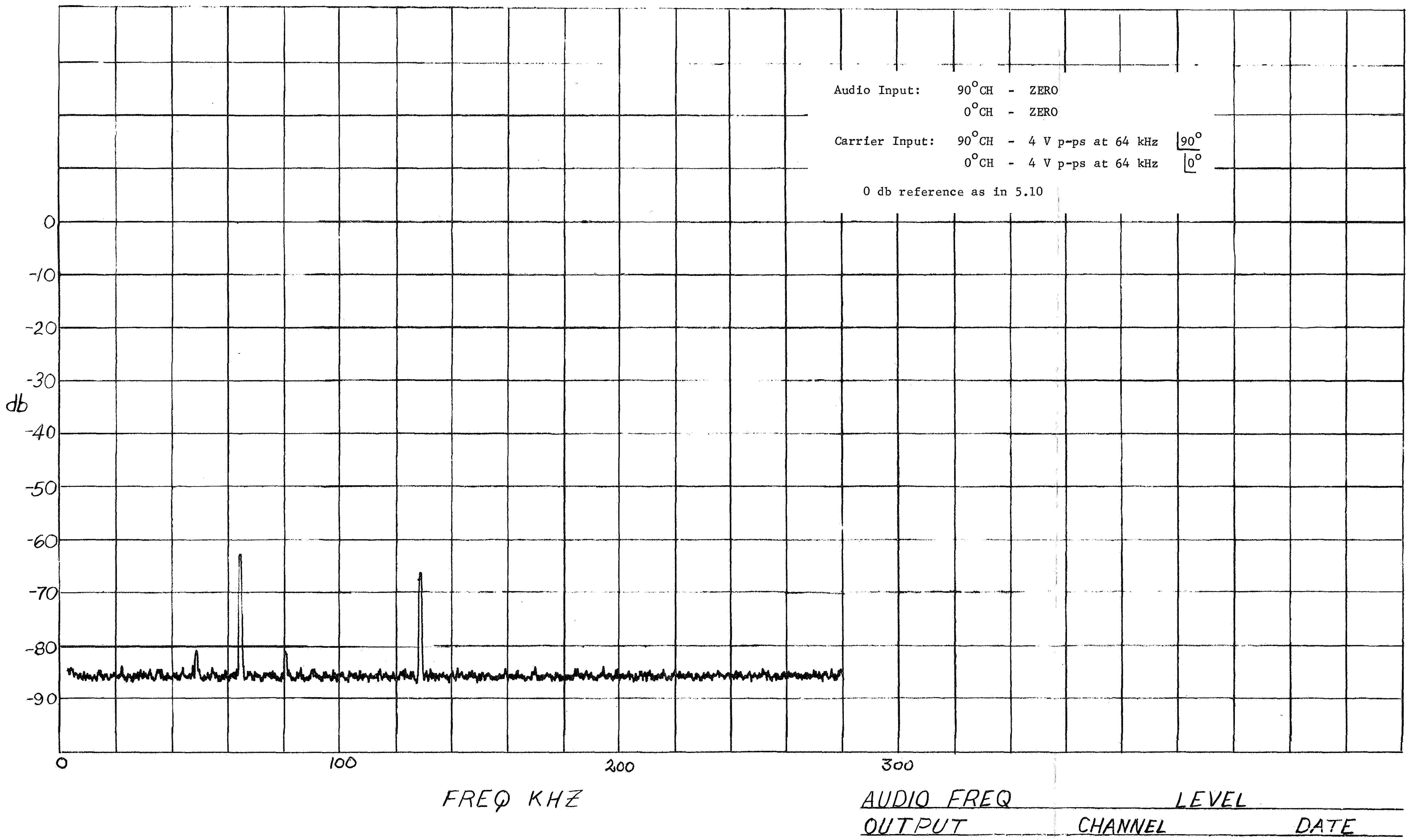

Figure 5.11

Modulator Null Voltages, 25°C

5.12 Modulator Phase Slope

PHASE LAG (DEGREES)

°C	90° CH			0° CH		
	FREQUENCY KHZ			FREQUENCY KHZ		
	200	100	50	200	100	50
+85	6.3	3.05	1.61	6.11	2.99	1.59
+25	5.92	3.02	1.47	5.80	3.0	1.46
-20	5.4	2.79	1.46	5.57	2.87	1.50

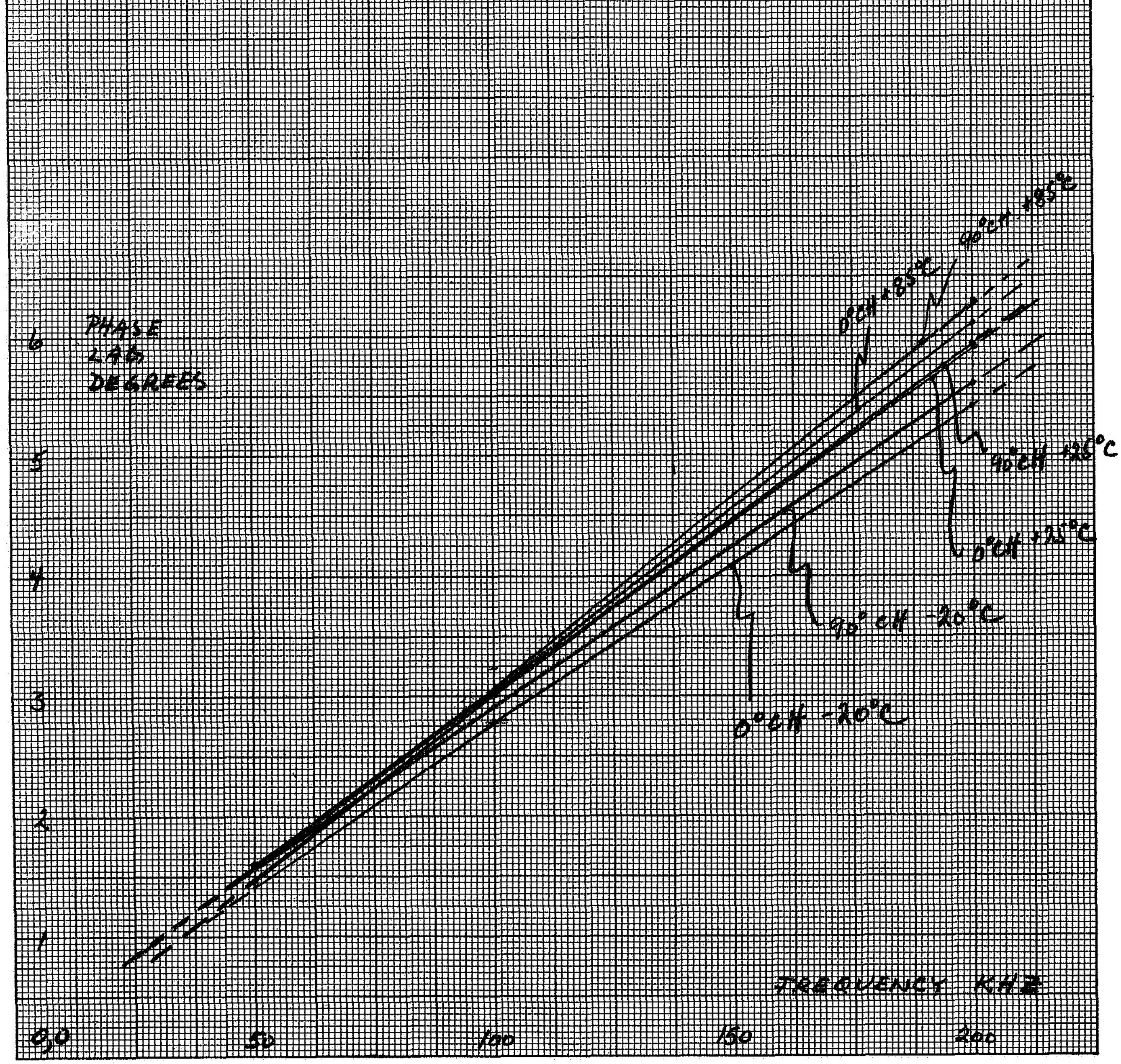

Figure No. 5.12

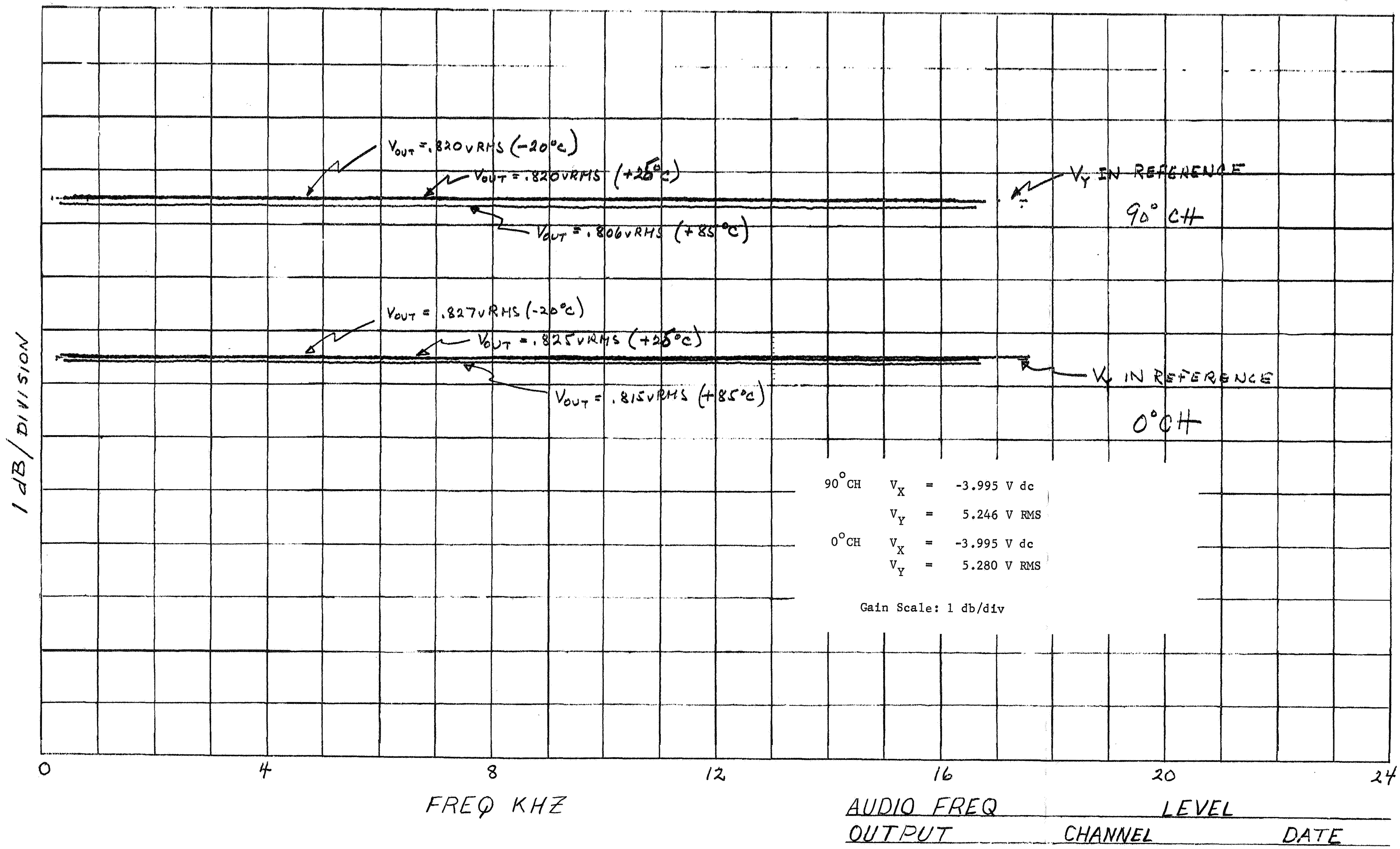

Figure 5.13
Modulator Frequency Response Y-Inputs

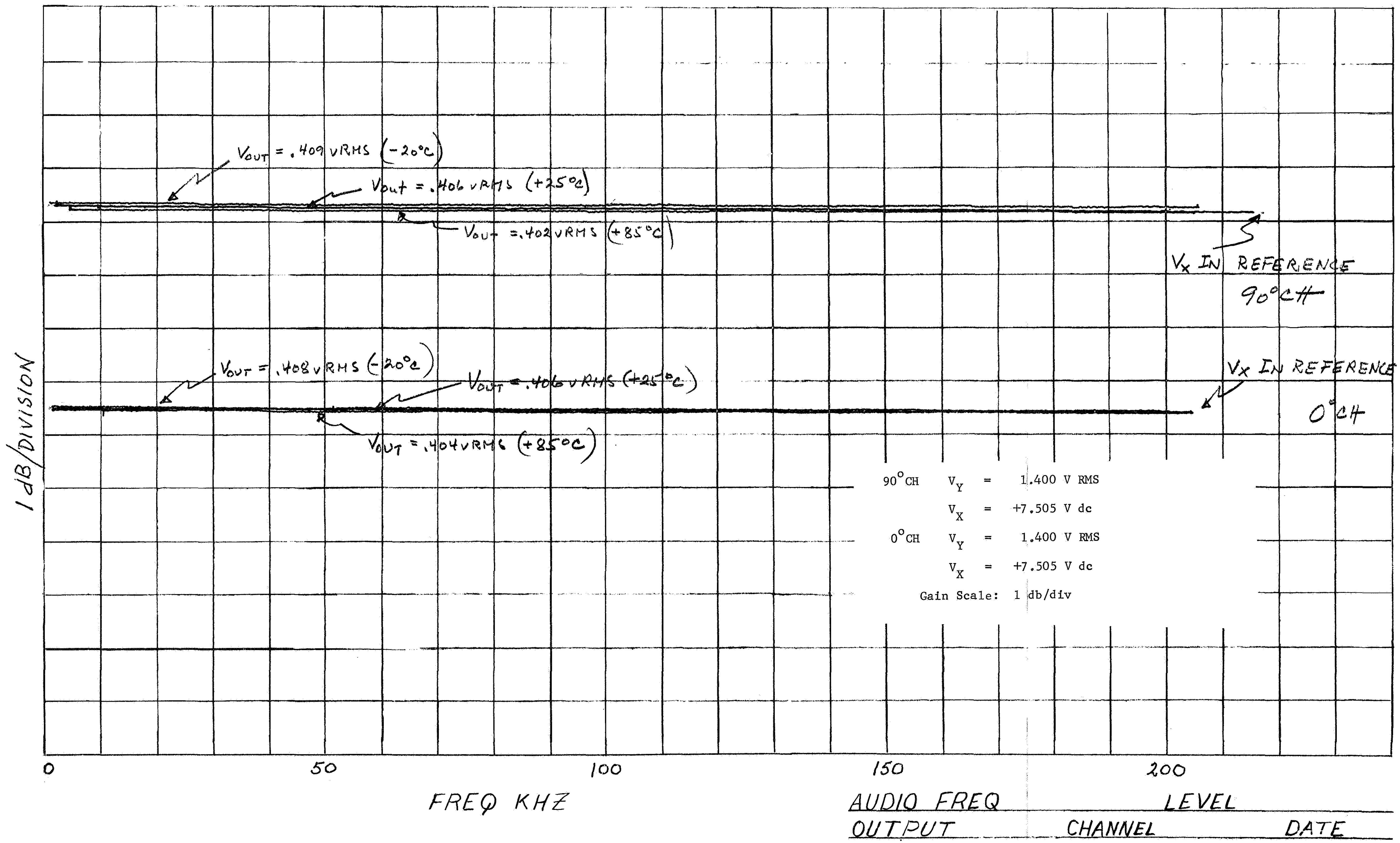

Figure 5.14
Modulator Frequency Response X-Input

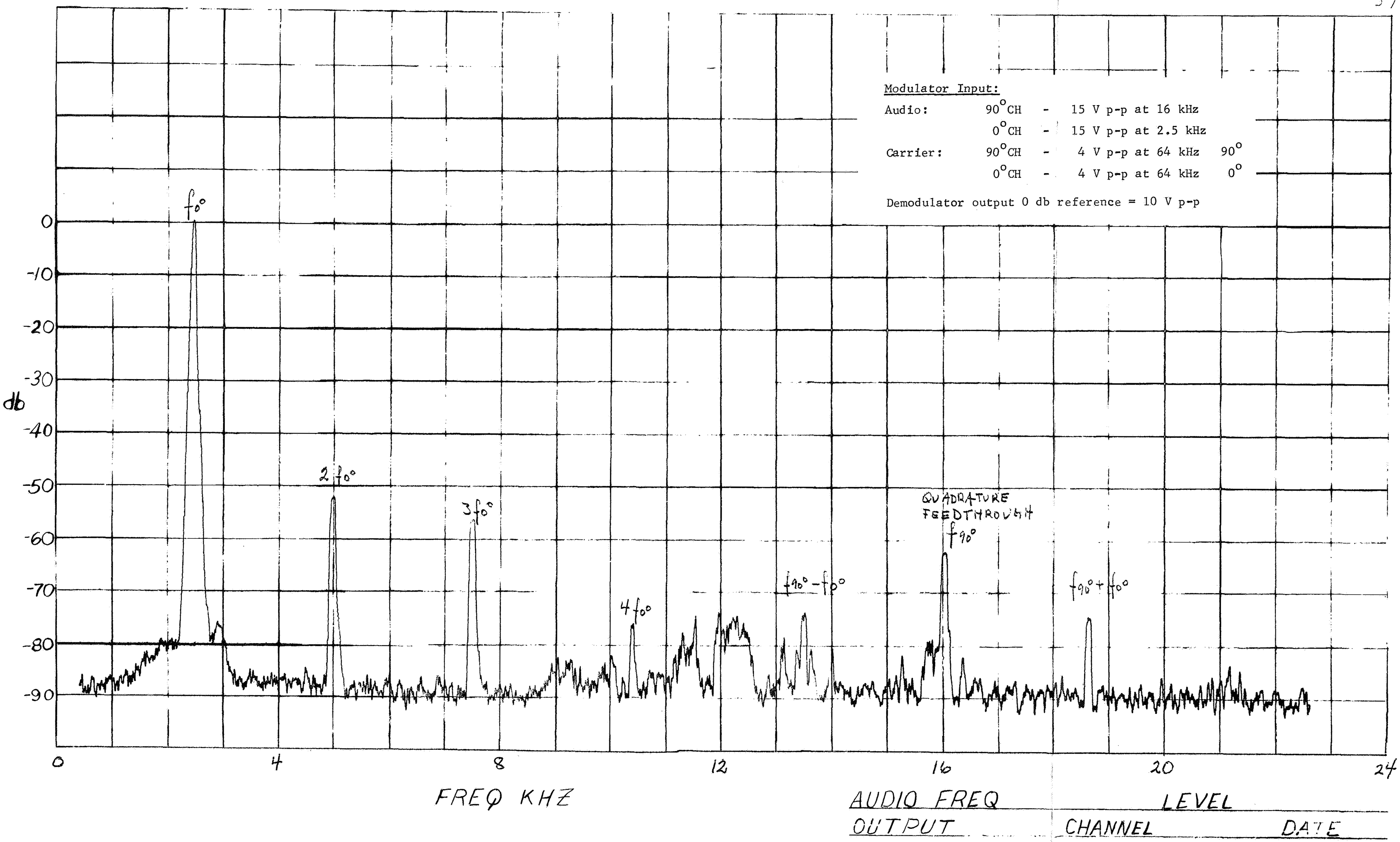

Figure 5.1
Demodulator Distortion Products an
Null Voltages, 0^{o}CH

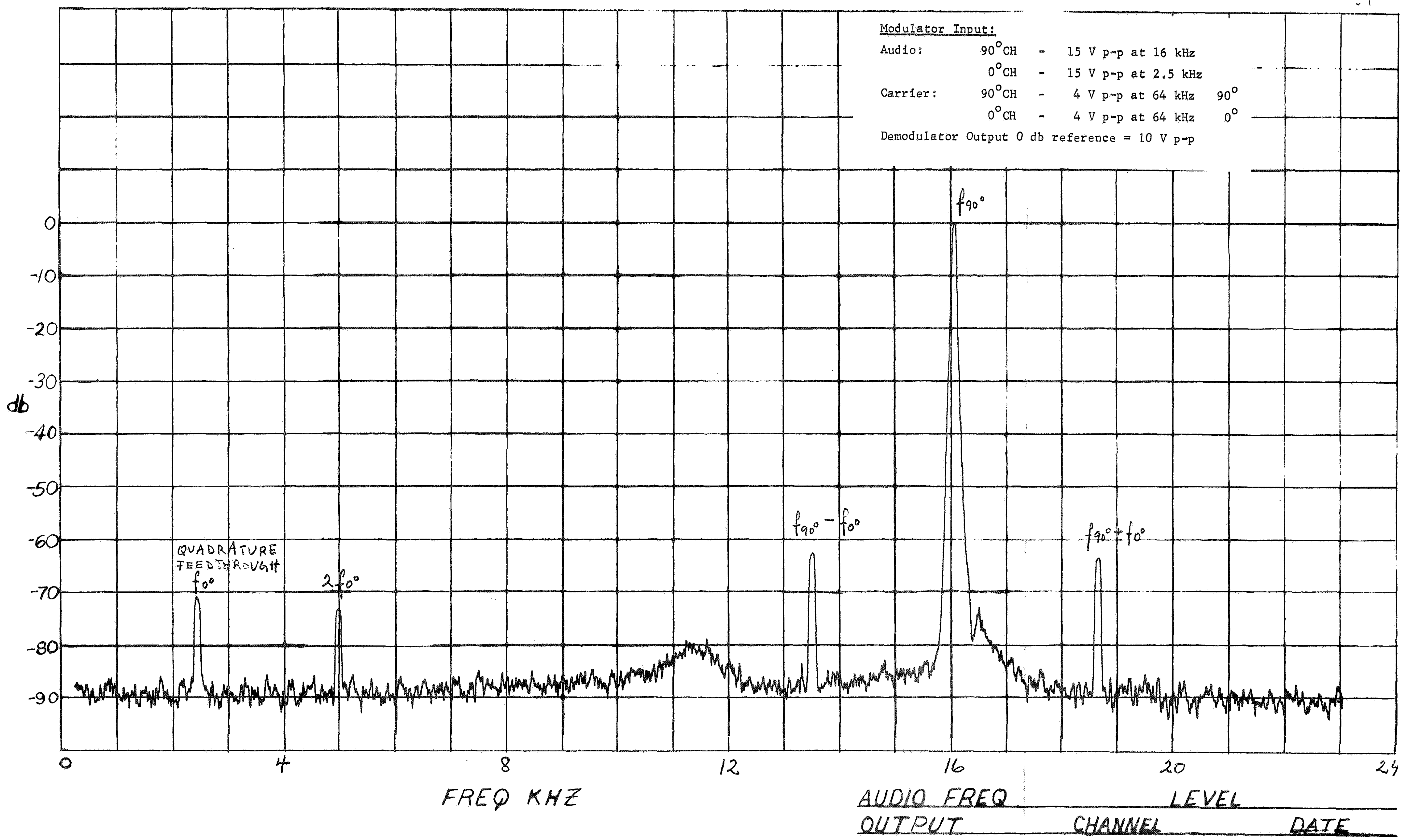

Figure 5.16
Demodulator Distortion Products
and Null Voltages, 90°CH

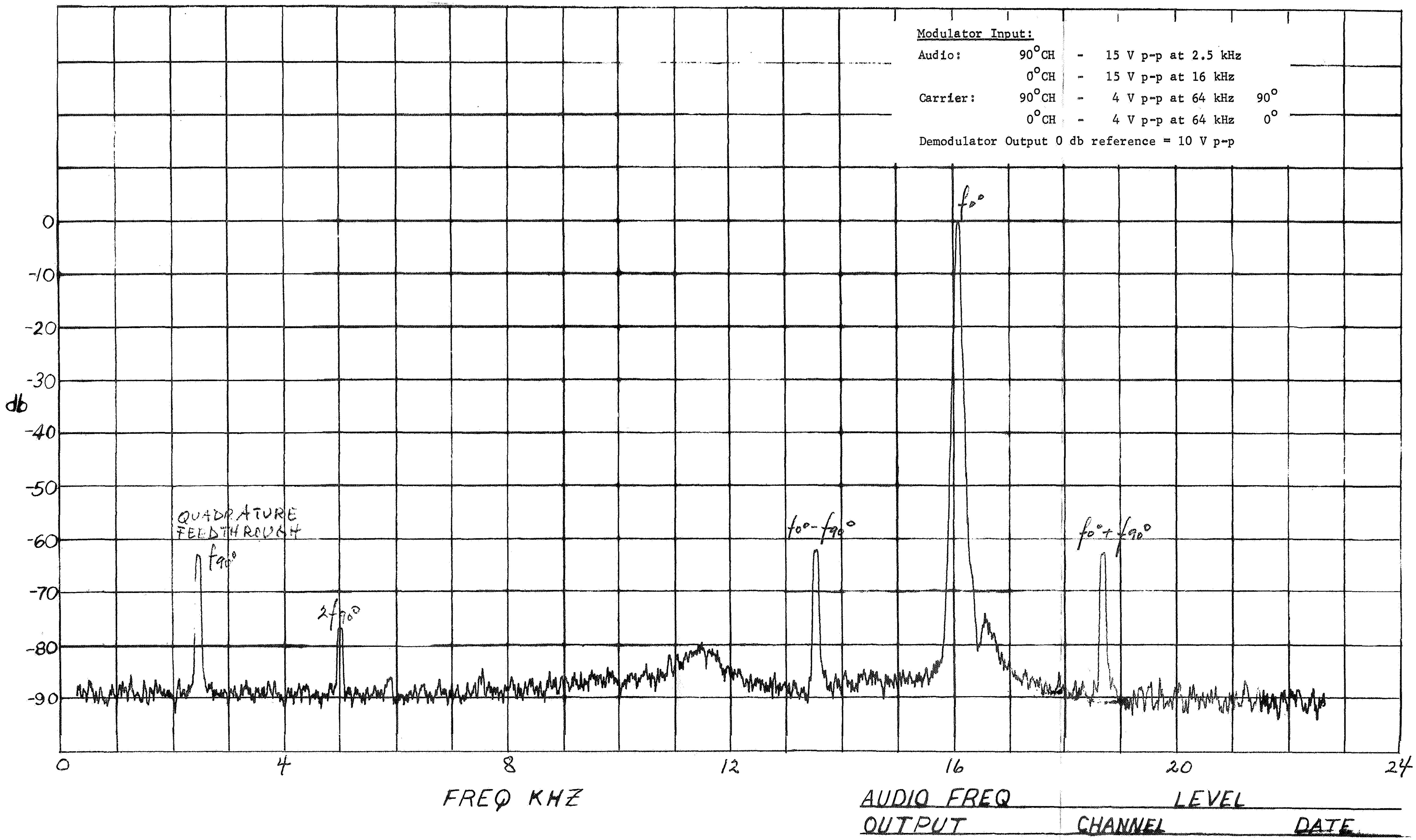

Figure 5.17
Demodulator Distortion Products
and Null Voltages, 0°CH

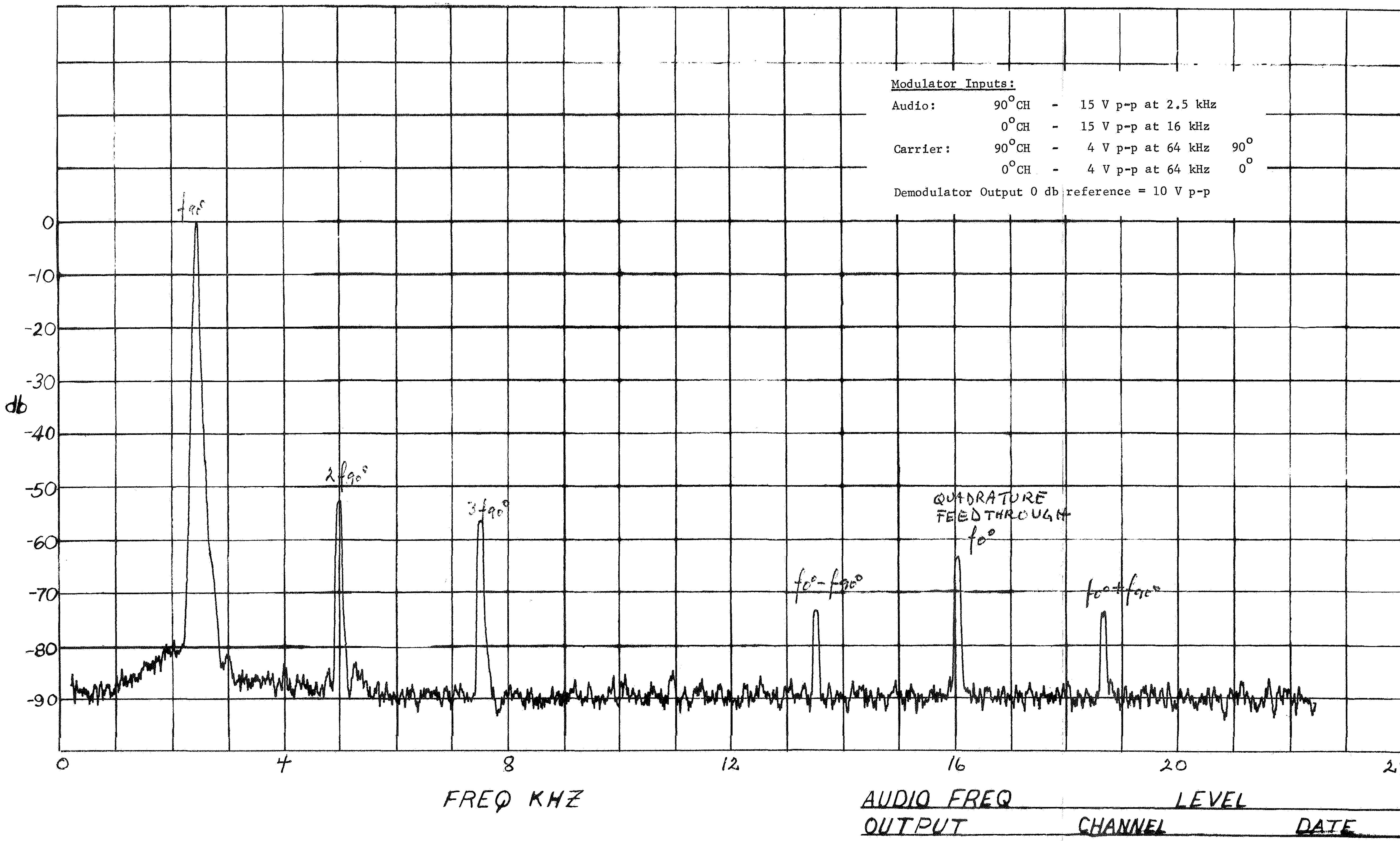

Figure 5.18
Demodulator Distortion Products and Null Voltages, 90°CH

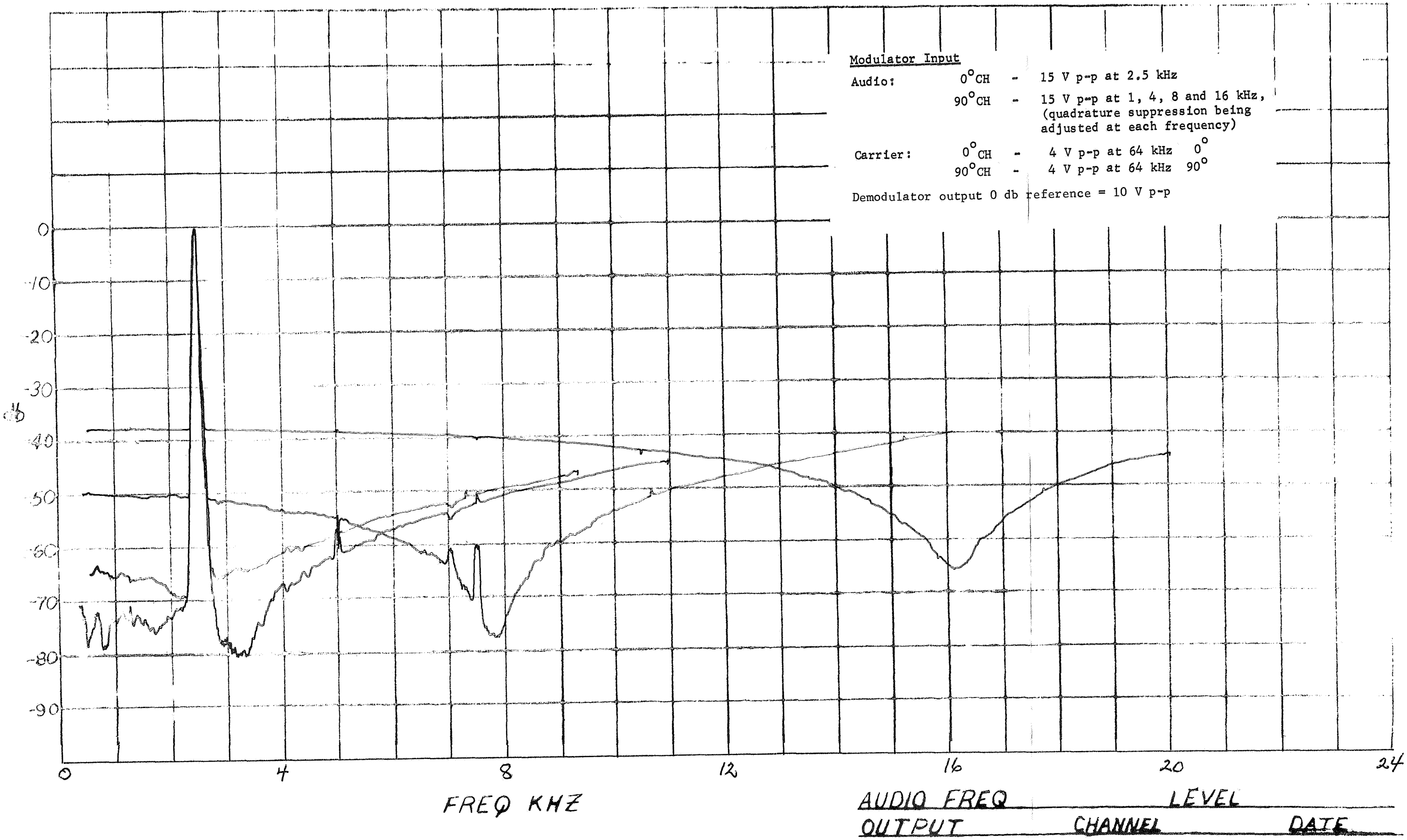

Figure 5.19
Demodulator Quadrature Feedthroug
0^{o}CH

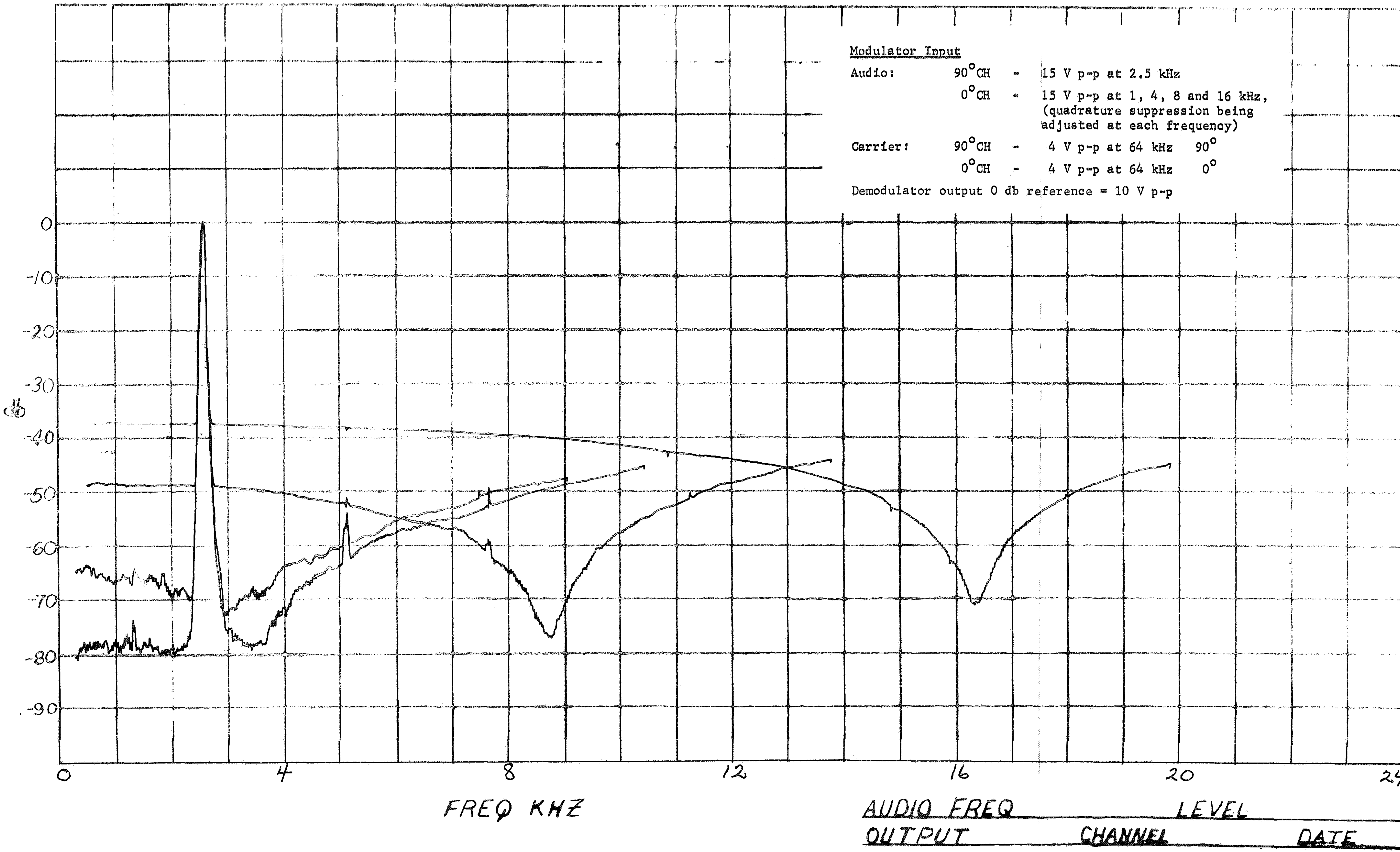

Figure 5.20
Demodulator Quadrature Feedthrough, 90°CH

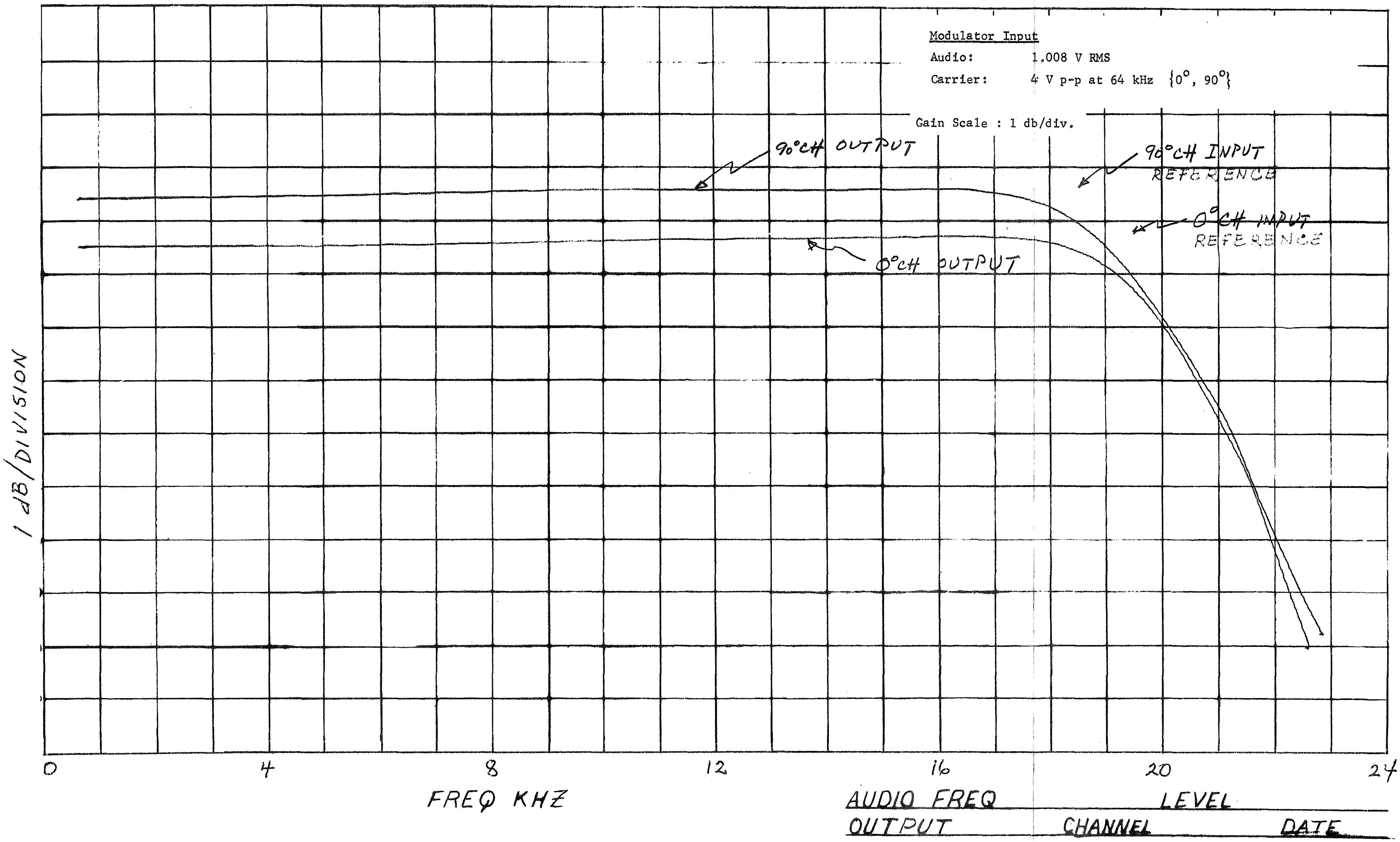

Figure 5.21
Demodulator Frequency Response

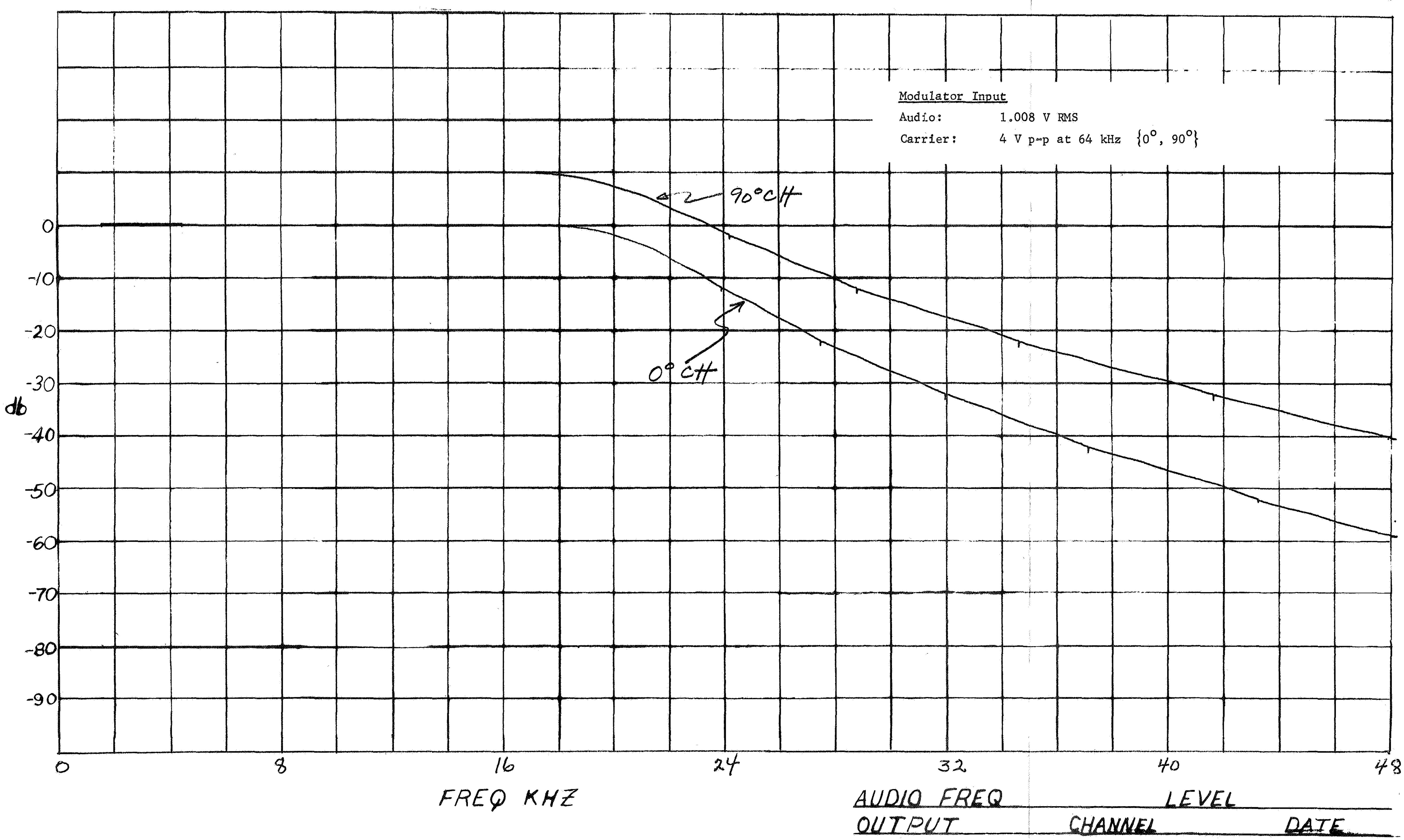

Figure 5.22
Demodulator Frequency Response

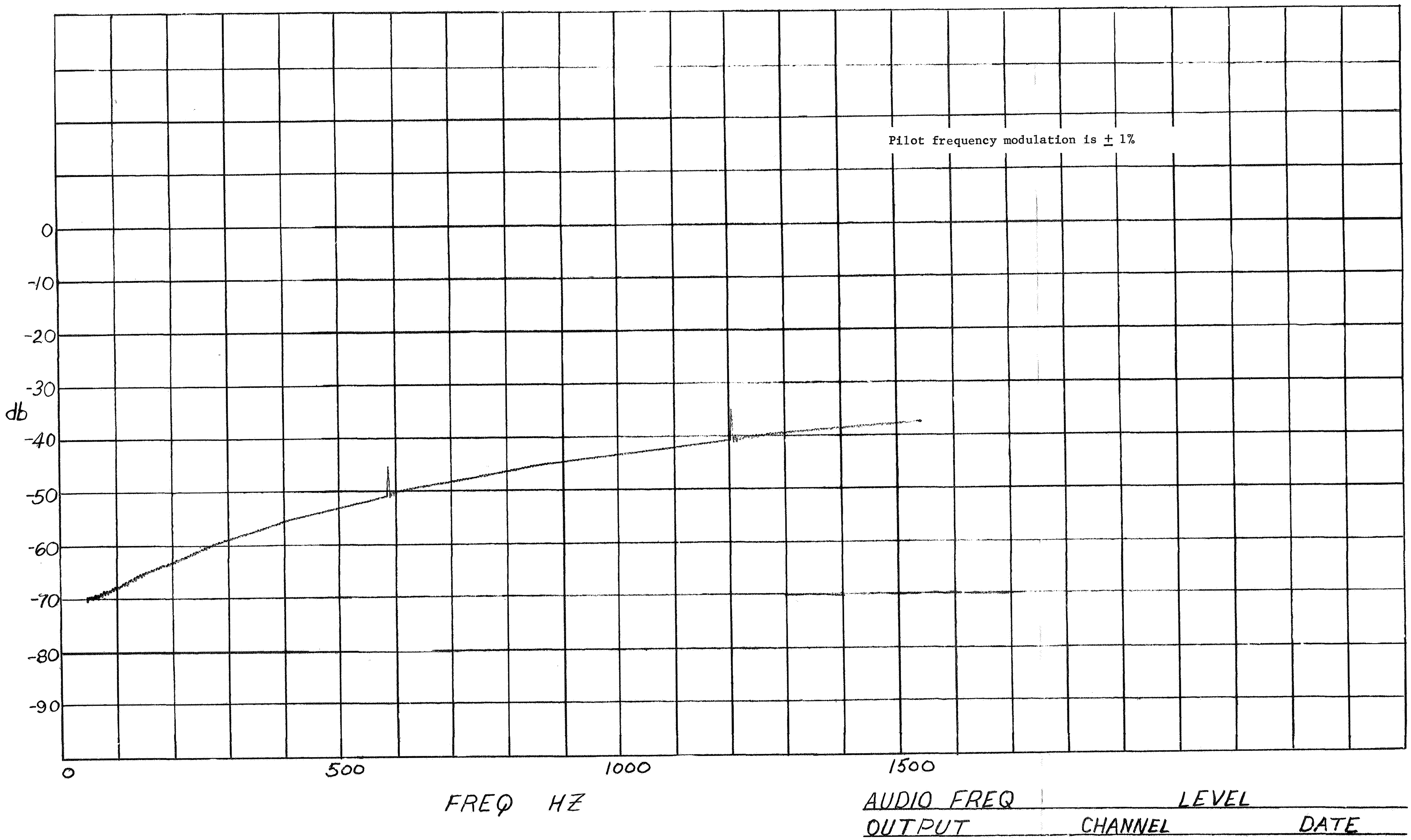

Figure 5.23
320 kHz Phase Locked Loop
Tracking Response

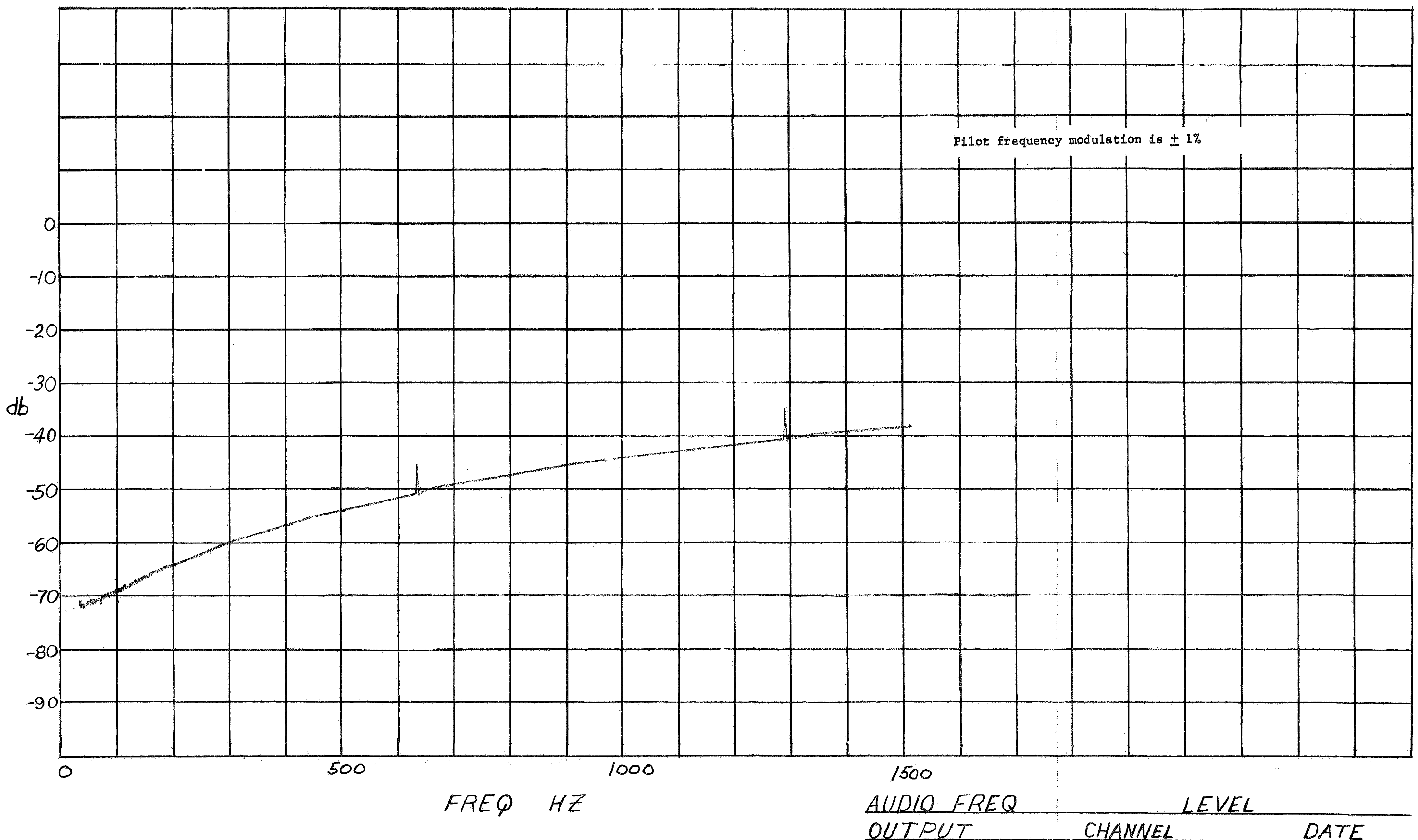

Figure 5.24
256 kHz Phase Locked Loop
Tracking Response

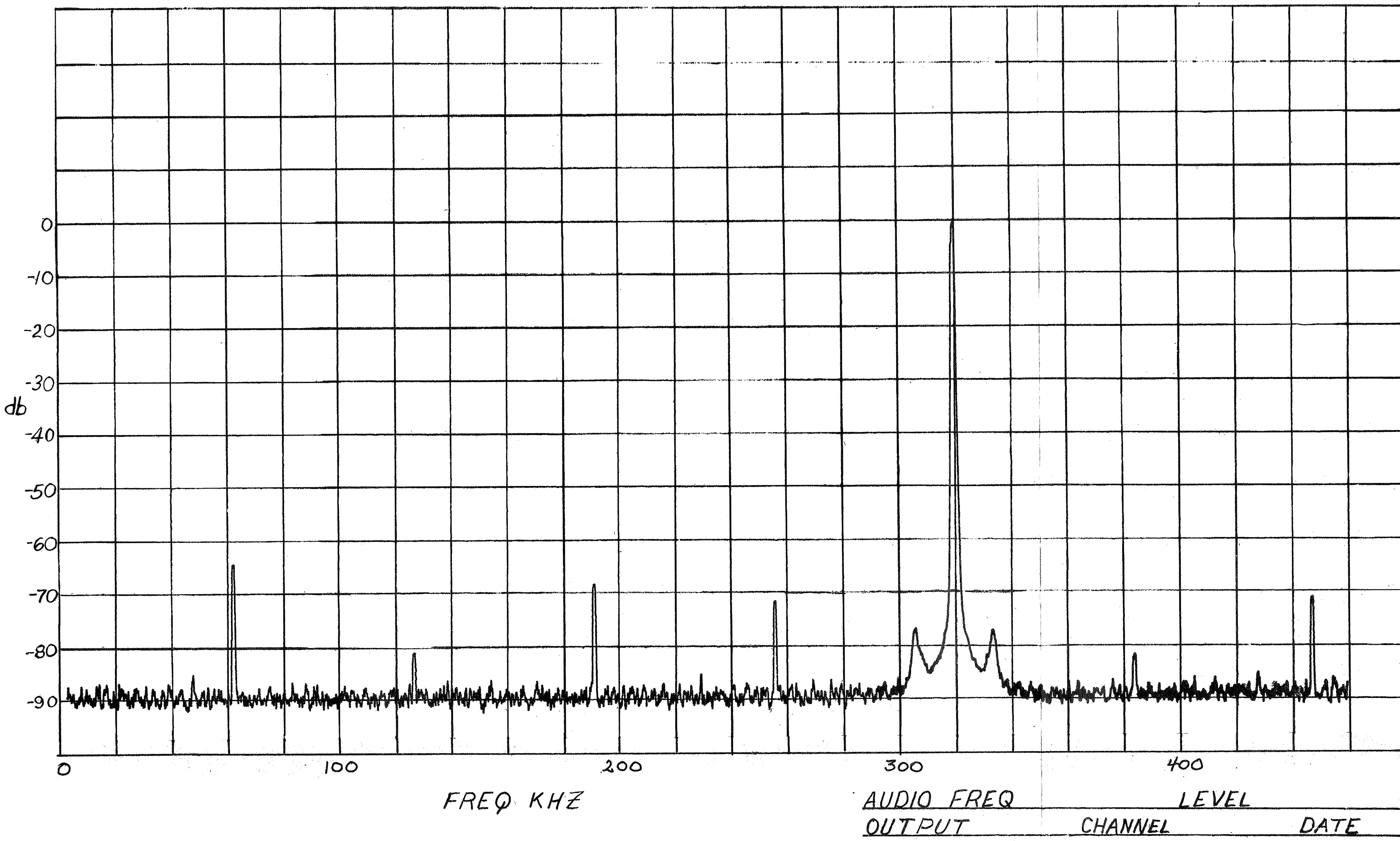

Figure 5.25
Frequency Spectrum of 320 kHz Output

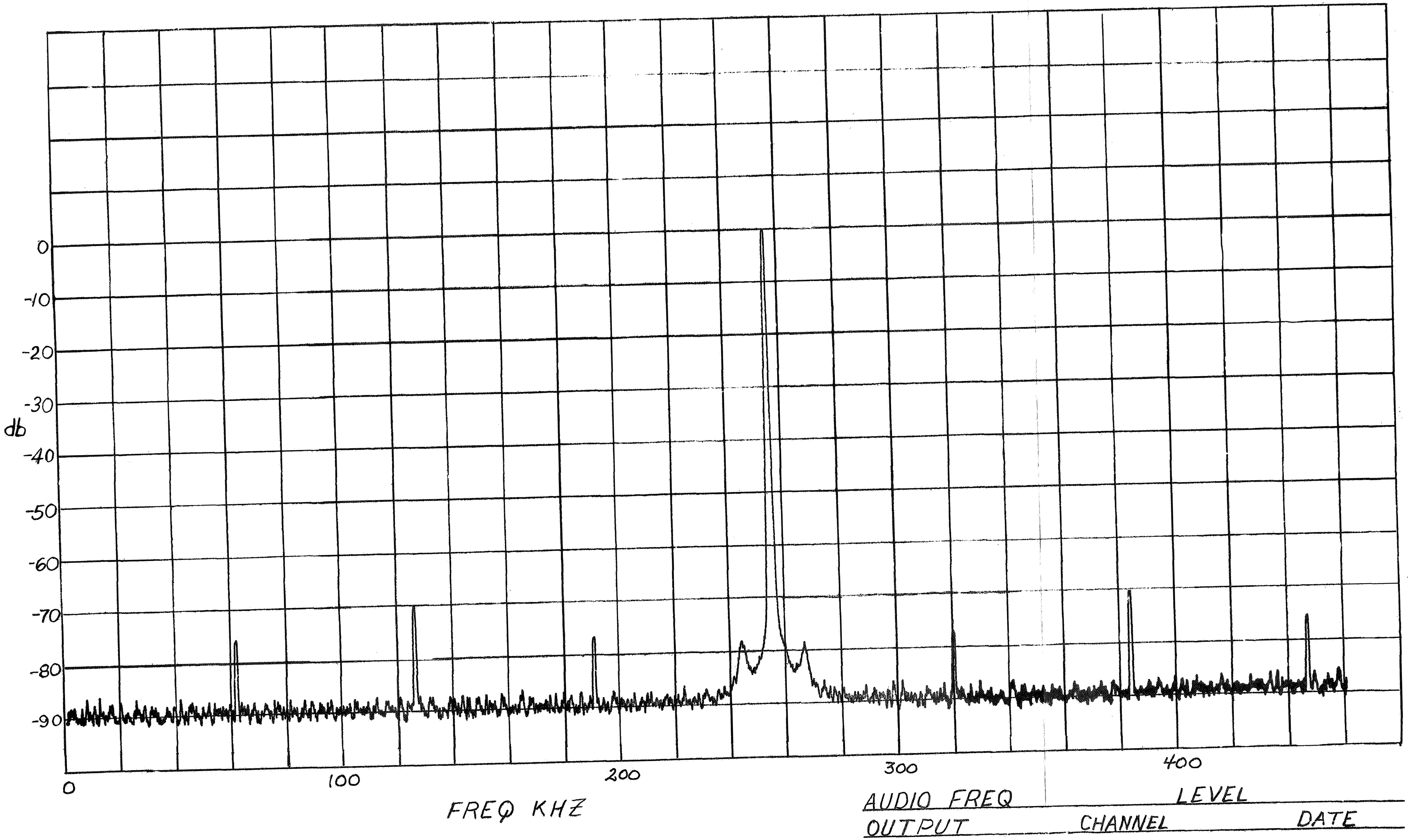

Figure 5.26
Frequency Spectrum of 256 kHz Output