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SILICON CONTROLLED RECTIFIERS WITH IMPROVED RADIATION RESISTANCE

BY

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PREPARED FOR

NATIONAL AERONATUICS AND SPACE ADMINISTRATION
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FINAL REPORT

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FOREWORD

The work described herein was conducted by the Semiconductor Products Department of the General Electric Company, Auburn, N. Y. under NASA Contract NAS3-11831. The project was directed by Julian F. Been, NASA Project Manager, Lewis Research Center, Cleveland, Ohio.

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ABSTRACT

A 600 volt, 475 ampere SCR was designed and optimized to improve the nuclear radiation resistance to exposures of 5×10^{13} nvt ($E_n > 0.1$ Mev) and 1×10^{6} rad (C). Theoretical device models were developed to analyze the SCR in a radiation environment and to predict consequent changes in device characteristics. Calculations were performed using numerical techniques to design a theoretically optimized structure characterized by a shallow diffused forward blocking junction, a narrow p-base and a highly sensitive gate using pilot triggering.

Fabrication of the above device was attempted, however, difficulties were encountered in producing devices which exhibited the desired blocking voltage. This resulted from non-uniformities in the shallow diffused junction. In order to obtain a reasonable blocking voltage yield, it was necessary to increase the diffusion depth of the forward blocking junction. Since the latter adversely affects the radiation resistance, it was concluded that a definite trade-off exists between radiation resistance and available processing technology required for high current SCRs.

TABLE OF CONTENTS

1. SUMMARY

The major objective of this work was to optimize the design of a 600 volt, 475 ampere SCR to improve the nuclear radiation resistance to exposures of 5×10^{13} nvt (E_n >0.1 Mev) and 1×10^{6} rads (C). An analytical study was performed to develop theoretical device models which would predict changes in device characteristics resulting from exposure to the above radiation levels. Numerical techniques were used to calculate the effects on the following device characteristics:

1) Reverse blocking characteristics
2) Forward blocking characteristics
3) Forward conduction characteristics
4) Gate trigger currents
5) Dynamic characteristics

The results of the calculations were used to optimize the device structure in the following manner:

1) The blocking voltage capability could be maintained by providing for increased depletion region spreading in the lightly doped n-base.

2) The n-base width could be optimized for minimal forward drop by judicious choice of the starting resistivity.

3) The gate characteristics could be improved by using a narrow p-base, selecting shallow diffusion profiles to create a high built-in field to aid minority carrier transport, increasing the lateral resistance in the p-base to increase the gate sensitivity, and using pilot gate triggering to establish high gate currents in the main SCR.

A major conclusion of this effort was that processing technology was not available to fabricate the desired structure. It was necessary to change the structure of the device predicted theoretically to one which could be fabricated using state-of-the-art processing technology.

2. INTRODUCTION

Since its commercial introduction approximately ten years ago, the silicon controlled rectifier (SCR) has become the workhorse in the field of power conversion and control. More recently, however, military and space applications often require such a solid state switch to have characteristics which do not change significantly when exposed to radiation environments.

As a result of a vast amount of research into the effects of electron, gamma, neutron, and heavy charged particle radiation fields upon semiconductors and metals (see, for example, Reference 1), it has become well established that sufficiently large doses of such radiation can cause both temporary and permanent changes in the characteristics of solid state devices. Early work (References 2-4) in connection with the radiation resistance of SCRs indicated a rapid degradation of the electrical characteristics of these devices. Wilson et al. (Reference 5), however, showed that the degradation observed in pnpn devices is actually less than found in bipolar transistors having comparable base widths. In contrast to previous work (References 2-5) associated primarily with commercially available SCRs, the purpose of this contract was to analyze, design, fabricate, and test SCRs which have been optimized for use in radiation environments. In particular, this program was directed toward the realization of SCRs capable of operation in a neutron environment of 5×10^{13} nvt ($E_n > 0.1$ Mev) and a gamma radiation field of 1×10^6 rads (C). The program consisted of three phases: (1) to perform an analytical study to optimize the design and materials of SCRs having improved radiation tolerance; (2) to design and fabricate a very high current SCR toward the realization of the objective specifications outlined in Appendix A, and having improved resistance to the above radiation

environment; and (3) to test the electrical characteristics of the SCRs, along with the bulk properties of representative samples of the devices prior to their exposure to a reactor radiation environment by NASA-LEWIS Research Center, Cleveland, Ohio.

The remainder of this report is divided into seven (7) sections. Section Three (3) is concerned with radiation effects in silicon and change in crystal properties. Section Four (4) presents the device analysis and considers the effects of the radiation damage on device characteristics, while Section Five (5) makes use of these results to formulate an optimized device design. Section Six (6) is concerned with processing and processing problems incurred during fabrication of the optimized device. Section Seven (7) presents the test results of the fabricated devices and compares these results to the objective device specifications. The remainder of the report, Sections Eight (8) and Nine (9), summarizes the results from the total effort and presents conclusions and recommendations for future work.

3. RADIATION EFFECTS IN SILICON

3.1 Introduction

The net effect of radiation upon a silicon crystal is damage due to collisions between incident high-energy particles and atoms of the material, and also subsequent collisions caused by both the high-energy particles and the recoiling atoms. The physical interaction involved in the collision is dependent upon the type of incident particle. For electrons and heavy charged particles, coulomb forces are dominant, while for neutrons, the interaction is due to collisions between the nucleus of an atom and the neutron. In the case of gamma radiation, electrons are produced by the Compton effect and coulomb forces then govern the electron's subsequent collisions. If as a result of such an interaction, the recoiling atom receives sufficient energy to be displaced from its equilibrium site in the lattice into an interstitial site, a vacancy is formed. It has been established that the basic event, which causes radiation damage in silicon, is the formation of the vacancy-interstitial pair. Of course, the actual damage can be much more complicated, depending upon the energy and direction of the incident particle. Both interstitials and vacancies are extremely mobile at room and even cryogenic temperatures. They also show a great affinity to each other and to the defects and impurity atoms, such as oxygen, existing in the crystal prior to irradiation. Therefore, although the basic damage event is the formation of a vacancy-interstitial pair, the actual result of damage from one or more incident particles is the formation of vacancy-interstitial, di-interstitial, di-vacancy, and vacancy-donor, vacancy-defect and interstitial-defect pairs, as well

as many others. These single defects and pairs affect the electrical properties of the crystal by the formation of additional energy levels in the forbidden energy gap. Since these energy levels may be either shallow or deep level sites, they may act as donors, acceptors or recombination centers. Thus, one might expect possible changes in the conductivity and minority carrier lifetime of the crystal. In addition, since the radiation damage represents a perturbation of the periodicity of the crystal lattice, one might also expect a decrease in the carrier mobilities, which, of course, also affects the conductivity of the crystal. The formation of additional energy levels is also expected at the surface of the crystal, thus affecting its surface mobility, conductivity and lifetime. In general, the extent of the damage is dependent upon (1) the type, energy and direction of the incident particle, (2) the concentration of defect and impurities and their type existing in the crystal prior to irradiation, and (3) the degree of annealing experienced by the crystal after irradiation.

3.2 Displacement Effects on Lifetime

The most significant change to semiconductor crystal properties caused by radiation is the degradation of minority carrier lifetime. As discussed briefly in Section 3.1, this degradation results from the addition of energy levels near the middle of the band gap, by defects and defect clusters. These additional energy levels act as recombination centers and will reduce the minority carrier lifetime in the crystal.

If one considers the recombination rate, R, which results from a given radiation fluence, ϕ, an expression of the form

$$R = R_o + K\phi \qquad (3.1)$$

is found[6]. Here R_o is the initial recombination rate and K is a damage constant which is dependent upon the type and energy of the radiation, the type and resistivity of the crystal, and even the effect of other impurities[7]. It can be seen that the final recombination rate R, and hence the lifetime, τ, is a function of both the initial lifetime and the radiation fluence.

The radiation environment specified in this contract is a neutron fluence of 5×10^{13} nvt (E_n >.1 Mev) and a gamma dose of 1×10^6 Rads (C). However, based upon results published in the literature[6,14] we have concluded that the displacement effects of the above gamma dose will not exceed ten percent of that of the neutron fluence and, consequently, only the neutron dose was considered in calculations of lifetime as a function of radiation fluence.

In order to calculate the effects of neutron radiation upon the minority carrier lifetime in silicon, a computer program was written. This program assumes the two level model of Hall, Shockley, and Read[8,9] to predict the effect of gold recombination centers on the initial lifetime and assumes the two level model and the capture probabilities given by Messenger[10] to predict the effect of neutron radiation. (A complete formulation is included in Appendix B). The results from this program can be seen on the curve in Figure 3.1.

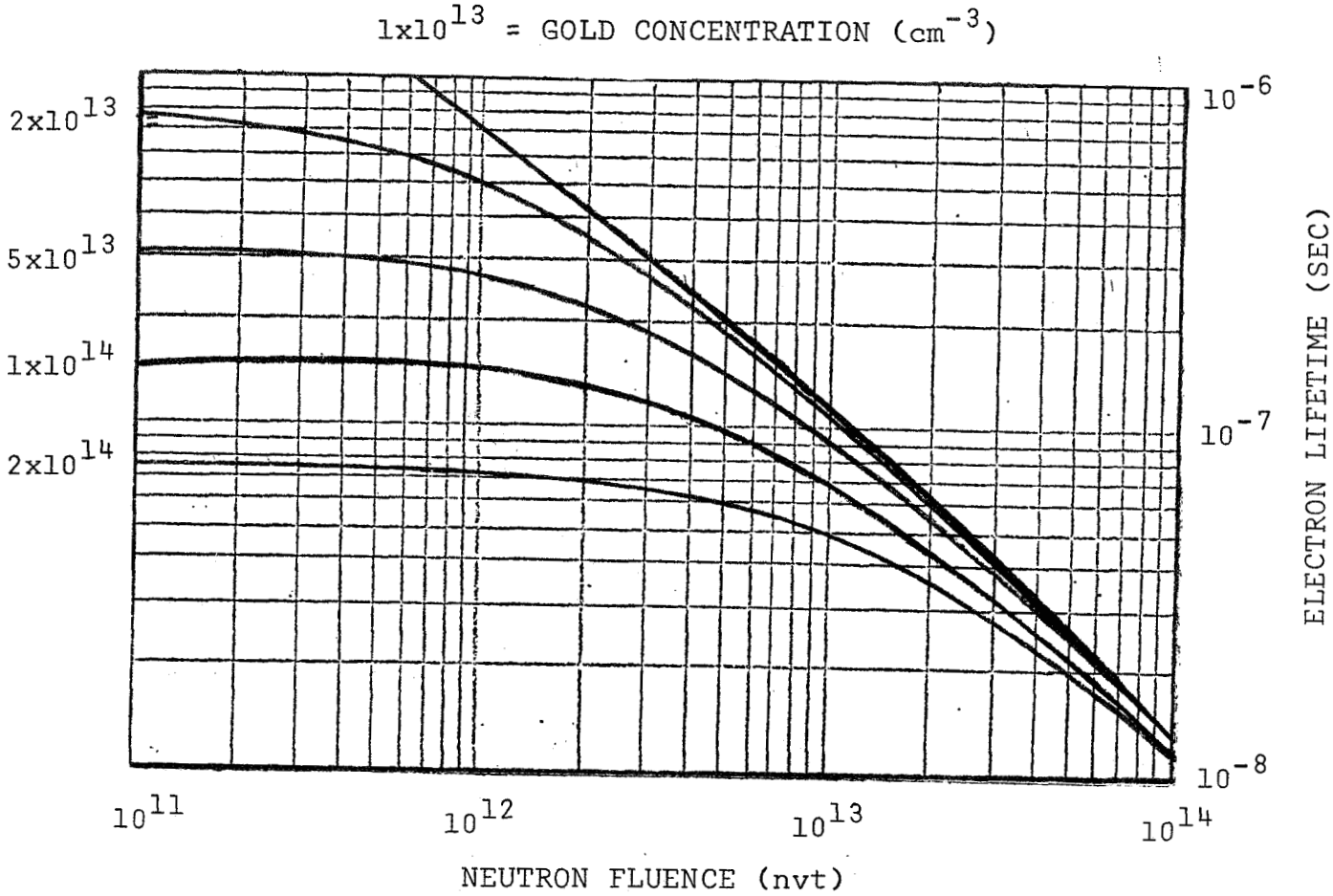


Figure 3.1 Minority Carrier Lifetime as a Function of Neutron Fluence for Various Initial Gold Concentrations.

Computer calculations by Gwyn et al.[11] using this approach have resulted in good agreement with measurements on transistors. Our calculations of high level lifetimes agree with the measurements of Wilson et al.[12].

3.3 Displacement Effects on Resistivity

Incident radiation can cause a change in the resistivity of silicon, especially in the high resistivity regions in much the same manner as gold can effect the resistivity. Energy levels created by

the radiation can capture majority carriers and thereby reduce the number of free carriers in the conduction band and raise the resistivity. This effect, called carrier removal, is especially noticeable when the density of damage centers approaches or surpasses the density of doping impurities.

The effect of neutron displacement damage on the carrier concentration can be given by the following equation

$$N = N_o - (\Delta N/\Delta\phi)\ \phi \qquad (3.2)$$

Here N_o is the initial carrier concentration, while the term $(\Delta N/\Delta\phi)$ is called the carrier removal rate. This rate has been measured by Curtis et al.[13] and varies between 1.0 and 4 carriers/n-cm for n-type silicon.

It is instructive at this point to step ahead and consider the change in resistivity expected on a typical 600 volt SCR in a 5×10^{13} nvt neutron environment. The base resistivity for this device would lie in the neighborhood of 20 ohm cm, which would correspond to a doping concentration of 2.4×10^{14} atoms/cm^3. If one assumes a carrier removal rate of 1.3/n-cm[6] then we have

$$N = 2.4 \times 10^{14} - (1.3)\ 5 \times 10^{13}$$

$$= 1.75 \times 10^{14} \ .$$

This corresponds to a change in carrier concentration of 27%. Buehler[15] has summarized carrier removal data and has presented curves of resistivity versus neutron fluence. The data fits the empirical relationship

$$n(\phi) = N_o \exp(-\phi/K) \qquad (3.3)$$

where K has been determined by Buehler as

$$K = 444\ N_o^{0.77} \text{ for n-type silicon.}$$

Using Equation 3.3 results in a change of 38% in carrier concentration. These figures will be used in the discussion of blocking characteristics.

4. DEVICE ANALYSIS

4.1 Introduction

The analysis of thyristor characteristics has been the subject of considerable study in past years. The earliest approaches used classical techniques in order to gain an understanding of device operation. However, in the effort to produce tractable equations, simplifying assumptions are necessary and often result in an inaccurate prediction of device characteristics. More recently, the analysis of thyristor characteristics has been treated numerically[20, 24,30,31,32]. In these cases, fewer assumptions are necessary, and the predictions are more accurate.

In consideration of this previous work, it seemed most promising to use numerical techniques in the optimization of the thyristor for radiation resistance. This work will be presented in this section. The objective is to present the model and simplified equations used in these analyses, so that a clear understanding of the effect of radiation on device characteristics can be developed. The detailed discussion of the specific numerical calculations will not be presented, although the results from these calculations will be used extensively in the design of the thyristor, Section 5.

4.2 Reverse Blocking Characteristics

In order to analyze an SCR for reverse blocking, consider Figure 4.1. Here an SCR is pictured with two junctions reverse biased, and the center junction forward biased.

If one considers the doping concentrations of the emitter base junction J3, one will see that this junction will have a limited blocking voltage capability in comparison to Junction J1. Therefore, the assumption is made that J3 will have no effect on the blocking

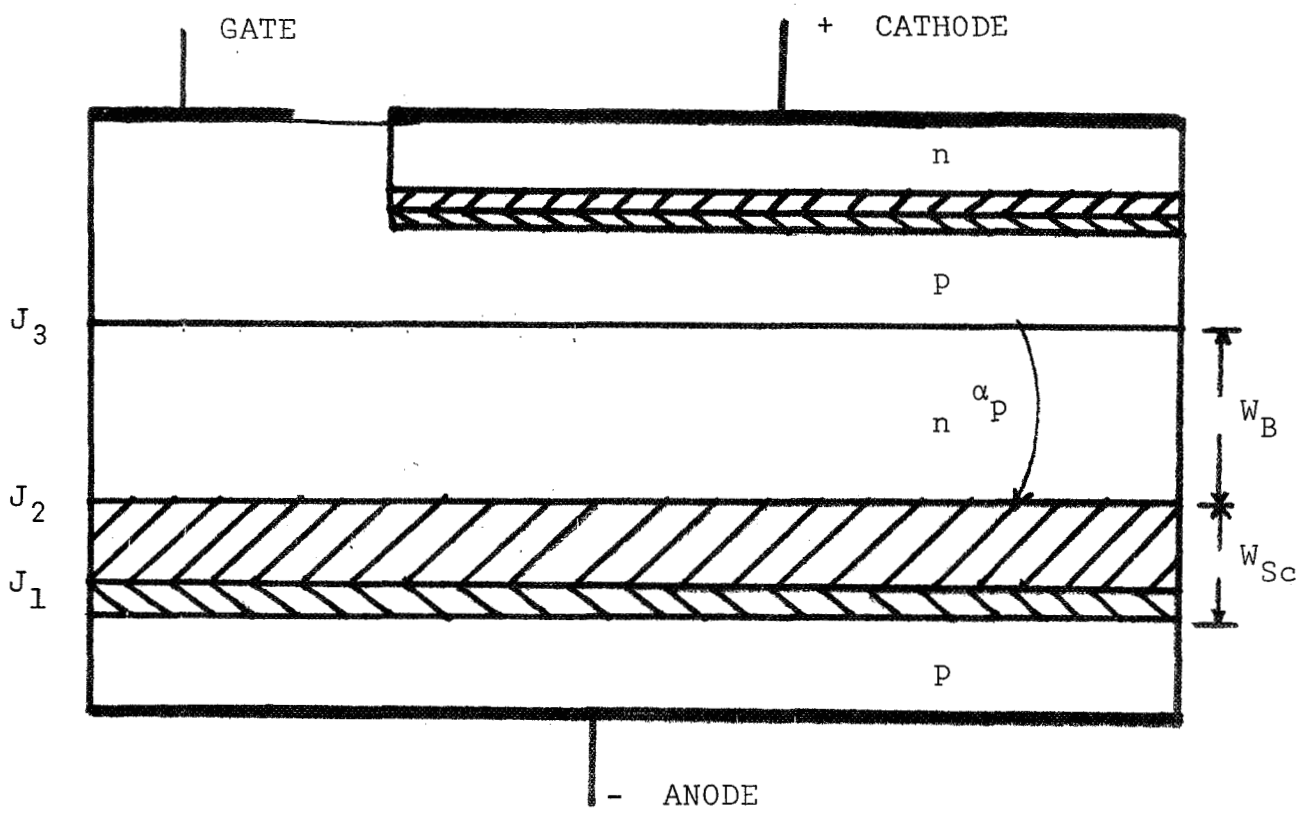


Figure 4.1 Model For Reverse Blocking SCR

characteristics of the SCR. Consequently, the main blocking junction is J1, the one adjacent to the high resistivity n-base region. From an equivalent circuit point of view, the model becomes one of a pnp transistor exhibiting a current gain, α_p, in series with an avalanche diode.

The reverse blocking current which flows through the SCR can be expressed by Equation 4.1.[16]

$$I_R = \frac{I_o}{1 - M_p \alpha_p} \tag{4.1}$$

Here, I_o, the junction leakage current, is a function of voltage and is given by[16]

$$I_o = M_n I_{dn} + M_p I_{dp} + M_{sc} I_{sc} \tag{4.2}$$

where M_n, M_p, and M_{sc} are the avalanche multiplication factors associated with electron, hole, and space charge generated currents, respectively. Also, I_{dn} and I_{dp} are the electron and hole diffusion currents, and I_{sc} is the space charge generated current. The current gain, α_p, is a function of voltage and can be approximated by[17]

$$\alpha_p = \gamma_1 \, \mathrm{SECH} \, \frac{W_B}{L_p} \tag{4.3}$$

where W_B is a function of voltage. While α_p is current dependent, the current levels of interest are normally below the point where the current dependence of α_p becomes significant. The current dependence can therefore be neglected for a simple analysis. This will play a significant role, however, in the forward blocking analysis.

According to the assumptions presented in Section 3, only changes in lifetime and resistivity need be considered to see the effects of radiation on the device characteristics.

Decreasing lifetime results from the formation of additional recombination centers in the silicon lattice. In the depletion region of a reverse biased junction, they act as generation centers and contribute an increased space charge generated leakage current to the total diffusion current. This space charge generated current is proportional to the space charge region width and, therefore, is higher for high voltage structures with higher base resistivity and, consequently, greater depletion region widths.

An increase in base resistivity by carrier removal will cause an increase in the depletion region spreading and will increase the avalanche voltage if the n-base is sufficiently wide to prevent punchthrough. If, on the other hand, a punchthrough condition is reached before avalanche, then the effective blocking voltage capability decreases. Since the percentage change in resistivity (or carrier concentration) is greater for higher resistivity material for a given radiation fluence, (see Equation 3.1), it is evident that the higher voltage devices are more likely to have their voltage capability impaired because of punchthrough than are lower voltage structures.

The numerical solution for the reverse blocking characteristics assumes a complementary error function profile for all diffused regions. Average majority carrier concentrations are calculated based upon these numbers. The lifetimes, mobilities, diffusion lengths, and minority carrier concentrations are calculated in each region based upon the assumptions presented in Appendix B. Also, depletion region widths for the blocking junction are calculated on both n and p sides as a function of applied voltage, along with the corresponding avalanche multiplication factors (see Appendix B). To calculate the current voltage characteristic, Equation 4.1 is calculated for voltages ranging from low values to avalanche. In

this calculation the current gain is calculated as a function of voltage and current (also discussed in Appendix B), and the calculation therefore predicts the negative resistance region associated with typical breakdown characteristics of transistors. It should be noted that the model for these calculations includes temperature dependence. However, the assumption is made that the temperature is sufficiently high to ionize all impurities.

4.3 Forward Blocking Characteristics

The most simple model which can be used to analyze the forward blocking characteristics of an SCR is one assuming a one dimensional analysis and continuous emitters. In this case, the equations and results for the blocking currents and voltages are very similar in form to those found in the reverse blocking analysis. However, this analysis is not valid for most high current SCRs, as continuous emitters are not generally used. It has been shown[18] that a shorted emitter structure improves the dynamic and high temperature characteristics considerably by controlling the effective emitter efficiency of the cathode junction. The analysis of a shorted structure requires a two dimensional model which considers lateral current flow.

In the following section both the continuous emitter and the shorted emitter structures will be analyzed. The one dimensional model will be discussed first, since it forms the basis for the subsequent analysis of the shorted structure.

In the analysis of the forward blocking characteristics for continuous emitters, the effect of two current gains must be considered, as pictured in Figure 4.2.

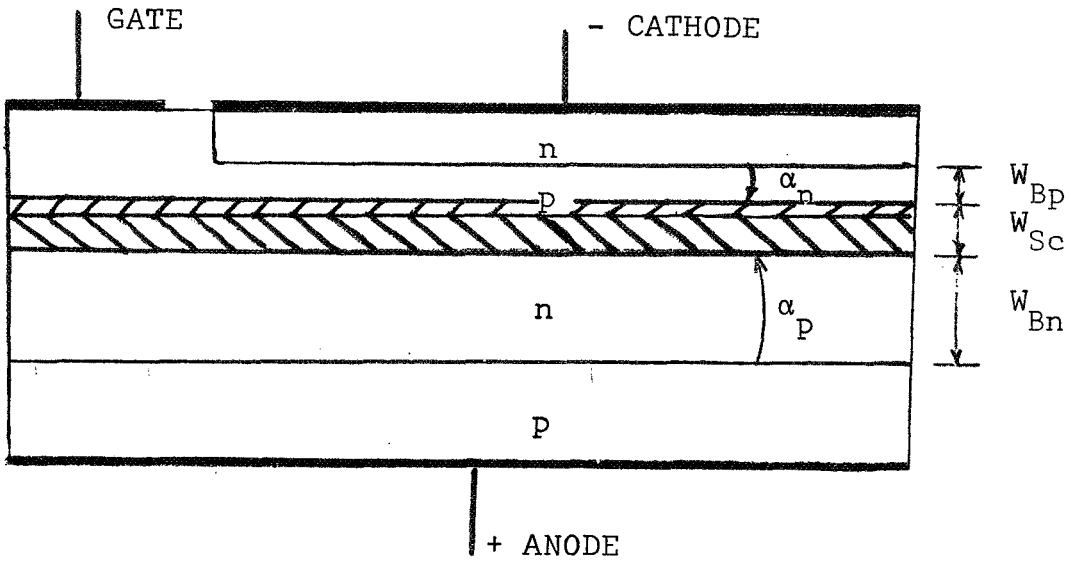


Figure 4.2 Model for Forward Blocking SCR with Continuous Emitter Junction.

An equation similar in form to Equation 4.1 is convenient to describe the current voltage relationship, namely[16],

$$I_f = \frac{I_o}{1 - M_p \alpha_p - M_n \alpha_n} \qquad (4.4)$$

The terms are the same as those defined in the previous section, except for α_p and α_n. In this case, the current dependencies must be taken into consideration.

If one considers α_p as a function of lifetime and current, a curve of the form of Figure 4.3 will be found. (A complete analysis of the lifetime and current dependence of α is found in the Appendix B).

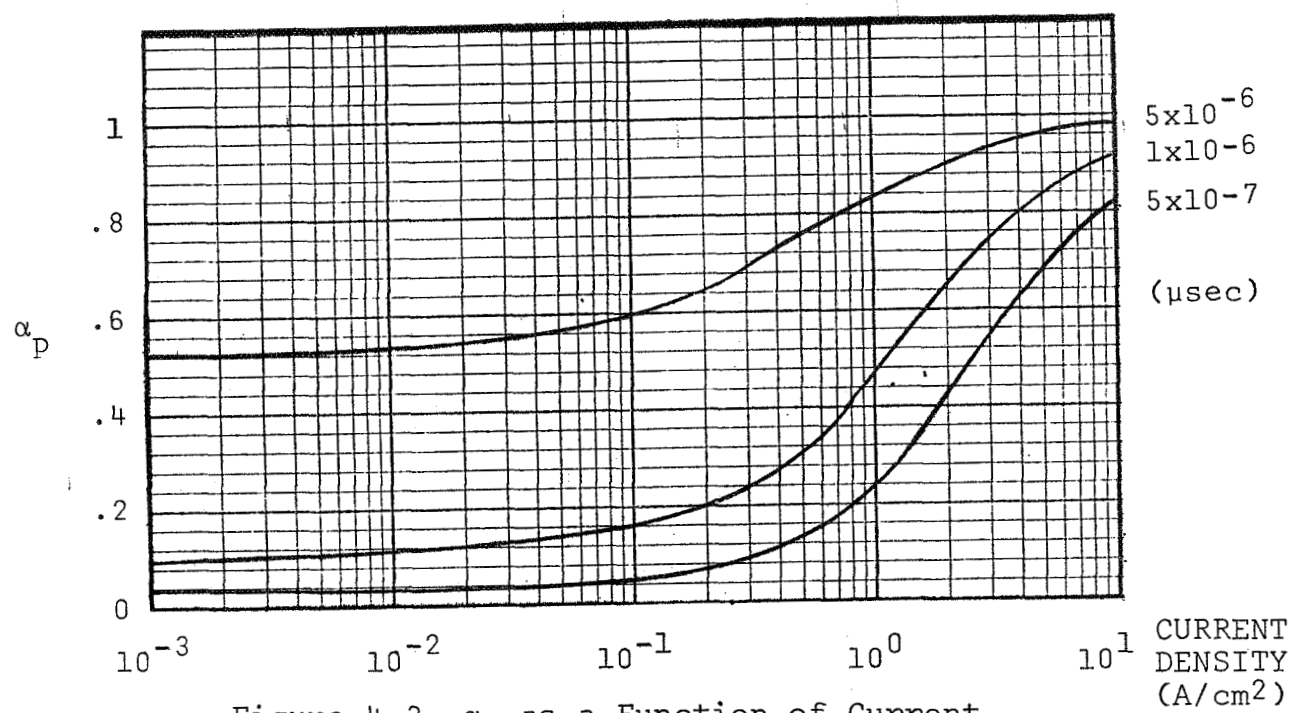


Figure 4.3 α_p as a Function of Current for Various Lifetimes Assuming Unity Injection Efficiency.

A knowledge of this function is necessary to predict the leakage current level and the point of turn-on.

The effects of radiation on the blocking characteristics are similar to the reverse case. In general, a decrease in lifetime will cause increase in leakage currents, while an increase in resistivity will cause the characteristic avalanche voltage to increase, but may cause the blocking voltage capability of the device to decrease by a punchthrough mechanism.

The difference between the forward and reverse characteristics is that in the forward case, as the blocking currents increase to a level $I_{(BR)}$, the device will turn-on and conduct current. The criterion for turn-on has been discussed by many authors[16,21,22] and can be expressed by the equation below.

$$\alpha_n + \alpha_p \geq 1 \qquad (4.5)$$

By inspection of Equation 4.4, one can see that as the sum of the current gains approachs unity, the forward blocking current will become large. Since both alphas increase as the total forward blocking current increases by Equation 4.4, the point will be reached

where Equation 4.5 is satisfied, and the device will turn on. To investigate the effect of lifetime on the turn-on point, one must only consider the effect of lifetime on the current gains. Since the current gain decreases with decreasing lifetime, the current at which the sum of the alphas equal unity will occur at a higher level.

It is important to note that in the above discussion of the current gains unity injection efficiency has been assumed, and since $\alpha = \gamma\beta$, the discussion has, in reality, only been concerned with the transport factor,β. However, the injection efficiency is also a function of current. At low levels recombination in the forward bias depletion region of an emitting junction results in an injection efficiency, γ, of much less than unity. The injection efficiency will increase with increasing current, because the effect of the recombination becomes small.

In the analysis of emitter efficiency, one other consideration is necessary as a result of the physical construction of a typical high power SCR. It has been found that the high temperature characteristics and the dv/dt capability of a thyristor can be improved significantly through the use of a shorted emitter structure[18] as shown in Figure 4.4.

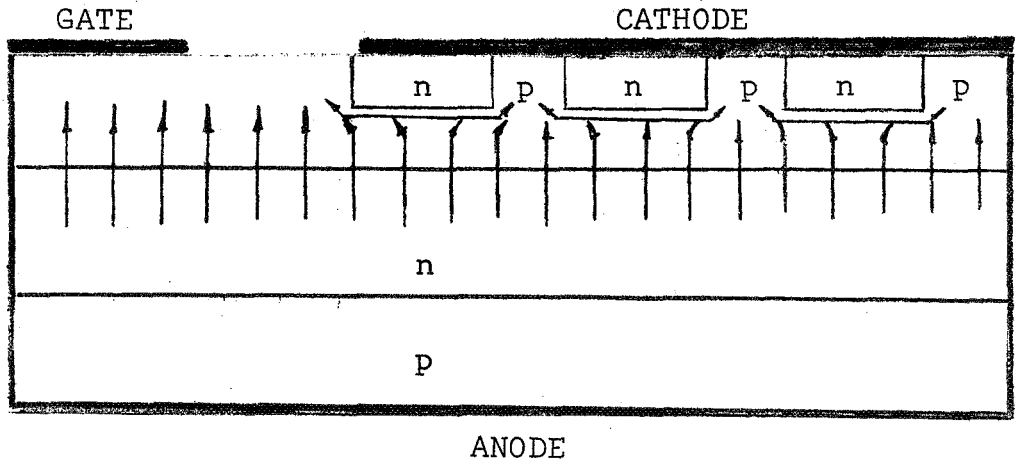


Figure 4.4 SCR With Shorted Emitter Structure.

In this case, the effective injection efficiency and its current dependence is controlled by the length of the emitter, the lateral resistance under the emitter, and the ratio of the total short to emitter area. Since the emitter is shorted by low resistance p regions, it is not forward biased at low current levels and, therefore, exhibits a low effective injection efficiency. However, as the current through the device increases, lateral currents flow under the emitter region and create a lateral bias, which begins to forward bias the center most portion of the emitter. As the lateral currents become sufficiently large, the emitter will become forward biased, and the device will turn on. From the above discussion, one can see that current flow is in two directions, and that the one dimensional analysis of the continuous emitter model does not strictly apply. In order to calculate accurate numbers, these lateral currents must be taken into consideration. This has been accomplished in two ways. The simpler way is to assume an effective emitter efficiency, based upon the short geometry, lifetime and diffusion profiles, and to use the one dimensional analysis with the assumed value of the injection efficiency to calculate the forward blocking characteristics. The more accurate procedure, however, is to perform an analysis of the lateral currents and their effect on device characteristics. Both have been done.

The computer analysis for the one dimensional forward blocking SCR with continuous emitter is almost identical to the analysis for the reverse blocking characteristic. In this case, however, Equation 4.4 is used, which included the effects of both alphas. The alphas are calculated as functions of current, voltage and lifetime where an effective emitter efficiency is assumed. The accuracy of the solution, therefore, becomes directly related to the correctness of the assumed injection efficiency.

To eliminate this inaccuracy, a two dimensional analysis was developed. In this analysis the lateral base bias is calculated under the emitter of the device, and the conventional diode equation determines the degree of forward bias of the junction and, consequently, the injection level. The remainder of this analysis is similar to both the forward and reverse cases, since the structure contains both pnpn and pnp regions, as is evident from Figure 4.4. The detailed model and equations are presented in Appendix C, since they are not necessary to gain insight into the effect of lifetime and resistivity changes on the blocking characteristics of thyristors.

4.4 Forward Conduction Characteristics

Many of the device parameters that affect the blocking characteristics of an SCR also affect the conducting characteristics so that of particular interest are the effects on the forward conduction drop, V_T, and the holding current, I_H. These will be discussed in the following sections.

4.4.1 Forward Conducting Voltage

When the sum of the alphas of the pnpn structure illustrated in Figure 4.2 equals unity, the device will be in its forward conduction state. In this state all three p-n junctions of the device will be forward biased. The forward voltage drop of the device is then a result of these junction drops, the ohmic drops in each region of the device, and the voltage drops at the metal to semiconductor contacts. The forward characteristic of a p-n-p-n device has been analyzed by Kokosa[20] using an abrupt junction model and including the effects of carrier-carrier scattering, conductivity modulation and the dependence of emitter efficiency upon current density.

As a result of this analysis, several conclusions are available concerning the forward drop of an SCR. The forward drop of an SCR under surge conditions is primarily in the wide lightly doped n-type

base. The voltage drop across this n-type base is proportional to $(W/2L)^2$ where W is the base width and L is the ambipolar diffusion length[23]. This relation applies for base widths much less than the diffusion length. The voltage drop becomes proportional to exp(W/2L) for base widths much larger than the diffusion length. This dependence upon the ambipolar diffusion length dictates a major trade-off between surge-current capability and radiation resistance. Decrease in lifetime can result in an exponential increase in forward drop. Therefore, it is important to obtain the minimum base width and the optimum voltage drop in the base, so that the current rating and the surge capability do not suffer drastically after irradiation.

It should be noted that during conduction the n-base is conductivity modulated. The resulting voltage drop is therefore dependent only on the base width and lifetime and not the initial resistivity.

The numerical calculation for this analysis has been performed by Kokosa and is discussed in the literature[20]. It will therefore not be discussed here in detail. Though an abrupt junction model has been assumed, average concentrations are calculated from diffused profiles, as in the blocking analysis.

4.4.2 Holding Current

In the low current, or holding current region, one is not so much concerned with the voltage drop across the device as with the current level. The holding current is defined as that current below which the device reverts to the forward blocking state. The magnitude of the holding current is dependent upon the current dependence of the transistor current gains α_n and α_p as shown in Figure 4.2. As the gain of the npn transistor, α_n, is normally quite high, one is especially concerned about the current dependence of α_p.

In high voltage thyristors the base width, W_n, of the pnp portion is large to accommodate the depletion region spreading with applied voltage. However, since the low current gain associated with the pnp is given by

$$\alpha_p = \gamma \, \text{SECH} \frac{W_n}{L_p} \tag{4.3}$$

where $W_n >> L_p$, the low current α_p is quite small, even for unity injection efficiency, γ. This low α_p permits the thyristor to block in the forward direction. Now, if one considers the current dependence of α_p, a relationship similar to that in Figure 4.5 is found.

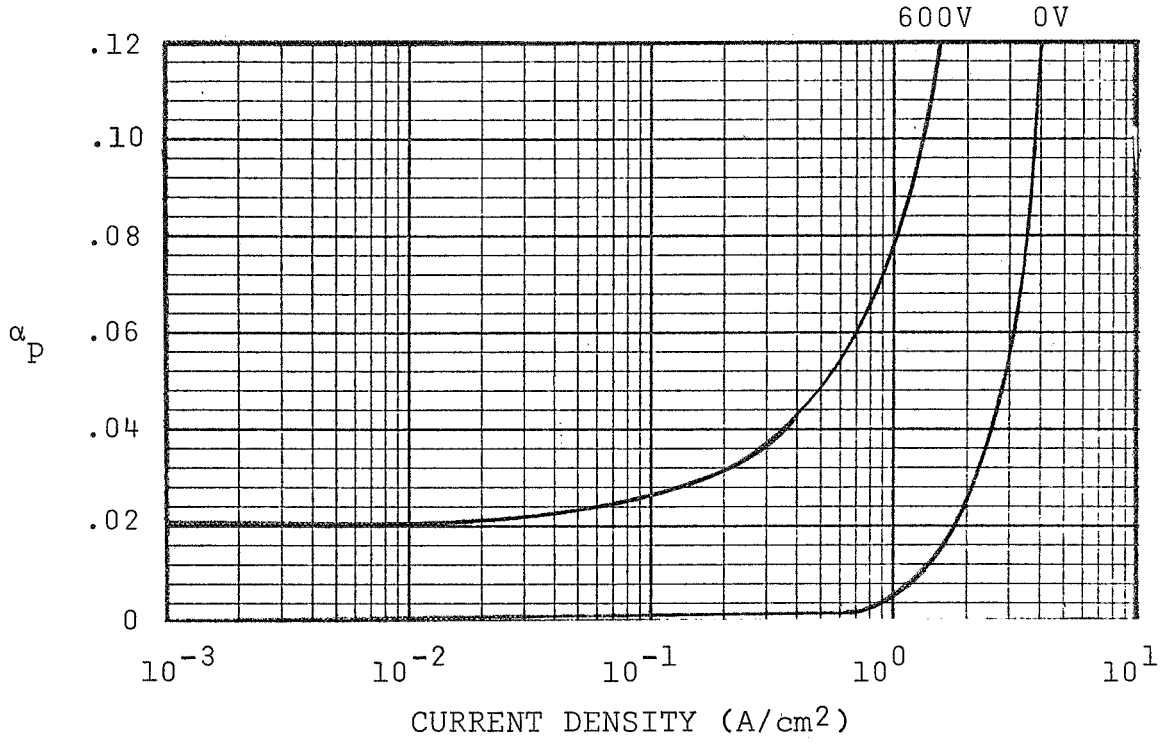


Figure 4.5 pnp Current Gain as a Function of Current for Blocking Voltages of 600 and 0 Volts. τ_p = .1 μsec

The condition which must be satisfied for conduction is the same as the turn-on condition that was discussed in the forward blocking section, namely:

$$\alpha_n + \alpha_p \geq 1 \tag{4.5}$$

If this condition is not maintained, the device will turn-off. If one assumes $\alpha_n = .9$, then $\alpha_p \geq .1$ for conduction. The current corresponding to the point on the curve just below $\alpha_p = .1$ then is the holding current.

The effect of lifetime and resistivity changes on holding current thus becomes a question of their effects on the current gains. Since α_n and α_p decrease with lifetime, it is evident from Figure 4.5 that the holding current will increase. The effect of increase in resistivity is a second order effect which depends explicitly upon the magnitude of the aiding field established as a result of majority carrier current flow in the base region. While, in general, the aiding field will increase and cause an increase in minority carrier transport, the specific result is dependent upon the specific structure and requires a detailed analysis (see Appendix B).

4.5 Gate Trigger Currents

Closely related to the subject of holding current is that of gate current, since the DC condition for turn-on, Equation 4.5, is identical for both cases. In the case of gate currents, however, one must also be concerned with the gain of the npn transistor, α_n, especially in the design for radiation resistance.

Consider the SCR in Figure 4.6.

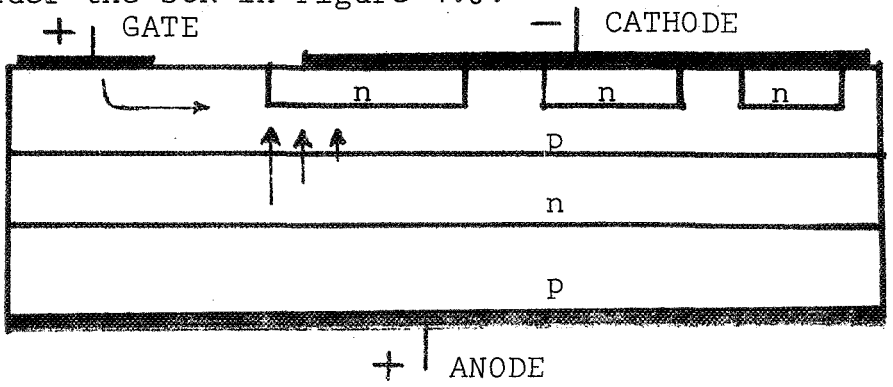


Figure 4.6 Conventional SCR

The total current flowing through the device, including the effects of gate current and current gains, can be described by the Equation below[2].

$$I_A = \frac{\alpha_n I_G + I_o}{1 - \alpha_n - \alpha_p} \qquad (4.6)$$

Here the effect of α_n becomes clear. As I_G increases, a quantity $\alpha_n I_G$ is collected at the n-base region, which becomes the drive for the pnp transistor, causing the current in the pnp to increase. Hence, by the curve in Figure 4.5, α_p increases, which further increases the total current I_A by Equation 4.6. This process continues until Equation 4.5 is satisfied, and the device turns on.

In order to analyze the effect of lifetime and resistivity changes on the gate characteristics, the two dimensional model discussed in the forward blocking analysis must be used. From Figure 4.6 it can be seen that turn-on results from the lateral flow of gate current under the emitter region to the short. This analysis was performed. The resultant numerical calculation is identical to the forward blocking calculation, except for the addition of the gate current term in Equation 4.6. The calculation is somewhat simpler, since the applied voltage is assumed constant.

4.6 Dynamic Characteristics

In considering the dynamic characteristics of a thyristor, one is concerned specifically with the dv/dt capability, the turn-off time, and the turn-on characteristics. In this case, both the dv/dt capability and turn-off time actually improve with decreasing lifetime, while the turn-on losses become greater. In fact, most switching thyristors are gold diffused specifically to improve the dynamic operation. As a result, analyses of the dynamic characteristics were

not treated in as great a detail as the previously discussed characteristics. They will be discussed here, so that one will gain an understanding of the device mechanisms.

4.6.1 dv/dt

Without the presence of excess charge in the bases left over from previous forward current, dv/dt triggering is caused by the displacement current required to charge the capacitance of the depletion layer during a rise in forward blocking voltage. If the current which results from charging the capacitance of the center junction is sufficiently great, the SCR will trigger to the conducting state. This problem is normally alleviated by using the shorted emitter structure discussed earlier. In this structure the displacement current is shunted around the emitter junction of the device through the low impedance short. Before this structure can trigger, the displacement current must be high enough to create a lateral base voltage sufficiently high to cause turn-on.

The dv/dt problem is interrelated with turn-off time and forward current, because the current through the device during a rapid rise of reapplied forward voltage is determined not only by the displacement current which flows through the center junction, but also by the minority carrier concentration stored within the base layers from a previous cycle. This collected current component depends on the forward current level and on the time interval from the peak of the forward current to the point at which the forward blocking voltage is reapplied (fall time, plus turn-off time).

The dv/dt capability is dependent upon the sensitivity of the npn section of the thyristor and may be increased in several ways. The density of shorts may be increased, thereby increasing the lateral current required to forward bias the emitter. However, this lowers the effective emitter area of the device, causing higher forward

dissipation and also reduces the sensitivity, causing higher gate currents. The lifetime in the device may be reduced, thereby reducing the npn current gain. Consequently, the dv/dt capability will improve with irradiation.

4.6.2 Turn-off Time

Turn-off time is a fundamental limitation on the repetition rate at which an SCR will function properly. Following conduction of current, both base layers of the device are heavily charged with excess minority and majority carriers. More correctly, the minority and majority carrier concentrations are many orders of magnitude higher than is the case in the reverse blocking condition. The problem is one of removing these carriers from the two bases, so that the center junction can block forward voltage. This can be accomplished by controlling minority carrier lifetime within the bases. Lowering the minority carrier lifetime permits the carriers within the base regions to recombine at a more rapid rate.

The conventional method uses gold doping to reduce the minority carrier lifetime and closely spaced emitter shorts to shunt the current, resulting from early application of dv/dt, around the cathode emitter. This method results in a turn-off time capability that is completely determined by the device. The same effect is observed from radiation. The minority lifetime is reduced and the turn-off time consequently improves.

4.6.3 Turn-on Characteristics

In order to achieve short turn-on time, rapidly rising current, and low turn-on losses, it is desirable to have the lifetime as high as possible. This is contradictory to good turn-off time and to the effects of radiation. In order to see this dependence, it is instructive to consider the dynamic turn-on process briefly.

The load current through an SCR does not immediately respond to the application of gate current (see Reference 24 for an analysis of delay and rise time). The gate must provide carriers to the p-base of the device, so that anode conduction begins. During this phase of turn-on, uniform injection along the periphery of the emitter is extremely important. Once sufficient charge has been injected into the device so that positive feedback between the two transistor portions of the device can begin, then charge within the bases builds up exponentially with time[15]. The accompanying current build up is determined by the transit time of carriers across the two bases, the minority carrier lifetimes, and the current density in the device. The transit time itself is governed by the base layer widths, the minority carrier lifetimes, and the current density.

While the above description of the turn-on process is correct, it must be realized that only a small portion of a high current SCR will turn-on initially, that being the region closest to the gate. The remainder of the SCR will turn-on by a spreading process[25,26,27] which requires a finite amount of time after the initial turn-on. During initial turn-on, a conventional SCR is susceptible to surge failure if the initial current and its rate-of-rise, (di/dt), is too high.

To aid in achieving very large gate currents, and to reduce the possibility of a di/dt failure, a two step triggering mechanism can be built internally to the SCR structure, as shown in Figure 4.7. This triggering scheme utilizes an amplifying thyristor[28] which triggers first and then conducts current from the anode to drive the gate region of the main conducting portion of the thyristor. This scheme allows the load circuit to provide the high current needed to drive a large initial turned-on area. A high lateral resistance in series with the pilot thyristor limits the peak dissipation in the pilot thyristor to a safe level. This type of triggering has advantages for radiation resistance, as will be seen in the following section.

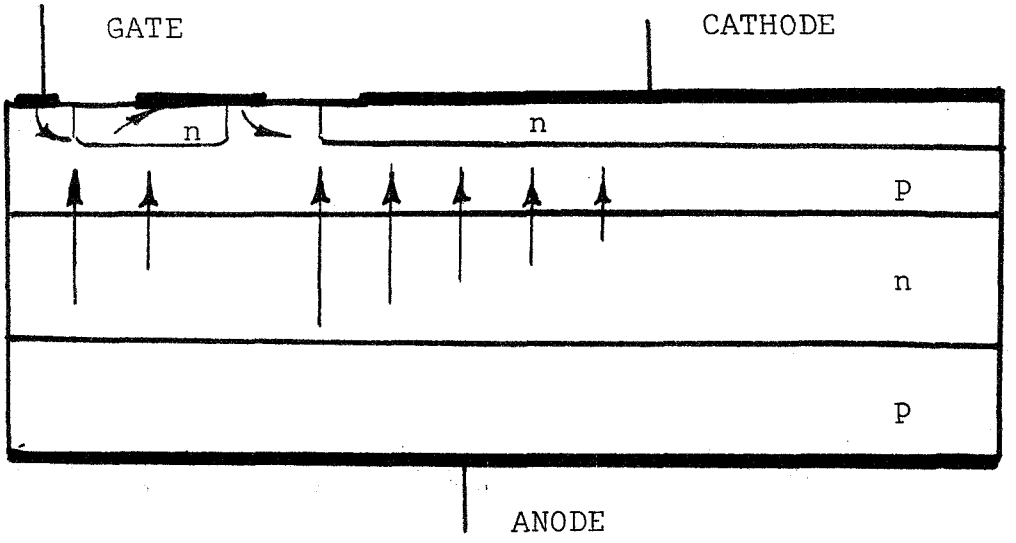


Figure 4.7 Amplifying Gate SCR

5. DEVICE DESIGN

5.1 Introduction

The effects of changes in lifetime and resistivity resulting from radiation on thyristor characteristics have been discussed in detail in the previous section. The task remaining is to use these results to design a device such that it is optimized for radiation resistance and yet still meets the objective device specifications listed in Appendix A. Before any design details are discussed, a thought should be given to the meaning of radiation resistance as applied specifically to thyristors.

With all the frills set aside, the major purpose of a thyristor is to function as a switch. This implies that it must possess an "off" state and, therefore, have the capability to block an applied voltage. It must also possess an "on" state, switch on with reasonable gate currents, and conduct a rated current without destruction. If the SCR cannot block voltage, or cannot switch with reasonable gate currents, then the device becomes useless and has failed for all practical purposes.

With this in mind, our main criterion in the design of a radiation resistant SCR was that the device must function after exposure to a radiation fluence of 5×10^{13} nvt and 1×10^{6} rads (C). In the following sections the philosophy and procedure behind the design of the device will be discussed. Curves which are representative of computer calculations will be presented and used to design the radiation resistant structure.

5.2 Design Philosophy

In order to design a thyristor so that the blocking voltage capability would not be degraded, the effect of carrier removal and increase in resistivity must be taken into consideration. This can be accomplished by designing the device with an n-base resistivity

lower than would normally be used to compensate for the expected rise in resistivity. In the same manner, the n-base width must be designed to be sufficiently wide to accommodate the increased space charge region spreading at the rated voltage without voltage degradation from punchthrough. It should be noted that the increase in base width is not favorable from a forward voltage drop consideration, especially at low lifetimes, since the forward dissipation will increase and the power handling capability will be impaired. It is therefore desirable to keep the base width minimal.

In order to meet the turn-on criterion for radiation resistance it is necessary to design the device with a high gain npn transistor component. In order for a thyristor to turn on, the npn transistor component must be able to transport minority carriers across the base region with reasonable gate currents. This can be accomplished in the following manner:

1) Diffuse the emitter junction deep enough to form a narrow p-base region.

   The turn-on sensitivity of an SCR is mostly determined by the gain of the npn transistor. This should be high even at low lifetimes. Since the gain can be approximated by Equation 5.1,

$$\alpha = \gamma \, \mathrm{SECH} \, \frac{W_p}{L_n} \qquad (5.1)$$

   a narrow base region will help the current gain at low lifetimes. The p-base region must be wide enough, however, to accommodate the depletion region spreading at the design voltage.

2) Diffuse a shallow forward blocking junction to establish a high built-in field in the p-base region.

   In a diffused junction a built-in field, E, is established as a result of the concentration gradient of the acceptor impurities, given by Equation 5.2,

$$E_x = \frac{kT}{qp} \frac{dp}{dx} \qquad (5.2)$$

where p is the majority carrier concentration and $\frac{dp}{dx}$ is the gradient of this concentration.

Since a steep gradient results from a shallow diffusion with a high surface concentration, this structure is desired for a high built-in field. In the p-base region of an SCR this field is in the direction to enhance the diffusion of minority carriers and, hence, to enhance the transport factor. Furthermore, it is independent of the lifetime of minority carriers and aids transport even at low lifetimes.

3) Diffuse steep concentration gradients near the emitter junction. To insure that the emitter junction will have a high injection efficiency at low lifetimes, it is essential that depletion region associated with the forward biased junction be narrow to reduce recombination of injected carriers. In graded junctions, resulting from deep diffusions, the depletion region will be large compared to abrupt junctions. Hence, shallow junctions approaching an abrupt profile are desirable. Steep gradients will also form high aiding fields as given by Equation 5.2.

4) Trigger with Pilot Gate

The gate sensitivity of an SCR is dependent upon the gate current density, since the carrier transport across the base region increases with current. However, the pilot is small in comparison to the main SCR, and high current densities can be created with reasonable gate current.

5) Gold Diffuse Heavily to Reduce Initial Device Sensitivity.

The blocking voltage and the dv/dt capability of a narrow base thyristor would be severely limited if the initial lifetime were not reduced. Gold in the device would reduce the lifetime, improving the blocking voltage and dv/dt capability, while degrading other characteristics, so that less change in device characteristics will occur after irradiation.

5.3 Design Procedure

The blocking voltage requirement places restrictions on the resistivity and the n-base width. However, since the forward voltage drop increases exponentially with n-base width, the resistivity should be selected such that the base width is minimal. In typical SCRs, this is straight forward. The resistivity is selected just high enough so the blocking voltage requirement can be met. The n-base width is then found by calculating the depletion region spreading for the maximum of the resistivity variation at design voltage. A length equal to two minority carrier diffusion lengths is also added to reduce punchthrough currents[33]. The total base width, W_B, can then be written.

$$W_B = W_{sc}(V,\rho) + 2\,L_p(\tau) \qquad (5.3)$$

Consequently, the base width is a function of voltage, resistivity, and lifetime.

In the design of a radiation resistant SCR, however, the situation is complicated by the influence of radiation on both resistivity and lifetime. Gold diffusion also affects the resistivity. Consequently, in the selection of the proper resistivity to obtain a minimum base width, one must consider these effects and detailed calculations are necessary.

The procedure for determining the minimum base width as a function of initial resistivity is summarized below:

1) Select a value of N_D, the doping concentration of the starting silicon, from the curve of avalanche breakdown voltages for a diffused p^+n junction in Figure 5.1.

2) Determine the effect of irradiation on the final base width, W_B' by:

   a) Calculating the effect of carrier removal on carrier concentration (resistivity) from Equation 2.2, as shown in Figure 5.2;

   b) Calculating the space charge region spreading, W_{sc}', at design voltage (720 volts);

   c) Calculating the minority carrier lifetime and, consequently, the diffusion length resulting from irradiation, as shown in Figure 5.3;

   d) Calculating the final base width from Equation 5.3.

3) Calculate the forward drop as a function of lifetime and base width, as in Figure 5.4. Then determine the minimum value of lifetime such that the initial V_f specification can be met for the base width W_B' (from Part 2).

4) Select an initial lifetime greater than that found in 3), and determine the initial base width, W_B, by:

   a) Calculating the effect of the initial lifetime (gold concentration) upon the starting resistivity, as in Figure 5.5;

   b) Calculating the space charge region spreading, W_{SC}, at design voltage;

   c) Calculating the diffusion length from the initial lifetime;

   d) Calculating the initial base width, W_B, from Equation 5.3.

5) Plot the value of W_B' and W_B as a function of N_D and repeat 1) - 4) above until a curve as shown in Figure 5.6 can be plotted.

The curve in Figure 5.6 provides the information necessary to select the initial resistivity and base width. The curve was plotted assuming an initial hole lifetime of .1 μsec from forward drop considerations. It can be seen that the minimum base width occurs at the highest concentration below avalanche breakdown. To allow for resistivity spreading and for process variations, a range of $N_D=2.5\times10^{14}-3.0\times10^{14}$ cm^{-3} was selected, which corresponds to a range of W_B' = 105-94 μmeters, respectively.

The remainder of the design is concerned with developing a high gain npn transistor component, so that the gate characteristics will be preserved at low lifetimes. This entails determining the diffusion profiles, such that conditions 1, 2, and 3 of the design philosophy are satisfied.

The minimum p-base width is determined from the depletion spreading into the forward blocking junction. This can be calculated at avalanche as a function of p surface concentration, N_{sp}, and junction depth, X_{jp}, as shown in Figure 5.7. As expected, the depletion region spreading increases with lower surface concentrations and deeper diffusions. The device sensitivity must also be considered in the selection of the p-base width. If the base is too narrow, the device will be extremely sensitive to punchthrough currents for three reasons: 1) when the device is blocking, the depletion region will spread into the p-base region and the effective base width will become small; consequently, the resultant transport factor will be very close to unity; 2) with the extremely narrow effective base region, the sheet resistivity of the base will become very high and the emitter bias will be very sensitive to lateral current flow; 3) also, process variations can cause changes in p-base width, and this must be taken into consideration. In conclusion, the base width should be selected considerably wider than the depletion region spreading.

Perhaps the most important consideration in the selection of the base width is the base transport factor β_n. This function has been plotted in Figure 5.8 as a function of lifetime and includes the effects of the aiding fields established as a result of the diffusion gradient. It can be seen that a base width of ten (10) μmeters will give high current gain β at low lifetimes for both low and high surface concentration diffusion. This base width is also compatible with the depletion region spreading from Figure 5.7 and was, therefore, selected for the initial design.

To determine whether a high or low p surface concentration should be selected for the forward blocking junction diffusion, the following facts must be considered: 1) the largest aiding fields will result from high surface concentration; 2) emitter injection characteristics

improve with lower surface concentration diffusion; 3) higher sheet resistance and, therefore, greater device sensitivity to gate current results from a low surface concentration; and 4) surface fields are more easily controlled with low surface concentration. As a result of these arguments, the low surface concentration ($N_{sp}=5x10^{17}$ cm^{-3}) was selected. As shown in Figure 5.8, the built-in field is sufficiently high with the low surface concentration. It should also be noted that a shallow junction depth ($X_{jp}=15$ μmeters) was selected. The standard emitter diffusion was selected with a high surface concentration and a junction depth selected to give the desired base width.

Since the base width, surface concentration, and junction depth have been selected, the only portion of the design remaining to be determined is the short spacing. Through the use of the two dimensional lateral base biasing calculation, discussed in Appendix C, the effects of the base width, sheet resistivity, and short spacing can be calculated as a function of lifetime on the forward blocking capability. A curve of the form of Figure 5.9 results. It can be seen that at a lifetime of 0.1 μsec, a half short spacing of 0.028 cm will theoretically result in the desired blocking voltage capability. This value was consequently selected for the initial design.

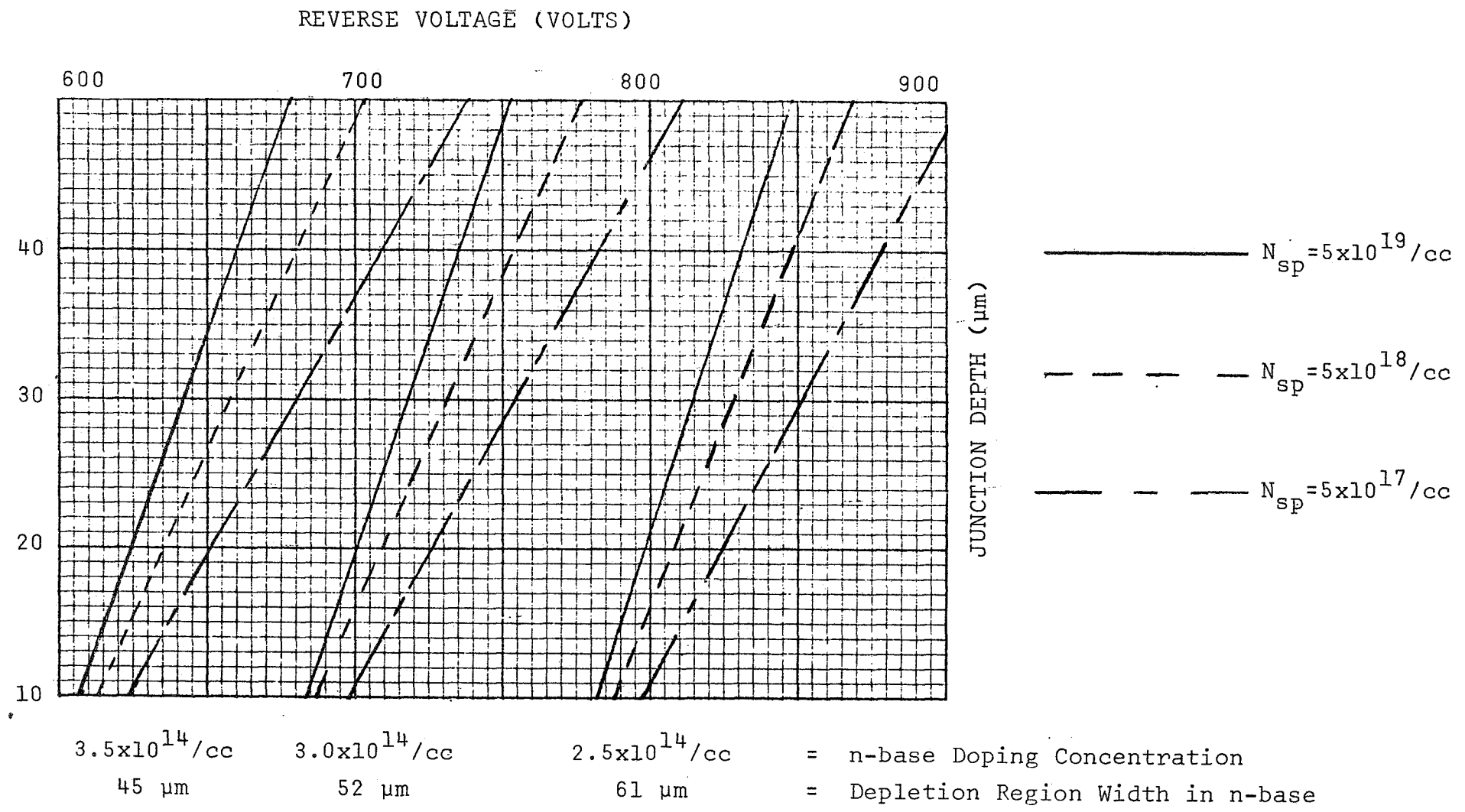


Figure 5.1 Peak Reverse Blocking Voltage for a Complementary Error Function Diffused p^+n Junction.

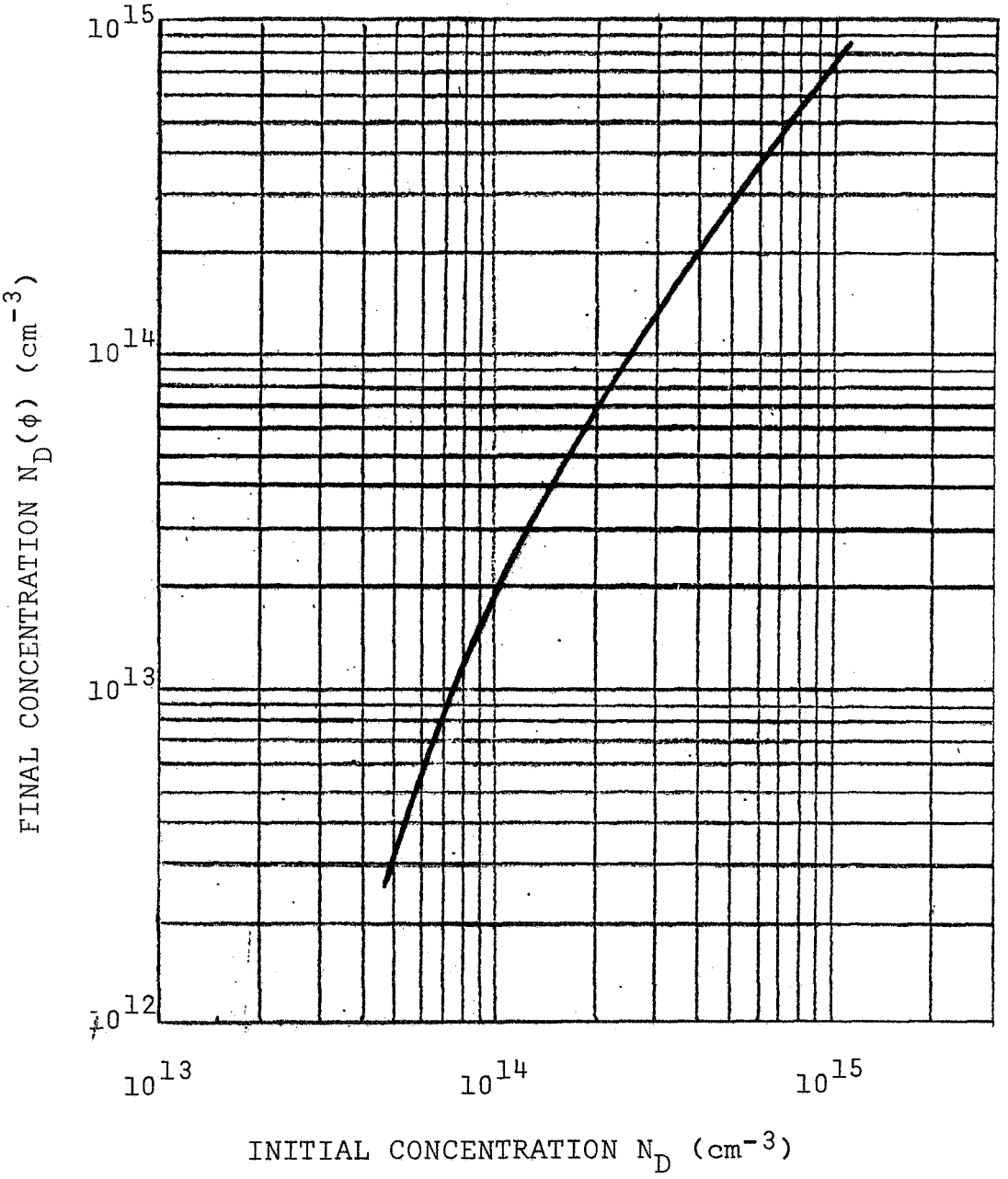


Figure 5.2 Effect of Carrier Removal on the Carrier Concentration in n-type Silicon. $\phi = 5 \times 10^{13}$ nvt

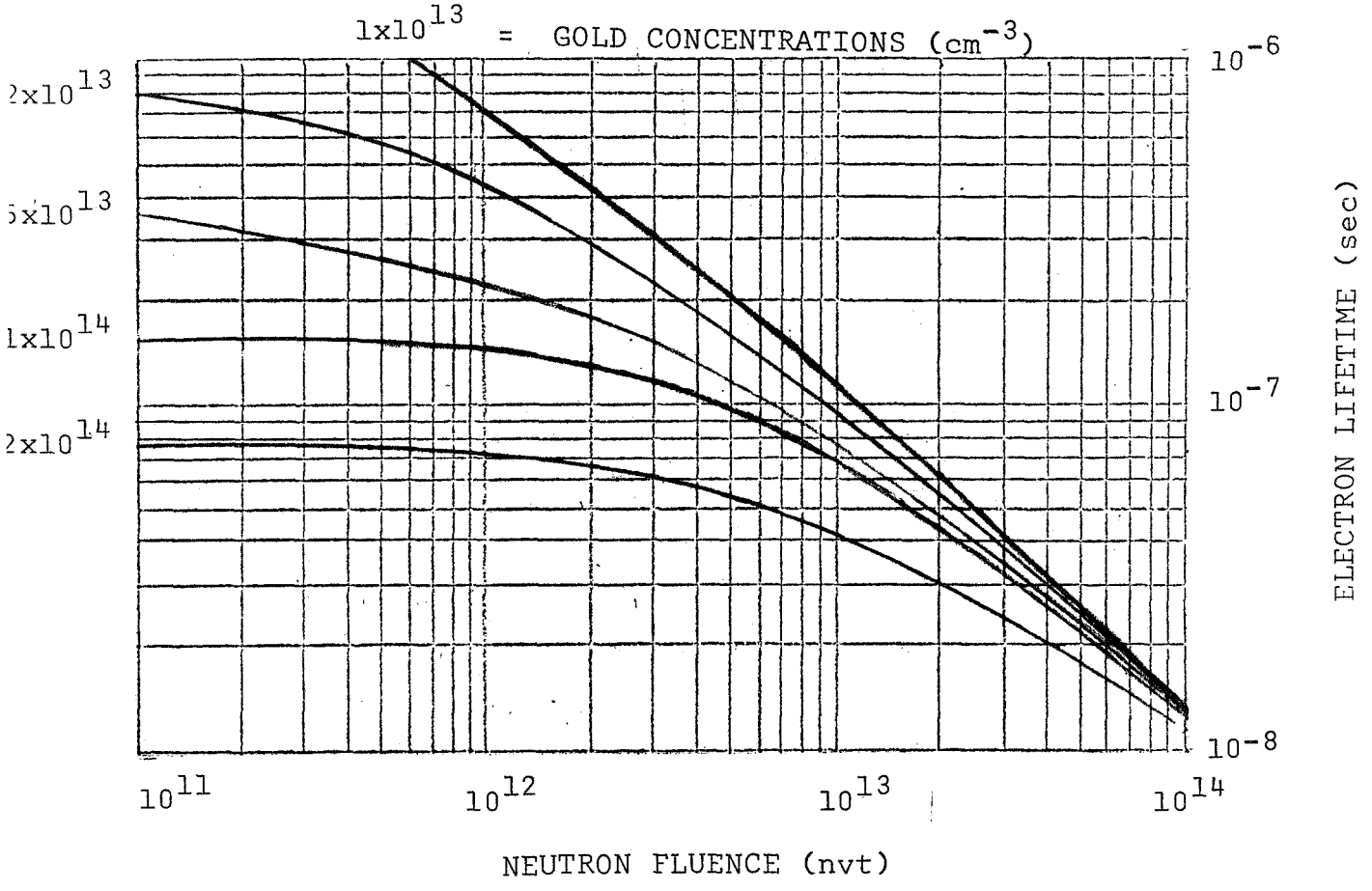


Figure 5.3 Electron Lifetime as a Function of Neutron Fluence in Silicon for Various Initial Gold Concentrations.

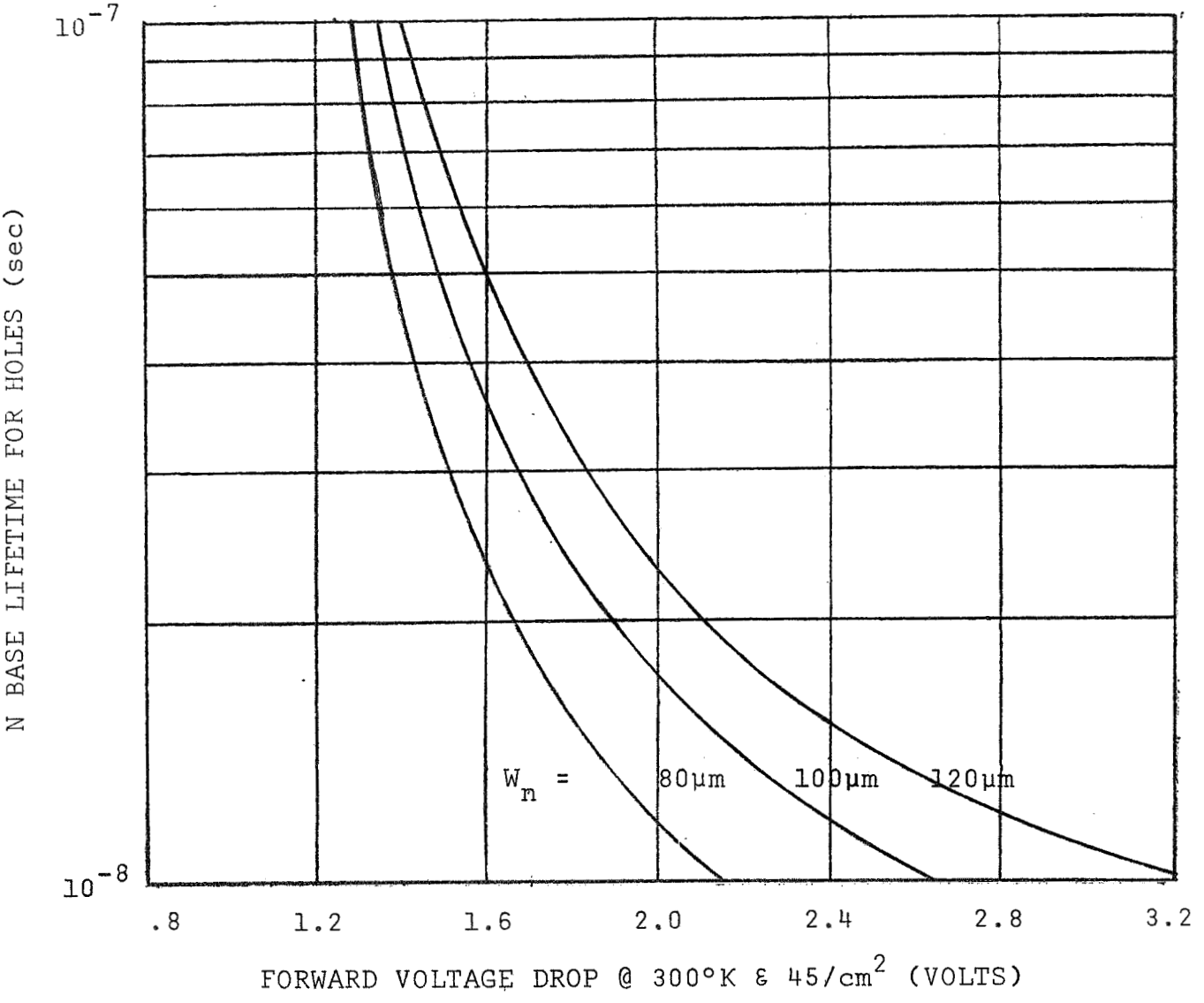


Figure 5.4 Forward Voltage Drop as a Function of n-base Lifetime for Various n-base Widths.

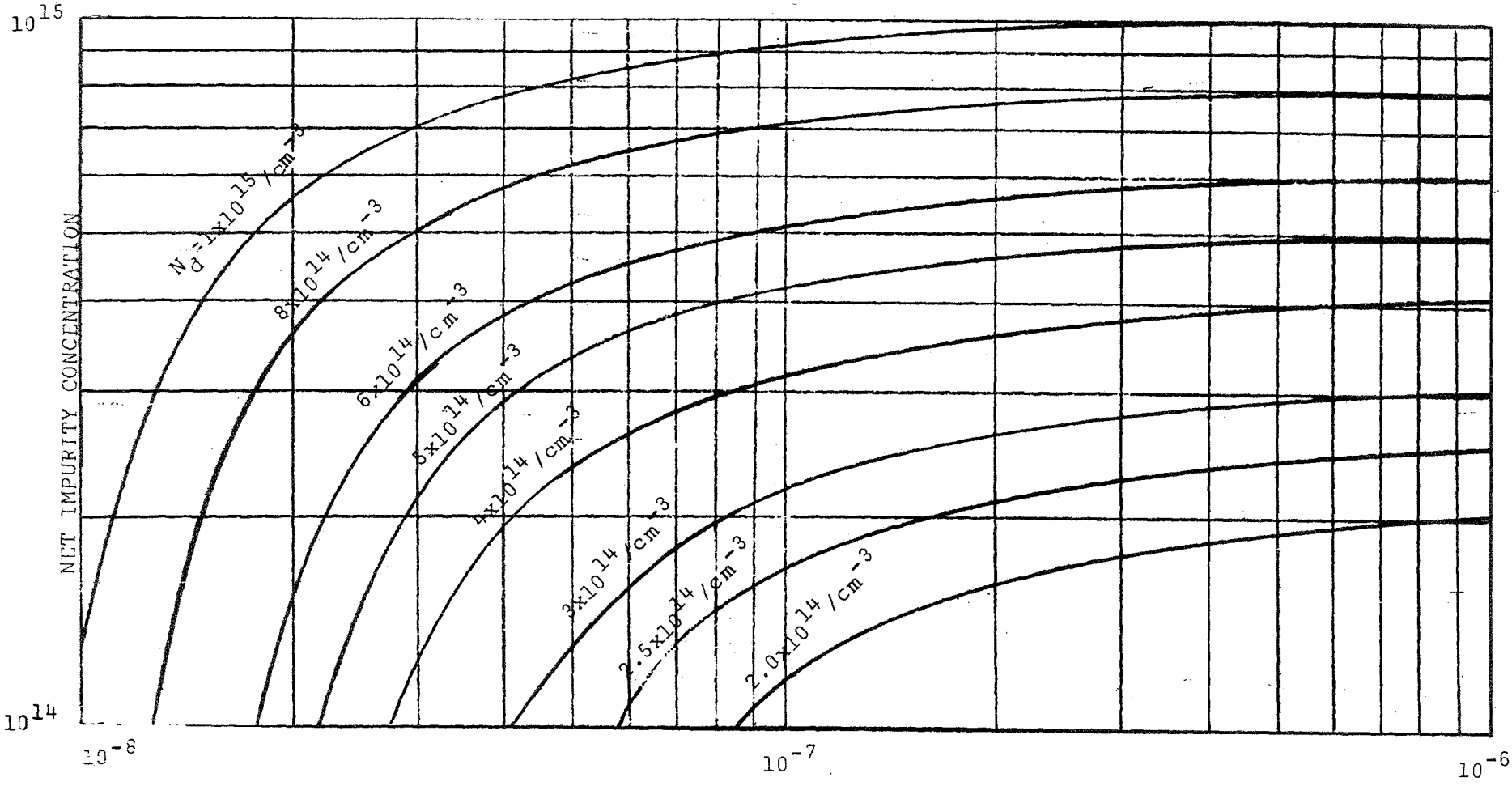


Figure 5.5 Net Impurity Concentration of a Gold Doped N Region as a Function of Hole Lifetime.

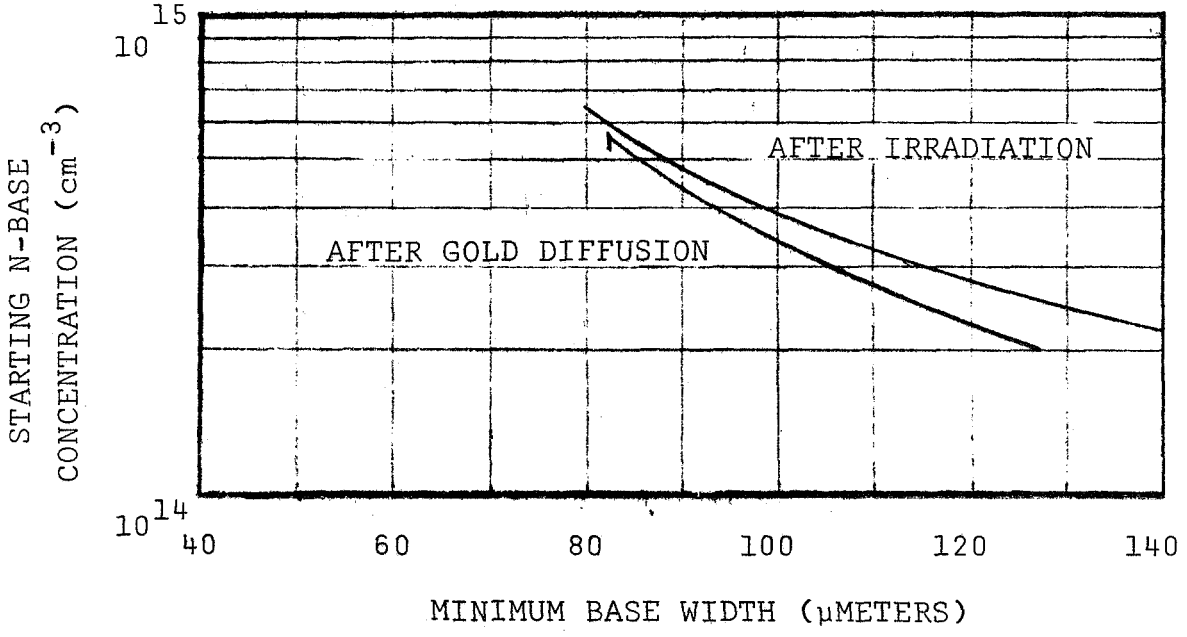


Figure 5.6 Minimum n-Base Width Required to Prevent Punchthrough as a Function of the Starting n-Base Concentration.

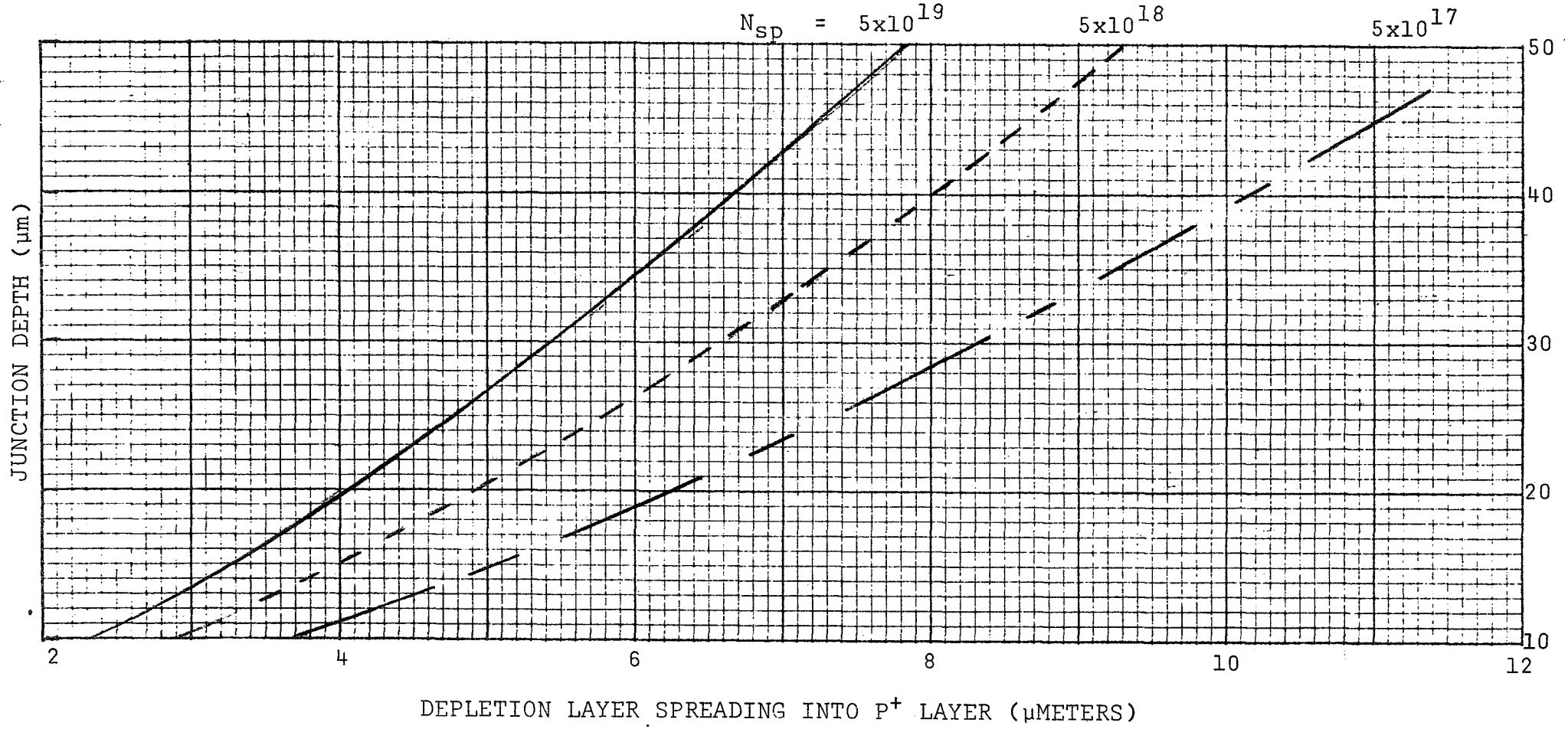


Figure 5.7 Depletion Layer Spreading into the P^+ Layer of a Complementary Error Function Diffused P^+N Junction in Silicon.

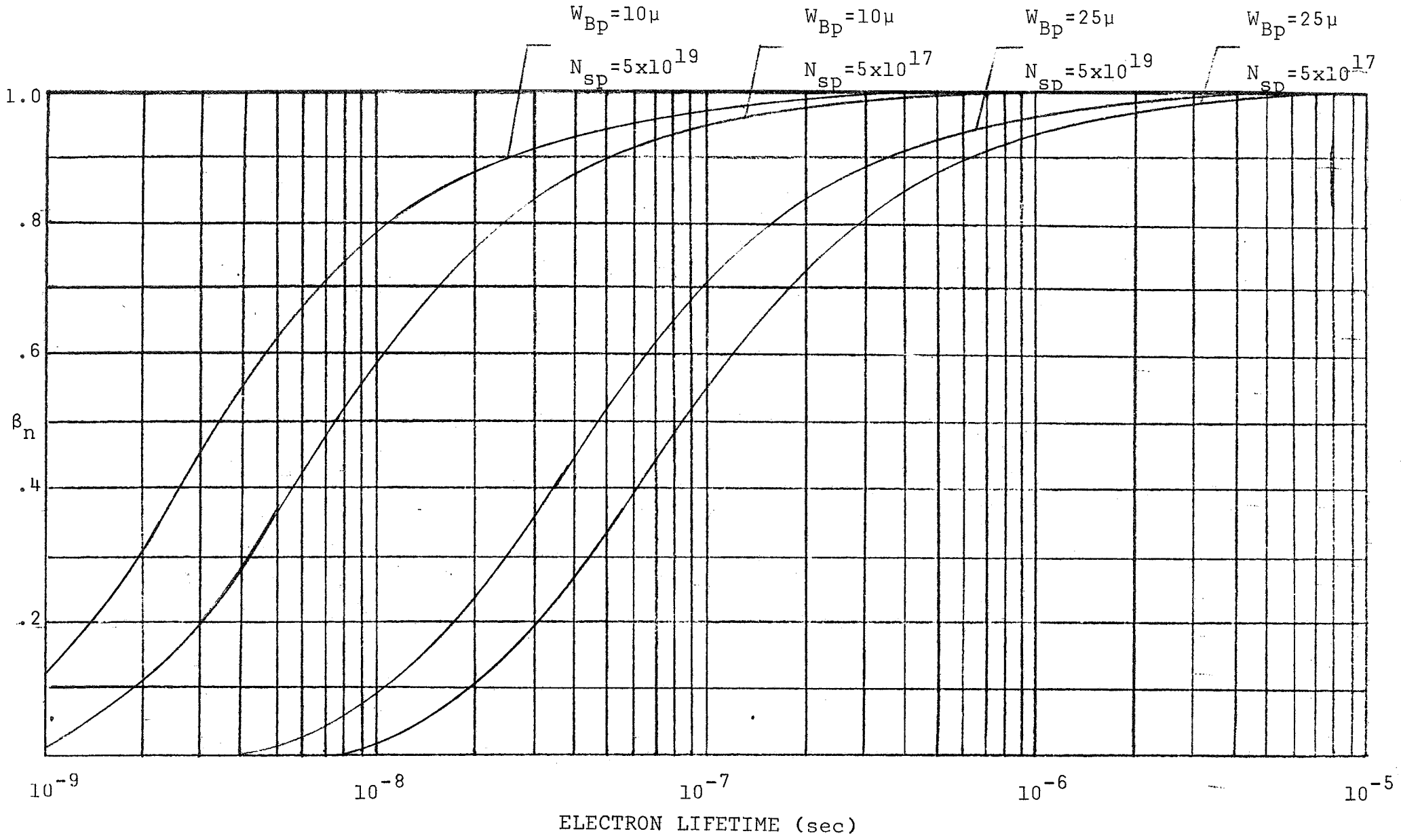


Figure 5.8 p-Base Transport Factor as a Function of Lifetime for Various Diffusion Profiles.

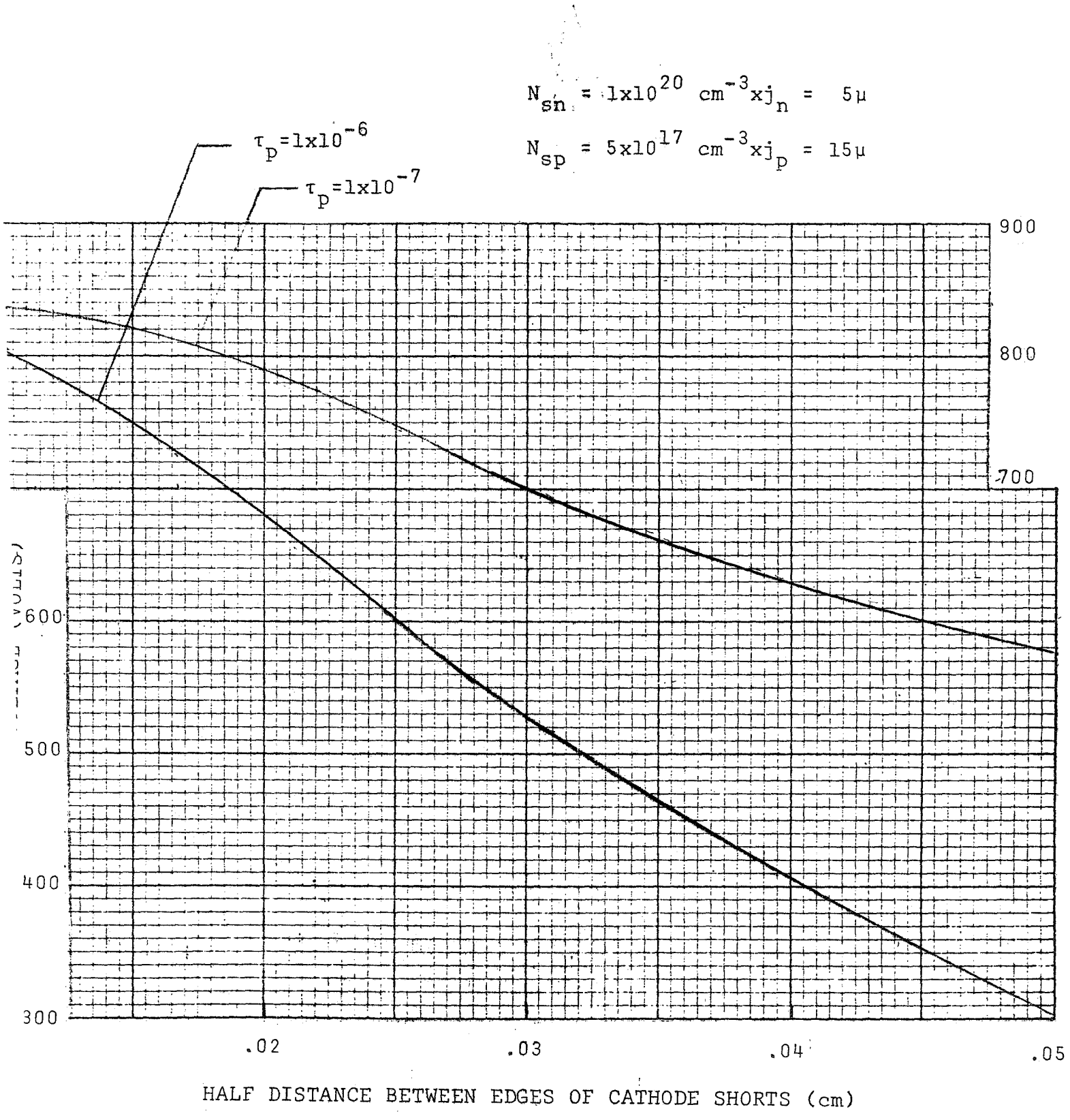


Figure 5.9 Forward Breakover Voltage as a Function of Short Geometry and Lifetime @400°K.

5.4 Proposed Device Design and Discussion

As a result of the discussion in the previous section, the structure of the SCR optimized for radiation resistance is pictured in Figure 5.10.

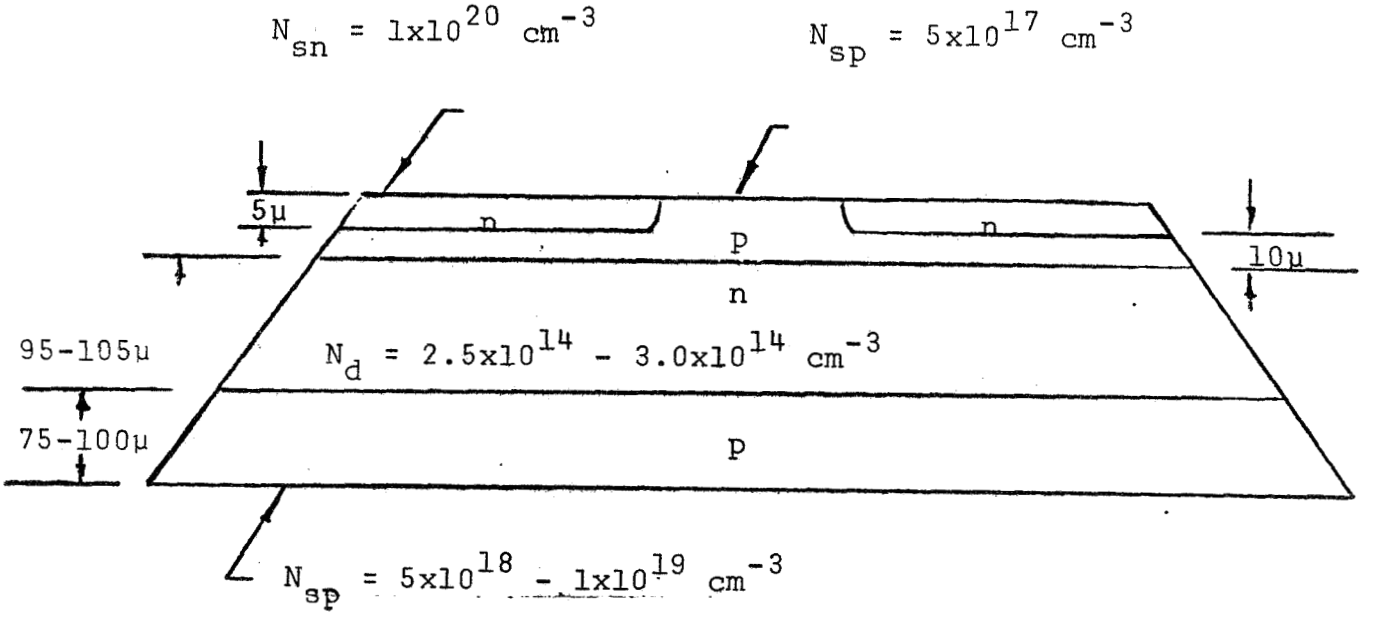


Figure 5.10 Optimized Structure for the Radiation Resistant SCR.

The following parameters were also determined:

n-base hole lifetime	.1 μsec
Half distance between emitter shorts	0.028 cm
Distance from emitter gate periphery to emitter shorts	0.034 cm
Active emitter area	6.9 cm^2

Several aspects of the design are worthy of discussion. The first is the design of the pilot gate. As can be seen, the distance from the emitter gate periphery to the emitter short is greater than the half distance between shorts. Since the resultant resistance under the gate region is greater than that under the main emitter, the pilot gate will be more sensitive than the main SCR and will trigger with lower gate currents. (The effect of short spacing on gate current can be seen in Figure 5.11). The pilot gate was also designed in the center of the device. In this manner, the pilot area can remain small and high current densities can be created in the pilot with relative low gate currents. One should recognize, however, that the gate voltage of an amplifying gate SCR will be greater than the gate voltage of a standard SCR, since two emitter junctions must now be forward biased.

The final curve in Figure 5.12 shows the expected reverse blocking current density before and after radiation. It should be noted that in the calculation of total reverse blocking current the emitter area of 6.9 cm^2 should not be used. Since the current is generated in the depletion region of the bottom junction, the area is greater than the active area of the emitter. First, the diameter is greater, since the top junction is bevelled. Also, the active emitter area includes only the emitter area and not the shorted area. The active device area of 11.0 cm^2 should, therefore, be used to calculate the total reverse blocking current from the curve in Figure 5.12.

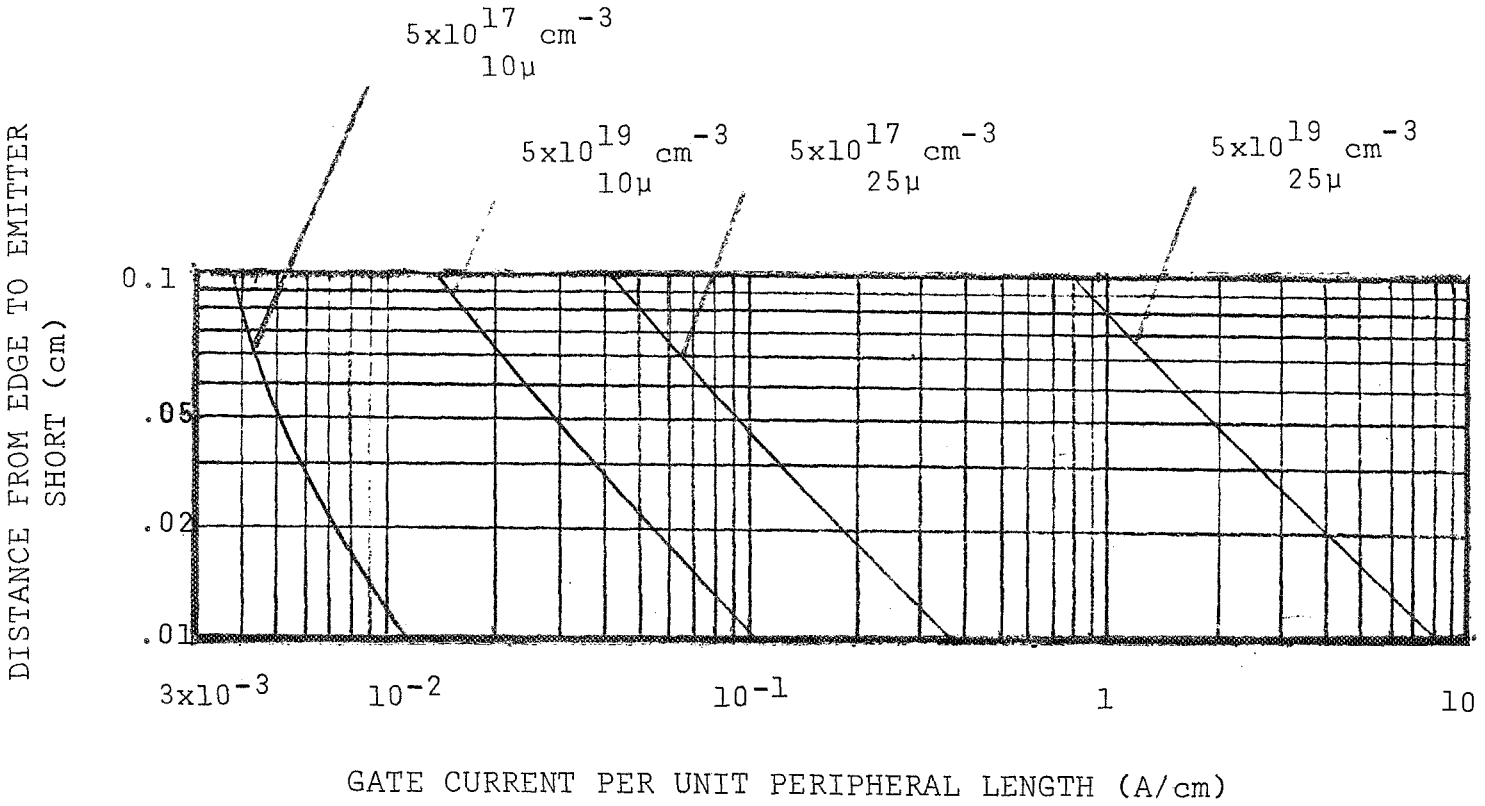


Figure 5.11 Gate Current to Fire as a Function of Distance to Emitter Shorts @ 300°K.

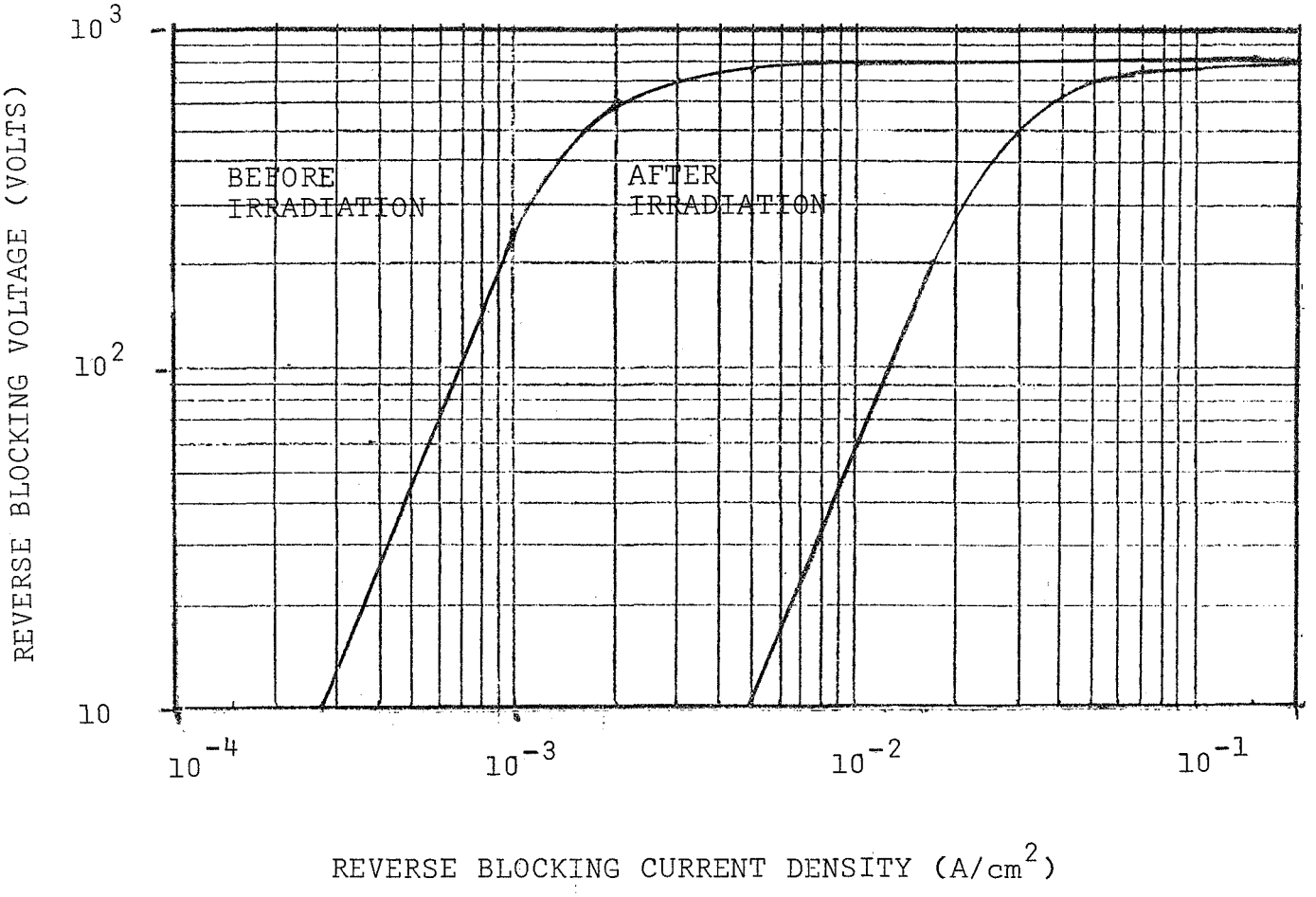


Figure 5.12 Reverse Blocking Characteristics Before and after Irradiation. τ_p=1x10-7, ϕ=5x10^{13} nvt

6. DEVICE FABRICATION

6.1 Introduction

The previous sections have dealt theoretically with the effects of radiation on device characteristics. A method to design a device optimized to reduce these effects and to improve its radiation resistance was also discussed. The task of fabrication, however, remains to be considered.

As might well have been expected, compromises were necessary between the idealized device predicted by the theoretical and analytical considerations, and what could be produced by state-of-the-art processing technology. Fabrication of the proposed structure proved to be difficult. Many problems were encountered.

In the following section a description of the initial process and identification of the initial problem areas will be given. These problem areas will then be discussed, along with experimental evidence which led to their identification. Conclusions will be reached with regard to the solution of these problems through a device redesign that would have a minimal effect on the radiation resistance. The intent will be to give a brief picture of the process problems and results and not to deal in detail with the experimentation which led to the final design. The section will be concluded by presenting the results from the fabrication of the devices with the redesigned structure.

6.2 Fabrication Process

The structure of the SCR which was optimized for radiation resistance was discussed in Section 5.3. In order to fabricate this structure, however, typical diffusion process steps had to be modified. This section will summarize the process steps involved in the fabrication of the proposed structure.

a) Wafer Preparation

1. Cut wafers from silicon billet.
2. Lap wafers.
3. Chemically polish wafers by etching.

b) Wafer Diffusion

1. Diffuse wafers with gallium on both sides (~80 microns).
2. Lap wafer to remove gallium on one side.
3. Chemically polish the lapped surface.
4. Diffuse boron on lapped side (~12 microns).
5. Oxidize both sides.
6. Etch emitter pattern on boron diffused side using photolithographic techniques.
7. Diffuse phosphorus emitter (5 microns).
8. Boron getter from anode side.
9. Diffuse gold from anode side.

c) Wafer Contact Metallization

1. Vapor deposit vanadium and silver on emitter side.
2. Etch contact pattern using photolithographic techniques.
3. Vapor deposit aluminum on anode.

d) Subassembly Fabrication

1. Alloy wafer to tungsten back up plate.
2. Bevel positive angle on the reverse blocking junction.
3. Bevel shallow negative angle on the forward blocking junction.
4. Chemically etch contour junctions.
5. Passivate junctions.

e) Electrical Evaluation

1. Preliminary voltage classification.
2. Hermetically house electrically good subassemblies.
3. Final electrical evaluation.

The foregoing process is different from the standard process for high current SCRs. The major differences include the addition of a single side lapping and polishing operation and a second shallow p type diffusion. Since these differences eventually were the cause for much concern, it is worthwhile to consider these differences briefly.

Typical SCR processing requires two diffusions, an initial double side p type diffusion, followed by an n type emitter diffusion. This results in a symmetrical structure, where both p regions have similar impurity profiles. These junctions are also typically deep, on the order of 75 to 100 microns. It has been the experience of people in this laboratory that high voltage devices with sharp avalanche breakdown characteristics can be fabricated very consistently with deep diffusions. This results since the junction region is located away from surface related damage and irregularities.

In the case of the radiation resistant SCR, however, the design required a shallow, 15 micron diffusion for the forward blocking junction. A double side shallow diffusion was not possible. For the above reason one would prefer a deep junction for blocking capability. In addition, a double side, shallow diffusion would result in an extremely thin wafer (~125 microns), one that would be very difficult to handle. For these reasons it was necessary to use two separate p type diffusions to form the desired structure. The addition of a one side lapping operation resulted from the fact that gallium used to form the deep junction and silicon dioxide will not serve as a diffusion mask for gallium.

6.3 Device Fabrication Problems

When devices were fabricated with the proposed process, a major problem was encountered with the blocking voltage. A feeling for the type of problem can be obtained through comparison to a power transistor, since the type of structure required for the forward blocking junction of the SCR is typical of the structure used in high voltage (600 volts) power transistors. The emitter area, however, is many times larger than any commercially available transistor. This fact becomes important when one considers yield.

Yield, specifically blocking voltage yield, is subject to degradation due to defects in the crystal, since the blocking voltage capability of a junction is impaired by the presence of a defect. In general, defects are caused either during the growth of the crystal or during subsequent high temperature processing, such as diffusion. They are distributed across the wafer in a random fashion, their density and location being dependent upon the history of the silicon crystal, including processing conditions and doping concentrations. The important point is that since the presence of a defect in a given piece of silicon is random, the probability of finding a defect in that piece of silicon is a function of area and will increase with increasing area. Consequently, when the area of a power transistor increases, the voltage yield will decrease. In the case of the SCR, the situation is even more demanding. Since the blocking junction covers the entire area of the pellet, only one defect is necessary to degrade the blocking characteristics. Therefore, the question of yield for an SCR reduces to the probability of finding a defect in an entire wafer. The ramifications from this result will be evident in the following sections.

6.3.1 Forward Blocking Voltage

A major problem arose during the course of fabrication of the proposed structure. None of the initially fabricated SCRs possessed the required forward blocking voltage capability of 600 volts. In fact, typical forward characteristics appeared resistive in nature, not what would be found from a four layer semiconductor. Many possible causes were investigated. Among these were spikes, poisoning, microplasmas, and surface breakdown. Before the experimental evidence is presented which identifies the specific problem areas, a brief description of the problem areas will be presented.

Spiking

Processing variables can introduce non-uniformities into the structure. One of the most persistently troublesome of these occurs during diffusion. It can be related to imperfections, introduced either by prior processing of the wafer or during the growth of the crystals themselves. The phenomenon is manifest as locally deep diffusion penetration. By whatever means they arise, these point-wise deviations from flatness of diffused junctions create localized points of high electric field. The depletion layer spreads unevenly, leading to premature breakdown wherever these points occur. Similarly, in a device whose breakdown characteristic is governed by punchthrough, these points can break down in advance of the remainder of the device and carry more than their share of reverse blocking current. The problem is referred to as spiking because of the resemblance of these deep points of enhanced diffusion to small spikes.

One cause of these spikes has been found in phosphorus diffusion using a P_2O_5 source. The usual procedure when using this diffusion process is, as follows: a source boat containing P_2O_5 is maintained in the diffusion tube at a temperature ranging from 100-400°C. A stream of oxidizing gas passes over this boat picking up and carrying with it the vapors of P_2O_5. Farther down the tube silicon wafers

are placed at the diffusion temperature, which is usually in the range of 1100-1300°C. The silicon wafers, being in an oxidizing environment, become covered with a glassy coat composed of silicon dioxide and P_2O_5. Ideally, this coating of glass is uniform all over the wafers. It sometimes happens, however, that small particles of P_2O_5 will be carried from the source boat to the silicon wafers. If such a particle lands on the silicon surface, a locally high concentration of phosphorus is created. Diffusion from such a source into the silicon slice may cause spikes[39,40].

To avoid this effect, particular care must be taken during phosphorus diffusion of silicon wafers. Other forms of phosphorus can be used as source materials. The surface concentration and temperature can be reduced. While these procedures will reduce or eliminate the incidence of spiking from diffusion, they do not decrease the occurrence of spikes from flaws in the silicon wafer.

Poisoning

Precipitation of undesired impurities, normally called poisoning, is an anomalous effect occurring most frequently during diffusion of silicon. It is generally attributed to local concentrations in the junction region of undesirable metallic impurities. If an undesired metallic impurity is present in a silicon slice, it can migrate to regions of high dislocation density under certain heat treating conditions frequently found in diffusion. At these points, the metallic element precipitates and forms small particles. The electric field in the vicinity of these particles is concentrated, leading to enhanced impact ionization in this area. These effects have been extensively studied and have been shown to be related to the occurrence of microplasmas[41,42,43], which are small light-emitting areas in the junction region and are associated with soft breakdown characteristics. These microplasmas were observed in the radiation resistant devices and will be discussed in more detail.

To reduce the effects of poisoning, gettering has been employed. Gettering makes use of the fact that poisoning impurities frequently have higher solubility in other metals, oxides, or glasses than in silicon. These metals, oxides, or glasses are applied to the surface of the silicon slice and a heat treatment is carried out. During this procedure, the undesired impurities migrate to the surface of the silicon slice and these dissolve in the surface coating, after which the coating and the impurities can be removed chemically. These methods have been employed widely in the manufacture of large-area, high-power silicon devices with beneficial effects.

Microplasmas

If a p-n junction is reverse biased, spontaneous light emission may be observed. These emissions can be divided into three classes. In very pure silicon crystals with plane-parallel junctions and without surface effects, a relatively uniform glow appears first. This is caused by hole-electron recombination in the depletion region under avalanche conditions. The breakdown voltage of these junctions agrees with theory.

More often, however, one sees a number of discrete points of light. The number and distribution of these depends on the frequency of occurrence of inhomogeneities in the blocking layer, such as lattice defects, metallic precipitates, and spikes. The dimensions of these points are small, less than one micron in diameter. The broad-area radiation referred to above is called macroplasma, while a point-wise source, which may be very numerous, is called a microplasma.

With repeated applications of reverse current, microplasmas recur in the same locations. If the voltage is very slowly increased, it is found that individual microplasmas will appear at the same value of voltage, which may differ for each. Investigations of microplasmas have shown that they are the result of avalanche breakdown of small, individual channels.

Surface Breakdown

Avalanche breakdown occurs in silicon when the electric field reaches a critical value[1]. A junction avalanches when a free carrier in the space charge layer is accelerated to a sufficient speed, such that its collision with the lattice results in the creation of hole-electron pairs which in turn accelerate, collide, and create more hole-electron pairs. A similar phenomena occurs at the surface of the device if the critical value of electric field is reached. Intuitively, one would expect that less electric field would be required to produce avalanche breakdown at the surface, since carriers are not as tightly bound to the lattice near the surface due to gross imperfections and disturbances at the surface-ambient interface. Consequently, one would expect surface breakdown to occur before the voltage across the device reaches a high enough value for breakdown within the silicon.

It is desirable to design a device so that breakdown occurs in the bulk, so that optimum blocking voltage capability can be achieved with the lowest starting resistivity. This implies that the surface field must be reduced. Several methods are available, however, the one most commonly used for high power SCRs (and the one used in the radiation resistant SCR) is surface contouring[44]. In this case the junction surface is bevelled, so that the depletion region at the surface spreads farther than in the bulk and, consequently, reduces the electric field. A detailed explanation of the effects of beveling angle, junction depth and surface concentration can be found in reference (44) For our purposes now, only two results are necessary:

(1) A positive angle contour (one where the region with the higher concentration of impurities has the larger diameter) is more effective in reducing surface fields than a negative angle and,

(2) A deep, low surface concentration diffusion will produce lower surface fields for a given contour than will a shallow high surface concentration diffusion.

These results are important, as the radiation resistant SCR was designed with a shallow forward blocking junction which is normally contoured with a negative angle for ease in fabrication.

6.3.2 Lifetime Control

A vital area in the fabrication of thyristors is lifetime control. In the structure of the SCR for radiation resistance, this area is even more critical, since the narrow p-base results in a high gain npn section of the SCR, which will cause premature turn-on if the lifetime is not reduced sufficiently to decrease this gain. This lifetime control is usually accomplished by diffusion of gold into the structures as one of the final stages of construction. Gold is quite effective in this application, but there are side effects which complicate its use.

Gold is one of several elements known to have two different diffusion rates in silicon. As an interstitial atom, it diffused very rapidly, while substitutionally the diffusion rate is slower. For lifetime control, we make use of the fast-diffusing nature of interstitial gold, because the gold can be put into a device as a final step after all other structure-forming processes are complete without any significant diffusion of other elements and, consequently, without changes in the device geometry. Gold diffusion is complicated, however,

when attempting to achieve a determined gold concentration in the base regions of an SCR, in our case, specifically the p-base. It has been shown that phosphorus layers inhibit gold diffusion in silicon. As a result, it is difficult to control the location and concentration in a device.

The effect of improper gold concentration on this device should be realized. If the gold concentration is too low, the gain of the npn will be too high and the device will turn on at low forward voltages. If the gold concentration is too high, the gold atoms will compensate the high resistivity n-base, causing punchthrough. In the design of the device, the starting resistivity was selected lower than normal to compensate for some rise in resistivity during gold diffusion. The area still remained critical, since further compromise was necessary between blocking voltage and forward drop.

6.3.3 Experimental Results and Discussion

In order to determine the precise cause of the limited blocking voltage problem, a series of experiments was performed. The intent was to isolate the cause of the blocking voltage problem, so that corrective measures could be taken on subsequent diffusions.

A feeling of the type of problem that was encountered can be gained by inspection of the table in Figure 6.1. The table summarizes the forward and reverse breakdown voltages obtained from the first two diffusion groups. A major blocking voltage problem is obvious, since no devices exhibited a forward blocking voltage capability.

	GROUP A		GROUP B	
DEVICE #	$V_{(BR)R}$	$V_{(BO)}$	$V_{(BR)R}$	$V_{(BO)}$
1	840	Short	780	Short
2	870	Short	880	Short
3	610	Short	-	-
4	800	Short	280	Short
5	100	Short	720	Short
6	Broken	Short	Short	Short
7	840	Short	-	-
8	880	Short	840	Short
9	840	Short	680	Short
10	440	Short	-	-

Figure 6.1 Summary of the Forward and Reverse Blocking Voltages From the First Two Diffusion Groups.

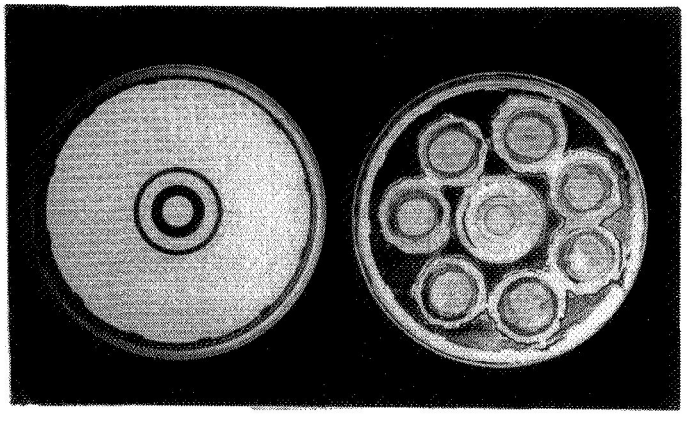


Figure 6.2 Subpelletized Wafer Used for Evaluation of the Forward Blocking Voltage.

In order to determine the cause of the problem, several of the above devices were subpelletized by etching down through the metallization and the forward blocking junction to isolate several small SCRs (~300 mils in diameter) on the same wafer, as shown in Figure 6.2. These individual pellets were then checked for forward blocking voltage capability. The table in Figure 6.3 summarizes the results.

Individual Sub-Pellet #	GROUP 'A' PELLET		GROUP 'B' PELLET	
	$V_{(BR)R}/I_R$ (ma)	$V_{(BO)}/I_D$	$V_{(BR)R}/I_R$	$V_{(BO)}/I_D$
1	800/5	Short	850/1	Short
2	900/2	Short	800/2	Short
3	950/.2	400/3	750/2	350/1
4	900/1	Short	500/6	Short
5	975/1	450/.5	550/2	60/3
6	975/2	40/2	750/2	Short
7	850/2	400/.2	100/2	60/7
8	975/1	450/20	550/4	350/4

Figure 6.3 Forward and Reverse Blocking Voltages of the Subpelletized Wafer of Figure 6.2.

As can be seen, some of the subpellets regained a forward blocking voltage capability. Several conclusions were evident as a result of this experiment:

1) Since the forward blocking voltage capability was regained on some of the subpellets, the problem was established to be localized.

2) Since some of the subpellets remained electrical shorts, the problem appeared to be caused by phosphorus spikes which had diffused through the p-base region to short the forward blocking junction.

3) Since none of the subpellets attained a forward blocking voltage capability near the design voltage of 720 volts, an additional problem was indicated.

In order to prove that spiking was, indeed, a problem, several wafers were angle lapped and stained so that the junctions could be observed. The pictures in Figure 6.4 of the forward blocking junction proved the existance of spikes, as one can see a continuous n-region extending from the n^+-emitter through the p-base region into the n-base region.

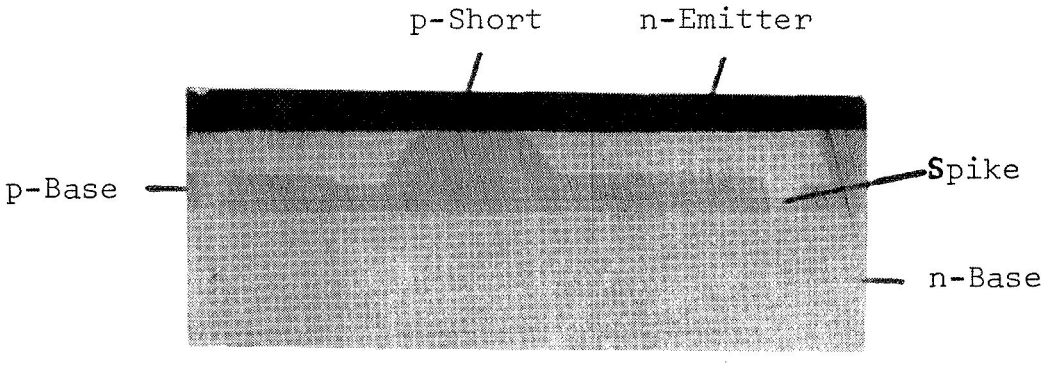


Figure 6.4 Angle Lapped and Stained Cross-Section of the npn Section of a Thyristor Showing the Existance of an n spike.

Since the existance of spikes had been clearly shown, the reason for the shorted forward blocking characteristics was established. However, the fact that the forward blocking voltage of the subpelletized subassemblies was below the designed voltage remained to be evaluated. This effect could result from one or all of the following:

1) Punchthrough to an n spike in the p-base region which had not extended into the n-base region to cause a short,

2) Degradation in the blocking characteristics resulting from junction poisoning, or

3) Surface breakdown resulting from an improper surface contour.

To gain more information as to the reasons for the limited voltage capability, a series of experiments were performed with shallow diffused junctions. Simple p n p diffused wafers were used as a vehicle for voltage experimentation in preference to actual devices. This simplified the experiments in several ways. It eliminated spiking as a cause for premature breakdown, since the pnp wafers would contain no n^+ emitters, and it simplified processing by eliminating oxidation, masking and diffusion steps. Also, by contouring a pnp wafer with one angle, both positive and negative contours could be evaluated on a single wafer.

Many experiments were performed. Both gallium and boron were evaluated as dopents. Open and closed tube diffusion processes were evaluated with various surface concentrations and junction depths. Wafers were mechanically polished to a mirror finish before diffusion so that the effects of the wafer surface on the junction characteristics could be evaluated. Even a simultaneous gallium-arsenide process was evaluated. The specific results from these experiments are important, for they determined the causes for the blocking voltage difficulties. However, the details are not esssential in the development of the radiation resistant SCR. In fact, they would do little more than obscure the major objective, the fabrication of a device with improved radiation resistance. Consequently, these details have not been included here. The general results and conclusions, however, are important and will be discussed in the following section.

6.3.4 Conclusions

As a result of the evaluation of the effects of shallow junctions on blocking voltage capability, several conclusions were drawn:

1) Spiking was definitely a problem with shallow junctions. The probability that spikes will occur within a device can be decreased by lowering the surface concentration of the phosphorus and by careful surface preparation, such as polishing. Operations on the silicon wafer, such as sawing and lapping, causes damage to the crystal lattice which extends below the surface. This type of damage enhances the probability of spiking, especially in devices with shallow junctions, since the junction may lie in the damaged region.

2) The surface contour had a pronounced effect upon blocking voltage capability of devices with shallow junctions. In general, designed voltage capability could be obtained only on devices which were contoured with a positive angle. The surface contour became even more critical on devices fabricated with shallow, high surface concentration diffusions.

3) The blocking voltage capability of junctions which lie close to the surface is subject to degradation caused by poisoning. Crystal damage sites which extend below the surface act as sinks for metal impurities, and when these sites are located in the depletion region, the blocking voltage can be impaired. The effects of poisoning can be reduced by using deeper blocking junctions and by careful surface preparation to reduce surface generated damage.

4) Since a combination of the above effects were found to be the cause of the blocking voltage problem, it was concluded that the proposed structure for the radiation resistant SCR could not be fabricated with conventional techniques in a reasonable amount of time.

6.4 Device Redesign

For the reasons which have just been discussed, a redesign of the radiation resistant SCR was necessary in order to fabricate devices and complete contract commitments. One question which must be answered, however, is what effect will a device redesign have on the inherent radiation resistance of the device. This question will be discussed in the following section. We will see that one further trade-off should have been considered at the time of the original design, that being processing feasibility. There is a trade-off between processing capability and radiation resistance.

6.4.1 Compromise Design

In order to fabricate an SCR with a blocking voltage capability of 600 volts, the problems associated with shallow junction had to be eliminated. Several alternatives were available. The occurrence of spiking can be reduced by lowering the surface concentration of the n^+ emitter diffusion. This could also be accomplished by increasing the p-base width and the p diffusion depth. The wider p-base would reduce the effect of shallow spikes which might totally short a narrower base region, while the deeper diffusion would reduce the effect of surface related damage, since the blocking junction would lie deeper in the silicon. A deeper diffusion would also reduce the likelihood of junction poisoning, since the impurities which precipitate at damage sites near the surface would not be located in the depletion region. The peak surface fields can be reduced by decreasing the p surface concentration and increasing the junction depth.

This causes a more graded junction which results in more depletion region spreading and lower peak fields. However, the same result can be effected by contouring the surface with a positive angle. So, in summary, for optimum blocking voltage capability, one would like deep diffusions, wide p-base width, low p surface concentration, and a positive bevel. However, this does not contribute to optimum radiation resistance. As discussed in section 4, a deeper, lower surface concentration p-type diffusion would cause a more graded junction which would decrease the aiding built-in field and, consequently, the transport factor (npn gain), especially at low lifetime. An increase in the p-base width (which would be necessary for a more graded junction, since the depletion region spreading would increase) likewise would decrease the transport factor. Since a high npn gain is desired for radiation resistance, these effects would decrease the radiation resistance inherent in the proposed structure. In short, there is a trade-off between radiation resistance and blocking voltage. More precisely, there is a trade-off between radiation resistance and the processing capability to build high voltage junctions.

In order to complete all contract commitments, it was necessary to optimize the design and to fabricate devices representative of this design. However, in consideration of the amount of time and expense spent in additional process development and experimentation, it became necessary to formulate a new objective: to design a device with optimum radiation resistance which could be fabricated using existing state-of-the-art processing and yet would meet all the desired objective device specifications. Since the time element was becoming an important consideration, one further requirement was placed on the design. The device would have to be fabricated with the conventional double beveled structure which places a small negative angle on the forward

blocking junction. This was important, since it had been determined that a limiting factor for the blocking voltage capability of a shallow junction was the surface contour; a positive angle was optimum. This meant that the p-base width and the junction depth had to be increased over and above that which would have been necessary with a positive angle. The results from the design are summarized in Figure 6.5.

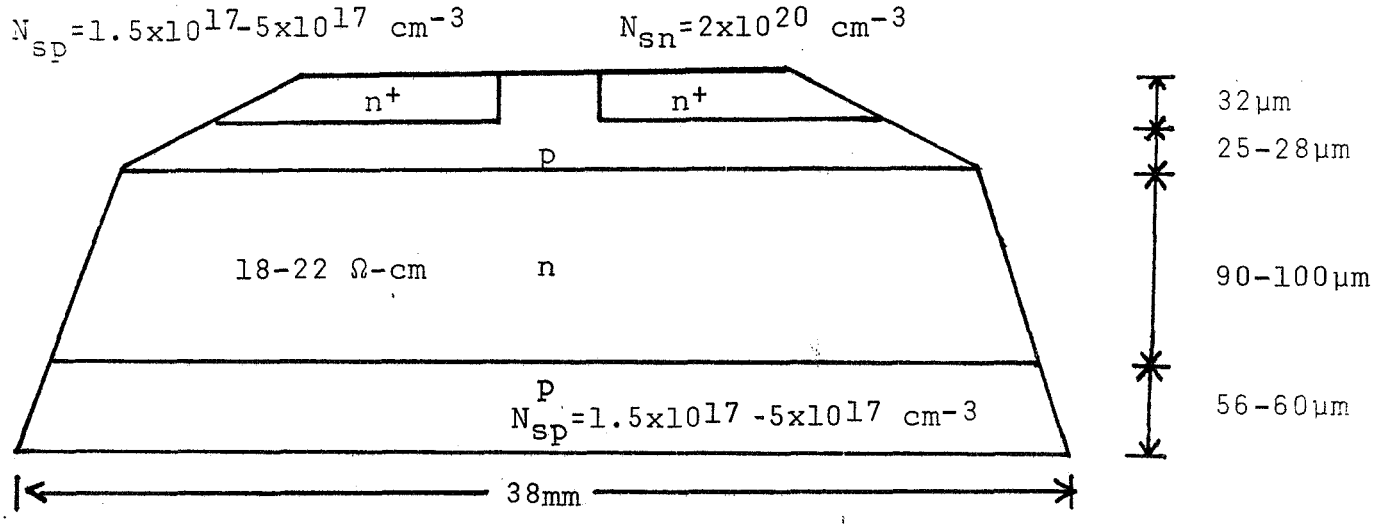


Figure 6.5 Redesigned Structure for the Radiation Resistant SCR.

This structure could be fabricated with standard processing. Since both p-type diffusions are relatively deep, it became possible to use the standard double side gallium diffusion and, consequently, to eliminate the single side lapping and etching operation which was required in the original structure. Of course, the additional shallow p-type diffusion was also eliminated. Devices representative of the above structure were fabricated successfully. The results are included in the following section.

6.4.2 Results

The results from the device redesign are summarized below. While the total yield was quite low, sufficient devices were fabricated with the desired blocking voltage to complete contract commitments. A complete summary of all test results can be found in Section 7. These results are included here to establish that blocking voltage was achieved on the redesigned structure.

DEVICE #	$V_{(BO)}/I_D$ (ma)	$V_{(BR)}/I_R$ (ma)
211- 1	720/1	730/1
211- 3	700/3	620/5
211- 6	700/2	700/2
212- 2	600/10	680/1
212- 3	640/10	740/1
212- 4	750/5	790/1
212- 8	700/4	740/1
212-10	700/5	700/1
212-13	660/5	720/1
212-15	700/2	730/1
212-16	760/1	740/1
212-19	680/1	680/1
212-22	700/1	710/1
215- 1	660/5	780/1
215- 2	730/1	740/1
215- 4	760/1	760/1
215- 6	760/1	740/1
215-13	770/1	770/1
215-16	690/1	780/1
216- 3	780/1	680/1
216- 4	720/1	720/1

Figure 6.6 Summary of the Results of the Blocking Voltage Capability of the Redesigned Radiation Resistant SCR.

7. TEST RESULTS

7.1 Crystal Measurements

The Table in Figure 7.1 summarizes the results of the measurements performed on the starting crystal ingot and wafers.

MEASUREMENT	METHOD	RESULTS
Homogeneity of Bulk Conductivity	2 Pt./4 Pt. Probe	Max.-21.6/22.2Ω-cm Min.-18.2/18.6Ω-cm
Uniformity of Lateral Wafer Conductivity	———	Min.Variation 6.3% Max.Variation 9.0%
Minority Carrier Lifetime	Photo Decay (ASTM-F28-06)	Min. 600 μsec Max. 1000 μsec
Majority Carrier Mobility (Hall)	van der Pauw (2 samples)	1686 cm^2/V-Sec 1733 cm^2/V-Sec
Crystal Growth Process	Mon-x Dislocation free	———
Crystalographic Growth Dimension	———	1-1-1
Degree of Compensation	———	<3%
Oxygen Content	Infrared	Below Detectable Level
Dopant Type and Concentration	———	Phosphorus $2.3\text{-}2.9 \times 10^{14}$ cm^{-3}

Figure 7.1 Summary of Test Results for Starting Crystal Ingot and Wafers.

7.2 SCR Measurements and Discussion

The Table in Figure 7.2 shows a summary of the forward and reverse blocking voltages and the forward voltage drop. In the case of the blocking voltages, two values are given. The first value corresponds to the readings taken immediately preceding complete electrical evaluation, while the second value corresponds to the readings taken immediately following completion. The table in Figure 7.3 shows a summary of forward and reverse blocking currents, gate current and voltage-to-fire, turn-off time, holding current, dv/dt, and thermal impedance. By comparison of this table with the objective device specifications found in Appendix A, it can be seen that all the objectives were accomplished with the exception of the forward and reverse blocking currents at 125°C. This objective could have been met by reducing the gold diffusion temperature. However, this could cause a reduction of the blocking voltage capability. As discussed in Section 5, the initial gold diffusion temperature and, hence, lifetime was selected such that the initial resistivity would increase, raising the blocking voltage. In accordance with our design philosophy, it was decided that the blocking voltage capability was more important than a slight increase in leakage current, especially since the post irradiation leakage currents will increase above this value.

An additional problem was encountered with the dv/dt measurement. As can be seen in the table, a few devices did not meet the 50V/μsec specification. It is believed that this resulted from junction irregularities in the p-base forming localized regions with high sensitivity, (high npn gain). This arguement is supported by considering the holding current data. A more sensitive device would, in general, have a lower holding current. In addition, several devices failed during dv/dt testing. A typical amplifying gate type SCR is designed such that the pilot SCR is more sensitive

to dv/dt. In this structure, the pilot SCR would turn-on first and provide safe gate drive for the main SCR. If a localized region becomes more sensitive to dv/dt, however, the device will trigger at this point, and this point must be sufficiently large to handle the initial current surge, or a failure will result. The fact that several dv/dt failures did result leads to the conclusion of localized sensitive regions. It should also be mentioned that the dv/dt measurements were not completed because of the chance of failure during testing.

	BEFORE TEST		AFTER TEST		
	$V_{(BO)}/I_D$	$V_{(BR)R}/I_R$	$V_{(BO)}/I_D$	$V_{(BR)R}/I_R$	V_T (300A)
DEVICE	(V/ma)	(V/ma)	(V/ma)	(V/ma)	(V)
A	600/10	680/1	600/12	660/1	1.2
B	640/10	740/1	600/8	730/1	1.3
C	750/5	790/1	750/7	780/1	1.3
D	700/4	740/1	700/5	720/1	1.3
E	700/5	700/1	680/5	680/1	1.3
F	660/5	720/1	660/5	700/1	1.2
G	700/2	730/1	700/2	720/1	1.2
H	740/1	750/1	720/1	740/1	1.3
I	680/2	680/1	680/2	680/3	1.3
J	700/1	710/1	700/1	710/1	1.2
K	660/5	780/1	660/5	740/1	1.2
L	760/1	760/1	740/1	740/1	1.3
M	770/1	770/1	750/1	750/1	1.2
N	690/1	780/1	660/1	760/1	1.4
O	780/1	680/1	780/2	660/1	1.3
P	720/1	730/1	700/1	720/1	1.7
Q	700/3	620/5	700/5	620/5	1.9
R	730/1	740/1	380/7	380/10	1.2
S	760/1	740/1	250/5	730/1	1.3
T	520/3	760/1	500/1	720/1	——

Note: Devices A thru O are encapsulated
Devices P thru T are subassembly

Figure 7.2 Summary of Forward and Reverse Blocking Voltages and the Forward Voltage Drop at T=25°C.

Figure 7.3 Summary of Device Data

DEVICE	I_{DM}*	I_{RM}*	I_{GM}/V_{GM}+	t_q+	I_H+	dv/dt**	Θ_{JC}+
	V_{DM}=600V	V_{RM}=600V	V_D=5V	I_F=300A		Exp. to 600V	
	(ma)	(ma)	(ma/V)	(μsec)	(ma)	(V/μsec)	(°C/W)
A	37	23	130/3.0	5	15	54	0.043
B	32	30	60/3.5	2	6	—	0.045
C	36	30	59/2.5	3	7	47	0.040
D	28	24	80/2.6	2	12	146	0.037
E	28	28	56/3.9	3	15	190	0.046
F	28	24	61/3.7	4	8	76	0.048
G	22	22	40/1.8	2	6	63	0.042
H	30	28	90/2.2	2	12	316	0.035
I	28	28	88/2.85	3	13	95	0.043
J	28	30	140/3.5	2	13	135	0.036
K	34 (450)	26	32/3.6	2	6	21	0.039
L	22	22	65/2.3	2	10	58	0.040
M	25	26	33/2.3	2	7	35	0.039
N	40 (500)	40	56/4.9	2	7	25	0.036
O	28	36	35/1.9	2	6	24	0.036
P	50	50	185/4.0	<1	—	95	———
Q	70 (540)	70	260/4.9	2	—	79	———
R	14 (200)	22	72/2.6	2	7	95	———
S	10 (200)	21 (400)	56/2.4	2	7	190	———
T	22	24	96/2.5	2	9	220	———

() Indicates Different Applied Voltage Conditions. *T=125°C. +25°C. **50°C

8. SUMMARY AND DISCUSSION OF RESULTS

Two major effects of radiation on silicon were considered, the decrease in minority carrier lifetime and the increase in resistivity. As a result of the above considerations, the following changes in SCR characteristics were predicted for increasing radiation fluence:

1) Avalanche voltage capability increases, while the blocking voltage capability of the device could decrease by punchthrough if the base width is not sufficiently wide to accommodate the depletion region spreading.

2) Forward and reverse blocking currents increase.

3) Forward conducting voltage increases.

4) Holding current increases.

5) Gate current and voltage increase.

6) Turn-on losses increase.

7) Turn-off time decreases.

8) dv/dt capability increases.

In order to design a device which would maintain its blocking voltage capability and switch with reasonable gate currents, the following design philosophy was established:

1) Select a lower starting resistivity to compensate for the expected rise in resistivity.

2) Increase the initial base width to accommodate for the increased space charge region spreading.

3) Diffuse a narrow p-base region.

4) Diffuse a shallow forward blocking junction to establish a high built in field in the p-base region.

5) Diffuse steep concentrations gradients near the emitter junction to establish high injection efficiency.

6) Use pilot gate triggering.

7) Gold diffuse to reduce the initial device sensitivity.

An SCR was designed based upon this philosophy and was shown in Figure 5.10. When this structure was fabricated, however, problems were encountered with the blocking voltage capability of the shallow diffused junction. As a result, the SCR was redesigned with a deeper diffused structure as shown in Figure 6.5. The major differences between the two structures are the deeper diffused forward blocking and a wider p-base region. Since both of these changes are in a direction to degrade the radiation resistance, some consideration should be given to the amount of degradation.

As a result of changes in the design, no degradation in the radiation tolerance of the blocking voltage capability will be experienced. This conclusion is evident, since no changes have been made in the n-base concentration or width. On the other hand, a definite degradation of the gate characteristics will be experienced, as a result of the increase in junction depth and p-base width. The reasons for this degradation are also evident. The p-base transport factor will decrease, since the base width is wider and since the built-in field is reduced for the deeper diffusion. Also, the injection efficiency will decrease (slightly), since the concentrations gradients are more graded. One can see the effect on the transport factor by examining the curve in Figure 5.8. Here, the second set of curves have been calculated for the base of the redesigned structure, i.e., $N_{sp}=5x10^{17}$, $X_{jp}=50$ μmeters, and $W_{Bp}=25$ μmeters. One can see that the theoretical transport factor falls off at a value of lifetime an order of magnitude higher than for the case of the initial design. Consequently, one should expect to see degradation of the gate characteristics at lower radiation levels than with the original structure.

9. CONCLUSIONS AND RECOMMENDATIONS

Based upon the work which has been done on this contract, the following conclusions can be drawn:

1) A high current, 600 volt SCR can theoretically be designed to be radiation resistant to a fluence of 5×10^{13} nvt and 1×10^{6} rads(C).

2) A trade-off was found between gate sensitivity and blocking voltage capability. In order to obtain high gate sensitivity, shallow junctions are required.

3) The shallow diffused, narrow base structure required for the radiation resistant SCR mentioned in 1) is not attainable on large area devices without significant process development.

In order to realize the optimized structure which was theoretically designed during the initial phase of this contract, we recommend that effort be directed toward the process development necessary to:

1) Solve the problems associated with shallow junctions, such that large area devices can be diffused with uniform narrow bases;

2) Solve the problems associated with surface breakdown on high voltage devices diffused with shallow junctions by using a positive contour or by other techniques, such as field limiting rings.

APPENDIX A

OBJECTIVE DEVICE SPECIFICATIONS

Characteristic	Symbol	Condition	Value
Minimum Forward Blocking Voltage	V_{FB}	T_j = 125°C	600V
Maximum Repetitive Peak Reverse Voltage	PRV	T_j = 125°C	600V
Maximum Forward Blocking Current	i_s	T_j = 125°C and rated dc V_{FB}	15ma
Maximum Reverse Blocking Current	i_r	T_j = 125°C and rated dc PRV	15ma
Minimum rms Forward Current	$I_{F(rms)}$		475A
Maximum Forward Voltage Drop	V_{FM}	I_F = 300A dc	1.6V
Maximum Gate Current to Trigger	I_{GT}	V_{FB} = 5V, T_j = 25°C	300ma
Maximum Gate Voltage to Trigger	V_{GT}	V_{FB} = 5V, T_j = 25°C	4V
Typical Holding Current	I_H	T_j = 25°C	25ma
Maximum Turn-off Time	t_{OFF}	I_F =300A, I_R = 20A, T_j = 25°C	30μs
Minimum dv/dt	dv/dt	Exponential to V_{FB}	50V/μs
Maximum Turn-on Time	$t_d + t_r$	I_F =300A, 10-90%, Under High Gate Drive	4μs

APPENDIX B

DEVICE PARAMETER CALCULATIONS

1. Lifetime

A two part model has been used to calculate the minority carrier lifetime. The first is the classical three charge state model proposed by Hall, Shockley and Read, assuming a double level recombination center for gold impurities[8,9]. The second is the two level model proposed by Messenger, assuming an incident neutron fluence and taking empirical data to determine radiation damage constants for silicon[10].

Assuming gold as the dominant recombination center, the minority carrier lifetimes for holes and electrons can be expressed by the following equations[35]:

$$\tau_p = \left[1 + \frac{p\ \beta_p}{n\ \beta_n} + \frac{n\ \alpha_n}{p\ \alpha_p}\right] \cdot \left[N_T \left[\beta_p + \frac{n}{p}\ \alpha_n\right]\right]^{-1}$$

$$\tau_n = \left[1 + \frac{p\ \beta_p}{n\ \beta_n} + \frac{n\ \alpha_n}{p\ \alpha_p}\right] \cdot \left[N_T \left[\alpha_n + \frac{p}{n}\ \beta_p\right]\right]^{-1}$$

Where

N_T = concentration of gold recombination centers,

α_n = probability of electron capture by neutral gold atom,

α_p = probability of hole capture by negative gold atom,

β_n = probability of electron capture by positive gold atom,

β_p = probability of hole capture by neutral gold atom.

In the space charge region of a reverse biased junction, the expression for recombination rate gives rise to a net generation of carriers. For a double level center, this generation rate is expressed in terms of both levels. In the case of gold, however, the acceptor level, E_a, is the dominant level[34], and the expression for the net generation rate reduces to the familiar single level expression,

$$G = n_i \cdot \left[2\sqrt{\tau_{pa}\,\tau_{na}} \quad \text{COSH} \quad \left[\frac{E_a - E_i}{kT} + \frac{1}{2} \ln \left(\frac{\tau_{pa}}{\tau_{na}} \right) \right] \right]^{-1}$$

where

$$\tau_{pa} = \frac{1}{N_T\,\alpha_p} \quad , \quad \tau_{na} = \frac{1}{N_T\,\alpha_n}$$

T = Absolute temperature,
E_i = Intrinsic fermi level,
n_i = Intrinsic carrier concentration.

Messenger has assumed that the lifetime τ results from the independent action of two recombination centers characterized by lifetimes τ_1 and τ_2, such that

$$\frac{1}{\tau} = \frac{\Phi}{K} = \frac{1}{\tau_1} + \frac{1}{\tau_2} .$$

Here the damage constant K and, hence, the low level lifetime can be found for electrons and holes by the following equations:

$$\frac{1}{K_{Ln}} = \frac{C_{p1}\ R_1}{1 + \frac{n_1}{n_o}} + \frac{C_{p2}\ R_2}{1 + \frac{C_{p2}\ P_2}{C_{n2}\ n_o}} ,$$

$$\frac{1}{K_{Ln}} = \frac{C_{n1}\ R_1}{1 + \frac{C_{n1}}{C_{p1}} \frac{n_1}{P_o}} + \frac{C_{n2}\ R_2}{1 + \frac{P_2}{P_o}} ,$$

where

n_o, p_o = Equilibrium electron, hole concentrations.

n_1, p_2 = Electron, hole, concentration with the fermi level were at the trap level.

C_{p1}, C_{n1}, C_{p2}, C_{n2} = Electron and hole capture rates.

R_1, R_2 = Introduction rates of centers.

These parameters were determined by a least square fit to silicon low level lifetime damage constant data.

2. Mobility

The mobility calculation takes into account the effects of lattice scattering, impurity scattering and carrier to carrier scattering. The calculations of lattice mobility is based on the empirical work of Ludwig and Watters[36] which proposes a mobility temperature dependency of $T^{-2.5}$ for electrons, and $T^{-2.7}$ for holes. A paper by DeBye and Conwell[37] presents a relationship for the impurity mobility

$$\mu_I = \frac{2^{7/2}\ K^2\ (kT)^{3/2}\ N_i^{-1}}{\pi^{3/2}\ m_n^{1/2}\ q^3\ \ln(1+b) - b/(1+b)} ,$$

where

$$b = \frac{6K\ m_n\ k^2 T^2}{\pi n\ \hbar^2\ q^2} .$$

The above paper also combines the impurity mobility with the lattice mobility by the relationship:

$$\mu_L = \mu_I \left[1 + z^2 \left[Ci\ z\ Cos z + Si\ z\ Sin\ z - \frac{\pi}{2} Sin\ z \right] \right]$$

where $z^2 = 6\mu_L/\mu_I$ and

Ci, Si are the integral cosine and sine.

The above expressions are used to calculate mobility which is valid under conditions of low level injection.

For high level injection, the effect of carrier to carrier scattering necessitates an additional calculation taken from L. W. Davies(38).

$$\mu_{cc} = \frac{3K^2 (kT)^{3/2}}{\pi^{1/2} 2^{5/2} nq^3} \left[\frac{m_n m_p}{m_n + m_p} \right]^{-\frac{1}{2}} \left[\frac{12K (kT)^2}{K^2 q^2 n} \frac{m_n m_p}{m_n + m_p} \right]^{-1}$$

where, K is the dielectric constant and m_n, m_p are the effective masses of holes and electrons. The high level mobility is then calculated from the equation

$$\frac{1}{\mu} = \frac{1}{\mu_o} + \frac{1}{\mu_{cc}}$$

where μ_o is the low level mobility.

3. Base Transport Factor

The model for this calculation is based on the work of Hoerni and Noyce(17). It takes into consideration the effects of conductivity modulation and built-in fields in the base regions.

The basic equation is the following:

$$\beta = \exp\left[\frac{W}{L_d}\right] \cdot \left[\text{COSH}\ \frac{W}{L_t} + \frac{L_t}{L_d}\ \text{SINH}\ \frac{W}{L_t}\right]^{-1}$$

where W is the width of the base region under consideration

$$L_n = \sqrt{\tau_n\ D_n} \quad , \quad L_p = \sqrt{\tau_p\ D_p}$$

are the characteristic lengths in the n or p base due to diffusion,

$$L_d = \frac{2\ kT}{q\ E_t}$$

is the characteristic length due to the total drift field, E_t, and

$$L_t = \left[L^{-2} + L_d^{-2}\right]^{-1/2}$$

is the total characteristic length.

The total electric field is equal to the sum of the built-in field, E_B, resulting from an impurity gradient and the field resulting from the ohmic drop across the base region E_J

$$E_T = E_B + E_J$$

$$= E_B + \rho J$$

where ρ is the resistivity and J is the current density.

It can be seen that in the absence of a built-in or an ohmic field, the equation for β reduces to the familiar form of

$$\beta = \text{SECH}\left[\frac{W}{L}\right] .$$

4. Avalanche Voltage Calculation

Avalanche voltage, depletion region widths, and the multiplication factors are calculated assuming a complementary error function diffusion profile.

To determine the depletion region widths as a function of a reverse voltage, Poisson's equation is solved in one dimension

$$\frac{d^2\psi}{dx^2} = \frac{q}{K\,\varepsilon_o}\,(N_d - N_a)$$

or

$$\frac{dE}{dx} = \frac{q}{K\,\varepsilon_o}\,(N_d - N_a) .$$

This equation, along with the condition of charge neutrality,

$$p\text{-}n + N_d - N_a = 0$$

is sufficient to solve for the electric field, E, the blocking potential ψ and the depletion layer widths on the n and p side of the junction.

The multiplication factors are determined from equations derived by Howard[39] and used by Kokosa[1].

$$M_n = \left[1 - \exp\left[-\psi(W)\right] \int_o^W \alpha_n(x) \exp\left[\psi(x)\right] dx \right]^{-1}$$

$$M_p = M_n \exp\left[-\psi(x)\right]$$

$$M_{sc} = \frac{M_n}{W} \int_o^W \exp\left[\psi(x)\right] dx, \quad \text{where}$$

$$\psi(x) = \int_o^x \left[\alpha_n(\omega) - \alpha_p(\omega)\right] d\omega$$

M_n, M_p and M_{sc} are the multiplication factors for electron hole and space charge generated current components, and α_n and α_p are the impact ionization rates for electrons and holes.

Since avalanche breakdown occurs when the multiplication factors approach infinity, it can be seen that the general condition for avalanche breakdown is

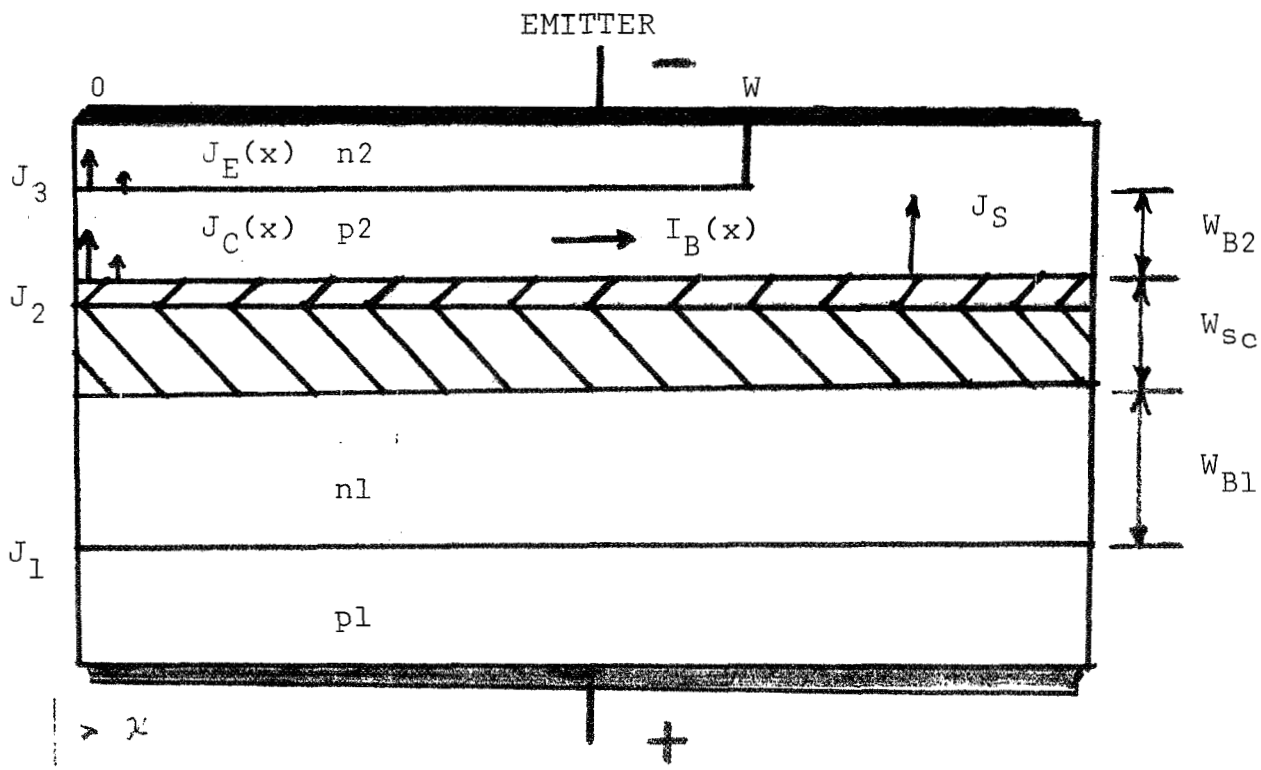
$$\exp\left[-\psi(x)\right] \int_o^{W'} \alpha_n(x) \exp\left[\psi(x)\right] dx \approx 1$$

where W' is the width of the depletion width at which breakdown occurs.

APPENDIX C

LATERAL BASE BIASING CALCULATION

The model used to calculate the effects of lateral base currents is pictured below. Here the portion from the center most point of the emitter junction to the edge of the short is analyzed.



Model for the Two Dimensional Analysis of the Lateral Base Biasing Effect.

Four current components have been indicated. $I_B(x)$ is the lateral base current per unit depth passing under the emitter to the short. The total base current is the sum of all the collected current components $J_C(x)$ across the emitter, minus the emitter current components, $J_E(x)$.

More specifically, at any point x

$$d\, I_B(x) = [J_c(x) - J_E(x)]\, dx \qquad \text{(C-1)}$$

so the total base current becomes

$$I_{Bo} = \int_o^W I_B(x)dx$$

$$= \int_o^W [J_c(x) - J_E(x)]\, dx\,. \qquad \text{(C-2)}$$

The collected current component $J_C(x)$ and the short current component J_S can be found from the equations

$$J_C(x) = J_S + \frac{M_n\, \alpha_n(x)\, J_E(x)}{1 - M_p\, \alpha_p(x)} \qquad \text{(C-3)}$$

$$J_S = \frac{J_o}{1 - M_p\, \alpha_p(x)} \qquad \text{(C-4)}$$

which are similar to the current equation for the pnp in the reverse blocking calculation. The emitter current component $J_E(x)$ is determined from the standard diode equation as a function of the lateral base bias V(x) caused by the flow of base current, i.e.

$$J_E(x) = J_o\left[\exp\left(\frac{qV(x)}{kT}\right) - 1\right] \qquad \text{(C-5)}$$

where

$$J_o = q \frac{D_n}{L_n} \frac{n_i^2}{N_p} \text{COTH}\left(\frac{W_B}{L_n} \right) + q \frac{D_p}{L_p} \frac{n_i^2}{N_n} \text{COTH}\left(\frac{W_E}{L_n} \right) \quad \text{(C-6)}$$

N_p and N_n are the doping concentrations in the p-base and emitter, respectively.

The effect of the short can be seen by considering the bias on the emitter junction from x=W to x=o. At x=W, the emitter edge and the emitter junction have zero bias and, hence, $J_E(W)=o$ by Equation (C-5). There is, however, a short current component at x=W equal to the current through the pnp portion of the device. The value of $J_C(x)$ from $o<x<W$ is equal to this short current, plus a quantity

$$\frac{M_n \alpha_n J_E(x)}{1 - M_p \alpha_p}$$

as can be seen in Equation (C-3). Thus, when $J_E(x)$ is small compared to $J_C(x)$, there is a base current which flows along the emitter given by Equation (C-2). This $I_B(x)$ causes a voltage drop across the emitter which biases the emitter with a voltage given by

$$V(x) = \int_o^x \frac{I_B(\xi)\, d\xi}{\sigma_{p2}\, W_{B2}} \quad \text{(C-7)}$$

This bias causes $J_E(x)$ to increase by Equation (C-5) which in turn causes $J_C(x)$ to increase by Equation (C-3). At x=o, the emitter current will reach a maximum, since V(x) is a maximum at that point. When the current at x=o reaches a level sufficiently high to cause

$$\alpha_n(o) + \alpha_p(o) = 1$$

the turn-on current will be known.

This type of calculation is useful to examine the effect of shorts in a given structure against forward blocking currents or dv/dt currents. If a gate current component is added to Equation (C-2), the same analysis can be used to calculate the gate currents to turn-on.

11. SYMBOLS

α_n, α_p	-	Gain of the npn and pnp transistor components, respectively.
β_n, β_p	-	Base transport factor in the npn and pnp, respectively.
di/dt	-	Rate-of-rise of anode current.
dp/dx	-	Concentration gradient of majority carriers.
dv/dt	-	Rate-of-rise of anode voltage.
E_i	-	Intrinsic energy level.
E_x	-	Electric field in the x direction.
γ	-	Injection efficiency.
I_A	-	Total current through the anode.
I_D	-	Forward blocking current.
I_G	-	Gate current.
I_H	-	Holding current.
I_o	-	Junction Leakage current.
I_R	-	Reverse blocking current.
I_{sc}	-	Space charge generated current
J	-	Current density
k	-	Boltzmann's constant.
L_n, L_p	-	Diffusion length for electrons and holes, respectively.
M_n, M_p, M_{sc}	-	Avalanche multiplication coefficients for electron, hole, and space charge generated currents, respectively.

n_i - Intrinsic carrier concentration.

N_D, N_A - Doping concentration for donors and acceptors, respectively.

N_T - Total number of recombination centers.

N_{sn}, N_{sp} - Diffusion surface concentration for n and p type, respectively.

ϕ - Radiation fluence.

$\Delta N/\Delta\phi$ - Carrier removal rate.

nvt - A unit of neutron fluence equal to the time integral of the neutron flux. (Equivalent to n/cm^2).

n, p - Electron or hole concentrations, n or p type silicon, or as subscripts meaning electron or hole.

ρ, σ - Resistivity or conductivity.

q - Electronic charge.

R - Recombination rate.

rad - A unit of radiation exposure equivalent to 100 ergs of energy transferred to 1 gram of a given material.

τ_n, τ_p - Lifetime of electrons and holes, respectively.

t_q - Turn-off time.

T - Absolute temperature.

V_D - Forward blocking voltage.

V_R - Reverse blocking voltage.

V_T - Forward conducting voltage.

$V_{(BO)}$ - Forward breakover voltage.

$V_{(BR)R}$ - Reverse breakdown voltage.

ω_B, W_{sc} - Width of base or space charge region, respectively.

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