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SOLDER-CIRCUITRY SEPARATION PROBLEMS ASSOCIATED WITH PLATED PRINTED CIRCUIT BOARDS

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16. Abstract

This report covers a detailed investigation of the problems of solder-circuitry separation associated with plated printed circuit boards. Gold and copper platings were studied and various circuitry conditions were evaluated, including tinned laminate copper, plated copper with brightener additives over laminate copper, and gold overplate. The laboratory test program included a technical survey, failure analyses, metallographic examinations, chemical analyses, and thermal conditioning. Factors pertinent to the separation mechanism were isolated and aging/strength studies were performed. Conclusions of these tests will be implemented in NASA documentation and imposed on future space hardware.

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SUMMARY

A detailed investigation (including failure analyses, metallographic examinations, chemical analyses, and a technical survey) was conducted to isolate, define, and solve solder-circuitry separation problems encountered on printed circuit (pc) boards. Boards that exhibited solder-circuitry separation were double-sided circuitry plated with copper that contained brightener additives and overplated with acid cyanide gold that contained cobalt. The circuit sides of the boards were wave soldered and the component sides were hand soldered. Both sides, including the plated through holes, exhibited solder separation.

Research into gold plating solutions revealed the existence of a polymer that is codeposited with acid cyanide gold plating solutions. Laboratory tests confirmed that this polymer could be isolated by a microchemical process. It was concluded that elevated temperature will, in time, concentrate the codeposited polymer at the solder-circuitry interface as a transparent film. A similar failure mechanism is produced by brightener additives in copper plating solutions.

It is recommended that copper plating solutions containing brighteners and other organic additives and cyanide gold plating solutions be suspended from future pc board fabrication processes. When gold plating is mandatory, it is recommended that a noncyanide gold be specified and that it be removed prior to soldering. Further research is required to chemically identify the organic polymers and to recommend a selection of acceptable gold and copper plating solutions for use in printed circuit board fabrication.

Detailed information and failure analysis data are provided in this report. Data on previous manifestations of the problem in other systems and electronic hardware are also included. Parallel analyses by Marshall Space Flight Center (MSFC) contractors and previous investigations by industry were incorporated into the overall effort.

INTRODUCTION

Malfunction of a Saturn V Launch Checkout Computer System at Kennedy Space Center (KSC) was traced to a discontinuity caused by the separation of a soldered connection from associated circuitry on a printed wiring board. Investigation of additional connections on this board and on boards from other launch checkout computer systems revealed similar widespread solder-circuitry separations.

As the widespread nature of the separation problem and its potential impact upon critical flight and GSE systems became more apparent, a broad testing program was initiated. The program was directed toward a short range analysis to correlate the failure mechanism and a long range effort to evolve revisions to material and process specifications.

The test program to solve the problem included environmental and comparative tests to isolate the factors pertinent to the solder-gold separation mechanism and chemical analysis of the gold plating to correlate industry findings as to the nature of these factors. Metallographic and metallurgical examinations, push-pull testing, and other techniques were used to support the failure analysis and investigation program.

SYSTEM/COMPONENT FAILURES

Saturn V Launch Checkout Computer

GENERAL

The failure of a 110A Launch Checkout Computer during Saturn V countdown tests at KSC was traced to an intermittent soldered connection on a computer module board. Gross solder-circuitry separation observed on this board led to investigation and analyses of other module boards used in the computer. Various circuitry conditions were evaluated, such as tinned laminate copper, plated copper with brightener additives over laminate copper then overplated with gold, and pyrophosphate copper without additives over laminate copper and gold overplate. Descriptions and analyses of the boards involved in the investigation are listed in Table 1. Details of the findings are given below.

TABLE 1. RCA 110A COMPUTER MODULE BOARDS

		Computer Location			Coating		Visual Appearance		Circuitry Plating			Mechanical Test Results	
Board Type	Serial Number	Huntsville	MSFC, Bldg. 4373	MSFC, Bldg. 4436	Urethane	MFP (Moisture Fungus Proof)	Dark Discoloration	Slight or no Discoloration	Solder — Over Laminate copper	Gold — Over Plated copper	Gold — Over Plated copper[a]	Lead/Solder Separation	Solder/Copper Separation
2110029-501	13			X		X	X		X			X	
2110103-501	27			X		X	X		X			X	
2110103-501	31			X		X		X	X			X	
2110129-501	4			X		X		X	X			X	
2110129-501	561			X		X		X	X			X	
2110047-504	3673		X		X		X		X			X	
PA2808A-504	W0234		X		X		X		X			X	
PA2808A-504	W0550		X		X		X		X			X	
2110127-504	10958		X		X		X			X			X
2110127-504	11875		X		X		X			X			X
2110129-504	18780		X		X			X		X			X
2110133-504	5671		X		X			X		X			X
2110129-504	19258[b]		X		X			X		X			X
2110131-504	10049		X		X			X		X			X
2110131-504	10240		X		X		X			X			X
2110133-504	5346		X		X		X			X			X
2110129-504	19078		X		X		X			X			X
2110103-503	3103	X			X		X			X			X
2110129-503	3715	X			X		X			X			X
2110129-504	10499		X		X		X				X	X	X[c]
2110129-504	20679		X		X		X				X	X	X[c]

a. Pyrophosphate-plated copper without brightener additives.
b. In storage since 1966 — rejected for damaged transistor solder pads.
c. On component side of the board only.

Initial Problem Board

This board (type 2110029, S/N 10059), normally referred to as a driver, was evaluated, and the failure was isolated to a soldered connection of a diode, CR21, located in a cluster of components. A slight probe pressure exerted upon this diode produced a discontinuity in its circuit. The double-sided board displayed discoloration of the urethane conformal coating and the substrate in the area of the clustered components, an indication of elevated temperature. The circuit side was wave soldered and the component side was hand soldered. Overall views of both sides of this board and the point of failure are shown in Figures 1 and 2. A higher magnification of the diode connection after urethane removal is shown in Figure 3.

The lead on the component side of this connection was cut and a slight force was applied to its free length; the clinched lead portion and the solder mass were raised completely off the solder pad (Fig. 4). The copper is bare except for a few small areas that exhibit some adherence of solder. This separation is a classic example of solder-circuitry interfacial deterioration and is not a result of differential thermal expansion forces.

An attempt to remove the darkened urethane from the circuitry in area B of Figure 2 resulted in "lifting" the solder coating along with the extremely tacky urethane conformal coating (Fig. 5). Also evident is the considerable discoloration of the copper from which the solder had "lifted."

Investigation of Additional Computer Boards

Based upon the investigation of the initial problem board, 21 additional boards were selected from other operating 110A computer systems (Table 1). These boards represented a cross section of the circuitry conditions used during manufacturing. All the gold-plated boards were double-sided circuitry of plated copper over laminate copper, and the nongold-plated boards were single-sided circuitry of tinned laminate copper.

Two types of nongold-plated, single-sided boards were used in the Launch Checkout Computer systems. These boards had solder coated circuitry. One type was populated with "baby boards" attached to a "mother" board and were moisture/fungus-proof (MFP) coated. The other type, urethane coated, consisted of components mounted on one side with connections wave soldered to the circuitry on the opposite side. Both types showed severe discoloration, caused by the elevated operating temperatures, in clustered component areas. Since gold or copper platings were not involved in the circuitry processing, specific emphases were given to the solder-circuitry bonding conditions. It was revealed that bond of the solder coatings and the soldered connections were of uncompromised integrity with no evidence of solder-circuitry separation. Thus, it was apparent that heat, coupled with time, was not the only factor causing the solder-circuitry separations.

The only evidence of solder connection deterioration visually observed on the gold plated boards were darkened gold areas adjacent to the solder. An example of this condition is shown in Figure 6. The metallographic examination of this connection confirmed that the darkened gold areas were indicative of solder-circuitry separation.

The "new generation" boards, copper plated with pyrophosphate without brightener additives, also exhibited darkened gold adjacent to solder similar to that shown in Figure 6. Metallographic examination confirmed solder-circuitry separation on the component side only.

ANALYSIS OF OPERATING TEMPERATURES

It was not possible to determine what the normal operating temperature of the module boards should be during the operation cycle of a 110A computer. Even the manufacturer's field service personnel were hesitant to venture allowable operating temperature extremes. However, it was evident by the severely discolored areas that temperatures were exceeding the design temperature limits. An operational temperature test was conducted at MSFC on the 504 Computer System to determine the maximum temperatures. Thermocouples were attached beneath components in discolored areas and on corresponding areas on the circuit side next to the board material; then, the disturbed areas were urethane coated. The maximum temperature reached during this test was 90°C. This temperature was recorded with the internal computer air conditioner in operation. However, previous and subsequent tests have shown that this board material does not discolor as severely at this temperature. Therefore other factors may be pertinent to the board discoloration condition caused by obviously higher temperatures. These factors may be a stoppage of the conditioned air flow or current surges caused by circuit malfunction.

MECHANICAL TESTS

Plated-Through-Hole Connections — Copper Plated/Brightener Additives/ Gold Overplate

Pull tests were performed only on the plated-through-hole connections that were plated with copper containing brightener additives and gold overplate.

The connection strengths were obtained by pulling on the free length of a soldered lead with its clinched portion clipped. The connection strength was established when the lead pulled out of the plated-through-hole or when the lead broke.

Pull test strengths of plated-through-hole connections that showed solder-circuitry separation ranged from 2.72 to more than 9.08 kg. The strengths of these connections were higher because the uneven plated hole surfaces caused mechanical "locks" between wall platings and solder during withdrawal of the leads and solder mass from the holes. An example of pull-tested connections exhibiting gross and complete solder-circuitry separation is shown in Figure 7. Note the bare discolored copper in the holes as pinpointed by the arrows. Pull-tested connection strengths that showed no solder-circuitry separation ranged from 11.35 to more than 22.68 kg.

Non-Plated-Through-Hole (Single Sided) Connections — Copper Plated/Brightener Additives/Gold Overplate

Push tests were performed on connections that were soldered only on the circuit side. By applying a force toward the board, in the direction of the clamped free lead length, on the component side, the connection strength was established. The push test results showed a wide variation in strengths and varied from less than 0.23 kg to approximately 7.80 kg. Some solder pads associated with these connections exhibited complete solder separation while others showed only small areas of bare copper of varying tarnish hues. The urethane coating flowed into the holes and restricted the movement of the leads. This accounts for higher strengths of the solder-circuitry connections that were completely separated.

A connection selected for push testing that met all visual acceptance criteria is shown in Figure 8. This same connection after push testing is shown in Figure 9. Note the completely bare copper pad pinpointed by the arrow. The lead with the solder mass, including the thinly feathered solder, is pinpointed by the double arrows. This solder pad exhibits a lesser degree of copper discoloration than most push-tested connections.

Plated-Through-Hole Connections — Copper Plated/Pyrophosphate Without Additives/Gold Overplate

The "new generation" boards exhibited no solder-circuitry separation on the wave soldered circuit side. The action of the wave solder system washed the gold off the circuitry into the solder pot. Either the leads would push out of the solder, or pads would lift along with the solder and leads, or the leads would bend; all of which is indicative of good solder-circuitry bonding. However, on the gold-plated component side, widespread solder-circuitry separation was observed. The separation was similar to that shown in Figure 9.

Single-Sided Circuitry — Tinned Laminate Copper

All tinned laminate copper boards exhibited acceptable push test results even in severe thermally discolored areas. Both the urethane and MFP coated boards showed similar acceptable push test results (i.e., pad lifted, lead pushed out of the solder, or the lead bent under the applied force).

METALLOGRAPHIC EXAMINATIONS

Metallographic examinations were made of connections of all circuitry conditions. The boards that were gold plated over plated copper containing brightener additives showed the most severe solder separations. The boards that were gold plated over plated pyrophosphate copper without brightener additives showed solder separation on the component side of the boards only. The tinned laminate copper boards showed no solder separation problem at all. Details of metallographic examinations of the various conditions observed are given in the following paragraphs.

Gold-Over-Copper

Plated-Through-Holes — With Copper Brightener Additives. A cross section of a plated-through-hole revealing a complete solder-circuitry separation is shown in Figure 10. Associated solder pads also showed similar solder separation. Note the irregular plated surface that caused mechanical restriction during pull tests and accounted for greater strength readouts. The connection shown in Figure 6 displayed a dark discoloration between the solder and the gold plating. Metallographic examination (Fig. 11) showed a gold rich solder as evidenced by acicular crystals dispersed throughout the solder mass. The gold-tin intermetallic shows separation from the copper and from the gold plating.

Single-Sided Connection — With Copper Brightener Additives. A connection displaying complete visual acceptance criteria is shown in Figure 12. This is a single-sided connection in a thermally discolored clustered component area. Metallographic examination showed uniform and complete separation from the circuitry, as illustrated in Figure 13. To provide a temperature variable comparison, a connection that was away from the discolored component clusters was selected. This connection was CR9 from the initially failed board. A cross section of this connection is shown in Figure 14. The integrity of this connection was not compromised during its operating life span, which was judged to be in excess of 5 years. This is indicative of the effect of temperature as a factor in the solder-circuitry separation.

A connection with a solder crack at the heel of a lead clinch from an area of discoloration was investigated, and it is shown in Figure 15. To result in such a crack, the solder bond to the copper pad was greater at this time than the strength of the solder. After exposure to increased temperatures, even the strain relieved solder eventually separated from its pad.

Plated-Through-Holes — Without Copper Brightener Additives. The "new generation" connections on the circuit side revealed acceptable bonding, as shown in Figure 16. This photomicrograph identifies the lead, solder, copper-tin intermetallic compound, plated copper, and laminate copper. Similar acceptable conditions existed in the plated-through-hole. However, on the component side, the separation was gross, as shown in Figure 17. A photomicrograph at higher magnification is shown in Figure 18. Note that some gold is still adhered to the copper. This photomicrograph is a classic example of the solder structure observed during metallographic examinations of connections on the component side of all gold plated boards. It is indicative that gold was not removed for the soldering operation.

Nongold-Plated Laminate Copper

The examinations repeatedly revealed acceptable solder-to-copper bonds, even in the most severe thermally discolored areas. A cross section of a specimen is shown in Figure 19. This photomicrograph is representative of all connections investigated on these boards.

Component Failures

Although the Saturn V Launch Checkout Computer is a classic example of the widespread solder-circuitry separation problems, this condition has been observed on soldered connections of other components. Representative examples of these occurrences are presented here to further identify the overall causes for the solder-circuitry separation.

PRESSURE TRANSDUCER TEARDOWN ANALYSIS

This unit was a part of the ECA package from a J-2 engine and was subjected to a teardown analysis[1] to isolate conditions that would create unstable performance. Particular emphases were placed on the integrity of the interconnections. Only those problems associated with the solder-circuitry separation are highlighted.

The conductors on the printed wiring board of this transducer were copper plated then overplated with a gold plating of approximately 0.00076 cm thick. Darkened areas between the gold plating and the solder were observed (Fig. 20). A cross section of this connection (Fig. 21) reveals definite solder separation from associated circuitry. Note that some gold plating is still present on the plated circuitry beneath the solder mass. These illustrations typify the overall connections on the transducer pc boards.

EVALUATION OF SOLDER JOINT FAILURES ON SWAGED, GOLD-PLATED TERMINALS[2]

The evaluation performed on gold-plated, single-sided circuitry boards was associated with the malfunctions occurring on Saturn V telemetry (270 Multiplexer) equipment. Again as observed on pc boards of other equipment, when connections were soldered to the gold, joints showed a "dark banding" condition and partial solder-to-gold separation where the solder terminates on the gold-plated surface. A dark band between solder and gold plating is shown in Figure 22. Metallographic examination of this connection revealed a condition similar to that shown in Figure 21. The circuitry on this board was laminate copper. A "push tested" connector showing "clean bond line separation" is shown in Figure 23. Metallographic examination of this separated connector showed the separation to be between the gold plating on this terminal and the gold-tin intermetallic.

A terminal that exhibited no visual surface defects was also metallographically examined. A gross solder-terminal separation was observed during this examination, and it is shown in Figure 24. This separation occurred between the remaining gold plating on the terminal and the gold-tin intermetallic.

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1. Pasciak, A. M.: Teardown Analysis of Pressure Transducer S/N 7957A (ECA Package). Memorandum to R. W. Neuschaefer, R-QUAL-ARM, Marshall Space Flight Center, Sept. 13, 1968.

2. Donnelly, J. H., and Burka, J. A.: Evaluation of Solder Joint Failures on Swaged, Gold Plated Terminals. Engineering Report, S&E-QUAL-ARM-ER-17, Sept. 16, 1969.

Failure Analysis Conclusions

To this point, the investigation showed the existence of two separate and unique problems. While normal cracking of solder joints (due to external stress) occurs within the solder [1], the phenomenon investigated here is the separation of solder and circuitry at the interface. The two problem areas are the brightener additives used in some copper platings and cyanide acid gold with hardener additives such as cobalt.

COPPER BRIGHTENER ADDITIVES

The significance of the effects of brightener additives on the soldered connections was illustrated in the comparison of wave soldered, gold-plated boards, where all the gold plating is washed into the solder pot. The boards having copper plating with brightener additives showed gross solder separation, while those having pyrophosphate copper without additives showed no separation. RCA [2] has conducted tests subsequent to the initial problem and has reached similar conclusions.

GOLD PLATING

The effects of gold plating on the solder separation were highly suspected at this point but were not fully conclusive. The fact that solder connections showed separation on the component side of the pyrophosphate copper plating without additives made gold a most likely candidate as contributor to the problem. However, laminate copper circuitry is in widespread use in pc board fabrication. The questions then arose: Would separation occur if laminate coppers were gold plated and hand soldered? Would conditions conducive to solder separation still be present if the gold were erased in the soldering areas?

Therefore, a laboratory test program to establish the contribution of gold plating to this major problem was proposed.

ANALYSIS OF GOLD PLATING EFFECTS

Technical Survey

A technical literature survey of the solder-circuitry problem revealed that not only the gold platings but also copper platings have plagued the manufacturers and fabricators of electronic printed wiring boards and hardware. Researchers and investigators conclude that gold platings in excess of 0.00012 cm thick reduce strengths of soldered connections.

W. B. Harding and H. B. Pressly [3] show that as the gold plating was increased from 0.00010 cm the strength of joints between metal strips decreased, with separation occurring in the gold-tin intermetallic. They state, "For plating thickness of approximately 0.25 mils (250 microinches), with soldering temperatures of approximately 500° F (260° C) and higher, the fracture occurred at the solder-copper interface, exposing bare copper."

S. D. Ebneter [4] reports a distinct trend toward porosity and reduced strengths of solder-over-gold connections as the gold plating thicknesses were increased. He also points out "a successive degradation in the appearance of the solder with successive increase in the gold plating thickness."

From her investigation, Gloria B. Munier [5] states, "An unsuspected polymer is codeposited at the cathode with all hard golds, and in lesser quantities, with soft golds that are plated from acid cyanide systems." By microchemical manipulation she has successfully separated an amorphous transparent polymer from the plated golds.

C. H. Kreck [2] reports that when normal quantities of brightener additives were added to copper platings, solder-copper separation occurred in approximately 168 hours at 125° C.

Laboratory Tests

GENERAL

The data and information gathered from technical survey and from the previous systems and component problems and failures show that the gold plating was the primary cause for porous, brittle, and weakened soldered connections. The test program was undertaken to furnish data and results on the effects of hand soldered connections over the gold plating when they were exposed to elevated temperatures over controlled increments of time. The design of this test permitted isolation of gold plating as a major contributing factor to solder-circuitry separation.

MATERIALS

Leads

The lead materials selected are those commonly used in printed wiring board assembly:

1. Gold-plated Kovar[3] 0.043 cm
2. Nickel 0.051, 0.063 cm
3. Copper 0.081 cm

Printed Circuit Boards

The design of the boards was compatible with lead sizes. The conductor foil was 56.6g laminate copper with G-10 glass epoxy material as a substrate. The board groups were: A — bare copper; B — gold plated copper; and C — erased gold in soldering areas. For each group, six boards were prepared, to furnish sufficient sample size. The copper conditions, lead materials, and number of connections are shown in Table 2. The gold plating used was cyanide acid gold containing cobalt, commonly known as hard gold. It was deposited approximately 0.00064 cm thick as shown in Figure 25. See the appendix for detailed soldering procedures performed on these pc boards.

TABLE 2. LABORATORY TEST BOARDS

Lead Material	Copper Condition and Number of Connections		
	A — Bare	B — Gold Plated	C — Erased Gold Plate
Kovar	162	162	162
Nickel	108	108	108
Copper	144	144	144
TOTAL	414	414	414

3. Kovar is a proprietary name commonly used for nickel-iron-cobalt composition lead material compatible for hermetic seals with hard glass.

VISUAL INSPECTION

Visual inspection of the completed boards revealed the connections on bare and erased gold boards to be free of voids and porosity. They were shiny and filleted to a low dihedral angle. The connections on the gold-plated boards were grainy, dull grey, and porous. The solder masses generally exhibited irregular solidification lines giving the overall connection a "fried egg effect." A view of a solder connection of each board condition is shown in Figure 26. Note the similarity in the lustre and smoothness of the bare copper and erased gold connections. The gold plated connection exhibits dull appearance and porosity in the solder and solidification lines. This is a normal appearance when soldering directly to the gold plated surfaces. The solder-over-gold connections were not reworked because the gold plating effects were being evaluated.

THERMAL TESTS

Previous investigations and data have shown that gold plating causes no serious deleterious effects upon connections over an approximate 5-year span at temperature less than 71.0°C. Therefore a temperature of 100°C was selected to closer correspond to operating temperatures known to exist in some areas on various printed wiring boards. Periodic inspections, mechanical push tests, and metallographic examinations were performed during this test to incrementally detect any change in conditions. The tests established that no change in the solder-circuitry conditions could be attributed to the lead materials.

MECHANICAL TEST RESULTS

Thermal aging of the solder-to-gold connections showed a significant strength degradation after only 166 hours of exposure to 100°C temperature. Progressively erratic and weaker strengths were experienced until termination of this test. The connections of both the bare copper and erased gold remained approximately constant in strength. A comparison of the average strengths within each group is shown in Figure 27. The ability of a system to perform reliably in its selected environment may be dependent upon the continued level of interconnection strengths. The minimum push strength within each group is shown in Figure 28. Note the relativelv weak connections in group B of approximately 0.91 kg as compared with groups A and C of 4.99 kg.

These connection strengths were compiled using the mechanical push tests. At no time did the solder separate from pads in groups A and C. Either the lead pushed out of the solder or, as in the majority of the cases, the pad lifted with the lead and solder. However, in the B group, partial solder separations occurred after 166 hours in thermal test. These separations displayed a darkened pad surface where the solder had separated. The solder remaining on the pads displayed a coarse and grainy structure. An example of this is shown in Figure 29. Another connection that separated after 658 hours in thermal test (Fig. 30) evidences bare copper on a portion of the pad. The first solder separation visually detected under the full length of the clinched lead was after 1054 hours in test. This connection is shown in Figure 31. Note that some solder is bonded to the side of the pad. This is because the unwanted copper on the board was etched after it was gold plated, leaving the sides with bare laminate copper which retained the solder during the thermal test. Similar separations were observed after the final inspection at 2230 hours in test, except that more of the bare copper on the pads was visible at this time.

METALLOGRAPHIC EXAMINATIONS

Metallographic examinations were performed on selected specimens at each of the evaluation intervals. However, only those photomicrographs that are significant when changes were observed are presented. This investigation has shown that prior to the temperature test all connections displayed good solder adhesion or bond to the solder pads. These are shown in Figure 32. In the gold-plated connection the solder appears to be bonded in part to the gold plating. Note the large void caused by outgassing of organics where the gold plating terminates. Voids were generally evidenced on all solder-to-gold connections that were cross sectioned. The bare copper and erased gold connections were similar in solder structure and copper-tin intermetallics and displayed complete and acceptable bonding characteristics.

Solder separation was first observed at the second evaluation interval (166 hours), and then only on the solder-to-gold B — group boards. This separation, shown in Figure 33, is approximately 0.00025 cm thick. Separations of varying degrees were observed on these boards until termination of the test. The connections on the bare copper and the erased gold boards have shown acceptable bondings throughout the examinations. Normal growth of the tin and the lead phases in the solder was observed as the test progressed. These connections after 2230 hours are shown in Figures 34 and 35. The increased thickness of copper-tin intermetallic is also a normal condition associated with elevated temperatures. Figure 36 shows a solder/gold separation on the C board, away from the erased area. Note the gold plating still on the copper as shown between the arrows. Not all the connections on the soldered-to-gold B boards revealed completely unbonded solder. An erratic separation pattern was noted with dark bands adjacent to the solder in many instances. Photomicrographs of B board separations that were more commonly seen are shown in Figures 37 and 38. Voids and widespread porosity in the solder beneath the clinched lead are in evidence. Note the bare copper surface between the arrows in Figure 38.

Upon completion of the test (2230 hours), attempts were made to separate the gold plating from the copper on an unsoldered conductor. Roll-backs, peeling, probing, and tape tests failed to separate it. Metallographic examination of the plating-copper interface revealed the plating to be acceptably bonded to the copper similar to that shown in Figure 25.

MICROCHEMICAL ANALYSIS

One of the most revealing tests of the structure of cyanide gold platings containing hardener additives was conducted by Gloria B. Munier [5]. She discovered that a polymer was codeposited with hard gold platings.

To determine whether a similar polymer was codeposited with the gold plating used on the test boards, a similar test was performed. Gold platings away from the soldered areas and platings from which the solder had separated were used. Detailed procedures are listed below.

1. Samples of the gold plating and the laminate copper were removed from test board.

2. Any visible solder was snipped off (when applicable).

3. The underside of the copper was carefully scraped to remove any adhesive.

4. The specimens were rinsed in distilled water and air dried.

5. The specimens were placed in a nitric acid solution to remove all the copper.

6. The gold plating fragments were rinsed with distilled water, air dried, and inspected for any copper residue.

7. The gold was then placed in aqua regia fuming chamber and was not disturbed until solubilized.

8. A cover slide was placed over this mass; small water droplets were directed at one end of the slide and withdrawn at the other end with a pointed filter paper. This was repeated several times.

Upon completion of this test, microscopic investigation revealed a transparent mass of polymer. By using a transmitted light, this polymer was photographed (Fig. 39). This polymer is from the gold plating from which solder was separated. Gold plating away from soldered connections yielded a similar polymer.

PROBLEM ANALYSIS AND CONCLUSIONS

The results of the tests performed show that solder separation from laminate copper circuitry can be produced by an acid cyanide gold plating over the copper. Similar separation can be produced by over-plating the laminate copper with a copper plate containing brightener and leveler additives. To a great degree, the rate of separation, or whether separation occurs, is dependent upon two factors — time and elevated temperature. These factors, in conjunction with brightener additives in copper plating solutions, or cyanide acid gold plating, with and without hardeners, will produce solder separation from printed circuitry. The time required for separation to occur is interdependent upon the temperature level and the specific composition of the plating solutions.

The existence of separations was supported by mechanical push tests in conjunction with metallographic examinations. The push tests did not accurately relate the maximum solder-circuitry bond strengths because of lead bending or pad lifting.

Further conclusions derived from the failure analysis, industry survey, and laboratory tests are summarized below:

1. Solder separation from circuitry has been experienced in the past on systems using printed circuit boards that were gold plated over copper plating containing additives. This resulted in gross solder separation from circuitry in areas where temperatures were estimated to be greater than 71.1°C for an approximate duration of 5 years.

2. RCA's [2] tests verified solder-circuitry separation when copper platings with brightener additives were used. At the same time and under the same conditions, no deleterious effects resulted when soldering to bare laminate copper or to pyrophosphate plated copper without additives.

3. Laboratory tests of solder connections to erased gold over laminate copper and to bare laminate copper produced no separation after 2230 hours at 100°C.

4. Laboratory tests of solder connections to gold plating over laminate copper produced widespread solder separation within 166 hours at 100°C.

5. Microchemical analysis performed on gold plating containing cobalt revealed that an organic polymer was codeposited with the gold.

6. It is concluded that the solder-circuitry separation, caused by either soldering to acid cyanide gold or copper plating with organic additives, is not an immediate occurrence following the soldering operation. It is a function of time and elevated temperatures which produces a progressive weakening of the bond at the solder-circuitry interface and ultimately an electrical failure.

RECOMMENDATIONS

Based upon the failure analysis and laboratory tests and supported by industry tests, the following recommendations are made. These recommendations are pertinent only in reference to soldered interconnections on printed circuit boards. It is recommended that:

1. No copper platings, including plated-through-holes, be allowed with copper solutions containing brightener or leveler additives.

2. No acid cyanide gold plating be permitted. Where it is mandatory to use gold, it shall be noncyanide gold. Where solder is to be applied, the gold must be completely removed in that area.

3. A qualified products list of acceptable platings, copper and gold, be compiled for use in printed circuit board fabrications. This will necessitate testing of proprietary solutions to determine the existence or absence of the separation phenomenon.

4. Further in-depth research be conducted in this relatively new problem area to further identify potential problems related to soldering to copper, gold, and other platings.

George C. Marshall Space Flight Center
National Aeronautics and Space Administration
Marshall Space Flight Center, Alabama, October 19, 1970
933-50-07-00-62

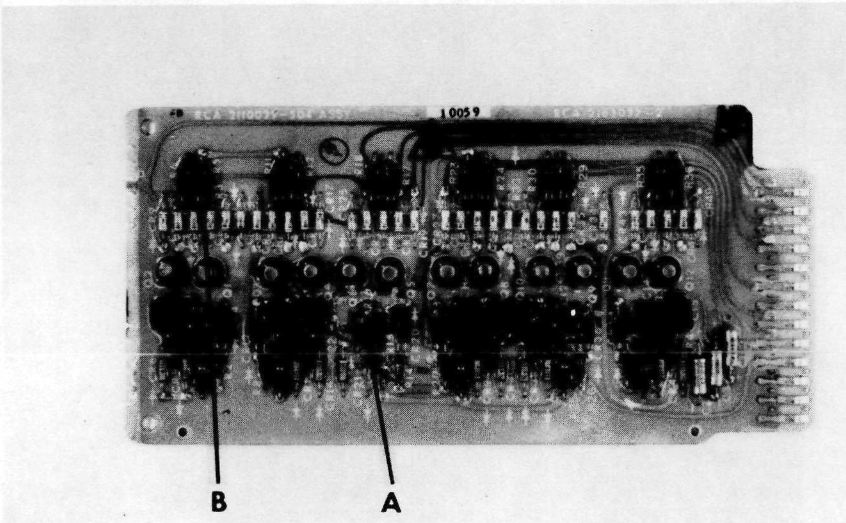


Figure 1. Component side of the initial problem board. (Arrow A indicates the "clustering" of components and area of failure; arrow B indicates the area with less component density.)

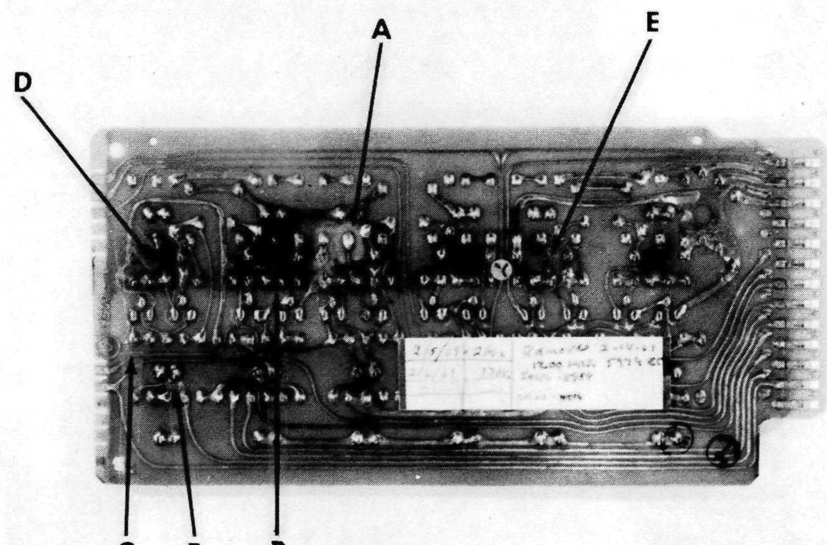


Figure 2. Circuit side of the initial problem board. (Arrows A through F pinpoint areas evaluated, with A and F corresponding to arrows A and B of Figure 1, respectively.)

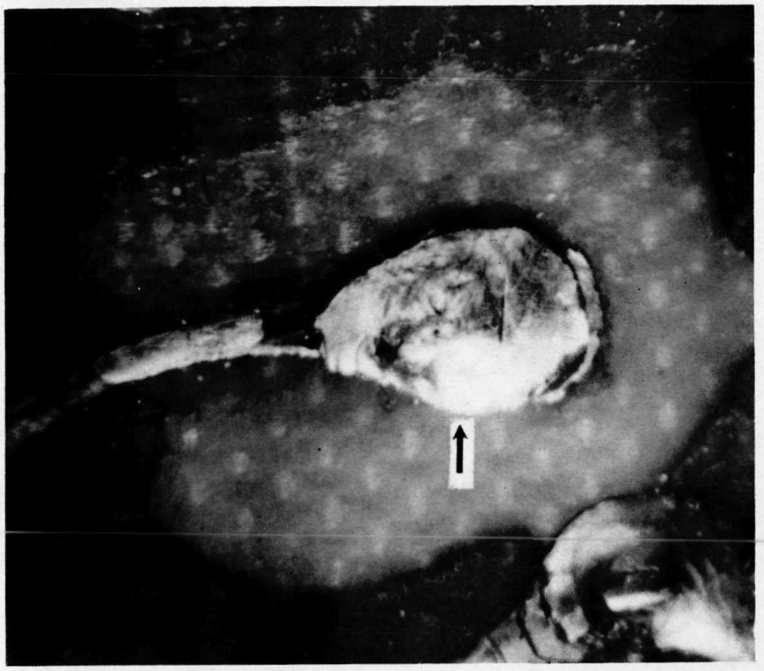


Figure 3. Connection that caused computer failure. (Reference arrow A, Figure 2.) (7X magnification)

Figure 4. Discrepant connection showing removed soldered lead (A) from its associated pad (B). (7X magnification)

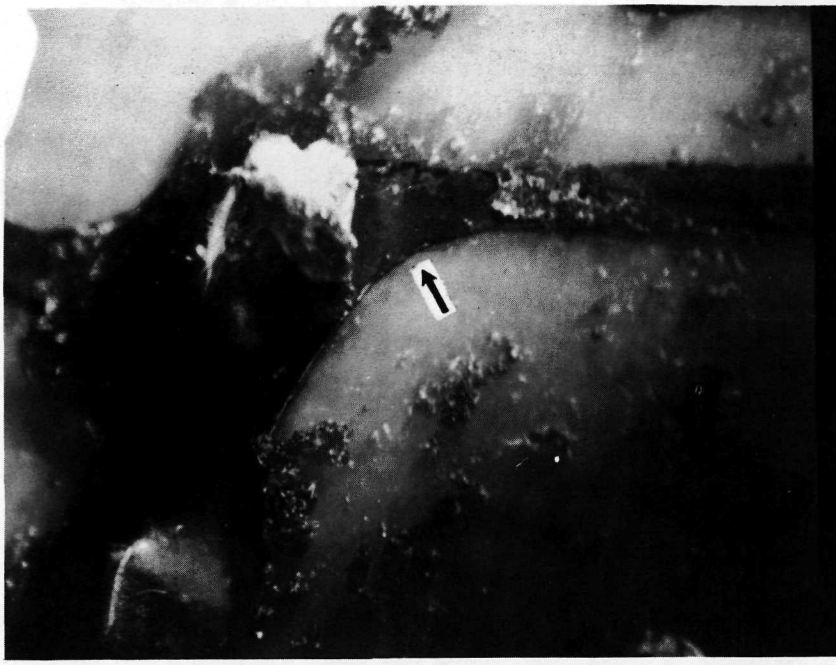


Figure 5. Solder coat lifted during urethane removal operation.
(10X magnification)

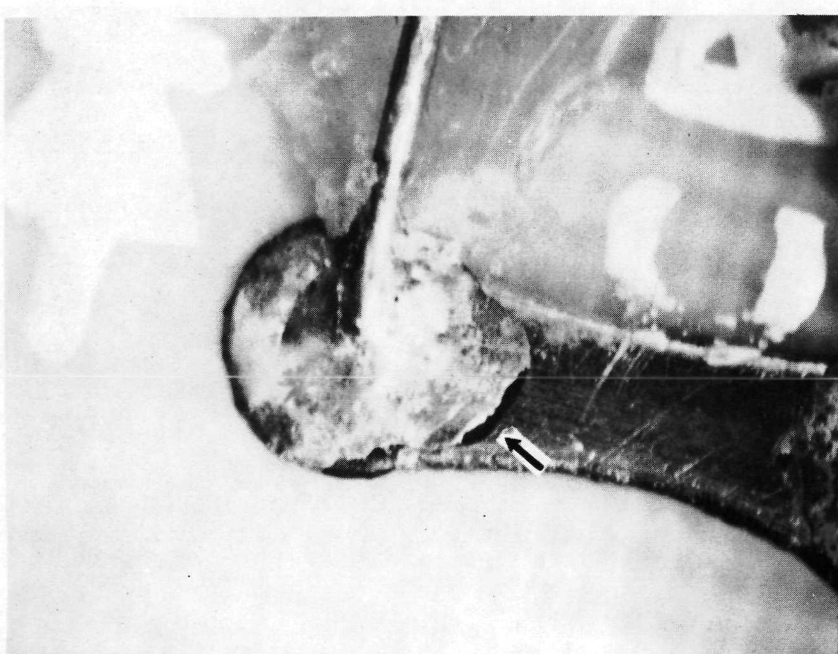


Figure 6. Darkened gold plating adjacent to a soldered connection.
(10X magnification)

Figure 7. Gross solder separation from solder pad and from hole plating. (Photo was taken immediately after the pull test.) (15X magnification.)

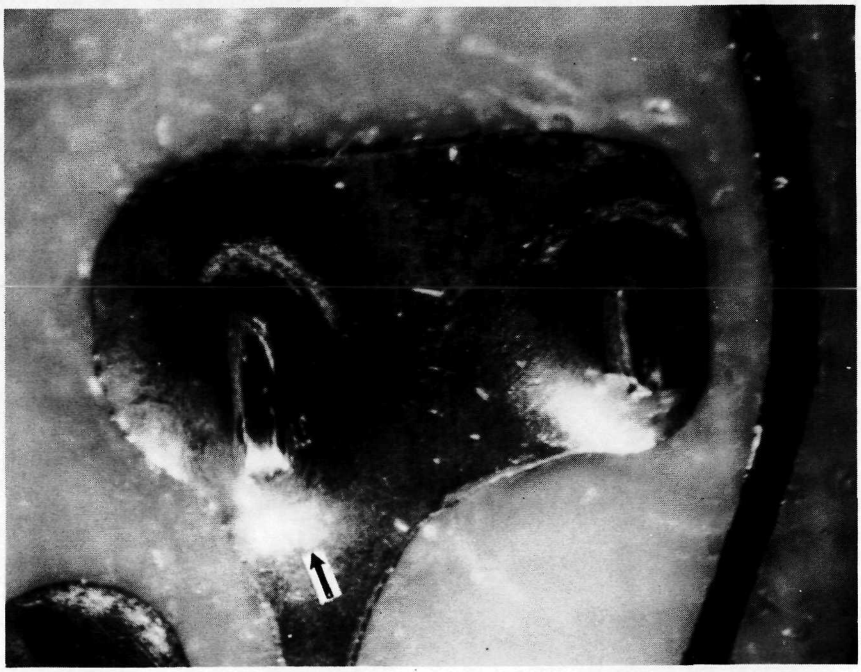


Figure 8. An acceptable connection by visual criteria. (10X magnification)

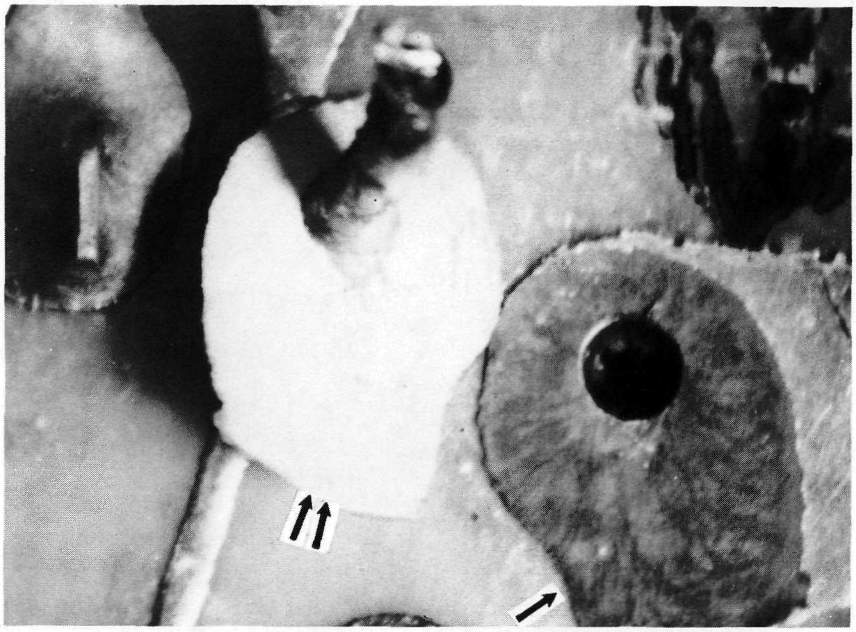


Figure 9. Connection, shown in Figure 8, after push test. (10X magnification)

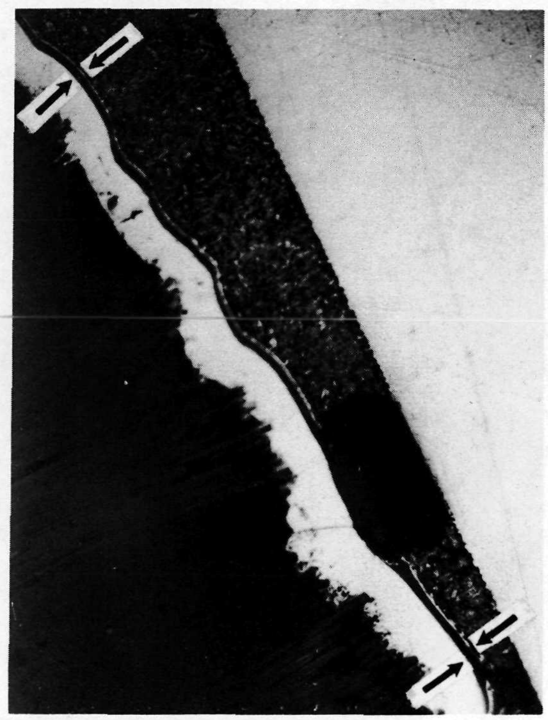


Figure 10. Complete solder separation from the hole plating of a gold-over-plated copper (with brightener additives) plated-through-hole. (185X magnification)

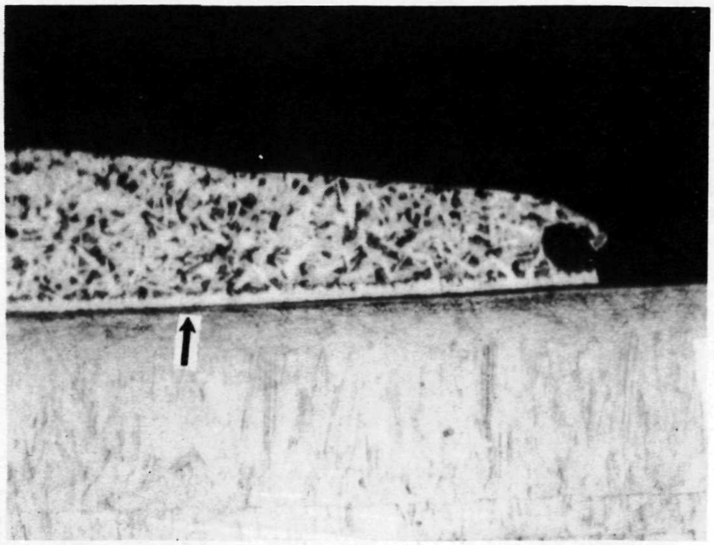


Figure 11. Solder separation from both the gold and the copper on the component side of connection. (Reference Figure 6. Arrow pinpoints gold plating termination.) (240X magnification)

Figure 12. Overall view of a visually acceptable connection in darkened area of a single sided connection. (10X magnification)

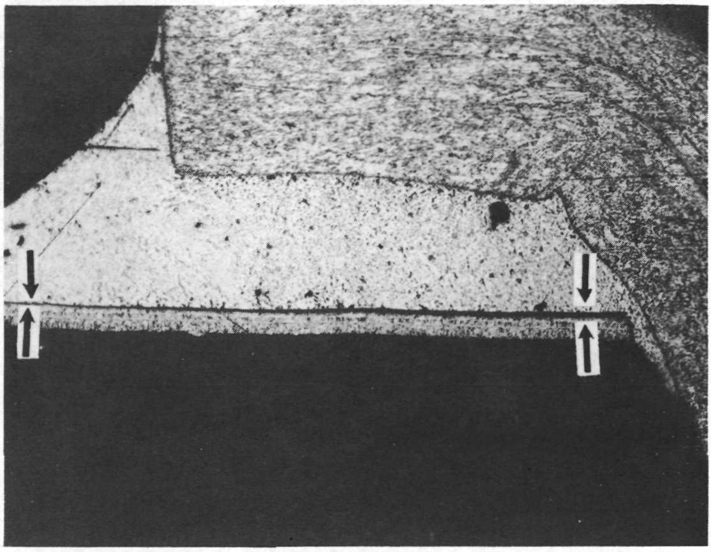


Figure 13. Cross section of connection shown in Figure 12. (The solder separation is shown between the arrows.) (50X magnification)

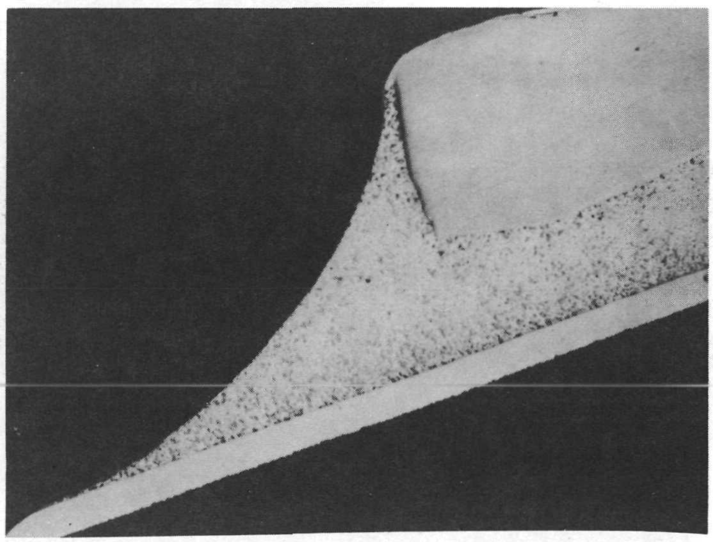


Figure 14. Connection showing acceptable solder bond. [This was taken from an area that showed no discoloration by heat. Gold-over-plated copper (with brightener additives).] (55X magnification)

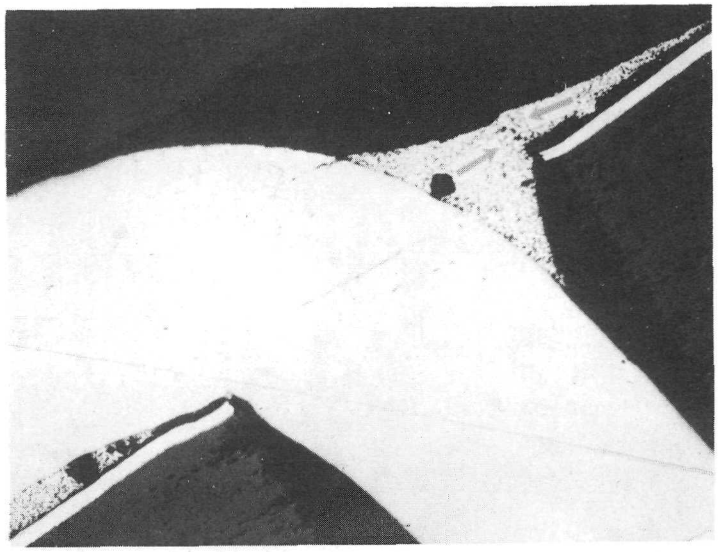


Figure 15. Cracked solder at heel of the clinched lead. (This indicates that the bond of solder to the pad was greater than the strength of the solder. This solder separated from the pad after the crack relieved the strain.) (35X magnification)

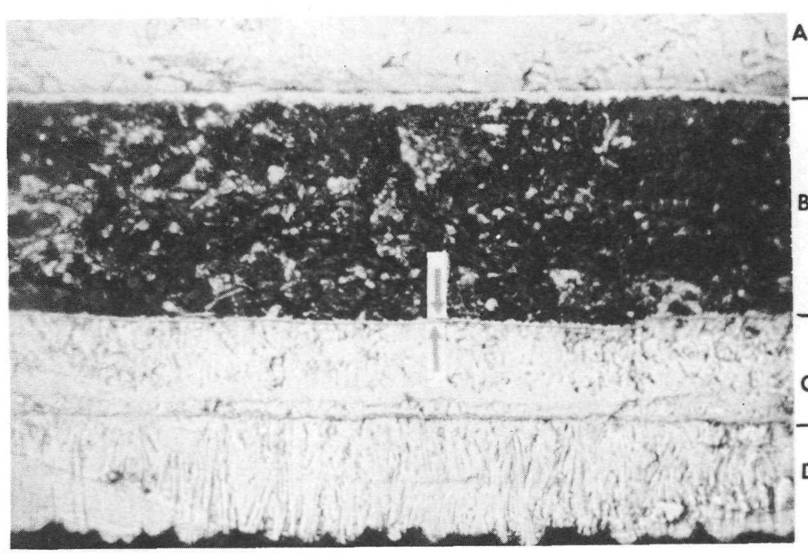


Figure 16. Photomicrograph of a soldered connection on circuit side from discolored area of "new generation" board — gold-over-plated pyrophosphate copper without brightener additives. (The lead is identified by A, the solder by B, plated copper by C, and laminate copper by D. Arrows pinpoint the copper-tin intermetallic bond to the solder pad.) (500X magnification)

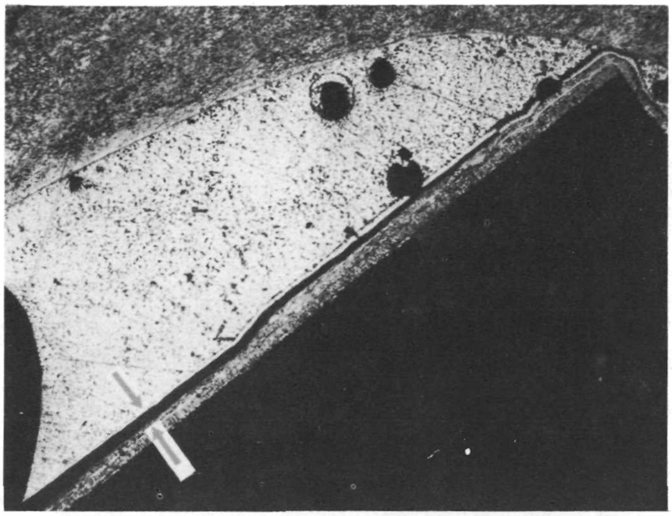


Figure 17. Component-side connection exhibiting separation under component lead at the solder-copper pad interface shown by arrows. (35X magnification)

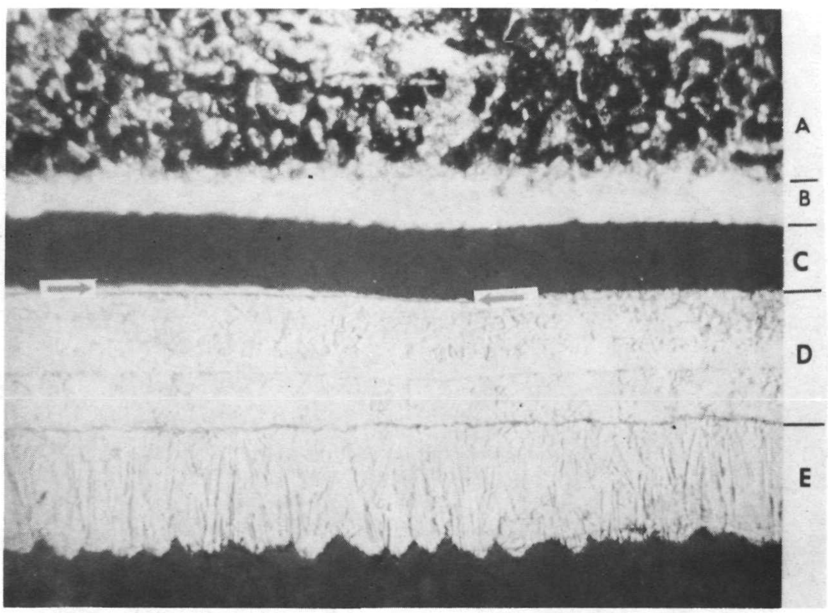


Figure 18. 500X magnification of connection shown in Figure 17. (Solder is identified by A, tin-gold intermetallic compound by B, separation by C, two plated thicknesses of copper by D, and laminate copper by E. Gold on the copper surface is indicated between arrows.)

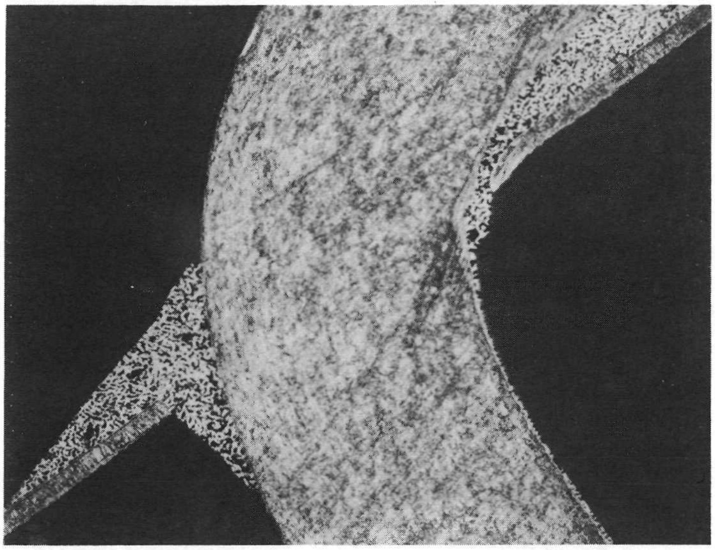


Figure 19. Cross section of a connection from a discolored area of a non-gold-plated board. (A good solder to copper bond is indicated.) (35X magnification)

Figure 20. Raised solder showing darkened gold plating. (20X magnification)

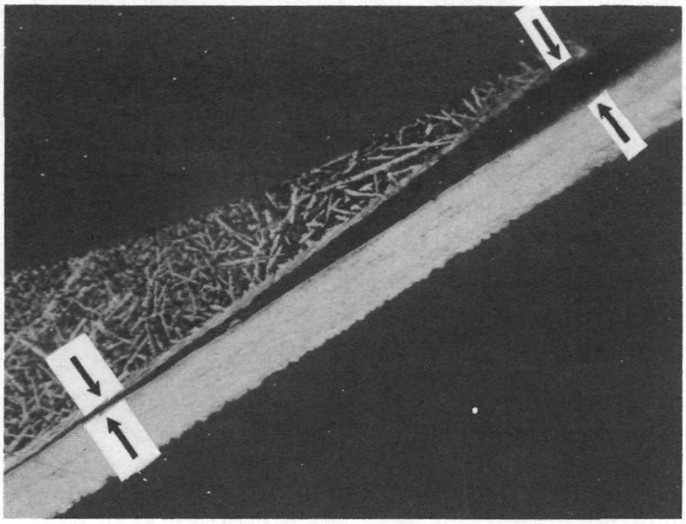


Figure 21. Cross section of connection shown in Figure 20, revealing the solder-circuitry separation. (130X magnification)

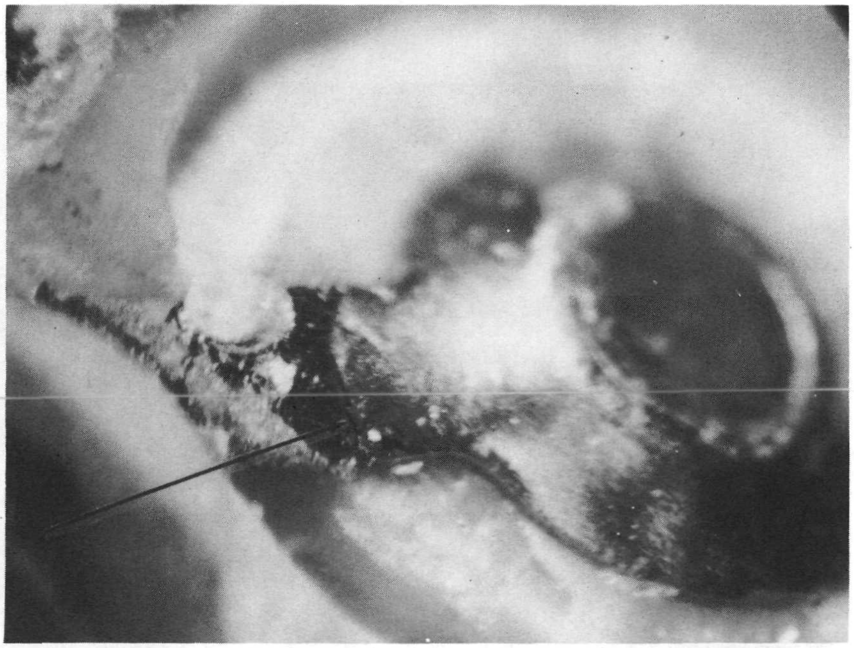


Figure 22. Solder fillet termination on a gold-plated circuit exhibiting a dark band. (25X magnification)

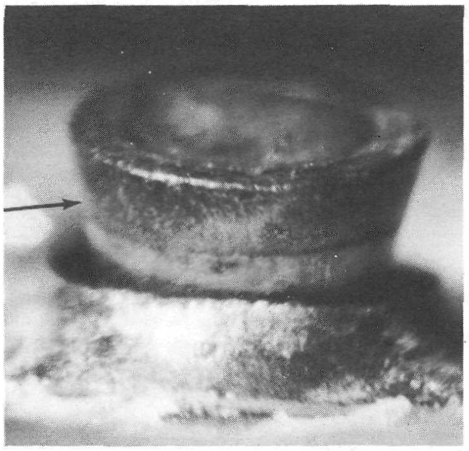


Figure 23. Push tested gold-plated terminal exhibiting solder separation. (25X magnification)

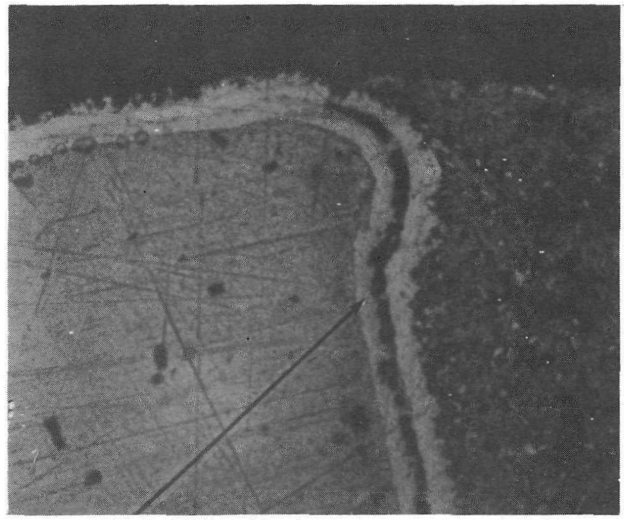


Figure 24. Gold-plated terminal that exhibited no visible surface defects. (Metallographic examinations show gross separation between the gold-plated terminal and the gold-tin intermetallic.) (410X magnification)

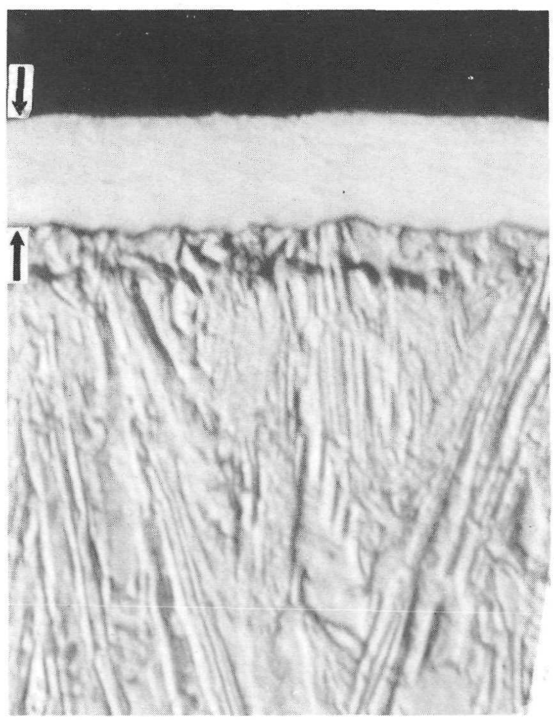
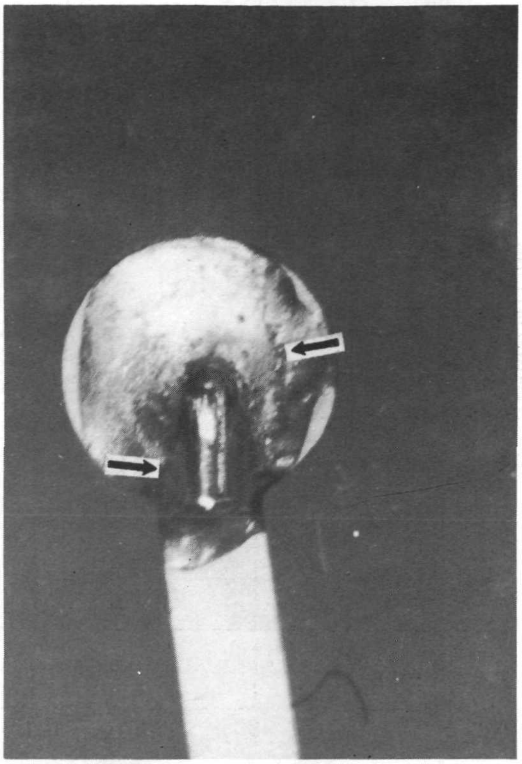
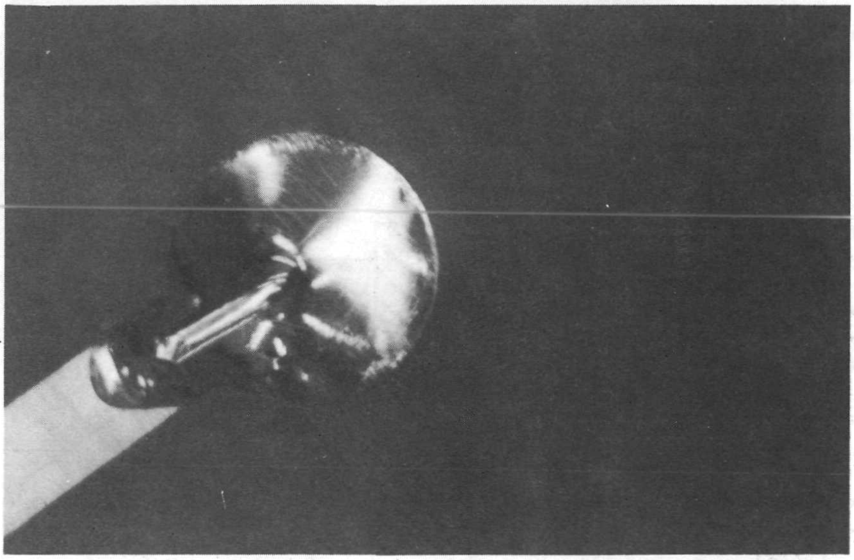


Figure 25. Cross section of gold-plated board before thermal testing. (Gold plating thickness approximately 0.00064 cm.) (2000X magnification)

Group A — bare copper

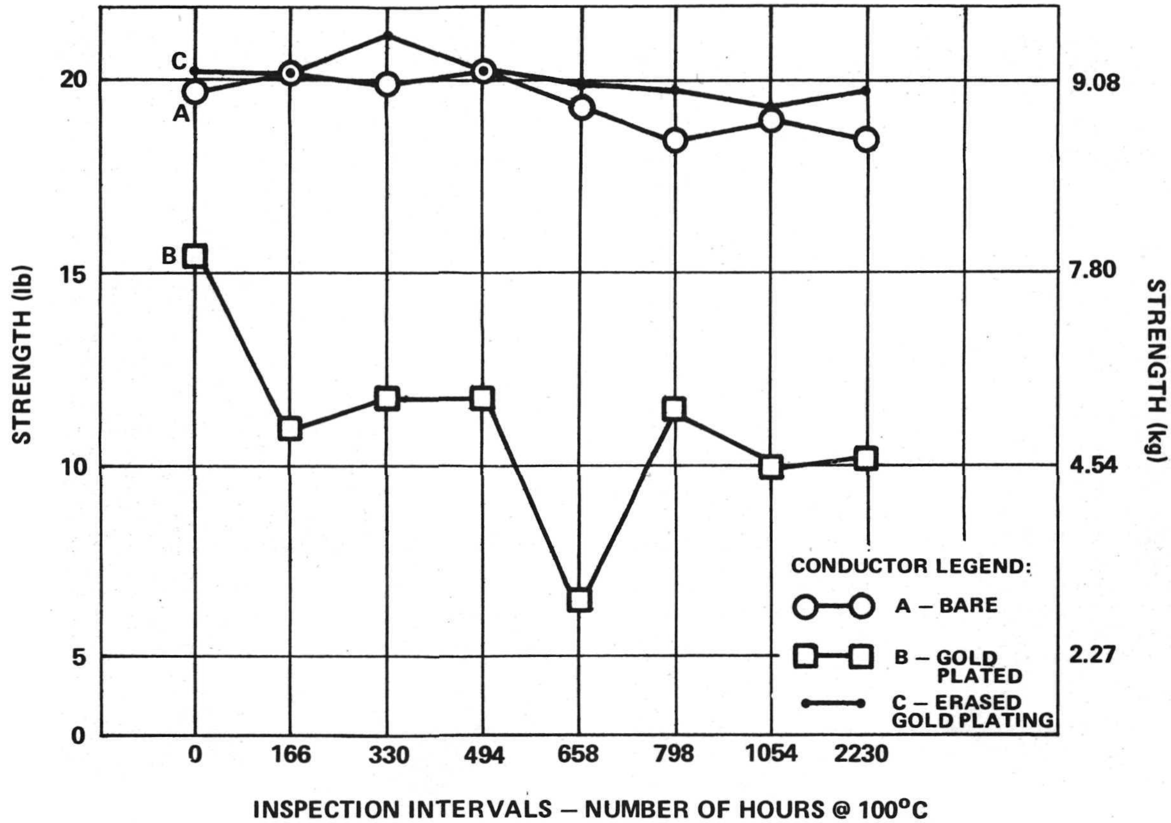


Group B — gold-plated



Group C — erased gold plating

Figure 26. Overall view of soldered connection of each test board group. (10X magnification)



Note: Push tests results for the A and C groups do not reflect the maximum strengths of the solder-circuitry bond because in many instances the leads bent or the pads lifted.

Figure 27. Average strength push test results.

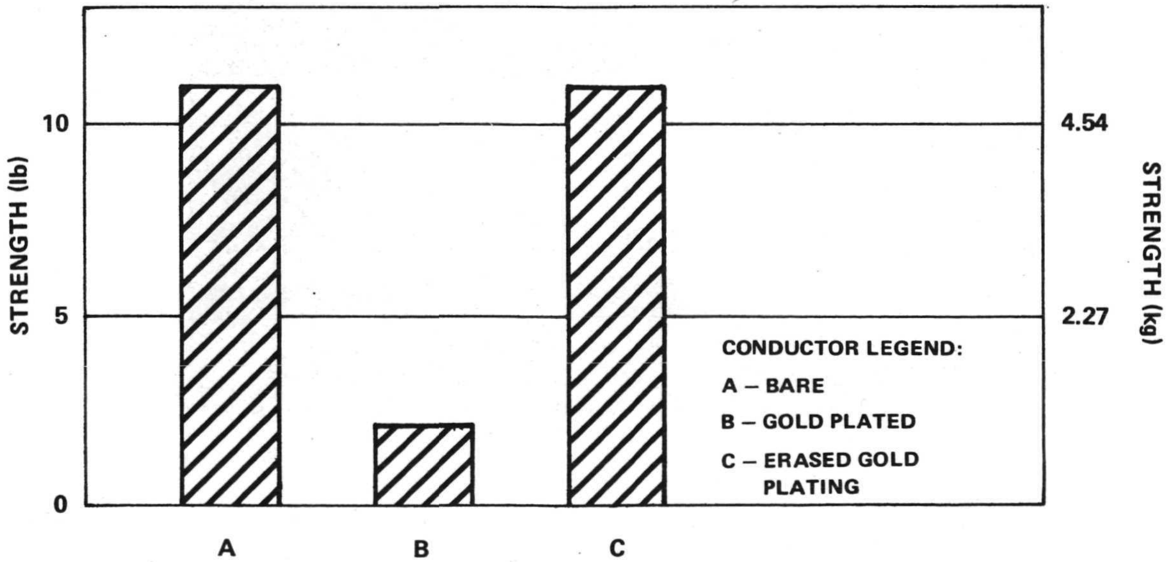


Figure 28. Minimum push strengths.

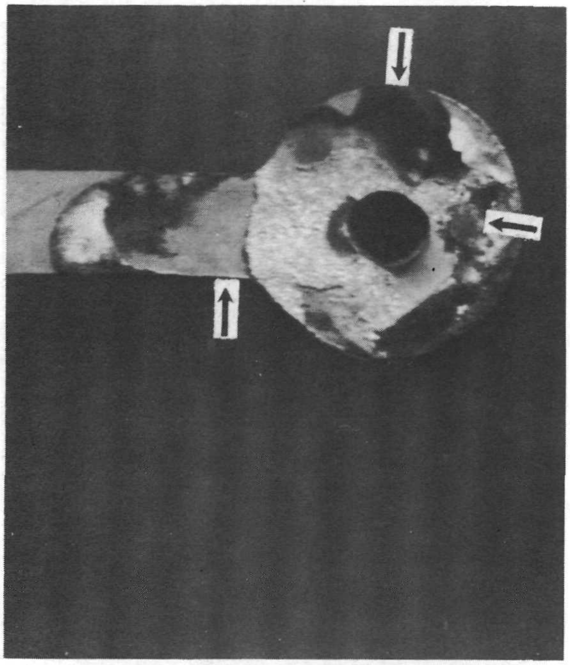


Figure 29. Partial solder separation, indicated by arrows, after 166 hours exposure to 100° C temperature. (10X magnification)

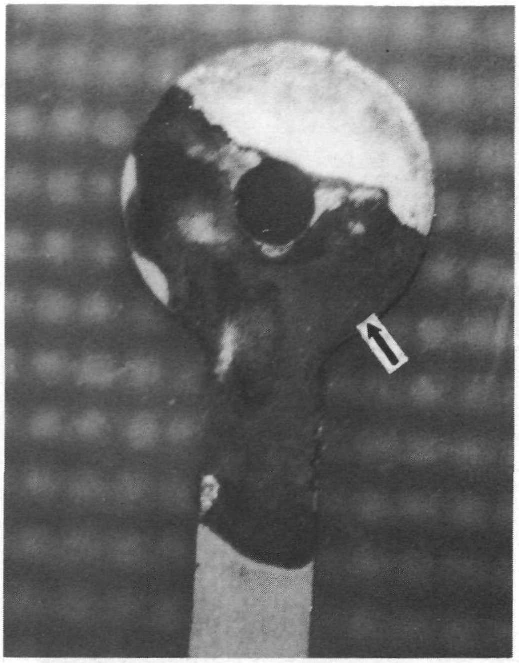


Figure 30. Solder separation from gold-plated laminate copper after 658 hours in test. (Bare copper is pinpointed by arrow.) (10X magnification)

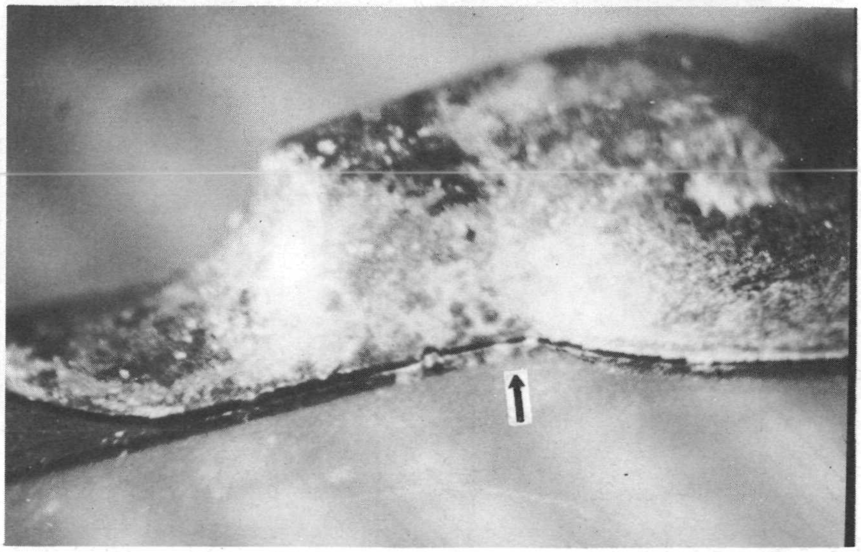
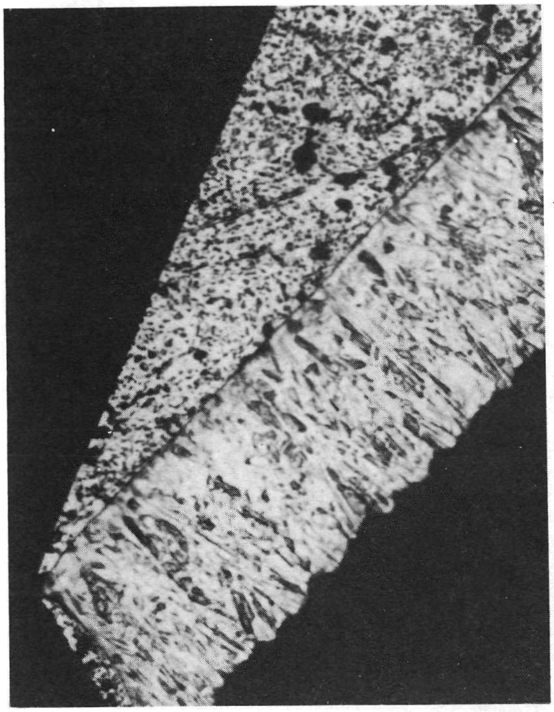
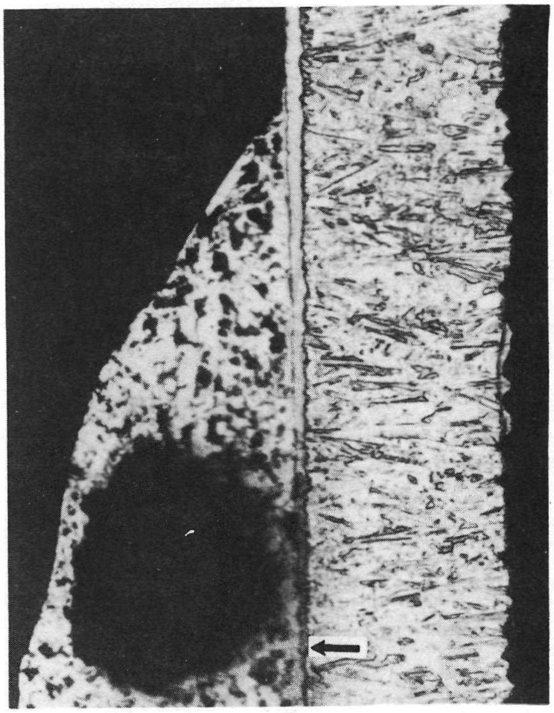


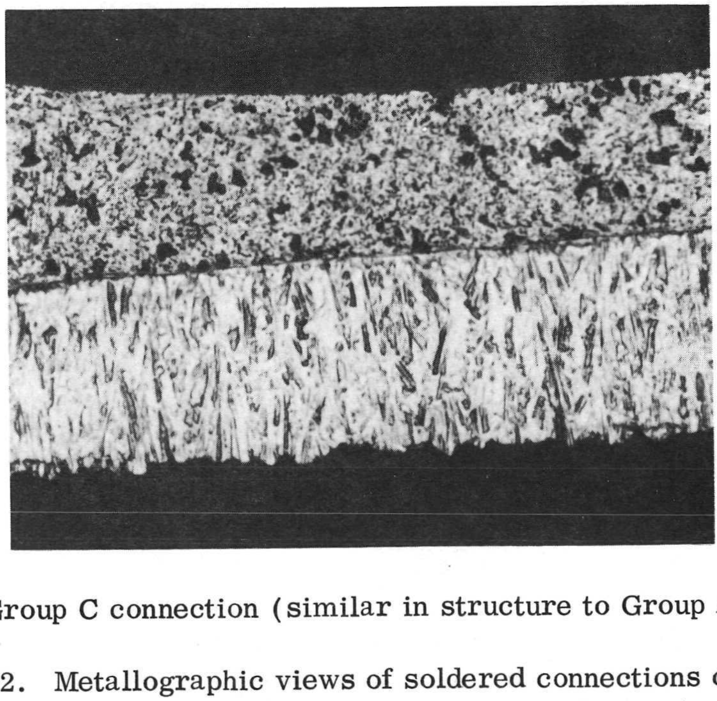
Figure 31. Solder separation from gold-plated copper after 658 hours exposure to 100° C temperature. (Solder is still bonded to the unplated side of the pad.) (25X magnification)



Group A connection



Group B connection
(Arrow indicates gold termination.)



Group C connection (similar in structure to Group A.)

Figure 32. Metallographic views of soldered connections of test board groups prior to tests. (400X magnification)

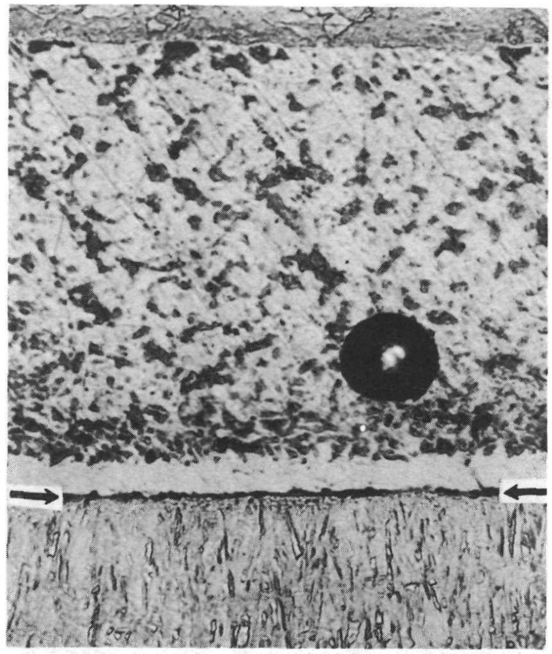


Figure 33. Initial indication of solder separation observed after 166 hours in temperature test. (400X magnification)

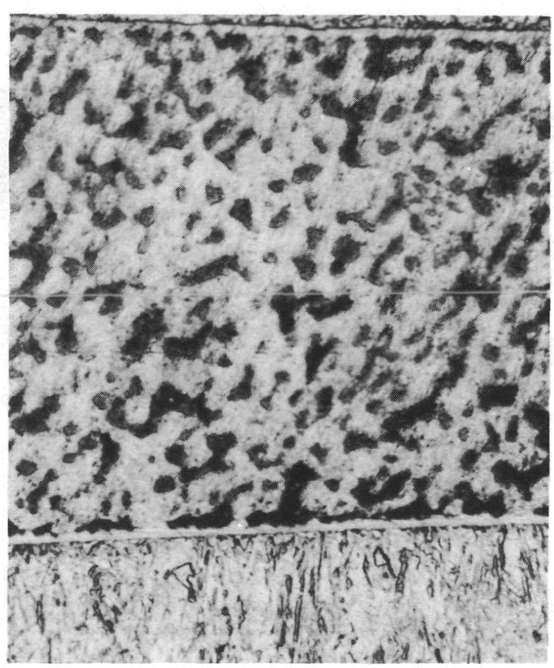


Figure 34. Group A connection upon test completion. (400X magnification)

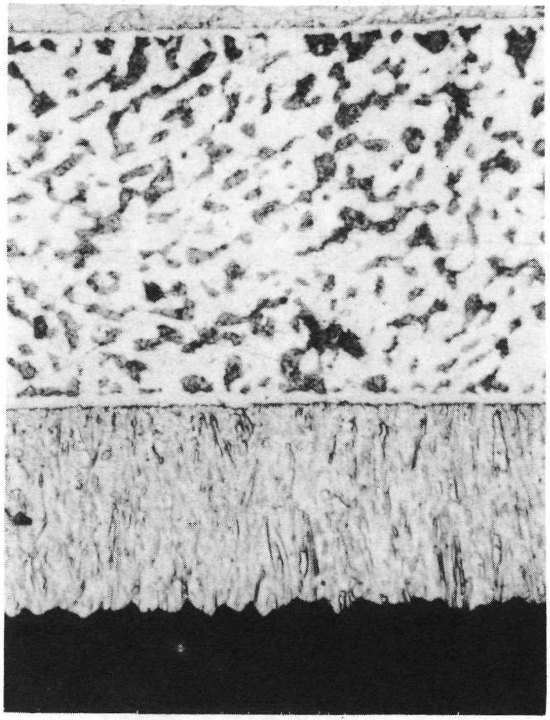


Figure 35. Group C connection upon test completion. (400X magnification)

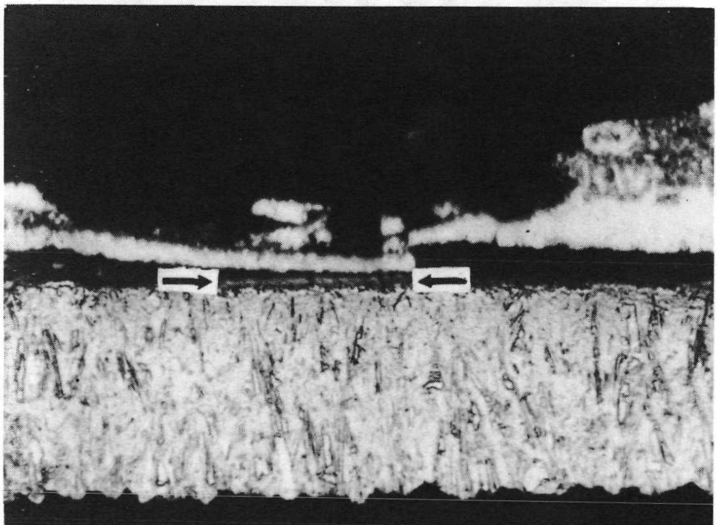


Figure 36. Group C solder away from erased gold area.
(400X magnification)

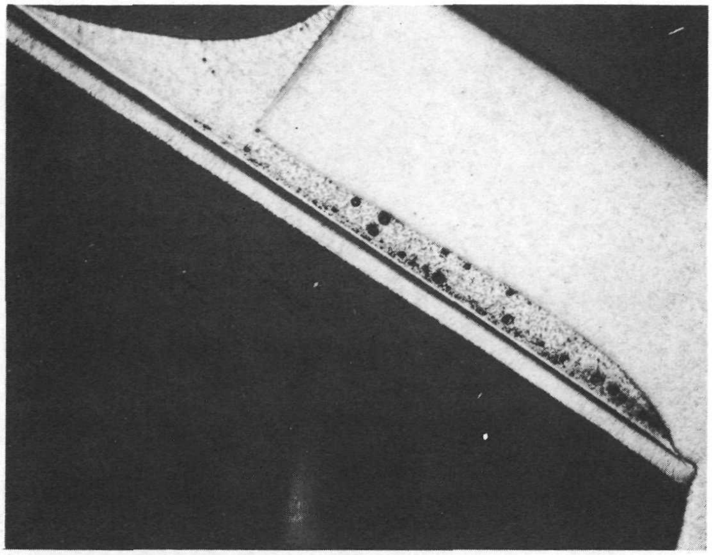


Figure 37. Connection soldered to gold — Group B — upon test completion. (Note outgaseous voids.) (35X magnification)

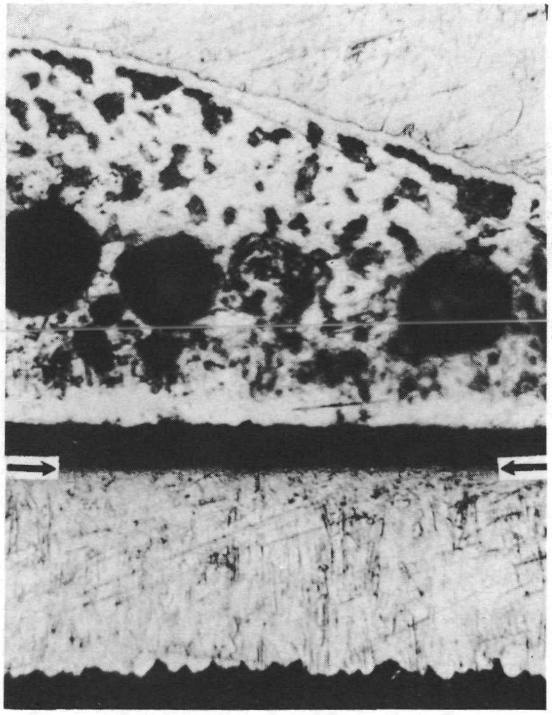


Figure 38. 400X magnification, showing bare copper, of connection shown in Figure 37.

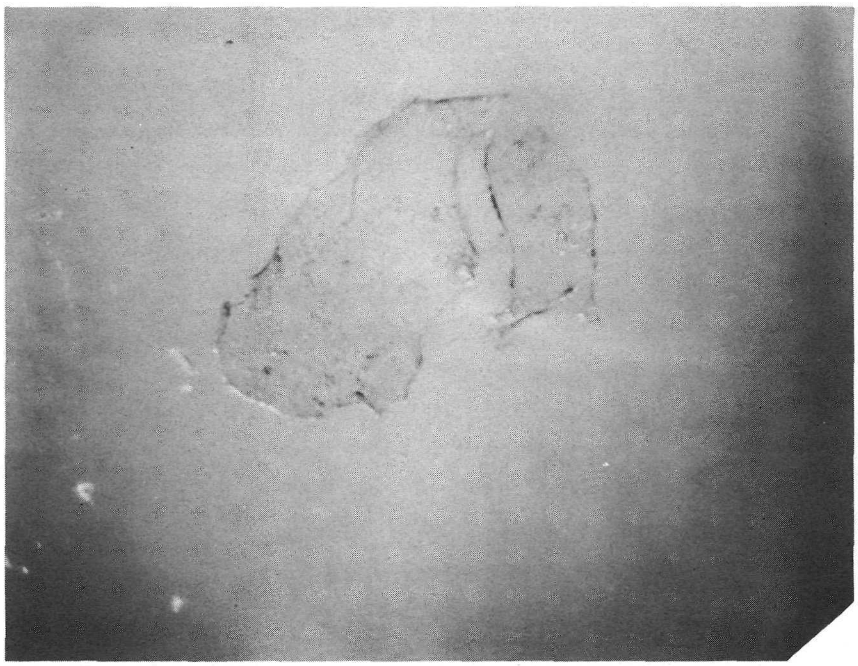


Figure 39. Transparent polymer isolated from a solder separated gold plating. (40X magnification)

APPENDIX

SOLDERING PROCEDURES AND VISUAL INSPECTION

The following procedures were used in the preparation, soldering, and inspection of the test assemblies. Once the boards were accepted, no further cleaning was performed throughout the program.

Leads

The lead materials were coated with a mildly activated rosin flux and pretinned in an ultrasonic soldering pot containing solder composed of 63 percent tin, 37 percent lead. The tinning temperature was approximately 249 to 260° C.

Printed Circuit Boards

All soldering was performed using a 25-watt hand soldering iron with a 0.16 cm diameter soldering tip. The flux was of the NASA approved, mildly activated type. The solder consisted of cored, mildly activated rosin flux, 60 percent tin, 40 percent lead. Ethyl alcohol was used throughout the program for cleaning and flux removal purposes. Tissues used were lint-free industrial type. Detailed procedures are given in the following paragraphs.

BARE COPPER BOARDS

1. Clean the copper by submersing board in Alpha 918 Copper Bright cleaner (Alpha Metals Company) for approximately 30 seconds and scrubbing it with a bristle brush.

2. Wash board with water.

3. Rinse board with alcohol; air dry.

4. Apply a thin coating of flux to soldering areas.

5. Coat pads with solder.

6. Remove flux and clean board with flux; air dry.

7. Install lead materials.

8. Reclean board with alcohol and bristle brush; air dry.

9. Apply a thin coating of flux to soldering area.

10. Solder connections.

11. Clean soldered areas with alcohol and tissue; air dry.

12. Inspect soldered connections for workmanship under 7X magnification.

13. Rework rejected connection as necessary, reclean, and reinspect.

GOLD-PLATED BOARDS

1. Clean all the circuitry surfaces with alcohol and bristle brush; air dry.

2. Install lead materials.

3. Reclean with alcohol and bristle brush; air dry.

4. Apply a thin coating of flux to soldering areas.

5. Solder connections. Use special precautions during soldering.

6. Clean board with alcohol and tissue; air dry.

7. Inspect soldered connections for workmanship under 7X magnification.

CAUTION

Do not rework solder-over-gold connections. The effects of the enriched gold in the solder are needed for evaluation.

ERASED GOLD BOARDS

1. Clean board with alcohol and bristle brush. Wipe with tissue and air dry.

2. Mechanically erase the gold plating from pad areas to be soldered.

3. Reclean board with alcohol and tissue; air dry.

4. Apply a thin coating of flux.

5. Coat pad areas with solder.

6. Clean with alcohol and tissue.

7. Install lead materials.

8. Clean with alcohol and bristle brush.

9. Apply flux to connections.

10. Solder connections.

11. Clean board with alcohol and tissue.

12. Inspect connections under 7X magnification.

13. Rework, reclean, and reinspect rejected connections.

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