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LINEAR MODULATOR

FINAL REPORT

CONTRACT NAS8-25987

MARCH 1971

Prepared for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Huntsville, Alabama 35812

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Approved by

C. W. Pederson
Program Manager

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FOREWORD

This report is presented in response to Paragraph II.2 of Exhibit A of Contract NAS8-25987. Supporting data is also contained in the Test Procedure and Report, MCR-71-82, March 1971.

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I. INTRODUCTION

The Denver Division of Martin Marietta Corporation designed, built, tested and delivered a single channel breadboard modulator, demodulator, and phase locked loops to NASA-MSFC. The breadboard is capable of modulating and demodulating quadrature double sideband suppressed carrier (QDSBSC) signals operating with channel frequencies from 4 kHz to 200 kHz and modulation frequencies from dc to 16 kHz.

The breadboard was tested and successfully passed the test requirements as outlined in Test Procedure and Report MCR-71-82.

This report discusses the breadboard design, theory of operation, alignment procedures, and recommendations for future development of FDM systems.

II. LINEAR MODULATOR AND PHASE LOCKED LOOPS DESCRIPTION

A. GENERAL

The linear modulator, demodulator, voltage controlled oscillator - phase lock loop (VCO-PLL) shown in the block diagram in Figure II-1 provides a single channel modulation and demodulation system capable of QDSBSC operation. The modulator and demodulator are capable of operating with signal frequencies from dc to 16 kHz and channel frequencies from 4 kHz to 200 kHz. The VCO-PLLs are phase-locked to a 128 kHz pilot frequency and provide the frequencies required in the double conversion demodulator. The phase locked loops are capable of following a $\pm$ 1% frequency change in the pilot frequency at a rate of dc to 500 Hz while maintaining a phase error of less than 0.18°. A crystal controlled channel frequency of 64 kHz at 0° and 90° provides the test signals for testing the modulator and demodulator operating in the QDSBSC mode.

B. MODULATOR

The modulator, Figure II-2, consists of two Intronics M502 true multipliers. The four input amplifiers A1 - A4 are required for input offset balance of the X and Y inputs of the M502 in order to provide input carrier and signal suppression. The resistor network into pin 2 of A2 including the sensistor R11 is to provide temperature compensation for good carrier suppression over the temperature range.

The two NH-0002 op-amps following the M502s provide impedance matching to the M502s in order to maintain constant output amplitude with frequency. The output impedance of the M502 increases to about 1 to 1.5 K ohms at 200 kHz which would cause a loss in amplitude without the high input impedance of the NH 0002.

Capacitors C9, C19, and C14 provide a small amount of phase lead to compensate for the phase lag in the circuit op-amps and multipliers. C14 and C19 along with R36 and R40 also provide a small amount of phase adjustment for phase matching of the two multipliers. Op-amp A7 is used as a summing amplifier for the two modulators.

C. DEMODULATOR

The demodulator, Figure II-3, is a double conversion type demodulator capable of demodulating QDSBSC channels from 4 kHz to 200 kHz. The desired channel of the composite signal (4 kHz to 200 kHz channels) is translated in the first balanced modulator (MOD 1) to a common frequency of 256 kHz. The translation frequency used depends on the channel to be demodulated and is 256 kHz + the channel frequency. For this breadboard the channel frequency is 64 kHz, therefore the translation frequency is 256 + 64 = 320 kHz. The translated composite signal is then fed through a low pass filter (LPFI) which removes the harmonic sidebands caused by the translation frequency.

The translated composite signal is then fed to two balanced modulators (MOD 2 and MOD 3) where the desired channel is translated down to base band by the 256 kHz translation frequency. Since the incoming composite signal is from a tape recorder, the signal can have as much as $\pm$ 1% frequency modulation on it due to the wow and flutter of the tape recorder. Also, the signal frequency from LPFI can have several degrees of phase modulation due to the phase slope of the filter. To compensate for this phase modulation of the signal, the second translation frequency (256 kHz) is fed through an identical low pass filter (LPF2) before being fed to the second balanced modulator (MOD2). This provides the same phase response for the signal frequency and the translation frequency. This is necessary for good suppression in the quadrature channel.

The 256 kHz translation frequency is also fed through a 90^{o} phase shifter before being fed to Mod 3 which provides detection of the quadrature channel. The 90^{o} phase shifter is automatic phase controlled by phase detecting the input and output signals of the phase shifter and using this phase error voltage to control the capacitance of the two varactor diodes which in turn controls the phase shift of the phase

shifter and maintains it at 90°. This is necessary in order to provide good quadrature suppression of the 0° channel in the 90° channel even though the frequency changes ± 1% due to the tape recorder.

Following the balanced modulators, MOD 2, and MOD 3, are two 16 kHz low pass filters which remove the translated signals of all of the adjacent and other channels.

D. VOLTAGE CONTROLLED OSCILLATORS AND PHASE LOCKED LOOPS

The translation frequencies for the double conversion demodulator are derived from two voltage controlled oscillators (VCO) used in phase locked loops (PLL) to provide phase coherent signals. The oscillators are at a frequency of 7680 kHz which provides a convenient frequency that can be simultaneously divided down to the pilot frequency of 128 kHz and translation frequencies of 256 kHz or 320 kHz. Figure II-4 shows the schematic diagram of the 320 kHz PLL. The oscillator output is shaped by transistors Q2 to Q4 to provide a clock pulse for the two divider chains. The divider chain consisting of A3 and A4 is a synchronous divider which provides a 128 kHz output frequency for use in the phase detector to phase lock the loop to the 128 kHz pilot frequency. The output of the phase detector is fed to amplifiers A10 and A11 which provide the very high loop gain required to maintain the phase error of 0.18° or less required for good quadrature suppression in the demodulator. The output of amplifier A10 is fed to voltage variable diodes CR3 and CR4 for frequency control of the VCO.

The oscillator clock pulse is also fed to a synchronous divider consisting of A1 and A2 to provide the 320 kHz translation frequency. Since the 320 kHz translation frequency is derived from a separate divider chain than the divider which provides the 128 kHz for phase locking the PLL, it is necessary to use synchronous dividers to maintain good phase correlation between the two divider chains. It is also necessary to synchronize the 320 kHz divider to the 128 kHz divider chain. The

sync signals are provided by logic gates A8 and A9 which get their inputs from the clock pulse and all of the dividers in the 128 kHz chain.

Figure II-5 shows the VCO-PLL for the 256 kHz translation frequency. It is identical to the 128 kHz portion of the 320 kHz loop. Since the 256 kHz for frequency translation and the 128 kHz for phase control can be derived from the same divider chain, a separate divider is not required. This divider chain is also synchronized from the sync pulses derived in the 320 kHz PLL.

The 500 Hz calibration amplifier shown in Figure II-4 is not a part of the PLL but is used only for measuring the phase error and jitter between the incoming pilot frequency and the PLL when the pilot frequency has frequency modulation due to the tape recorder's wow and flutter.

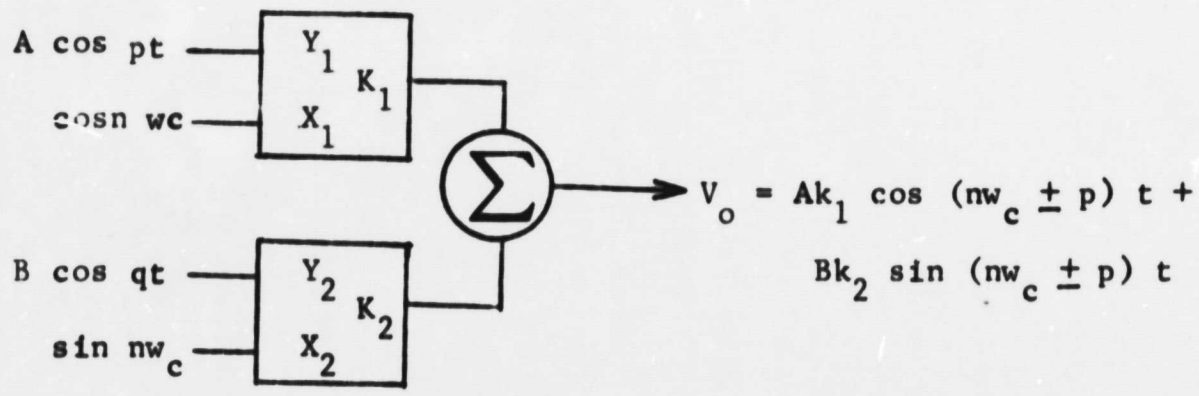
E. TEST OSCILLATOR

Figure II-6 shows the schematic diagram of the test oscillator used to provide frequencies of 64 kHz at 0^{o} and 64 kHz at 90^{o} for use as channel carrier inputs to the modulator. The test oscillator also provides the 128 kHz pilot frequency for phase locking the two PLLs. The crystal oscillator is digitally divided down to 128 kHz and 64 kHz. The 64 kHz is filtered to provide a clean sin wave for use in the true multipliers. The filter is followed by an adjustable phase shifter to provide adjustment for phase coherence between the demodulator input signal and the 320 kHz translation signal. This is followed by a 90^{o} phase shifter to provide the quadrature carrier input to the modulator.

III. THEORY OF OPERATION

A. MODULATOR

The modulator consists of two Intronics M502 true multipliers. The multiplier outputs are summed to produce QDSBSC output as shown in Figure III-1.



K_1, K_2 = channel gain factors

nw_c = channel carrier frequency

p,q = modulation frequencies

A, B = modulation amplitudes

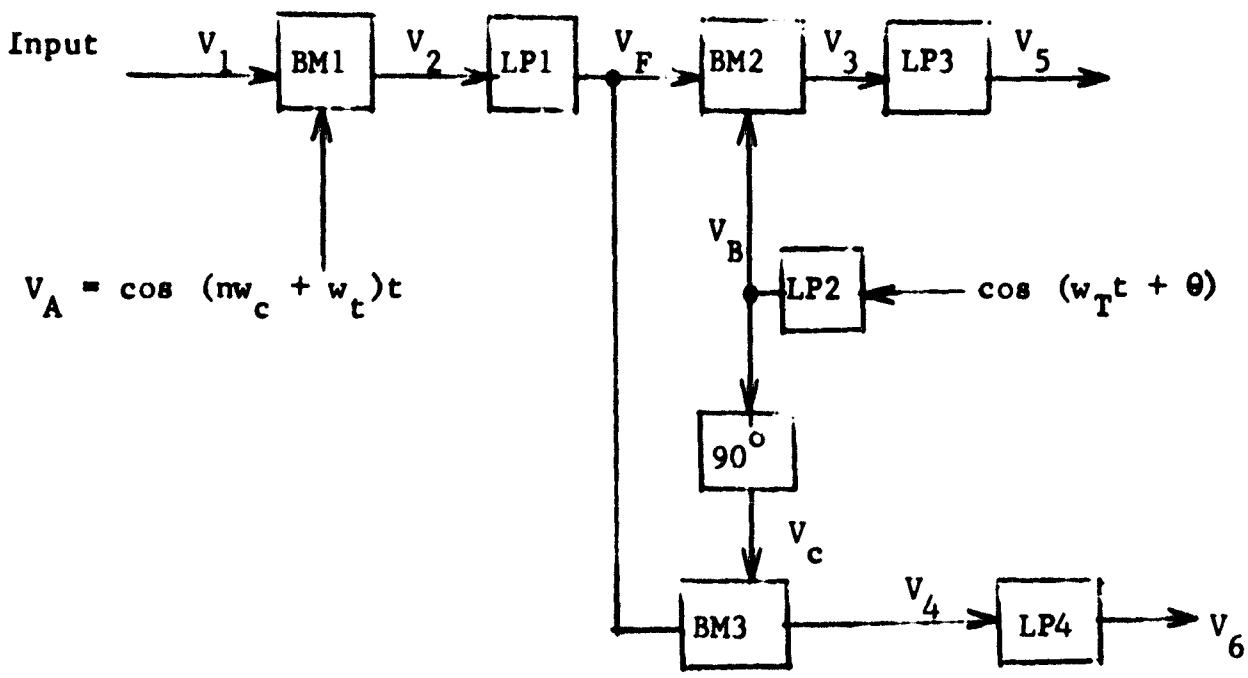
Figure III-1
Modulator Block Diagram

It should be noted that in addition to the two quadrature components on the output, the second harmonic of both the modulating and the carrier frequencies will be present at the output. This is inherent in trans-conductance type multipliers. These components, however, will be more than 50 db below the desired side bands for the M502 units. Feedthrough of the fundamental frequencies will also occur, however. Suppression

of these freqiencies can be cpntrolled with dc balance on the inputs to about 70 db below the desired sidebands.

B. DEMODULATOR

The demodulator uses balanced modulators in a double-frequency conversion scheme to demodulate QDSBSC signals from a composite waveform made up of channel frequencies from 4 to 200 kHz. The block diagram of the demodulator is shown in Figure III-2. BM1-3 and balanced modulators and LP1-4 are low pass filters.



nw_c = channel frequency; n = 1, 2, ... 50; $w_c = 2\pi$ 4 kHz

w_t = translation frequency; $w_t = 2\pi$ 256 kHz

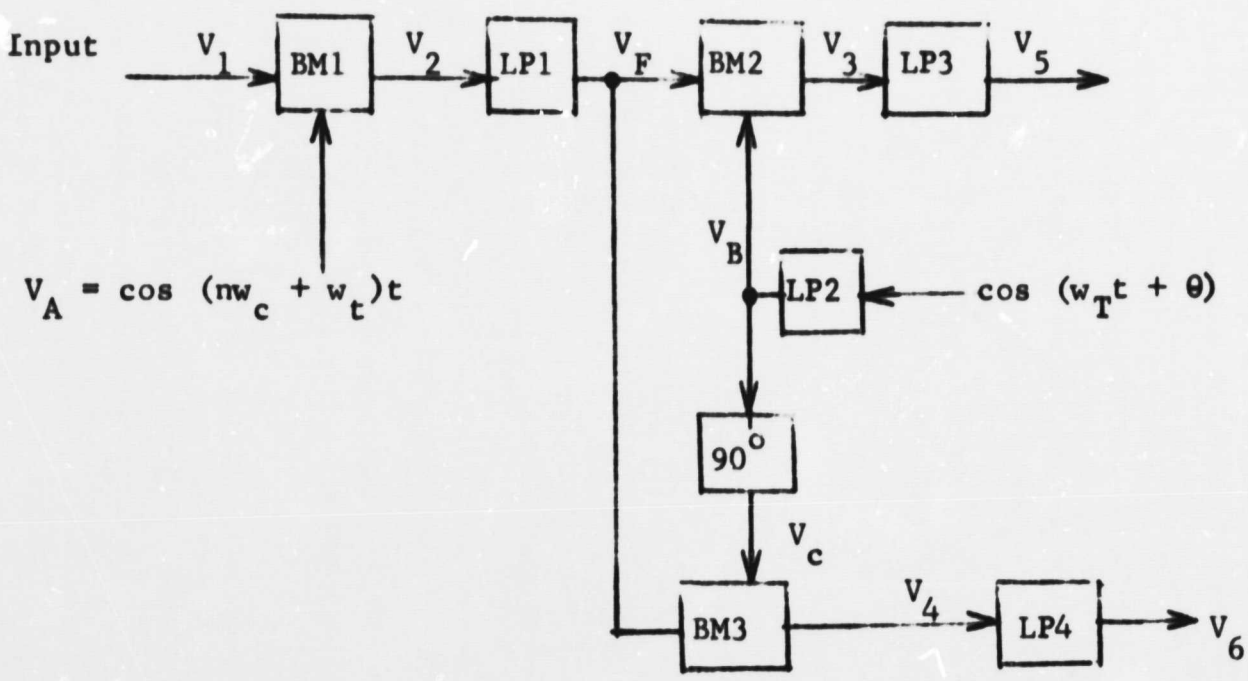
Figure III-2
Demodulator Block Diagram

The inherent disadvantage of the balanced modulator is that harmonics of the carrier frequency are generated. Consider a modulating input,

of these freqiencies can be cpntrolled with dc balance on the inputs to about 70 db below the desired sidebands.

B. DEMODULATOR

The demodulator uses balanced modulators in a double-frequency conversion scheme to demodulate QDSBSC signals from a composite waveform made up of channel frequencies from 4 to 200 kHz. The block diagram of the demodulator is shown in Figure III-2. BM1-3 and balanced modulators and LP1-4 are low pass filters.



nw_c = channel frequency; n = 1, 2, ... 50; $w_c = 2\pi$ 4 kHz

w_t = translation frequency; $w_t = 2\pi$ 256 kHz

Figure III-2
Demodulator Block Diagram

The inherent disadvantage of the balanced modulator is that harmonics of the carrier frequency are generated. Consider a modulating input,

A cos $\omega_m t$, and a carrier input, B cos $\omega_c t$, applied to a balanced modulator. Due to the switching action of the carrier signal within the balanced modulator, the output signal V_{BM} contains all the harmonics of the carrier's fundamental frequency according to the Fourier series,

$$V_{BM} = 2KAB \cos\omega_m t \sum_{n=1}^{8} An \cos n\omega_c t.$$

where

$$An = \left[\frac{\sin \frac{n\pi}{2}}{\frac{n\pi}{2}}\right]$$

and K is the gain of the balanced modulator.

As can be seen from the above equation the amplitude of the harmonic decreases as the order of the harmonic increases. Using a fundamental trigonometric identity, it can be shown that the output of the balanced modulator is:

$$V_{BM} = \frac{AB}{2} \cos\left(\omega_c \pm \omega_m\right)t + \frac{AB}{6} \cos\left(3\omega_c \pm \omega_m\right)$$
$$+ \frac{AB}{10} \cos\left(5\omega_c \pm \omega_m\right) + \ldots$$

Therefore, due to the switching action of the balanced modulator, sidebands of the odd harmonics of the fundamental carrier frequency are generated in addition to sidebands of the carrier and modulating fundamental frequencies.

The first balanced modulator, BM1 translates the incoming signal to a carrier frequency (256 kHz) high enough so that the harmonics of the carrier frequency are too high to demodulate any of the channels

from 4 to 200 kHz. The output of BM1 is then frequency translated a second time to bring the desired channel down to base band. Adjacent channels are attenuated by the output low pass filters. BM2 demodulates the 0^{o} component of the desired channel and BM3, the 90^{o} component. LP1 is required to filter the output from BM1 to prevent the harmonic sidebands of its carrier from combining with harmonics of the 256 kHz 0^{o} and 90^{o} carriers in the second balanced modulators to produce interference in the demodulated data. It is interesting to note that carrier suppression in the balanced modulators is not required.

Assume that part of V_A is present in the output of BM1 and part of V_B and V_C in the outputs of BM2 and BM3; after mixing with the carriers of BM1 and BM2 and neglecting harmonics we have:

$$V_3 = \cos\ (2\ w_T + nw_c)\ t + \cos\ w_T\ t$$

$$V_4 = \cos\ \left[(2\ w_T + nw_c)\ t - 90^{o}\right] + \cos\ (w_T t - 90^{o})$$

All these components will be rejected by the output low pass filters LP3 and LP4.

The output equation for the double-frequency translation scheme is derived below. The input (composite) signal representing the quadrature components of one channel is:

$$V_1 = \cos\ (nw_c \pm p)\ t + \sin\ (nw_c \pm q)\ t$$

where $p = 0^{o}$ modulation frequency,
and $q = 90^{o}$ modulation frequency.

Neglecting odd harmonic sidebands of V_A, since they will be filtered by LP1; and also neglecting the sum-frequency sidebands because they will

be $2nw_c$ above w_t and will be rejected by LP3/4, and disregarding gain factors, we get

$$V_2 = \cos\ (w_t \pm p)\ t\ +\ \sin\ (w_T \pm q)\ t$$

The output, V_F, from LP1, using notations from filter characteristics in Figure III-3, is:

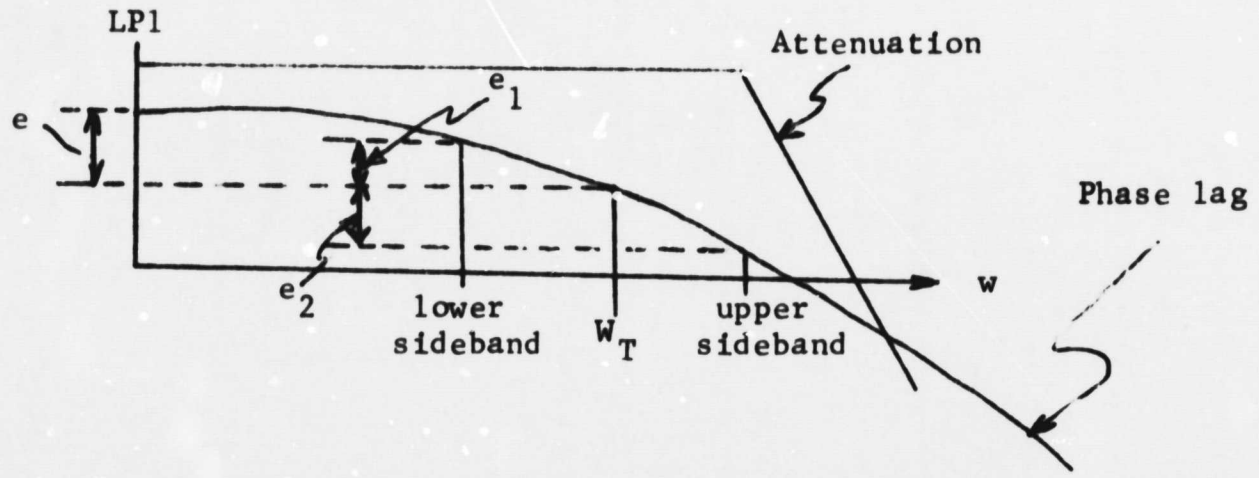


Figure III-3
Filter Characteristics

$$V_F = \cos\ \left[(w_T + p)\ t + e + e_{2p}\right] + \cos\ \left[(w_T - p)\ t + e - e_{1q}\right]$$

$$+ \sin\ \left[(w_T + q)\ t + e + e_{2q}\right] + \sin\ \left[(w_T - q)\ t + e - e_{1q}\right]$$

Using the carrier for the second balanced modulator as $V_{B,C} = \cos\ (w_T t + \theta)$ and disregarding the phase shift of the audio frequency in LP2/3, we get the output signal:

Equation A.

$$V_{5,6} = \cos pt \cos (\emptyset - e_{2p}) + \sin pt \sin (\emptyset - e_{2p})$$
$$+ \cos pt \cos (\emptyset + e_{1p}) - \sin pt \sin (\emptyset + e_{1p})$$
$$- \sin qt \cos (\emptyset - e_{2q}) + \cos qt \sin (\emptyset - e_{2q})$$
$$+ \sin qt \cos (\emptyset + e_{1q}) + \cos qt \sin (\emptyset + e_{1q})$$

where $\emptyset = \theta - e$

For simplicity, assume linear phase slope in LP1, i.e.

$$e_{1p} = e_{2p} = e_p \text{ and } e_{1q} = e_{2q} = e_q$$

For $\emptyset = 0^\circ$, equation A reduces to $V = \cos (pt + e_p)$ and for $\emptyset = 90^\circ$ equation A reduces to $V = \cos (qt + e_q)$. These are the desired 0° and 90° components respectively. It can be seen from the above that the phase adjustment making $\emptyset$ equal to 0° or 90° can be made either in the first or the second balanced modulator carrier inputs. It should be noted that for a non-zero phase slope in LP1 a lag will be be introduced for the audio output frequencies. The lag is proportional to the steepness of the phase slope.

For $\emptyset = 0$ and $e_1 \neq e_2$ we have

$$V = \cos pt \cos e_{1p} - \sin pt \sin e_{1p} + \cos pt \cos e_{2p} - \sin t \sin e_{2p}$$
$$+ \sin qt \cos e_{1p} - \cos qt \sin e_{1p} - \sin qt \cos e_{2q} + \cos qt \sin e_{2q}$$

The sin pt and cos pt terms are the wanted 0° signal; however, there is an amplitude loss dependent upon the difference between e_1 and e_2. For

$e_1 - e_2 = \pm 0.18^o$ this amplitude loss amounts to less than 0.1%. The audio frequency lag mentioned above is also present.

The sin qt and cos qt terms represent quadrature feedthrough and the amount of feedthrough is dependent on the difference between e_1 and e_2. For $e_1 - e_2 = \pm 0.18^o$, the amount of feedthrough is 0.3% of the wanted signal (or 50 db down).

Similarly for $\theta = 90^o$, it can be found that the quadrature feedthrough into the 90^o channel is less than 0.3% for $e_1 - e_2 = \pm 0.18^o$.

For $e_q = e_p = 0$ it can similarly be found that 50 db quadrature feedthrough suppression requires error in total phase $\emptyset$ (from 0^o or 90^o) of less than 0.18^o.

The modulator input composite signal may have a $\pm$ 1% frequency flutter. This frequency flutter will cause a phase flutter in the signal on the output of LP1. To compensate for this phase flutter, LP2 is added in the carrier path for the second balanced demodulator. The phase slope of LP2 is matched to the phase slope of LP1. The synthesizer VCOs are locked to the pilot and will follow the frequency flutter so that the carrier frequencies used in the demodulator will have the same flutter. LP2 provides a phase change for the BM2 carrier that is matched to the phase change of the signal in LP1 during the frequency flutter so that the total demodulator phase, $\emptyset$, is independent of the $\pm$ 1% frequency flutter. Therefore, no feedthrough will occur as a result of the $\pm$ 1% frequency flutter in the 0^o channel. The 90^o phase shifter in the BM3 carrier path must be independent of frequency. This is accomplished by using a phase locked loop which automatically tracks the phase of the BM2 carrier, and provides an output signal for use as BM3 carrier, whose phase is shifted 90^o from that of the BM2 carrier. The feedthrough in the 90^o channel will therefore also be independent of the $\pm$ 1% frequency flutter. It is worth noting that the frequency flutter of the composite signal and the demodulator carriers will cause a proportional flutter in the audio output frequency.

C. PHASE LOCKED LOOPS

The two phase locked loops each consist of a phase detector (θ), loop amplifier/filter (A) voltage controlled oscillator (VCO) and a frequency divider (D) as shown in Figure III-4.

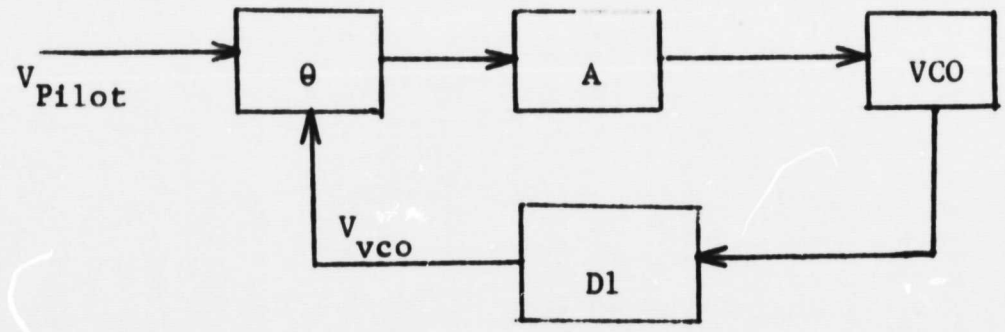


Figure III-4

Phase Locked Loop Block Diagram

A phase detector employing a balanced modulator produces an output voltage that is proportional to the phase difference between the reference input signal, pilot, and the digitally frequency divided VCO output. The phase error signal is passed through the loop amplifier/filter and provides the driving voltage for the VCO in such a direction as to minimize the phase error. The loop amplifier/filter provides high loop gain at low frequency to minimize static error and to provide good low frequency tracking response. It also provides attenuation at high frequency to attenuate the 256 kHz phase detector output for adequate 256 kHz output jitter suppression. The VCO gain is defined as the output frequency change divided by the control voltage required to produce that change. For the LC-VCOs used the gain constant referred to the 128 kHz output is:

$$K_o = 3.15\ (10)^8 \text{ degrees/sec/volt} = 161 \text{ db}$$

The phase detector operates on the following two input signals (neglecting fundamental feedthrough and odd harmonics):

1. $V_{pilot} = \cos \quad (w_{128} + w_p) \quad t$

where w_p = reference signal frequency modulation to be tracked by the phase locked loop

and 2. $V_{vco} = \cos \quad \left(w_{128} \quad t + \emptyset \right)$

where $\emptyset$ = VCO phase error.

The phase detector output signal is given by:

Equation B. $e_{out} = K_{PD} \quad \cos \left[\left(w_p t \; - \theta \; + \cos \; 2w_{128} t + w_p t + \theta \right) \right]$

where K_{PD} is the phase detector output voltage versus input phase difference constant. For the balanced modulator circuit used, this constant is:

$$K_{PD} = 0.055 \; {}^{\text{volts}}/_{\text{degree}} = -25 \text{ db}$$

With the present modulator design, the second term of equation B can be neglected as follows.

Assuming a phase detector steady state input phase error of 0.1°, the detector output will be 5.5 m V dc; and, at 500 Hz and 0.1° phase error, the output will be 5.5 m V peak at 500 Hz. The output of the phase detector will, in both cases, contain a 256 kHz square wave at 2.5 V RMS; thus, the 256 kHz component is 53 db larger than the dc to 500 Hz error signal. The loop filter attenuates the 256 kHz component 85 db with respect to the dc signal and 66 db with respect to the 500 Hz signal. The 256 kHz error voltage at the VCO input is therefore 32 db down with respect to the dc and 11 db down with respect to the 500 Hz error signal for a 0.1° dc or 500 Hz error and may therefore be neglected. Equation B then reduces to:

Equation C. $e_{out} = K_{pd} \cos (w_p t - \emptyset)$ volts/degree

This shows that the phase detector output voltage is zero when the

input phase difference, $w_p t - \emptyset$, is 90^o. Hence, the loop locking condition will be for V_{Pilot} and V_{vco} to be 90^o apart because this is the condition for which the error signal output is zero.

Now consider the input signal to the phase detector as a frequency difference (w_p) instead of a phase difference. Assume the phase detector is a perfect integrator with transfer function K_{PD}/s and equation C transforms to:

$$e_{out} = \frac{K_{PD} \sin (w_p t - \emptyset)}{w_p} \qquad \text{folt sec/degree.}$$

Combining gains, we get the open loop gain of the phase locked loop as:

$$G = \frac{AK_o Kpd}{w_p} \sin (w_p t - \theta).$$

The gain is maximum for input phase differences ($w_p t - \emptyset$) of 90^o and decreases toward zero as $w_p t - \emptyset$ approaches 0^o or 180^o, or, if the loop amplifier saturates. In a high gain system the loop amplifier saturates at a few degrees of phase error (for the present system the saturation occurs at 0.1^o for dc and 2.5^o at 500 Hz error signal). The required loop amplifier gain for a given static phase error, Ψ, can be found from the open loop gain equation by setting G=1 and w_p equal to the maximum expected open loop frequency difference. Assume a maximum allowable phase error of 0.1^o at the highest channel frequency of 200 kHz, and a corresponding phase error at 0.062^o of 128 kHz. This phase error will occur when the frequency error is the greatest (maximum frequency error being $\pm$ 1% of 128 kHz). Substituting the above in the gain equation:

$$A = \frac{Gw_p}{K_o K_{pd} \sin (w_p t - \theta)} = \frac{2\pi \cdot 1.28 \quad 10^3 \cdot 360}{3.15 \cdot 10^8 \cdot 0.055 \sin 0.062^o} = 86 \text{ or } 38 \text{ db}$$

The loop amplifier gain is 37 db at 500 Hz and 56 db at 10 Hz and below. The theoretical phase error should therefore be approximately 0.1^{o} or 54 db for a 500 Hz error signal and approximately 73 db or 0.01^{o} for error signal frequencies below 10 Hz. The phase locked loop locking range, f_L is defined as the maximum open loop difference in frequency between the input pilot and the VCO that the system can accommodate in the closed loop condition.

$$f_L = AK_oK_{pd} \text{ degree/sec}$$

Using the previous gain values: f_L = 120 kHz. Because the VCO cannot be pulled 120 kHz with respect to a nominal 128 kHz, the system has considerable excess gain and saturation of the loop amplifier will determine the locking range.

The time constants in the loop have not yet been considered, but it can be seen that they do not effect the locking range or the static phase error because w_p is zero in the locked condition. If, however, the pilot frequency starts from some value above the locking range and is slowly brought closer to the VCO frequency, the amount of frequency modulation of the VCO frequency will be equal to the loop gain as reduced by the loop filter when w_p is above the loop filter cut-off frequency. Since G is less than 1 when the pilot frequency is outside the locking range, the frequency modulation on the VCO frequency is not enough to make the VCO frequency intersect the pilot frequency and locking, therefore, cannot occur. In the present system the open loop gain is 1 at approximately 2.5 MHz, and there is sufficient gain beyond the range at which the VCO can be pulled that the capture range is limited by the amplifier saturation.

IV. ALIGNMENT PROCEDURE

A. VOLTAGE CONTROLLED OSCILLATORS - PHASE LOCKED LOOPS

Two adjustments are available on the phase locked loops. One is L2, which adjusts the free running frequency of the VCO, and the other is R30, which adjusts the output balance of the phase detector and therefore the PLL phase relative to the pilot to some degree. To align the PLL connect on oscilloscope probe to the output of A10 with the vertical scale set for 5 V/div dc. The output of A10 should be near 0V dc. If it is not, adjust L2 so that the output is close to 0V dc for the 320 kHz PLL and about -1 to -2 V dc for the 256 kHz PLL. If phase lock cannot be accomplished by adjusting L2 then R30 should be alternately adjusted along with L2 until the loop is brought into locking range. Then L2 should be adjusted as described above.

B. MODULATORS

The modulators are adjusted for minimum carrier and modulating frequency feedthrough by adjusting offset potentiometers R5, R15, R21, and R26. Carrier inputs of 64 kHz at 0^{o} and 90^{o} at a 4 V p-p level is fed into the X inputs. Modulating frequencies of 2.5 kHz and 15 kHz at 15 V p-p are fed into the Y inputs. Connect a wave analyzer to the modulator summer output and set it to 64 kHz $\pm$ one of the modulating frequencies to establish the odb reference. Tune the wave analyzer to 64 kHz and alternately adjust R5 and R21 for minimum carrier feedthrough. Set the wave analyzer to one of the modulating frequencies and adjust the appropriate potentiometer, R 15 or R26, for minimum signal feedthrough. Set the wave analyzer to the other modulating frequency and repeat above.

To adjust for equal output levels measure both of the carrier inputs and adjust R23 on the test oscillator board. Then measure both signal inputs and adjust for equal inputs levels. Alternately disconnect each signal input and adjust the gain potentiometers R14 and R31 for equal outputs at the modulator outputs. The phase lead potentiometer adjustments cannot be adjusted without the special phase detector and procedure as outlined in the Test Procedure and Report, MCR-71-82.

C. DEMODULATOR

The modulator, demodulator, PLLs, and test oscillator are connected as a system on the delivered breadboard. With the system as delivered, the necessary signals for alignment for the demodulator are furnished by the other parts of the system. With audio signals applied to the inputs of the modulator, connect a wave analyzer to the output of the first translation summing amplifier A20. Set the analyzer for 320 kHz and adjust R2 for minimum carrier feedthrough. Set the wave analyzer to one of the input signal sidebands (64 kHz $\pm$ f_m) applied to the demodulator input by the modulator. Adjust R14 for minimum signal feedthrough. Adjust R17 for symmetrical output about the dc axis as observed by an oscilloscope connected to the output of A2.

Connect the wave analyzer to the output of A7 and adjust R55 for minimum 256 kHz carrier feedthrough. Connect the wave analyzer to the output of A8 and adjust R79 for minimum 256 kHz carrier feedthrough. It should be noted that although adjustments are provided for carrier feedthrough suppression in the balanced modulators, carrier suppression is not required as noted in Section III-A.

To adjust for quadrature suppression feed two different signal frequencies into the demodulator and connect the wave analyzer to demodulator output 2. Set the wave analyzer to the 90° output frequency and adjust scale for 0 db reference. Move the wave analyzer input to O.P.1 and adjust R16 of the 64 kHz phase shifter on the test oscillator board for minimum 90° channel feedthrough on the 0° channel. Move the wave analyzer input to O.P.2 and adjust the phase of the 90° phase shifter on the demodulator board by adjusting R35 for minimum 0° feedthrough on the 90° channel. It is always necessary to adjust the 0° quadrature suppression first and then the 90° quadrature channel. Potentiometers R66 and R91 provide for adjustment of O.P.1 and O.P.2 outputs respectively to 0 V dc.

Adjustment of the 90° phase shifter on the test oscillator board should not be attempted without the use of an accurate phase detector.

V. PERFORMANCE AND RECOMMENDATIONS

We believe that the work performed on this contract has provided valuable information in determining the performance characteristics of state-of-the-art modulators, demodulators, and VCOS and their use in FDM systems.

A. MODULATORS

A survey of the industry revealed that only one true multiplier, the Intronics M502, provided the linearity, frequency and phase response characteristics necessary for use as a modulator for QDSBSC operation over the temperature range of -20° to $+85^{\circ}$C.

The results using the M502 multiplier show that when used as a modulator the harmonic distortion and carrier suppression are down better than 50 db; the amplitude linearity is better than 0.15%; the frequency response is flat to within 1% from dc to 200 kHz; the phase lag is about 5° at 200 kHz; and the phase linearity is better than 0.18° from dc to 200 kHz. At 200 kHz the phase drift of the two units tested was such that their phase stayed within about 0.2° of each other over the temperature range of -20°C to $+85^{\circ}$C. This indicates that it should be possible to maintain quadurature suppression of 45 db over the temperature range if all units used in a system track this well. As the frequency is decreased, the phase drift also decreases, so, below 100 kHz, 50 db of quadrature suppression should be possible.

Disadvantages of the Intronics M502 multiplier from a system standpoint are price, size, and power consumption. For a system requiring 50-100 units these factors could make its use prohibitive. A solution to this problem might be the new Motorola MC1594L monolathic multiplier which has recently been introduced. Specifications of this unit indicate that while the linearity may not be quite as good, the phase stability and frequency response may be better. This unit should be evaluated.

Double conversion was not considered feasible for the modulator because the required phase tracking in the filters could not be maintained over the temperature range.

B. DEMODULATOR

The demodulator used is a double conversion system using Motorola 1596G balance modulators. This system was selected to enable operation with the ± 1% frequency modulation on the incoming composite signal due to the tape recorder wow and flutter. This system has the advantage that identical filters are used for all channels. This is important because, as shown by the analysis in Section III-B, any frequency modulation on the channel frequencies causes a phase change due to the filter characteristics. When this phase change in the signal path is matched by an equal phase change in the demodulation frequency path, good quadrature suppression can be maintained. A single conversion system would require true multipliers with sine wave inputs. This would require input filters for the demodulation carriers with a matching filter in the signal path for each channel. Because the lower channels would use a large percentage of the filter BW, it would not be possible to maintain the equal phase shift above and below the channel frequency that would be necessary for the modulation sidebands. Also, the single conversion system would require matched pairs of filters at each channel frequency while the double conversion system uses the same filter for all channels.

The results of the demodulator tests show that, at the demodulator output, harmonic distortion is down better than 50 db; the frequency response is flat to within 0.1 db from dc to 16 kHz; the amplitude linearity is better than 0.15%; and the quadrature suppression is down better than 50 db from dc to about 8 kHz and can be adjusted to 50 db suppression for any given frequency from dc to 16 kHz.

In order to provide 50 db suppression from dc to 16 kHz without readjusting phase, better phase linearity of the first LPF in the operating portion of the filter is required as shown in Section III-B.

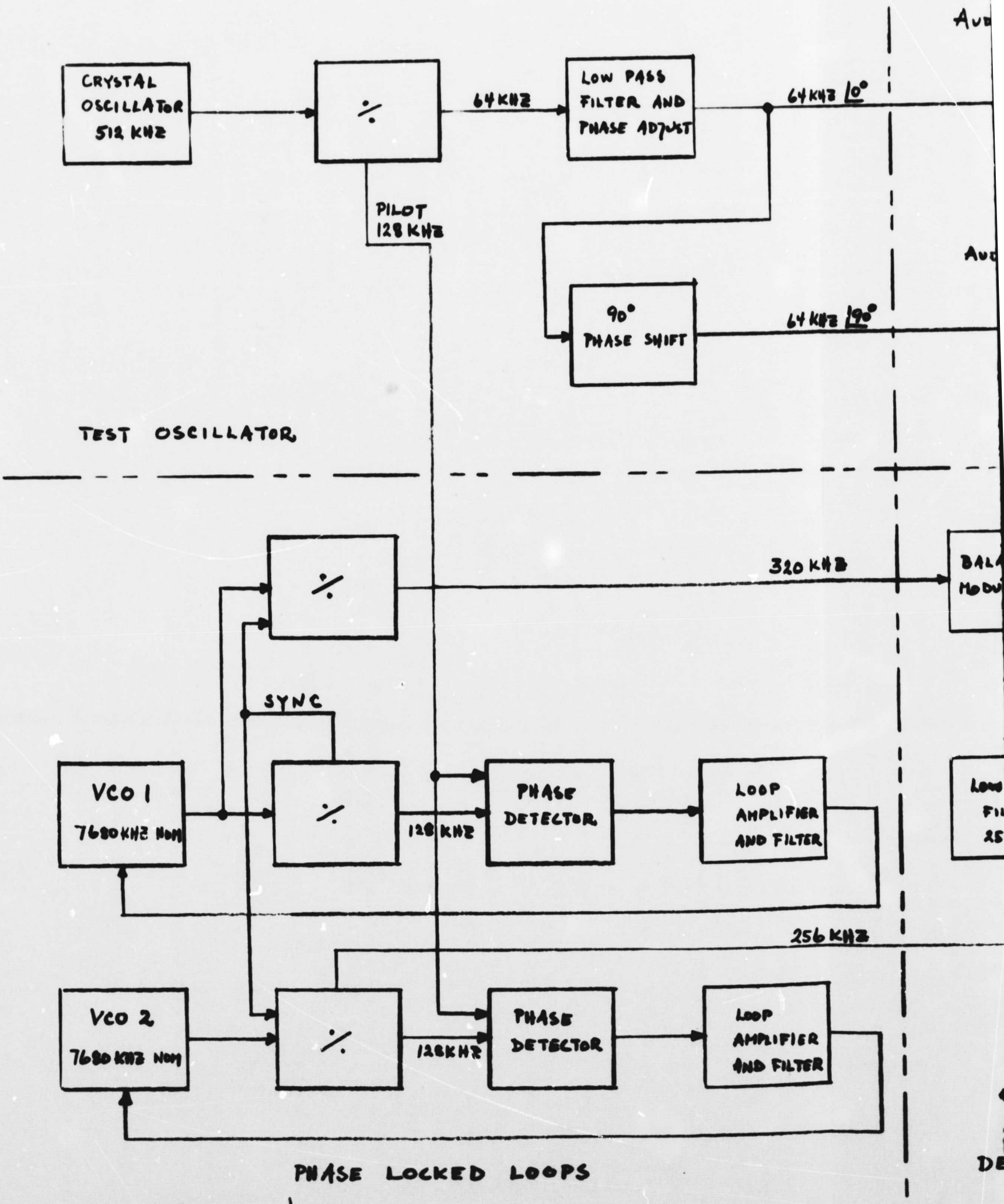
This probably can be accomplished by a special LPF designed for linear phase versus frequency or possibly by using a band pass filter instead of a LPF.

C. VOLTAGE CONTROLLED OSCILLATOR - PHASE LOCKED LOOPS

The voltage controlled oscillators use in the phase locked loops in this system are LC-VCO using two hyper-abrupt junction diode varactors for frequency control. The PLLs are capable of following a frequency modulation of $\pm$ 1% of the pilot frequency with a phase error of less than 0.18° (-50 db). The noise floor of the oscillators and divider chains is down greater than 80 db. All spurious and unwanted responses are down greater than 60 db.

A sync signal is derived from one of the VCO divider chains which has a frame rate of 64 kHz (the lowest channel frequency used). This is used to sync the other two divider chains. For a complete FDM system this sync rate would have to be at 4 kHz or the lowest channel used. It would also be an advantage to inhibit the sync signal unless any one of the loops dropped out of sync.

Crystal controlled VCO oscillators were tried and, although a frequency pulling range of $\pm$ 1% could be obtained, it is doubtful that the crystal frequencies could have been pulled fast enough to follow the $\pm$ 1% FM at a 500 Hz rate. Since the LC-VCO are clean enough and can be frequency modulated faster, they are a better choice for this application. Also, from a system standpoint, LC-VCO would be much cheaper.


CRYSTAL OSCILLATOR 512 KHZ
÷
64KHZ
LOW PASS FILTER AND PHASE ADJUST
64KHZ 0°
PILOT 128 KHZ
90° PHASE SHIFT
64KHZ 90°
TEST OSCILLATOR
÷
320 KHZ
SYNC
VCO 1 7680KHZ NOM
÷
128 KHZ
PHASE DETECTOR
LOOP AMPLIFIER AND FILTER
256 KHZ
VCO 2 7680 KHZ NOM
÷
128KHZ
PHASE DETECTOR
LOOP AMPLIFIER AND FILTER
PHASE LOCKED LOOPS
FOLDOUT FRAME

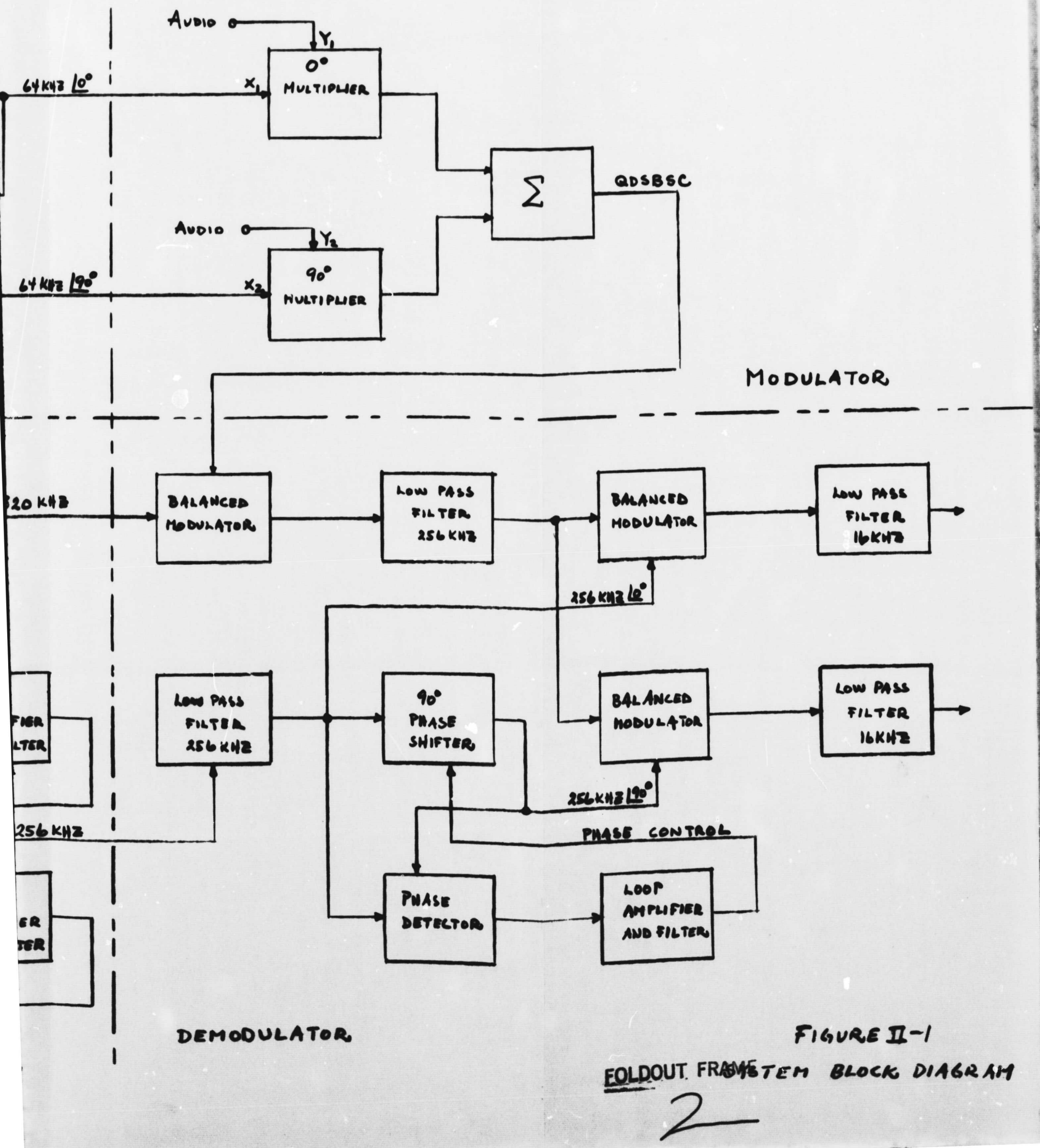
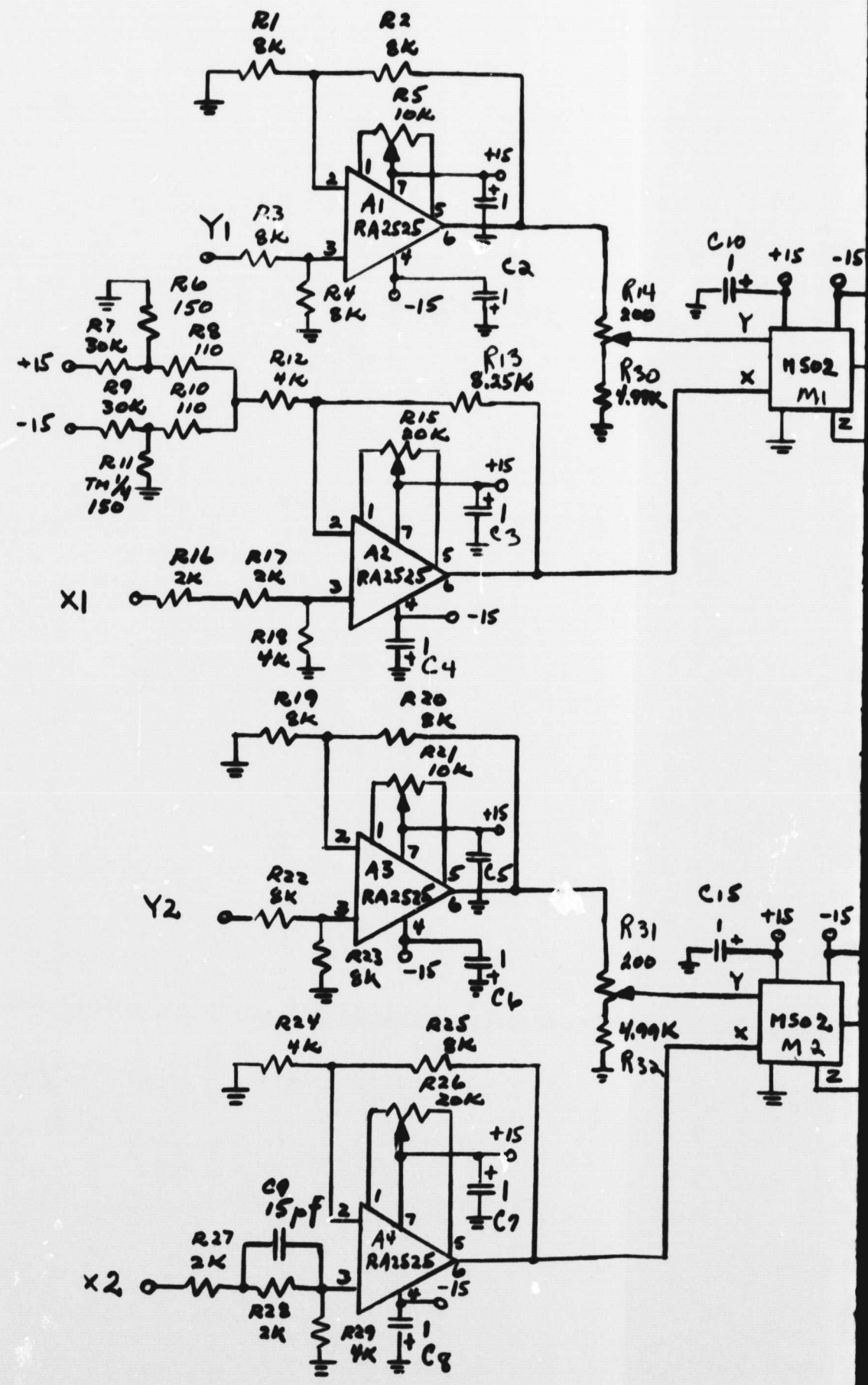


FIGURE II-1

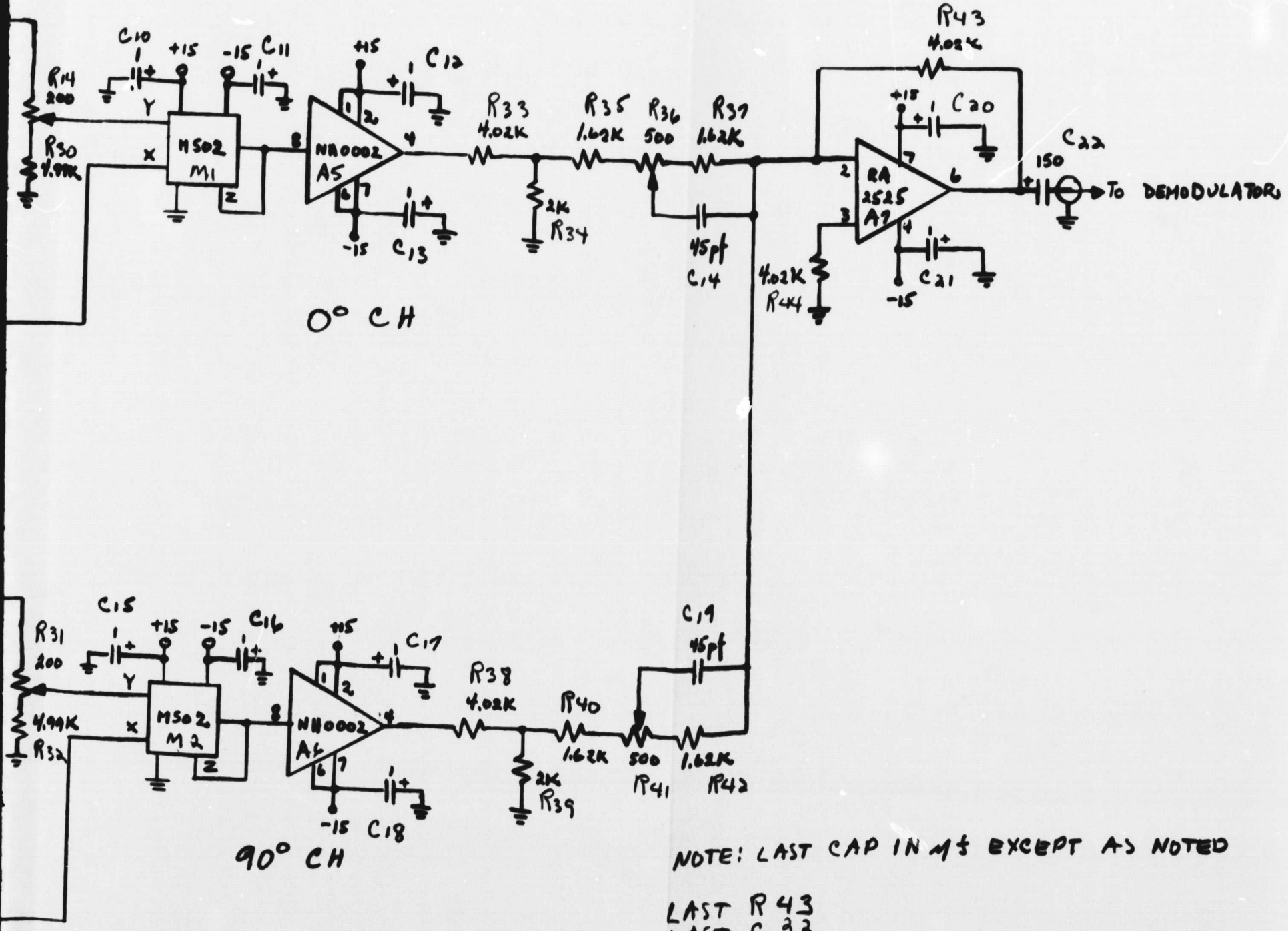
FOLDOUT FRAME SYSTEM BLOCK DIAGRAM

2



FOLDOUT FRAME

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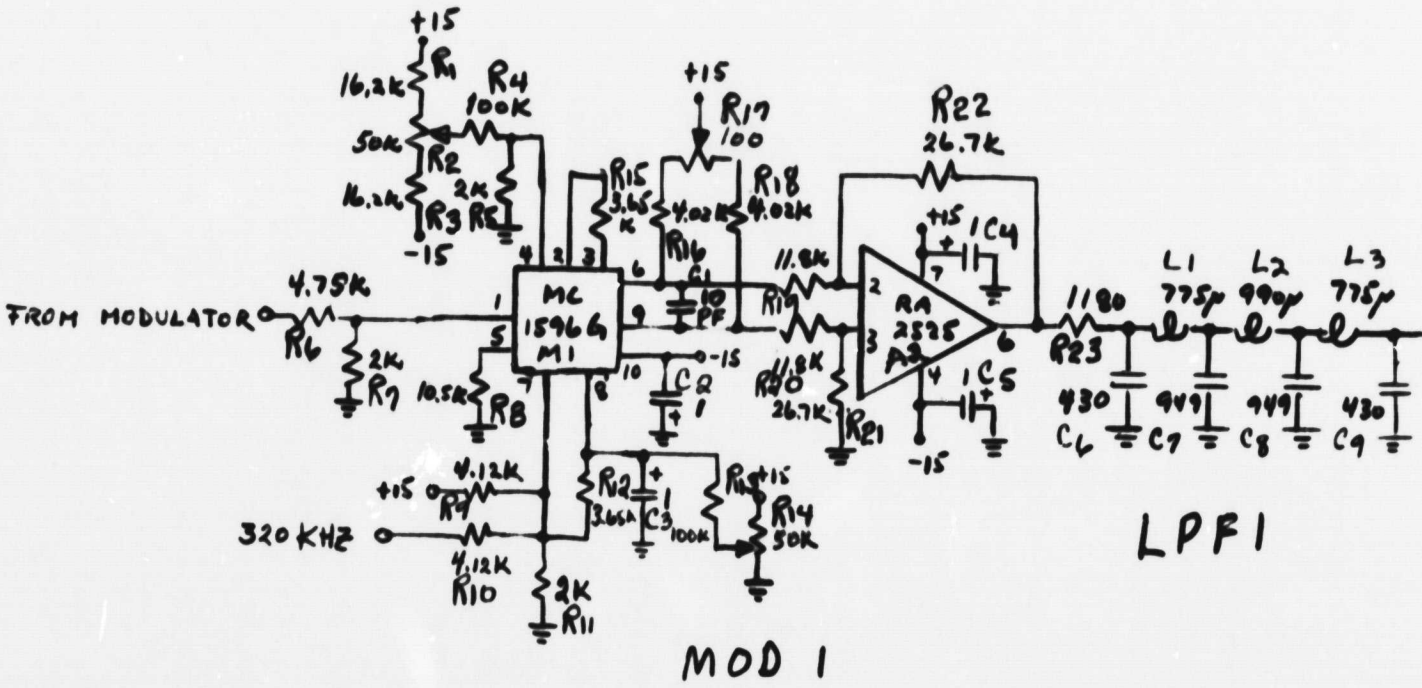
NOTE: LAST CAP IN M's EXCEPT AS NOTED

LAST R 43
LAST C 22
LAST A 7
LAST M 2

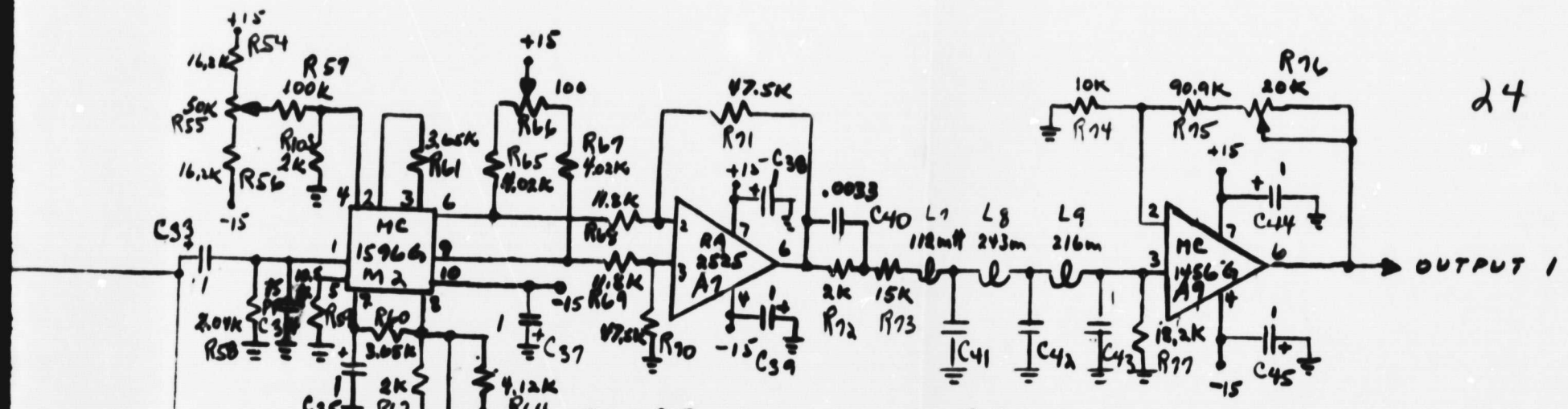
FOLDOUT FRAME 2

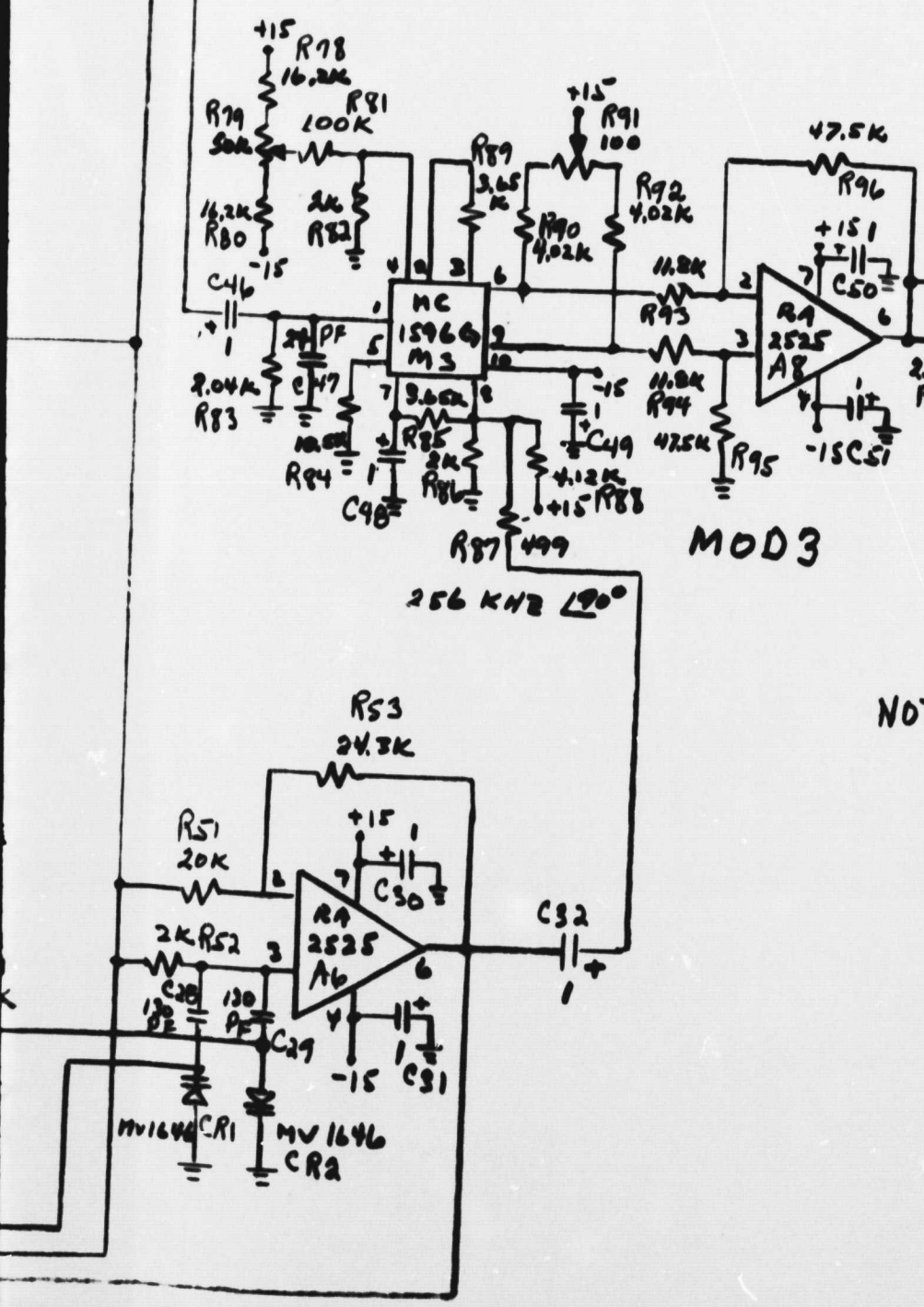
MODULATOR

FIG II-2



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90° PHASE SHIFTER

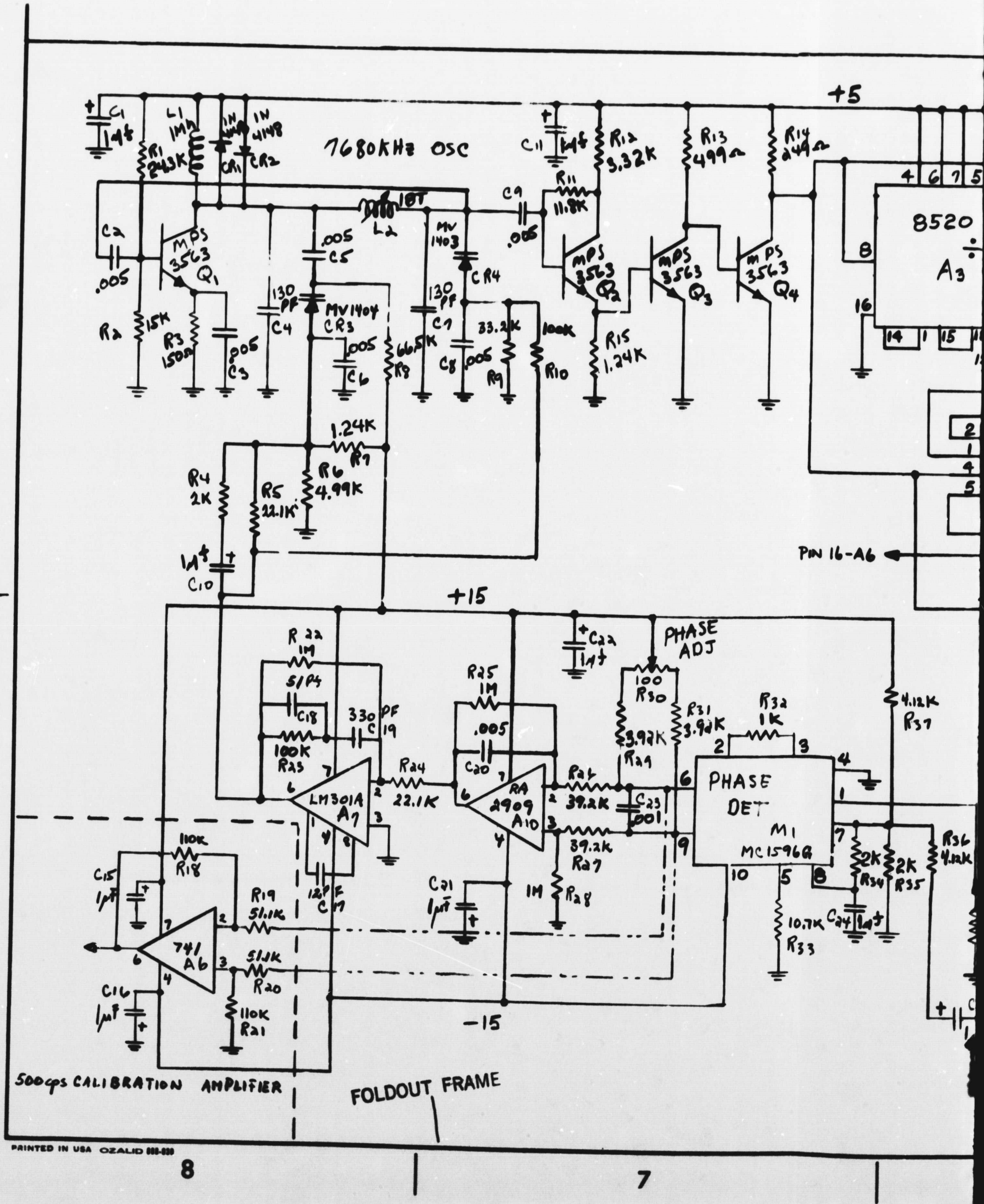
NOTE:

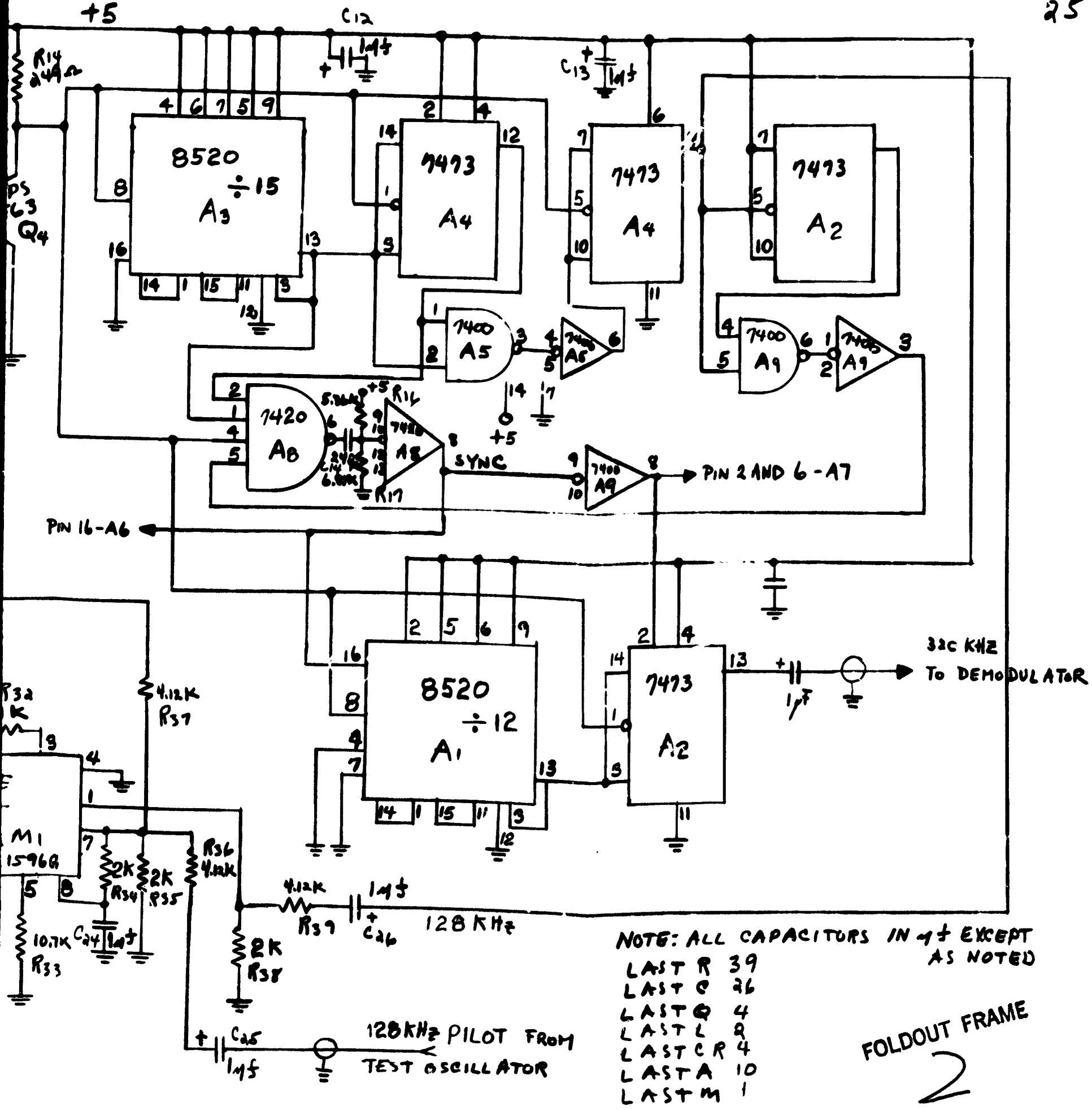
ALL CAPACITORS IN μFd EXCEPT AS NOTED

LAST A10
LAST R103
LAST C 57
LAST M4
LAST L 12
LAST CR 2

FOLDOUT FRAME 2

FIG II-3
DEMODULATOR


+5
7680KHz OSC
C1 1µf
L1 1MH
1N 4148
1N 4148
CR1
CR2
R1 243K
C2 .005
MPS 3563 Q1
R2 15K
R3 150Ω
C3 .005
130 PF C4
.005 C5
MV 1404 CR3
C6 .005
665K R8
1.24K R7
R4 2K
R5 22.1K
R6 4.99K
1µf C10
10T L2
MV 1403 CR4
130 PF C7
C8 .005
33.2K R9
100K R10
C9 .005
C11 1µf
R11 11.8K
R12 3.32K
R13 499Ω
R14 249Ω
MPS 3563 Q2
MPS 3563 Q3
MPS 3563 Q4
R15 1.24K
8520 A3
PIN 16-A6
+15
R22 1M
51P4 C18
100K R23
330 PF C19
LM301A A7
R24 22.1K
R25 1M
.005 C20
RA 2909 A10
C22 1µf
PHASE ADJ
100 R30
3.92K R29
R31 3.92K
R32 1K
4.12K R37
R26 39.2K
C23 .001
39.2K R27
1M R28
PHASE DET M1 MC1596G
2K R34
2K R35
R36 4.12K
10.7K R33
C24 1µf
110K R18
C15 1µf
R19 51.1K
12PF C17
C21 1µf
741 A6
51.1K R20
110K R21
C16 1µf
-15
500cps CALIBRATION AMPLIFIER
FOLDOUT FRAME
PRINTED IN USA OZALID

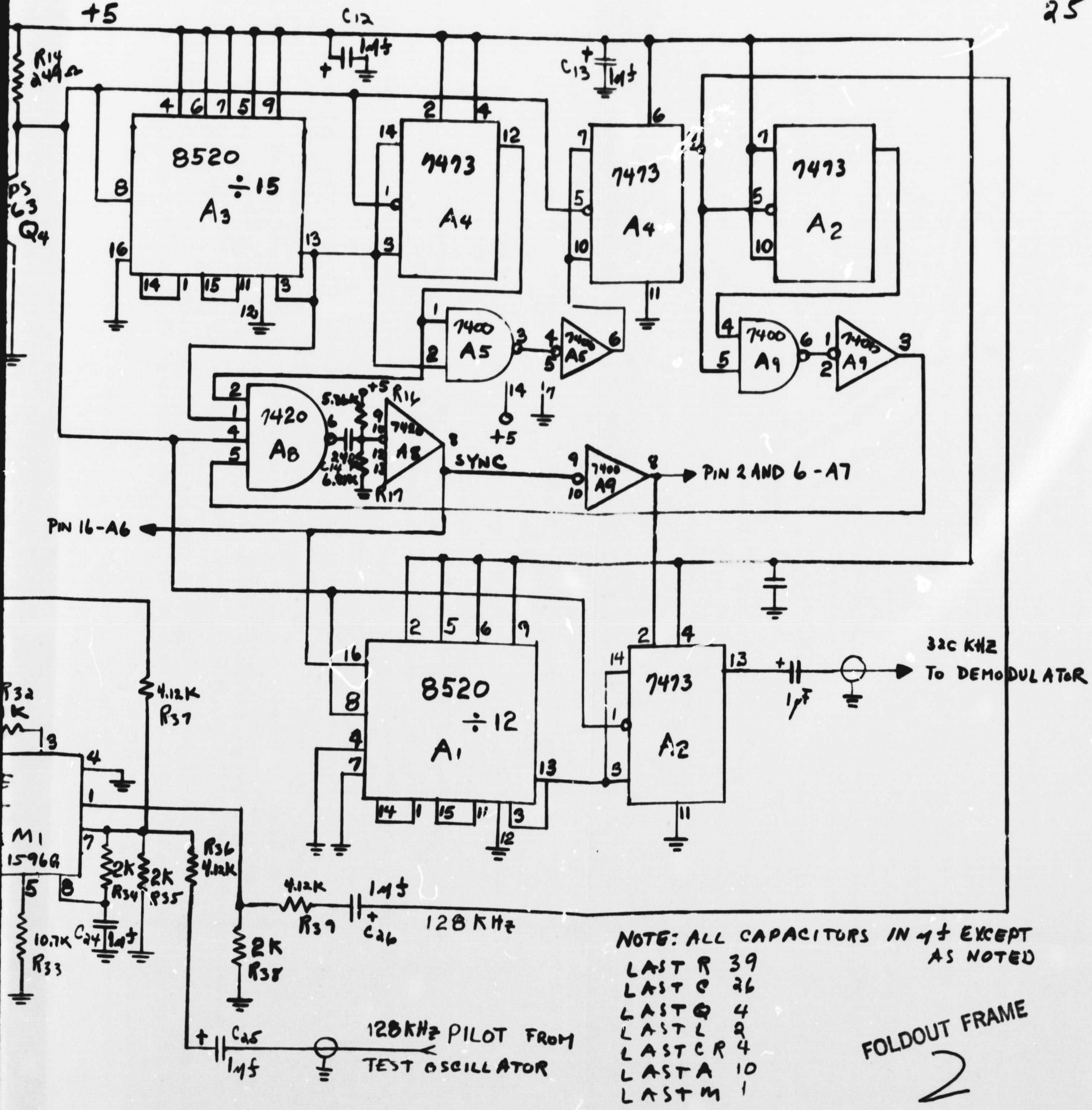


NOTE: ALL CAPACITORS IN µf EXCEPT AS NOTED

LAST R 39
LAST C 26
LAST Q 4
LAST L 9
LAST CR 4
LAST A 10
LAST M 1

FOLDOUT FRAME 2

320 KHz PHASE LOCKED LOOP
FIG II-4



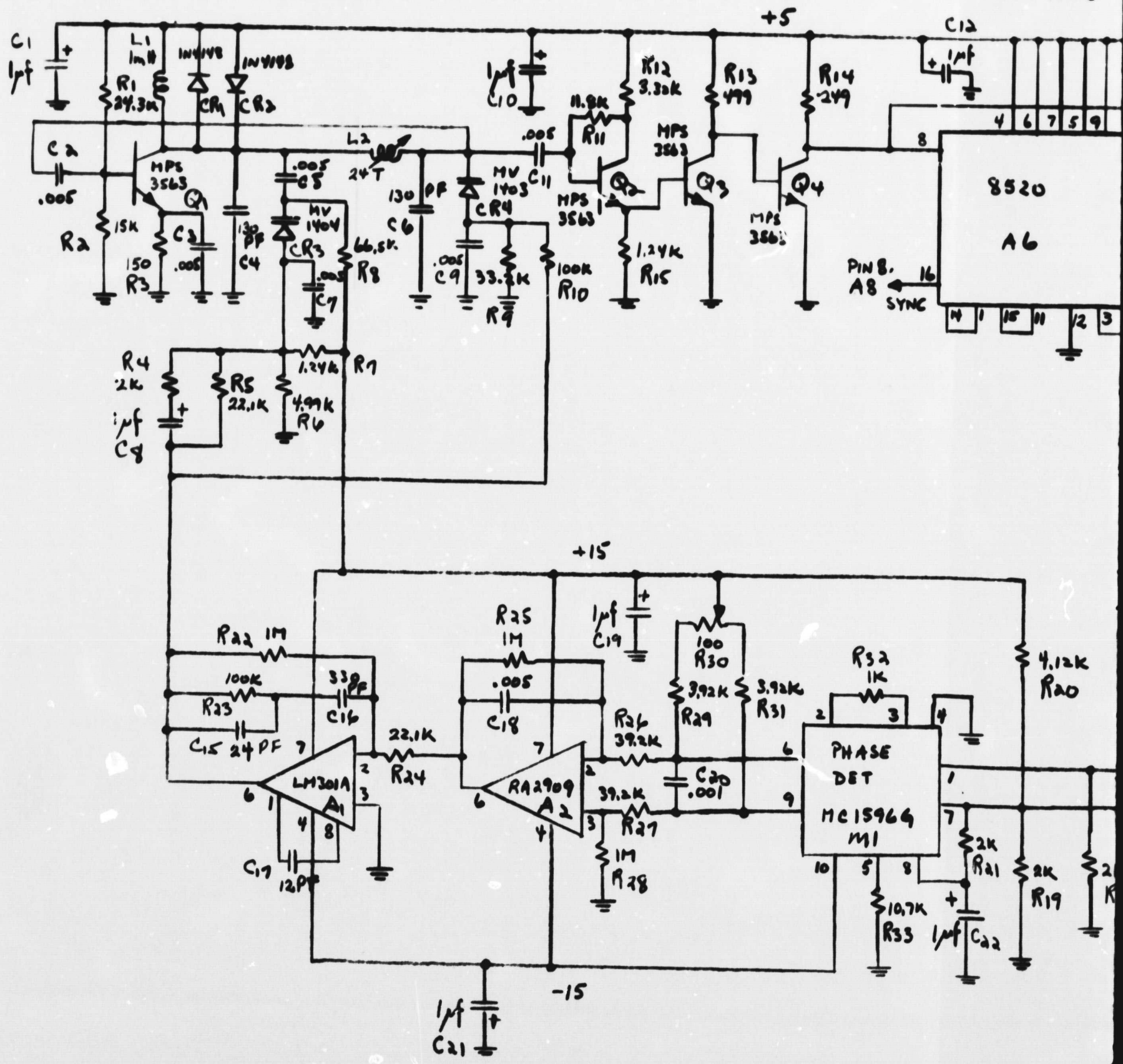
NOTE: ALL CAPACITORS IN µf EXCEPT AS NOTED

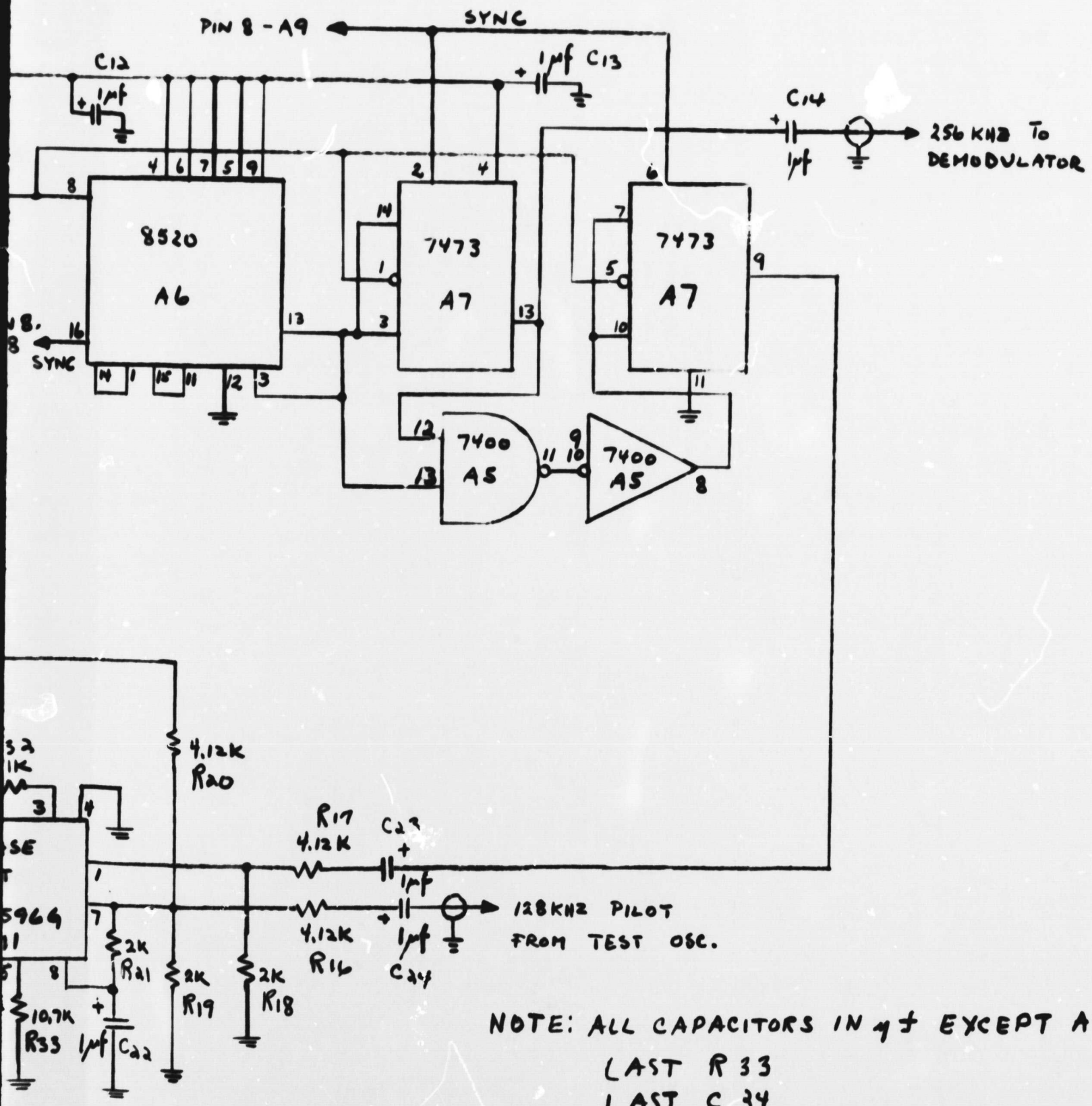
LAST R	39
LAST C	26
LAST Q	4
LAST L	2
LAST CR	4
LAST A	10
LAST M	1

FOLDOUT FRAME 2

320 KHz PHASE LOCKED LOOP

FIG II-4


PIN 8 -
+5
C1
1μf
L1
1mH
1N4148
1N4148
R1
24.3K
CR1
CR2
C2
.005
Q1
MPS
3563
R2
15K
C3
.005
150
R3
130
pF
C4
.005
C5
MV
1404
CR3
66.5K
R8
.005
C7
L2
24T
130 pF
C6
MV
1403
CR4
.005
C9
33.2K
R9
100K
R10
1μf
C10
.005
C11
11.8K
R11
MPS
3563
Q2
1.24K
R15
R12
3.32K
MPS
3563
Q3
R13
499
R14
249
MPS
3563
Q4
C12
1μf
4
6
7
5
9
8
8520
A6
PIN 8,
A8
SYNC
16
14
1
15
11
12
3
R4
2K
1μf
C8
R5
22.1K
4.99K
R6
1.24K
R7
+15
R22 1M
100K
R23
C15 24 PF
339 pF
C16
22.1K
R24
LM301A
A1
C17
12PF
R25
1M
.005
C18
1μf
C19
100
R30
3.92K
R29
3.92K
R31
R26
39.2K
RA2909
A2
39.2K
R27
1M
R28
C20
.001
R32
1K
PHASE
DET
MC1596G
M1
4.12K
R20
2K
R21
10.7K
R33
1μf
C22
2K
R19
-15
1μf
C21
FOLDOUT FRAME
B
A
PRINTED IN USA OZALID
8
7



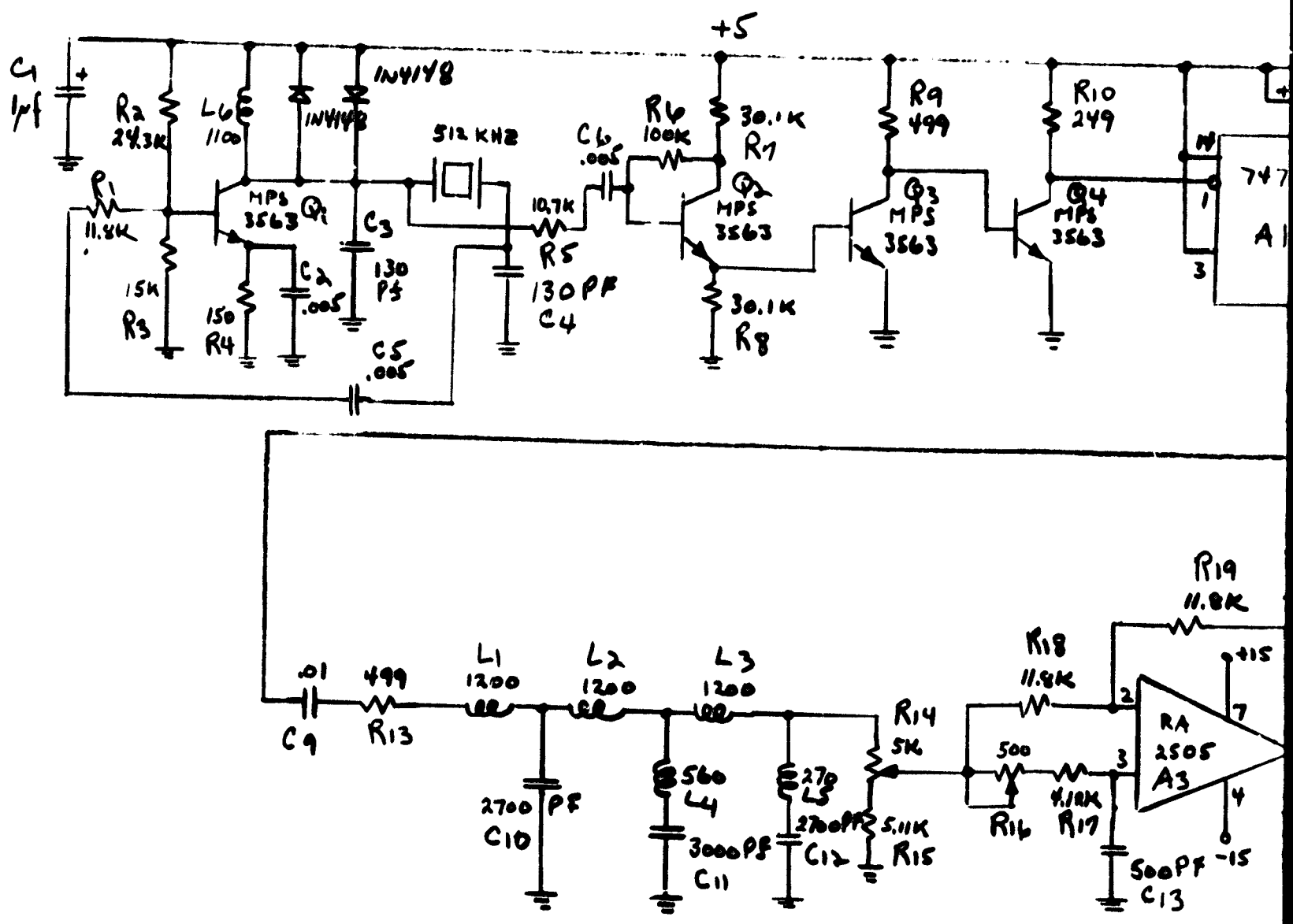
NOTE: ALL CAPACITORS IN μf EXCEPT AS NOTED

LAST R 33
LAST C 24
LAST A 7, 3 & 4 MISSING
LAST M 1
LAST L 2
LAST CR 4
LAST Q 4

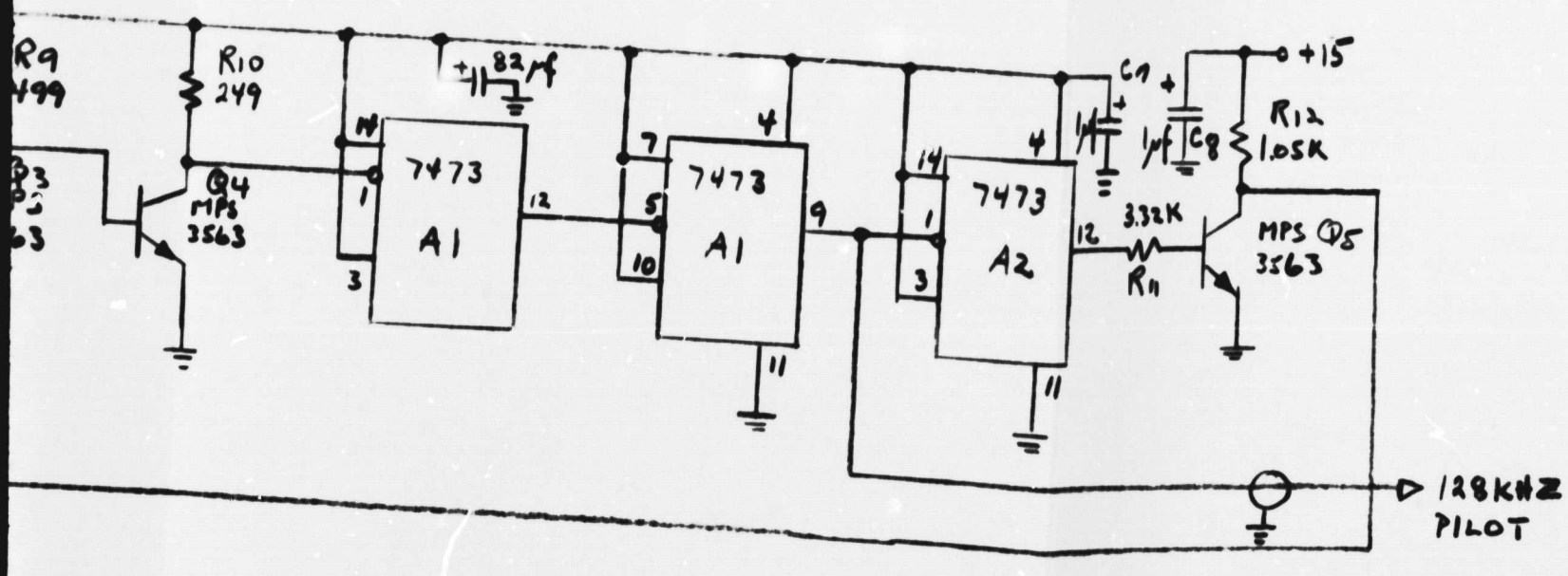
FOLDOUT FRAME 2

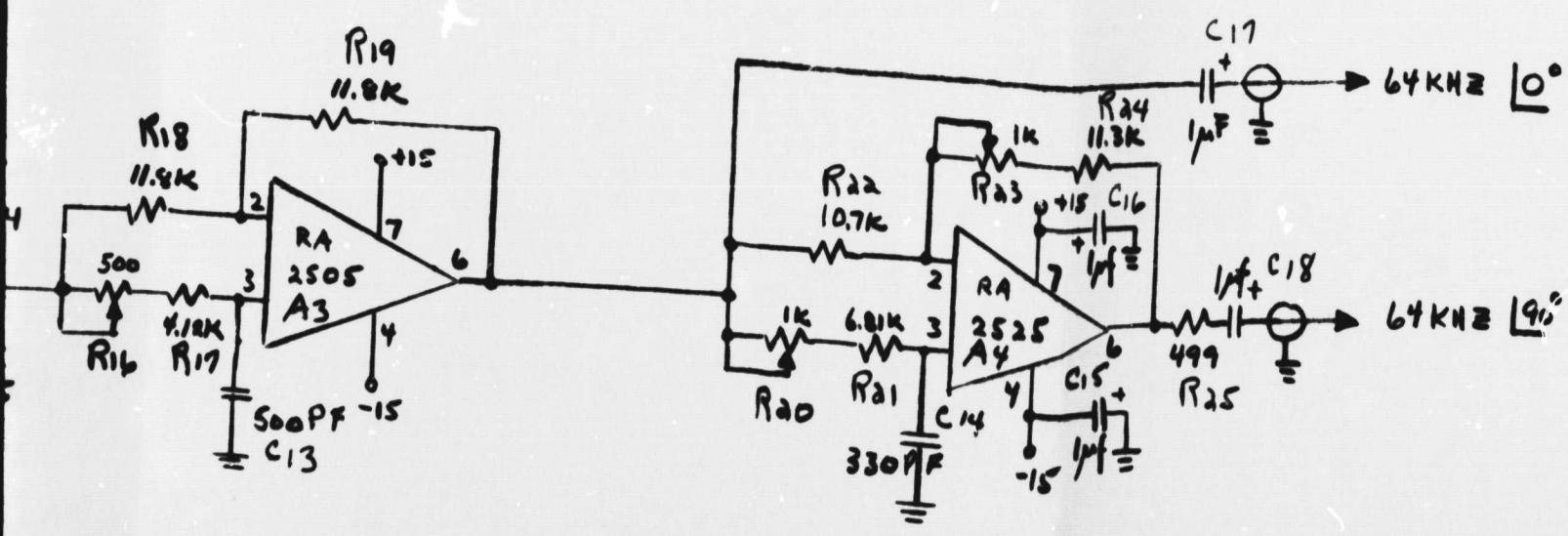
256 KHZ PHASE LOCKED LOOP

FIG II-5



FOLDOUT FRAME





NOTE ALL CAPACITORS IN μFD EXCEPT AS NOTED

LAST R 25
LAST C 18
LAST L 6
LAST A 4
LAST Q 5

FOLDOUT FRAME 2

64KHz CHANNEL TEST OSCILLATOR

FIG II-6