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MEMORANDUM

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FEASIBILITY STUDY – ON-LINE DIGITAL COMPUTER FOR ANALYTICAL OPERATIONS DIVISION, APPLIED TECHNOLOGY BRANCH, MATERIALS ANALYSIS SECTION OF QUALITY AND RELIABILITY ASSURANCE LABORATORY

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16. ABSTRACT

This document examines the feasibility of utilizing a digital computer system to support the development and exercise of various engineering and scientific activities that will be conducted by the Analytical Operations Division, Applied Technology Branch, Materials Analysis Section of Quality and Reliability Assurance Laboratory.

The functions of this system will include the following:

1. Real-time monitoring and controlling of test procedures.
2. Acquisition of data in real-time to support chemical kinetic testing.
3. Acquisition of infrared data for compounds testing.
4. Acquisition of X-ray diffraction data for materials research and testing.
5. Performing a quick-look analysis of these data.
6. Generation of edited data for off-line detailed analysis.

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SUMMARY

This document examines the feasibility of utilizing a digital computer system to support the development and exercise of various engineering and scientific activities that will be conducted by the Analytical Operations Division, Applied Technology Branch, Materials Analysis Section of Quality and Reliability Assurance Laboratory.

The functions of this system will include the following:

1. Real-time monitoring and controlling of test procedures and the provision of instrumentation and calibration checkout.

2. Real-time monitoring and controlling of chemical reaction kinetic studies; acquisition of digital data in real-time to support mass spectrometer, infrared, and X-ray experiments.

3. Performing a quick-look evaluation.

4. Generation of edited data for off-line detailed analysis for mass spectrometer, infrared, and X-ray defraction experiments.

The conclusion reached as a result of consideration of requirements imposed by the above functions, by the schedules for these projects, and by funds available is that a procurement be initiated for a mini-computer with analog/digital (A/D) and digital/analog (D/A) interfaces, as delineated later in this document. A Marshall Space Flight Center survey of existing computer systems revealed that two computers, the SEL 810 and RCA 110A, are available. However, the SEL 810 and RCA 110A are not sufficient for present requirements and cannot be readily upgraded for projected requirements. The proposed system is sufficient for present and near future requirements and can be readily upgraded for projected requirements.

INTRODUCTION

The intent of this document is to evaluate the economic and operational feasibility of the application of a digital computer system to support applied research activities of the Materials Analysis Section of Quality and Reliability Assurance Laboratory (S&E-QUAL-ARA). The Physics and Astrophysics Division, Astrophysics Branch of Space Sciences Laboratory (S&E-SSL-PA) has derived and applied algorithms for some of the instruments that will be interfaced to the computer including the mass spectrograph and will serve as a consultant with S&E-QUAL-ARA and Computer Systems Division, Systems Analysis Branch of Computation Laboratory (S&E-COMP-CS).

The Saturn, advanced Apollo, Space Shuttle, and Skylab mission and earth resources support tasks involve complex, stringent, near-field requirements for minimizing contamination and pollution in weight-limited aerospace vehicle systems and structures. As the complexity of future aerospace vehicles increases, the requirements for simulating the actual environment in which these vehicles will operate demand more detailed materials testing, manufacturing procedures, data recording, and test analyses. Advances in analytical instrumentation have resulted in instruments that have a high volume of data output to ensure accurate determination of the appropriate compounds. Although the existing spectrometer produces an accurate spectrum for "fingerprint" analysis, the present analog recording system has a limited dynamic range. For this reason, it is mandatory to record the data digitally to preserve the accuracy of the measured spectrum. Also, the massive amount of data resulting from the use of such instruments causes the analyst presently to spend more time performing routine data reductions than is spent on test procedures, development, equipment operation, and data analysis. This routine, on-line data reduction task will be performed automatically using the proposed system. The proposed system will allow the analyst to devote his time to more productive endeavors and simultaneously will increase the necessary volume and accuracy of analyses performed.

PROJECT DEFINITION – PURPOSE OF TOTAL SYSTEM

The Environmental Simulation and Materials Testing System will test electronic, chemical, and electromechanical components of aerospace systems under many space environmental or contaminate conditions such as pollution, temperature, pressure, radiation, and other atmospheres. The proposed

computer system will provide the Materials Analysis Section with an engineering tool needed to advance the development and implementation of environmental engineering and scientific studies. These applied studies are needed to simulate the large booster engine combustion materials behavior under upper atmosphere and reentry conditions and to perform experiments for material contamination research. The computer systems will perform on-line data collection, real-time processing, on-line data compression, and limited statistical analyses.

The proposed computer and associated interface systems will provide S&E-QUAL-ARA with the additional capabilities necessary to achieve the following objectives:

1. Automated control to perform instrumentation calibration and checkout.

2. Real-time monitoring and controlling of kinetic, infrared, and X-ray analysis testing.

3. Performing a real-time quick-look evaluation.

4. Recording of edited data for off-line detailed analysis.

5. Identification of compounds and alloys and verification of the integrity of vehicle components, sensors, and subsystems.

These are the objectives of tasks that are being conducted in the context of overall research and development programs in support of Apollo, Skylab, Shuttle research, and other Advanced Apollo Application Extension Programs including earth resources and related projects.

TECHNICAL DESCRIPTION

Functions of Total System

The major functions (Figs. 1 and 2) of the proposed computer system are the on-line control of the mass spectrometer, infrared and X-ray diffraction spectroscopy, and the provision of systems verification that is necessary to support contamination testing and metallurgical research. The mass spectrometer produces a spectrum versus wavelength of the specimen

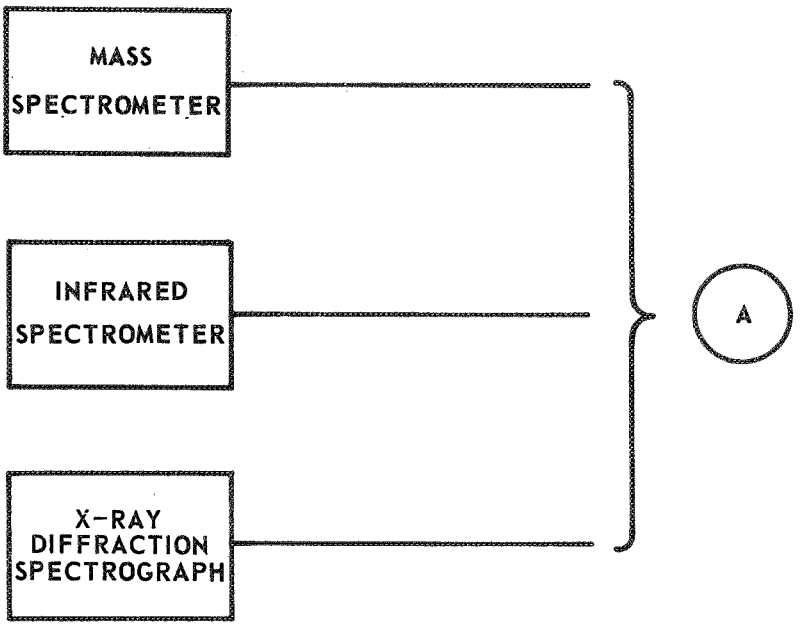

Figure 1. Environment Simulation and Materials Testing Computer System.

sample being tested. The output spectrum is recorded so that a more detailed analysis can be performed to determine those compounds present. The infrared spectrophotometer supplies an infrared absorption spectrum of a sample by irradiating a sample with successive wavelengths of infrared light and measuring the degree to which the sample absorbs this light. This instrument is used continually to measure the degree of hydrocarbon (CH group) contamination in gas bearings, air bearing systems, and components. The measured output spectrum is used in identifying unknown contaminants, such as lubricants, and tracing leaks in fuel systems. When an X-ray beam falls upon a crystal, it is transmitted as a number of diffracted beams and these beams can be recorded. Since every crystalline chemical element produces a pattern that is characteristic of the particular kind and arrangement of atoms, it can be used to identify a solid by comparison with known patterns. A crystal can be used as a reflection grating, and in this connection the Bragg equation is used. This is given as $n\lambda = 2d \sin \theta$, where n is the order of the spectrum (if nonchromatic radiation is used, n is the order of reflection), λ is the wavelength, d is the distance between the parallel planes of atoms, and $(90^\circ - \theta)$ is the angle of incidence.

The function of the computer is to record the spectrum in order to compute d, σ, and λ. The computer system will produce a library of various spectra that are needed by the laboratory to verify the integrity of vehicle

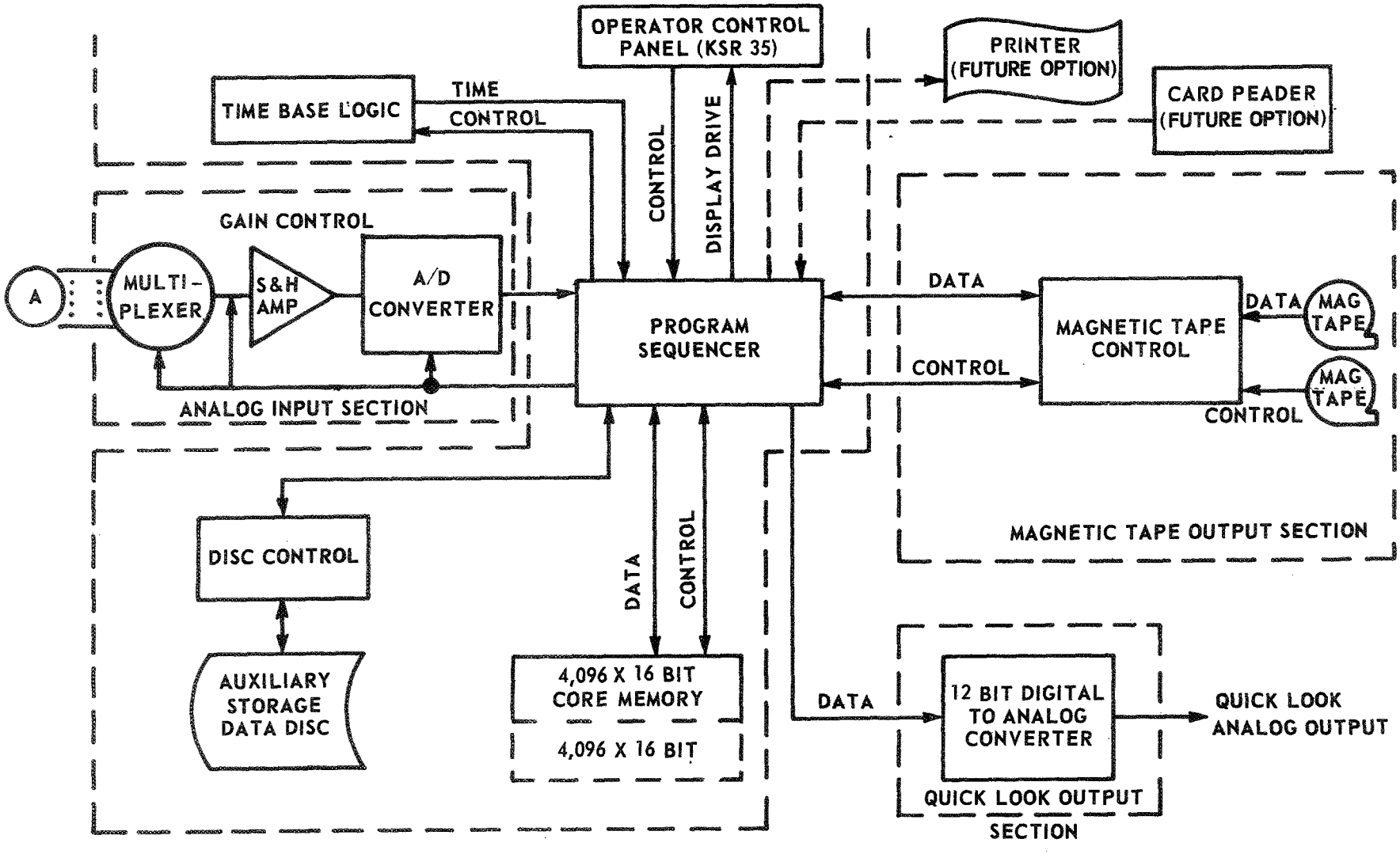

Figure 2. High resolution data acquisition and computer system block diagram.

components, materials, and subsystems. The computer system will be time-shared with kinetic, infrared, and X-ray testing. Other functions that the computer will perform are as follows:

1. Calibration and identification of spectra peaks for nonlinear output of the mass spectrometer, X-ray, and infrared data.

2. Performing various data operations on the mass spectra such as data compression and data correction including background subtraction, peak removal, and dc drift.

3. Performing experiment control based on closed-loop feedback parameters such as temperature, pressure, radiation, and intensity.

The data acquisition subsystem must be capable of accepting 16 data channels (readily upgradable to 32 channels of analog inputs over a range of 10 V). The most stringent requirements of the computer system are to simultaneously record a large number of data channels necessary to preserve dynamic range and to monitor and control test procedures in real-time. Table 1 delineates the sampling rate requirements per channel and the number of channels necessary for a typical test.

Functions of Digital Computer

To support the environmental testing activities, the computer system will analyze spectral data from the following tests:

1. Mass/electron charge (kinetic).

2. Infrared.

3. X-ray diffraction.

These data will include the following types:

1. Spectral.

2. Intensity wavelength (near field).

3. Intensity (space or a field).

4. D Spacing (Bragg's Law).

TABLE 1. CHARACTERISTICS OF ENVIRONMENTAL SIMULATION AND MATERIALS TESTS

Type of Test	Maximum Time Duration/Test (sec)	Typical Sampling Rate/Channel (samples/sec)	No. Channels Required, Total/On Line	System Recording Throughput (characters/sec), 7 Track Mag Tape	A/D, 15 Bits
Mass Spectrometer (Spectral Output)	1800	40 000	1	119 790	15
Temperature	1800	10	1	30	15
Pressure	1800	10	1	30	15
Other Inputs	1800	10	5	150	
Subsystem Totals	1800	40 070	8	120 000	15
[a] X-Ray System	30	3 000	4	36 000	15
[a] Infrared	30	3 000	4	36 000	15

a. Time-Shared with Mass Spectrometer

The analysis performed on these data will determine the following:

1. Identification of spectral "fingerprints."
2. Intensities.
3. Detection of spectral shifts.
4. Fast Fourier transforms (filtering).
5. Inverse Fast Fourier transforms.

The mathematical operations that the computer system will be required to perform to determine the above-mentioned functions involve conventional statistical analysis techniques. Prime use will be made of simple data compression techniques and the Fast Fourier transform algorithms.

Of utmost importance is that the computer system provide the control functions necessary to acquire, identify, compress, and record the proper data from the engineering systems. These functions will include sampling rate changes, control response functions, test point address changes, interrupt conditions, monitoring, and on-line query/response communications with operation personnel. It is most important also that the computer be able to perform data compression so that the mass spectrometer data can be digitally recorded accurately in real-time.

The output produced by the programs required to support these functions will include printed quick-look test reports and digital plots, particularly of mass distribution, correlations, and transfer functions.

Proposed Computer System Hardware Configuration and Component Functions

To satisfactorily meet the requirements dictated by the engineering systems described in the section entitled Functions of Total System and the computer functions delineated in the section entitled Functions of Digital Computer, the computer system selected for this application must possess certain configuration and functional characteristics. These characteristics are outlined in the following and are grouped under the headings Computer/Peripherals Subsystem, Computer Interface Subsystem, and Data Acquisition Subsystem.

Figures 1 and 2 illustrate a functional block diagram of such a computer system.

COMPUTER/PHERIPHERALS SUBSYTEM

The computer system must have the ability to perform within a time frame of 25 μ sec in the following sequence:

1. Position multiplexer to a random specified data channel.

2. Set A/D program gain option.

3. Acquire any one data channel of maximum (1000 to 40 000 samples per second) word rate. Six other data channels also are to be sampled at a much lower rate (10 samples per second).

4. Compress the 40 000 samples per second data rate so that this meaningful data can be recorded on digital magnetic tapes accurately.

All first and most second generation mini-computers are unable to perform this rapid recording rate. Can older available computers be upgraded with special hardware that would perform these rapid recording tasks? No, because manufacturers of these available computers will not upgrade their older designed hardware. This obsolete hardware is no longer available and to retool for manufacturing is beyond economical realities.

The data compression technique is described in the following in a more detailed way to explain why most second generation mini-computers are unable to perform this recording task.

For at least one data channel, the computer system must have the ability to compare each data sample to a specified threshold value (TV). A counter must be maintained for all incoming data samples smaller than the TV, and the sequence is repeated starting at 1. When an input data sample is greater than TV, the counter if greater than zero is placed in an output buffer along with an identifier, the counter is reset, and the output buffer address is incremented, or the counter is incremented. A test is made when each output address is incremented to determine if the magnetic tape record length has been completed. If the record length has been completed, the contents of the output buffer are initiated to be recorded on digital magnetic tape. The output buffer is switched to the next buffer. At least two output buffers are required to maintain tape recording efficiency. This computer subsystem will provide overall system control, data handling, and program

processing functions. It should consist of the following components, performing the indicated functions:

1. Central Processing Unit. This may be a single processor with the capability to initiate and receive control signals and information transfer to and from other subsystem components and other subsystems. The Central Processor Unit (CPU), or system, must provide real-time input/output (I/O) capability to control A/D and D/A conversions. Each peripheral device must have a hardware pointer to its own unique vector address memory words which, in turn, point to the devices' service routine. The devices' interrupt priority and service routine priority must be independent to allow dynamic adjustment of system behavior in response to real-time conditions. The CPU, or system, must provide nested interrupt servicing that can be carried out to any level. While servicing an interrupt for a device, the system must provide the capability for four hardware interrupts for servicing a higher priority device or devices.

A peripheral device register must be provided that can be either read or set by the control processor or other peripheral devices; thus, the same register must be capable of being used for both input and output functions. A master-slave relationship must be provided between the I/O bus and the CPU. At any point in time, there is one device that has control of the I/O bus.

The bus master control capability must be granted to each peripheral, including the CPU, every 950 nsec so that about 12 computer instructions can be executed every 25 μsec per data transfer. No device or controller may lock out any other peripheral device for a time greater than one memory cycle. The system must provide capability for asynchronous operations and for the system memory. All I/O devices transferring directly to or from memory should offer the ability to steal memory cycles during instruction operation.

Provision should be made so that the processor's priority can be set under program control to one of eight levels in the processor's status register. The capability to set a priority level that inhibits granting of I/O bus requests on the same or lower levels must be provided. Also provisions must be made that enable one to connect devices to the bus request line so that slower peripherals can be honored prior to a faster system peripheral. Also, peripheral buffers and status registers should have the capability to be interrogated, as memory locations do.

In addition, the CPU must perform the bit manipulation within each data sample interval and must compare logic as necessary to format, parse data words, and carry out the necessary mathematical operations with the required accuracy.

2. Primary Memory Unit. This unit must be directly accessible from the CPU or I/O bus, in random fashion, and capable of initiating parity error indications. It must be 8192 words or larger to contain program segments and data blocks of a sufficient size to allow optimum efficiency of system operation. The memory cycle time must be less than 950 nsec to perform about 12 necessary processing instructions between interrupts.

3. Hardware Interrupt Lines. These lines should establish direct, discrete communication links between the components/test points being monitored and the CPU. There should be approximately eight interrupt lines available to provide effective communication for on-line system monitoring and control by the CPU.

4. Two Direct Data I/O Channels. These channels will provide the direct communication links necessary for control information and data transfers between the CPU and the computer peripherals that are part of this subsystem. There must be a sufficient number (minimum of two) to allow attachment of the peripherals indicated below. The channel I/O rate must exceed that of the fastest attached peripheral device. It should be capable of parallel transfer of at least a full CPU word so that transfer of large blocks of data can be initiated by the execution of a single set of instructions, after which normal CPU operation may be resumed.

5. Auxiliary Storage Units(s). This peripheral device should be attached to the director-multiplexed I/O channel and will store both final (long term) and interim data from both systems and applications software. In view of the latter, it should have the highest possible transfer rate (obviously it is not necessary that the rate exceed that of the I/O channel), and its transfer bite size should be compatible with that of the CPU word. This unit should also generate appropriate parity error indications.

6. Digital Printer/Plotter. This peripheral device should be attached to the A-character I/O channel. The plotter will be used to present graphic digital plots as system output in a final form. The printer will produce the greatest majority of final form, alphanumeric report data. In addition, it will serve as the output media for assembly listings, diagnostics printouts, and other hardcopy reports.

7. Teletypewriter. This peripheral device should be attached to the A-character I/O channel. It will be used to record (in final form) such information as run accounting data, etc. Primarily, however, it will provide the system's main man-machine interface device to present relatively small amounts of program control and other data of an interim nature.

8. Card Reader. This peripheral device should be attached to the multiplexed I/O channel. It will function as the main device for input of software-processor and other program development/control related input data.

COMPUTER INTERFACE SUBSYSTEM

The computer interface subsystem will provide the necessary interface between the data acquisition subsystem hardware (see the section entitled Data Acquisition Subsystem) and the digital computer mainframe itself. Functionally, it will consist of the following components with the indicated responsibilities:

1. Control Logic. This component sequences operation of other components of this subsystem and provides the computer CPU with information concerning the status of the subsystem.

2. Computer Interface. This system of buffers provides interface linkage between the CPU and other components of this subsystem.

3. Assembly Register and Gating. These components provide a communication link between the interface subsystem and the specific external device being utilized.

4. Holding Register. This device puts the external device address code, received from the CPU, into proper format and transmits it to the data acquisition subsystem component responsible for accessing that particular external device.

5. Instruction Decode Buffer. This device sets up particular external devices, specified by code from the CPU, for accessing by the data acquisition subsystem (primarily used to initialize or reset external devices).

DATA ACQUISITION SUBSYSTEM

The data acquisition subsystem will provide the interface between the computer system hardware and the engineering system hardware and will consist of the following components which will perform the indicated functions:

1. Sample-and-Hold Amplifiers. These components will collect data samples from each test point and preserve each signal until it can be converted by the multiplexer/digitizer. This will give the system the capability to multiplex 16 data channels.

2. Multiplexer/Digitizer. This unit will switch the input channel among the various external test points and convert incoming analog signals from the sample-and-hold amplifier to digital values. It will contain the following components:

a. The multiplexer will provide input data of several channels to one gain-control, sample-and-hold amplifier that will feed one A/D converter.

b. The multiplexer sequencer will switch the input channel to a particular external test point.

c. The A/D converter changes the analog input signal to digital values.

3. D/A Converters. These units will convert digital values provided by the computer subsystem to analog voltage values and transmit them along a specified output control channel.

4. Line Drivers and Cabling. The configuration of the data acquisition facility will require the system to receive and transmit information and control signals over approximately 36.4 m (120 ft). To preserve the integrity of the signal under these conditions, the system will require three line drivers and the necessary shielded cabling to carry the signals from the recording equipment hardware to the data acquisition hardware.

Proposed Computer System Hardware Characteristics

The hardware characteristics presented below are specified for the components of the configuration outlined in the preceding section, Proposed Computer System Hardware Configuration and Component Functions. This

configuration, possessing these characteristics, is believed to most efficiently satisfy the system requirements, as specified in previous sections of this document, within the constraints of operational aspects and economic realities.

1. Central Processing Unit

a. Single processor.

b. Word size should be a multiple of data sample size, which for accuracy is 14 bits; therefore, the CPU word size should be 16 bits or greater.

c. Instruction set.

(1) The instruction set must provide addressing capabilities as follows:

(a) sequential addressing.

(b) full address indexing.

(c) full 16-bit word addressing.

(d) 8-bit byte addressing.

(e) stack addressing.

(f) indirect addressing (minimum 32 068 words).

(2) The instruction set must possess the following characteristics:

(a) the ability to interrogate peripheral buffers and status registers as it would memory locations.

(b) the capability to utilize memory locations as accumulators.

(c) the ability for a single instruction to move a source operand to a destination location.

1 provide the capability to load all general registers with the contents of memory addresses.

2 provide the capability for operands to be pushed onto a stack; provide the capability for operands to be popped off a stack.

3 the ability to move the contents of one register to another register must be provided.

(d) the capability for automatic nesting of subroutines, reentry, and multiple entry points. Subroutines may call other subroutines (or indeed themselves) to any level of nesting without making special provisions for storage of return addresses at each level.

To perform simultaneous operation, control response, and acquire data, the system must be equipped with a minimum of eight general registers and a central processor status register. At least six registers must be program (software) accessible and be capable of use as accumulators, pointers to memory, and/or as full-word index registers. At least two of these registers must provide the capability for stack pointing and program queing, respectively. The control processor status register must provide information on the current priority of the processor, the result of previous operations, and an indication for detecting the execution of an instruction to be trapped during program debugging.

(e) the arithmetic capability for 8-bit byte, single 16 bit, and double 32 bit operand addressing.

1 add — double word timing $\leq 2.3\ \mu$ sec.

2 subtract — 32-bit product timing $\leq 2.3\ \mu$sec.

3 multiply — 32-bit product timing $\leq 4.3\ \mu$ sec.

4 divide — 15-bit quotient + 15 $\leq 4.8\ \mu$ sec.

5 arithmetic — shifts, remainder (left and right).

6 normalize.

7 rotation.

8 complement and two's complement.

(f) conditional branches (conditional and unconditional).

1 branch if plus.

2 branch if minus.

3 branch if overflow.

4 high, low, equal, branch.

5 jump to subroutine.

6 return from subroutine.

2. Primary Memory Unit

a. Size — 8192 words or greater.

b. Memory cycle time — 0.95 μ sec.

c. Access method — randomly addressable.

d. Error indications for parity errors.

e. Memory protection — power fail-safe feature to prevent improper control of external engineering system hardware in case of power failure.

3. Hardware Interrupt Lines — Number-minimum of four lines, preferable on more than one level.

4. I/O Channel

a. Six buffered channels.

b. Word buffer size equal to CPU word size.

c. Direct memory access capability.

d. Transfer rate of greater than 100 000 words per second (one word transfer should not occupy more than 7 μ sec).

5. Auxiliary Storage Unit(s)

a. Disc — 65 000 words

b. Size — approximately 1.2 million bits or greater.

c. Speed — present requirements for minimum of 90 000 words per second; future requirements for 90 000 words per second.

UTILIZATION OF EXISTING EQUIPMENT AND PROGRAMS

Survey of Available Computer Hardware

An extensive, comprehensive survy of all category A and B hardware that is scheduled for release has been performed. Based on this survey, there are only two computer systems, the SEL 810 and the RCA 110A, that are available for this application.

The RCA 110A computer is not technically or economically feasible to upgrade because the CPU cycle response which is 28.75 μ sec compared to the 1 μ sec that is needed, is too slow to meet recording requirements, requires more floor space than is available, and requires excessive electrical power and air-conditioning.

The SEL 810 (4096 word memory with teletype, serial number 10495) does meet the floor plan requirements, electrical power requirements, and air-conditioning requirements but is not technically or economically feasible to upgrade because the core memory is no longer manufactured and no surplus SEL 810 computer memory has been located. A minimum of 8192 word memory input/output is required to meet the demands of the data acquisition. Three large 2096 data word buffers are required to maintain recording efficiency of the digital data and for generating end-of-record gaps on the magnetic tape. The remaining core is used by the system, user program modules, and overlay software structures.

Survey of Existing Software

Several mini-computers supply system software that includes a Fortran compiler, an assembler, a loader, and a monitor. The proposed system and the SEL system software satisfy all demands except in the area

of the real-time executive program. This executive software could readily be developed by the Computation Laboratory (Fig. 3).

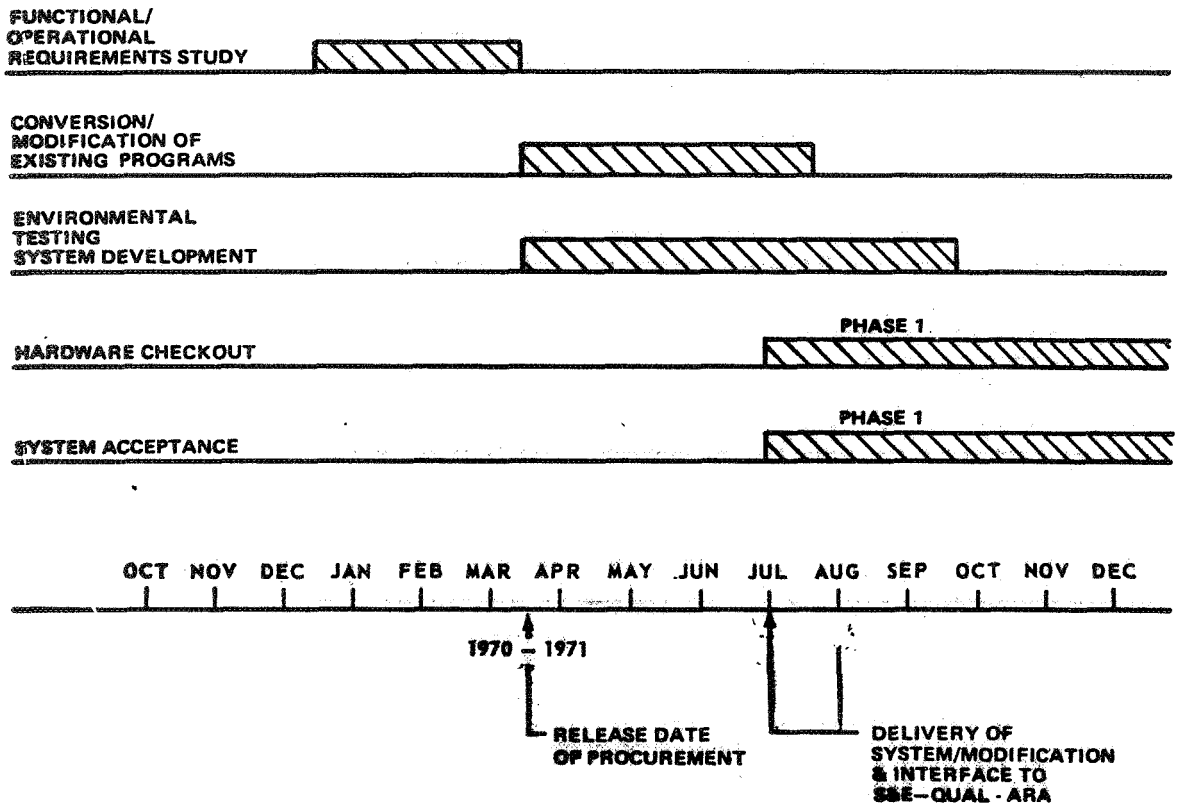

Figure 3. Projected schedule.

Proposed Software Functions

SYSTEM APPLICATIONS MONITOR

The System Applications Monitor must provide the ability to call and update user programs from disc into core memory and the ability to execute each test required via control teletype, sense switches, or a card reader. It also must provide interface to the library, math routines, and the I/O drivers' user programs and provide user data bank allocations of disc memory. Any restrictions would also be defined.

USER PROGRAMS

The Mass Spectrometer Program is a real-time program that would acquire 40 000 samples per second of real-time data from data acquisition, edit the data for validity, and record the compressed data on digital tape.

An infrared recording program would acquire 3000 samples per second of real-time data from data acquisition, and edit and record the data on digital tape.

An X-ray recording program would acquire 3000 samples per second of real-time data from data acquisition, and edit and record the data on digital tape.

Some minor application software has previously been developed for the SDS-930 compiler in Fortran II and XDS SIGMA 5 Fortran IV. The system monitor and user program development is approximately a 1 year man-effort plus an additional 2 man-months (Fig. 3).

Survey of Existing Educational/Training Service

The vendor will provide 40 hours training on the computer system. In-house personnel have previously developed computer system software and many of these programs have been in use for several years. Additional training may also be offered by the vendor or S&E-COMP-CS upon request.

OPERATIONS

The computer system will be used for approximately 5 to 6 hours of prime shift per day to support scientific testing. The remainder of the time will be used to develop and check out system software or to calibrate hardware.

The majority of engineering systems support will be on-line operations, at least in the later phases of development. There will be, however, requirements for some off-line operations related to the on-line activities. In some of these cases, it will be more efficient to do off-line work via the UNIVAC 1108 remote terminal or other computers.

Maintenance of the system hardware must be provided. Part of this cost can be deferred by having some preventive maintenance performed by Quality and Reliability Assurance Laboratory or Computation Laboratory in-house personnel.

COSTS

The approximate investment cost of the entire computer and the data acquisition under consideration (that is, the proposed computer system hardware) is estimated to be between $70 000 and $80 000, which amounts to about three-tenths of the total system. The mass spectrometer, infrared spectrometer, X-ray diffraction spectrometer, and accessories are already installed and operational; this equipment is estimated to be worth about $210 000. The cost figure for the proposed new system is based on the range of such costs for hardware comparable to that described in Tables 2 and 3.

RECOMMENDATIONS

Since the RCA 110A and SEL 810 computers are not technically or economically feasible, it is recommended that procurement be initiated to purchase a system such as described in Table 2.

TABLE 2. COST OF TYPICAL SYSTEM

Computer Equipment PDP-11/20CB		
1.	KA 11 Central Processor	$12 650
	a. 4096-word, 16-bit read/write memory, 0.95-μ sec cycle time b. Programmer's console c. Basic mounting, box and power supply rack mounted, sides and cabinet included, 230 V 60 Hz d. KSR 33 teletype and control (LT 33-CC)	
2.	MM11F (4096-word, 16-bit read/write core memory), 0.95-μ sec cycle time, includes system unit and Unibus connector	$ 3 500
3.	KE 11-A Extended Arithmetic Element — multiplies, divides, multiple shifts, and normalizes	$ 1 800
4.	Interface Equipment	
	a. KW 11-L real time clock (time interrupt)	$ 250
	b. DR 11-B, general purpose digital interface to the PDP-11 Unibus	$ 1 800
	c. Device controllers, Preston A/D converters (sign and 14 bits), 40 000 samples per second gain control and 16-channel multiplexer	$16 000
5.	Tape Controller TU10FA	$ 3 000
	a. Additional expense for upgrading to 150 IPS	$10 000
	b. Two tape transport AMPEX TM-16 150 IPS	$24 000
6.	Disc 65 000 word memory (DATA DISC, Inc.)	$ 7 130
	Total	$73 000

TABLE 3. ESTIMATED COST OF UPGRADING SEL 810 SYSTEM CONFIGURATION TO SEL 810A

1.	CPU with 8192-word, 16-bit Memory, ASR-33 Teletype, Hardware, Multiply and Divide	$ 23 000
2.	Direct Access Memory Channel	$ 4 000
3.	DATA DISC	$ 20 000
4.	Data Acquisition Controller Tapes and A/D	$ 16 000
5.	Two Tape Drives	$ 20 000
6.	A/D Converter, Multiplexer, and Gain Control	$ 8 000
	Total	$ 91 000

APPROVAL

FEASIBILITY STUDY – ON-LINE DIGITAL COMPUTER FOR ANALYTICAL OPERATIONS DIVISION, APPLIED TECHNOLOGY BRANCH, MATERIALS ANALYSIS SECTION OF QUALITY AND RELIABILITY ASSURANCE LABORATORY

By Murl H. Newberry

The information in this report has been reviewed for security classification. Review of any information concerning Department of Defense or Atomic Energy Commission programs has been made by the MSFC Security Classification Officer. This report, in its entirety, has been determined to be unclassified.

This document has also been reviewed and approved for technical accuracy.

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