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VOLTAGE TRANSIENTS DUE TO PHASE-ANGLE SWITCHING OF SPEED CONTROL POWER FOR A BRAYTON CYCLE ALTERNATOR

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16. Abstract
The voltage transients resulting from phase-angle switching of the Brayton cycle alternator speed control circuit were investigated. The alternator, speed control circuits, and the parasitic load were simulated on an analog computer. This simulation confirmed that these voltage transients resulted from the effect of the self-inductance of the alternator on the rapidly switching currents of the speed control. It was also demonstrated that an inductance-capacitance (LC) line filter, presently designed into the speed control circuit, effectively suppressed these transients from the alternator output terminals.

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SUMMARY

The Brayton engine speed control consists of speed sensing circuitry, logic for regulation and control of electronic switches, and inductance-capacitance (LC) line filters. Speed control is accomplished by switching the excess generated power into a parasitic load resistance through a silicon controlled rectifier during a portion of the voltage cycle. This switching action results in the generation of voltage transients. The circuit was simulated on an analog computer to examine the characteristics of these transients, to evaluate the effectiveness of the filters incorporated into the speed control design for transient suppression, and to determine whether supplementary filter circuits may be desirable.

Test results showed that the voltage transients are generated by the effect of the alternator self-inductance on the parasitic load current. The existing LC filter suppresses transients to minimal levels at the alternator terminals. Additional filtering at the parasitic load proved to be impractical. Waveforms taken during actual steady-state operation of the alternator and speed control are compared with those obtained from the analog simulation for approximately 3 kilowatts of parasitic load, considered to be the "worst case."

INTRODUCTION

The Brayton cycle power conversion system, under development by NASA Lewis Research Center (refs. 1 and 2) is now in the hardware testing stage. The system delivers up to 15 kilowatts of useable electric power at 1200 hertz, three phase, 120 volts line to neutral. A turbine-driven four-pole brushless alternator (ref. 3) operating at 36 000 rpm generates the electrical power.

Alternator speed depends entirely upon the relation between the net input power furnished by the turbine and the load demand at the alternator output. Any change in either the input or output will result in a change in speed and, hence, in frequency unless some speed control device is employed. Power delivered by the turbine may be controlled by valves (ref. 4) which adjust the system gas flow to suit changes in the alternator load. On the other hand, if turbine input power is constant, alternator output load may be held approximately constant by means of an electronically controlled parasitic load (ref. 5) which dissipates the excess generated power when user load demand is reduced.

The Brayton engine uses parasitic loading to control engine speed. The speed is sensed by continuously monitoring the alternator frequency with the speed control package. The sensing circuit develops a dc error signal which is proportional to the deviation from the preset frequency. This signal is fed to a magnetic amplifier, the output of which is applied to the control winding of a saturable reactor. The saturable reactor in turn develops the voltage to control the phase angle for gating a silicon controlled rectifier (SCR). The SCR is switched closed during the period that gating is applied and connects a fixed parasitic load resistance to the alternator output for a portion of each cycle. The length of that period is a function of the deviation from the set frequency. Thus, a small increase in engine speed caused by a reduction in user load causes more current to flow through the parasitic load resistance and net load on the engine to remain nearly constant.

The speed control is designed to operate in three stages, or channels, each of which is sized to dissipate 6 kilowatts of electrical power. When user load is reduced slightly from its 100 percent value, a slight increase in speed occurs which causes channel A, the first stage, to begin to load the parasitic load resistor (PLR). As user load continues to decrease, the loading of the PLR by channel A continues until the full 6 kilowatts of this first stage is reached, resulting in an alternator speed proportional to an increase of about 14 hertz. If user load continues to decrease, an increase in speed beyond the 14 hertz range of channel A occurs, and channel B turns on, dissipating up to 6 kilowatts of additional load. In the same manner, channel C turns on for the third 14 hertz of overfrequency. Channel C does not normally operate for speed control, since at the point it would turn on, the engine would be delivering more than 12 kilowatts to the PLR, and little, if any to the user load. In effect channel C is standby speed control capacity in the event of failure of channel A or B. There is an incremental increase in engine speed of approximately 25 hertz, or about 2 percent in the range from zero to 100 percent user load demand. Reference 6 explains the design and operation of the speed control in detail.

The speed control package contains the filtering components necessary to suppress voltage and current transients which occur at the moment the SCR is gated. These transients were studied by analog simulation of a circuit which included the alternator, user load, parasitic load, SCR, and the line filter. To verify the accuracy of the analysis, waveforms obtained by this simulation were compared with the corresponding waveforms obtained earlier during subsystem tests. The computer simulation is discussed in more detail in the appendix.

SYMBOLS

C_1	line filter capacitor, 2 μF
f	frequency, Hz
I_L	current to user load
I_T	total alternator current, $I_L + I_0$
$\dot{I}_T$	differential alternator current, dI_T/dt
I_0	total current to speed control, $I_1 + I_2$
I_1	current to parasitic load resistor (PLR)
I_2	current to filter capacitor
L	inductance, H
L_s	alternator inductance, 100 μH
L_1	line filter inductance, 10 μH
L_2	parasitic load filter inductance (simulated), 10 μH to 100 μH
M01, M02	computer comparators
R_L	user load resistor
R_1	parasitic load resistor, 6 Ω
V	voltage, V
V_T	alternator terminal voltage
V_0	internally generated alternator voltage
V_1	source impedance voltage drop
V_{1T}	transient source impedance voltage drop
V_2	line filter L_1 voltage drop
V_3	line filter C_1 voltage drop
V_3'	parasitic load voltage drop
V_4	parasitic load filter L_2 voltage drop

V_5 parasitic load resistor R_1 voltage drop

ω frequency, rad/sec

RESULTS AND DISCUSSION

A simplified representation of one phase of the alternator, user load, and speed control circuit is shown in figure 1. L_s and R_L represent the alternator inductance and user load, respectively; and L_1, C_1, and R_1 are the filters and PLR resistance in one channel of one phase of the speed control. Inductor L_2 was added into the analog computer simulation to evaluate its effect on the voltage and current waveforms.

A very detailed study of the steady-state operating performance of the speed control and PLR over a wide range of load power demands was performed (ref. 7). Figure 2(a) shows a set of typical oscilloscope waveforms that were photographed during performance of those tests. These photographs were taken at an alternator output of 10.7 kilowatts and a user load of 8 kilowatts at 1.0 power factor, leaving a net of 2.7 kilowatts to be dissipated in the PLR. At this level of user load, channel A takes the entire excess of alternator power output. Channels B and C of the speed control are full off. Waveforms 1 and 2 are approximately sinusoidal and are typical of the output voltage and current generated by the Brayton alternator. Of particular interest in this report is the photograph of waveform 3 which shows the voltage across the PLR terminals. In that photograph it is seen that voltage switches abruptly to its full value at about a 90° phase angle, then dips momentarily to approximately half the initial level, recovers, then drops in a near-sinusoidal form to zero at 180°. The second half of the cycle then repeats but with polarity reversed. The initial surge occurs at the moment the SCR's are gated. The gating angle is determined by the proportion of alternator power output that is to be dissipated by the PLR in order to maintain constant speed. Smaller user loads cause the SCR to fire earlier, and thus divert power to the PLR for a longer time segment. A 90° firing angle occurs when a PLR channel is operating at one half its capacity or 3 kilowatts. In terms of transient interference this is considered to be the most troublesome condition since switching occurs at the peak voltage value.

In order to evaluate the performance of the filter circuit and to investigate possible design changes which could improve transient suppression, the circuit of figure 1 was simulated on an analog computer. Waveforms obtained by this simulation are reproduced in figure 2(b) beside the corresponding traces obtained in reference 7 during steady-state operational tests with the actual hardware. Both were taken with approximately 3-kilowatt power dissipation in one PLR channel. The almost identical waveshapes of the corresponding traces verify the accuracy of the simulation by the computer. The parasitic load voltages V_3' show a particularly striking similarity. The very pronounced voltage transient immediately following the firing of the SCR's led to the investigation covered in this report.

It was presumed from the outset that this transient is a function of the inductance of the alternator and filter circuits since there was relatively little effect at the alternator voltage output as compared with the extreme distortion observed at the PLR. The validity of this concept was verified on the analog computer, using the simulation of figure 3. Attenuator 3 was varied from a value simulating the inductance of the filter circuit alone (10 μH) through values which simulated a very high source inductance L_s. Through this range, the parasitic load voltage V_3' varied from almost no dip in voltage immediately following SCR turn-on to nearly a 100 percent dip. Setting the attenuator to a value corresponding to an inductance of 110 microhenries reproduced most nearly the waveforms shown in figure 2 and confirmed that the self-inductance of the alternator is equal to 100 microhenries. This test also verified that a total inductance of 10 microhenries in the filter circuit and the 2-microfarad capacitor C_1 in conjunction with the 100-microhenry alternator inductance effectively reduced the voltage transient at the alternator terminals to an acceptable level.

A further investigation was performed to evaluate the waveform improvement that may be expected at the alternator terminals by an added inductance L_2 inserted in series with the PLR. Very little improvement was observed for values of L_2 below 100 microhenries, as expected. The time constant for a 100-microhenry inductance, in series with the 6-ohm PLR is less than 17 microseconds, very small compared to the half-cycle period of 415 microseconds for the alternator voltage.

An inductance of 100 microhenries appears to be the minimum inductance value that may be installed for any noticeable improvement. However, since nine of these would be required-one for each channel in three phases of the PLR-and each must be heavy enough to carry the maximum PLR phase current, it is evident that the small improvement in performance can be obtained only at disproportionate increases in space and weight requirements.

A final test was performed to observe the effect on the voltage transients by eliminating the speed control filter components L_1 and C_1 and PLR filter L_2 entirely. For this test, the simulation of figure 3 was modified to the configuration shown in figure 4. It was expected that switching of the PLR current without the filters would cause switching transients to appear on the alternator terminal voltage V_T. The simulation of figure 4 verified this prediction as shown in the waveforms of figure 5. Comparison of the unfiltered with the filtered circuit waveforms shows a serious spike in the alternator terminal voltage, also reflected in the line current at the time of switching. This test further verified that the existing filters are necessary for satisfactory performance of the speed control.

CONCLUSION

Alternator output voltage transients caused by speed control parasitic load switching were investigated by comparing results of an analog simulation with experimental data. From this comparison it was shown that the voltage transients correlate very closely with the simulated value of the source inductance. It was, therefore, concluded the voltage transients seen across the parasitic load resistor (PLR) were the result of the combined effects of the phase-angle switching technique used and the alternator inductance.

By comparing traces of line voltage V_T with and without the line filter, it can be seen that the filter was successful in suppressing the line voltage transients to acceptable levels, thereby reducing possible sources of conductive and radiative line interference.

It was also demonstrated that additional filtering at the PLR terminals was not required and that, if installed, would provide only marginal improvement.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, February 23, 1971,
120-27.

APPENDIX - DISCUSSION OF ANALOG COMPUTER SIMULATION

The schematic of the analog simulation is shown in figure 3. In this figure, amplifiers 00, 01, and 02 with attenuating potentiometers 1 and 2 comprise the basic oscillator for the circuit. The operating frequency of 1200 hertz is determined by the setting of the attenuators. For this case

$$\omega = 2\pi f$$

$$= (6.280)(1200) = 7550 \text{ rad/sec} \tag{A1}$$

To make the computer operate in real time was not practical; therefore, equation (A1) was time scaled down by a factor of 10^5 to give an attenuator setting of 0.0755.

The total speed control current I_0 is obtained from amplifier 11 which integrates the voltage drops across the source impedance L_s and filter inductor L_1. These voltage drops are designated V_1 and V_2. For the analog simulation, the load current I_L was assumed to be at its steady-state condition so that it generated no transient voltage across the source impedance L_s; also, the steady-state voltage drop in L_s due to I_L was neglected. Voltages V_1 and V_2 can then be obtained by subtraction of V_3, the voltage across the filter capacitor C_1 from the oscillator voltage V_0. This is accomplished in amplifier 03. The integration rate, set by potentiometer 3, is obtained from the following equation:

$$V = L \frac{di}{dt} \tag{A2}$$

or

$$I = \frac{1}{L} \int V\, dt$$

Substituting the correct variables and assuming I_L to be at steady state give:

$$I_0 = \frac{1}{L_s + L_1} \int (V_1 + V_2) dt \tag{A3}$$

and the attenuator setting, after applying the time scale factor, is

$$\frac{1}{L_s + L_1} \times 10^{-5} = \frac{10^6}{(100 + 10)(10^5)} = \frac{1}{11} = 0.091$$

The voltage across the filter capacitor V_3 is obtained by integration of I_2 in amplifier 20, where I_2 is the difference of I_1 from I_0 (amplifier 12). The setting for attenuator 6 is obtained from the following equation:

$$V = \frac{1}{C} \int i \, dt \tag{A4}$$

Assuming a value of 2 microfarads for C_1 and applying the time scale factor, 10^{-5} result in the attenuator setting becoming

$$\frac{1}{C_1} = \frac{10^6}{2 \times 10^5} = 5$$

which is accomplished by setting attenuator 6 to a value of 0.50 and following with an amplifier with a gain of 10.

The PLR and its filter L_2 are simulated with amplifiers 23, 21, and 22. The switching of the SCR's is simulated by comparators M01 and M02. The firing angle is controlled by using potentiometer 9, while potentiometer 8 controls the "on" time. It is set to hold the comparator on until V_3 falls to near zero. By varying attenuators 8 and 9, while maintaining a difference of 0.005 for stability, the firing angle could be varied from 0° to 90°. Control beyond 90° would have unnecessarily complicated the simulation.

Amplifiers 07, 08, and 09 are used to obtain dI/dt, required to obtain the line voltage waveform V_T. Since V_1 is the voltage drop across the source impedance, the terminal voltage V_T is equal to $V_0 - V_1$. The impedance drop is obtained from equation (A2)

$$V_1 = L_s \frac{dI}{dt}$$

and the attenuator setting, corrected by the time scale factor, is

$$L_s \times 10^5 = \frac{100}{10^6} \times 10^5 = 10$$

which is obtained by an attenuator setting of 0. 100 and an amplifier gain of 100.

Amplifier 14 generates a user load current, and amplifier 15 sums this current with I_0 to produce the total alternator current I_T.

The rest of the amplifiers are used as inverting multipliers.

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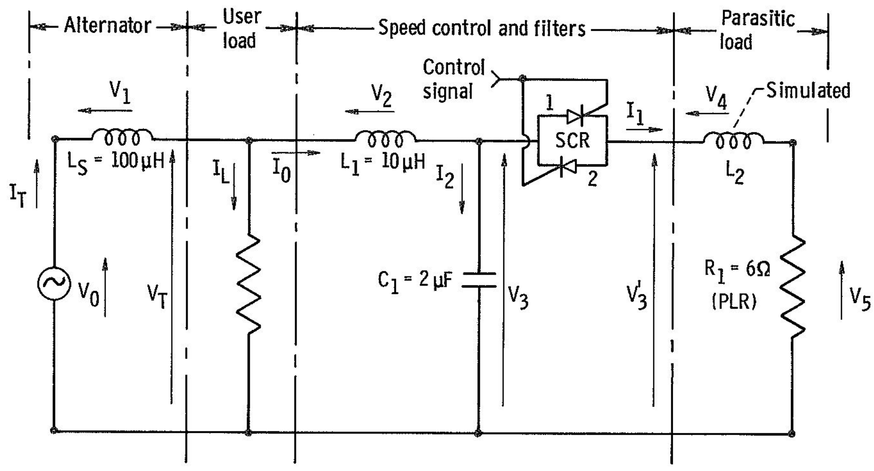
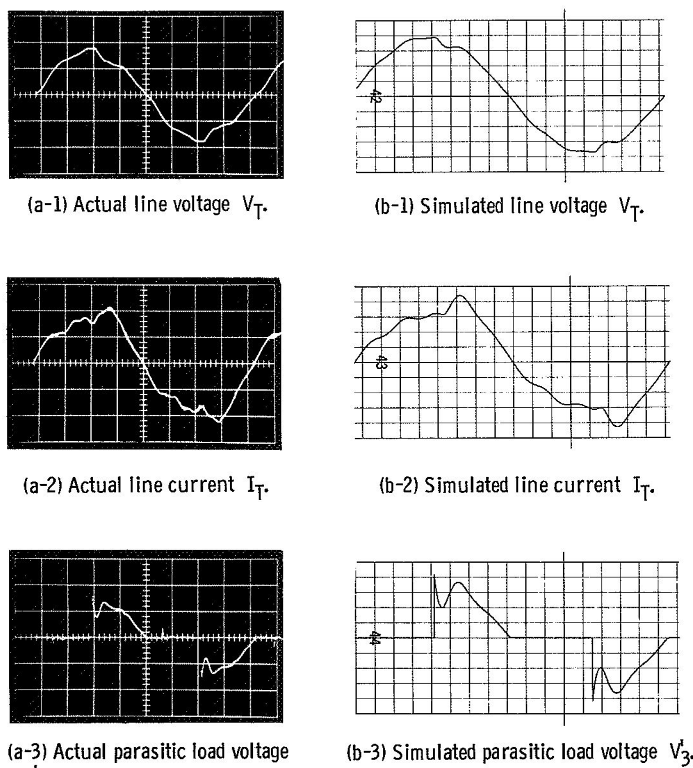


Figure 1. - Simplified diagram of one phase of Brayton cycle alternator and speed control.



(a-1) Actual line voltage V_T.

(b-1) Simulated line voltage V_T.

(a-2) Actual line current I_T.

(b-2) Simulated line current I_T.

(a-3) Actual parasitic load voltage V_3'.

(b-3) Simulated parasitic load voltage V_3'.

(a) During steady-state tests.

(b) Analog computer simulation.

Figure 2. - Comparison of voltage and current waveforms at unity power factor. Alternator output, 10.7 kilowatts; user load, 8 kilowatts.

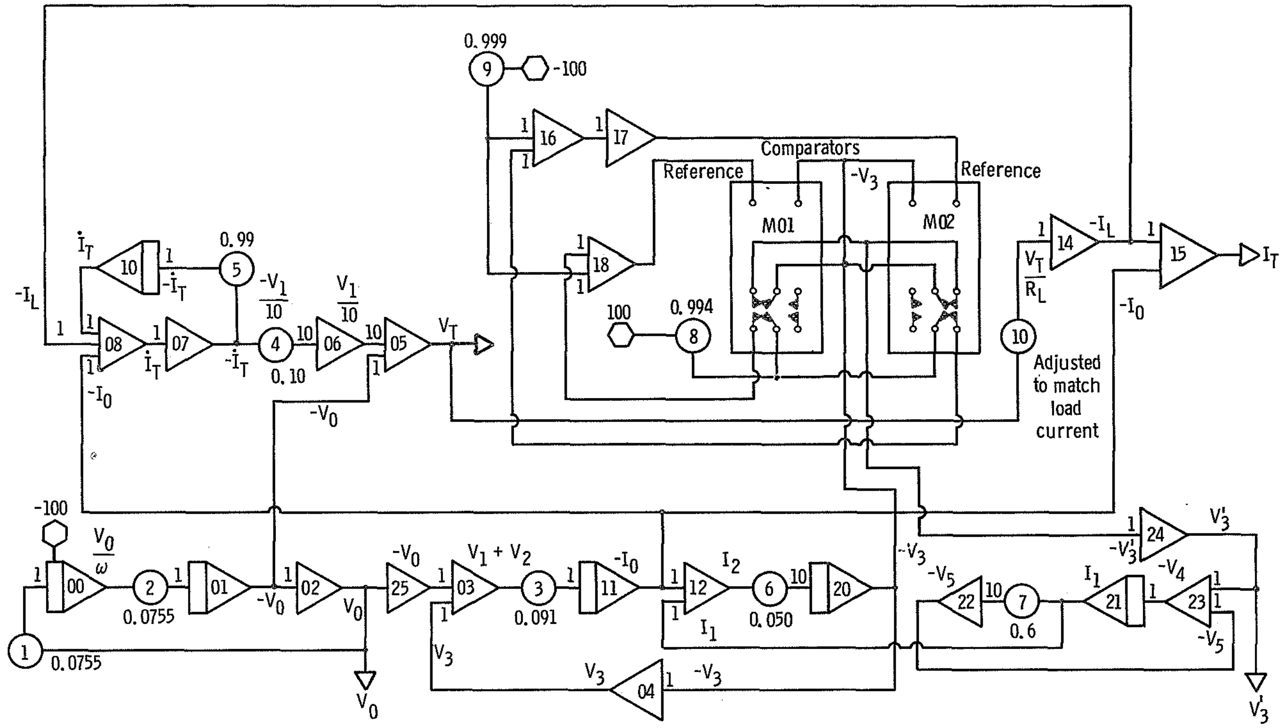


Figure 3. - Analog computer simulation of Brayton cycle alternator and speed control.

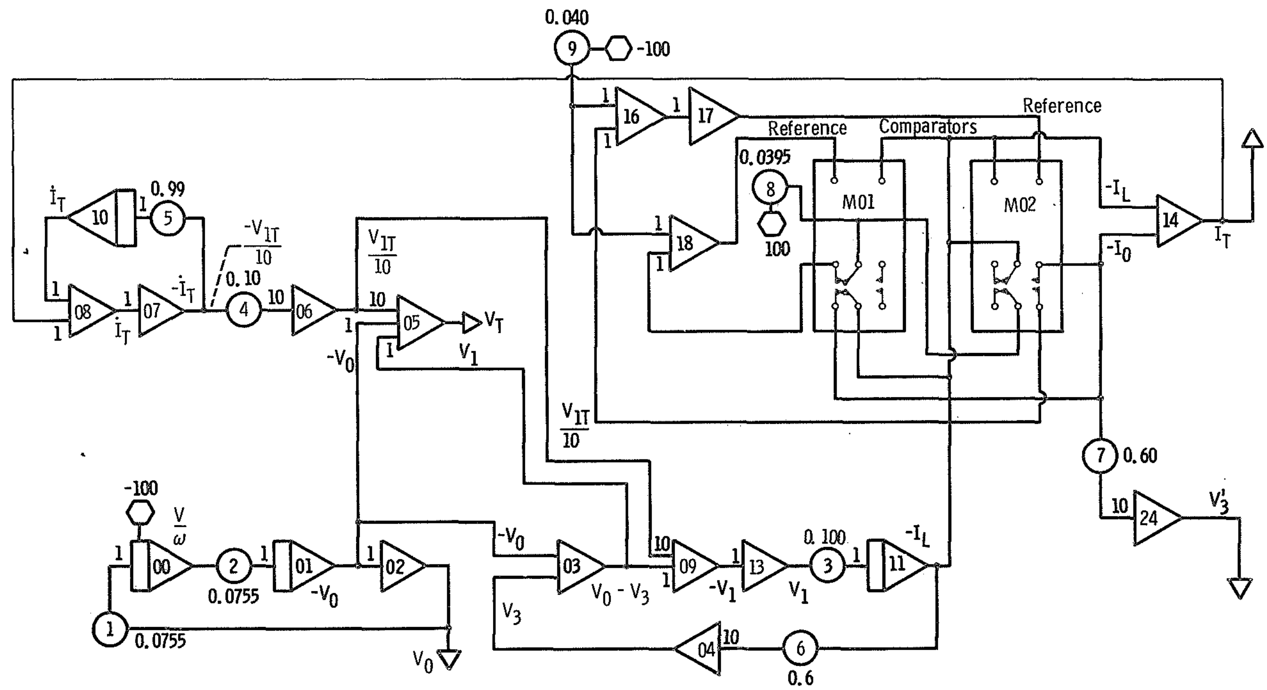
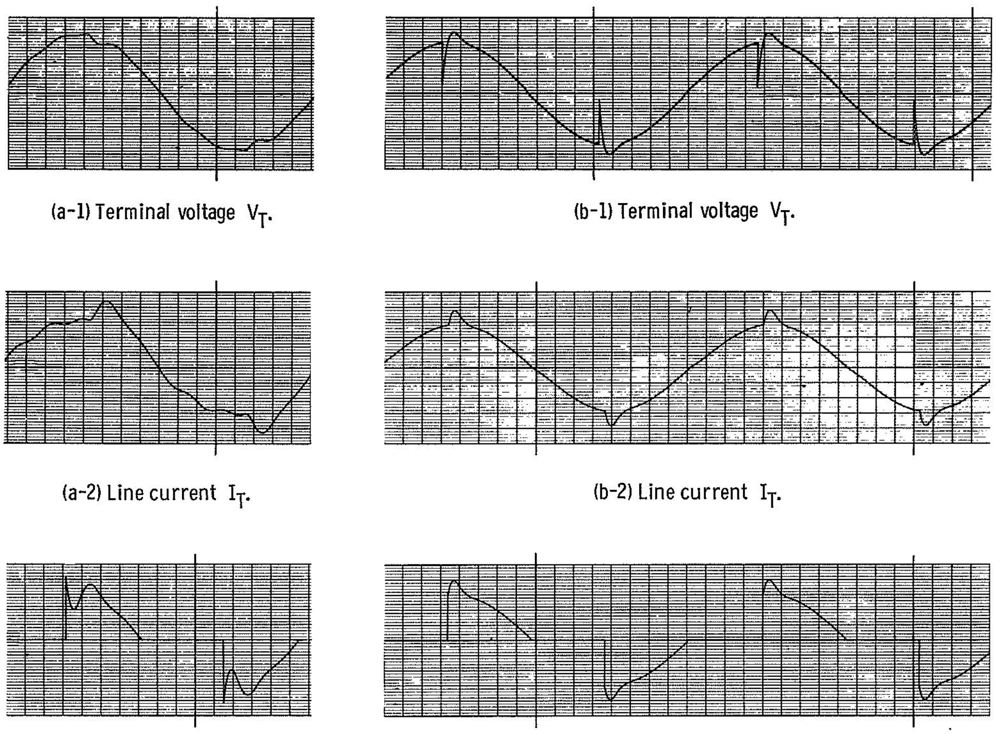


Figure 4. - Analog computer simulation of figure 1 omitting line and parasitic load resistor filters L_1, L_2, and C_1.



(a-1) Terminal voltage V_T.

(b-1) Terminal voltage V_T.

(a-2) Line current I_T.

(b-2) Line current I_T.

(a-3) Parasitic load voltage V_3'.

(b-3) Parasitic load voltage V_3'.

(a) With normal speed control LC filters.

(b) With filters omitted.

Figure 5. - Voltage and current waveforms obtained by analog simulation at unity power factor. Alternator output, 10.7 kilowatts; user load, 8 kilowatts.

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