REPORT NO. P71-59
CONTRACT NO. NAS8-26380

STUDY TO DEVELOP PROCESS CONTROLS FOR LINE CERTIFICATION ON HYBRID MICROCIRCUITS

FRANK KEISTER, Program Manager
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Microelectronic Technology Department
Equipment Engineering Divisions
Culver City, California 90230

MARCH 3, 1971

FINAL REPORT

Prepared for
GEORGE C. MARSHALL SPACE FLIGHT CENTER
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PREFACE

Objective

The objective of this study was to develop documentation for a program of Line Certification based on process controls for producing thin film and thick film hybrid microcircuits for NASA use.

Scope

Flow charts were developed listing the basic process steps used to produce typical hybrid microcircuits. Based on these flow charts, key process steps were selected at which a microcircuit manufacturer normally makes a measurement, test, or inspection to maintain process control over his hybrid microcircuit line in order to achieve a homogeneous end product with good yield and reliability. These key process steps are those which should be certified and demonstrated to a NASA Certification Team as reasonable assurance to NASA that the manufacturer's line is capable of producing acceptable and consistent hybrid microcircuits. For each of the key process steps, the manufacturer is asked to identify certain factors, such as: type, method, material, controls, processing steps, equipment, test methods, documentation, inspection, and quality assurance criteria.

The ten key process steps selected were:

1. Design and Layout
2. Masks and Screens
3. Parts and Materials Control
4. Substrate Characterization
5. Film Patterning
6. Substrate Sizing
7. Trimming
8. Parts Mounting
9. Interconnect Bonding
10. Package Sealing

The particular process steps and specific examples used in this Line Certification document represent those methods, materials, controls, etc.

currently being used in the Microelectronic Technology Department, Hughes Aircraft Company, to produce thick film and thin film hybrid microcircuits for military applications.

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I. GENERAL REQUIREMENTS FOR LINE CERTIFICATION OF HYBRID MICROCIRCUITS

1.0 IDENTIFICATION OF HYBRID MICROCIRCUIT TYPE

Using Table 1, the manufacturer shall identify each type of hybrid microcircuit in which he has sufficient production experience to warrant a request for Line Certification. Table 1 is not extensive enough to cover all possible hybrid microcircuit types, materials, mounting and bonding processes, etc. Therefore, the manufacturer should identify, by a written statement, his particular hybrid microcircuit type if it is not included in Table 1. For example, if the manufacturer deposits thin film and thick film capacitors (rather than using capacitor chips) this should be indicated by a separate statement.

2.0 PROCESS FLOW CHARTS

The manufacturer shall furnish to the NASA Certification Team a process flow chart (or charts) showing the sequence of operations used to fabricate the type (or types) or hybrid microcircuit to be certified. The manufacturer shall indicate on this flow chart those points at which a visual and/or quality control inspection takes place. The flow chart (or charts) should cover all pertinent operations from the initial substrate preparation through sealing, testing, and delivery of end item. In addition, if applicable, the manufacturer shall furnish a flow chart diagramming the design, layout, and mask making steps which result in the final artwork, schematics, drawings, screens, reduced film or glass masks, and deposition masks. The following flow charts in Appendix A are typical examples of hybrid microcircuit process flow charts:

Exhibit 1. Typical sequence of events for making a hybrid design and layout resulting in a set of manufacturing engineering drawings and the required 1:1 working masks.

Exhibit 2. Flow chart of typical thick film hybrid microcircuit processing.

Exhibit 3. Flow chart of typical thin film hybrid microcircuit processing.

Exhibit 4. Flow chart of typical hybrid microcircuit assembly.

Table 1. Hybrid microcircuit groups for which the manufacturer desires certification

Code	Type of Hybrid Microcircuit	Code	Primary Substrate Material	Code	Primary Resistor-Conductor Materials	Code	Chip Configuration and Mounting Method	Code	Chip Interconnect Bonding Material and Form	Code	Chip Interconnect Bonding Process	Code	Primary Package Type
A.	Thick Film	1.	Glazed alumina		Resistor		Chip Configuration		Material			A.	Ceramic flatpack
B.	Thin Film	2.	Unglazed alumina	A.	Nickel-chromium	1.	Beam lead	A.	Gold	1.	TC wedge	B.	Metal flatpack
C.	Multichip	3.	Glass	B.	Tantalum	2.	Flip chip	B.	Aluminum	2.	TC ball	C.	Flatpack
D.	Thick/thin combination	4.	7059 Glass	C.	Tantalum nitride	3.	Regular face-up chip	C.	Copper	3.	Ultrasonic	D.	TO-3
E.	Other (specify)	5.	Beryllia	D.	Chromium	4.	Spider	D.	Nickel	4.	Solder	E.	TO-5
		6.	Quartz	E.	Rhenium	5.	LID	E.	Gold plated Kovar	5.	Solder reflow	F.	TO-8
		7.	Silicon	F.	Tin oxide	6.	Ceramic carrier	F.	Solder	6.	Parallel gap weld	G.	Dual in-line
		8.	Sapphire	G.	Thin film cermet	7.	Molytab or Kovartab	G.	Tinned copper	7.	Parallel gap solder	H.	Plastic package
		9.	Steatite	H.	Gold-iridium	8.	Other (specify)	H.	Silver	8.	Laser weld	I.	Plastic conformal coating
		10.	Barium Titanate	I.	Thallium oxide		Chip-To-Substrate Mounting	I.	Other (specify)	9.	EB weld	J.	Custom
		11.	Plastic	J.	Platinum-base	9.	Au-Si preform		Form	10.	Wobble bond	K.	Other (specify)
		12.	Other (specify)	K.	Ruthenium oxide	10.	Au-Ge preform	T.	Wire	11.	Compliant bond		
				L.	Palladium oxide-silver	11.	Au-Sn preform	U.	Ribbon	12.	Conductive adhesive		
				M.	Palladium-silver	12.	Sn-Pb alloy	V.	Beam lead	13.	Solder paste		
				N.	Proprietary	13.	Sn-Ag alloy	W.	Bumps	14.	Weld		
				O.	Other (specify)	14.	Special solder alloy	X.	Deposited film	15.	Other (specify)		
					Conductor	15.	Conductive adhesive	Y.	Special plastic carrier				
				P.	Aluminum	16.	Direct scrubbing	Z.	Other (specify)				
				Q.	Gold	17.	Non-conductive adhesive						
				R.	Platinum-gold	18.	Bumps on chip						
				S.	Palladium-gold	19.	Bumps on substrate						
				T.	Palladium-silver	20.	Beams on chip						
				U.	Silver	21.	Beams on special carrier						
				V.	Copper	22.	Plastic						
				W.	Solder coated thick film	23.	Other (specify)						
				X.	Moly-manganese								
				Y.	Proprietary								
				Z.	Other (specify)								

Example: [B-2-(A, Q)-(3, 15)-(B, T)-3-A] is a thin film microcircuit on an unglazed alumina substrate with nichrome resistors and gold conductors. Regular face-up chips are mounted on the substrate using a conductive adhesive. The chips are interconnected with aluminum wire by ultrasonic bonding. The microcircuit is packaged in a ceramic flatpack.

3.0 FAILURE ANALYSIS CAPABILITY

The manufacturer shall demonstrate his capability in failure analysis of hybrid microcircuits and identify the equipment and techniques normally used in his failure analysis work. This demonstration may be by means of failure analysis reports, photomicrographs, equipment demonstrations, or other means.

Example: Failure analysis ordinarily starts with electrical trouble-shooting and a magnified visual examination to isolate the failed part. The initial evaluation will ordinarily determine the failure mode and provide a basis for further analysis. The following methods are used to determine the actual cause of failure and may require disassembly and dissection of the microcircuit.

a. Infrared radiometric microscopy
b. Fluoroscopic analysis
c. Scanning electron microscopy
d. Microprobe analysis
e. Radiographic analysis
f. Photographic record of all anomalies observed

The following techniques and equipment are also available to determine more precisely the exact physical processes that took place.

a. Metallographic sample preparation and analysis
b. Chemical analysis
c. X-ray diffraction analysis
d. Absorption/transmission spectrophotometry

One of the most important aspects of failure analysis is the feedback of the data and the corrective action cycle. The manufacturer should show evidence that his failure analysis capability includes an "evaluation-feedback-corrective action" closed loop.

4.0 ELECTRICAL TESTING CAPABILITY

4.1 Electrical Test Equipment

The manufacturer shall furnish evidence of a capability for electrically testing the hybrid microcircuit types to be certified. As a minimum

requirement, this capability should include a test area with electrical test equipment sufficient for monitoring parameters such as resistance, capacitance, inductance, voltage, current, frequency, etc. The manufacturer shall also indicate whether his capability includes equipment for the electrical testing of active and passive chip components, such as integrated circuit chips, transistor chips, capacitor chips, etc. and whether or not this test equipment is automatic or computer-controlled. For example:

Hybrid microcircuit electrical test area complete with

a. General purpose, low noise power supplies
b. Precision, low noise power supplies
c. General purpose oscilloscopes
d. High frequency response oscilloscopes
e. Oscilloscope camera
f. Waveform generator
g. General purpose pulse generators
h. Very fast pulse generators
i. Counters and timers
j. Digital voltmeters
k. Digital ohmmeters
l. Precision digital volt-ohm meters
m. Automatic capacitance bridge
n. High frequency reactance meter
o. Resistor noise analyzer
p. Digital IC tester
q. Linear IC tester
r. Transistor curve tracers
s. Volt-ohm-milliammeters
t. Microwave network analyzer
u. DC vacuum tube voltmeters
v. Multiple microprobe stations for chip testing
w. Miscellaneous special test fixtures

4.2 Equipment Calibration

The manufacturer shall furnish evidence that the electrical test equipment used to test hybrid microcircuits undergoes a regularly-scheduled calibration to insure satisfactory operation and accuracy. For example:

a. Curve tracers calibrated every 6 months by Secondary Standards Lab.

b. Oscilloscopes calibrated every 84 working days by Secondary Standards Lab..

c. Digital voltmeters calibrated every 105 working days by Secondary Standards Lab.

d. Volt-ohm-milliammeters calibrated yearly by Secondary Standards Lab.

e. Potentiometer bridges calibrated every 147 working days by Primary Standards Lab.

4.3 Flow Charts

The manufacturer shall indicate on the applicable flow charts (see Exhibits 2, 3, 4, and 5 in Appendix A) at what points electrical testing is done in the hybrid microcircuit fabrication operation. For example:

a. Thick film resistors electrically tested before and during trimming.

b. Thin film resistors electrically tested before and during trimming.

c. Hybrids tested before and after sealing.

5.0 ENVIRONMENTAL AND ACCEPTANCE TESTING CAPABILITY

5.1 Environmental Test Equipment

The manufacturer shall furnish evidence of a capability for environmentally testing the hybrid microcircuit types to be certified. For example:

Environmental test capability consists of the following:

a. Storage ovens capable of at least +150°C

b. Cold chambers capable of at least -65°C

c. Acceleration equipment

d. Vibration equipment

e. Altitude test chamber

f. Salt spray chamber

g. Mechanical shock equipment

5.2 Acceptance Testing

The manufacturer shall indicate the types of environmental, mechanical, and electrical tests normally given to hybrid microcircuits as part of his pre-seal or post-seal acceptance testing. This should include any special chip burn-in tests, if applicable. This may be done in flow chart format (see Exhibit 5 in Appendix A) or in tabular format. The specific acceptance tests and test parameters will depend on the particular program requirements.

5.3 Equipment Calibration

The manufacturer shall furnish evidence that the environmental and mechanical test equipment used to test hybrids undergoes regularly-scheduled calibration to insure satisfactory operation and accuracy. Calibration should especially include those equipment items used in the assembly, measurement, and control of the hybrid microcircuits being fabricated, including special tools, gauges, and control meters. For example:

a. Ovens calibrated every 3 months by Secondary Standards Lab.

b. Thermometers calibrated yearly by Primary Standards Lab.

c. Humidity chambers calibrated yearly by Secondary Standards Lab.

d. Pin recorders calibrated every 4 months by Secondary Standards Lab.

e. Accelerometers calibrated every 6 months by Secondary Standards Lab.

f. Centrifuge counters calibrated every 84 days by Secondary Standards Lab.

g. Temperature recorders calibrated every 3 months by Secondary Standards Lab.

h. Manometer calibrated every 6 months by Primary Standards Lab.

6.0 DEIONIZED WATER CONTROLS

The manufacturer shall identify the controls used to maintain the purity of the deionized water which he uses in hybrid microcircuit processing. If

deionized water is not used, the manufacturer shall indicate the type of water used. These controls, as a minimum, shall consist of the following.

a. Water resistivity (e.g., water resistivity must be greater than or equal to 12 megohms as determined by a Beckman Solu Resistance Bridge, Model RD-146-Y1; etc.)

b. Water solids (e.g., a particle count is periodically taken using a 0.45 micron membrane filter, examination of the filter is done under 40X magnification with an accuracy of ±10 percent for 0.5 micron particles; etc.)

c. Other controls, if applicable (e.g., ultraviolet sterilizer; total electrolytes count; no other controls applicable, etc.)

7.0 WORK AREA CONTROLS

The manufacturer shall identify the requirements and controls used for the operation and maintenance of the hybrid microcircuit work areas.

7.1 Personnel

a. Protective garments (e.g., personnel entering the microcircuit work area shall wear nylon or Dacron smocks of approximately knee length; personnel handling microcircuits or microcircuit materials shall wear gloves or finger cots, etc.)

b. Smoking, eating, and drinking (e.g., smoking, eating, and drinking is prohibited in all microcircuit fabrication, inspection, and test areas; etc.)

7.2 Equipment

a. Equipment (e.g., compressed air hoses shall have adequate filters; all vacuum pumps or other devices that produce hydrocarbons, aerosols, or synthetic lubricants shall be vented outside the area or be equipped with adequate exhaust filters; only closed top waste containers with disposable plastic bags shall be permitted within microelectronic production areas; etc.)

7.3 Work Area

a. Work area (e.g., gelatin or fiber type floormats are provided at each entrance to the microcircuit production area; laminar flow benches within the microcircuit production area shall have a minimum airflow rate of 100 linear feet per minute; HEP A absolute filters 99.97 percent effective in removing airborne particles 0.3 microns in size or larger, and prefilters capable of removing gross amounts of larger airborne particles; an anteroom is provided to prevent the flow of contaminated air from the out-of-doors into the production areas; all floor areas are dry mopped daily, wet mopped weekly, and vacuumed every two weeks; all air ducts, inlets and exhausts are vacuum wiped monthly; etc.)

7.4 Environmental Controls, If Any

a. Temperature (e.g., no specific room temperature requirements or controls other than regular thermostats; room temperature continually monitored in all microcircuit production areas; assembly area temperature 75° ± 2°F, thick film area temperature 71° ± 2°F, thin film area temperature 76° ±2°F; etc.)

b. Relative humidity (e.g., no specific relative humidity requirements or controls; relative humidity is 45 percent ± 5 percent in microcircuit fabrication areas; etc.)

c. Particle count, if applicable (e.g., no particle count requirement, etc.)

d. Class of clean room, if applicable (e.g., controlled area used rather than clean room, etc.)

8.0 PACKAGES OR PACKAGING METHODS

The manufacturer shall identify the package types or packaging methods which he uses to enclose or protect the hybrid microcircuits to be certified. He shall also indicate the controls used to assure the integrity of these packages or packaging methods.

8.1 Package Type, Material, and Size

a. Package type (e.g., flatpack, TO-8 header, dual in-line, etc.)
b. Package material (e.g., alumina ceramic, Kovar, gold plated Kovar, etc.)
c. Lid material (e.g., tin plated iron-nickel-cobalt alloy, nickel, Kovar, etc.)
d. Package sizes (e.g., 1 inch x 1 inch 30-lead, 1 inch x 2 inches 74-lead; 12-lead and 16-lead TO-8 sizes; etc.)

8.2 Package Controls

a. Lead integrity (e.g., leads shall be capable of withstanding a pull of 1.0 pound for a minimum duration of 30 seconds when tested per MIL-STD-883, Method 2004, Condition A, etc.).
b. Lead fatigue (e.g., leads shall be capable of meeting requirements for resistance to metal fatigue when subjected to a bending force of 3 ± 0.3 oz. for three 90 ± 5 degree arcs per MIL-STD-883, Method 2004, Condition B2, etc.)
c. Lead peel strength (e.g., each lead shall be capable of withstanding a force of at least 8.0 oz. directed upwards at right angles to the lead plane, etc.)
d. Lead solderability (e.g., lead surfaces shall be wet by solder without degradation of the package when immersed for 5 ± 0.5 second in a solder bath at 230° ±5°C per MIL-STD-883, Method 2003, etc.).
e. Lead finish (e.g., lead finish shall be gold plate per MIL-G-45204, Type I, Class 1, Grade A, 0.00005 inch minimum thickness, etc.)
f. Ceramic or metal base (e.g., aluminum oxide, 94 percent purity minimum with a flexural strength of 35,000 psi, a minimum bulk specific gravity of 3.4 grams per cc, maximum surface roughness of 63 microinch per ASA publication B46.1-1962, etc.)
g. Metalization if any (e.g., gold over nickel, nickel plate per QQ-N-290, Class 2, 0.0003 inch thick minimum, gold plate per MIL-G-45204, Type I, Class 1, Grade A, 0.00005 inch thick minimum, etc.)

h. Workmanship (e.g., ceramic shall be free from cracks, fissures, bubbles, pores, chips, etc.; metalization and plating shall be free of excessively ragged edges, corrosion, lifting, pulling, cracks, scratches, blisters, etc.; leads shall be free of burrs greater than 0.0015 inch in any direction and free of any defects as specified in MIL-STD-883, Method 2009 when viewed under 10X magnification, etc.)

i. Rupture strength (e.g., the package shall be capable of withstanding 3 atmospheres pressure differential when sealed on a resilient surface, etc.)

j. Hermeticity (e.g., when tested per MIL-STD-883, Method 1014, Condition A, the measured leakage rate shall be less than 1×10^{-8} atm. cc/sec., etc.)

k. Environmental (e.g., packages shall withstand thermal shock per MIL-STD-883, Method 1011, Condition C; packages shall withstand vibration fatigue per MIL-STD-883, Method 2005, Condition A; packages shall withstand salt atmosphere per MIL-STD-883, Method 1009, Condition A, etc.)

9.0 PRODUCT ASSURANCE

The manufacturer shall show evidence of a product assurance program similar to the requirements of MIL-M-38510, Appendix A.

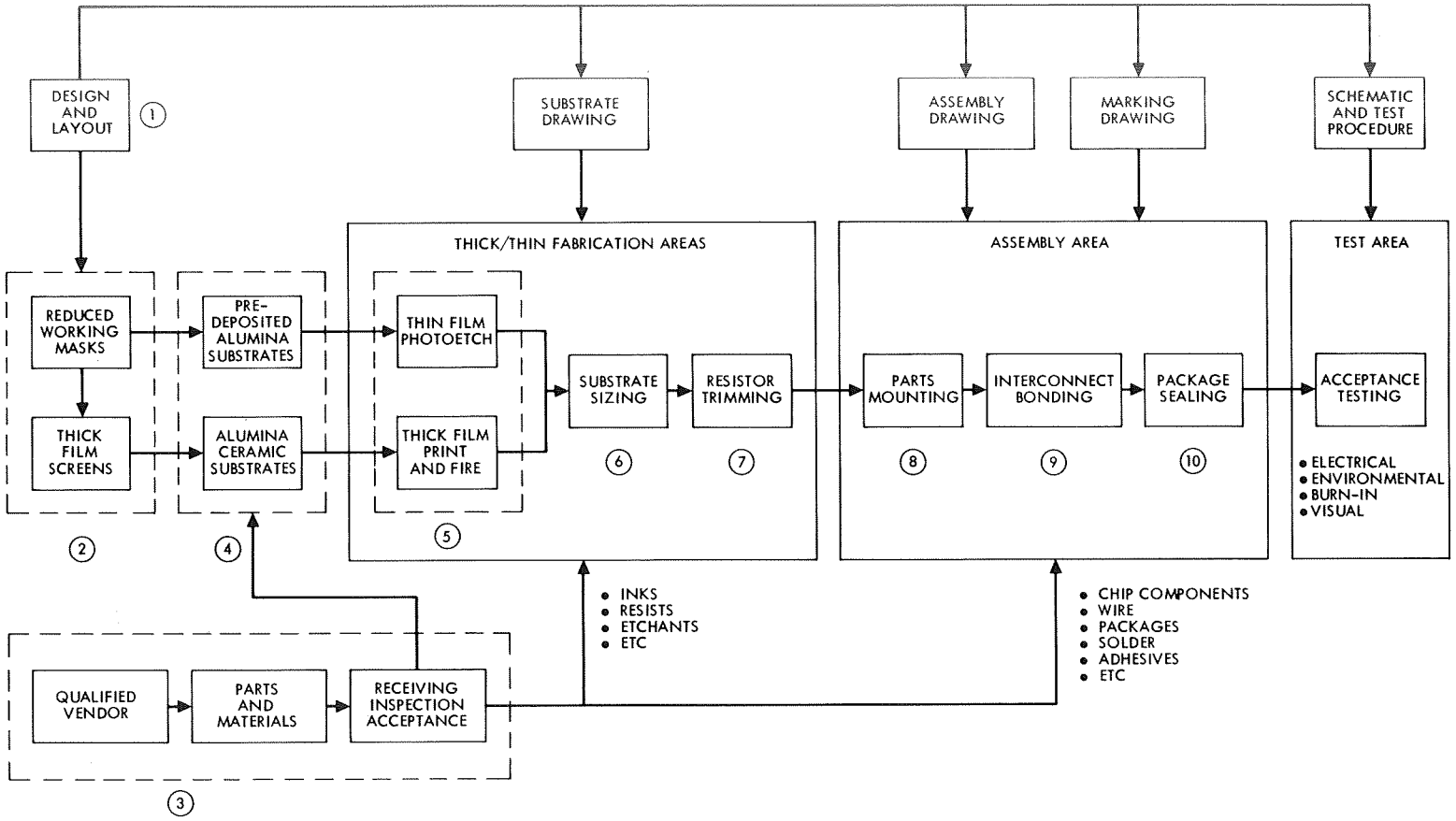
II. CERTIFICATION OF KEY PROCESS STEPS

This section of the Line Certification document includes the key process steps required to produce typical thin film and thick film hybrid microcircuits. These ten key process steps start with design and layout and continue through package sealing:

1.0 Design and Layout
2.0 Masks and Screens
3.0 Parts and Materials Control
4.0 Substrate Characterization
5.0 Film Patterning
6.0 Substrate Sizing
7.0 Trimming
8.0 Parts Mounting
9.0 Interconnect Bonding
10.0 Package Sealing

Figure 1 is a flow diagram showing how these ten key process steps are interrelated in a typical flow sequence. The last seven process steps (i.e., substrate characterization through package sealing) are intimately associated with the actual fabrication processes. For each of the key process steps, the manufacturer is asked to identify his materials, processing methods, controls, documentation, and inspection and quality assurance criteria. The manufacturer must also demonstrate to the NASA Certification Team his processes, controls, equipment and test methods, where applicable. This is done in order to assure NASA that a particular hybrid microcircuit line is capable of fabricating a consistent and highly reliable product.

In no instance is the manufacturer required to furnish documentation which the manufacturer considers proprietary. If necessary, the existence of proprietary documents shall be established by a listing of those proprietary documents necessary to the hybrid microcircuit operation.



NOTE: CIRCLED NUMBERS DESIGNATE KEY PROCESS STEPS FOR CERTIFICATION.

1. DESIGN AND LAYOUT
2. MASKS AND SCREENS
3. PARTS AND MATERIALS CONTROL
4. SUBSTRATE CHARACTERIZATION
5. FILM PATTERNING
6. SUBSTRATE SIZING
7. TRIMMING
8. PARTS MOUNTING
9. INTERCONNECT BONDING
10. PACKAGE SEALING

Figure 1. Typical flow diagram showing the overall interrelationships between the various hybrid microcircuit key process steps which require certification.

1.0 DESIGN AND LAYOUT

1.1 Scope

This process step involves the schematics, drawings, Rubyliths, artwork, layouts, etc. necessary for the design and layout of a hybrid microcircuit. Regardless of the different types of drawings, their format, or the manner in which they are prepared, these drawings, together with the appropriate specification call-outs and parts lists, must be complete enough to permit the fabrication of a hybrid microcircuit. This process step does not include the preparation of the reduced working masks (e.g., film negatives, etc.), deposition masks, or thick film screens, as they are covered in Section 2.0 of this Line Certification document.

References: The flow chart in Exhibit 1 (Appendix A) illustrates a typical sequence of events resulting in a set of manufacturing engineering drawings for the fabrication of either a thick film or thin film hybrid microcircuit. For prototypes or engineering models, the substrate, assembly, and artwork drawings are usually eliminated. In these cases, the final layout serves as the all-purpose drawing. The manufacturer should furnish a similar flow chart showing his design and layout procedure.

1.2 Identification of Drawing Types

The manufacturer shall identify the different types of drawings, artwork, layouts, etc. which he uses for the fabrication of production-type hybrid microcircuits. For example:

a. Artwork drawings. The artwork drawing is an undimensioned drawing which duplicates the Rubylith artwork. Working masks are prepared by photographic reduction of the artwork drawings.

b. Substrate drawing. The substrate drawing shows the complete resistor-conductor network as it would appear after photoetching or after screening and firing.

c. Assembly drawing. The assembly drawing shows the assembled substrate inside the package enclosure with all chips, wire bonds, etc., shown in their proper positions.

d. Marking drawing. The marking drawing shows the package outline with the correct callouts to be stencilled on the outside of the package cover.

e. Schematic diagram. The schematic diagram shows the electrical circuit in symbolic format with all components identified as to type, value, tolerance, etc.

1.3 Identification of Method Used to Prepare Master Drawings

The manufacturer shall identify the method or methods used to prepare the master drawings. Master drawings are those drawings or artwork (e.g., Rubyliths, taped masters, etc.) ordinarily done at an enlarged scale from which the final reduced working masks are prepared.

1.3.1 Method. (e.g., Rubyliths cut manually on 48-inch coordinatograph; master artwork prepared by automated drafting machines using computer control; etc.)

1.3.2 Scale. (e.g., Rubyliths normally prepared at a 20:1 scale, etc.)

1.4 Identification of Resistor-Capacitor-Conductor Design Requirements

The manufacturer shall identify his capabilities in the fabrication of hybrid microcircuits by listing his passive device design requirements for each basic type of hybrid microcircuit to be certified (e.g., thick film, thin film, multichip, etc.)

1.4.1 Resistors.

a. Type (e.g., thick film; thin film; chip; etc.)

b. Resistivity (e.g., 225 ohms/square for thin film resistors; ink values used for thick film resistors range from 10 ohms/ square/ mil up to 1 megohm/square/mil; etc.)

c. Temperature coefficient of resistance (e.g., ± 100 ppm/°C from -55°C to +150°C for thin film resistors; ± 150 ppm/°C from -65°C to +150°C for ink values from 50Ω/□/mil to 500,000Ω/□/mil; etc.)

d. Size (e.g., thin film resistors widths are nominally 0.005 inch, minimum width = 0.0025 inch; thick film resistor widths are nominally 0.040 inch, minimum width = 0.030 inch; etc.)

e. Power density (e.g., thin film and thick film resistors designed to either 25 or 100 watts/sq. inch on ceramic substrates depending on the resistor tolerance, etc.).

1.4.2 Capacitors.

a. Type (e.g., chip; thin film; thick film; etc.)
b. Capacitance (e.g., chip capacitors range from 10 to 100,000 pf; thick film and thin film printed capacitors are not normally used; etc.).
c. Temperature coefficient of capacitance (e.g., NPO chip capacitors = ± 30 ppm/°C; etc.)
d. Voltage rating (e.g., K1200 chip capacitors rated at 50 vdc; etc.)

1.4.3 Conductors.

a. Type (e.g., thin film; thick film; etc.)
b. Resistivity (e.g., 0.003-0.015 ohms/square; etc.)
c. Minimum line width (e.g., 0.0025 inch for thin films; 0.010 inch for thick films; etc.)

1.5 Documentation

The manufacturer shall furnish evidence of design and layout documentation in regards to design guides, rules, procedures, or the equivalent for:

a. Preparation of drawings and layouts
b. Conductor dimensions and layouts, if applicable
c. Resistor dimensions and layouts, if applicable
d. Capacitor dimensions and layouts, if applicable
e. Chip layouts
f. Interconnections
g. Multilayered designs, if applicable

1.6 Demonstration of Design and Layout Capability

1.6.1 Examples of working drawings. The manufacturer shall furnish examples of each of his different types of working drawings. These examples shall include as a minimum:

a. Schematic diagram
b. Final layout or assembly drawing
c. Parts list and materials call-out, if not included on layout or assembly drawing.
d. Rubylith artwork or the equivalent, if applicable.
e. Artwork, drawing, or master pattern resulting from automated artwork generation or computer-aided design process, if applicable.

1.6.2 Demonstration of layout processes and equipment. The manufacturer shall demonstrate his layout processes and equipment to the NASA Certification Team if done in-house. This demonstration shall primarily consist of cutting an actual Rubylith (or the equivalent) for a thick film or thin film layout showing the methods, tools, and controls used. If automated or computer-aided design processes are used (and if done in-house), the manufacturer shall demonstrate the operation of the applicable equipment (e.g., computer, digitizer, plotter, graphics terminal, etc.) and controls used.

2.0 MASKS AND SCREENS

2.1 Scope

This process step involves the materials, equipment, and controls used by the manufacturer which result in reduced working masks (positives or negatives on film or glass), screens, or "additive" masks for vacuum deposition or sputtering. The manufacturer shall indicate whether the masks and/or screens are prepared in-house or purchased from an outside vendor who specializes in making masks or screens.

References: The flow chart in Exhibit 1 (Appendix A) illustrates a typical sequence of events resulting in a set of screens for thick film printing and in a set of reduced 1:1 working masks for thin film photoetching. If applicable, the manufacturer should indicate his process steps on a similar flow chart.

2.2 Identification of Mask or Screen Type

The manufacturer shall identify the type of mask or screen, its intended usage, and the mask or screen material. For example:

a. Dark field film mask on 0.007-inch thick Cronar for thin film "subtractive" photoetching using negative resist. Fabricated by outside vendor.

b. No. 200 mesh stainless steel screen with "direct" type stencil emulsion for use in printing thick film resistors and conductors with line widths ≥ 0.010 inch. Screen and frame purchased from outside vendor, but emulsion applied and exposed in-house.

2.3 Identification of Mask or Screen Controls

For each mask or screen type to be certified, the manufacturer shall identify the controls used in the preparation of that particular type of mask or screen. If the masks and/or screens are purchased from an outside vendor, indicate any controls or requirements imposed on the vendor.

2.3.1 Environment (e.g., prior to photographic reduction, the artwork shall be stabilized for 8 hours minimum in a controlled environment of 72 ± 3°F at 45-55 percent relative humidity; Gerber photoplotter environment controlled at 69 ± 2°F and 45 ± 5 percent relative humidity; etc.)

2.3.2 Reduction (e.g., all reductions of related multiple patterns shall be generated during the same session, on the same camera, with the same orientation of all related artwork, and from the same lot of film; reduction from 20:1 artwork to be within ±0.0005 inch between designated targets; etc.)

2.3.3 Screen exposure, if applicable (e.g., emulsion-coated screen frame held in vacuum holder of NuArc Flip-Top Platemaker and exposed to mercury light source at a distance of approximately 15-inch, exposure time preset on timer and automatically controlled; etc.)

2.3.4 Film mask exposure, if applicable (e.g., 20:1 reduction done in one step using an 8-1/4-inch lens at a distance of approximately 182-inch from film plane to copy; reduction camera isolated on air pads; etc.)

2.3.5 Touch-up (e.g., touch-up permitted on screens using block-out emulsion; touch-up permitted on film masks using an alcohol-base black opaquing ink; etc.)

2.3.6 Vacuum deposition mask exposure, if applicable (e.g., metal masks coated with dry film resist and exposed from both sides using double-sided exposure equipment, masks spray etched from both sides, etching tolerances for openings in mask are ±0.001-inch; vacuum deposition not normally done through masks; etc.)

2.3.7 Automatic mask generation. If photographic masks are automatically generated, the manufacturer shall identify the equipment and controls used. For example:

a. Equipment (e.g., Gerber Model 532 photoplotter, general-purpose PDP-9 computer, digitizer, card punch and reader, etc.)
b. Control system (e.g., computer and punched card; computer and tape; etc.)
c. X, Y speed (e.g., 1 inch per second, etc.)
d. Accuracy (e.g., ±0.0009 inch over 48 inches x 60 inches table, etc.)
e. Repeatability (e.g., ±500 microinch, etc.)
f. Resolution (e.g., ±300 microinch, etc.)
g. Plotting head (e.g., 24 apertures, etc.)
h. Size of final mask generated (e.g., 1X final mask size on Kodalith Ortho Type 3 Estar Base, etc.)

2.3.8 Step-and-repeat (e.g., thin film photographic masks normally step-and-repeated, step-and-repeating done by outside vendor; thick film screen patterns not normally step-and-repeated; etc.)

2.4 Documentation

The manufacturer shall furnish evidence of documentation regarding the fabrication of masks and screens, if applicable, the controls used, and the inspection requirements.

2.4.1 Inspection requirements (e.g., evaluation of photolithographic film masks documented by Process Instruction PI XXXX; thick film screen stencil inspection documented by Process Instruction PI XXXX; etc.)

2.5 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance requirements related to the following.

2.5.1 Storage (e.g., photographic masters and film working masks shall be stored at 72 ± 5°F and 30-55 percent relative humidity; films are stored flat or on edge where film flatness can be maintained; screens and glass masks stored in such a manner as to avoid scratching or otherwise damaging the emulsion surface; etc.)

2.5.2 Handling and cleanliness (e.g., gloves or equivalent finger covering are worn at all times when handling films; films and film sets individually packaged in clean polyethylene bags or envelopes; films shall be kept free of dust, dirt, fingerprints, and other contamination; etc.)

2.5.3 Identification (e.g., all films are identified with name, drawing number and revision, and pattern type; etc.)

2.5.4 Visual inspection of photographic masks.

a. Workmanship (e.g., all film masters are examined at 55 X magnification for process contaminants within film emulsion which appear as pinholes, scratches or voids, and thin opaque areas appearing as spots; there shall be no scratches, pinholes, or opaque spots > 0.0005 inch; there shall be no more than 5 defects > 0.0002 inch in any resistor areas; etc.)

b. Image definition/edge acuity (e.g., all film masters are examined at 200-250 X magnification for image definition and edge acuity, the photographic image shall appear sharp and distinct, the zone between the fully opaque area to the fully clear area shall be < 0.00005 inch, there shall be no more than 5 rows of emulsion particle scatter beyond the demarcation between film base opacity and the clear film; etc.)

c. Registration (e.g., all film masters of a set shall be examined at 30-55 X magnification for registration of all circuitry elements, registration shall be within ±0.0005 inch, the images of step and repeat arrays shall register with ±0.0005 inch, etc.)

d. Image size (e.g., line widths shall be within -0.0001 inch and +0.0003 inch for lines ≤ 0.003 inch wide and within -5 percent and +10 percent for line widths > 0.003 inch as measured at 110 X magnification; photographic reduction between designated targets shall be within ±0.0005 inch; etc.)

2.5.5 Visual inspection of screens. Each screen is examined emulsion side up for the following criteria:

a. Workmanship (e.g., screens examined at 10 X magnification for pinholes, scratches and voids which would allow ink to be applied to the substrate other than where specified, etc.)

b. Image definition (e.g., screens examined at 30 X magnification in 3 random locations to assure that the line edge is straight and firmly attached to screen, etc.)

c. Polarity (e.g., pattern identification mark on screen is examined to make sure the identification markings read in mirror image fashion, etc.)

2.6 Demonstration of Mask and Screen Processing

2.6.1 Examples of masks and screens. The manufacturer shall furnish to the NASA Certification Team examples of each of the different types of masks and screens used in the fabrication of his hybrid microcircuits. These examples shall include as a minimum:

a. Reduced 1:1 photographic film and/or glass working masks, if applicable.

b. Vacuum deposition masks, if applicable.

c. Screens for thick film processing, if applicable.

2.6.2 Demonstration. Using available documented procedures, the manufacturer shall demonstrate the processes and controls used to produce film

masks, deposition masks, and screens if these masks and screens are produced in-house. This demonstration shall include, where applicable, photographic reduction, step-and-repeating, exposure and etching of metal deposition masks, exposure and etching of chromium glass masks, emulsion application and exposure of screens. If masks and screens are fabricated by an outside vendor, the manufacturer shall demonstrate his inspection procedures. If film and/or glass masks are automatically generated in-house, the manufacturer shall demonstrate the control system and photoplotter or photogenerator.

3.0 PARTS AND MATERIALS CONTROL

3.1 Scope

This process step involves the procedures, documents and equipment involved in procuring (from outside vendors) and controlling parts and materials required in the fabrication of hybrid microcircuits. Examples of parts falling into this category are: integrated circuit chips, transistor chips, capacitor chips, resistor chips, packages, etc. Examples of materials falling into this category are: substrates, solder, thick film inks, adhesives, wire or foil, etc. Included in this step are the manufacturer's incoming inspection procedures, acceptance test procedures, and qualification test procedures.

3.2 Identification of Purchased Parts and Materials

The manufacturer shall identify those parts and materials used in the fabrication of hybrid microcircuits which are normally purchased from outside vendors. Exclude items which do not appear in the end product, such as solvents, fluxes, etchants, resists, etc.

3.2.1 Purchased parts (e.g., integrated circuit chips, transistor chips, diode chips, capacitor chips, resistor chips, inductors, flat packs, TO-8 headers, etc.)

3.2.2 Purchased materials (e.g., substrates, thick film inks, gold and aluminum bonding wire, conductive and non-conductive adhesives, solder, eutectic preforms, etc.)

3.3 Vendor Qualification

3.3.1 Procedures for vendor qualification. The manufacturer shall identify the procedures which he uses to qualify outside vendors as suppliers of parts and materials for high reliability hybrid microcircuits, if applicable. This may be done by flow chart or narrative format. Exhibit 6 in Appendix A is an example of a typical flow chart which results in a qualified part or material and a qualified vendor for that part or material.

3.3.2 Qualification tests for chip components. The manufacturer shall provide a brief listing of the qualification tests required for typical semiconductor chip components and typical passive chip components. The intent here is not to require a lengthy listing of test requirements, but rather to provide evidence to NASA that the manufacturer has used reasonable care in the selection of his chip components and vendor. Table 2 lists a typical group of qualification tests for semiconductor chips. Table 3 lists a typical group of qualification tests for capacitor chips. Tables 2 and 3 are excerpts from in-house documents.

Table 2. Qualification tests for unencapsulated semiconductor chips. The paragraph references specify tests per MIL-STD-883 or MIL-STD-750 and other test requirements as applicable.

Test	Control Level		Reference Paragraph		Test Group 2/	Number of Specimens	Number of Failures Allowed
	B	C	Requirement	Test			
Electrical characteristics	X	X	3.7.4	4.5.4	I	20	1
High-temperature reverse bias life	X	X	3.7.5.2	4.5.5.5			
Operating life	X	X	3.7.5.1	4.5.5.4			
Electrical characteristics	X	X	3.7.4	4.5.4			
Contact resistance	X	X	3.7.2	4.5.5.2	II	20	1
Temperature cycling	X	X	3.7.6.2	4.5.5.7			
Component isolation 1/	X	--	3.7.3	4.5.5.3			
Contact strength	X	X	3.7.8	4.5.5.1			
Gold backing adhesion 3/	X	X	3.7.9	4.5.5.8	III	20	1

1/ IC dice only.
2/ See 4.4.1.1 and 4.4.1.2 for packaging and mounting instructions for Groups I and II, respectively.
3/ Bipolar transistor and diode dice only.

Table 3. Qualification test table for fixed, ceramic dielectric capacitor chips. The paragraph references specify tests per MIL-C-11015 and other test requirements as applicable.

Test	Control Level				Reference Paragraph		Test Group	Number of Specimens
	A	B	C	S	Requirement	Test		
Visual and mechanical examination			X		--	4.5.2	I	37
Materials, design, construction, and workmanship			X		3.6, 3.6.1, 3.6.2	4.5.2		
					3.6.3, 3.8.1, 3.8.2			
Physical dimensions			X		3.6.4	4.5.2		
Dielectric withstanding voltage			X		3.7.2	4.5.2(a)		
Barometric pressure (reduced)			X		3.7.10	4.5.2(b)		
Insulation resistance			X		3.7.10	4.5.2(c)		
Capacitance			X		3.7.10	4.5.2(d)		
Dissipation factor			X		3.7.10	4.5.2		
Shock, medium impact			X		3.7.3	4.5.2	II	12
Vibration, high frequency			X		3.7.4	4.5.2		
Temperature cycling			X		3.7.5	4.5.2		
Dielectric withstanding voltage			X		3.7.2	4.5.2(a)		
Insulation resistance			X		3.7.1	4.5.2(c)		
Capacitance			X		3.7.1	4.5.2(d)		
Dissipation factor			X		3.7.1	4.5.2		
Salt spray			X		3.7.6	4.5.2		
Termination strength			X		3.7.7	4.5.3.1	III	12
Moisture resistance			X		3.7.8	4.5.2		
Dielectric withstanding voltage			X		3.7.2	4.5.2(a)		
Insulation resistance			X		3.7.10	4.5.2(b)		
Capacitance			X		3.7.10	4.5.2(d)		
Voltage temperature limits			X		3.7.10	4.5.2(e)	IV	12
Life			X		3.7.9	4.5.2(f)		
Dielectric withstanding voltage			X		3.7.2	4.5.2(a)		
Insulation resistance			X		3.7.1	4.5.2(b)		
Capacitance			X		3.7.1	4.5.2(d)		
Dissipation factor			X		3.7.1	4.5.2		

3.4 Incoming Inspection and Testing

The manufacturer shall identify the procedures, methods and tests used to insure the quality and acceptability of purchased parts and materials used in the fabrication of high reliability hybrid microcircuits. A flow chart (see Exhibit 7 in Appendix A) may be used to illustrate the manufacturer's incoming inspection and test procedures.

3.4.1 Listing of quality conformance and acceptance tests. The manufacturer shall provide a brief listing of the quality conformance or acceptance tests required for typical semiconductor chip components and typical passive chip components. The intent of this listing is to provide evidence to NASA that the manufacturer uses reasonable care to assure that all active and passive chip components conform to a given set of quality requirements. Where applicable, this listing should include the sampling plan.

Example:

a. Tables 4 and 5 list the quality conformance inspection requirements and sampling plan schedules for transistor chips.

b. Table 6 lists the quality conformance inspection requirements and sampling plan schedule for fixed, ceramic dielectric capacitor chips.

Note: Tables 4, 5, and 6 are excerpts from in-house documents.

3.4.2 Performance of quality conformance tests. The manufacturer shall indicate whether the quality conformance tests are done by his own incoming inspection area or by the vendor and whether or not a certification is furnished.

Example:

Chip components tested by vendor per quality conformance requirements of manufacturer's specification. Vendor furnishes a certificate of compliance. All chip components visually inspected as part of incoming inspection procedure. Acceptance testing may be done at the option of the manufacturer to insure that the parts supplied conform to prescribed requirements.

Table 4. Quality conformance inspection requirements for unencapsulated, silicon, PNP transistor chips. The paragraph references specify test parameters per MIL-STD-883 or MIL-STD-750 and other test requirements as applicable.

Inspection or Test	Reference 1/	AQL 2/ Control Level					Acc No.	Rej No. 3/
			B	C				
Process conditioning	*4.4.3		100%	100%			--	--
Wafer electrical tests	*4.5.4 and Table II herein		100%	100%			--	--
Visual inspection	*4.5.5.6		100%	100%			--	--
Subgroup 1 (packaged dice)	*4.4.1, *4.4.1.1		1.5	2.5			0	2
Contact resistance	*4.5.5.2							
Critical electrical parameters	*4.5.5.5 and Tables III and V herein							
High-temperature reverse bias life	*4.5.5.5 and Table V herein							
Critical electrical parameters	*4.5.5.4 and Tables II and V herein							
Operating life (Level B)	*4.5.5.4 and Table V herein							
Electrical characteristics	*4.5.4 and Table III herein							
Subgroup 2	*4.4.1, *4.4.1.2		1.5	2.5			0	2
Temperature cycling (Level B)	*4.5.5.7							
Contact strength	*4.5.5.1							

1/ Numbers prefixed by an asterisk identify paragraphs in General Specification 933000.
2/ AQL is for procurement order of 201 dice or more. Refer to 4.4.5 of General Specification 933000 for sample sizes and for sampling information concerning smaller orders.
3/ For one reject, double sampling shall apply.

Table 5. Sampling plan schedule for transistor and diode chips per MIL-STD-105.

Purchase Quantity	Control Level B		Control Level C		Acc No.	Rej No.
	AQL 1/	Sample Size	AQL 1/	Sample Size		
Up to 200	2.5 (17.6)	13	4.0 (26.5)	8	0	2
		26		16	1	2
201 and up	1.5 (11.8)	20	2.5 (17.6)	13	0	2
		40		26	1	2

1/ Approximate LTPD shown in parenthesis is for information only. The sample sizes for the second sample are accumulative total.

Table 6. Quality conformance inspection requirements for fixed, ceramic dielectric capacitor chips. The paragraph references specify tests per MIL-C-11015 and other test requirements as applicable. The sampling plan is in accordance with MIL-STD-105.

Test	Control Level				Reference Paragraph		AQL Control Level				Insp. Level			
	S	A	B	C	Requirement	Test	S	A	B	C	S	A	B	C
Visual and mechanical examination				X	--	4.5.2				1.0				II
Dielectric withstanding voltage				X	3.7.2	4.5.2(a)				1.0				II
Insulation resistance				X	3.7.10	4.5.2(b)								
Capacitance				X	3.7.10	4.5.2(d)				100%				
Dissipation factor				X	3.7.10	4.5.2				100%				

3.5 Packaging and Storage

The manufacturer shall indicate any special packaging and storage requirements which he uses for chip components or materials.

3.5.1 Packaging (e.g., semiconductor dice shall be packaged in multicavity containers which will prevent intermingling of, or damage to, the dice during shipment; the cavities shall be uniformly arrayed and of a depth approximately twice the overall die thickness; the dice shall be inserted with contacts facing upward; a flat transparent lid shall fit over the cavity surface tight enough to seal out dust particles that are 5 microns or larger; capacitor chips packaged per Level C of MIL-C-39028; etc.)

3.5.2 Storage (e.g., chip components shall be stored in a dry nitrogen atmosphere until ready for assembly; conductive and non-conductive adhesives kept under refrigeration and labeled with a "limited shelf life" sticker; etc.)

3.6 Documentation

The manufacturer shall furnish evidence of specification documentation used in the procurement of high reliability parts and materials for hybrid microcircuits. Specifications shall exist for at least the following classifications of parts and materials:

3.6.1 Parts

a. Transistors and transistor chips
b. Diodes and diode chips
c. Integrated circuits and integrated circuit chips
d. Capacitors and capacitor chips
e. Resistors and resistor chips
f. Inductors
g. Packages or enclosures (hermetic or otherwise)

3.6.2 Materials

a. Substrates (predeposited or otherwise)
b. Bonding wire, foil, ribbon, or preforms

c. Adhesives (non-conductive or conductive) appearing in the end product.

d. Encapsulants, conformal coatings, potting compounds, or other plastics appearing in the end product.

e. Thick film inks (conductor, resistor, dielectric, overglaze, insulating, etc.)

3.7 Demonstration

The manufacturer shall demonstrate, using documented procedures, his qualification and/or quality conformance tests and controls where applicable, including documentation of the test results. If burn-in tests are used for chip components, the manufacturer shall demonstrate his burn-in capability at the time and temperature specified for the particular part under test.

4.0 SUBSTRATE CHARACTERIZATION

4.1 Scope

This process step involves the materials, processes, equipment, and controls involved in the characterization of substrates on which hybrid microcircuits are to be fabricated.

4.2 Identification of Substrate Type

The manufacturer shall identify the substrate type or types with respect to:

4.2.1 End usage (e.g., thick film applications; thin film applications; etc.)

4.2.2 Material and purity (e.g., 96.0 ± 0.10 percent pure alumina for thick film; 99.5 ± 0.05 percent pure alumina for thin film; etc.)

4.2.3 Metalization, if applicable (e.g., thin film substrates predeposited with resistive and conductive layers on one side only per Table 7; thick film substrates unmetalized; etc.)

Table 7. Thin film substrate metalization layers. Nickel-chromium is the bottom layer and the plated gold is the top layer.

Metal or Alloy	Deposition Method
Nickel-chromium	Vacuum deposited
Nickel	Vacuum deposited
Gold	Vacuum deposited
Gold	Electroplated

4.2.4 Substrate surface finish (e.g., 25 microinch, centerline average, for thick film applications; 10 microinch, centerline average, one face only, for thin film applications; etc.)

4.2.5 Vendor. The manufacturer shall indicate whether the substrates he uses are made and/or metalized in-house or purchased from an outside vendor (e.g., predeposited thin film substrates purchased from outside vendor; thick film unglazed alumina ceramic substrates purchased from outside vendor; etc.)

4.3 Identification of Substrate Controls

The manufacturer shall identify the substrates controls which he uses. The controls shall include the following, where applicable:

4.3.1 Workmanship (e.g., the substrate shall be clean and free from cracks, scratches, chips, burrs, and similar mechanical damage which extend more than 0.010 inch from an edge; there shall be no blisters, pits, pocks, pinholes, porous areas, foreign inclusions, or other defects that would affect the material's properties; for predeposited substrates there shall be no more than 5 pinholes larger than 0.001 ± 0.0005 inch on the entire substrate and no more than 3 craters, nodules, or blisters on any one substrate nor shall any of these defects exceed 0.002 inch; there shall be no nicks or scratches extending through the conductor layer to expose the resistor layer underneath; etc.)

4.3.2 Basic substrate material properties. The manufacturer shall identify specific material property controls, where applicable:

a. Specific gravity (e.g., 3.67 minimum per ASTM D20, etc.)
b. Water absorption (e.g., < 0.05 percent per ASTM C373, etc.)
c. Hardness (e.g., minimum of 75 on Rockwell 45N scale per ASTM E18, etc.)
d. Flexural strength (e.g., 40,000 psi minimum per ASTM C369, etc.)
e. Thermal conductivity (e.g., 200 BTU/ft^2/in/hr/°F minimum per ASTM C201, etc.)
f. Thermal shock (e.g., no evidence of chipping or cracking after successive 5 minute exposures to -55°C and 100°C with no more than 5 seconds transfer time, etc.)
g. Dielectric constant (e.g., 9.0 minimum at 1 MHz and +25°C per ASTM D150, etc.)
h. Loss factor (e.g., 0.003 minimum at 1 MHz and +25°C per ASTM D150, etc.)
i. Surface resistivity (e.g., 1 x 10^{14} ohms/square minimum after 10 hours at +125 ± 10°C per ASTM D257, etc.)

4.3.3 Substrate metalization properties, if applicable. The manufacturer shall identify the controls used for the substrate metalization layers:

a. Temperature coefficient of resistance (e.g., TCR of thin film resistor layer ≤ ±100 ppm/°C over the range -55°C to +150°C when tested per MIL-STD-202, Method 304, etc.)
b. Uniformity (e.g., TCR shall be uniform between test resistors on the same substrate within 25 ppm, etc.)
c. Adhesion (e.g., the resistor layer shall firmly adhere to the ceramic substrate and the conductor layers shall firmly adhere to the resistor layer when subjected to a "Scotch tape adhesion test"; the substrate is photoetched and one end of a 4-inch length of L-T-90, Type I, Class A pressure sensitive tape is pressed on the metalized surface and smoothly pulled off at a 90-degree angle, the tape is then inspected at 7 to 30X magnification for any evidence of adhering metal, etc.)

d. Solderability (e.g., electroplated conductors shall be solderable without loss of firm interlayer adhesion as demonstrated by soldering a 5-mil diameter copper wire to at least 4 conductor pads on a substrate, soldering is done per MIL-STD-454, Requirement 5A using a 6-watt soldering iron with Sn63, Type R solder, etc.)

e. Electrical. Predeposited thin film alumina substrates are controlled as to the electrical properties of the resistor and conductor layers as follows:

- Resistor layer sheet resistance shall be 225 ohms per square ±10 percent after stabilization as determined by a digital ohmmeter accurate to 0.01 ohm.
- Conductor layer sheet resistance ≤ 0.02 ohms per square as determined by a digital ohmmeter accurate to 0.01 ohm.
- Stability of the resistor layer shall not exceed ±0.3 percent after exposure to +125°C for 1000 hours.

4.3.4 Cleanliness (e.g., prior to processing, thick film substrates are cleaned by ultrasonic cleaning in two different solvents, rinsed in deionized water, and oven dried; prior to processing, thin film substrates are cleaned by immersion in special cleaner, deionized water rinse, methanol rinse, blow dry with nitrogen, and oven dry; etc.)

4.3.5 Storage (e.g., prior to processing, cleaned substrates are placed in clean, covered containers and stored in nitrogen atmosphere dry boxes, the nitrogen flow rate is 6 to 10 cubic millimeters per minute minimum with a dew point ≤ -40°C, etc.)

4.4 Documentation

The manufacturer shall furnish evidence of substrate material specification control (e.g., metalized thin film substrates suitable for resistor-conductor networks covered by material specification HMS XX-XXXX; unglazed alumina ceramic substrates covered by material specification HMS XX-XXXX; etc.)

4.5 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance method related to the following.

4.5.1 Visual (e.g., substrates 100 percent visually inspected for workmanship requirements, metalized film coverage, packaging, and marking, etc.)

4.5.2 Dimensional. Substrate dimensions are inspected for:

a. Thickness (e.g., thick film and thin film substrate thickness is controlled to 0.025 ± 0.0002 inch as measured at 5 locations on the substrate surface using a Pratt and Whitney thickness gauge, etc.)

b. Width and length (e.g., substrate width and length are controlled to ±0.010 inch or ±1.0 percent as measured by vernier calipers with a dial indicator accurate to ±0.001 inch, etc.)

c. Flatness or camber (e.g., substrate flatness tolerance for thick film substrates is 0.003 inch per inch and for thin film substrates is 0.002 inch per inch as determined by a Pratt and Whitney thickness gauge measured at the center of the substrate and three perimeter locations, etc.)

d. Surface roughness (e.g., thin film substrates shall be no rougher than 10 microinch, centerline average, as measured by a Talysurf 4 Profilometer with a rectilinear recorder in accordance with ASA-B 46.1, etc.)

4.5.3 Adhesion and solderability, if applicable (e.g., one sample from each lot of predeposited thin film substrates is inspected for adhesion and solderability, etc.)

4.5.4 Metalization layer electrical resistance (e.g., one sample from each lot of predeposited thin film substrates is inspected for resistor layer and conductor layer resistivity and for temperature coefficient of resistance; resistivity evaluation is done on a special test pattern photoetched in three or more well-spaced places on the test substrate; etc.)

4.6 Demonstration of Substrate Characterization

For each substrate type to be certified, the manufacturer shall demonstrate, using documented procedures, the substrate controls and inspection processes normally used. The NASA Certification Team will be given randomly-selected substrates prior to fabrication for inspection in accordance with the manufacturer's documents.

5.0 FILM PATTERNING

5.1 Scope

This process step involves the materials, methods, equipment, and controls used by the manufacturer to delineate resistor and conductor patterns on substrates for thin film and thick film hybrid microcircuits. Included are such processes as photoresist application, exposure, development, and etching for thin film networks and screen printing and firing for thick film networks. This process step does not include resistor trimming, substrate sizing, or any assembly operations as they are covered in process steps which follow.

5.2 Identification of Electrically-Functional Materials

The manufacturer shall identify the materials used to form the resistor, conductor, dielectric, crossover, insulating, and passivating layers. The manufacturer shall also indicate whether the particular material's end usage is for a thin film or thick film network.

5.2.1 Resistor materials (e.g., nickel-chromium alloy used for thin film resistors; proprietary cermet inks used for thick film resistors; etc.)

5.2.2 Conductor materials (e.g., electroplated gold-over-nickel used for thin film conductors; proprietary cermet ink used for thick film conductors; etc.)

5.2.3 Crossover and/or dielectric materials (e.g., proprietary dielectric ink used for thick film crossovers and also as an insulating layer for thick film multilayer designs; no crossover materials used in thin film designs; etc.)

5.2.4 Overglaze or passivating materials (e.g., protective overglaze used over thick film resistors when required; no passivating or protective overcoating used over thin film resistors; etc.)

5.3 Identification of Electrically-Functional Material Controls

The manufacturer shall identify his controls for those materials which, when processed, perform an electrical function, such as a resistive, conductive, dielectric, or passivating function.

5.3.1 Thin film materials. Since all thin film microcircuits are processed from predeposited substrates purchased from an outside vendor, the controls used for the resistor and conductor films have been covered in Section 4.0 of this document since they are an inseparable part of the substrate.

5.3.2 Thick film materials.

a. Indicate whether thick film inks are formulated in-house or purchased (e.g., thick film inks purchased from outside vendor in accordance with manufacturer's specification; certificate of compliance furnished by outside vendor; etc.)

b. Viscosity (e.g., viscosity of resistor ink shall be determined per ASTM D1824 using a Brookfield Viscometer at 10 RPM with a No. 7 spindle and 0.75 inch immersion of 190,000 ± 40,000 centipoises at 79 ± 2° F, etc.)

c. Drying and firing (e.g., resistor ink shall be free of solvent after a XX minute bake at XX° C; resistor ink shall form a uniform cermet without any visible defects after a firing cycle including XX minutes at XX°C; etc.)

d. Performance characterization. Each bottle of thick film ink is characterized by screening, firing, and testing the resultant film for the applicable characteristics, such as:

- Resistance and TCR (e.g., resistor inks after drying and firing to form a XX ± 0.1 mil thick film shall comply with the requirements in Table 8; TCR is measured at -55° C, +25° C, and +150° C; etc.)

Table 8. Resistance tolerances and TCR

Nominal Sheet Resistivity (ohms/square)	Resistivity Tolerance (percent)	Maximum TCR (ppm/ C)
10	±50	±300
100	±20	±150
1K	±20	±150
10K	±20	±150
100K	±25	+150, -250
1 MEG	±30	+50, -800

- Conductivity (e.g., conductor inks, after drying and firing to form a film XX ± 0.2 mil thick, shall have a sheet resistance of 0.003 - 0.015 ohms per square; etc.)
- Adhesion, if applicable (e.g., conductor inks, when fired on a 96 percent alumina substrate, shall adhere firmly to the substrate material without flaking or separation; adhesion is tested by TC bonding a 2-mil diameter gold wire to at least 4 pads and then pulling the wires off at a 90-degree angle; if the conductor material separates from the substrate before the bond or wire fails, the material is not acceptable; etc.)
- Solderability, if applicable (e.g., conductor inks, when fired on a 96 percent alumina substrate, shall be solderable as determined by soldering a 30-36 AWG copper wire to at least four conductor pads using a 6-watt soldering and Sn62, Type R solder; the solder must completely wet the conductor pad and form smooth joints without evidence of locally dissolving all the conductor material; etc.)

e. Screenability, if applicable (e.g., overglaze inks shall be capable of passing through a 200 mesh screen to produce a uniform layer of paste on the substrate, etc.)

f. Blending of inks, if applicable (e.g., resistor inks of the same type are blended to obtain required sheet resistance values by mixing weighed quantities of two ink values in accordance with a

predetermined blending curve of resistivity versus percentage composition, etc.)

g. Storage (e.g., all thick film ink compositions are stored on a rotating jar mill so that each container goes through 3.8 complete revolutions per 24 hours; all ink jars contain a shelf life label with an expiration date from 6 months to 1 year after the manufacturing or arrival date; etc.)

5.4 Thin Film Processing

The manufacturer shall identify his thin film processing method (or methods) and controls. A flow chart similar to that shown in Exhibit 3 of Appendix A shall be submitted to the NASA Certification Team showing the various thin film processing steps in their proper sequence.

5.4.1 Processing method (e.g., "subtractive" method - photoetching resistive and conductive films predeposited on alumina substrates; etc.)

5.4.2 Thin film multilayer capability (e.g., multilayer thin film hybrids are not fabricated, etc.)

5.4.3 Photoresist processing and controls. The manufacturer shall identify his photoresist processing methods and controls with respect to:

a. Photoresist processing area (e.g., photoresist area has yellow filtered illumination with temperature thermostatically controlled to 75° ± 5° F, etc.)

b. Type of photoresist (e.g., negative-type photoresist, etc.)

c. Photoresist material controls (e.g., photoresist is controlled with respect to solids residue and viscosity; solids residue is determined by means of solvent evaporation and differential weighing to an accuracy of ±1.0 percent on one sample from each photoresist lot; viscosity is determined by either the torque method utilizing a Synchro-Lectric Viscometer with a No. 2 Spindle to an accuracy of ±1 percent or per ASTM D445-65 using a Cannon-Fenske Viscometer where a fixed volume of liquid is allowed to flow by gravity through a capillary; a viscosity test is performed on every lot of photoresist; etc.)

d. Preparation of photoresist (e.g., a new batch of photoresist is prepared daily by filtering through a Millipore No. AD2504200 prefilter and a Millipore No. URWG04700 filter in sequence; photoresist is thinned with electronic grade thinner; etc.)

e. Application of photoresist (e.g., photoresist is applied by spinning at XXXX rpm under a Microvoid dust-free hood; photoresist prebaked in a circulating air oven; etc.)

f. Photoresist application controls (e.g., spinner RPM determined by General Radio Type 1531.A Strobotac; thickness of photoresist film determined by counting interference fringes using a metallurgical microscope with a 5500 Å filter; vacuum hold-down keeps substrate on spinner head during spinning; photoresist film examined at 7-30 X magnification for dust, lint, pinholes and other surface defects; pinhole density determined by counting the number of pinholes in 16 random 0.025 inch x 0.025 inch squares under 200 X magnification; etc.)

g. Mask alignment, exposure, and development (e.g., photomask aligned emulsion-side down in specially-designed alignment fixture with vacuum hold-down using 7-30 X magnification; pattern exposed under ultraviolet light and developed in developer for X minutes; pattern postbaked for X minutes at XX° ± 5° C; etc.)

h. Exposure controls (e.g., light intensity measured by BLAK-RAY UV Meter, Type J-221; resist pattern inspected under 7-30 X magnification for pattern definition, voids, inclusions, and similar defects; touch-up is allowed using staging ink for gross pinholes and a needle probe to scratch off unwanted photoresist; unacceptable patterns are stripped and redone; etc.)

5.4.4 Pattern etching and controls. The manufacturer shall identify his etching processes and controls with respect to:

a. Type of etching (e.g., chemical etching, etc.)

b. Type of patterns etched (e.g., gold-over-nickel conductor patterns etched; nichrome resistor patterns etched using a composite resistor-conductor photomask; etc.)

c. Etching processes and materials (e.g., conductor patterns etched using proprietary etchants; conductor etching done at XX° ± 5° C using titanium substrate holders; resistor patterns etched using a proprietary oxidizing and reducing solution at XX° ± 5° C; etc.)

d. Etching controls (e.g., etchant temperature controlled by constant temperature water bath; fresh etchants mixed daily using deionized water; etching done under a fume hood; operator visually examines patterns during etching to determine when conductor or resistor film is completely removed; patterns inspected immediately after etching under 30 X magnification for complete removal of metal; etc.)

5.4.5 Resist removal and cleaning (e.g., resist removed by soaking substrates for 45 ± 15 seconds in proprietary stripper at room temperature followed by cotton swabbing; substrates inspected under 10 X magnification for complete removal of resist; substrates cleaned by a water rinse, solvent degrease, solvent rinse, nitrogen blow dry, special cleaner immersion, deionized water rinse, solvent rinse, nitrogen blow dry; etc.)

5.4.6 Resistor stabilization, if applicable (e.g., etched resistors stabilized for XX hours ± 5 minutes at XXX° ± 5° C, etc.)

5.5 Thick Film Processing

The manufacturer shall identify his thick film processing method (or methods) and controls. A flow chart similar to that shown in Exhibit 2 of Appendix A shall be submitted to the NASA Certification Team showing the various thick film processing steps in their proper sequence.

5.5.1 Processing method (e.g., thick film hybrids processed by screening and firing conductor, resistor, dielectric, and overglaze inks on alumina ceramic substrates, etc.)

5.5.2 Thick film multilayer capability (e.g., multilayer thick film hybrid microcircuits are fabricated with up to three conductor levels, etc.)

5.5.3 Screen printing and controls. The manufacturer shall identify his screen printing process and controls with respect to:

a. Screen printer set-up (e.g., screen printers set up for proper air pressure, screen-to-substrate breakaway distance, squeegee printing pressure, squeegee travel speed across screen, leveling of screen, X-Y location of screen with respect to substrate, squeegee stop, alignment of printed patterns with respect to each other, etc.)

b. Screen printing controls (e.g., micrometer controls on screen printer for adjusting breakaway distance, X-Y alignment, angularity, screen parallelism, squeegee down stop; special screens used which are parallel to ±0.002 inch; printed pattern registered on substrate within ±0.001 inch; dry film thickness measured using Zeiss Light Section Microscope on sample substrates prior to printing final parts at either 200 X or 400 X magnification; test firing of all resistor prints done prior to printing the entire lot to assure correct sheet resistance value; etc.)

5.5.4 Drying (e.g., printed patterns allowed to level for at least XX minutes, then placed in drying oven for X minutes at XXX° ± 5° C, etc.)

5.5.5 Firing process and controls. The manufacturer shall identify his firing processes and controls with respect to:

a. Firing process (e.g., firing of resistor, conductor, dielectric, and overglaze inks is done in 4-zone and 5-zone furnaces; three separate furnaces are used - one for resistor and conductor inks, one for multilayer conductor and dielectric inks, and one for overglaze inks; conductor and crossover dielectric inks are cofired; all resistor ink types are printed, dried, and then fired simultaneously; printed substrates are placed on the furnace belt, circuit side up, and allowed to transverse the length of the furnace; a filtered dry air atmosphere is used in the resistor-conductor 5-zone furnace; etc.)

b. Firing controls (e.g., furnaces adjusted for belt speed, peak temperature of each zone, and furnace profile; temperature

profiles performed weekly using chromel-alumel, Type K, thermocouple and temperature recorder; peak temperature measurements are made daily prior to any firing operations; belt speed verification is done weekly; firing furnaces accurate to 1000° C ± 1° C; etc.)

5.6 Documentation

The manufacturer shall furnish evidence of the following.

5.6.1 Process documentation for thin film and thick film processes (e.g., production of etched thin film resistor-conductor networks documented by process specification HP XXXX together with separate process instruction specifications for photoresist exposure and development, resistor pattern etching, conductor pattern etching, resist removal, and resistor stabilization bake; production of thick film resistor-conductor networks documented by process specification HP XXXX together with separate process instruction specifications for screen printing, drying, and firing; etc.)

5.6.2 Material documentation control for thick film inks (e.g., conductive printing inks controlled by material specification HMS XXXX, resistive printing inks controlled by material specification HMS XXXX, protective overglaze controlled by material specification HMS XXXX, dielectric coatings for multilayer applications controlled by material specification HMS XXXX; etc.)

5.6.3 Environmental test data. Test data showing that thin film and thick film resistor-conductor networks processed in accordance with the manufacturer's internal specifications are capable of withstanding the following environments:

a. +125° C for 1000 hours at a power loading of 25 watts per square inch with less than 0.1 percent resistance drift.

5.6.4 Static discharge test data. Test data showing the effect of static electricity discharge on thin and thick film resistors, such as that caused by polyethylene bags, gloves, latex finger cots, Dacron lab smocks, etc. The manufacturer shall show what precautions he has taken to minimize or eliminate static discharge effects, such as using special antistatic polyethylene bags to package the substrates.

5.7 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance methods related to the following.

5.7.1 Visual examination and inspection (e.g., all thin film and thick film resistor-conductor networks are visually examined under a minimum of 30 X magnification for the following workmanship requirements: voids, holes, cracks, nicks, scratches across resistors or conductors, unetched or misprinted conductor and resistor areas, misalignment of conductor and resistor patterns, foreign material on surface of substrate, open circuits, short circuits, metalization too close to edge of substrate, nicks or cracks in substrate, any evidence of lifting of resistor or conductor; visual inspection done in accordance with a set of visual inspection criteria sketches; thin film resistor-conductor networks inspected per requirements of MIL-STD-883, Method 2010 except as modified; etc.)

5.7.2 Resistance (e.g., all thin film and thick film resistors tested for DC resistance per MIL-STD-202, Method 303 using a digital ohmmeter or digital voltmeter to determine conformance with the tolerances specified on the applicable engineering drawing or to insure that the resistors are within trimming capability; resistance readings are recorded on applicable data sheet; etc.)

5.7.3 Handling and storage (e.g., processed substrates are handled only by the edges or by means of clean gloves or tweezers; processed substrates are individually packaged in antistatic polyethylene bags labeled with the part number and serial number; processed substrates are stored in a dry box under nitrogen atmosphere at a flow rate of 6 to 10 cubic millimeters per minute minimum; etc.)

5.7.4 Acceptance inspection for thin film resistor-conductor networks.

a. A minimum of 3 test patterns, each containing at least 5 resistors, are tested for resistance drift per MIL-STD-202, Method 108A, Condition B at 150° ± 3° C.

b. A special test pattern having 0.005-inch lines and spaces is tested for insulation resistance per MIL-STD-202, Method 302, Condition A at room ambient. The resistance between unconnected circuit elements shall be greater than 5×10^9 ohms.

c. The adhesion of a resistor-conductor network is tested by a tape test. The metalized layers shall not separate from each other or from the substrate.

5.7.5 Acceptance inspection for thick film resistor-conductor networks.

a. Special test pattern tested for resistance drift after 200 hours at +150° ± 3° C per MIL-STD-202, Method 103A, Condition D.

b. Conductor resistivity is determined on a special test pattern at 100 ± 5 milliamperes and +25° ± 5° C. The resistivity shall be less than 0.1 ohm per square per mil.

c. Three test patterns for each different resistor ink are tested for temperature coefficient of resistance per MIL-STD-202, Method 304 between the temperatures of -55° C and +122° C.

d. Three test patterns, each containing at least 5 resistors, are tested for resistance drift after temperature cycling per MIL-STD-202, Method 102A, Condition C (except high temperature to be +150° C, +3°, -0° C).

e. Three test patterns are tested for insulation resistance per MIL-STD-202, Method 302, Condition A at room ambient. The resistance between unconnected circuit elements shall be greater than 5×10^9 ohms.

f. Three test patterns are tested for conductor-to-substrate adhesion by soldering a 32 gage solder coated copper wire to 0.1-inch square test pads and pulling the wire perpendicular to the pad at a rate of 2 inches per minute. The minimum adhesion strength shall be 175 pounds per square inch.

g. Three test patterns are tested for resistor-to-conductor overlap adhesion with a minimum overlap of 0.015 inch in accordance with Federal Test Method Standard No. 141, Method 6301.1, except that the substrates are not immersed in water before testing and

the parallel scratch test is not performed. The resistor material on the resistor-conductor overlap shall not be lifted from the conductor by the use of adhesive tape.

h. Test patterns are tested for solderability by manually soldering 32 gage solder coated copper wires to test pads using Sn60, Sn62 or Sn63 tin-lead solder, form W, type RMA conforming to QQ-S-571. The conductor areas must readily accept solder.

i. The thickness of the glass or dielectric layer in production multilayer and crossover applications must be a minimum of 0.0012-inch.

j. The electrical continuity of multilayer and crossover designs is determined by measuring the voltage drop using a volt-ohm-milliammeter. A suitable detector is used to indicate any discontinuities of one microsecond duration. There shall be no evidence of continuity between the crossover conductor(s) and the lower conductor.

k. The dielectric breakdown voltage of the glass or dielectric layer is tested per MIL-STD-202, Method 301 using a production pad or a test specimen. The breakdown voltage shall be a minimum of 300 volts (dc)/mil.

5.8 Demonstration of Film Patterning

For each film patterning method to be certified, the manufacturer shall demonstrate, using documented procedures, the processes and controls used. For thin film resistor-conductor networks, this demonstration shall at least include photoresist application, exposure, development, etching, and resist removal. For thick film resistor-conductor networks, this demonstration shall at least include printing, drying, and firing of resistor, conductor and dielectric inks.

At least 10 random samples of each type of network to be certified shall be selected from a production run and examined under magnification by the NASA Certification Team in accordance with the manufacturer's visual acceptance criteria. No samples shall fail this examination.

6.0 SUBSTRATE SIZING

6.1 Scope

This process step involves the methods, equipment, and controls used by the manufacturer to cut (e.g., saw, scribe, break, etc.) the substrate to the proper size so that it will properly fit within the package enclosure. This step may consist of sizing an individual substrate containing one circuit or of separating several circuits formed on the same substrate (i.e., such as by using step-and-repeat multiple patterns) into a number of smaller individual substrates. This process step is not intended to cover the methods used to scribe, dice, or otherwise size semiconductor chips, capacitor chips, or similar discrete chips which are eventually intended for mounting on substrates.

References. Figure 1 shows the position of the substrate sizing process step in relation to the overall hybrid microcircuit operation. The position of this process step may vary widely depending upon the particular processing steps which precede or follow the substrate sizing operation. The flow charts in Exhibits 2 and 3 (Appendix A) show the specific position of the substrate sizing step in a typical thin film and thick film fabrication sequence. The manufacturer shall include on a similar flow chart or charts, the position of the substrate sizing step in relation to his particular fabrication sequence.

6.2 Identification of Substrates to be Sized

The manufacturer shall identify the substrates to be sized with respect to the following.

6.2.1 Fabrication type (e.g., thick film substrates; thin film substrates; etc.)

6.2.2 Material and thickness (e.g., unglazed alumina, 0.025-inch thick; etc.)

6.2.3 Size and tolerance (e.g., 0.750 ± 0.005 inch x 0.750 ± 0.005 inch, etc.)

6.2.4 Condition of substrate (e.g., thick film substrates sized prior to screening and firing; thin film substrates sized following photoetching, but prior to trimming; etc.)

6.3 Identification of Substrate Sizing Method

The manufacturer shall identify each of the substrate sizing methods to be certified.

6.3.1 Method (e.g., diamond scribe and manually break; saw; diamond scribe and machine fracture; substrates purchased from vendor precut to size; laser scribing; etc.)

6.4 Identification of Substrate Sizing Controls

For each combination of substrate sizing method and substrate type, the manufacturer shall identify the substrate sizing controls.

6.4.1 Diamond scribing of thin film unglazed alumina substrates.

a. Diamond type (e.g., 4-sided, etc.)
b. Diamond angle (e.g., 20 degrees ±5 degrees, etc.)
c. Diamond pressure (e.g., pressure controlled by manually adjusting spring tension to within ±40 grams of the prescribed value; etc.)
d. Accuracy of cut (e.g., micrometer adjustment set by operator to within 0.005-inch in either width or length; etc.)
e. Method of breaking scribed substrates (e.g,, substrates manually broken by operator along scribed line; etc.)
f. Substrate hold-down (e.g., substrate held in spring-loaded clamp; etc.)
g. Scribing speed (e.g., operator manually controls speed of diamond tool, etc.)

6.4.2 Sawing of thick film unglazed alumina substrates.

a. Substrate hold-down (e.g., substrates bonded to cutting block using special cement at +160° C, etc.)

b. Saw blade type and thickness (e.g., 10-mil wide diamond blade, etc.)

c. Speed of cut (e.g., transverse travel of saw blade manually controlled by operator to approximately 10 inches/minute, etc.)

d. Depth of cut (e.g., depth of cut pre-set by micrometer adjustment to cut completely through substrate, etc.)

e. Accuracy of cut (e.g., micrometer adjustment pre-set by operator to within 0.005-inch in either width or length, etc.)

f. Cleanliness (e.g., after cutting, operator demounts substrate from block and cleans substrate by successive solvent rinses; etc.)

6.5 Documentation

The manufacturer shall furnish evidence of:

6.5.1 Process documentation (e.g., diamond scribing documented in Aerospace Engineering Process Instruction AEPI XXXX, Rev. B; substrate sawing documented in process specification HP XXX and process instruction PI XXXX; etc.)

6.5.2 Test data. Test data substantiating that the substrate sizing process used in no way affects the electrical performance of the hybrid microcircuit.

6.6 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance methods related to the following.

6.6.1 Visual examination of sized substrate (e.g., substrates 100 percent inspected under 30 X magnification for raggedness of edge, cracks in substrate, chips, misalignment of cut, cleanliness, etc.)

6.6.2 Dimensions of sized substrate (e.g., the length and width of the sized substrates are measured using vernier calipers accurate to ±0.001 inch, measurement is done on a sampling basis — one out of every 5 substrates, etc.)

6.7 Demonstration of Substrate Sizing

For each combination of substrate sizing method and substrate type, the manufacturer shall demonstrate, using documented procedures, the substrate sizing process and the controls used. A minimum of 10 individual substrates shall be sized, cleaned (if applicable), examined under 30 X magnification, and dimensionally measured to the specified tolerance. This demonstration shall include the sizing of multiple substrate patterns (if applicable) as well as the sizing of individual substrates containing only one circuit pattern.

7.0 TRIMMING

7.1 Scope

This process step basically involves the methods, equipment, and controls used by the manufacturer to trim (or adjust) passive components to the values and tolerances specified and to insure that the trimming operation is under control and will produce consistent results. More specifically this process step is primarily concerned with the trimming of thick film and thin film resistors. However, also included within the scope of this process step is the trimming of other passive components, such as capacitors, if applicable. In addition this step is intended to include the trimming of passive chip components, as well as those passive components formed directly on the substrate.

References: Figure 1 shows the position of the trimming step in relation to the overall hybrid microcircuit operation. The flow charts in Exhibits 2 and 3 (Appendix A) show the specific position of the trimming step in relation to the thick film and thin film fabrication processes. The manufacturer shall include a similar flow chart as part of his certification.

7.2 Identification of Parts to be Trimmed

The manufacturer shall identify:

7.2.1 Types of devices to be trimmed (e.g., thick film resistors; thin film resistors; capacitor chips; etc.)

7.2.2 The range of values of the devices normally trimmed (e.g., thin film resistors from 10 ohms to 100K ohms; thick film resistors from 10 ohms to 1 megohm; etc.)

7.2.3 The trimming tolerance (e.g., ±0.1 percent; ±2 percent; ±10 percent; etc.)

7.2.4 Special requirements. Any special circuit or design requirements related to the trimming process (e.g., resistor tolerances ≥20 percent do not require trimming; resistors "hot trimmed" with the circuit operating to a specified circuit output voltage when required; etc.)

7.3 Identification of Trimming Method and Controls

The manufacturer shall identify:

7.3.1 The trimming method (e.g., laser trimming for thin film resistors; air abrasive trimming for thick film resistors; etc.)

7.3.2 Trimming controls.

a. Device parameter monitoring (e.g., 5-place digital ohmmeter continually observed by operator; automatic resistance monitoring to a preset tolerance; etc.)
b. Cleanliness (e.g., trimming shall be done in a controlled area; substrates shall be handled only with tweezers or gloves; after trimming, all parts are cleaned to remove any contamination, chips, etc. from the networks; etc.)
c. Equipment controls (e.g., digital ohmmeter or digital voltmeter calibrated every 120 working days; airbrasive nozzle size selected to match resistor; micrometer adjustments to control movement of part under laser beam; operator controls focus of laser beam; etc.)
d. Speed (e.g., table travel speed under nozzle or beam manually controlled by operator; etc.)
e. Optics (e.g., operator observes trimming operation under 7 X - 30 X magnification, etc.)

7.4 Documentation

The manufacturer shall furnish evidence of the following.

7.4.1 Specification control. Specification control of trimming process.

7.4.2 Test data. Test data showing the effects of the trimming process used on the part parameters (e.g., the resistor drift does not exceed 1.5 percent per 1000 hours when tested under burn-in conditions, etc.)

7.5 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance methods related to the following.

7.5.1 Visual inspection of trimmed part for workmanship (e.g., trimmed resistors examined under 30 X magnification for ragged trim line, trimming confined to designated area, physical damage due to trimming, impurities or foreign materials left after trimming; etc.)

7.5.2 Electrical (e.g., resistance value within specified limits as measured on a 5-place digital ohmmeter, etc.)

7.5.3 Inspection level (e.g., 100 percent of all trimmed resistors, etc.)

7.5.4 Packaging (e.g., trimmed substrates packaged individually in anti-static bags and stored in dry nitrogen cabinet until next operation, etc.)

7.5.5 Identification (e.g., trimmed substrates clearly identified by lot number and/or serial number to permit traceability, etc.)

7.6 Demonstration of Trimming Process

For each type of device to be trimmed and for each trimming method used, the manufacturer shall demonstrate, using documented procedures, the trimming process. This demonstration will consist of trimming 10 devices of each type within their specified tolerances, including a magnified visual examination after trimming and an electrical verification of the device values.

8.0 PARTS MOUNTING

8.1 Scope

This process step involves the methods, equipment, and controls used by the manufacturer to mount or attach discrete components to the substrate or package. More specifically this process step concerns the mounting of semiconductor chips, capacitor chips, resistor chips, etc. to the thin film or thick film substrate or to the package. In addition this process step also includes the mounting or attachment of the thick film or thin film substrate within the package enclosure, if applicable.

References: Figure 1 shows the position of the parts mounting step in relation to the overall hybrid microcircuit operation. The flow chart in Exhibit 4 (Appendix A) shows the specific position of the parts mounting steps in relation to the hybrid microcircuit assembly operation, together with the materials used and inspection stations. The manufacturer shall include a similar flow chart as part of his certification showing the various parts mounting steps in their proper sequence.

8.2 Identification of Parts to be Mounted and Configuration

The manufacturer shall identify the types of parts to be mounted:

8.2.1 Semiconductor chips (e.g., transistors; diodes; integrated circuits; etc.)

8.2.2 Passive device chips (e.g., capacitors; resistors; etc.)

8.2.3 Substrates, if applicable (e.g., thin film substrate; thick film substrate; etc.)

8.2.4 Configuration (e.g., regular face-up chips; beam lead chips; flip-chips; molytab-mounted chips; leadless inverted devices (LID); rectangular capacitor chips metalized on each end; etc.). A sketch of the particular chip configuration may be used for clarification. See Figure 2.

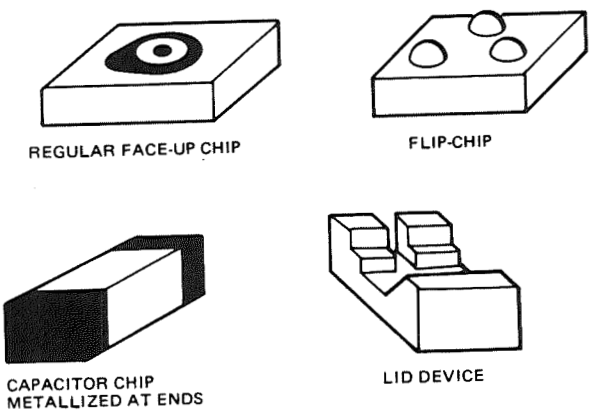


Figure 2. Chip configuration examples.

8.3 Identification of Mounting Material

The manufacturer shall identify the mounting materials used for each part type and part configuration to be certified. A sketch may be used for clarification. See Figure 3.

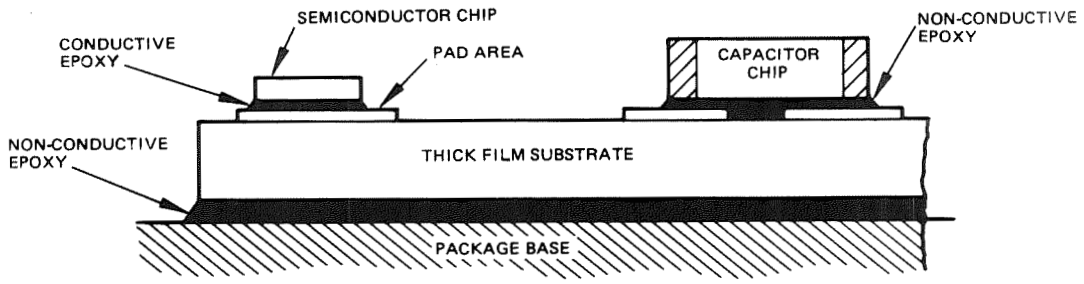


Figure 3. Illustration of materials used in mounting parts and substrates.

8.3.1 Semiconductor chips (e.g., conductive silver epoxy; etc.)

8.3.2 Passive device chips (e.g., non-conductive epoxy; etc.)

8.3.3 Substrates (e.g., non-conductive epoxy; etc.)

8.4 Identification of Mounting Method

The manufacturer shall identify the mounting method used for each part type and part configuration to be certified.

8.4.1 Semiconductor chips (e.g., operator manually positions chip on dot of conductive epoxy using vacuum pencil, the epoxy is subsequently oven cured; operator manually positions preform on bonding pad, molytab chip is automatically picked up and positioned over preform, parallel gap electrodes are positioned on ends of preform and current flows sufficiently to melt preform and form die bond; etc.)

8.4.2 Passive device chips (e.g., operator manually presses capacitor chip on spot of non-conductive epoxy using vacuum pencil, adhesive is subsequently oven cured; etc.)

8.4.3 Substrates (e.g., operator spreads non-conductive epoxy on package mounting area with special tool and on back of thin film substrate; operator then positions and presses substrate on mounting area using tipped tweezers; adhesive is subsequently oven cured; etc.)

8.5 Identification of Mounting Controls

For each combination of part type, configuration, material, and mounting method, the manufacturer shall identify the controls used for parts mounting. These controls shall include the following, if applicable.

8.5.1 Cleanliness (e.g., parts to be mounted shall be free of foreign material, corrosion, etc.; parts cleaned prior to mounting by immersion in boiling solvent followed by solvent rinse; etc.)

8.5.2 Ambient (e.g., parts mounting done in controlled area; chip die bonding done under nitrogen atmosphere at 2 cfm; etc.)

8.5.3 Temperature (e.g., oven temperature controlled to XXX° ± 3° C and calibrated every 3 months; etc.)

8.5.4 Time (e.g., adhesive cure time controlled to XX hours ± 2.5 hours; parallel gap pulse duration set at 1000 milliseconds; etc.)

8.5.5 Pressure (e.g., operator manually controls pressure by aided visual observation of adhesive fillet along perimeter of chip; etc.)

8.5.6 Voltage (e.g., voltage pulse preset at 0.55 volts on constant voltage power supply, etc.)

8.6 Identification of Material Controls

For each mounting material used, the manufacturer shall identify his material controls. These controls shall include the following, if applicable.

8.6.1 Composition (e.g., the non-conductive adhesive composition is XX pbw adhesive and XX pbw catalyst as weighed on a calibrated gram scale; the solder alloy composition is 60 Sn - 36 Pb - 4 Ag as determined by either wet-chemical or spectrochemical-analysis techniques per Methods 111.2 or 112.2 of Federal Test Method Standard No. 151; etc.)

8.6.2 Shear strength (e.g., the lap shear strength of the non-conductive adhesive shall be a minimum of 1900 psi when tested at room temperature per ASTM D1002; etc.)

8.6.3 Electrical resistivity (e.g., the electrical resistivity of the conductive adhesive shall not exceed 5×10^{-4} ohm-cm at 50 milliamps of current; etc.)

8.6.4 Outgassing (e.g., the conductive adhesive shall not release visible condensable material during 5 days exposure to +160° C under 1×10^{-6} torr vacuum, etc.).

8.7 Documentation

The manufacturer shall furnish evidence of the following.

8.7.1 Process documentation (e.g., parts mounting by non-conductive adhesive is covered by process specification HP XXXX and by Process

Instruction PI XXXX; eutectic die bonding to Molytabs covered by process specification HP XXXX and by Process Instruction PI XXXX; etc.)

8.7.2 Test data. Test data showing that parts mounted by the manufacturer's processes are capable of passing the environmental test procedures listed in Table 9.

Table 9. Environmental test procedures.

Test	Reference	Method	Condition
High Temp. Storage	MIL-STD-883	1008	B
Temp. Cycling (1)	MIL-STD-883	1010	B
Mech. Shock (2)	MIL-STD-883	2002	B
Acceleration (2)	MIL-STD-883	2001	B
Thermal Shock (1)	MIL-STD-883	1011	A
Seal	MIL-STD-883	1014	A and C

(1) Either temperature cycling or thermal shock may be specified.

(2) Either mechanical shock or acceleration may be specified.

8.8 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance methods related to the following.

8.8.1 Visual inspection of mounted part (e.g., 100 percent inspection of all mounted parts at 30 - 50 X magnification to determine compliance with workmanship requirements and visual acceptance criteria, including orientation, tilt, cracks or breaks in chip or substrate, excessive material flow, adequate bond fillet, cleanliness, and potential electrical shorts; etc.)

8.8.2 Strength (e.g., the strength of a eutectic die bonded chip shall be a minimum of 300 grams when subjected to a shearing load per MIL-STD-883, Method 2011, Condition F, etc.)

8.8.3 Electrical (e.g., the saturation voltage of the mounted chip when tested per MIL-STD-750B, Method 3071 shall not exceed the rated value for that particular chip type, etc.)

8.9 Demonstration of Parts Mounting

For each combination of part type, configuration, material, and mounting method to be certified, the manufacturer shall demonstrate, using documented procedures, the parts mounting operation. This demonstration shall consist of mounting 3 parts of each type, configuration, and material showing the controls used. These parts shall be visually inspected under 30 - 50 X magnification and mechanically and/or electrically tested, if applicable, to demonstrate the integrity of the parts mounting process.

9.0 INTERCONNECT BONDING

9.1 Scope

This process step includes those materials, processes and controls involved in electrically interconnecting active and passive chip components to the bonding pads of the substrates, to the output leads (or pins) of the package, or to each other. This step also includes the materials, processes and controls involved in electrically interconnecting the input-output circuitry on the substrate to the leads (or pins) of the package. More specifically this process step includes such processes as: thermocompression wire bonding, ultrasonic wire bonding, flip-chip bonding, beam-lead bonding, microsoldering, parallel gap welding, etc.

References. Figure 1 shows the position of the interconnect bonding step in relation to the overall hybrid microcircuit operation. The flow chart in Exhibit 4 (Appendix A) shows more specifically the interconnect bonding processes (i.e., thermocompression and ultrasonic wire bonding) and the applicable wire types in relation to a typical hybrid microcircuit assembly process. The manufacturer shall include a similar flow chart as part of his certification showing the interconnect bonding processes and materials in their proper sequence.

9.2 Identification of Bond Types

The manufacturer shall identify each type of interconnect bonding to be certified. A sketch of the particular bond types to be certified may be used for clarification since it is realized that a manufacturer may use many

combinations of interconnect bonding techniques and materials in a single hybrid. See Figure 4.

9.2.1 Type of lead or interconnect (e.g., flying wire; beam lead; flip chip; etc.)

9.2.2 Lead or interconnect material (e.g., aluminum wire; gold wire; gold beam; solder bump; silver-filled conductive epoxy; etc.)

9.2.3 Interconnect technique (e.g., ultrasonic bond; thermocompression ball bond; solder reflow; conductive adhesive; wobble bond; etc.)

9.2.4 Main usage of each interconnect bonding process (e.g., face-up semiconductor chips ultrasonically bonded to thin film circuitry using 1-mil aluminum wire; capacitor chips thermocompression ball bonded to thick film circuitry using 2-mil gold wire; etc.)

9.3 Identification of Interconnect Bonding Material Controls

The manufacturer shall identify the controls used for each of the interconnect bonding materials to be certified. These controls shall include the following, if applicable.

9.3.1 Size (e.g., gold wire 0.002 ± 0.0002 inch in diameter as determined by weighing a 20 cm length on an analytical balance accurate to 0.01 milligram, the specimen shall weigh 7.82 milligrams ±10 percent; aluminum wire 0.001 ± 0.0001 inch in diameter as determined by weighing a 100 cm length on an analytical balance accurate to 0.01 mg., the specimen shall weigh 1.370 mg. ± 10 percent; etc.)

9.3.2 Composition (e.g., aluminum wire with 0.8 - 1.2 percent silicon as determined by chemical or spectroscopic analysis per Method 111 or Method 112 of Federal Test Method Standard 151; gold wire 99.99 percent minimum purity as determined by spectroscopic analysis per Method 112 of Federal Test Method Standard 151; etc.)

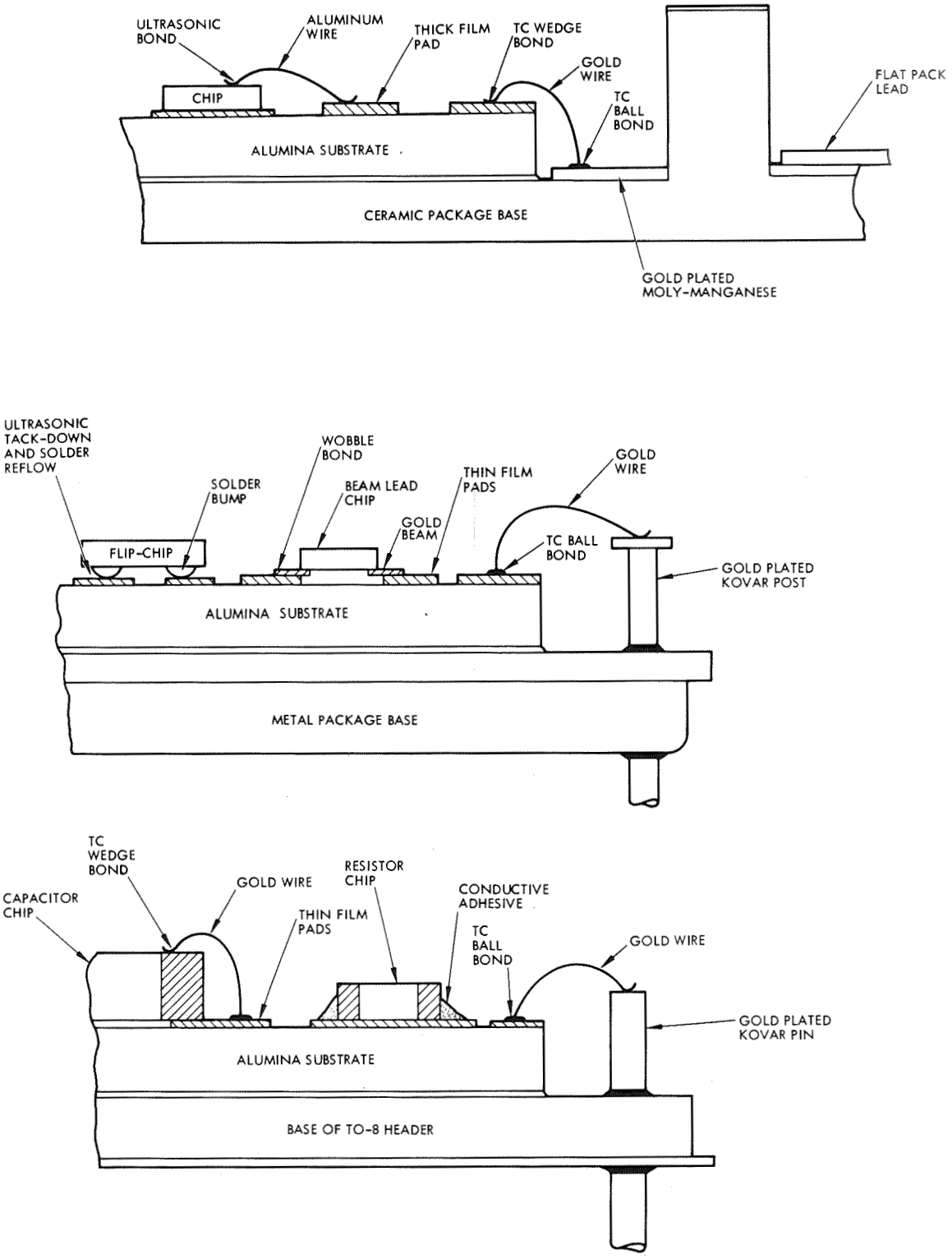


Figure 4. Sketches showing typical bond types, materials, and techniques which might be used in the interconnection of hybrid microcircuit components.

9.3.3 Elongation and/or breaking strength (e.g., breaking strength of 1-mil aluminum wire to be 15 - 18 grams as determined by testing 3 specimens per ASTM-E-8 using a 10-inch gauge length; elongation of 2-mil gold wire to be from 3 to 8 percent as determined by testing 3 specimens per ASTM-E-8 using a 10-inch gauge length; etc.)

9.3.4 Workmanship (e.g., each spool of wire shall be visually examined for kinks, nicks, corrosion, foreign material, and proper spooling, etc.)

9.3.5 Storage (e.g., except when in use, spooled wire shall be stored under dry nitrogen atmosphere at 6 - 10 cubic millimeters per minute flow rate or in a plastic cabinet with dessicant; etc.)

9.4 Identification of Bonding Controls

For each combination of interconnect bonding technique and material to be certified, the manufacturer shall identify the controls used.

9.4.1 Bond schedules (e.g., optimum bond schedules are determined for each material combination by means of isostrength or isoforce diagrams, process control limits to be calculated from a sample of 25 bonds using a 3 sigma lower control limit; etc.)

9.4.2 Pressure or force (e.g., tip pressure set at 27 grams to comply with bonding schedule using a 0 - 50 gram gauge, etc.)

9.4.3 Time or duration (e.g., Channel 1 and Channel 2 time controls set at 2.0 to comply with bonding schedule; time-at-temperature set to comply with bonding schedule; etc.)

9.4.4 Power, voltage, or current, if applicable (e.g., power control set at 2.5 to comply with bonding schedule; etc.)

9.4.5 Temperature, if applicable (e.g., tip temperature control set at 31 to comply with bonding schedule; stage temperature set at 300°C; etc.)

9.4.6 Calibration or tuning (e.g., bonder calibrated prior to each new set-up and every 4 hours when in use; bonder re-calibrated after any change in operating conditions, such as tip replacement or moving equipment to a new location; etc.)

9.4.7 Ambient (e.g., no special ambient used; bonding done under nitrogen blanket at 2 cfm; etc.)

9.4.8 Cleanliness (e.g., at the beginning of each shift, the bonder shall be completely wiped down to remove all dust particles and surface contamination, the bonding tip shall be cleaned with lens tissue moistened in methyl alcohol and blown dry with nitrogen; the operator shall wear finger covering during all lead bonding operations in which fingers come in contact with the bonding wire, wire spool, bonding tip, bonding stage, or substrates; flux removal shall be accomplished by successive rinses with light brushing in flux remover, methyl alcohol, and special solvent until all residues are completely removed as determined by a 20 X magnification visual examination; etc.)

9.5 Documentation

The manufacturer shall furnish evidence of the following.

9.5.1 Process documentation (e.g., ultrasonic bonding processes documented by process specification HP XXXX and process instruction PI XXXX; thermocompression bonding processes documented by process specification HP XXXX and process instruction PI XXXX; etc.)

9.5.2 Visual inspection criteria. Visual inspection criteria shall be available, such as sketches or photographs, for each type of interconnect bonding to be certified showing acceptable and rejectable conditions where applicable.

9.5.3 Environmental test data. Test data showing that parts interconnected by the bonding process to be certified are capable of passing the environmental tests listed in Table 9 (Section 8.7).

9.5.4 Time-temperature test data. Test data showing the effects of time and temperature on the strength and/or resistance of the interconnect bonding process (e.g., no evidence of thermocompression bond strength degradation after 1500 hours at +150° C; 46.8 percent decrease in ultrasonic bond strength after 400 hours at +150° C; etc.)

9.5.5 Current fatigue test data. Test data, if available, showing the effects of current fatigue on wire bonds (e.g., no failures after 15,000 cycles at 50 milliamperes on 1-mil aluminum wire ultrasonically wire bonded to transistor chips with current cycled on and off at 2-minute intervals, chips operating at maximum rated power; etc.)

9.6 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance methods related to the following.

9.6.1 Visual inspection of interconnect bonds (e.g., 100 percent pre-seal visual inspection at 30 - 50 X magnification per visual acceptance criteria for requirements such as lifted bonds, excessive deformation, misalignment, excessive sag, etc.; 100 percent internal visual inspection per MIL-STD-883, Method 2010, Condition B; etc.)

9.6.2 Bond strength (e.g., pull tests for bonds shall be performed per MIL-STD-883, Method 2011, Condition C using a special pull test fixture with the direction of pull normal to the substrate and with a pull rate not exceeding 1 foot/minute, at least 3 pull test specimens shall be made at the start of each working shift and at no more than 4-hour intervals during the working shift, the breaking strength shall be recorded and compared with the control limits, the failure mode shall also be recorded; etc.)

9.6.3 Interconnect bond resistance, if applicable (e.g., bond resistance shall be determined at a current of 10 milliamperes using a four-point probe test setup, the total resistance shall be less than 0.1 ohms; etc.)

9.6.4 In-line screening tests, if applicable (e.g., prior to sealing, each assembled hybrid is submitted to 5 impact shocks at the 2500 G level in the

Y1 direction; prior to sealing, each assembled hybrid is submitted to a 30 second nitrogen blast per MIL-STD-883, Method 2011, Condition E with the nozzle positioned 1 - 2 inches from the package at an air pressure of 25 ± 5 psig; etc.)

9.7 Demonstration of Interconnect Bonding

9.7.1 Interconnect bonding technique. For each combination of interconnect bonding technique and material to be certified, the manufacturer shall demonstrate, using documented processes, the interconnect bonding operation and the controls used. At least 20 bonds of each type shall be made and inspected per the manufacturer's visual acceptance criteria. Verification of the integrity of the interconnect bonding process shall be done by electrical and/or mechanical tests, such as resistance measurements or in-line screening tests (e.g., impact shock, gas blast, etc.). The demonstration may be done on actual hybrid microcircuits or on suitable test patterns which are representative of production hybrids.

9.7.2 Bond strength testing. The manufacturer shall demonstrate his method for bond strength testing and data recording by testing at least 10 bonds of each type.

10.0 PACKAGE SEALING

10.1 Scope

This process step involves the sealing of the hybrid microcircuit package after the pre-seal visual inspection. Included in this process step is the actual sealing operation, post-seal inspection, leak testing, and cleaning, if required.

References. Figure 1 shows the position of the package sealing step in relation to the overall hybrid microcircuit operation. The flow chart in Exhibit 4 of Appendix A shows the specific position of this step in relation to the assembly process. The manufacturer shall include a similar flow chart as part of his certification showing the package sealing steps which he uses, in their proper sequence.

10.2 Identification of Package Type to be Sealed

The manufacturer shall identify the types of packages to be sealed and their materials.

10.2.1 Package type (e.g., ceramic flatpack; TO-8 header; all-metal plug-in package; etc.)

10.2.2 Package sealing surface (e.g., gold plated sealing surface which has been pretinned; gold plated Kovar; etc.)

10.2.3 Lid or cover material (e.g., tin plated iron-nickel-cobalt alloy cover; nickel cover; etc.)

10.3 Identification of Sealing Material

The manufacturer shall identify the sealing material.

10.3.1 Sealing material (e.g., SnXX solder per QQ-S-571, form W, type S; cap welded, no sealing material used; etc.)

10.4 Identification of Sealing Method

The manufacturer shall identify the sealing method.

10.4.1 Method (e.g., soldered manually with soldering iron, no flux used; resistance weld; etc.)

10.5 Identification of Sealing Controls

The manufacturer shall identify the controls used in each sealing process to be certified.

10.5.1 Cleanliness (e.g., lids cleaned prior to sealing by solvent degrease for 5 minutes and +150° C bake for 10 minutes; parts handled with gloves, finger cots or tweezers; all sealing surfaces free from organic matter and corrosion products; etc.)

10.5.2 Pre-seal bake (e.g., packages and covers baked for X hour at XXX° C ±5° C in dry nitrogen flowing at a rate of 2 cfm; etc.)

10.5.3 Sealing ambient (e.g., sealing done in glove box under dry nitrogen with a flow rate of 1 cfm and a dew point equal to or less than -40° C as determined by an Alnor 7000 U Dew Pointer; etc.)

10.5.4 Sealing schedule (e.g., weld schedule for sealing caps to TO-8 headers is controlled by setting electrode alignment, head pressure, approach speed, squeeze rate, holding time, and voltage in accordance with pre-established set-up schedules; sealing of lids to pretinned flatpacks is done manually using a special holding and clamping fixture and a 60-watt temperature-controlled soldering iron, the operator visually observes the solder fillet formation; etc.)

10.6 Leak Testing

The manufacturer shall identify the method or methods used for gross and fine leak testing to verify the integrity of his sealing process. The manufacturer shall indicate whether leak testing is done in-house or by an outside testing laboratory.

10.6.1 Fine leak test (e.g., fine leak test done in-house per MIL-STD-883, Method 1014, Condition A, exposure pressure is 30 psig for a minimum of 2-1/2 hours; etc.)

10.6.2 Gross leak test (e.g., gross leak test done in-house per MIL-STD-883, Method 1014, Condition C; only gross leak step 1 is performed; etc.)

10.6.3 Leak test controls

a. Cleanliness (e.g., all packages cleaned in solvent after gross leak testing, etc.)
b. Temperature (e.g., temperature of FC-43 fluid controlled to +125° C ± 5° C, etc.)
c. Calibration of leak detector (e.g., helium leak detector calibrated daily using sensitivity calibrator, etc.)

10.7 Documentation

The manufacturer shall furnish evidence of the following.

10.7.1 Process documentation (e.g., header capping documented by process specification HP XXXX and process instruction PI XXXX; solder sealing documented by process specification HP XXXX and process instruction PI XXXX; hermeticity leak testing documented by process instruction PI XXXX; etc.)

10.7.2 Test data. Test data showing that sealed packages are capable of withstanding the environmental tests listed in Table 9 (Section 8.7). The maximum leak rate after environmental testing shall not exceed 5×10^{-7} atmospheres cc/sec.

10.8 Inspection and Quality Assurance

The manufacturer shall identify his inspection and quality assurance methods related to the following.

10.8.1 Post-seal external visual inspection.

a. Inspection level (e.g., 100 percent inspection, etc.)
b. Magnification (e.g., 20 X binocular microscope, etc.)
c. Workmanship (e.g., bent, twisted, or nicked leads; dents, cracks, or scratches in package base or lid; solder splashes or smears; excessive weld flow or spikes; lid tilted, warped, or misaligned; cracks, pinholes, voids, bulges, or other irregularities in solder fillet; etc.)

10.8.2 Hermeticity (e.g., all packages shall have a measured leak rate less than 5×10^{-7} atmospheres cc/sec., etc.)

10.8.3 Sealing (e.g., prior to the actual sealing operation, 5 dummy packages shall be sealed, visually examined and leak tested, failure of any part shall be cause for realignment or readjustment of the welding electrodes; etc.)

10.8.4 Rework (e.g., any package not meeting the visual criteria or leak rate requirement is resealed and retested; etc.)

10.9 Demonstration of Package Sealing and Leak Testing

For each combination of package type, sealing material, and sealing method to be certified, the manufacturer shall demonstrate, using documented

procedures, the package sealing operation and controls used including pre-seal baking (if applicable) and both fine and gross leak testing. At least 10 packages of each combination shall be sealed, leak tested, and visually inspected under 20 X magnification. No more than 2 packages shall fail the leak tests or visual examination. All failed packages must be reworked, leak tested, and visually examined without failure.

APPENDIX A

EXHIBITS

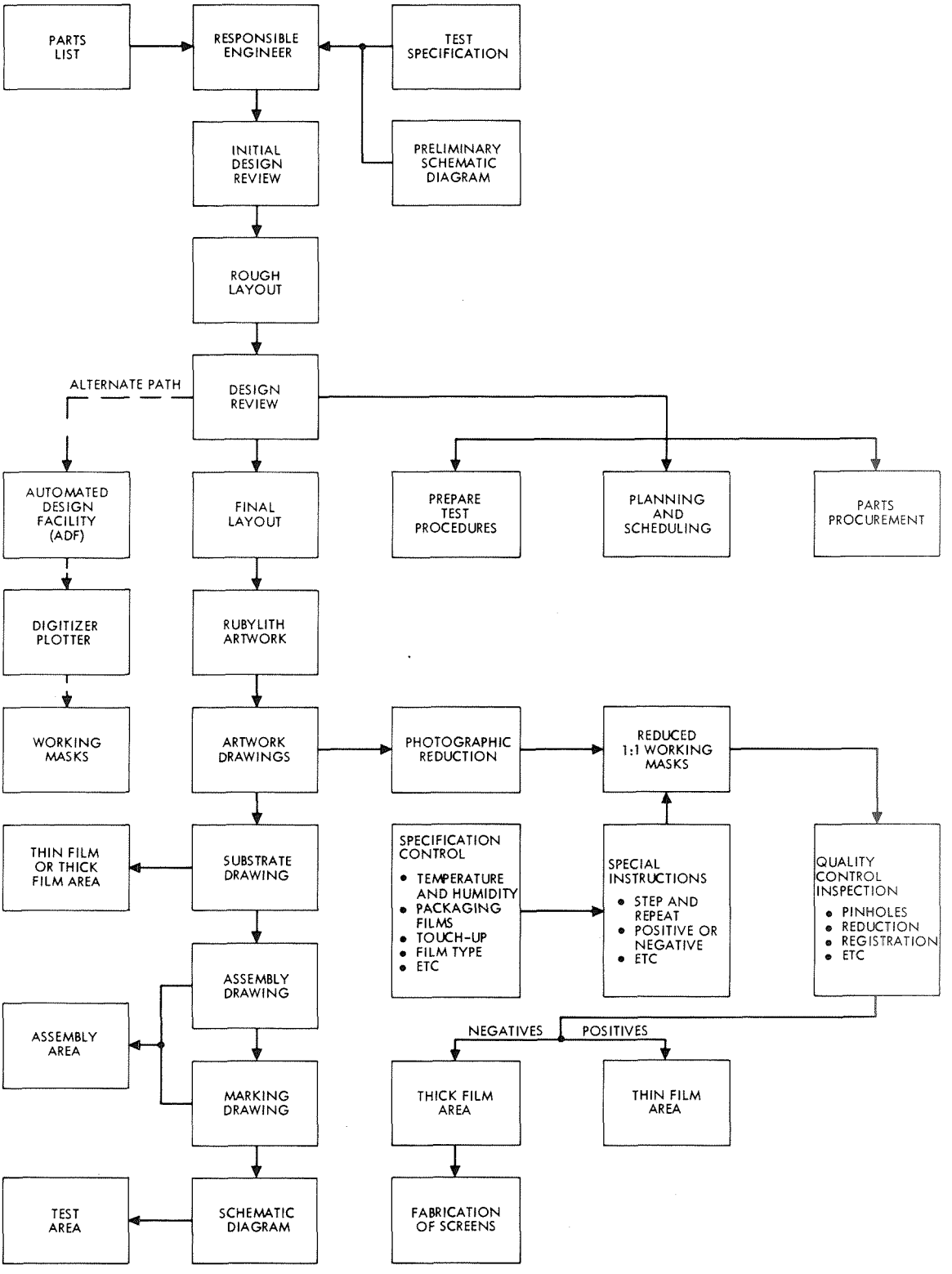


Exhibit 1. Typical sequence of events for making a hybrid design and layout resulting in a set of manufacturing engineering drawings and the required 1:1 working masks.

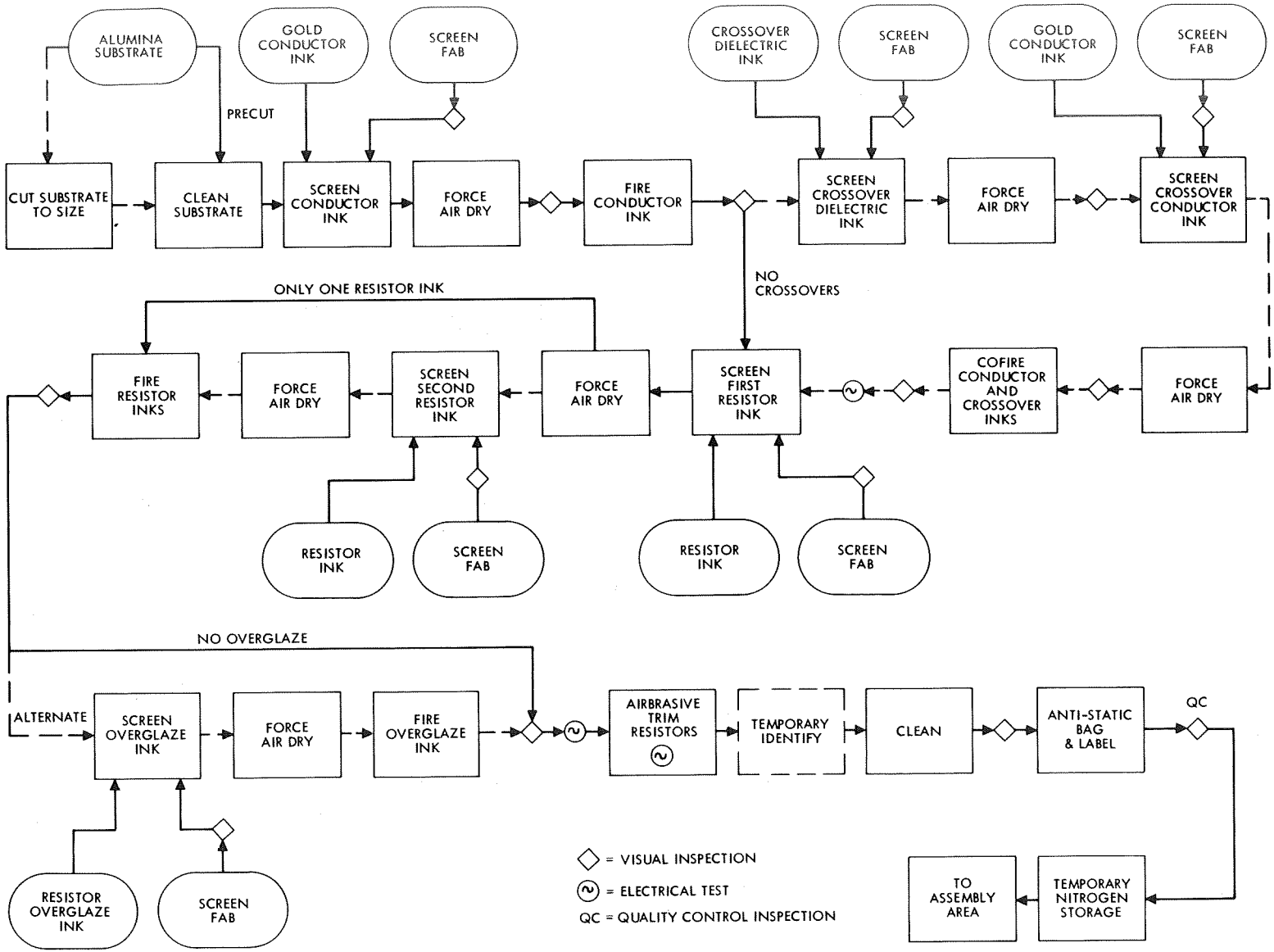


Exhibit 2. Flow chart of typical thick film hybrid microcircuit processing.

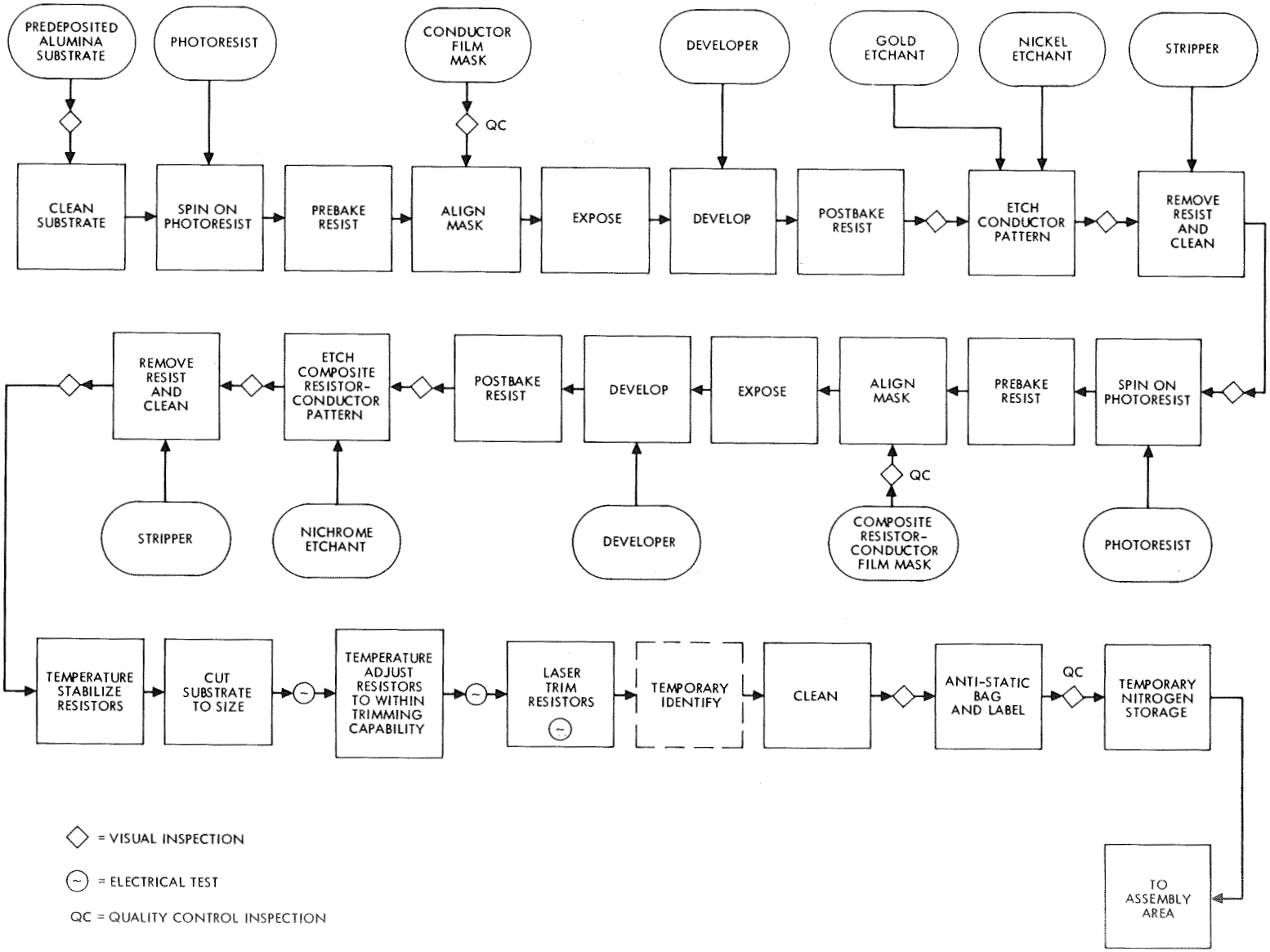


Exhibit 3. Flow chart of typical thin film hybrid microcircuit processing.

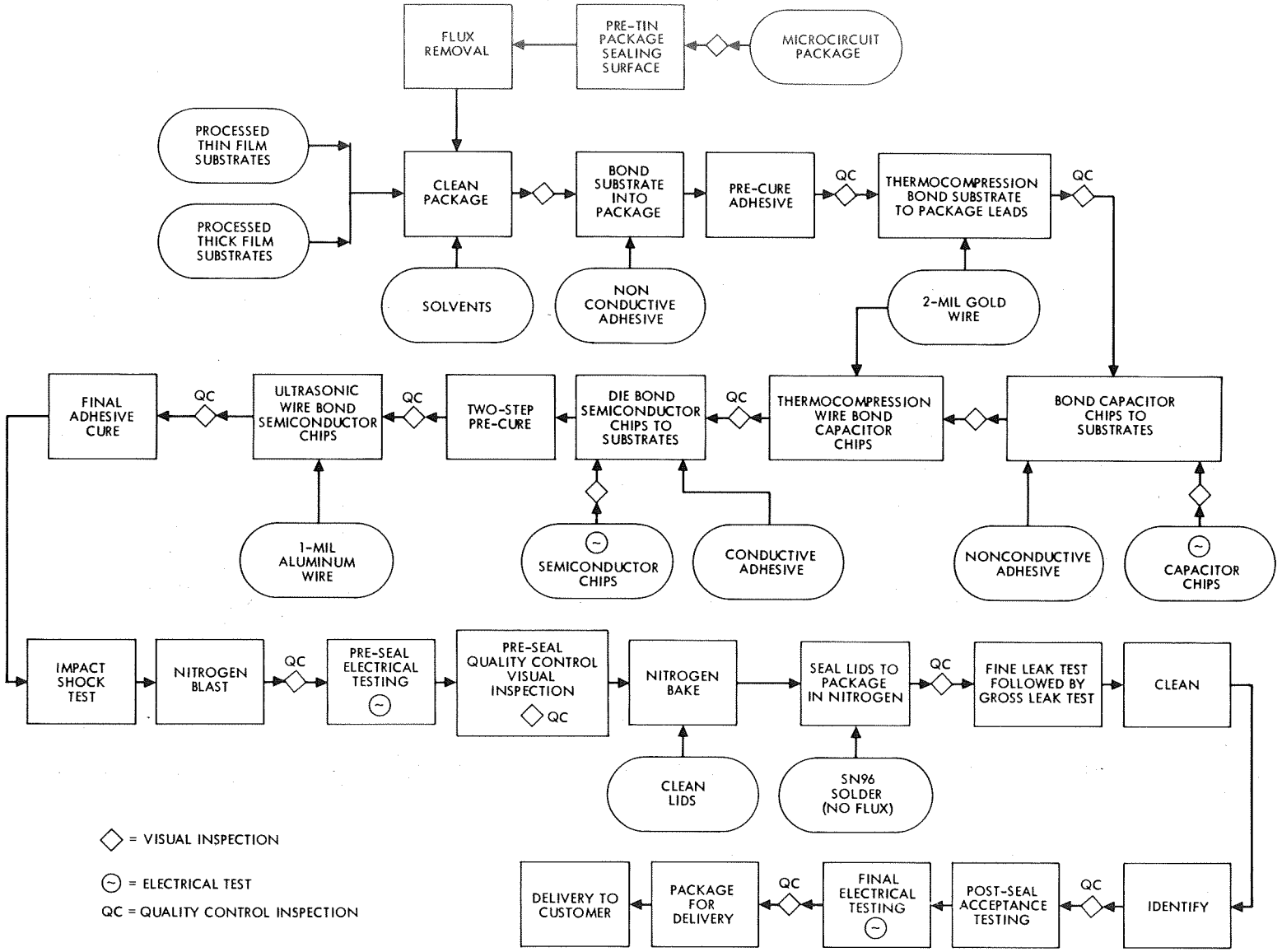


Exhibit 4. Flow chart of typical hybrid microcircuit assembly.

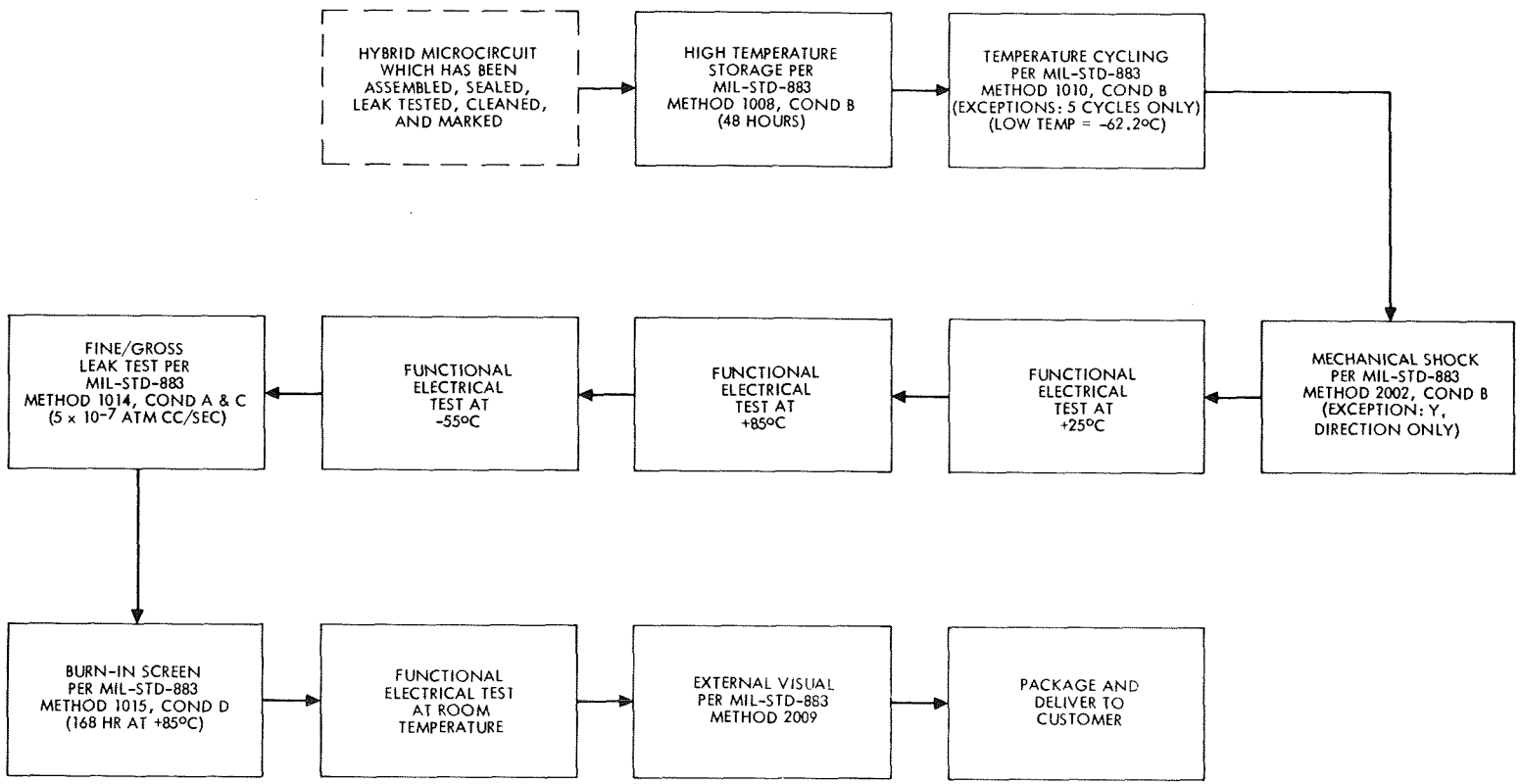


Figure 5. Flow chart of typical acceptance test procedure. These tests and test procedures may vary depending upon particular program requirements.

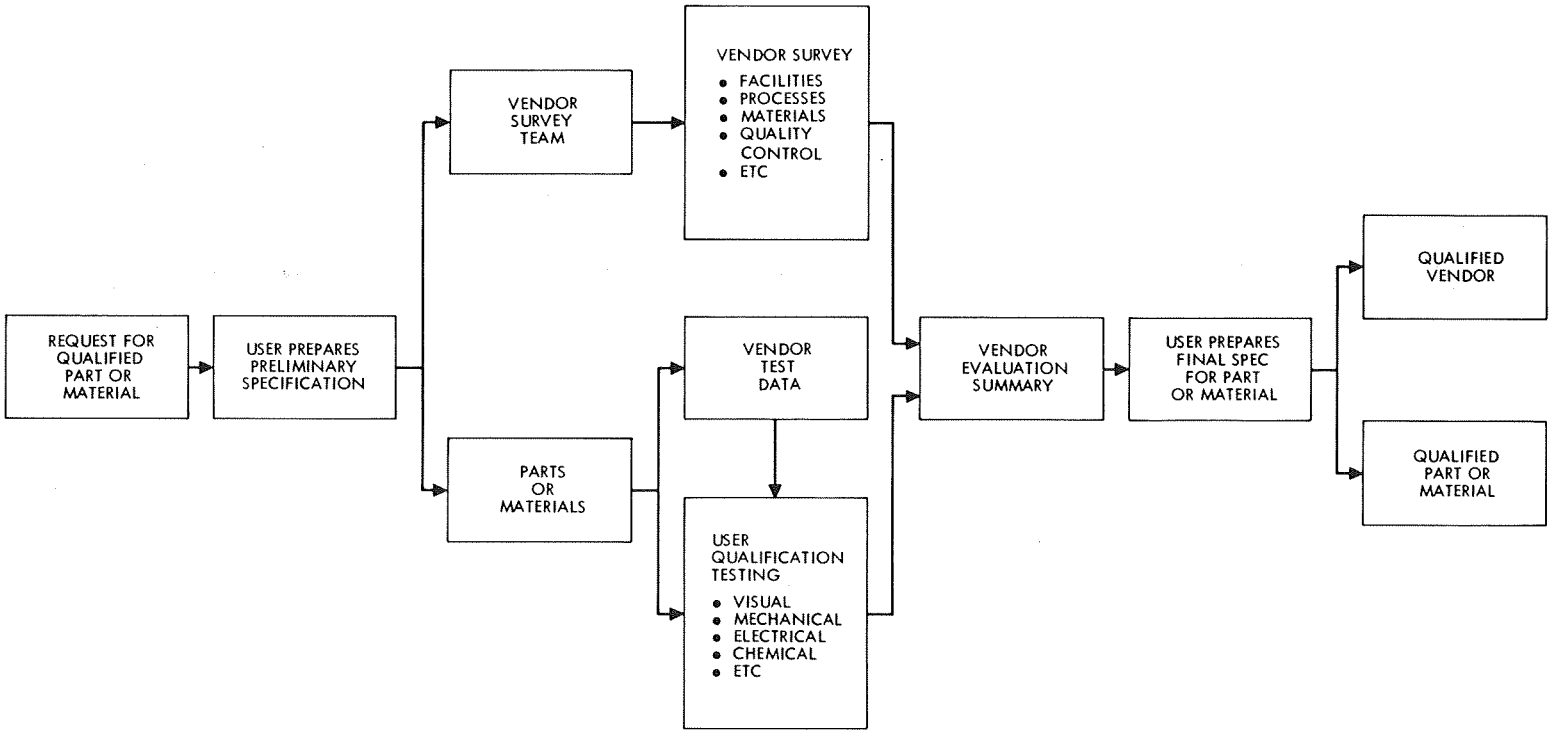


Exhibit 6. Flow chart showing typical steps taken to ensure that the vendor and his part or material will meet hybrid microcircuit requirements.

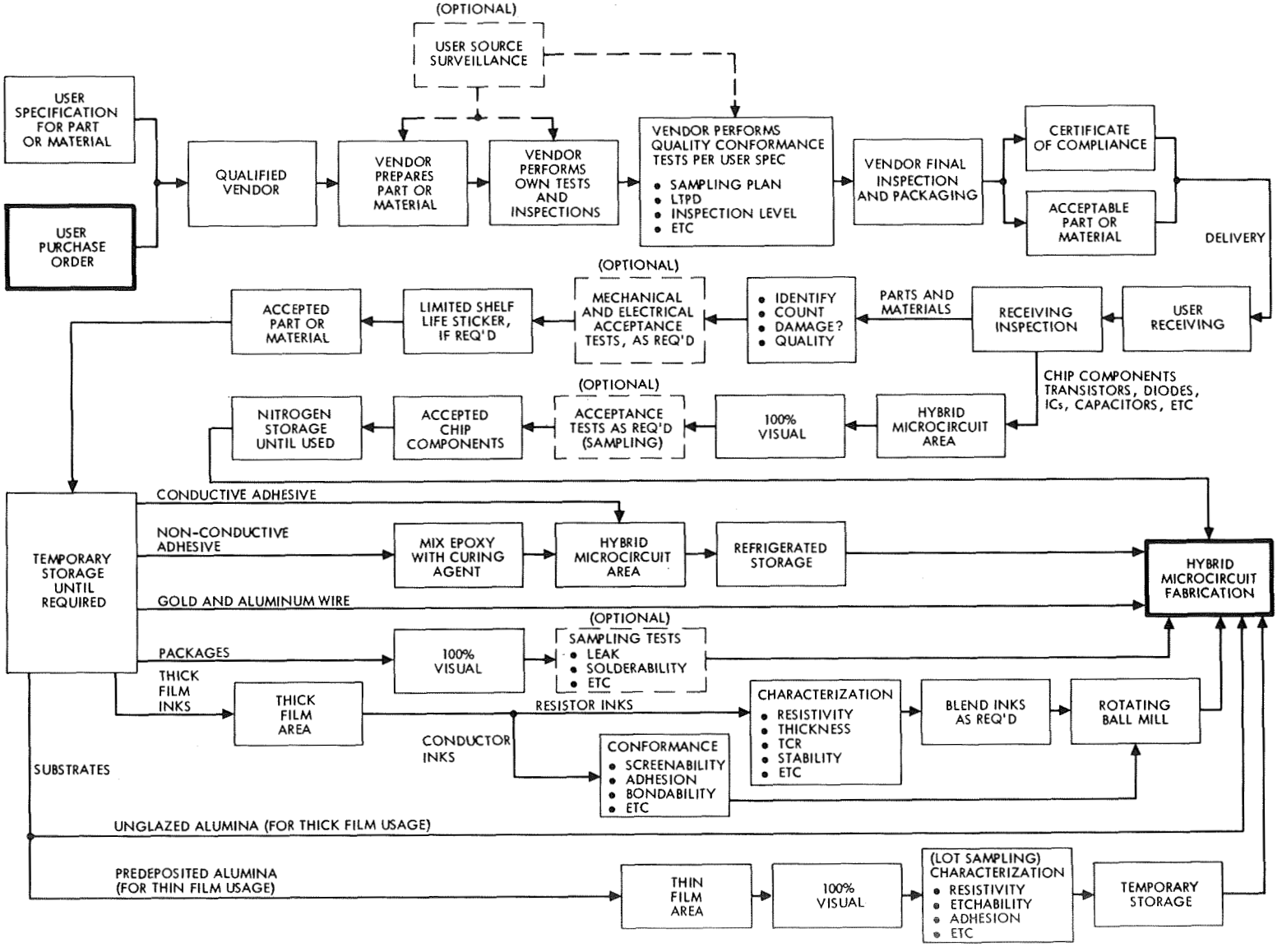


Exhibit 7. Typical flow chart illustrating user quality control over certain critical vendor-purchased parts and materials used in the fabrication of hybrid microcircuits.

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