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Final Report

VOLUME I

ESTABLISHING AN ELECTRICAL TEST PHILOSOPHY FOR LSI MICROCIRCUITS

February 1971

GRUMMAN

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During the course of this project, the authors have been privileged to visit over thirty (30) semiconductor manufacturing and user companies (see Appendix B) to discuss a great variety of problems related to this project with the engineering and managerial personnel of these companies.

Practically without exception, we received outstanding cooperation from all the organizations contacted. On our visits to Collins Radio, Fairchild Semiconductor, Texas Instruments, and Univac Division of Sperry to name but a few, key personnel in a wide variety of specialized areas generously rendered their time and experience to us. To all those persons we are deeply indebted and it is our sincere pleasure to acknowledge this fact.

In the process of executing this project and preparing the report, considerable effort and perseverance was expressed by the multi-talented Grumman engineer, R. Bisey, to whom we would like to express our thanks.

The authors

TABLE OF CONTENTS

VOLUME I

TABLE OF CONTENTS (Continued)

VOLUME II

LIST OF ILLUSTRATIONS

VOLUME I

LIST OF TABLES

VOLUME I

VOLUME II

1. INTRODUCTION

1.1 Objective of Report

This document consists of two volumes and is intended to serve as a guideline for the electrical testing of high-reliability Large Scale Integrated (LSI) bipolar and MOS Microcircuits. The scope of this guideline includes the areas of functional and parametric electrical testing of LSI devices. The user of these devices must gain as much meaningful performance and reliability data on the device as practicable prior to system installation. Since the user will usually only test the package device, he is limited, therefore, as to the types of tests and the extent to which these tests can be performed on the unit. As the major mode of testing LSI circuits is primarily electrical in nature, the interpolation and extrapolation of functional and parametric electrical test data used to assist the user in the evaluation of device performance degradation and latent failure mechanisms is very desirable.

This study has two overall objectives. First, to identify Metal Oxide Semiconductor (MOS) and Bipolar LSI electrical parameters and assess their usefulness for measuring functional performance and their capability to detect mechanisms of failure and performance degradation. Secondly, the study will establish an LSI electrical test philosophy and testing techniques for MOS and Bipolar LSI.

1.2 Organization of Tasks

In Volume I, a preliminary study on various contemporary LSI testing techniques was conducted. These techniques were categorized into logic type (combinatorial and sequential), and types of electrical testing (functional and parametric). First, electrical parameters specified on each type of LSI device were listed and the parameters specified by each manufacturer were tabulated. A complete listing of 38 LSI manufacturers and users was then compiled and categorized and a questionnaire outlining areas of specific interest was written and forwarded. A study was made of available data, failure analysis reports, technical journals, and in-house user experience. A study was also made of available LSI test equipment. The electrical parameter test philosophy included an evaluation of all parameters specified to assess how useful each is in predicting the performance and reliability of the device.

In Volume II, specific guidelines are developed for high-reliability testing at the wafer and package levels. Functional and parametric testing is discussed and recommendations are made for MOS and bipolar devices. Finally, specifications for an LSI test system are outlined and a scope for future work is presented.

2. MANUFACTURERS AND USERS OF LSI MICROCIRCUITS

The evolution of LSI has resulted in a pressing need for a different approach to device design, testing, and utilization. The delineations that once separated manufacturer and user are no longer apparent. State-of-the-art LSI devices are "systems on a chip" and, as a result, device manufacturers cannot use discrete device concepts when designing LSI circuits. Also, the users have had to apprise themselves of device technology in order to make intelligent tradeoffs when deciding what technology best suits their system requirements. Unfortunately, neither user nor manufacturer have fully appreciated the task of LSI testing. The device manufacturer, beset by low yields and a dynamic technology, is not eager to stress his devices too vigorously from the initial wafer fabrication to the final packaging stage for several reasons. For one, he cannot survive with too low a yield and often feels that overly comprehensive testing will destroy good devices with no tangible increase in reliability. The manufacturer, therefore, will usually establish his own general electrical test scheme as part of device qualification and will, happily or unhappily, test anything else the user desires to evaluate, provided that the user is prepared to pay for such services. The user is typically not familiar enough with the technology of his device to be able to develop a meaningful, comprehensive, and efficient test scheme: usually, his only recourse is to write a "spec to protect." He develops such a

rigorous test program that only a very few devices per wafer can be qualified. The need for an interpretive approach to testing is, therefore, quite apparent. Without a properly defined test interface between vendor and customer, overtesting and high cost inevitably result.

In this study, many manufacturers and users of LSI were visited for the purpose of discussing this testing interface. The proliferation of companies, products, and process techniques provided a broad information base. Table 2-1 lists several manufacturers and users with brief descriptions of their product activity and test capability. A list of addresses for these companies is included in Appendix B. Figures 2-1 through 2-6 picture various MOS and Bipolar LSI devices which include Read only Memories, Random Access Memories, and Shift Registers.

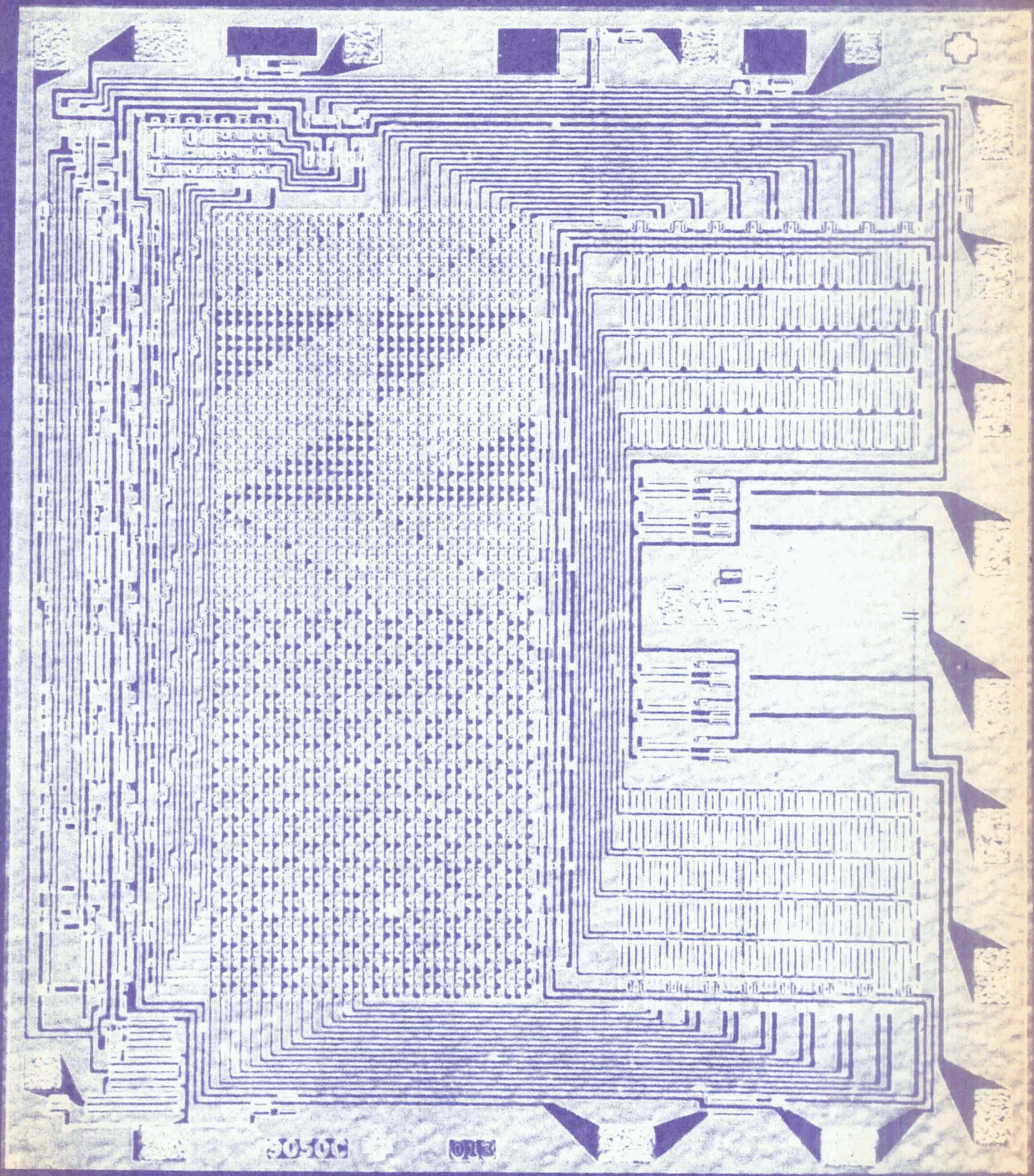


Figure 2-1. American Microsystems 2048x1 ROM

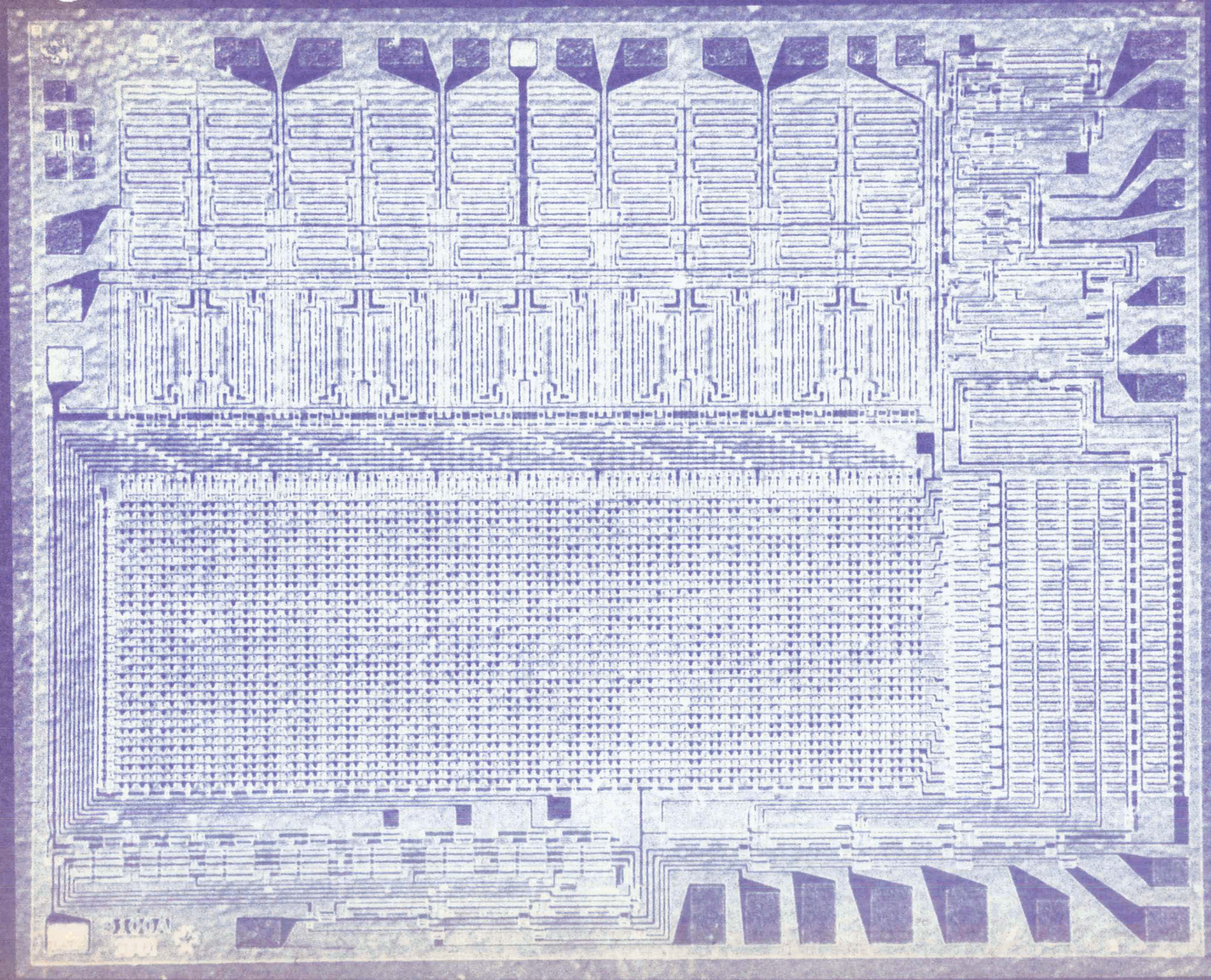


Figure 2-2. American Microsystems 256x10 ROM

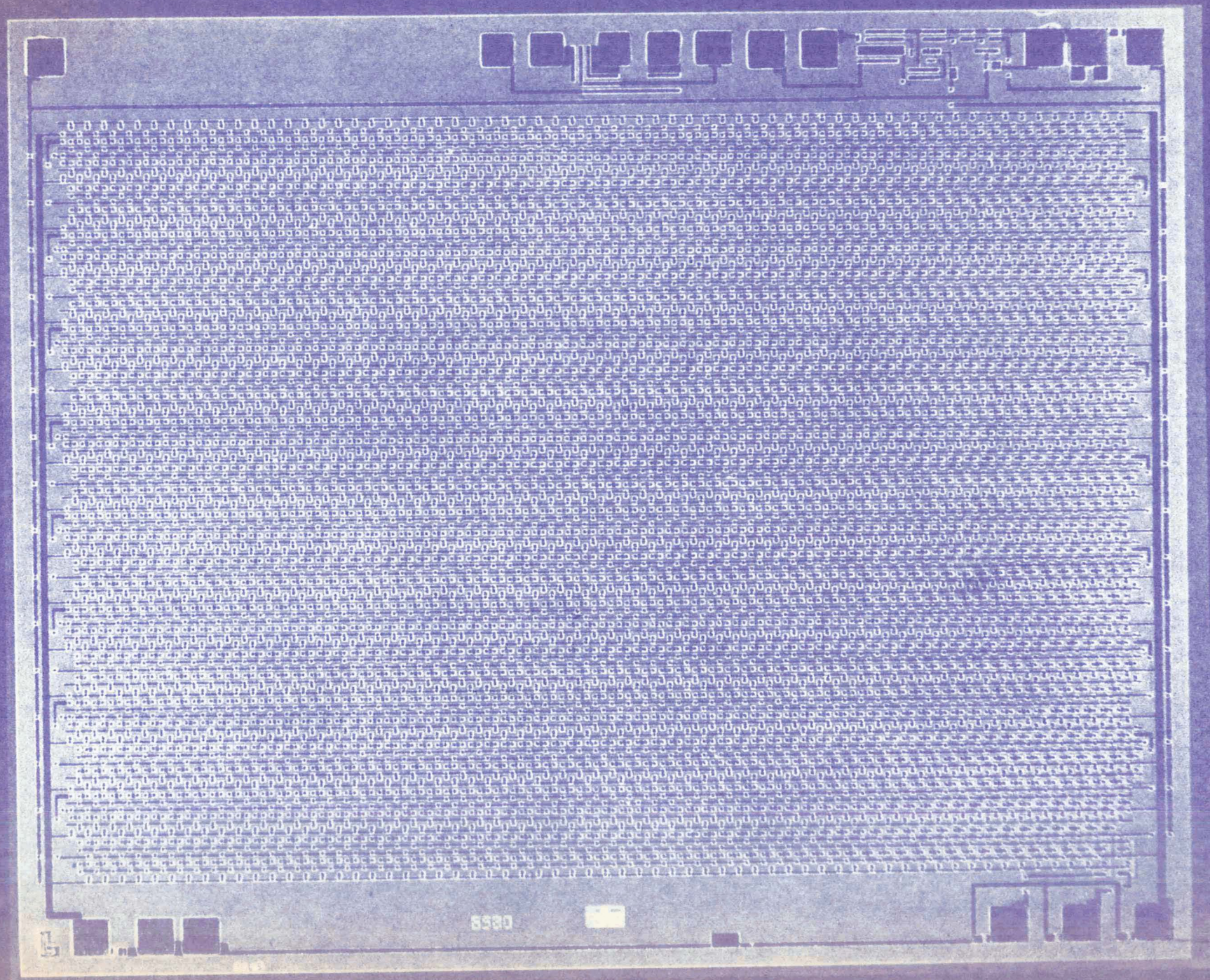


Figure 2-3. Collins 1024-Bit Shift Register

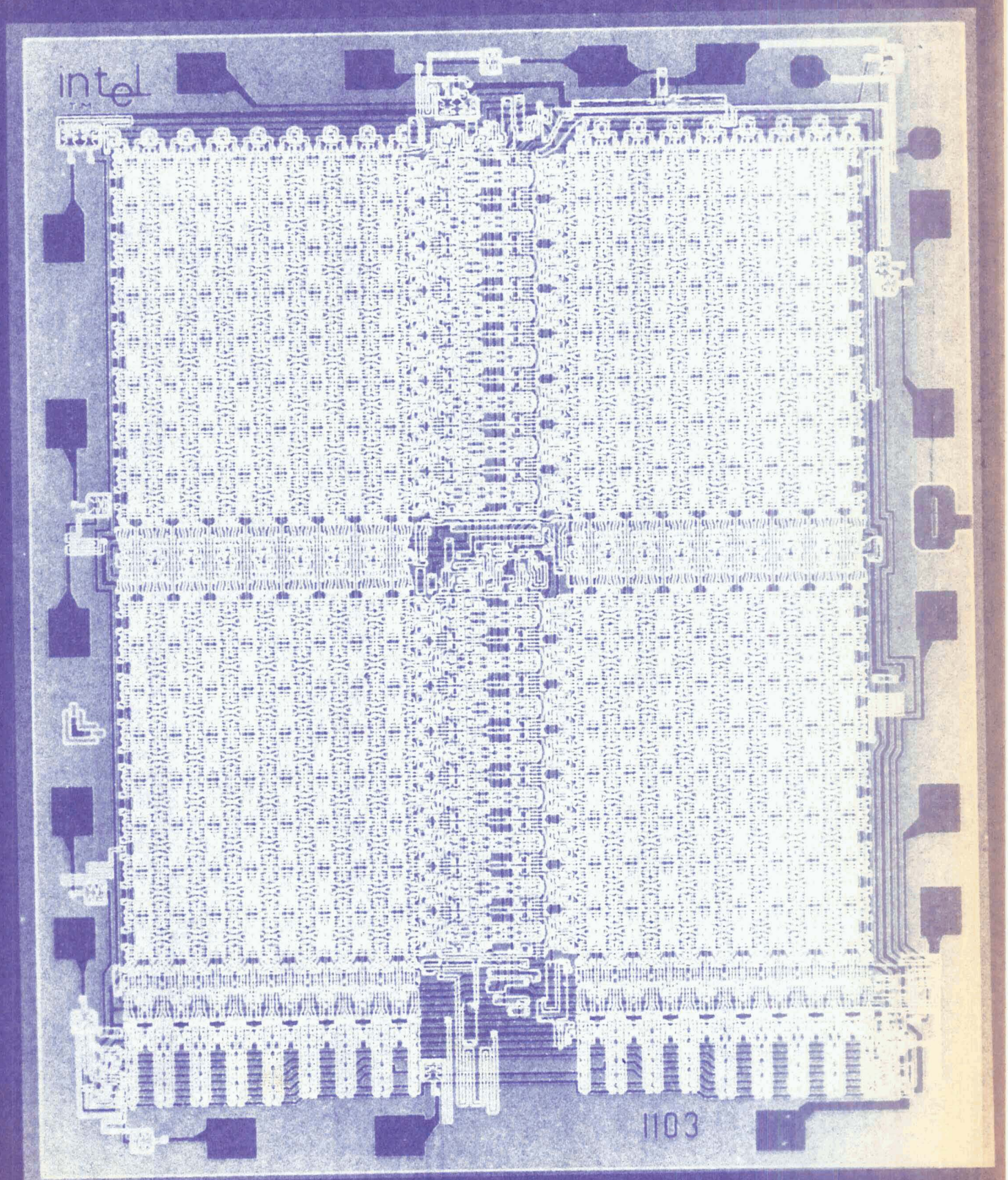


Figure 2-4. Intel 1024-Bit Dynamic MOS RAM

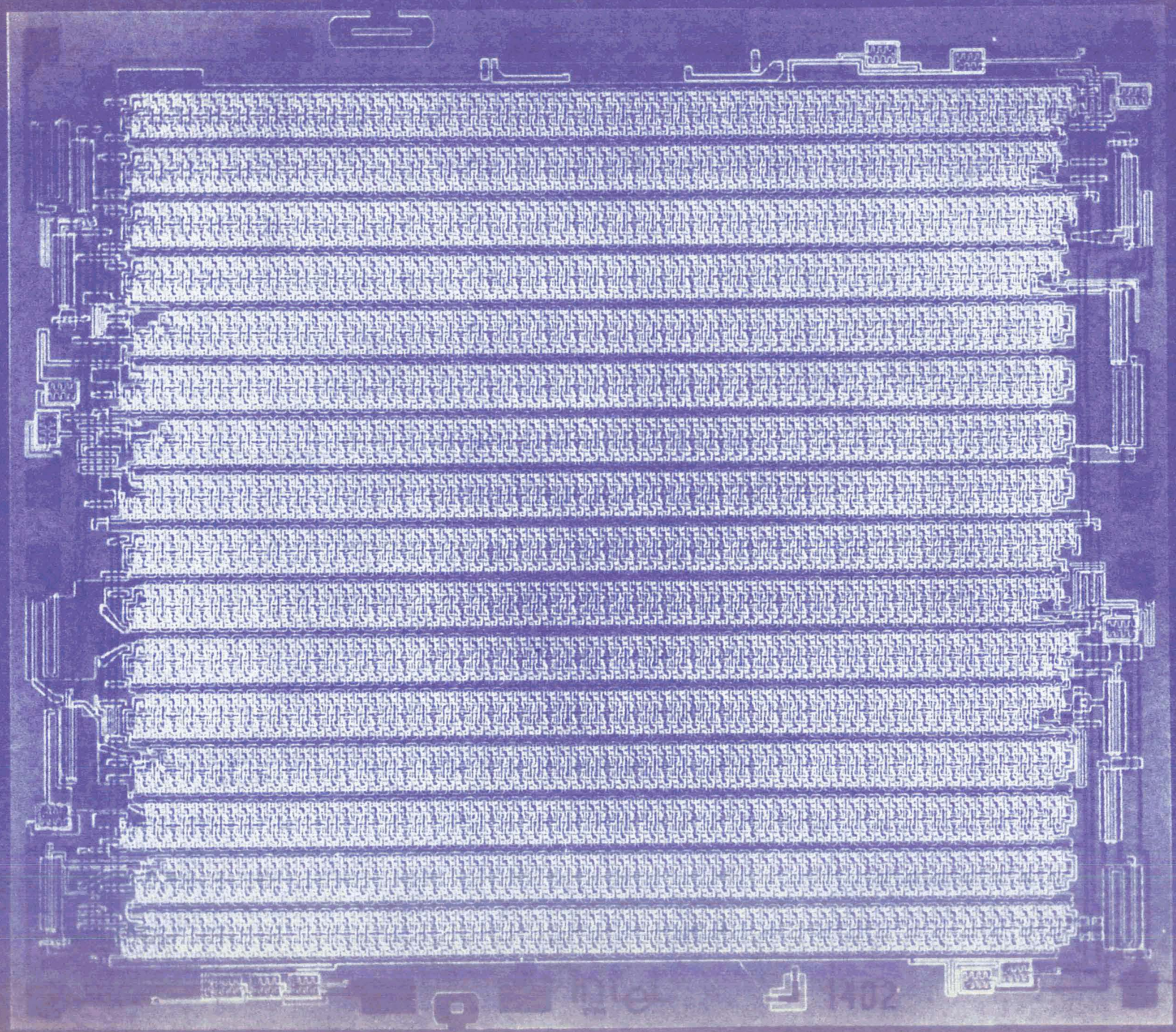


Figure 2-5. Intel Model 1402 Four 256-Bit MOS Dynamic Shift Registers

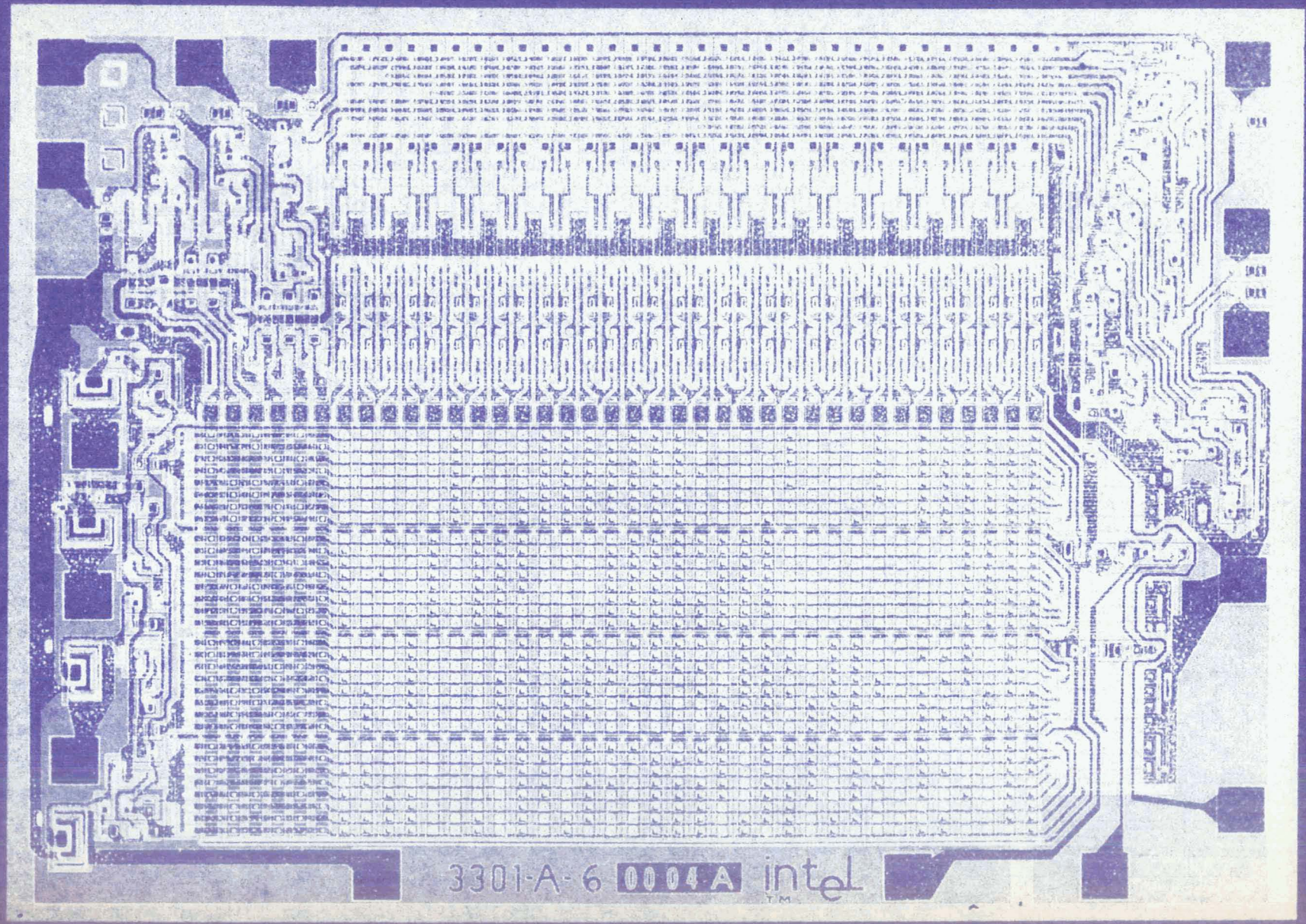


Figure 2-6. Intel 1024-Bit Bipolar ROM

TABLE 2-1 Manufacturers and Users of LSI Microcircuits

COMPANY	PRODUCT	LSI TEST CAPABILITY
American Microsystems	MOS	Redcor PAFT I&II Test Systems
Autonetics	MOS - Shift registers and memories.	Teradyne J259 NAA tester
Bell Telephone	Reliability studies of integrated circuits & MSI devices.	Fairchild Sentry 400
Boeing Space Center	Monolithic & Hybrid MSI (in-house & outside use)	Fairchild Sentry 400
Collins Radio	MOS	Collins DPI System
Computer Microtechnology	Bipolar & MOS	
Fairchild	Bipolar & MOS	Datatron Tester Teradyne J283 Fairchild Test Systems (5000, Sentry 400)
General Digital	MOS/LSI Testers	Spartan 770
General Instrument	MOS	In-house-built test systems (utilizing DEC PDP-8 & PDP-9 computers)
Honeywell	Computer Systems	Honeywell supplies test simulation graded card deck to vendor
Hughes Aircraft	MOS (Ion implanted devices)	Teradyne J259 (DC) LSI Tester North American Tester
IBM	Computer Systems	In-house Tester
ICE	Bipolar & MOS fabrication consultation. CAD (ICEMAP)	
Intel	Bipolar and MOS Memories (Schottky Diodes)	

TABLE 2-1 Manufacturers and Users of LSI Microcircuits (Cont'd)

COMPANY	PRODUCT	LSI TEST CAPABILITY
Intersil	Bipolar & MOS LSI	Teradyne J283
Macrodata	CAD, MOS LSI Tester Fabrication	Macrodata MD200
Motorola	MOS & Bipolar	Fairchild 5000
NCR	Computer Systems	
National	MOS	Teradyne J283
Nortec	(MOS) Wafer processing	
Philco	Bipolar & MOS MSI	Fairchild Sentry 400 Teradyne J283 & J259
Radiation	MOS	Teradyne J283
RCA	Complimentary MOS, MOS	Teradyne J259, J283 Spectra 70
Raytheon	Bipolar & Hybrid LSI (Beam lead technology)	Raytheon 703
Signetics	Bipolar & MOS LSI	Teradyne J263 Signetics 1700
Solid State Scientific	MOS, CMOS	Fairchild 5000
Solitron	MOS LSI	In-house tester
Teledyne-Ryan	MSI Shift Registers	MEMA automated tester
Texas Instruments	Bipolar & MOS	Fairchild Sentry 400 LSI Tester North American Tester Teradyne J283 (Slot)
TRW	Hybrid & Monolithic LSI (in-house use)	North American Tester
UNIVAC	Fabrication of MSI & LSI Hybrid circuits for in-house.	In-house-built tester.

TABLE 2-1 Manufacturers and Users of LSI Microcircuits (Cont'd)

COMPANY	PRODUCT	LSI TEST CAPABILITY
Varadyne	MOS	Macrodata MD200
Viatron	Computer Systems	Testing of individual parameters.
Xintel	LSI Tester fabrication	Xintel - Spectrum I MOS/Bipolar tester

3. LSI TEST SYSTEMS AND SPECIFICATIONS

3.1 LSI Test Systems - Introduction

Quite often, the electrical test philosophies of manufacturer and user are governed by the type of test equipment available rather than by the actual test requirements. One of the main reasons for this is the high cost of LSI testers and the fact that a change over to a new test system is expensive. Another reason for manufacturers basing their test philosophy on their present equipment is that many new test systems with impressive specifications on test capabilities are still untried. Also, the dynamics of LSI state-of-the-art technology are such that package configuration, pin count, wafer size, electrical parameters, device circuitry, and the like are continually changing, oftentimes causing the modification of expensive test systems with the inevitable hesitancy on the part of prospective test equipment buyers to buy new test systems. As a result, many manufacturers and users have gone the route of building their own test systems for in-house use only. While this requires a large initial investment, it can allow the manufacturer to keep his test equipment capabilities abreast of the LSI state-of-the-art by anticipating changes in his product in the initial test equipment design. This also paves the way for a possible new product line for the manufacturer should he feel that his newly-created test system can be competitively marketed.

3.2 LSI Test System Specifications

All of the LSI testers described in this section have capabilities for the functional testing of LSI devices. Many have parametric test capabilities in varying degrees. They are described in terms of the circuit type(s) tested, computer model and test software and pin count, along with data rate specifications (including maximum timing resolution) and the number of parametric tests performed per second in Table 3-1. Figures 3-1 through 3-5 picture state-of-the-art MOS and Bipolar LSI test systems.

Two methods of functional test pattern storage are illustrated in the system diagrams of Figures 3-6 and 3-7. The system shown in Figure 3-6 employs shift registers for pattern storage. This technique allows the capability of synthesizing extremely long test pattern word lengths through the aegis of shift register chaining. The system shown in Figure 3-7 employs random access techniques which allow the selection of specific segments of functional test patterns in storage at very high speeds.

A self-generating pattern system is shown in Figure 3-8. This technique, known as feedback sequence testing which compares self-generated logic sequences provided by the device under test with previously recorded sequences.

TABLE 3-1 Specifications of LSI Test Systems

MANUFACTURER	MODEL NO.	CIRCUIT TYPES TESTED	COMPUTER	TEST LANGUAGE	MAXIMUM PIN COUNT ACCEPTED	FUNCTIONAL		PARAMETRIC
						TEST RATE	TIMING RESOLUTION	TEST RATE
Adar	DR 32	Bipolar/ MOS	DEC PDP8/L	ATLS 1	32	10 MHz	.5n sec at high frequency	100 Test/second
Autonetics	312	MOS	-	-	40	1 MHz	-	-
Collins	DPI -101A	MOS	Collins 7404J-3	Collins	24	1 MHz	180nsec	-
DATATRON	4400	Bipolar	NOVA	DATATRON	100	40 KHz	-	Up to 50,000 Tests/sec/pin
Fairchild	Sentry 400	Bipolar/ MOS	FST-1	Users	240	300 KHz	350nsec	250 Tests/second
General Digital	Spartan 770	MOS	General Digital	-	52	5 MHz	-	-
General Radio	1790	Bipolar	GR	GR	96	625 KHz	-	1100 Tests/sec
LSI	4024	MOS	PDP 8	LSI	24	2 MHz	-	-
Macrodata	MD 200	MOS	Interdata 4	TOIL	64	2 MHz	-	200 Tests/second

TABLE 3-1 Specifications of LSI Test Systems (Continued)

MANUFACTURER	MODEL NO.	CIRCUIT TYPES TESTED	COMPUTER	TEST LANGUAGE	MAXIMUM PIN COUNT ACCEPTED	FUNCTIONAL		PARAMETRIC
						TEST RATE	TIMING RESOLUTION	TEST RATE
North American	TC9200 TC4800	LSI LSI	- -	Patchboard Binary	90 48	- -	- -	- -
Redcor	Paft II	MOS	Redcor RC70	Fortran	64	2 MHz	50nsec	250 Tests/sec
Teradyne	J283 (Slot)	Bipolar	PDP 8/1	MOP	120	50 KHz	-	200 Tests/sec
UNIVAC	-	Bipolar	UNIVAC 1218	-	160	500 Hz	-	50 Tests/second
Xintel	Spectrum 1	Bipolar/ MOS	NOVA	XINTOS	64	5 MHz	10nsec	Up to 10,000 tests/second/ pin

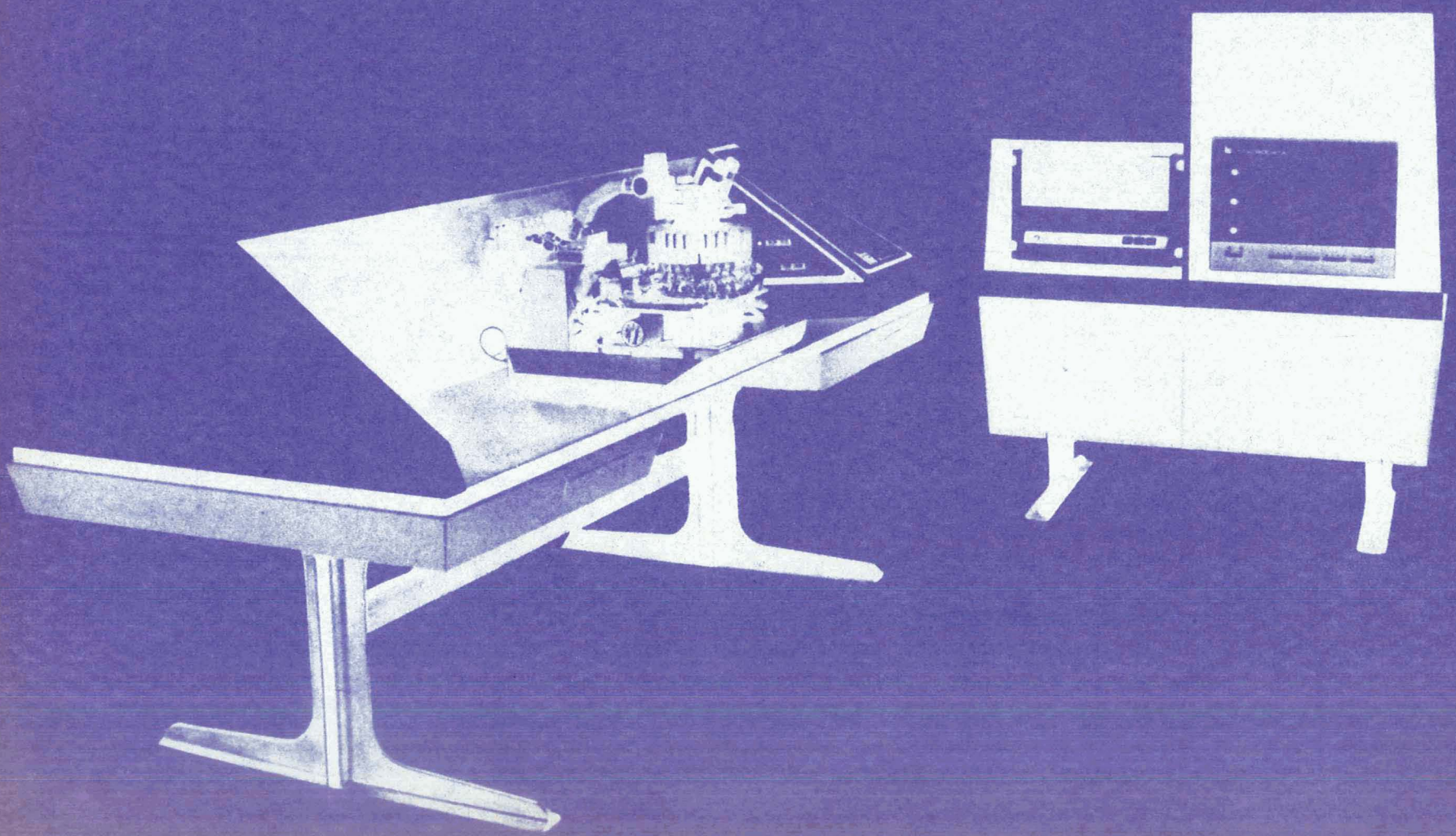


Figure 3-1. Macrodata MD-200 MOS Test System

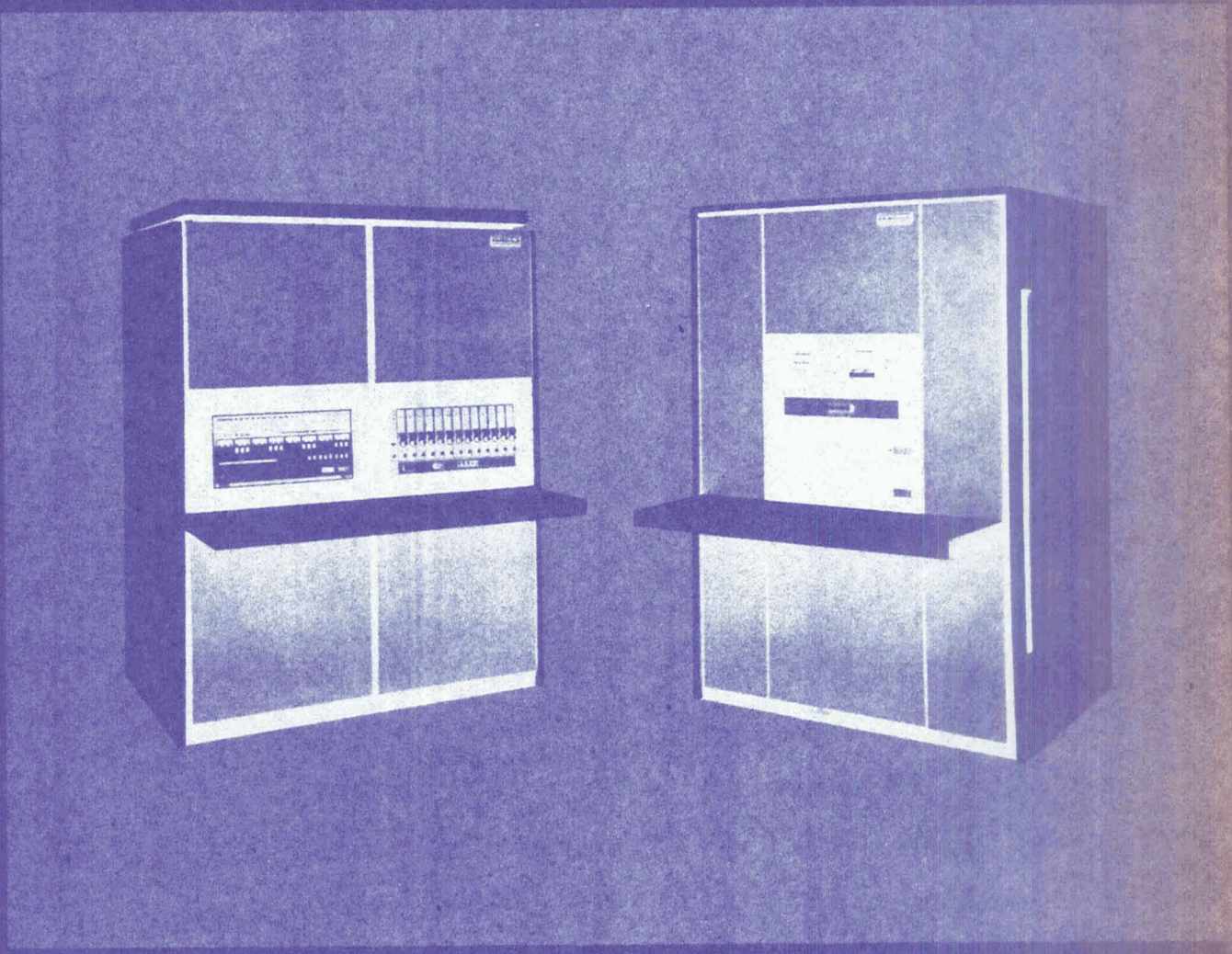


Figure 3-2. Fairchild Sentry 400 Bipolar/MOS Test System

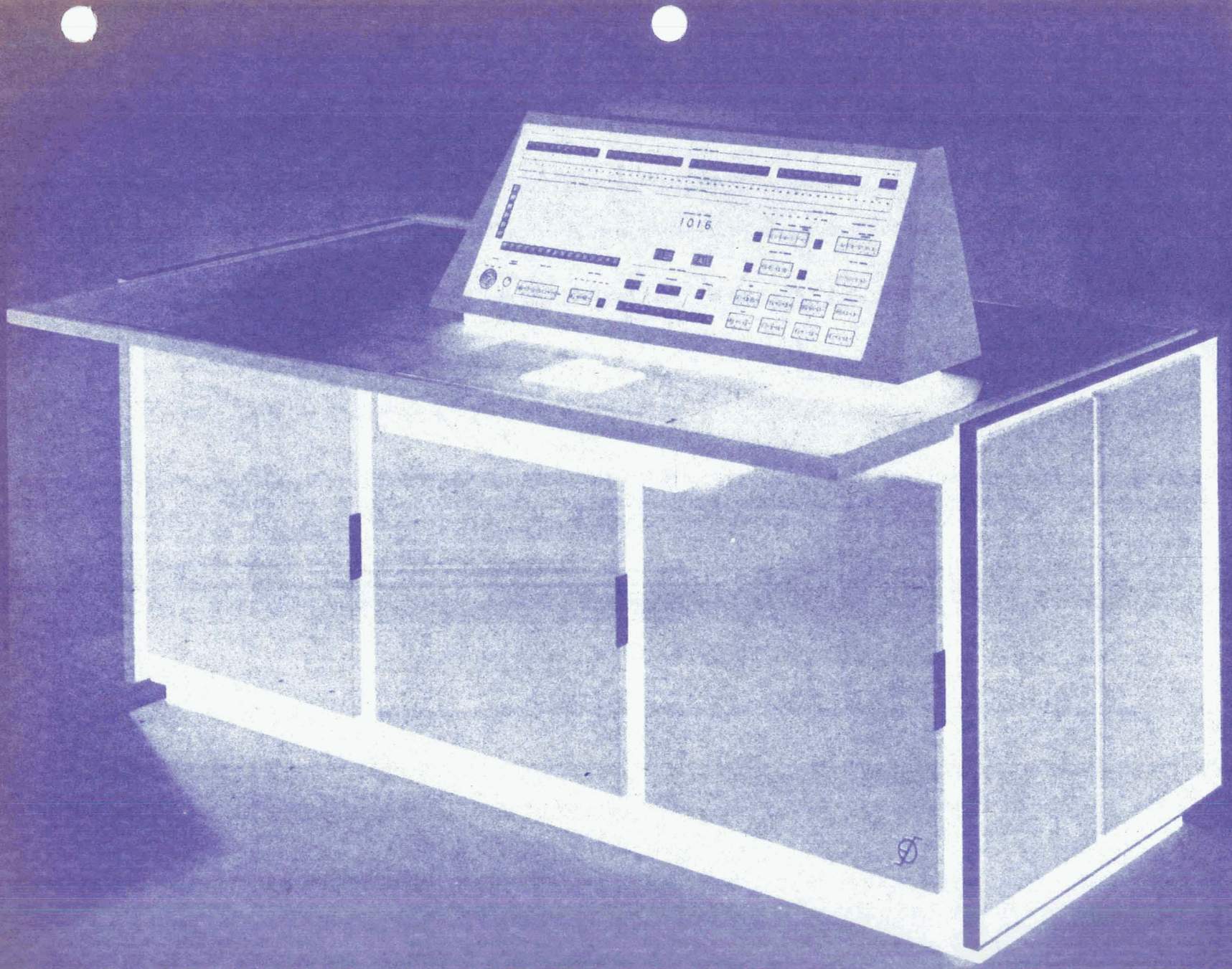


Figure 3-3. General Digital Spartan 770 MOS Test System

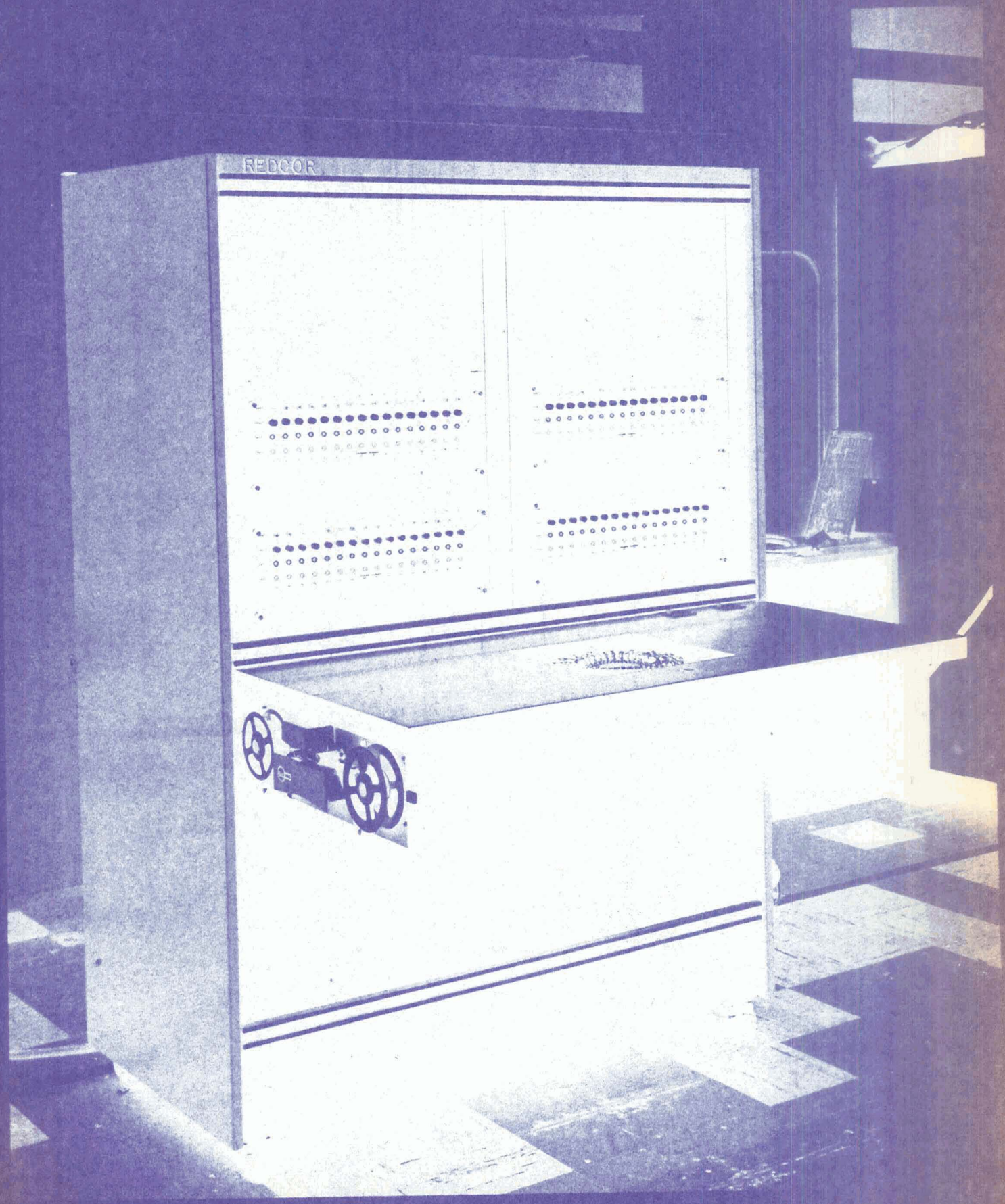


Figure 3-4. Redcor PAFT II MOS Test System

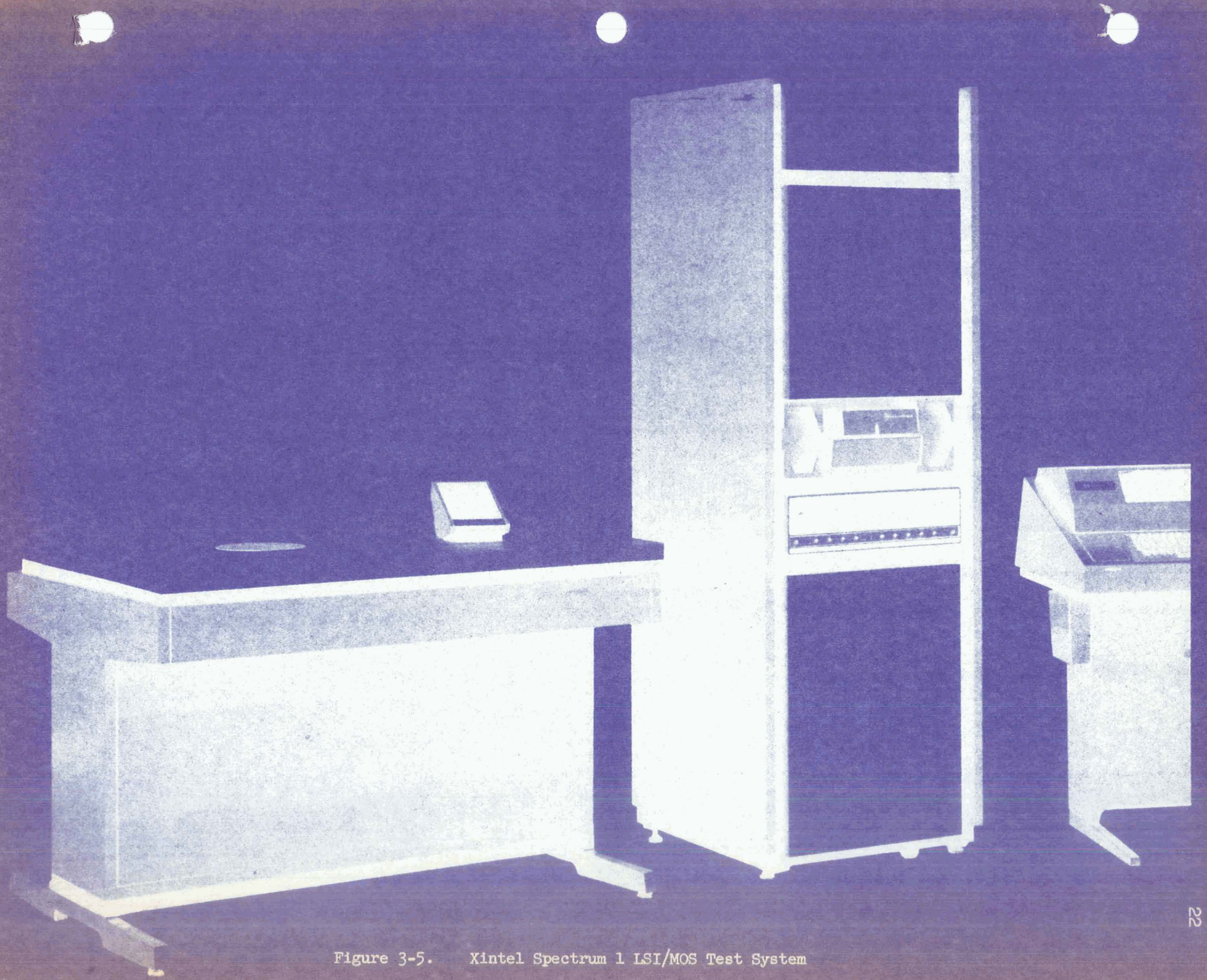


Figure 3-5. Xintel Spectrum 1 LSI/MOS Test System

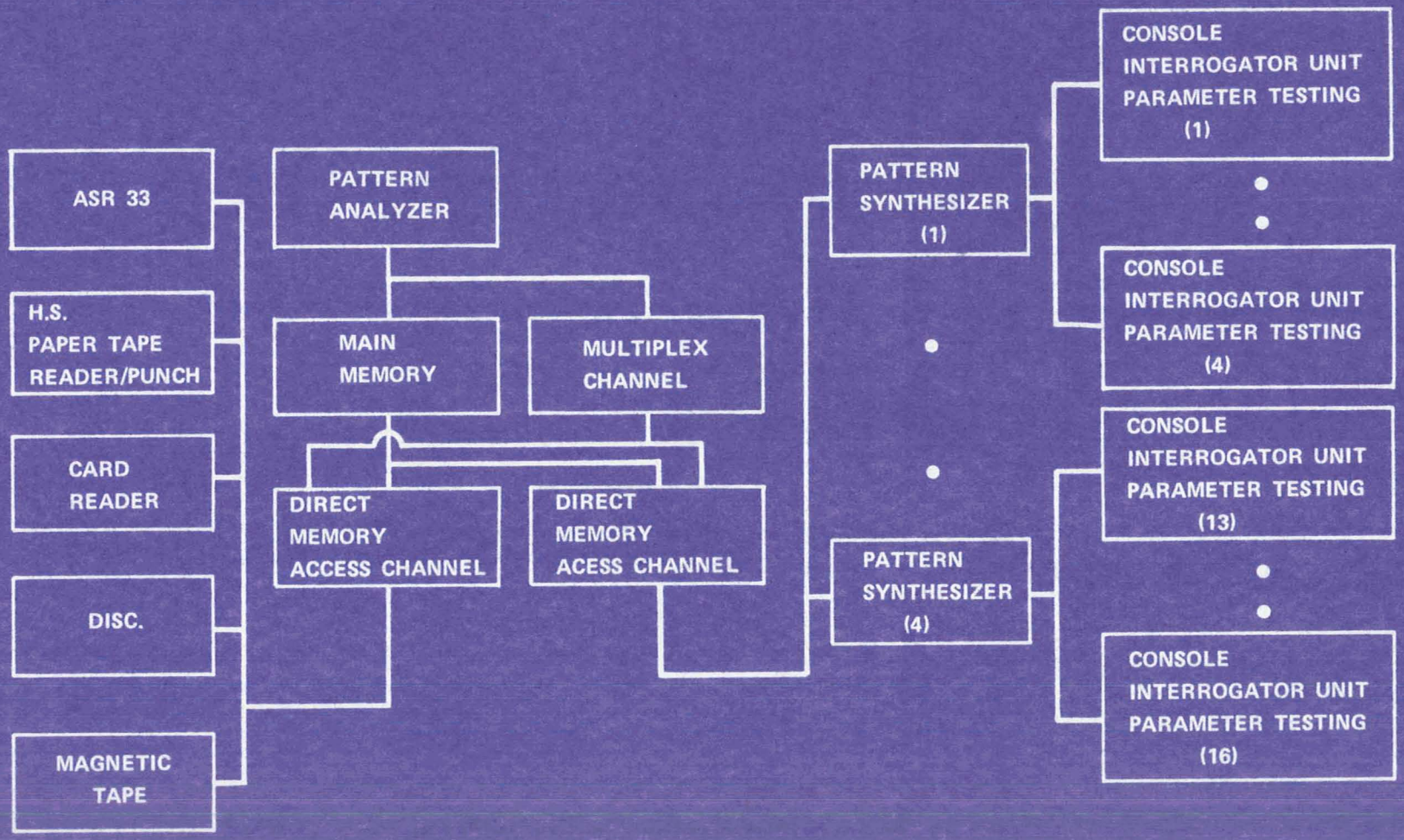


Figure 3-6. System Configuration MD-200 (Macrodata)

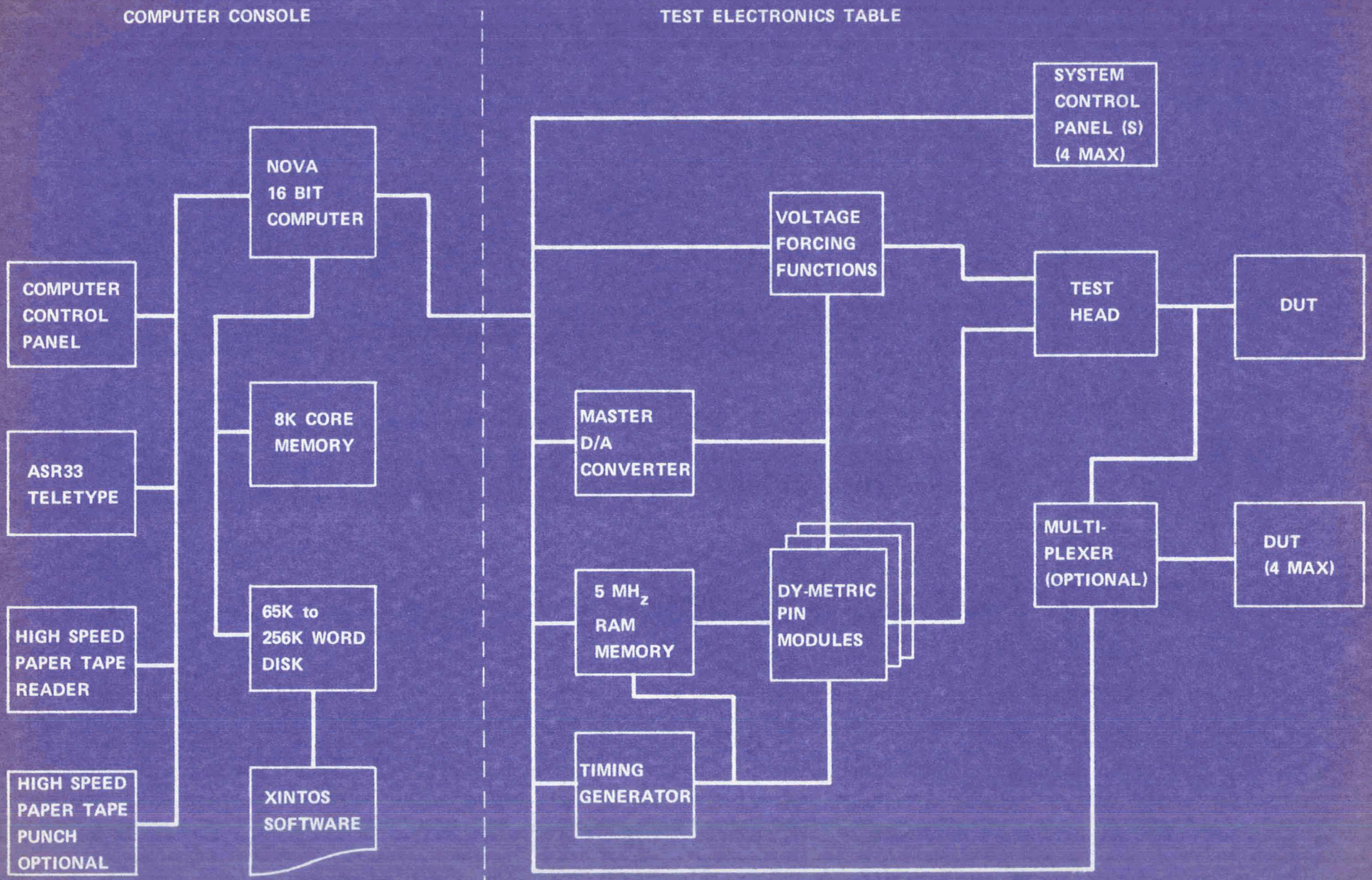
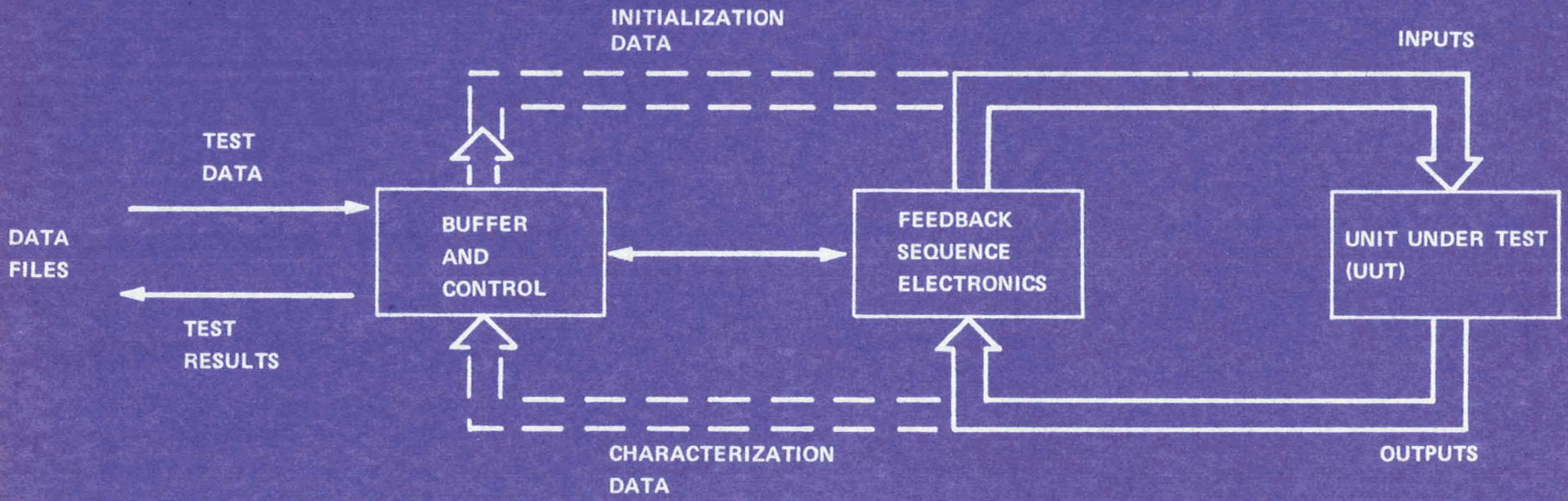


Figure 3-7. System Configuration Spectrum 1 (Xintel)



FEEDBACK SEQUENCE DATA FLOW DIAGRAM.
(COLLINS RADIO)
DPI SYSTEM

Figure 3-8. DPI System Configuration (Collins Radio)

4. TEST PHILOSOPHIES FOR LSI DEVICES

4.1 Introduction

Functional and parametric testing comprise the two general areas of LSI testing. These areas are further divided into wafer and package level testing, temperature testing, and high-and low-speed testing. LSI electrical testing is a particularly problem-ridden area due to high chip complexities, limited internal chip access, a proliferation of custom logic, mixtures of sequential and combinatorial logic, the continual evolution of new technologies (CMOS, MOS,threshold lowering, N-channel MOS), and lack of uniformity throughout the industry in testing of LSI devices.

Wafer-level testing can involve severe handling problems and, in fact, this is where a significant amount of infant attrition occurs. However, testing at this level is very important since one would rather discover device defects and process problems at this level rather than at final assembly after significant monetary value has been added to the device and several lots have been processed. Process monitoring of the wafer should include key parameters such as resistivity, oxide thickness (MOS) metalization, thresholds, leakage,and breakdown. Capacitance-Voltage (CV) variation plotted over temperature is also helpful in process monitoring. Desirable as it would be, tight process control and/or intensive visual inspection are not substitutes for electrical testing.

Functional testing of LSI microcircuits comprises the generation of specific test patterns which, when applied to the input terminals, will yield information indicating the presence or absence of faults in the device. These tests routines are generally classified as either fault diagnosis or fault detection routines. Fault diagnosis includes the location and determination of the fault, while fault detection is, in general, the verification of the Boolean response of the device. Assumptions usually made in functional testing include the following:

- Faults can only occur one at a time
- Faults are static, not intermittent (i.e., stuck at 1, or stuck at 0)
- Logic is non-redundant

Functional testing is also categorized according to the type of logic to be tested. The logic type is either combinational or sequential. Combinational logic networks respond to each input pattern independently of the previous input. Sequential logic networks respond according to their present state and the incoming input pattern. As a result, sequential logic testing is more complicated than combination testing. Sequential test routines, however, often include a capability for testing combinational logic.*

It is well known that the application of all possible combinations of input patterns to a device for functional testing is not at all practical, particularly with complex devices. Additionally, in as much as most LSI microcircuits are usually pin-limited, it is ofter impractical if not often impossible to provide sufficient external test point for monitoring the performance of internal circuit elements. The singular prohibitive factor

*Developments in L.S.I. - Motorola Semiconductors, Inc.

in this exhaustive testing concept is time. As a result, algorithms have been developed outlining more efficient test approaches that will sufficiently exercise a device. Section 9.2 (Volume II) discusses several of these algorithms. In the area of LSI testing, this lends itself to more than one discipline of thought. One testing philosophy dictates that all gates shall be exercised at least once, while another approach is to exercise most of the gates several times. In the latter technique, a grading system is used to grade each test sequence according to how many gates were exercised. Testing sequences can be combinations of all 1's followed by all 0's or alternate 1's and 0's (checker board array) or some other variation of binary elements.

In functional testing, it is desirable to have a test system that permits a variable allocation of input and output pins and which also possesses the capability of changing all inputs at once. This allows testing flexibility from device to device and permits testing of various I/O pin configurations with maximum binary exercising.

The length and configuration of data patterns depends on the type of device to be tested. In general, the various LSI devices fall under the classifications of Random Access Memory (RAM), Read Only Memory (ROM), Shift Registers, and Logic Arrays.

ROMS require a pattern depth of 2^N, as a minimum, where N is the number of address lines. RAMS require relatively long, yet simple data patterns (e.g., write 1's, write 0's, write checkerboard) and it may be desirable

to use self-generating pattern techniques to produce the large words required. The testing of Shift Registers requires propagating a logic 1 through all existing logic 0 stages and vice versa. Random logic arrays require the generation of special complex patterns.

4.3 Parametric Testing - DC and AC

Electrical parameter testing of LSI devices fall into two general categories: DC or static parameter measurements, and AC or switching characteristic measurements. Parametric tests relate directly to process verification and as a result are a mandatory part of LSI device testing. Test time for individual parameters is much longer than functional test time. This is due to the setup time required for each parameter along with proper sequencing of current and voltage measurements.

Measurement of device parameters at temperature extremes is a significant problem particularly for switching-time type measurements where test fixturing difficulties can compound the problem of temperature testing. Evaluation of the temperature performance of a device should therefore be accomplished as efficiently as possible, measuring only those parameters which yield significant temperature response information. Column C of the Tables in Section 6 show the relative temperature sensitivity of MOS and Bipolar device parameters for several types of devices.

Some useful parametric information may be derived through exhaustive worst-case functional testing where functional test patterns are applied to the device under test (DUT) for various worst-case input or supply conditions. Verification

of electrical parameters is inferred by the realization of a correct output sequence for all worst case situations. The "functional" parametric testing is faster of course, since measurement time is eliminated.

The extent of AC testing should be related to the intended ultilization of the device. Switching characteristics of devices should be verified at as close to the designed operating speed as practicable. Characterization of circuit parameters is, at best, a compromise of proper testing procedures. For very high-reliability applications, neither bipolar nor MOS LSI processesing technology is controlled sufficiently to allow ambient temperature characterization of DC parameters or low speed characterization of dynamic parameters to preclude actual testing of the device under temperature or speed extremes.

5. TEST VEHICLES - DESIGN AND APPLICATION

The technique of employing test vehicles (test elements) on the wafer allows the verification of process control at the wafer level. The test vehicle can either be a part of the device mask or a separate mask exposed at specified locations on the wafer. The makeup of the test vehicle may range from a simple transistor to an entire circuit. Figure 5-1 shows an example of a test vehicle developed for process evaluation of custom MOS LSI devices. The device consists of a dual 32-bit shift register, a capacitor, gate- and field-oxide transistors, and a resistor. One shift register (Figure 5-2) is designed with state-of the-art topology (i.e., design rules of the manufacturer of this device) while the other is designed with "tight" topology. The 0.2 mil wide p-diffused resistor is used to test sheet resistivity with nominal readings between 2500 ohms to 4500 ohms. The discrete transistors allow testing of individual MOS device parameters. Typical parameters measured are shown in Table 5-1.

TABLE 5-1. Parameters Measured on a Test Vehicle (Varadyne)

PARAMETER	VALUE/RANGE	CONDITIONS
Threshold Voltage	3-5v	I_D = 1 μA
Drain Breakdown	35v min	I_D = 1 μA
Field Threshold	30v min	I_D = 1 μA
ON Resistance	V_g = 20v	I_D = 100 μA
Punch Through	40v min	
Sheet Resistivity	2500 to 4500 ohms	
Oxide Rupture Voltage	70v min	

Another test vehicle device developed for process monitoring and reliability testing is shown pictorially in Figures 5-3 and 5-4 and schematically in Figure 5-5. This test vehicle contains:

- A discrete inverter and MOS load device to allow power life testing in the ON condition. Resultant data will define expected drift within arrays.
- A p-n junction covered by an MOS capacitor, used to monitor oxide stability which indicates the presence of ionic contaminants.
- A p-n junction identical to the one covered by an MOS capacitor for correlation of drift.
- A metal stripe of minimum design width crossing etched cutouts which allows life testing with acceleration of metal separation in the presence of moisture or other contaminants.
- A series of metal stripes crossing a deeply etched area which permit checks to be made on metal quality. These stripes are destructed by burn out; a distribution plot is derived to provide a quantative measurement of quality.*

The devices are tested on the wafer immediately after final metallization and are then packaged in a TO-5 configuration for life testing. Typical measurements are given in Table 5-2. They can also be mounted in other types of packages to study the overall degradation characteristics of a particular chip-package combination.

---

*Evaluation of A.M.I. D Process Rel-Chips - AMI, June, 1970.

TABLE 5-2. Parameters Measured on Test Vehicle (AMI)

PARAMETER	SYMBOL	VALUE/RANGE
Load Device Threshold Voltage	V_{TL}	2v min, 8v max.
Field Inversion Device Threshold Voltage	V_{TF}	10v min., 30v max.
Modulated Diode Breakdown Voltage	BV_a	40v min., 80v max.
Drain-to-Source Breakdown voltage	BV_b	40v min., 80v max.
Intrinsic Material Breakdown Voltage	BV_{PN}	80v min.
Inverter Threshold Voltage	V_T	2v min., 8v max.
Metal Line Continuity Check	R_{ML}	20mV max.
Inverter ON Resistance	R_{ON}	500mV max.
Isolated Gate, Zero Bias Capacitance	C_a	5.0pF max.
Isolated Gate Capacitance-Bias Exceeding V_T	C_b	3.0pF max.
Biased Gate Modulated Diode Capacitance	C_c	5.0pF max.
Output Load Device Logic Levels	V_o, V_1	10.0v min., 2.0v max.

It should be noted that the validity of the test vehicle concept is based on the assumption that an individual chip on a wafer is a reasonable facsimile of other chips in the immediate area. Typical distributions of test vehicles on a production wafer are shown in Figure 5-6.

Various schools of thought about the distribution of wafer defects generally agree that defects are not randomly distributed but clustered. This is illustrated in Figure 5-7 where the graph shows that yield falls off at a less than exponential rate with increasing active area.* Test vehicles, therefore, can generally serve as valuable checkpoints during processing and allow a fairly rapid assessment of the entire wafer. Proposed test vehicle models must guarantee the manufacturer the option of assessing the design and functional characteristics of a particular device regardless of functional and/or physical complexity. The weighting values assigned to the data derived from test vehicles conceived in this manner will enhance the validity of reliability predictions.

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*What Level of LSI is Best For You? - G. Moore. Electronics, Feb. 16, 1970.

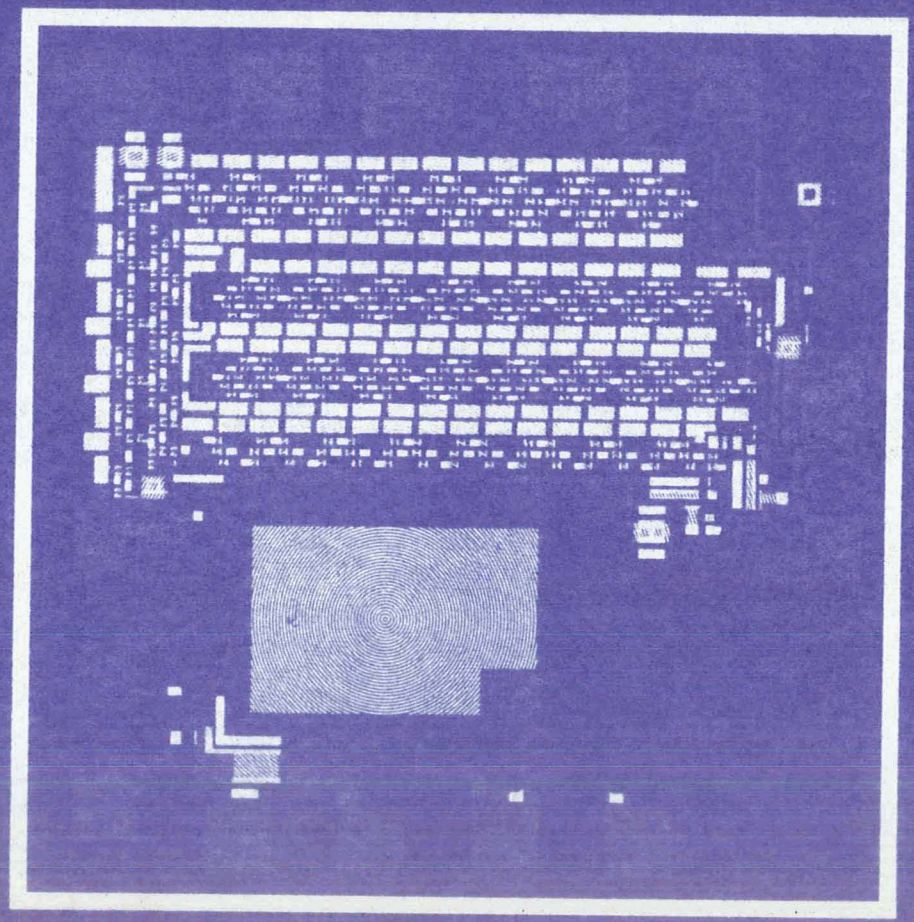

Figure 5-1. Wafer Process Evaluation Device (Varadyne)

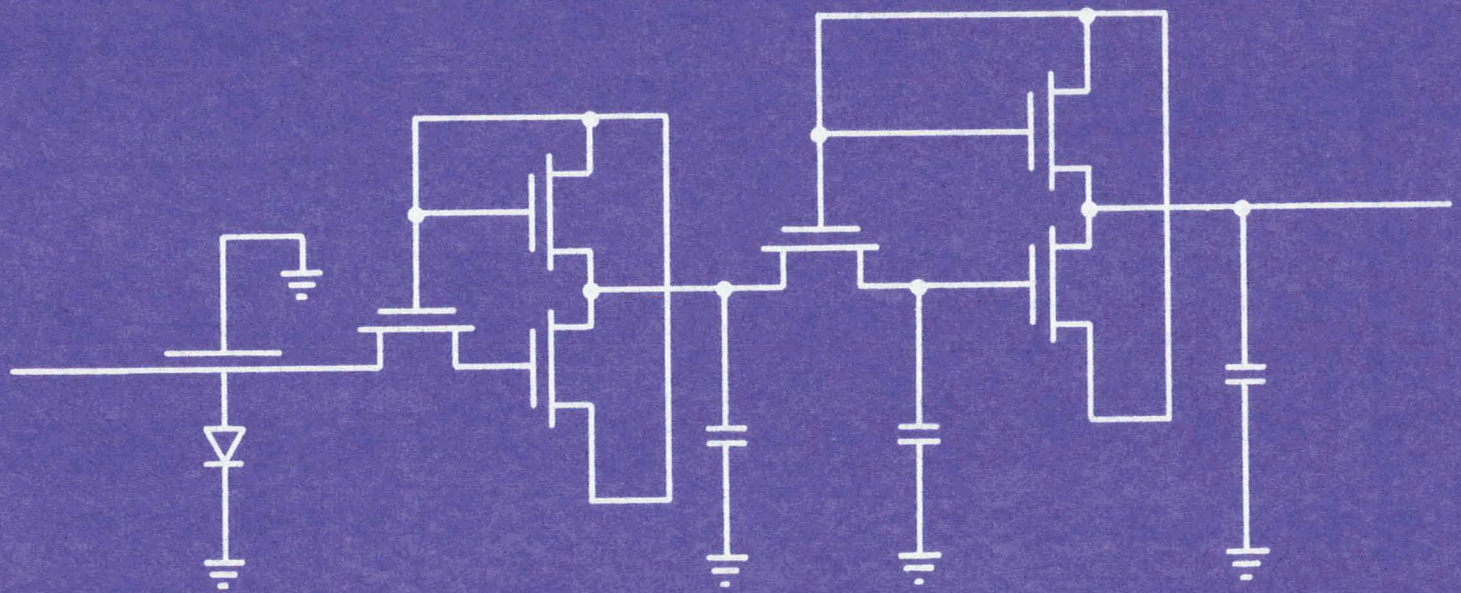

Figure 5-2. Shift Register Employed on Evaluation Device (Varadyne)

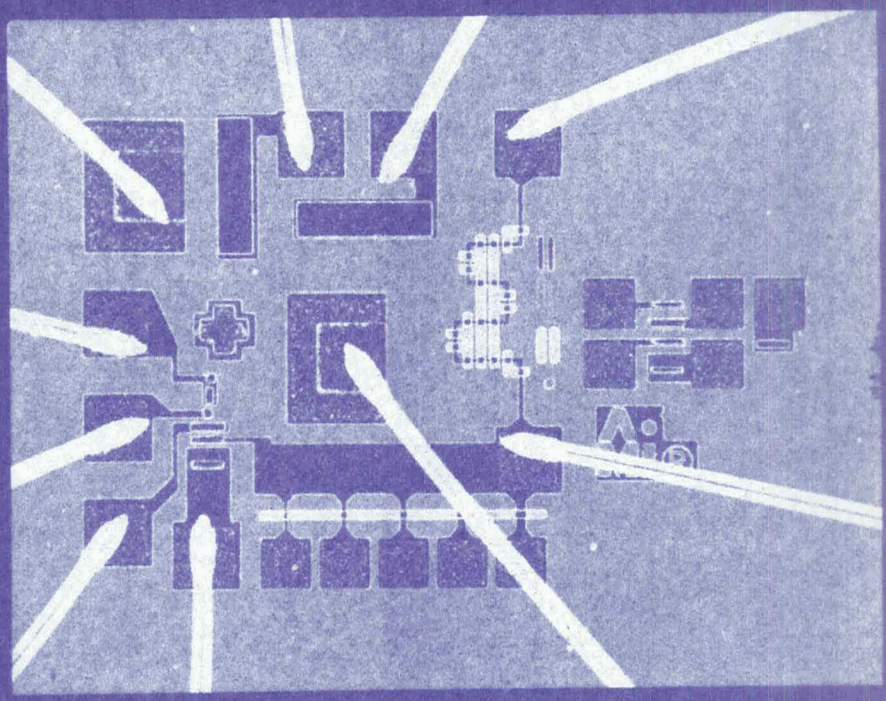

Figure 5-3. Test Vehicle (AMI)

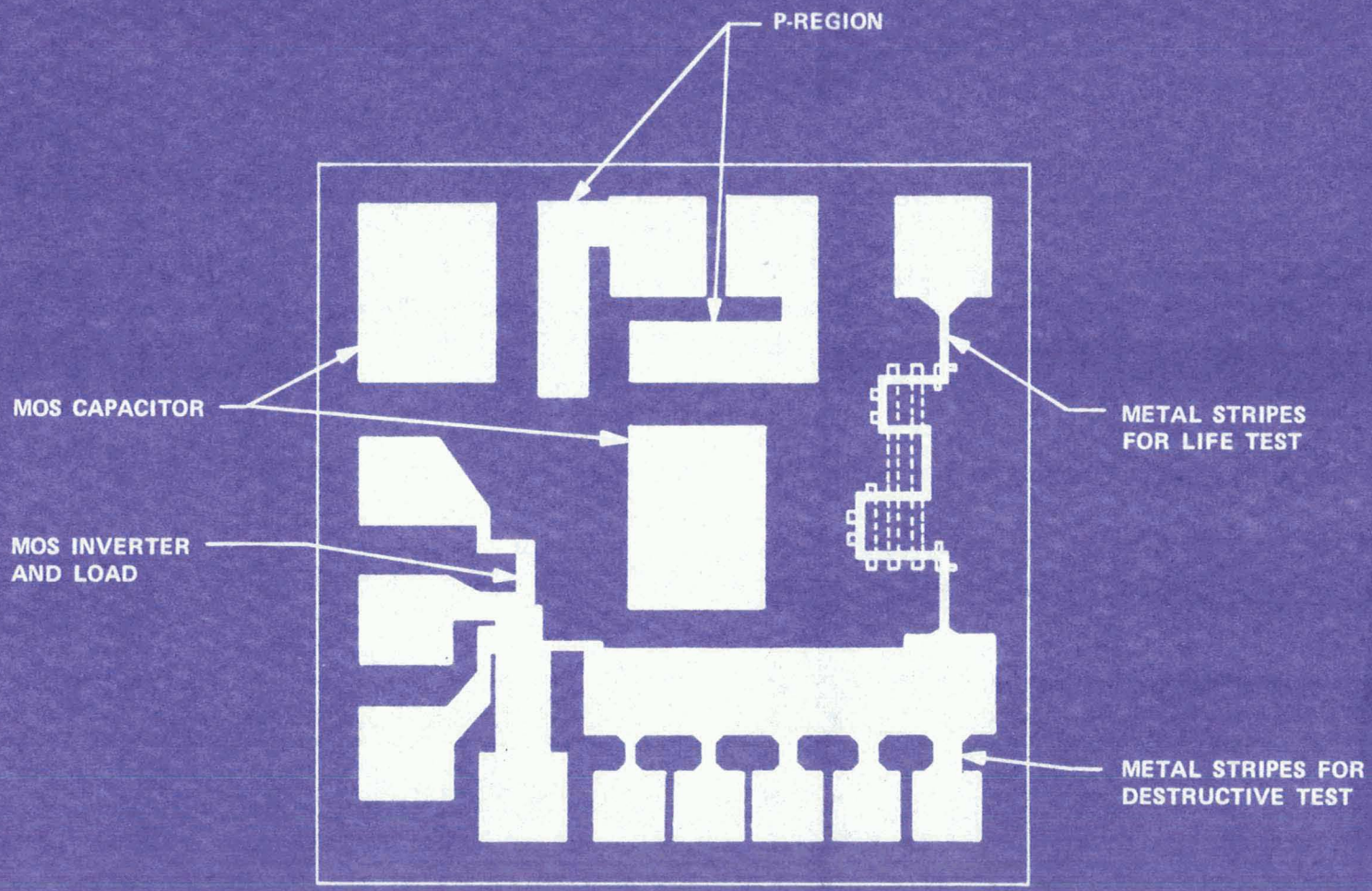

Figure 5-4. Test Vehicle Geometry (AMI)

1 = Output of inverter device
2 = Input of inverter device
3 = Field inversion device
4 = Isolated diode
5 = Ground and body
6 = Metal line over oxide steps
7 = Isolated gate
8 = Gate of gate modulated diode
9 = Gate modulated diode
10 = VDD/VGG Load Device

NOTE: Numbers refer to Pin Numbers

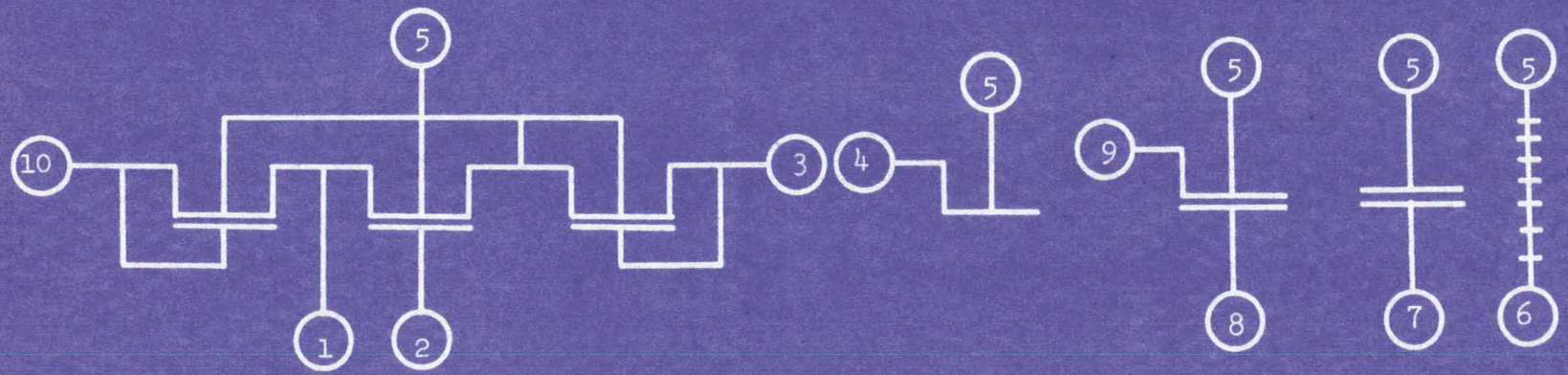

Figure 5-5. Schematic of Test Vehicle (AMI)

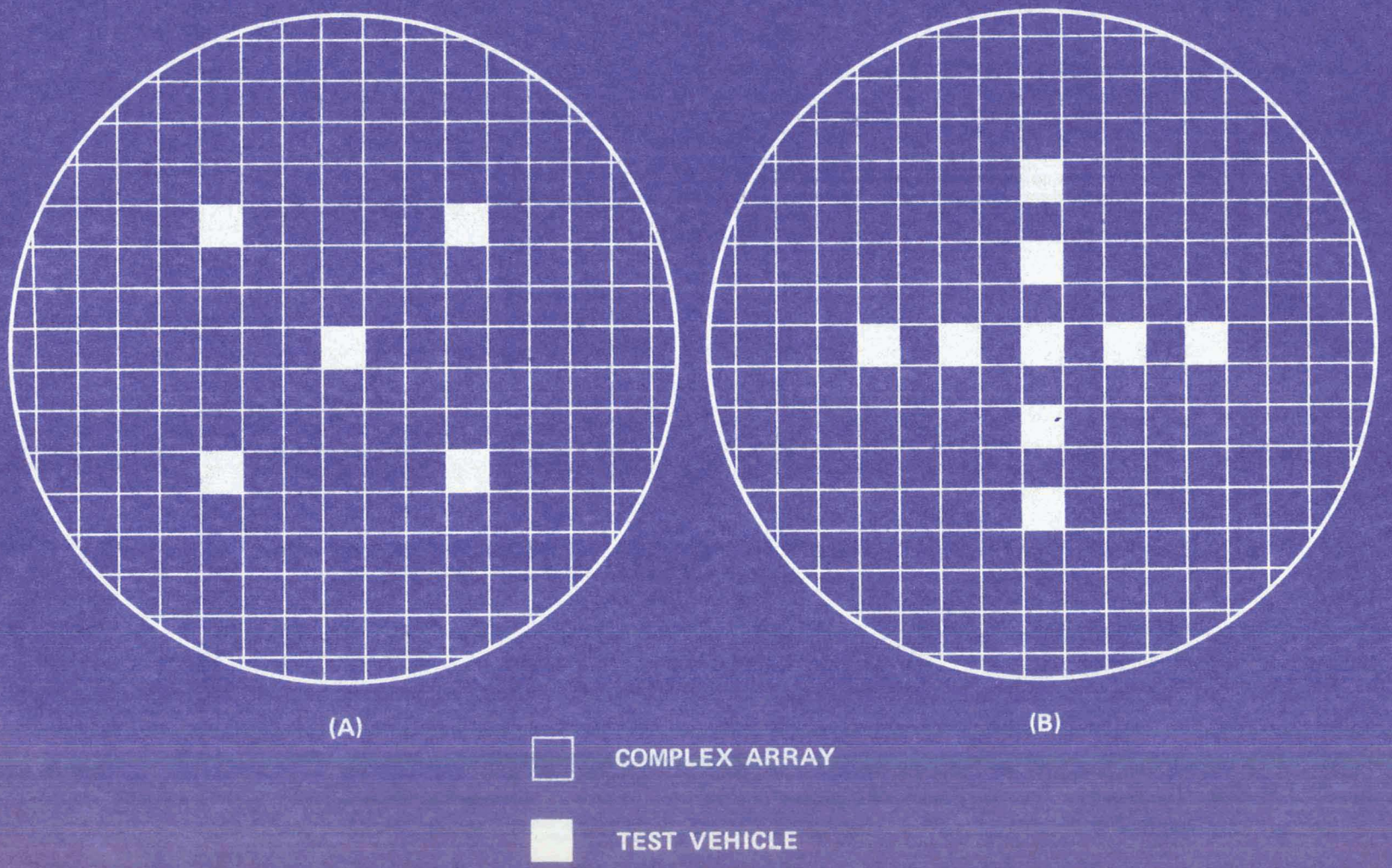

Figure 5-6. Typical Locations of Test Vehicles on a Production Wafer

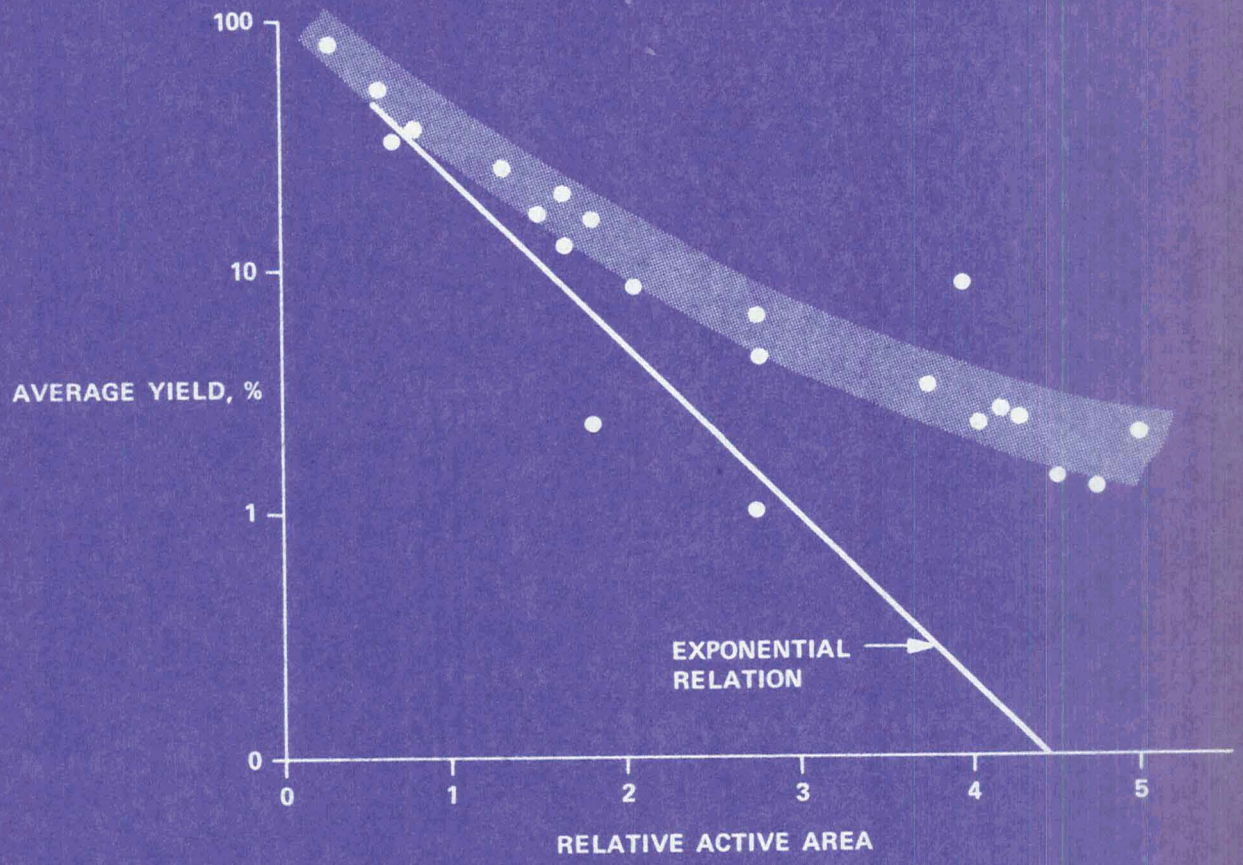

Figure 5-7. Graph of Wafer Area vs. Yield

6. EVALUATION OF LSI ELECTRICAL PARAMETERS

6.1 Introduction

The task of evaluating individual LSI electrical parameters was initiated by first selecting four standard LSI device types: Static Shift Registers, Dynamic Shift Registers, Read-Only Memories (ROM's) and Random Access Memories (RAM's). Parameters associated with each type of device for both MOS and Bipolar technologies were then compiled in tabular form and each parameter was evaluated according to its effectiveness in each of the following three areas:

- Functional Performance Indicator
- Performance or Latent Failure Indicator
- Temperature Performance Indicator

Each parameter was evaluated in accordance with these criteria using the following quantitative scale delineating the degree of significance of each parameter:

5 Extremely Significant

4 Very Significant

3 Significant

2 Moderately Significant

1 Not Very Significant

0 Insignificant

Parameter evaluation sheets from over 25 manufacturers and users were then statistically averaged and compiled. The resulting composite ratings give a comparative overview of the relative importance of individual electrical parameters in these indicator categories. Within any one device category, the numerical ratings are inversely related to the

significance of each parameter, e.g., 1 = Most Significant, 2 = Less Significant . . . . 50 = Least Significant, etc. More than one parameter may have the same numerical rating within a given functional, latent failure, or temperature performance indicator column (i.e., some statistical averages were coincident).

6.2.1 MOS Static Shift Registers

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Clock,			
Amplitude	2	4	
Capacitance	13		
Fall Time	9		
Leakage Current		1	1
Pulse Frequency	9		
Pulse Width	4		
Rise Time	9		
Shift Frequency	11		
Delay Time,			
Reset	15		
Input,			
Capacitance	16		
Current high, low logic level	17		
Fall Time	16		
Frequency	3		
Leakage Current		1	1
Pulse Width	7		
Rise Time	16		
Noise Immunity,			
Threshold Voltage	16		
Output,			
Current Drive Capability	12		
Leakage Current		3	2
Fall Time	8		
Impedance	6		
Propagation Delay	9		
Rise Time	11		
Transition Time	10		
Voltage	1	2	

6.2.1 MOS Static Shift Registers (Continued)

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Power,			
Dynamic Network-bit Consumption			3
Supply Current			4
Pulse Duration,			
Reset	14		
Set-up Time,			
Data	5		

6.2.2 MOS Dynamic Shift Registers

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Access Time,			
Data	10		
Clock,			
Amplitude	7	8	
Capacitance	23		
Inter-Capacitance	20		
Leakage Current		1	1
Pulse Delay	8		
Pulse Frequency (Maximum, Minimum)	4		
Pulse Spacing	10		
Pulse Width	2		
Rise Time	17		
Fan-in	27		
Fan-out	16		
Input,			
Capacitance	26		
Frequency	5		
Leakage Current		2	2
Pulse Width	6		
Pull-up, down Resistance	12		
Logic Level	3	3	
Noise Immunity,			
AC	22		
DC	25		
Output,			
Drive Capability-Capacitance	10		
Fall Time	15		
Impedance	13		
Leakage Current		7	4
Pull-up, down Resistance	18		
Pulse Width	24		
Resistance	21		
Rise Time	19		
Sink Current	9	5	5
Voltage	1	3	

6.2.2 MOS Dynamic Shift Registers (Continued)

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Power,			
Dynamic Network-bit Consumption		4	6
Supply I,		6	7
Total Consumption-static, quiscent			3
Set-up Time,			
Address and Chip Select	14		
Data	11		

6.2.3 MOS Random Access Memories

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTIBILITY TO VARIATION OVER TEMPERATURE RANGE
Access Time,			
Chip Disable	5		
Read	4		
Write	4		
Address,			
Current-logic 1,0		3	7
Input Capacitance	9		
Clock,			
Capacitance	7		
Delay Time,			
Readout-Read after write, Read	3		
Input,			
Capacitance	8		
Leakage Current		2	1
Load Current		4	8
Voltage	2	7	
Output,			
Capacitance	10		
Impedance	6		
Leakage Current		5	2
Sink Current		6	3
Source Current		6	4
Voltage	1	1	
Power,			
Supply I,			6
Total, static, quiescent Consumption			5

6.2.4 MOS Read Only Memories

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Access Time,			
Address Output Delay	4		
Chip Inhibit	5		
Input,			
Capacitance	7		
(and) Chip Inhibit Leakage Current		1	1
Leakage Current		2	2
Voltage-high, logic one	2		
Voltage-low, logic zero	2		
Output,			
Capacitance	6		
Leakage Current		3	3
Pulse Delay	3		
Voltage	1		
Power			
Supply Drain I,			4
Total static quiescent Consumption			5

6.3.1 Bipolar Static Shift Registers

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Clock,			
Amplitude	6	3	
Capacitance	14		
Fall Time	11		
Input Impedance	14		
Noise Immunity	8		
Pulse Frequency (Maximum)	6		
Pulse Width	6		
Rise Time	11		
Delay Time,			
Turn-off	9		
Turn-on	9		
Input,			
Leakage		2	1
Load Current	10	4	
Capacitance	16		
Impedance	15		
Logic Levels	1		
Pulse Width	5		
Noise Immunity,	14		
Output,			
Logic Levels	2	2	
Fall Time	12		
Rise Time	13		
Power,			
Total static, quiescent Consumption			2
Pulse Width,			
Minimum-Maximum Reset	7		
Recovery Time	8		
Release Time	8		
Response Time, tpdt, tpd-	0		

6.3.2 Bipolar Random Access Memories

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Access Time,			
Chip Select	4		
Address	4		
Input,			
Address Clamp Voltage	3		
Address Leakage Current		1	2
Address Load Current		4	5
Chip Select Clamp Voltage	3		
Chip Select Leakage Current		1	2
Chip Select Load Current		4	4
Data Clamp Voltage	3		
Data Leakage Current		2	3
Data Load Current		4	4
Write Clamp Voltage	2		
Output,			
Leakage Current		3	1
Recovery Time	4		
Voltage-low, logic zero	1		
Power,			
Supply I_1			6
Supply I_2			6
Write,			
Pulse Width	5		
Recovery Time	6		

6.3.3 Bipolar Read Only Memories

PARAMETER	A OVERALL FUNCTIONAL PERFORMANCE	B PERFORMANCE DEGRADATION OR LATENT FAILURE	C SUSCEPTABILITY TO VARIATION OVER TEMPERATURE RANGE
Access Time			
Address Output Delay	3		
Chip Inhibit	4		
Input,			
Address Capacitance	8		
Address Clamp Voltage	9		
Address Leakage Current		1	1
Address Load Current		4	7
Chip Inhibit Leakage		1	1
Chip Select Capacitance	8		
Chip Select Clamp Voltage	9		
Chip Select Leakage Current		1	1
Chip Select Load Current		4	6
Voltage	2		
Output,			
Data Capacitance	7		
Leakage Current		2	2
Sink Current		3	3
Voltage	1		
Power,			
Dynamic Network-bit Consumption			5
Total, static, quiescent Consumption			4
Supply Drain			4
Propagation Delay,			
Leading Edge	5		
Trailing Edge	6		

APPENDIX A

LSI TECHNOLOGY— DEFINITIONS.

The term LSI (Large Scale Integration) commonly refers to a technology which permits the integration of a large (more precisely over 100 equivalent gates) number of electronic devices, such as diodes and transistors into one single functional package such as a shift register, multiplexer, decoder, counter etc., built normally on and within a single semiconductor chip or wafer.*

In addition to characterizing LSI and MSI microcircuits by their complexity, they can also be characterized by the technology or device structure (Bipolar vs MOS) and by the interconnection technique (discretionary wiring vs fixed wiring approaches). The following are some basic definitions in LSI technology.

Complimentary MOS (CMOS)— Devices made with MOS technology with both P- and N-channel devices on a chip:the circuits dissipate power only during a change of state. The instant of change is the only time that significant current flows and this current can be kept extremely low, on the order of a few microamperes. Along with low power consumption, CMOS also offers greater speed than conventional MOS circuitry. CMOS also has good noise immunity characteristics and a strong insensitivity to supply voltage variations. Two extra masking steps are

*Some LSI microcircuits may be comprised of several LSI microcircuits of lesser complexity, which, in combination with some discrete components and an interconnecting film network, form a functional package. However the term "Hybrid LSI" would be more appropriate in this case.

Complimentary MOS (CMOS)——(Continued)

required in CMOS fabrication: one step to add the N channel transistors and another to electrically isolate them from the P channel devices. Contamination precautions must be more elaborate with CMOS because of the high sensitivity of N channel transistors to contamination.

Discretionary Wiring—A technique which permits the selective interconnection of good cells on the chip, bypassing the defective units—the layout for such interconnection paths is generally computer programmed and generated. Each cell is a complete basic circuit (a "building block") with pads for preliminary probing. This means that there is no efficient usage of potentially good silicon material. On the other hand since the interconnection patterns are only required to connect the large probe pads, it is not necessary to have high resolution masks. To simplify routing the interconnections, two additional levels of metalization are required. The discretionary wiring approach is capable of producing a wide variety of functions within a short time at low design but relatively higher manufacturing costs.

Field Shield—Self aligning passivated MOS process allowing bipolar speed compatible N-channel devices—very low threshold and extremely high field inversion voltages also result.

Fixed Wiring—(Or the Chip Approach) - A technique whereby identical chips are used across the wafer, each chip with complete identical interconnection patterns regardless of fault location—since there are no probing pads provided for each cell, a higher circuit density

Fixed Wiring—(Continued)

(and hence a more efficient utilization of silicon wafer) can be achieved. Test pads are provided only for input-output access to the circuits: therefore the circuits cannot be readily tested until fabrication has been completed. The fixed wiring approach requires greater design time and cost and much higher resolution masks, but is capable of producing quantities of components relatively inexpensively.

Between discretionary and fixed wiring approaches, there are various compromises which tend to optimize the manufacturing cost of circuits for a particular application. The following are some established terms:

Ion Implantation—A method of doping semiconductors using a high energy (80-300 Kev) accelerator to drive the dopants into the bulk silicon—using a focusing mechanism the accelerator selects by mass the dopant to be used emanating from an Ion source such as boron trichloride or boron trifluoride. Ion implantation is a faster process than diffusion and can be done at room temperature. It lowers device capacitances allowing higher operating speeds. In addition, Ion implantation lowers and can precisely control device thresholds while delivering a high ratio of field oxide to device threshold.

Micromatrix——(Per Fairchild Semi-Conductor Corporation) Using standard cellular arrays, complete, except for metalization interconnections — each array consists of a predetermined matrix of component pattern cells which may be interconnected to form the required customer circuits. In addition, each cell may be individually customized by cell interconnections to become one of a variety of building blocks, such as AND-OR gates, flip-flops, etc.

Nitride Passivation — The use of silicon nitride instead of silicon oxide as the gate/channel insulating layer resulting in low threshold voltages. The protective properties of nitride passivation may make the hermetic chip a reality.

Polycel — (Per Motorola Semiconductor Company) Very similar to micromatrix, and geared more toward computer aided design——this is also called "Master Slice" or "DRA" (Discretionary Routed Arrays, per Texas Instruments, Inc.).

Silicon Gate — MOS technology using highly doped silicon instead of aluminum for the gate electrode ——in fabrication, the number of masking steps are the same as in conventional MOS but in etching the oxide over the source and drain the polycrystalline silicon acts as a mask preventing the gate oxide from being etched. This results in a precisely-formed, self-aligned gate. Silicon gate technology allows low thresholds compatible with bipolar devices, higher component density, higher speed, and the fabrication of MOS and bipolar devices on one chip.

ADDRESSES OF MANUFACTURERS AND USERS OF LSI MICROCIRCUITS

American Microsystems
3800 Homestead Road
Santa Clara,
California, 95051

Autonetics
3370 East Miraloma
Anaheim,
California, 92803

Bell Telephone
555 Union Boulevard
Allentown,
Pennsylvania, 18103

Boeing Space Center
P.O. Box 3999
Seattle
Washington, 98124

Collins Radio
19700 Jamboree Blvd.
Newport Beach,
California, 92663

Computer Micro Technology
610 Pastoria Avenue
Sunnyvale,
California, 94086

Fairchild
464 Ellis Street
Mountain View
California, 94040

General Digital
19242 Red Hill Avenue
Newport Beach,
California, 92663

General Instrument
600 West John Street
Hicksville,
New York, 11802

Honeywell
13350 U.S. Highway 19
St. Petersburg,
Florida, 33733

Hughes
500 Superior Avenue
Newport Beach,
California, 92663

I.C.E.
4900 East Indian School Rd.
Phoenix,
Arizona, 85018

Intel
365 Middlefield Road
Mountain View,
California, 94040

Intersil
10900 North Tantau Avenue
Cupertino,
California, 95014

Macrodata
20440 Corisco St.
Chatsworth,
California, 91311

Motorola
5005 East McDowell Road
Phoenix,
Arizona, 85008

NCR
16550 W. Bernado
San Diego,
California, 92127

National
2900 Semiconductor Drive
Santa Clara,
California, 95051

Nortec
3697 Tahoe Way
Santa Clara,
California, 95051

Philco-Ford
1400 Union Meeting Road
Blue Bell,
Pennsylvania, 19422

Qualidyne
3699 Tahoe Way
Santa Clara,
California, 95051

Radiation
P.O. Box 37
Melbourne
Florida, 32901

Raytheon
Bedford,
Massachusetts, 01738

RCA
Somerville
New Jersey

Signetics
811 East Arques Ave.,
Sunnyvale,
California, 94086

Solid State Scientific
Commerce Drive
Montgomeryville,
Pennsylvania, 18936

Solitron
8808 Balboa Ave.
San Diego,
California, 92123

Teledyne-Ryan
5650 Kearny Mesa Rd.
San Diego,
California, 92112

Texas Instruments
12201 Southwest Freeway
Stafford,
Texas

TRW
R6/2188
1 Space Park
Redondo Beach,
California, 90278

UNIVAC
P.O. Box 3525
St. Paul,
Minnesota, 55101

Varadyne
10432 North Tantau
Cupertino,
California, 95014

Viatron
105 Terrace Mall
Burlington,
Massachusetts, 01803

Xintel
20931 Nordhoff Street/Box 665
Chatsworth,
California, 91311

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