Report No. 03-71-27

Final Report – Phase II

DEVELOPMENT OF QUALITY STANDARDS FOR BIPOLAR LSI DEVICES

April 1971

For the Period
1 March 1970 through 31 March 1971

Contract No. NAS8-21319
Control No. DCN 1-8-60-00152 (IF) and S1 (1F) and S2 (1F)

Prepared by

Texas Instruments Incorporated
P.O. Box 66027
Houston, Texas 77006

for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

Report No. 03-71-27

Final Report – Phase II

DEVELOPMENT OF QUALITY STANDARDS FOR BIPOLAR LSI DEVICES

April 1971

For the Period
1 March 1970 through 31 March 1971

Contract No. NAS8-21319
Control No. DCN 1-8-60-00152 (IF) and S1 (1F) and S2 (1F)

Prepared by

Texas Instruments Incorporated
P.O. Box 66027
Houston, Texas 77006

for

National Aeronautics and Space Administration
George C. Marshall Space Flight Center
Marshall Space Flight Center, Alabama 35812

ACKNOWLEDGMENT

This report was prepared by Texas Instruments Incorporated under Contract No. NAS8-21319, "Development of Quality Standards for Bipolar LSI Devices," for the George C. Marshall Space Flight Center of the National Aeronautics and Space Administration. The work was administered under the technical direction of the Quality and Reliability Assurance Laboratory of the George C. Marshall Space Flight Center.

TABLE OF CONTENTS

TABLE OF CONTENTS (Continued)

LIST OF ILLUSTRATIONS

LIST OF ILLUSTRATIONS (Continued)

LIST OF TABLES

SECTION I

INTRODUCTION

This final report summarizes the program activities of Phase II on Contract No. NAS8-21319.

The program objectives for Phase II follow.

- Study the parametric and functional characteristics of bipolar LSI devices and, as a result, establish a philosophy for conduction of electrical tests consistent with the anticipated high-reliability application of bipolar LSI.
- Study the strengths of bipolar LSI devices when subjected to simulated aerospace environments and, as a result, analyze the strength of bipolar LSI devices.
- Analyze the design considerations for bipolar LSI and establish the applicability of certain design rules and guidelines to help assure reliable LSI units.
- Assist another MSFC (Vanzetti Infrared and Computer Systems, Boston, Massachusetts) in evaluation of LSI characteristics, using infrared techniques.

These objectives are discussed in subsequent sections of this report.

Comprehensive analysis of the infrared testing program was believed beyond the scope of Contract No. NAS8-21319. Previous reports have concerned parts and assistance supplied to Vanzetti Infrared and Computer Systems; consequently, further discussion has been omitted from this report.

SECTION II

RESULTS AND ANALYSIS OF TEST PROGRAMS

A. MECHANICAL TESTS

1. Definition of Test Device

A special test device was designed and fabricated for use in the mechanical and thermal testing program. This is shown in Figures 1 and 2. The test patterns follow:

- Pattern I. This is of continuous metal with both second- and third-level patterns connected in series. The third-level metal lines were opened by capacitor discharge and repair wire bonds were made to test the integrity of repair bonding on the slice surface.
- Pattern II. This pattern was used primarily to test the integrity of metallization deposition over steps in the oxide (that result from underlying metal and oxide layers). It consists of a pattern on third-level metallization structured at a right angle to the pattern on second level. In this way, 180 oxide steps are generated in a continuous metal run.
- Pattern III. This was designed as an additional measure of the integrity of slice repair procedures. At times, in even the well-controlled multilevel process, it becomes necessary to repair directly on the slice surface. One of the repair procedures includes wire bonding onto pads that include via connections to the underlying metal. That is, a ball of the repair wire bond must be placed directly over a feedthrough (via) that interconnects 2nd and 3rd metal lines. This test pattern duplicates this occurrence when repair wire bonding is added. Resistance measurements were utilized to monitor the integrity of this test pattern and bonds.
- Pattern IV. This consists of 92 series-connected feedthroughs. Initial-resistance and final-resistance measurements provide an indication of feedthrough reliability as a function of environmental stresses.

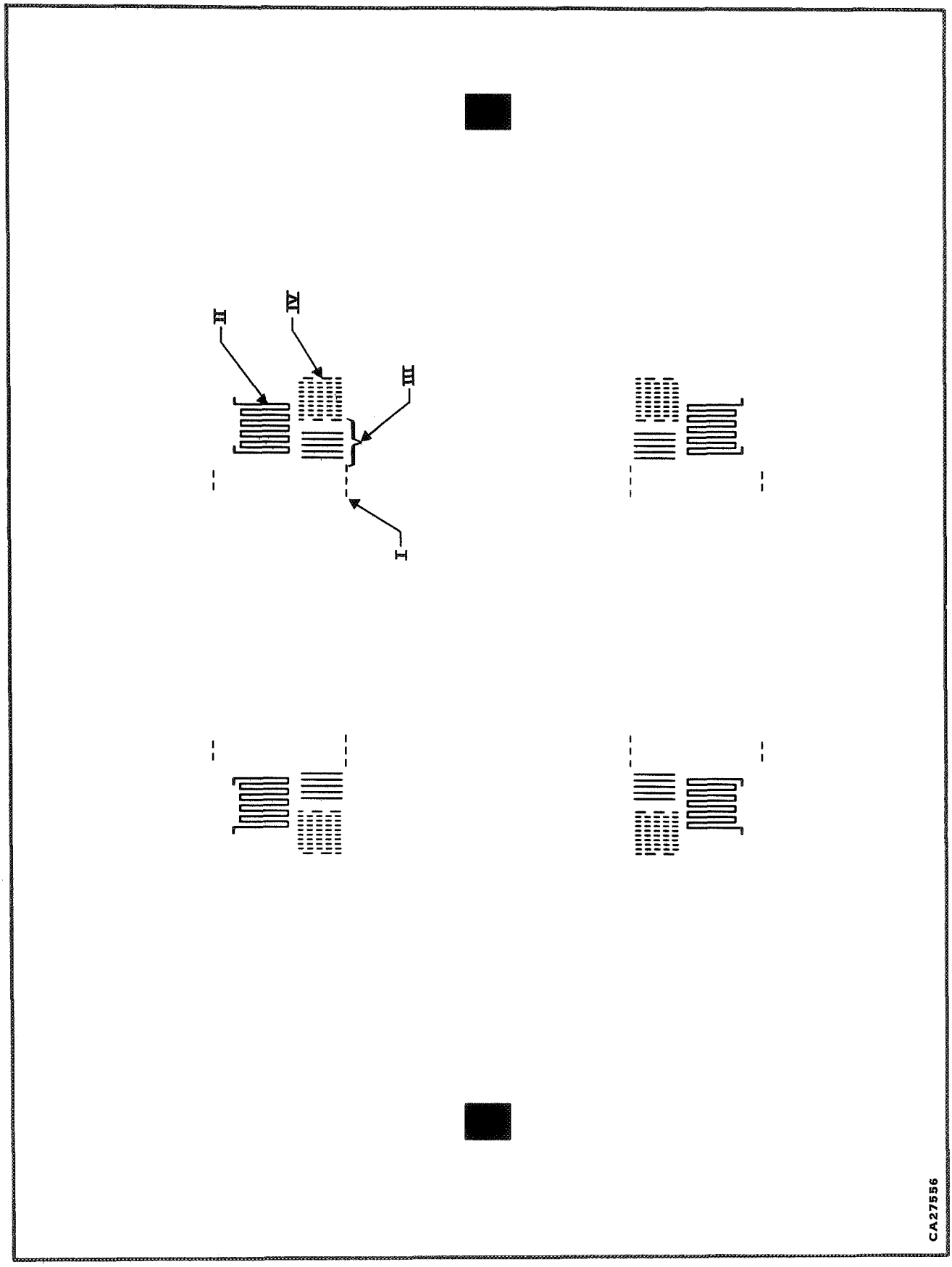


Figure 1. Environmental Test Vehicle (Second-level metal approximately 10X)

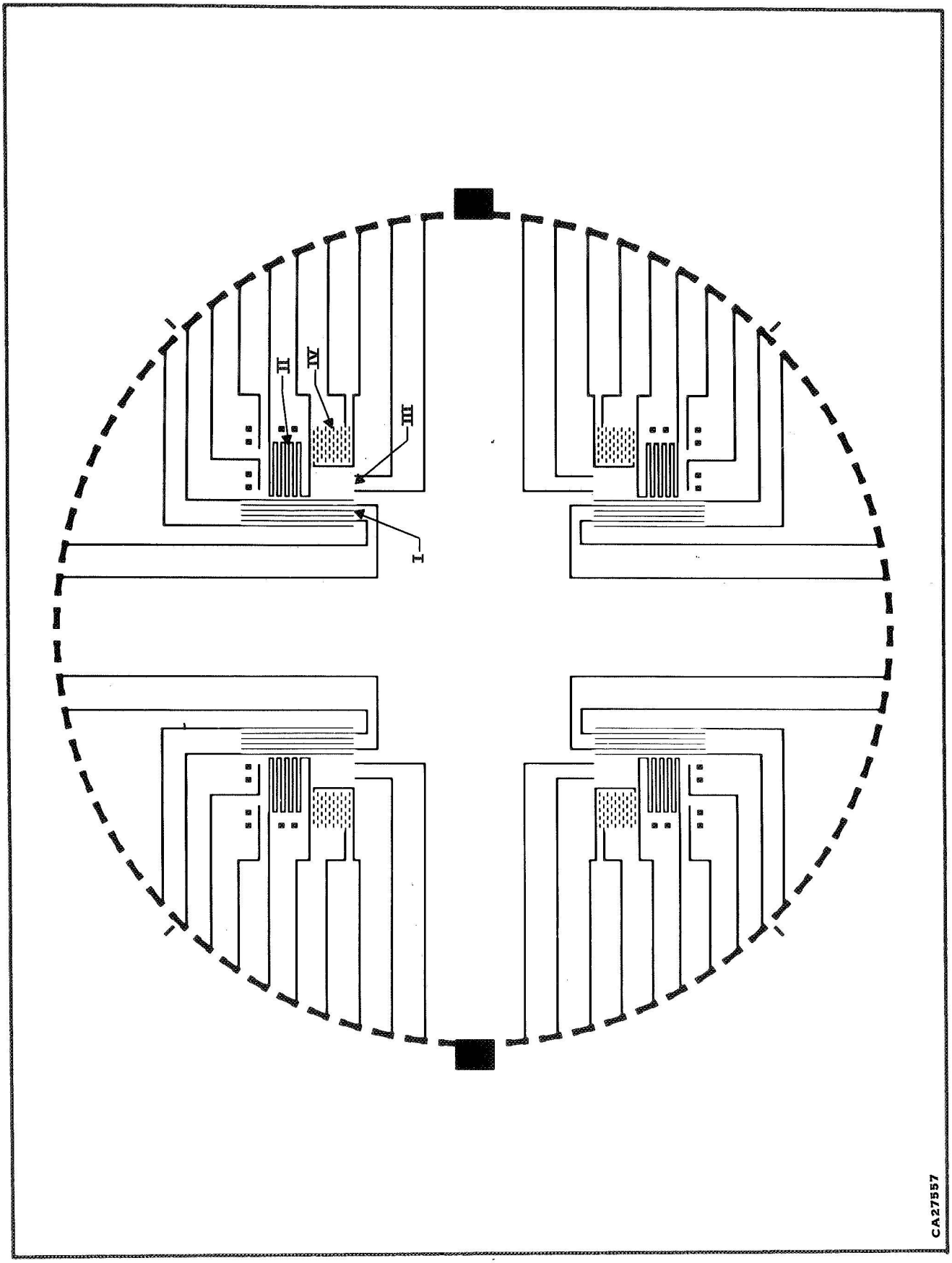


Figure 2. Environmental Test Vehicle (Third-level metal)

2. Test Sequence for Mechanical Testing

The mechanical testing sequence consisted of the testing flow shown in Figure 3. As indicated, the five units manufactured for this testing were run sequentially through the tests to each successively higher stress level.

The variable-frequency vibration tests were run through condition C of MIL-STD-883, Method 2007. Constant acceleration tests progressed through 1000 G's peak acceleration tested according to MIL-STD-883, Method 2001 in X1 and Y1 directions. This stress level, although not nearly as severe as IC stress levels (30,000 G's typical, maximum), is more severe than anticipated system stress levels. For example, MIL-STD-810B specifies maximum anticipated system stress levels of 30 G's.

The constant acceleration test of MIL-STD-883 is performed primarily to evaluate the integrity of the wire bonds of the array. To apply forces to actually stress the bond wires, the constant acceleration test must be run to at least 20,000 G's.

However, in the case of LSI devices (including full slice LSI and MOS/LSI in larger packages), acceleration testing at greater than 5000 G's produces a test not of wire bonds, but of the package.

In most cases, the ceramic packages (viz., 2.125-inch X 2.125-inch ceramic header) will be destroyed before stress levels necessary to actually test bonds are reached.

The mechanical test units were ultimately processed through mechanical shock (condition D, Method 2002 of MIL-STD-883) to 5000 G's. One device had to be removed from test after mechanical shock to condition C; the device came loose from the mechanical shock fixture and was damaged.

The remaining units were processed through condition D, mechanical shock, without further failure. During shock testing to 10,000 G's, it became evident that the fixture would not allow testing the 2.125-inch X 2.125-inch package. The mechanical tests were terminated at this stage. The results are shown in Table I and analyzed in the following section.

3. Results of Mechanical Tests

The results of mechanical tests, shown in Table I, indicate that, when subjected to mechanical stresses consistent with package size, the LSI package performs quite well.

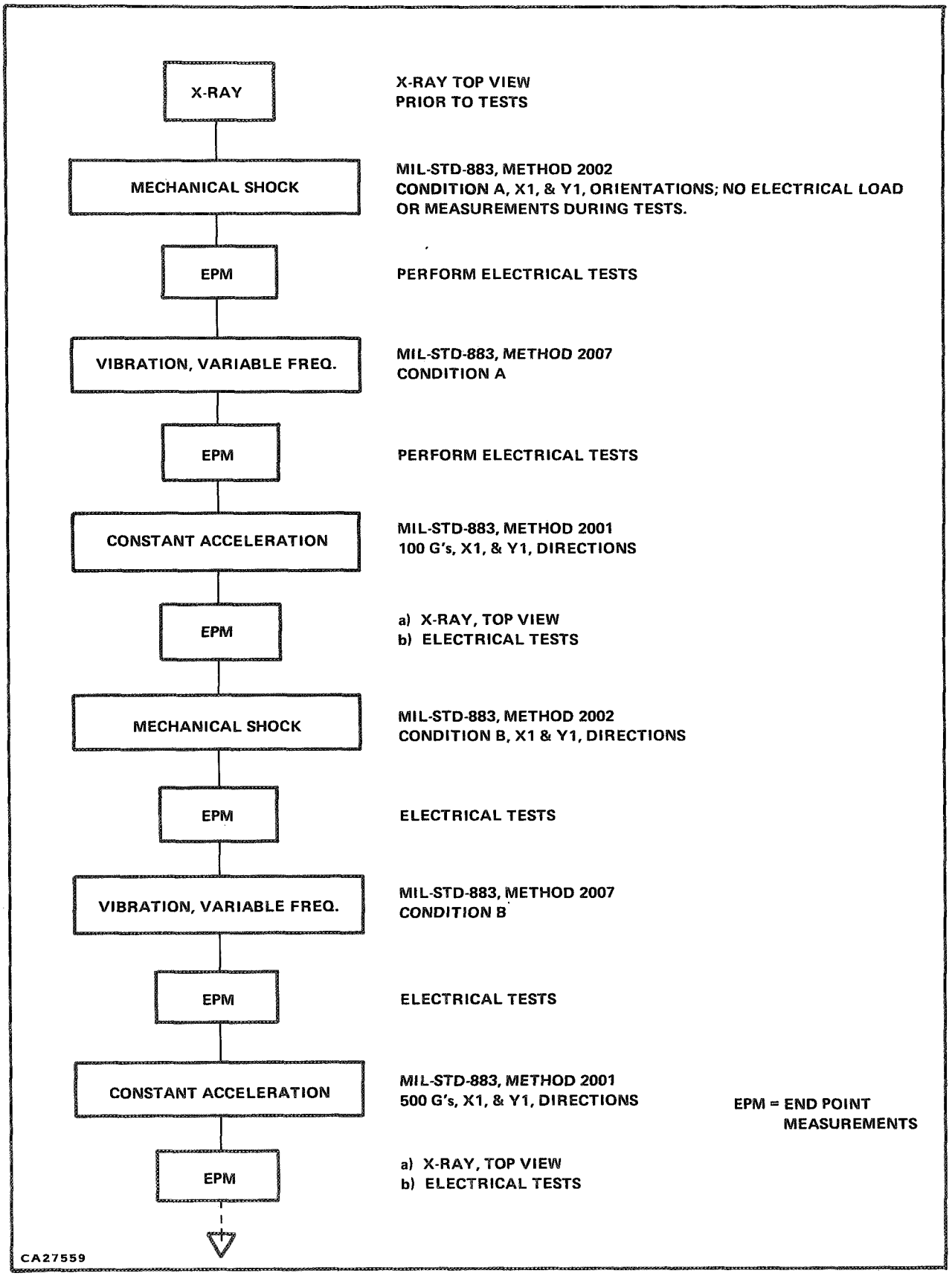


Figure 3. Mechanical Shock Test Sequence (Sheet 1 of 2)

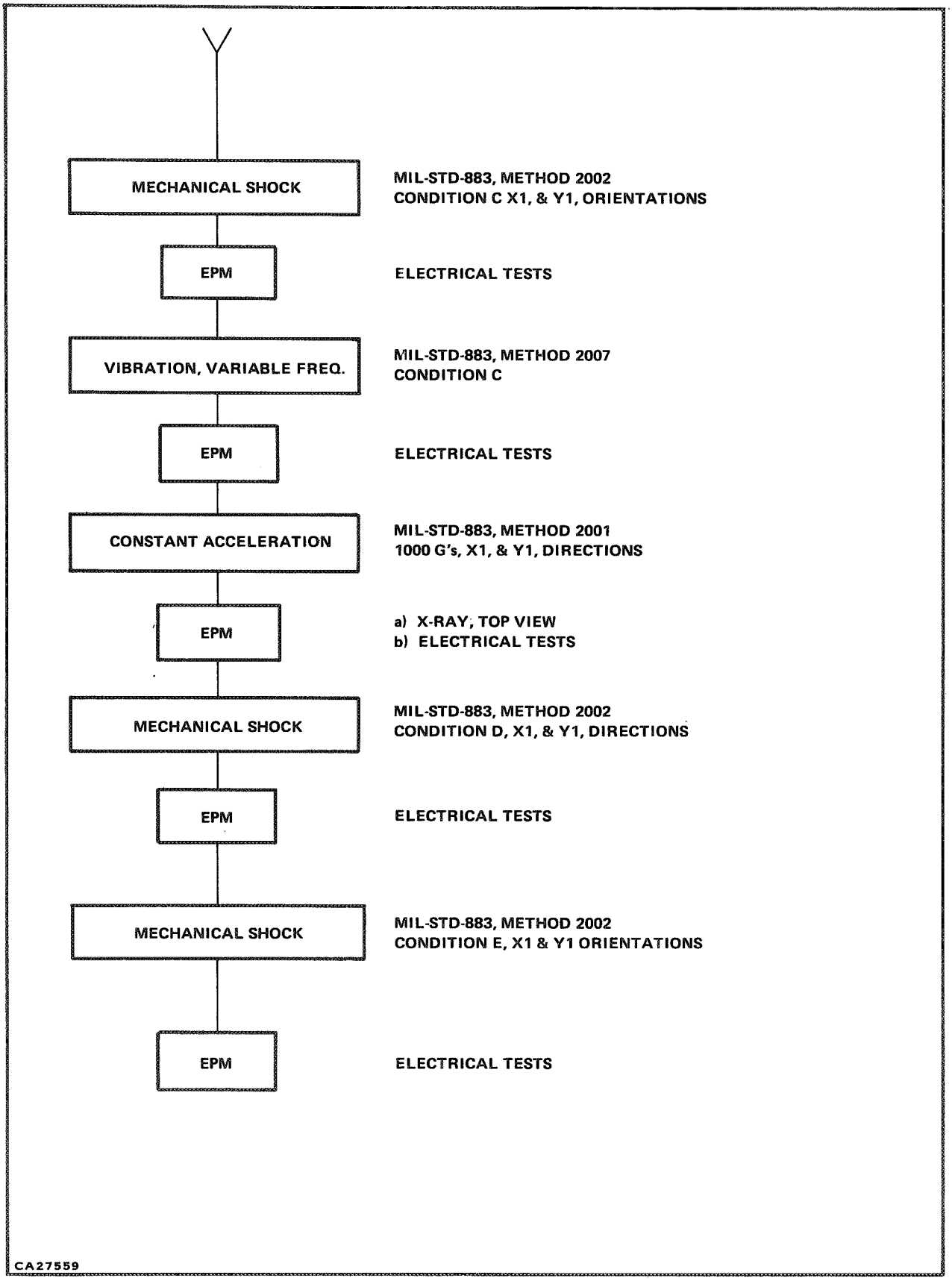


Figure 3. Mechanical Shock Test Sequence (Sheet 2 of 2)

Table I. Mechanical Test Sequence Results

Test–MIL-STD-883 (Method Shown in Fig. 3)	Device No.	Total Continuity Measurements/No. of Opens	Total Additional Opens per Test
Mechanical Shock 500 G's	1-SN2404	24/1	
	2-SN1912	23/0	
	3-SN1816	24/0	1
	4-SN2409	24/0	
	5-SN1718	24/0	
Vibration, Variable Freq.; 20 G's	1	23/0	
	2	23/0	
	3	24/0	0
	4	24/0	
	5	24/0	
Constant Acceleration, 100 G's	1	23/0	
	2	23/0	
	3	24/0	0
	4	24/0	
	5	Broken when being inserted in fixture	
Mechanical Shock, 1500 G's	1	23/0	
	2	23/0	
	3	24/0	0
	4	24/0	
Vibration, Variable Freq.; 50 G's & Acceleration, 500 G's	1	23/0	
	2	23/0	
	3	24/0	0
	4	24/0	
Mechanical Shock, 3000 G's	1	Unit thrown off shock fixture & damaged	
	2	23/0	
	3	24/0	0
	4	24/0	
Vibration, Variable Freq.; 70 G's	2	23/0	
	3	24/0	0
	4	24/0	
Constant Acceleration, 1000 G's	2	23/0	
	3	24/0	0
	4	24/0	
Mechanical Shock, 5000 G's	2	23/0	
	3	24/0	0
	4	24/0	
Mechanical Shock, 10,000 G's	Test Could Not Be Completed Due to Size of Package.		

The only failure was "1," which failed continuity measurement after the initial mechanical shock test to 500 G's. The cause of this failure is believed to have been a discrepant repair bond wire. This particular device was later damaged during the mechanical shock testing and the cause of the discrepant continuity measurement could not be determined. As the units progressed through the mechanical test sequence, no further continuity failures were seen. As shown in Table I, two devices were damaged during the test sequence due to failures in the test fixtures.

The mechanical test results indicate the good mechanical stability of the LSI packaging system. There was some concern that the Sylgard compound used to encapsulate repair bond wires on the slice surface would be pulled loose during mechanical tests and would subsequently damage bonds. The results indicate that the repair-bond encapsulating technique does not compromise the mechanical integrity of the array.

Since most of these tests are at stress levels considerably greater than those normally associated with a system (or subsystem), it can be concluded that the replacement of a system of ICs on boards with a single LSI array can substantially improve the mechanical integrity of the system.

B. THERMAL TESTS

1. Definition of Test Vehicle

To determine the integrity of LSI arrays when subjected to thermal stresses, test devices identical to those described in Section II-A were manufactured.

These test units were processed through the environmental test seequence shown in Figure 4.

Table II summarizes the results of the temperature-testing program, showing open circuits determined by the continuity measurements taken as electrical end-point measurements (EPM).

A discussion of the failures indicated in Table II is appropriate.

As shown in Section II-A, the test devices consist of 24 resistance paths tied to external pins so that continuity measurements can be performed to ascertain the integrity of the multilevel metal and repair bonding on the slice surface.

The failed continuity measurements shown in Table II were analyzed after the test units had been subjected to the entire test sequence, which resulted in cracked ceramic headers in three of the four test devices remaining in the test sequence for the last thermal shock. Analysis showed, in all cases, the failures were attributable to broken repair wires on the slice surface.

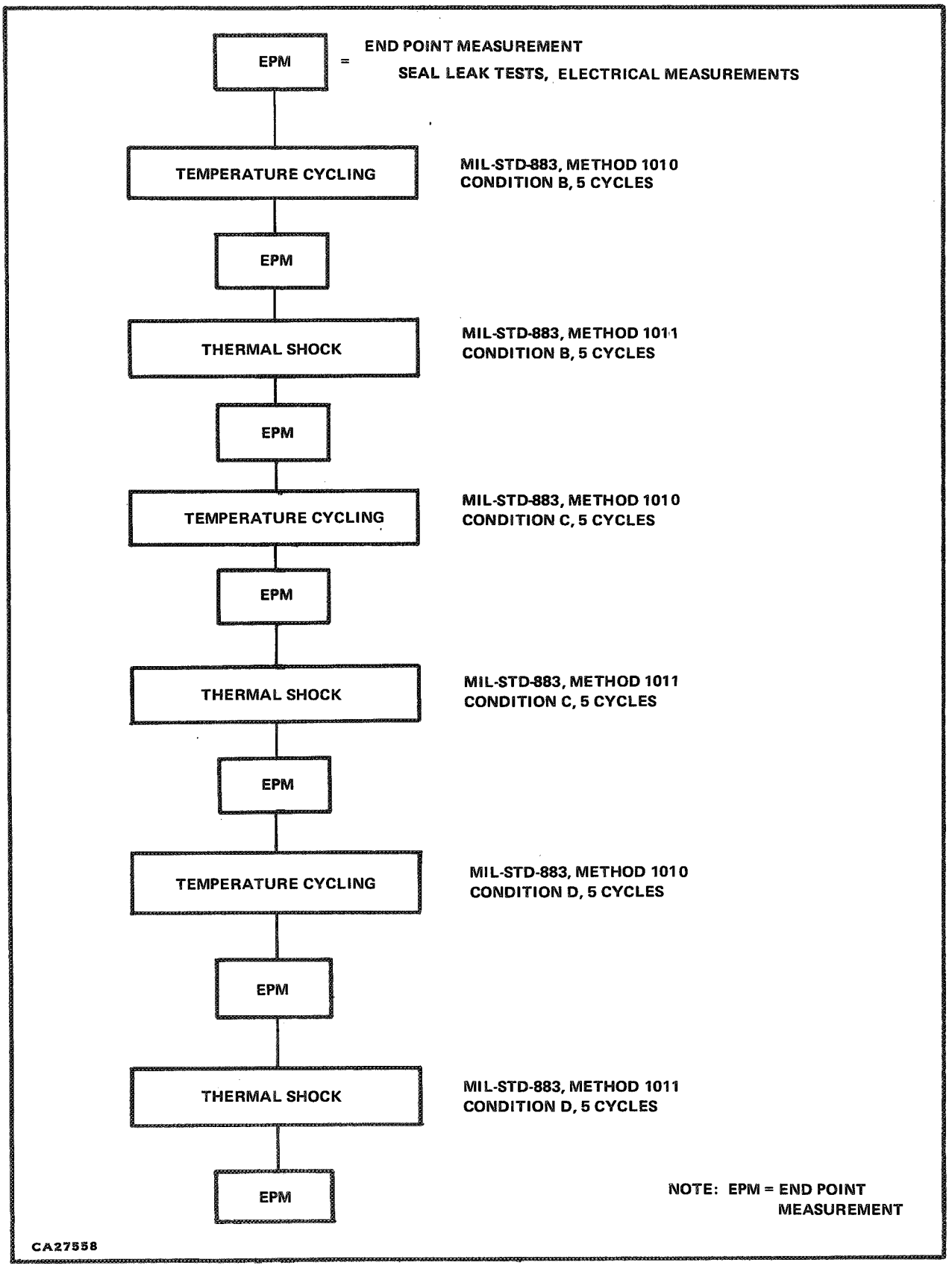


Figure 4. Thermal Shock Test Procedure

Table II. Temperature Test Sequence Results

Test–MIL-STD for 5 Cycles	Device No.	Total Continuity Measurements/No. of Opens	Total Additional Opens per Test
Temperature Cycling (–55 to +125°C)	1-SN1817	24/4	
	2-SN2402	23/0	
	3-SN1801	22/3	10
	4-SN2018	23/2	
	5-SN2110	24/1	
Thermal Shock (–55 to +125°C)	1	20/0	
	2	23/0	
	3	19/3	5
	4	21/1	
	5	23/1	
Temperature Cycling (–65 to +150°C)	1	20/0	
	2	23/0	1
	3	16/0	
	4	20/1	
	5	22/0	
To evaluate cause for failures, device SN1817 was removed from test and decapped for analysis.			
Thermal Shock (–65 to +150°C)	2	23/0	
	3	16/0	1
	4	19/0	
	5	22/1	
Temperature Cycling (–65 to +200°C)	2	23/0	
	3	16/1	1
	4	19/0	
	5	19/0	
Thermal Shock (–65 to +200°C)	2	Ceramic crack	
	3	15/1	1
	4	Ceramic crack	
	5	Ceramic crack	

The photograph of Figure 5 shows a typical failure of a repair wire on the slice surface. All of the failures analyzed showed wire breakage at the stitch of repair wire bonds.

A discussion of the mechanics and restraints inherent in the repair bonding of an LSI slice with isolated faults in the multilevel metallization system is appropriate.

As reported previously on Contract NAS8-21319, Phase I, to mount full-slice LSI units, the slice-mount-to-header system must not be so rigid as to allow stresses resulting from normal thermal coefficient difference between silicon and alumina (as well as warping forces due to thermal

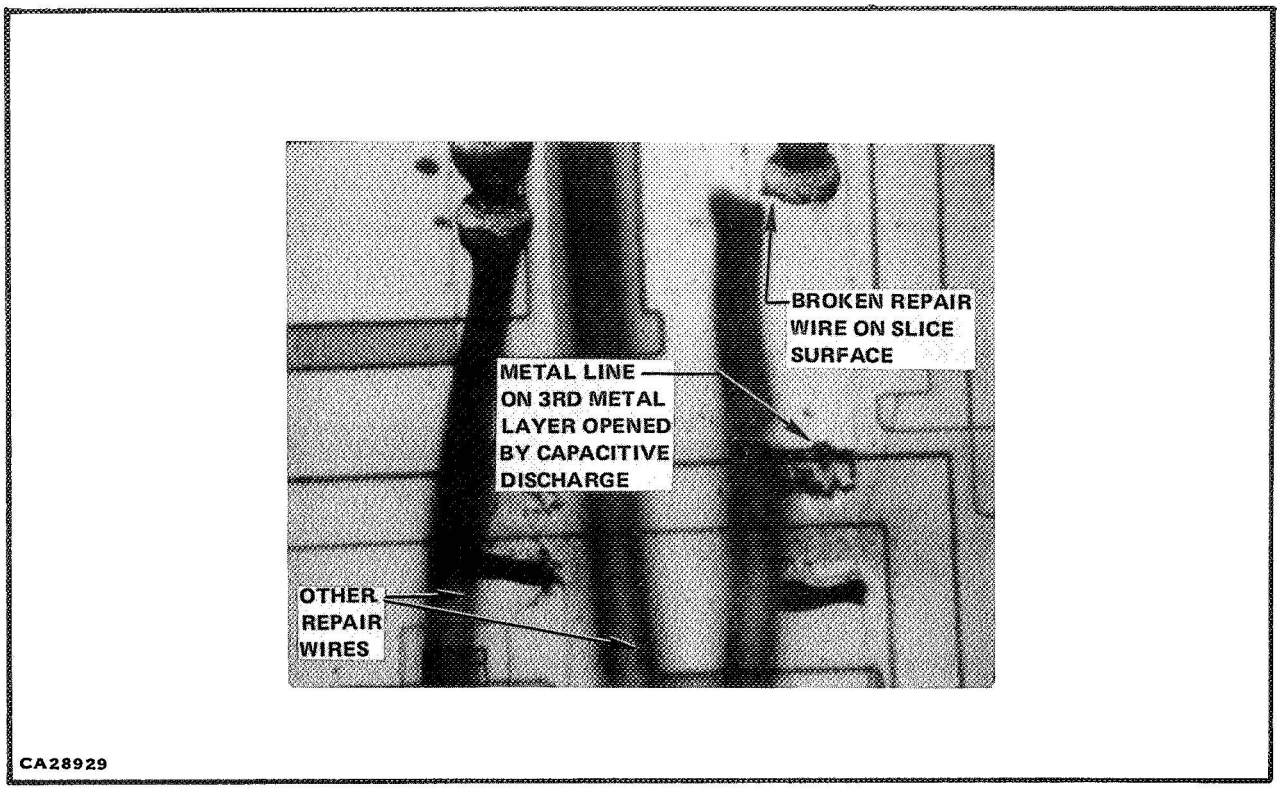


Figure 5. Typical Repair-wire Failure at Stitch

gradients across the silicon slice) to be transmitted to the silicon. Additionally, producing a ceramic header with a 1.5-inch-diameter mounting surface with sufficient flatness to use a "solid" mounting scheme is economically impractical. For these and other reasons, TI has chosen to utilize a thermally cured epoxy mounting compound to mount the slices to the header surface. This epoxy is cured at 150°C, and has a limited temperature range over which it has useful integrity. Therefore, the gold-wire ball-bonding operation must be performed with slice temperature less than 200°C. Normal gold-wire ball-bonding operations utilize machine set-up conditions that heat the substrate (chip) to greater than 300°C. Since gold-wire ball-bonding techniques are based on the interrelationship of temperature and pressure to form a thermocompression bond between the wire and slice metallization, the machine set-up conditions must maintain capillary temperature greater than typical to compensate for the lower substrate temperature. The resulting departure from typical thermocompression bonding machine setup introduces new process-control problems.

For example, utilization of capillary temperatures greater than 200°C causes repeatability problems. As the capillary temperature rises, the weight used to effect the thermocompression bonds tends to cut through the gold wire. This tendency seems to necessitate rigid operator and machine controls to ensure that overbonding does not occur at the stitch end of the bond wire, resulting in severed, or unduly reduced, cross sections of the wire at the stitch.

Implementation of high-reliability systems utilizing full-slice LSI would have to recognize the possible reliability variance due to repair bond failures and implement process controls (during the bonding operation) to assure repeatability for this operation.

2. Thermal Test Results

The results of the thermal testing are shown in Table II. This indicates the open continuity measurements detected after each stress level of the test sequence.

Examination of the internal structure of the test devices (Figure 2) shows that, after the initial open occurs, unless the device is decapped for analysis, it is impossible to determine the total number of bonds that has failed through a particular stress level of testing. For this reason, it is impossible to determine a percent failure for each level of stress.

An added variable in the analysis of failures after decapping is the Sylgard-removal process to de-incapsulate the repair wires on the slice surface. The Sylgard stripping agent has a tendency to expand the Sylgard and, thereby, destroy bond wires that were intact prior to Sylgard stripping.

Due to the number of failures experienced in the thermal testing, the absolute number of failures with respect to total bonds is relatively unimportant. Of more concern is the failure mechanism seen in the devices.

The summary of thermal test results in Table II can be restructured to the form of Table III. As shown, the failures detected in various stages of thermal testing indicate that the failing areas of the devices are all limited to Test Pattern I – This is the area where multiple bonds with several crossovers (wire over wire) occur. Due to the repair techniques, this necessitates encapsulating the bond wires with Sylgard and results in a buildup of Sylgard wherever wire crossovers occur.

Analysis of the failure of pre- and post-Sylgard removal showed bond failures (previously indicated as in Figure 5). It is believed that these failures occurred due to difficulty in maintaining a repeatable bonding operation, primarily because the bonding-machine setup (previously discussed) allowed more bond dependency on operator techniques than should be the case.

In the normal repair-bonding sequence, the bonder makes only one or two bonds per device at a given time. The test devices necessitated placing approximately 84 bonds on a given device. This drastic increase in total bonds over normal bonding practices caused the operator to use less care in bonding procedures.

Table III. Regrouped Temperature Test Results

Array No.	Stress Level MIL-STD-883 (5 Cycles)	No. of Additional Continuity Failures	Test Patterns Failing*	Predominant Failure Mechanism
1,2,3,4,5	−55 to 125°C (T. Cycle)	5,0,3,2,1	I	Broken stitches
1,2,3,4,5	−55 to 125°C (T. Shock)	0,0,3,1,1	I	Broken stitches
1,2,3,4,5	−65 to 150°C (T. Cycle)	0,0,0,1,1	I	Broken stitches
2,3,4,5	−65 to 150°C (T. Shock)	0,0,0,0	–	–
2,3,4,5	−65 to 200°C (T. Cycle)	0,1,0,0	I	Broken stitches
2,3,4,5	−65 to 200°C (T. Shock)		I (Unit 3)	Broken stitches

Device numbers correspond to failures; i.e., at −55 to +125°C, array 1 had 5 failed continuity measurements.

*See page 66, Section IV-B-3, for description of test patterns.

The bonding defects, that subsequently were evidenced as testing failures, indicate a potential failure on LSI devices quite difficult to visually screen after the bonding is performed. Inspection of the failed stitches after Sylgard removal showed stitch bonds that would pass the criteria of MIL-STD-883, Method 2010.1, Paragraph 3.2.4.2, (visual inspection of wedge bonds). At the same time, adjacent bonds that appeared to have almost identical stitch bond characteristics remained intact after all testing (including the slice cracks caused by the final thermal shock). Figures 6 and 7 show several bonds after thermal stressing. Figure 6 shows a wire failure and Figure 7 shows a wire that remained intact.

In summary, several practices need close surveillance to ensure reliable repair bonds (No problem was evident on slice-to-package bonds). These practices are:

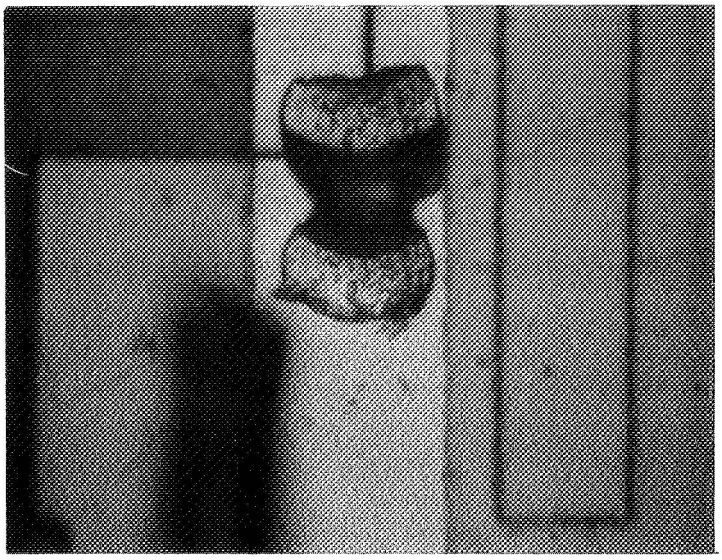
a) Tight controls on bond machine setup conditions

b) Minimization or elimination of repair bond crossovers that result in a buildup of Sylgard in certain areas of the slice

c) Assurance that bonding operators exercise caution in repair bonding. Since the typical number of repair bonds is small, greater care can be exercised on LSI devices than would be typical on SSI products, where throughput is considerably greater.

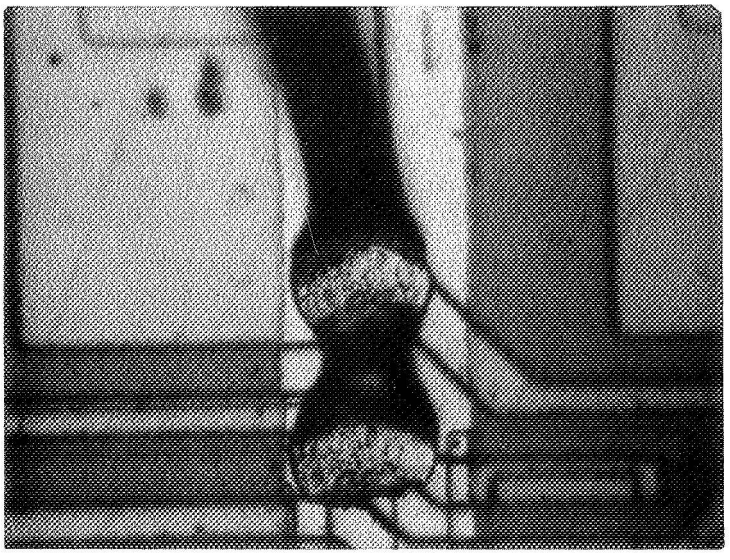
d) In-line screens for bond integrity by visual methods do not appear adequate to ensure reliable bonds. Several approaches should be investigated and/or specified to ensure repair bond integrity.

- A type of "nondestructive" bond test should be investigated for LSI process monitoring.



CA28930

Figure 6. Bond Failure Due to Broken Stitch



CA28931

Figure 7. Adjacent Bond Intact After All Testing

- Real-time bond monitoring systems should be investigated to ensure the quality of the bonding system, including optimization of machine setup and repeatability of operation.
- A reliable destructive sampling system on each unit to monitor bond quality by pulling a certain percentage of bonds made (extra bonds) should be implemented.

C. MOISTURE-RESISTANCE TESTS

1. Definition of Test Vehicle

The moisture-resistance test vehicle is structured as shown in Figure 8. This illustration shows the second-level metallization that was applied over first-level metal, with an insulating oxide layer between the two. The basic wafer was an electrical reject unit after first metal. These reject units (rather than origin slices without first metal or diffusions) were used so that typical multilevel surface contours would be obtained. The top layer of metal (the actual test pattern) was molybdenum-gold to simulate the normal third-level metallization.

The four slices were installed in hermetic packages and gross and fine-leak tested. Of the four devices, three were determined to be hermetic to $< 5 \times 10^{-6}$ atm/cc/sec; the fourth failed the gross-leak test.

It was believed that, to determine device capabilities, it would be advantageous to test both hermetic and nonhermetic devices simultaneously.

2. Test Sequence and Results

The units described in the previous section were subjected to the test sequence shown in Figure 9.

The initial and post-test leakage measurements are shown on the curves of Figure 10.

The measurements indicated were performed on all of the test devices simultaneously. Each slice has the five test patterns shown in Figure 9. Since all devices were measured for leakage current simultaneously, there were actually 20 (4 X 5) test patterns in parallel.

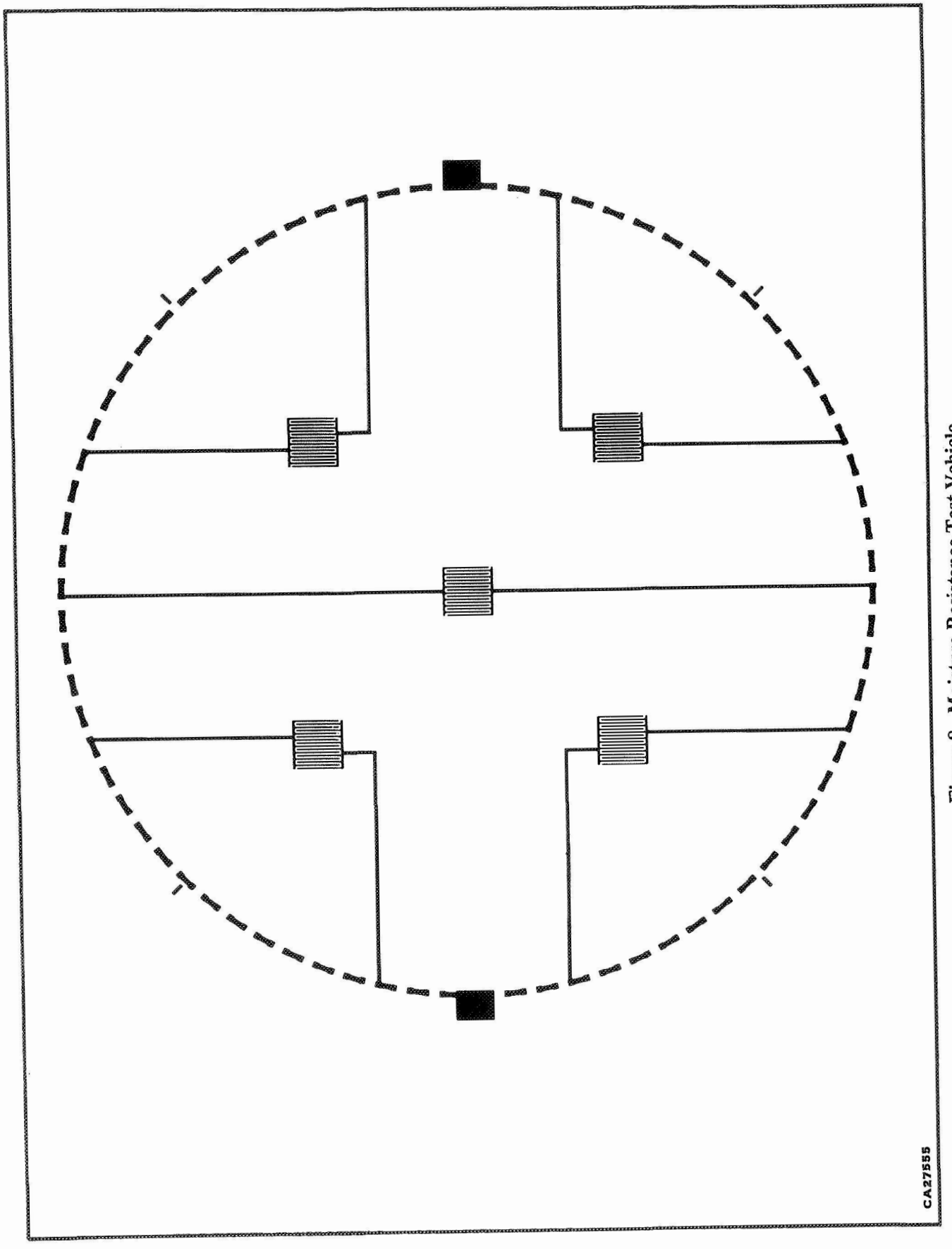


Figure 8. Moisture Resistance Test Vehicle

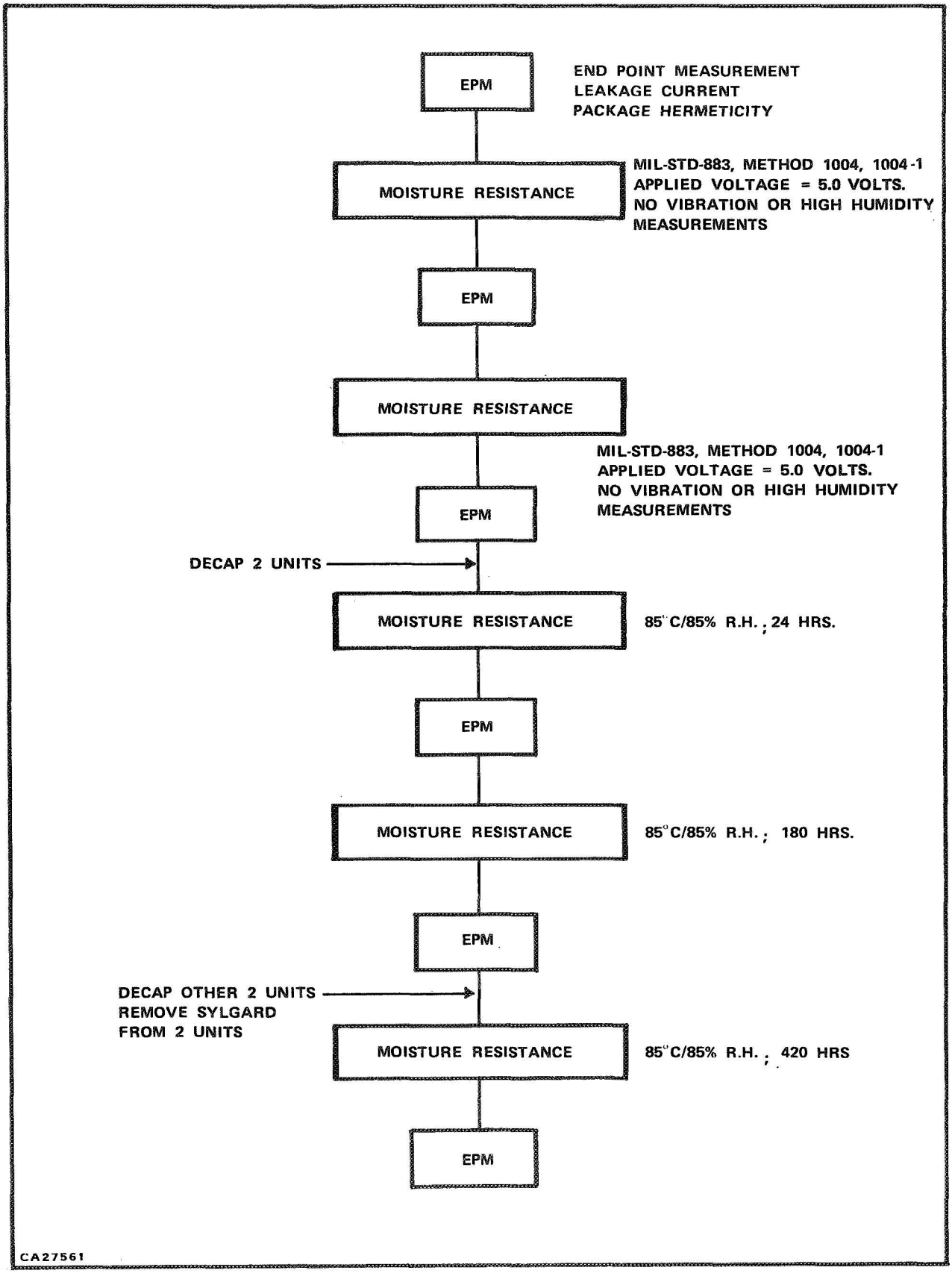


Figure 9. Moisture Resistance Test Sequence

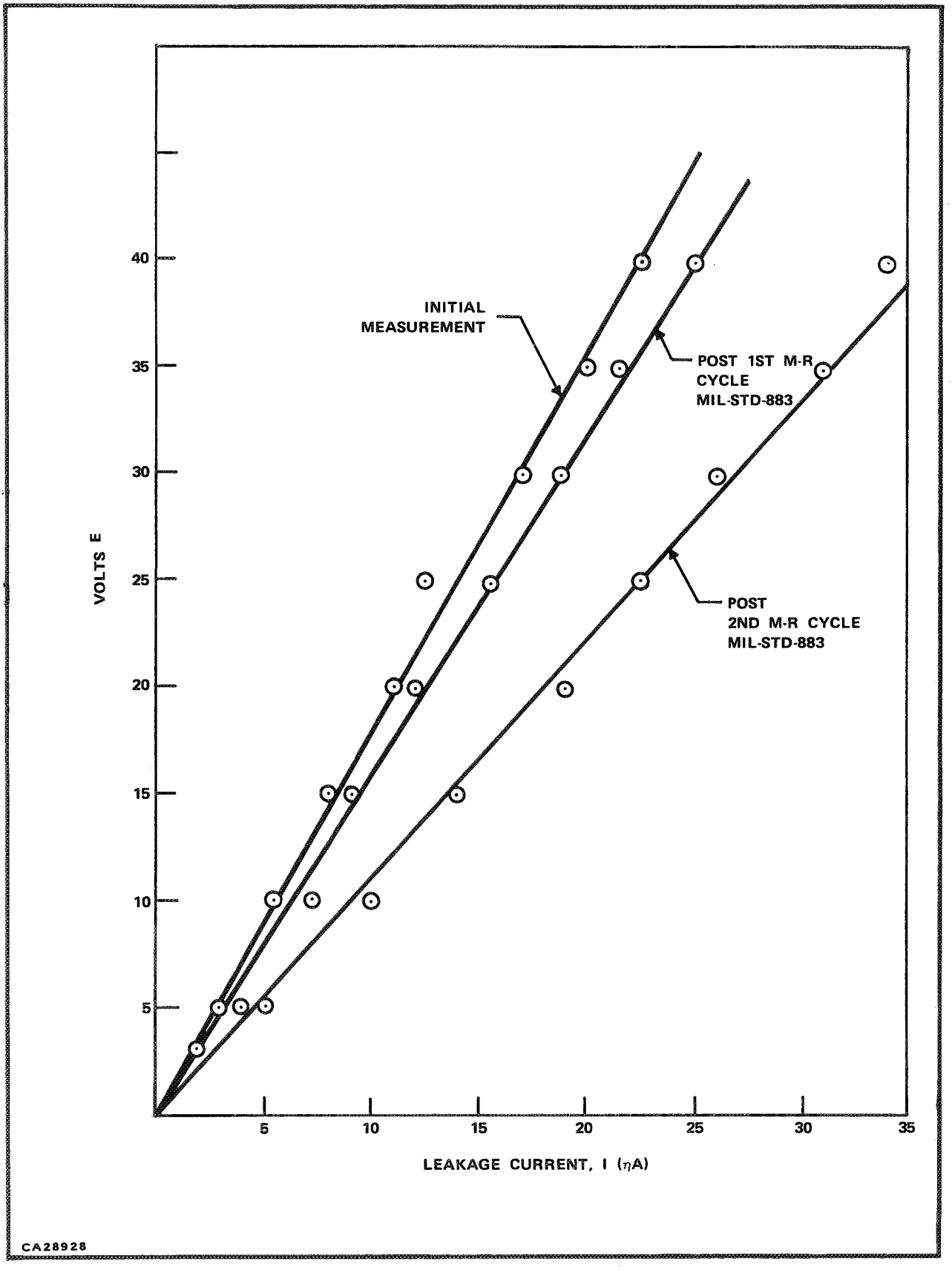


Figure 10. Moisture Resistance Test – Leakage Measurements

There were 20 leakage patterns in parallel; the total drift in leakage, after two passes through MIL-STD-883, Method 1004-1, showed an increase of only 11.2 nanoamperes. Taking an average of the 20 test patterns shows only an increase of (11.2 nanoampere/20) 0.56 nanoampere after testing. Inspections before and after testing did not reveal visual anomalies on any of the tested units.

To further identify the capabilities of LSI devices to withstand moisture-resistance tests, the lids were removed on two of the four test devices; the Sylgard was left on the surface of the two decapped units.

After 24 and 180 hours of 85°C and 85% relative humidity exposure, the four units in parallel had measured leakages as shown in Figure 11. As seen, no significant increase in leakage was apparent at either the 24-hour or 180-hour leakage tests.

For a final test, the remaining two units were decapped and the four units (two with and two without Sylgard) were installed on the 85°C/85% relative humidity moisture-resistance test. Figure 12 shows the visual effects of the final moisture test on decapped units, both with and without Sylgard. This last test duration was an additional 420 hours on 85°C/85% moisture testing.

Leakage measurements on the two units with Sylgard, after the no-lid testing on 85°C/85% relative humidity, showed a maximum leakage of 5 nA @ 40 volts. The units without Sylgard, to be expected from the photomicrograph of Figure 12, could not be quantitatively measured due to erratic leakage measurements; the readings were significantly higher than the units with Sylgard.

D. Life Tests

1. Definition of Test Vehicle

Figure 13 is a cross-sectional view of the LSI wafer fabrication through first metallization. The wafer processing of Figure 14 has interconnected the components on the silicon slice into the cellular pattern shown in Figure 15.

Each of the cells shown in Figure 15 is further defined in Figures 16, 17, 18, and 19 by the definitization of input-output pads for each cell type.

The basic semiconductor slices, defined above, must now be discretionarily routed, through utilization of the multilevel interconnection generation system, into a functioning monolithic LSI array.

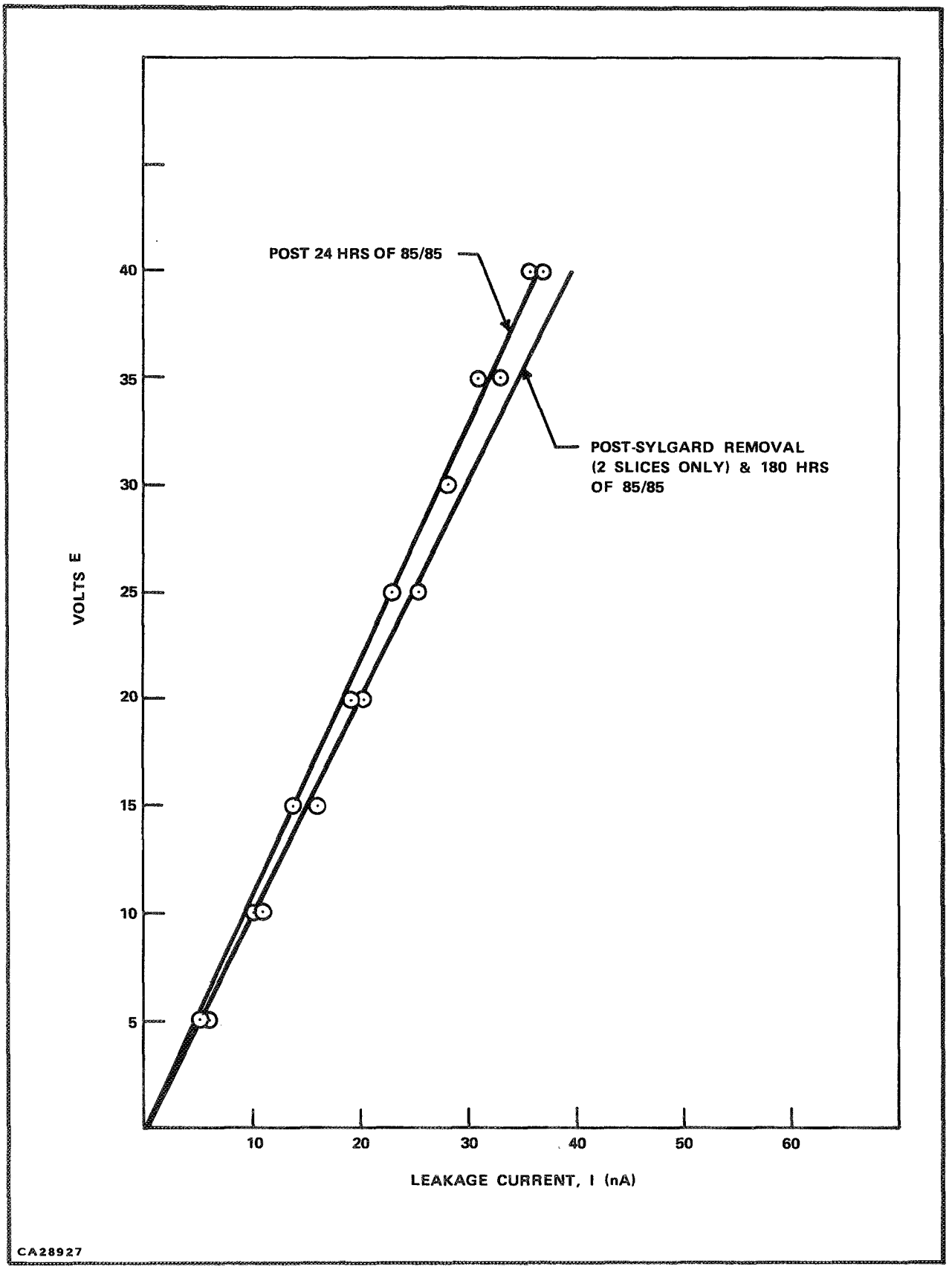
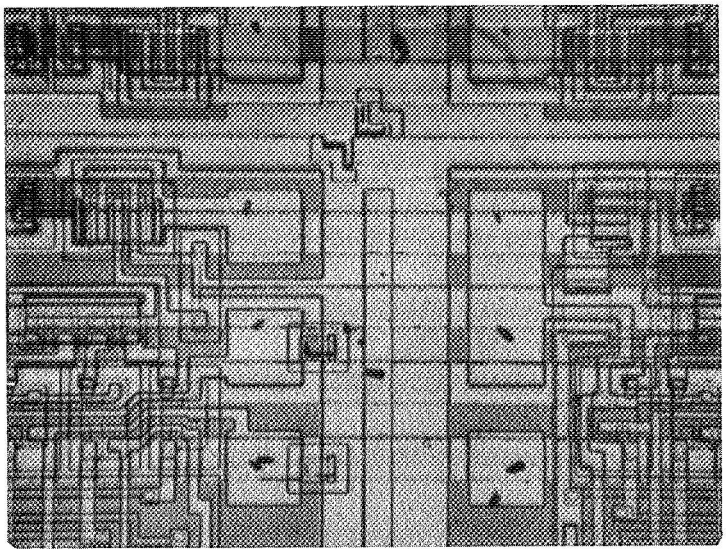
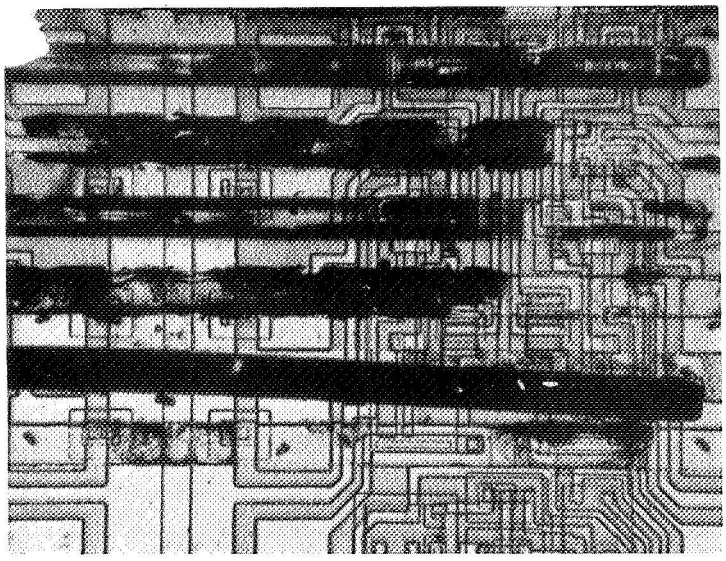


Figure 11. Moisture Resistance Test – Leakage Measurements



SAMPLE UNIT WITH SYLGARD
AFTER ALL TESTING

NO VISUAL ANOMALIES



SAMPLE UNIT WITH SYLGARD
REMOVED FOR FINAL 600 HRS
ON 85°C/85% R.H.

VISIBLE CORROSION

CA28926

Figure 12. Photomicrographs: Units Placed on 85°C/85% RH Test
(with and without Sylgard)

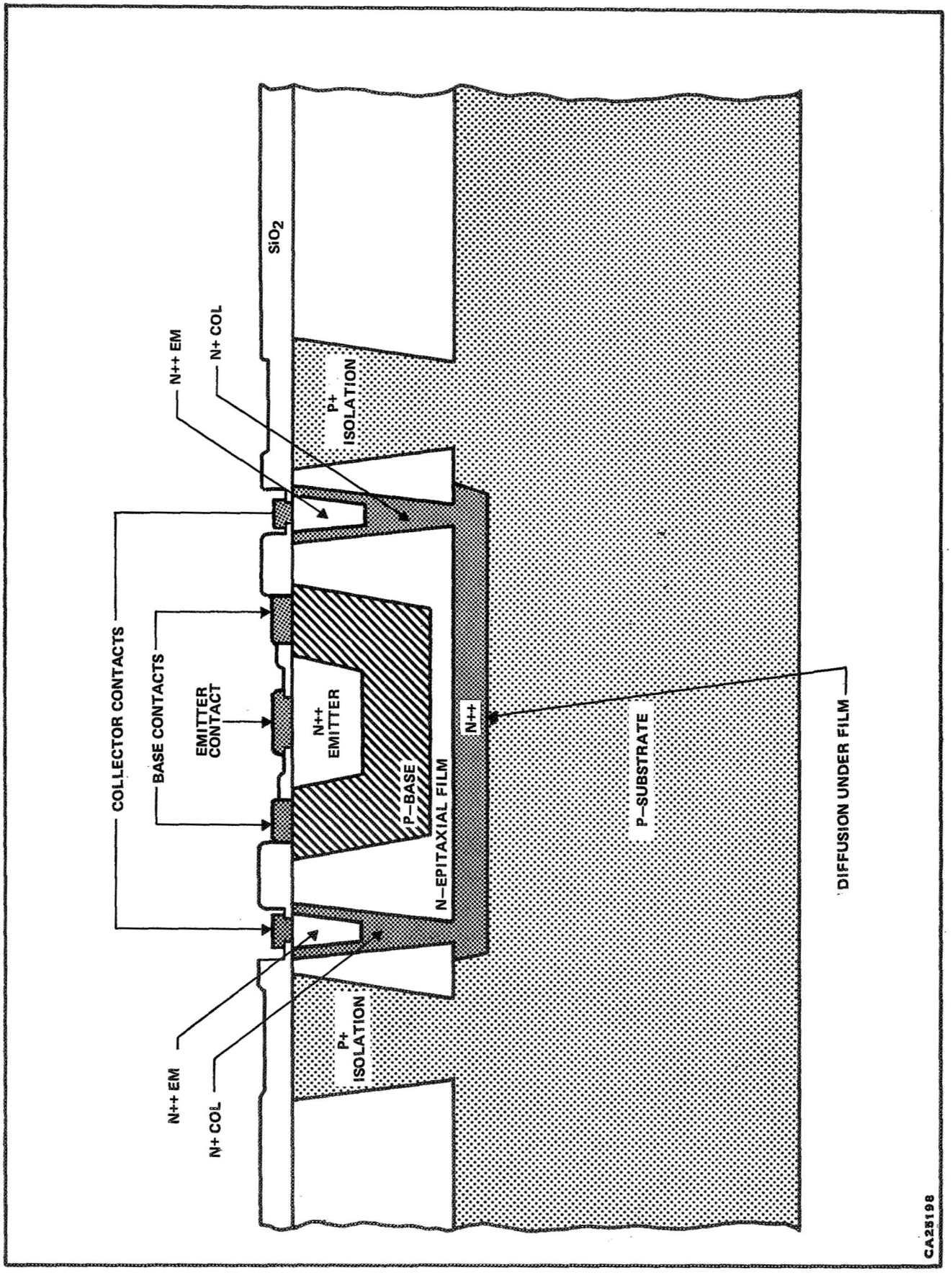
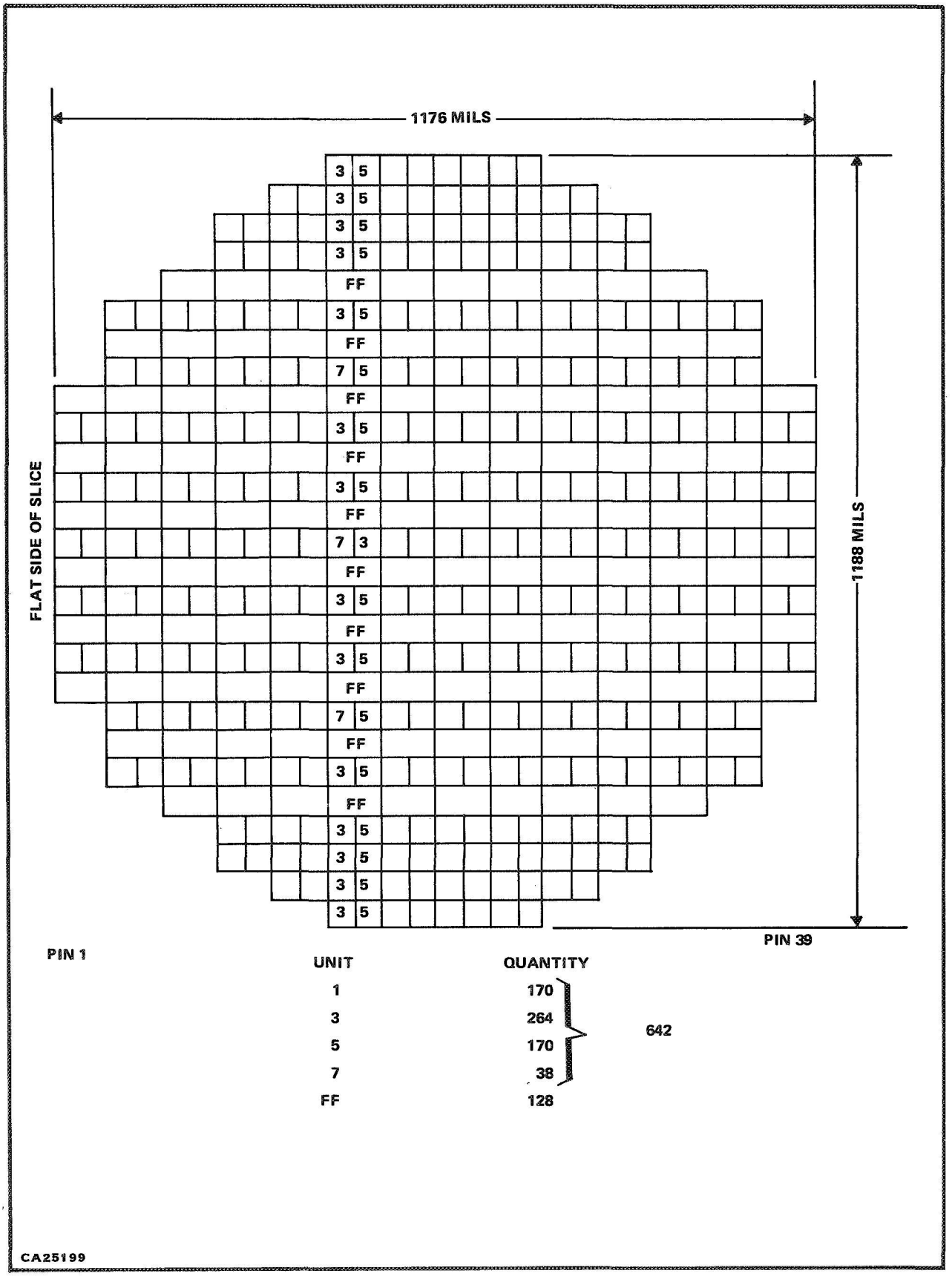


Figure 13. Cross-Sectional View of Slice Processing through First Metallization



UNIT	QUANTITY	
1	170	642
3	264	
5	170	
7	38	
FF	128	

Figure 14. L-Slice Layout (Columns are repeated)

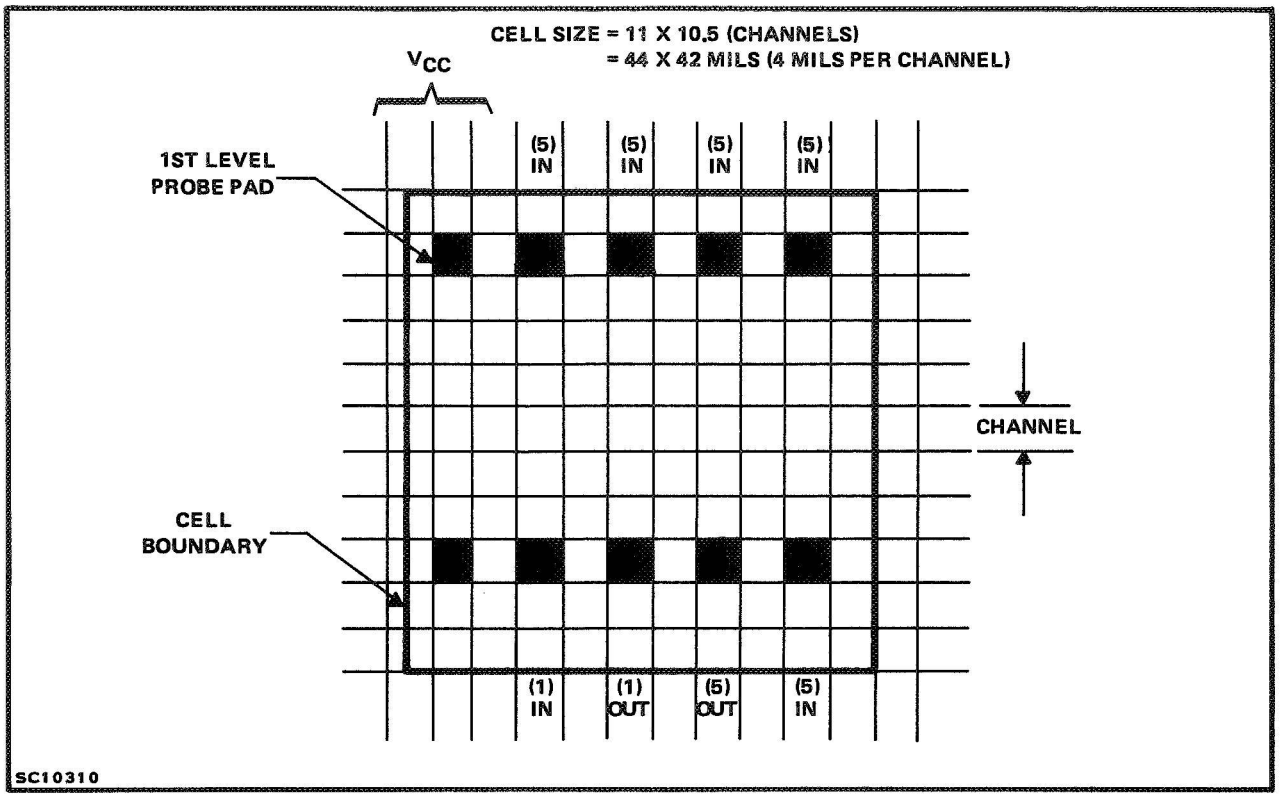


Figure 15. Unit Cell Structure for Combination Five-Input and One-Input Gate Cell

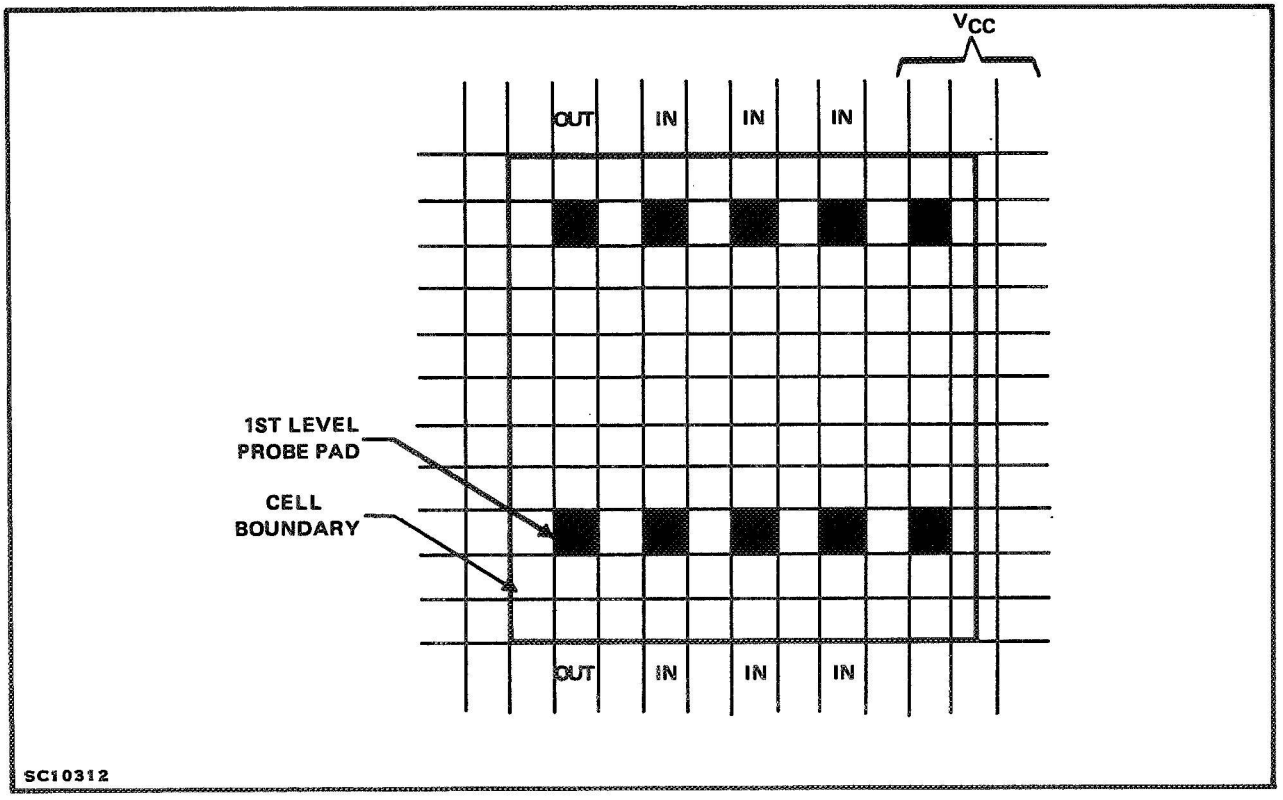


Figure 16. Unit Cell Structure for Dual Three-Input Gate Cell

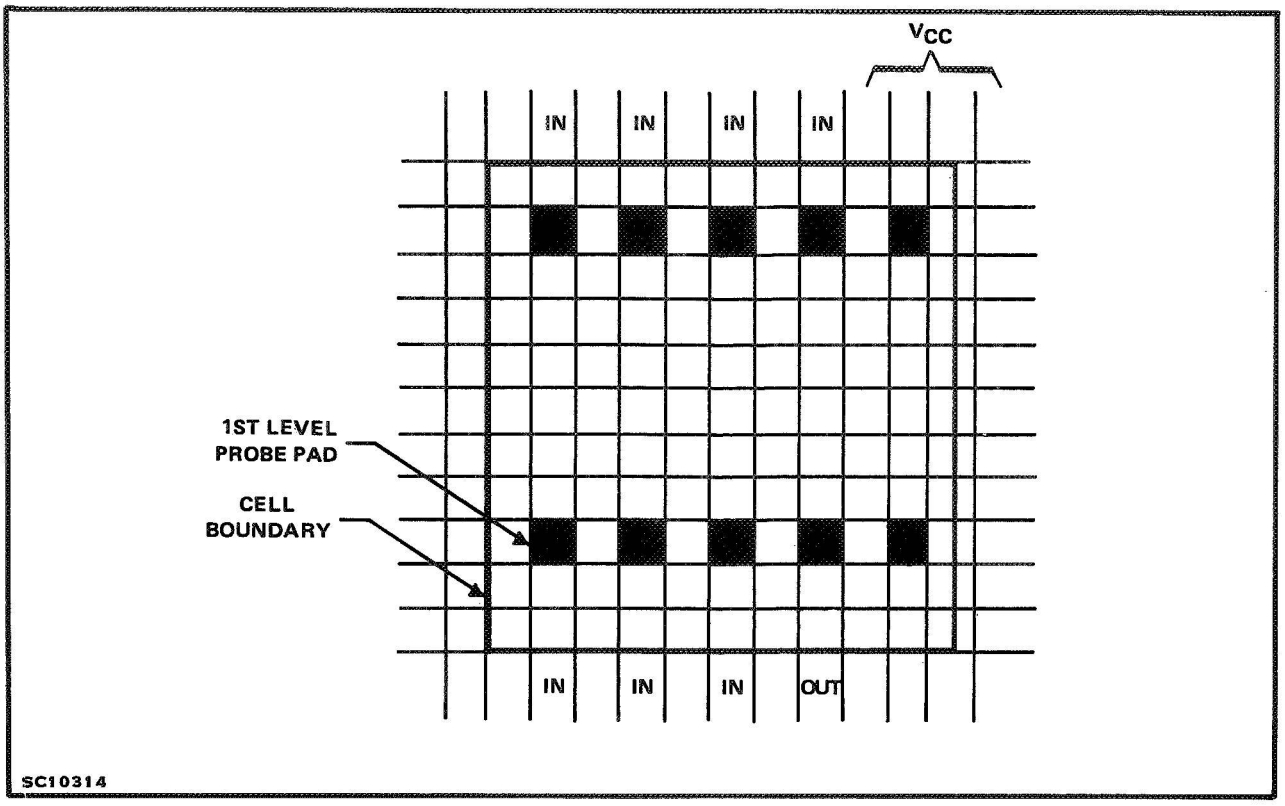


Figure 17. Unit Cell Structure for Seven-Input Cell

The design of a logic configuration of sufficient complexity to indicate LSI characteristics, but still facilitate monitoring of characteristics during life test, was an obstacle to overcome before submission of wafers for application of the multilevel metallization.

The logic configuration of Figure 19 was developed for several reasons:

- Characterization of given slice cell switching characteristics (gate delays, flip-flop switching times) could be implemented to determine cell parameter distributions. By routing gates to serve as inverters, the performance before and after application of multilevel metal could be determined.
- The relatively simple logic configuration facilitates completed array testing at temperature extremes.
- The total complexity of approximately 316 gate equivalents is characteristic of logic complexity currently considered to be LSI.
- The use of odd-multiple inverter strings has allowed generation of all signals necessary for true operating-life tests to be accomplished within the array. External V_{CC} and ground connections, combined with simple pin-to-pin connections, will generate operational signal conditions. This has overcome a common drawback

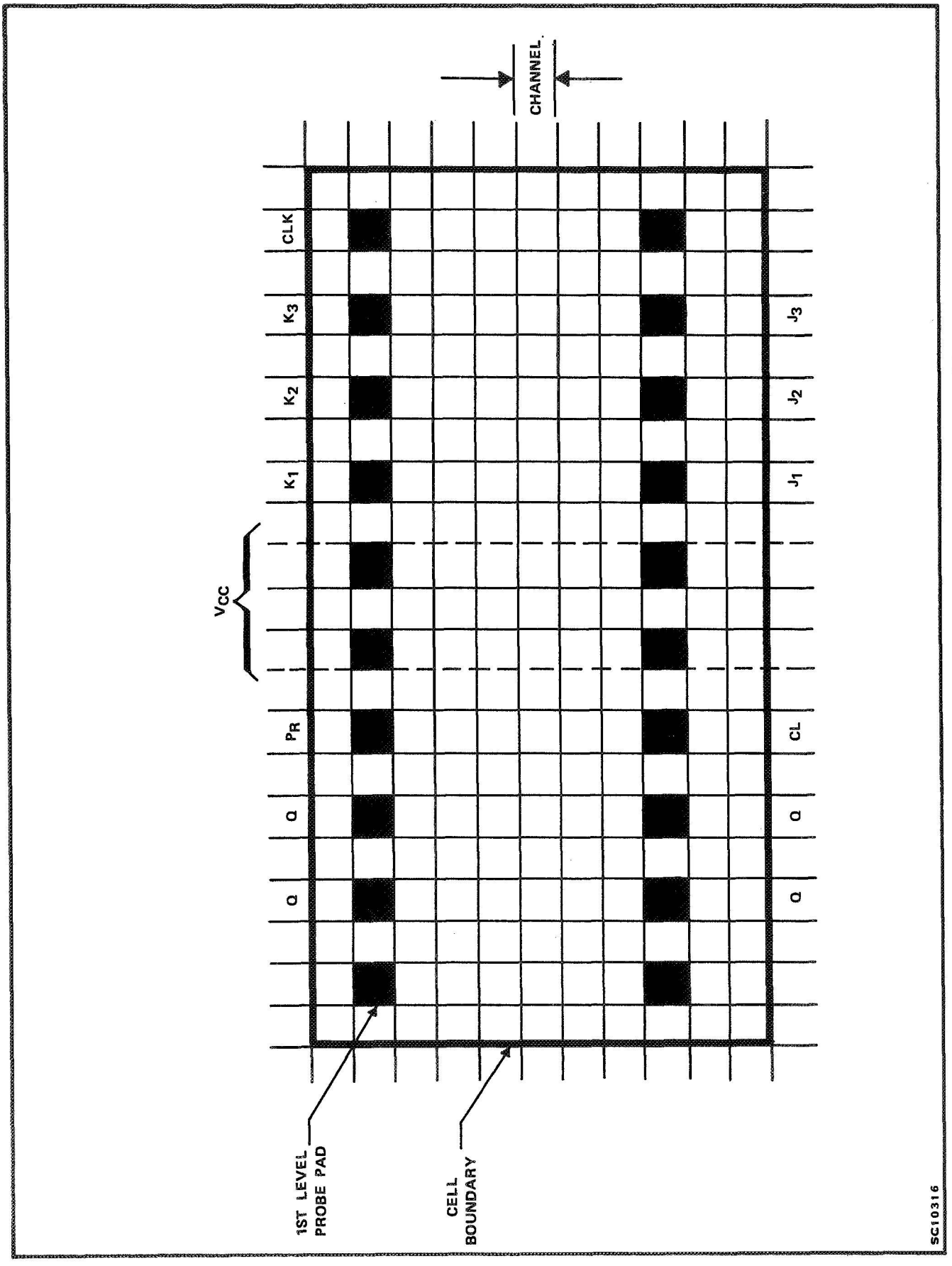


Figure 18. Unit Cell Structure and Pad Locations for J-K Flip-Flop Cell

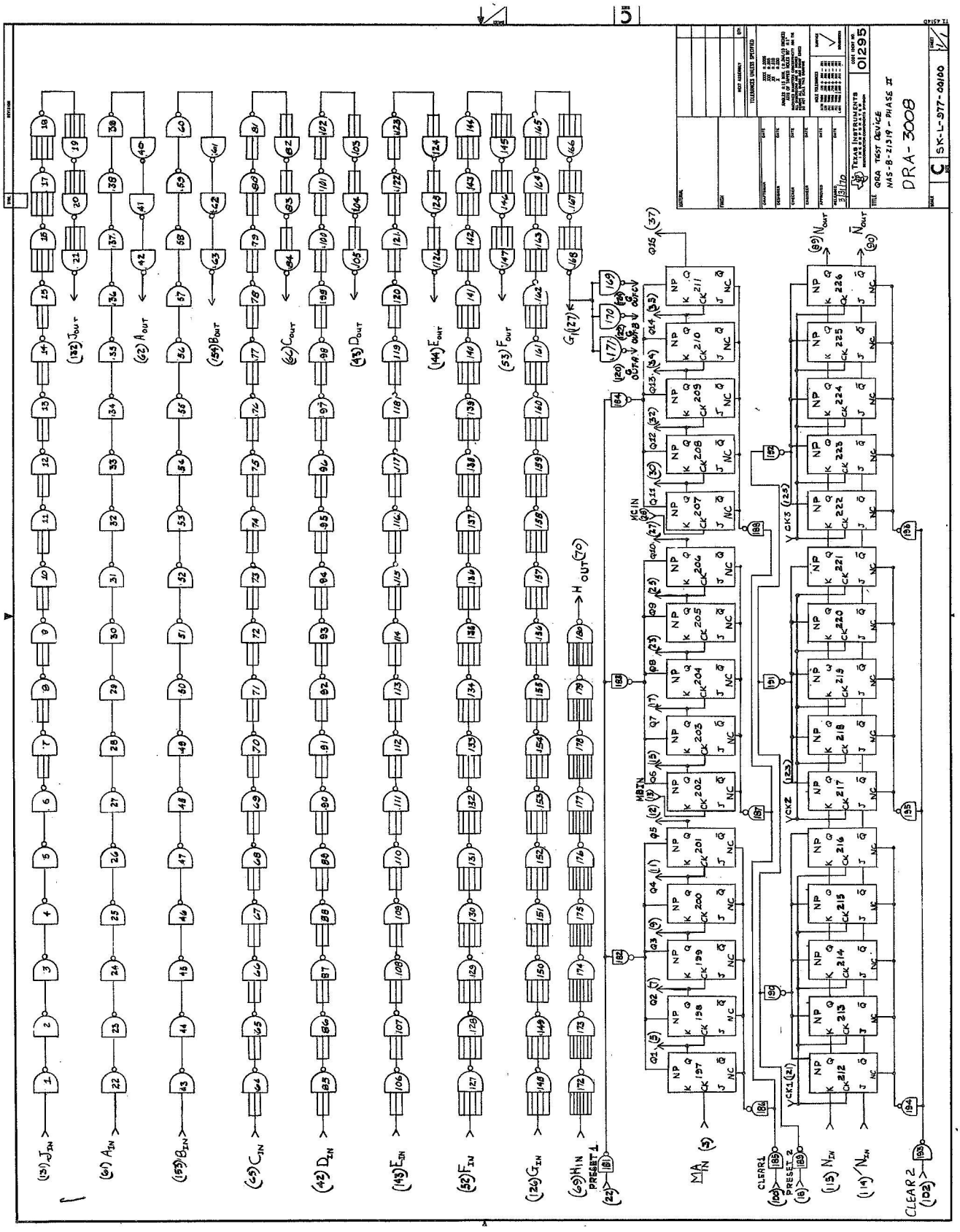


Figure 19. Logic Configuration for LSI Test Device

concerning LSI life testing; that is, the life test must degenerate to a static bias test, not truly indicative of circuit-deployment conditions, because the complexity of necessary exercising circuitry is overwhelming.

In addition to the logic pattern of Figure 19, there was a multilevel test cell used to monitor multilevel integrity as a function of time included in the test arrays. This test cell, shown in Figure 20, was wire bonded to the LSI package leads, and the parameter measurements indicated below were monitored to study multilevel integrity in a life-test environment.

Test Pattern I – Interpad resistance measurements could be used to indicate:

- Metal delamination
- Contaminated metallization at via contacts

Test Pattern II – Resistance measurements on each level, as well as interlevel leakage, indicate:

- Changes in intralevel current leakage resulting from metal corrosion or annealing effects of high-temperature testing
- Alterations of insulating oxide characteristics (i.e., drift of contaminants) as a function of time and high temperatures
- Interlevel shorts that could be generated at crossover points.

Test Pattern III – This is a series of vias and second- and third-level metal patterns that will yield feedthrough characteristics from second- to third-level metal. Resistance measurements before and concurrent with testing will monitor multilevel and via integrity. To evaluate the molybdenum-gold-molybdenum multilevel integrity under current stresses, each series feedthrough pattern was connected to V_{CC} voltage through appropriate resistors to yield current densities comparable to operating conditions, as well as densities that exceed design conditions.

2. Probe Testing (Manual and Automatic)

In TI's bipolar LSI manufacturing, an automatic multiprobe test is performed immediately after the etching of first-level metal to form the cells (see Section III – B-1) which currently are similar to TTL SSI products. For example, the "L" slice, used in the manufacture of the DRA-3008 test devices, is composed as follows:

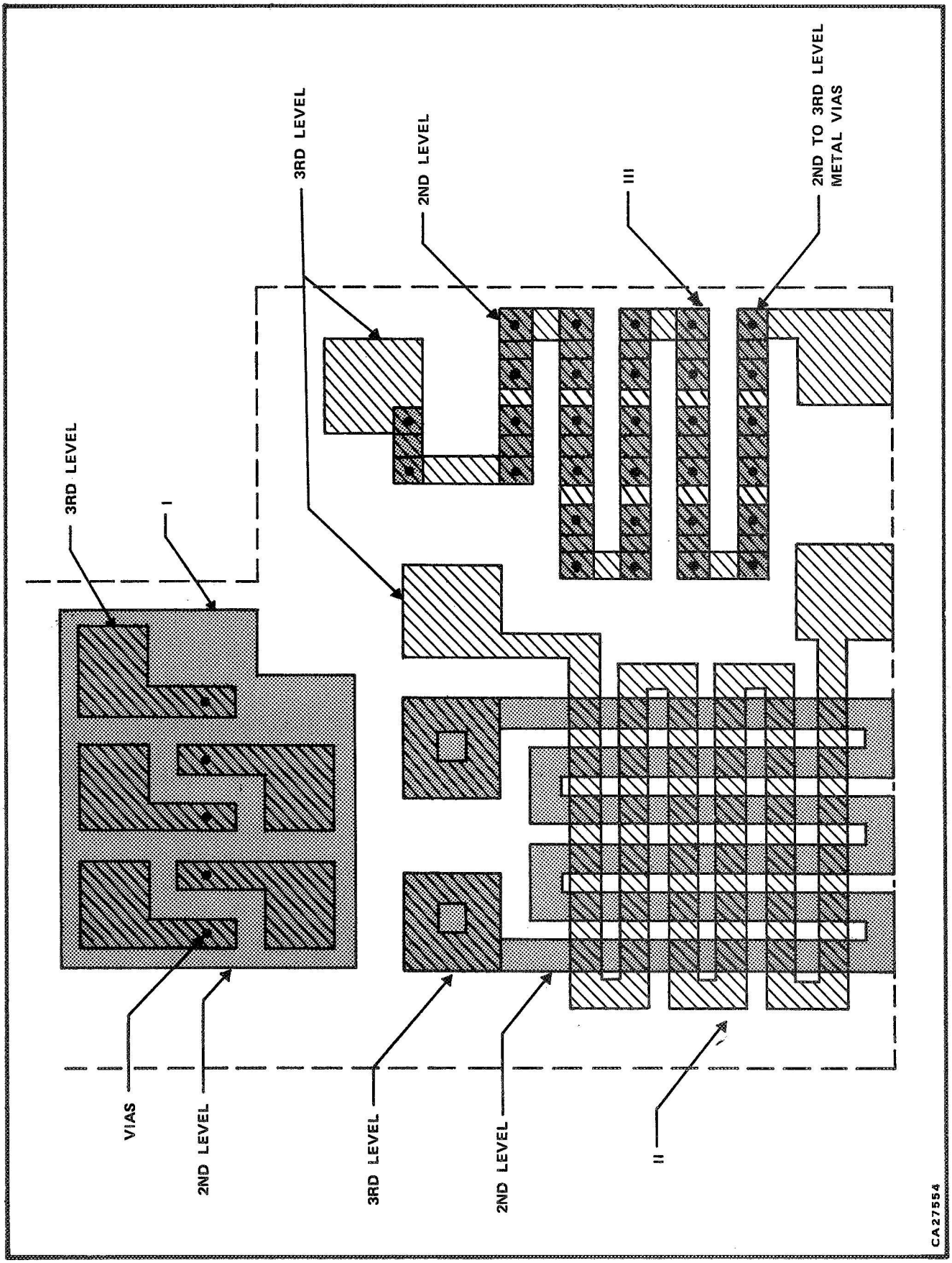


Figure 20. LSI Test Pattern (2nd- and 3rd-level Metals and Vias)

Circuit Type	Total on Slice
J-K Flip-Flop	128
1-Input Gate	170
3-Input Gate	264
5-Input Gate	170
7-Input Gate	38

The cells are then probed, using an automated multiprobe test head interfaced with a computer to store the location of good and faulty cells for reference. The criteria used in probing the slices at this stage closely resemble what would normally be a final or probe test for a TTL product.

Typical tests, performed at probe for series 5400 devices to indicate performance of the finished product over their intended temperature range, include those shown in Table VI.

The probe tests shown above are performed on the cells of the LSI slice; statistical data generated for TTL devices show that using this type of test at the cell level provides a high level of confidence that the cells will perform to TTL standards over the full −55 to +125°C temperature range.

Subsequent to the automatic probe testing (performed at the slice level to identify cells for routing into the finished array), a manual probe test was performed on the slices to be routed into DRA-3008 arrays.

This manual probe test was used to identify the ac transfer characteristics (propagation delays) of the gates to further ascertain the integrity of the cells that would constitute the array.

The probe test parameter data and post-routing data concerning gate delays are shown in the following tabulation for comparison.

Gate Type	Average Probe Delay (Mean of T_{pd0}, T_{pd1})	Average Delay After Route
1-Input NAND	8.052	8.05
3	8,344	8.34
5	9.183	9.17
7	11.177	11.26
FF	11.833 (clk to output)	Not available

Note: All data taken at 25°C.

The data show the similarity of delay characteristics before and after multilevel metallization layers are applied to the basic wafer.

The information on the delay characteristics of flip-flops after routing was not available in the same form as before probe because, after routing, only maximum frequency of operation was monitored.

3. Life-Test Results

The 10 DRA-3008 logic devices (see Figure 19) with three levels of metal interconnects were characterized as above for cell delays and put on life test for 1000 hours.

Figure 21 presents mean gated-delay characteristics measured at probe and after wafer fabrication, as well as propagation delay changes with respect to time.

As shown, the results indicate quite close correlation between probe and initial tests after cell interconnection. The only gate type that shows significant discrepancy is the high value of delay for the 7-input NAND gates. This high value was to be expected because the manual probe head used had only four available probe points. This meant that, for a 7-input NAND gate, only V_{cc}, ground, 1 input, and the output could be contacted.

The capacitance associated with the unterminated inputs of the 7 gates contributed to the slower operating speeds. The 7 gates, as interconnected on the slice, had all inputs tied together, increasing loading, but lowering "floating input" capacitances and decreasing gate delays.

Examination of gate characteristics on a slice to determine integrity of each cell showed typical cell-delay variance as follows:

Parameter	$T_{pd(0)}$ (propagation delay time to logic-0 level)
Mean	8.547 nsec
Standard Deviation	0.735 nsec

As evident from this typical example, the delay characteristics of functional cells (determined at automatic probe) are quite consistent. This consistency within a slice is to be expected because the delay times are primarily a function of the device geometrics. For a given diffusion operation, the cell (transistor) geometries (including diffusion depths, doping levels) will be uniform.

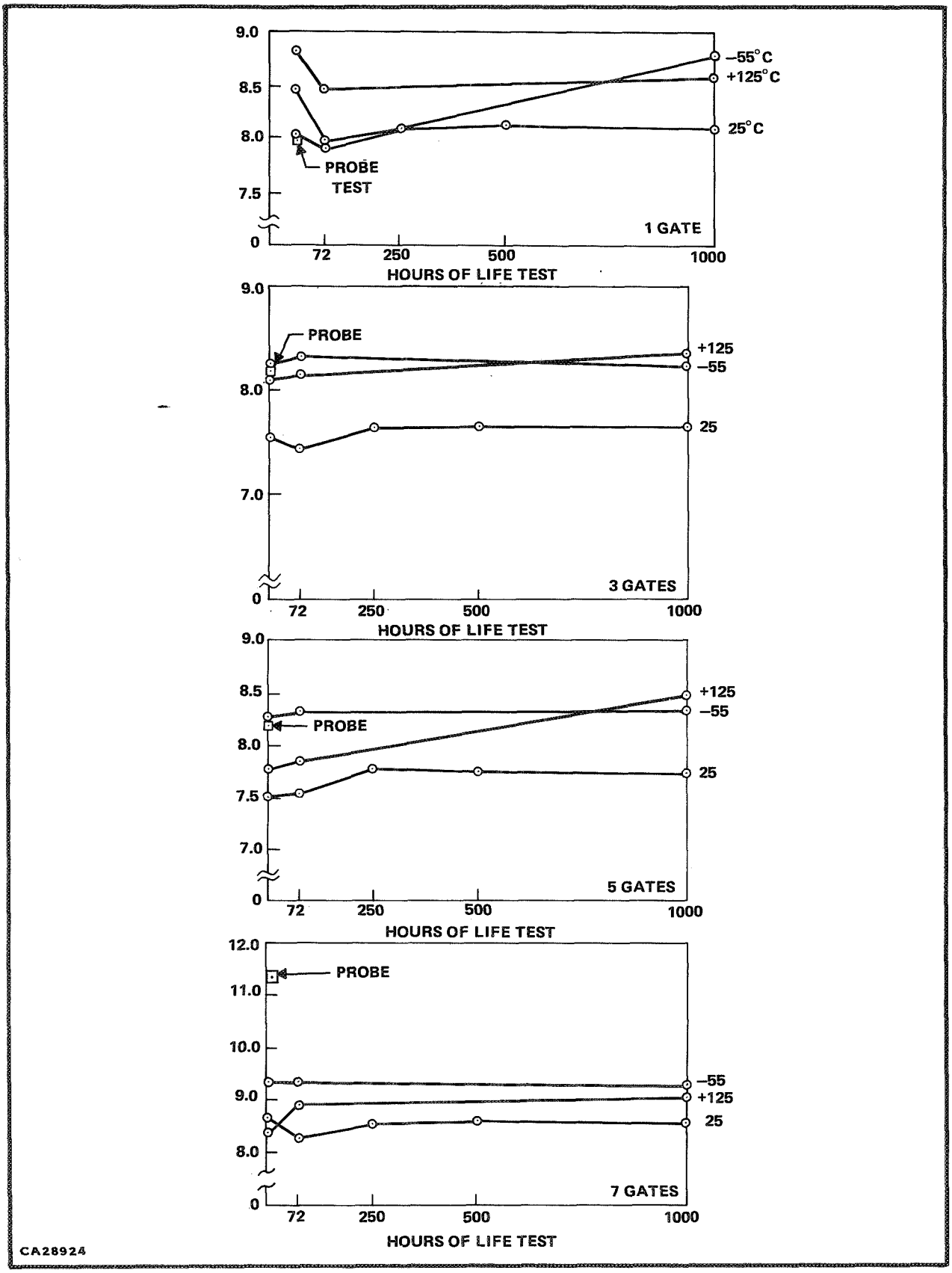


Figure 21. Mean Gate-Delay Characteristics

Analysis of characteristics at probe and after cell interconnect has shown that the dc parametric tests performed at the cell level (keeping in mind transfer-characteristics dependence on device geometries) are adequate to ensure finished array performance over the anticipated temperature range. Further definition of the tests that should be performed at the cell level is given in Section IV of this report.

Further investigation of the curves in Figure 21 shows that the propagation characteristics of completed slices remained relatively constant over the 1000-hour life-test period, indicating (at least for these bipolar units) that propagation delay characteristics are not particularly valuable indicators of array integrity with respect to time, except for determining gross-slice diffusion anomalies that are more readily obtainable (as well as economically necessary) at diffusion-evaluation probing.

The variability of the curves at the 0- and 72-hour readings can be partially attributed, not to the arrays themselves, but, to difficulties experienced in the socket of the fixture used to measure frequency response. The socket used to feed signals through the door of the environmental chamber was found to be changing characteristics during the temperature cycling for high- and low-temperature testing. After the initial readings (0, 72 hours on five units), the socket was eliminated from the test fixture. The repeatability of $I_{in(1)}$ and $V_{out(0)}$ readings was improved, and was indicative of improved repeatability in the text fixture.

Other parameters monitored during the period of the life test included $I_{in(0)}$, I_{os}, $I_{in(1)}$, $V_{out(0)}$ and test-pattern resistances. Figure 22 shows typical plots of these parameters with respect to time on life test. The plots neglect variances of parameters with respect to temperature because the values are directly correlatable to values seen at 25°C. For example, if an input current $I_{in(1)}$ is unusually large at 25°C, it remains significantly greater than average at −55 and +125°C. Analysis of anomalous data for 25°C, in light of results at other temperatures, can yield information about the nature of the anomaly within the device.

Figure 22 indicates that the parameters measured were typically consistent with time. The most variable parameter, to be expected because measurements were in the μA range, was $I_{in(1)}$, one-level input current. This current corresponds to a transistor operating in the inverse β mode (input biased for normal conduction; only emitter and collector regions are interchanged) with typical inverse β of less than 0.02, which yields input currents of less than 20 μA. This parameter is most sensitive to ionic contamination and slight changes in input-transistor parameters.

All arrays tested showed good stability of $I_{in(1)}$ and, therefore, good overall stability of cell operation. No contamination that would degrade cell performance appeared to be introduced by the application of multilevel interconnects.

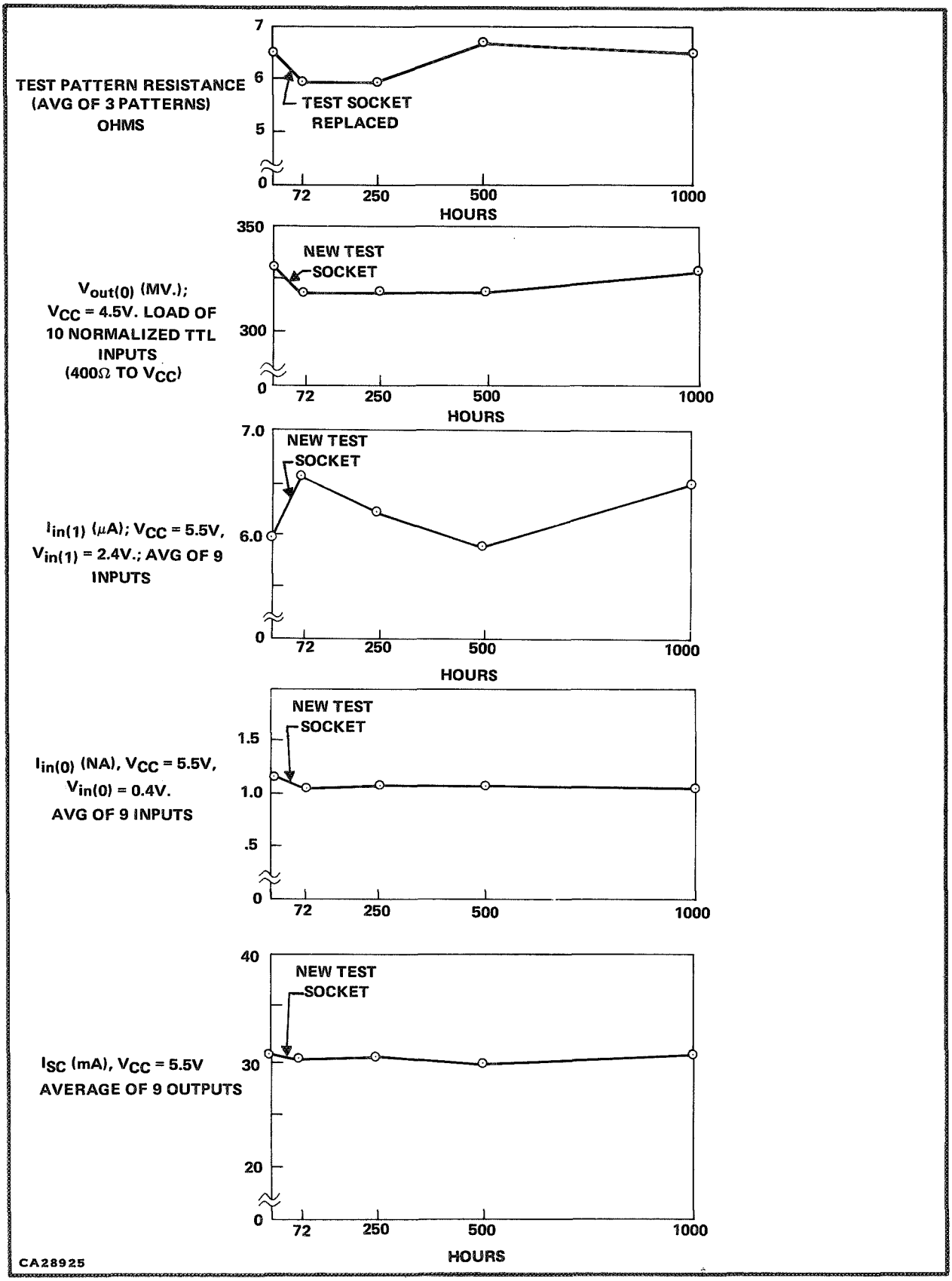


Figure 22. Typical Array Parameter Changes as Function of Time on Life Test

Anomalous parameter characteristics measured during life tests are discussed in Section II-D-3. A summary of life-test results is given in Table IV.

Several anomalous readings were detected during the parametric testing of the DRA-3008 life-test devices; each of these is discussed by device serial number.

- DRA-3008, all units – Typical TTL device characteristics specify that, with no more than 10 external loads on the output, $V_{out(0)}$ will remain less than 0.40 volt. For the case of bipolar LSI, where slice-interconnect patterns can be quite long to fulfill the customer's pin-out diagram, general design limitations restrict external loads to a limit of five (for "0" output, this would be sinking a maximum of 8.0 mA). In addition, this external drive limit will, in some cases, need to be reduced to comprehend high internal fan-out (where perhaps 10 loads are used internally).

  The DRA-3008 life-test units were tested for $V_{out(0)}$ levels with a nominal external load of 10 applied (400 Ω to V_{cc}). The usual output that exhibited greater than the generally accepted "0" level (400 mV) was output pin No. 127. This was undoubtedly due to the three gate inputs that this output was required to drive internally.

  Had the arrays been tested to the recommended operating conditions, no unit would have shown $V_{out(0)}$ levels higher than the specified 400 mV.

- DRA-3008, SN 2618 – Device 2618 showed input pin No. 69, $I_{in(1)}$ (V_{in} = 2.4 V, V_{cc} = 5.5 V) equal to 44.0 μA (4 μA greater than the maximum accepted reading) at 0 hours and 125°C T_A; $I_{in(1)}$ was equal to 30 μA for 25°C T_A for an initial reading. This slightly higher-than-normal value for $I_{in(1)}$ at 125°C would probably remain within acceptable limits if the high-temperature test were performed at ≈ 125°C T_C as would be typical for TTL operating at 125°C T_A. The extra temperature rise of the LSI slice, due to the power dissipation (≈3.7 watts), is reflected in the case temperature of ≈ 143°C. Since the power dissipation is large, the typical LSI specification is currently based on an upper limit of 100°C ambient. This can be exceeded with adequate heat-sinking arrangements.

  Monitoring of this input throughout the life of the test of 1000 hours showed no change in the parameter with time. After 1000 hours, $I_{in(1)}$ remained at 44.0 μA. Again, operation of the LSI device under recommended conditions (T_A = 100°C) would yield an $I_{in(1)}$ parameter within accepted standards.

Table IV. Life Test Result Summary

Array Serial No.	Total Hrs. on Life Test[1] [2]	Comments
1606	1000	Array OK
1910	1000	Array OK
2604	1000	Intermittent undiagnosed functional failure at 1000-Hr.EEP
2618	1000	Array OK
2607	1000	Array OK
2005	72	Functional failure;Multilevel short at a 2nd to 3rd level
2302	1000	Array OK
2313	1000	Functional failure believed due to multilevel short; unable to verify in failure analysis.
2307	1000	Array OK
1216	1000	Array OK

[1] Life test was performed with arrays operating at 125°C ambient (T_{case}=140°C), V_{cc}=5.0 volts.

[2] Life-test failures are discussed further in Section II-D-3.

- DRA-3008, SN 2005 – This device was removed from life test at the 72-hour parameter reading when it was found to have a functional failure. The input of a 5-input NAND gate was ≈ 0.2 volt; the output was only 0.44 volt.

  The unit was submitted to failure analysis; the following five photographs show stages in the analysis.

  Figure 23 shows (through Sylgard, with probe marks as dark spots on the metal line) the suspect area with the via (later determined to be defective) marked.

  Figure 24 shows the mechanical scribing to isolate the defective area (this destroyed the short to ground). Since scribing at this point destroyed the short, the defect was believed to be adjacent to the scratch in the vicinity of the via.

  Figure 25 shows the suspect via after third metal was removed. The arrow points to the run-out geometry of the via that occurs due to the underlying step in first-level metal.

  Figures 26 and 27 are scanning-electron micrographs of the defective via detailing the suspected oxide fault (occurring over the first-metal step) that allowed the second metal to short to ground.

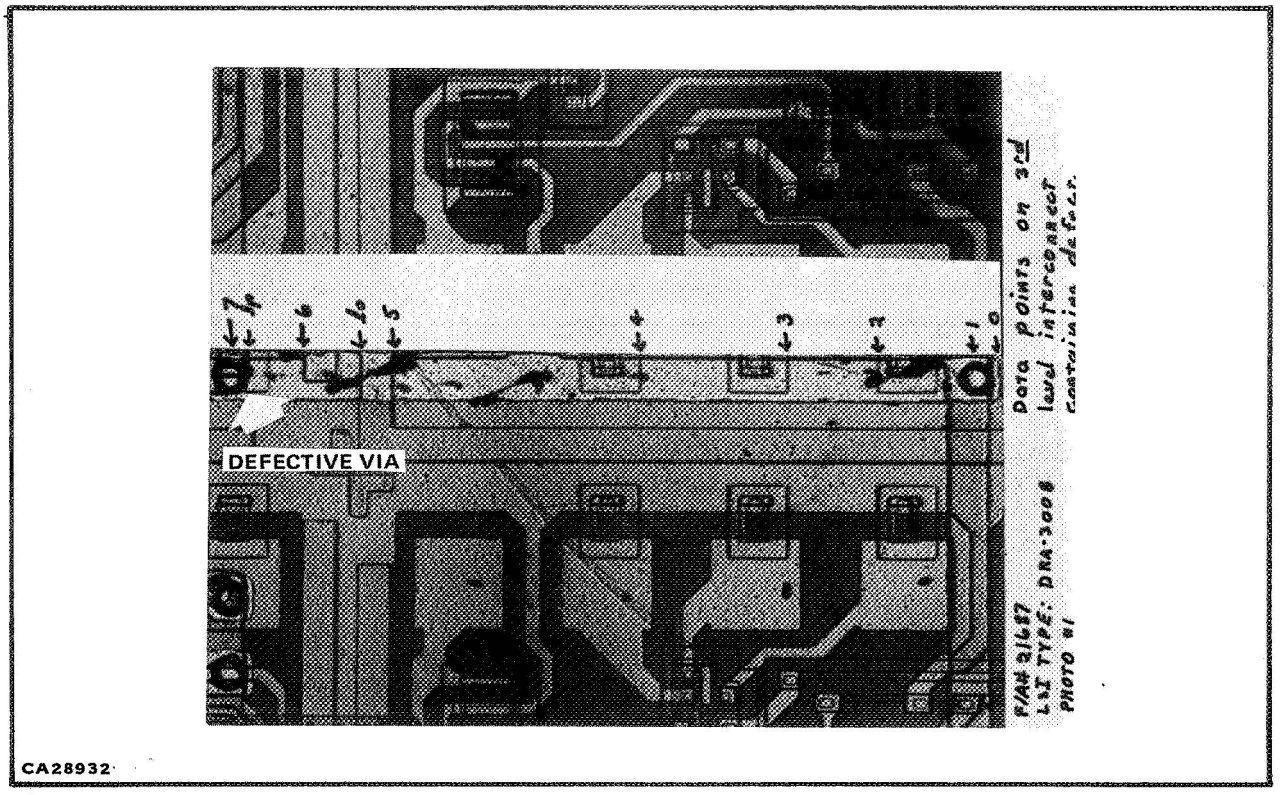


Figure 23. Area of Defect

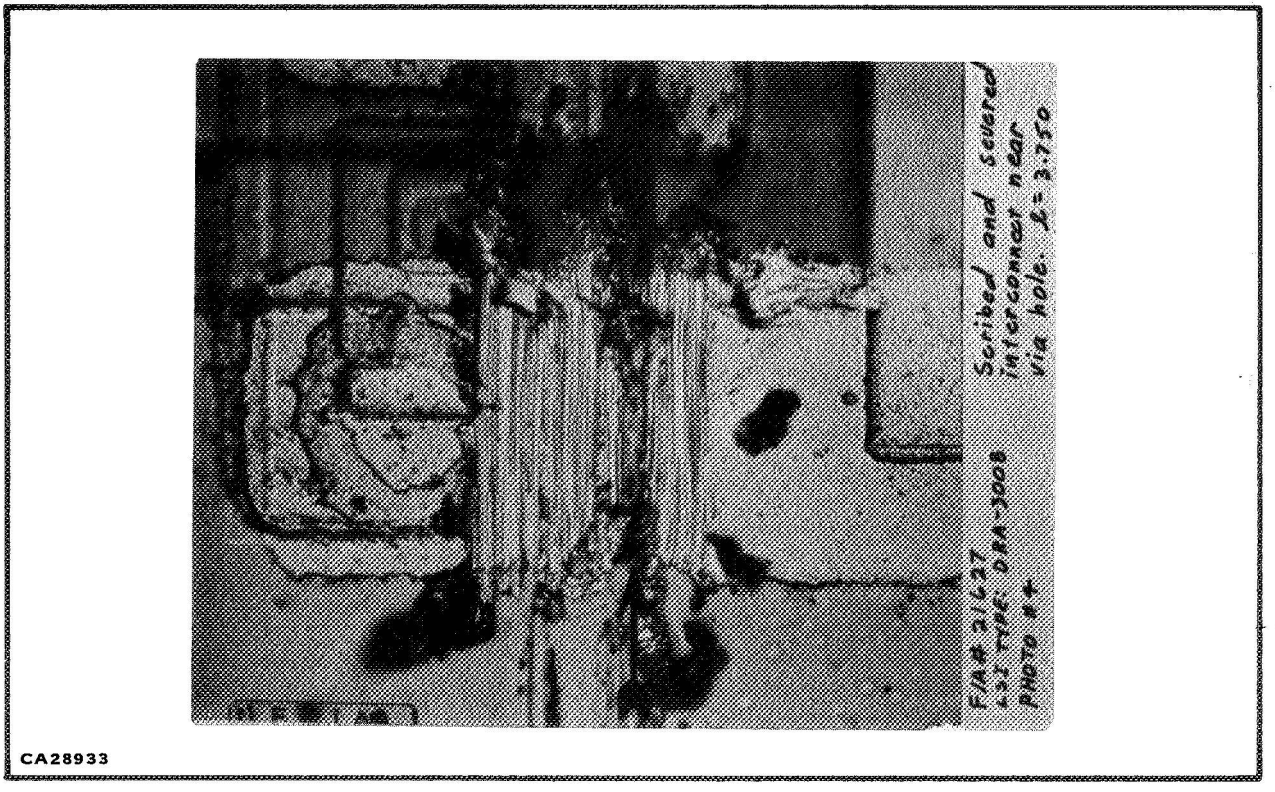


Figure 24. Defective Via (Mechanical scribe to isolate defect)

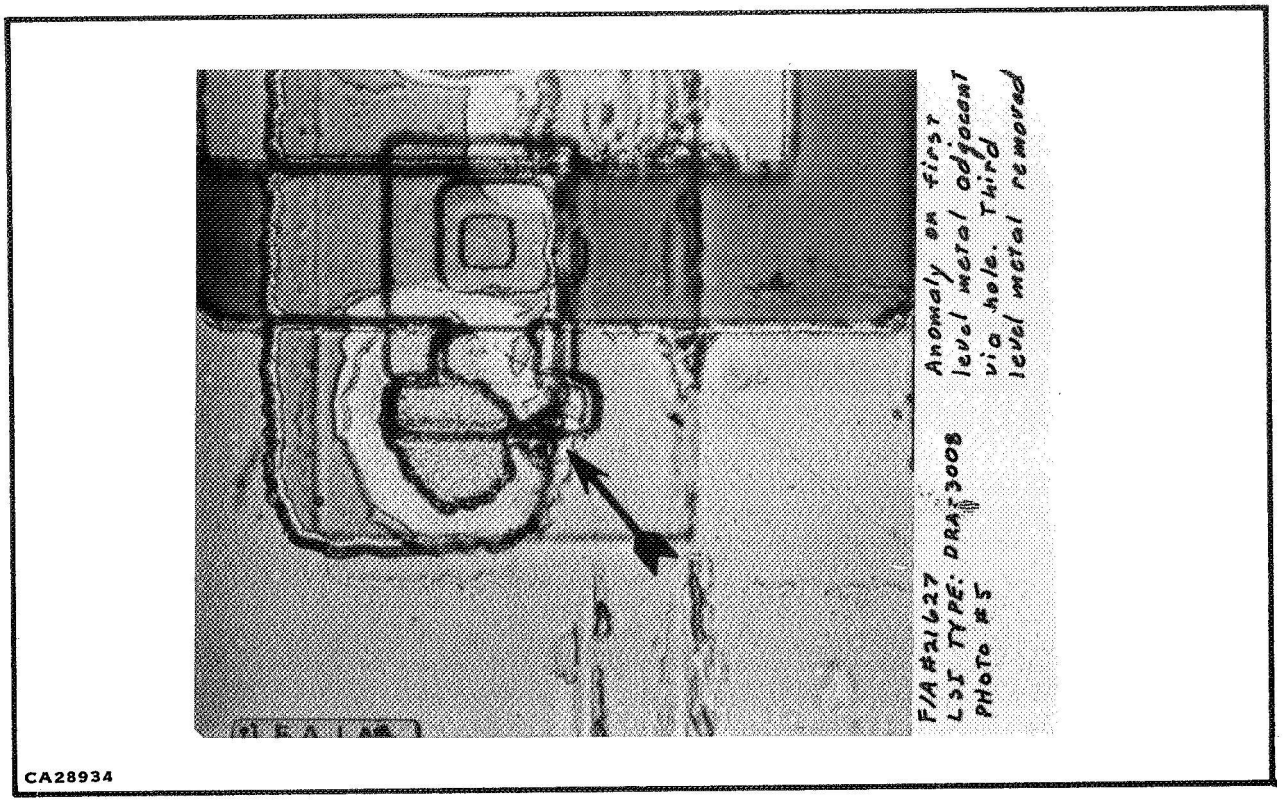


Figure 25. Defective Via (3rd metal removed)

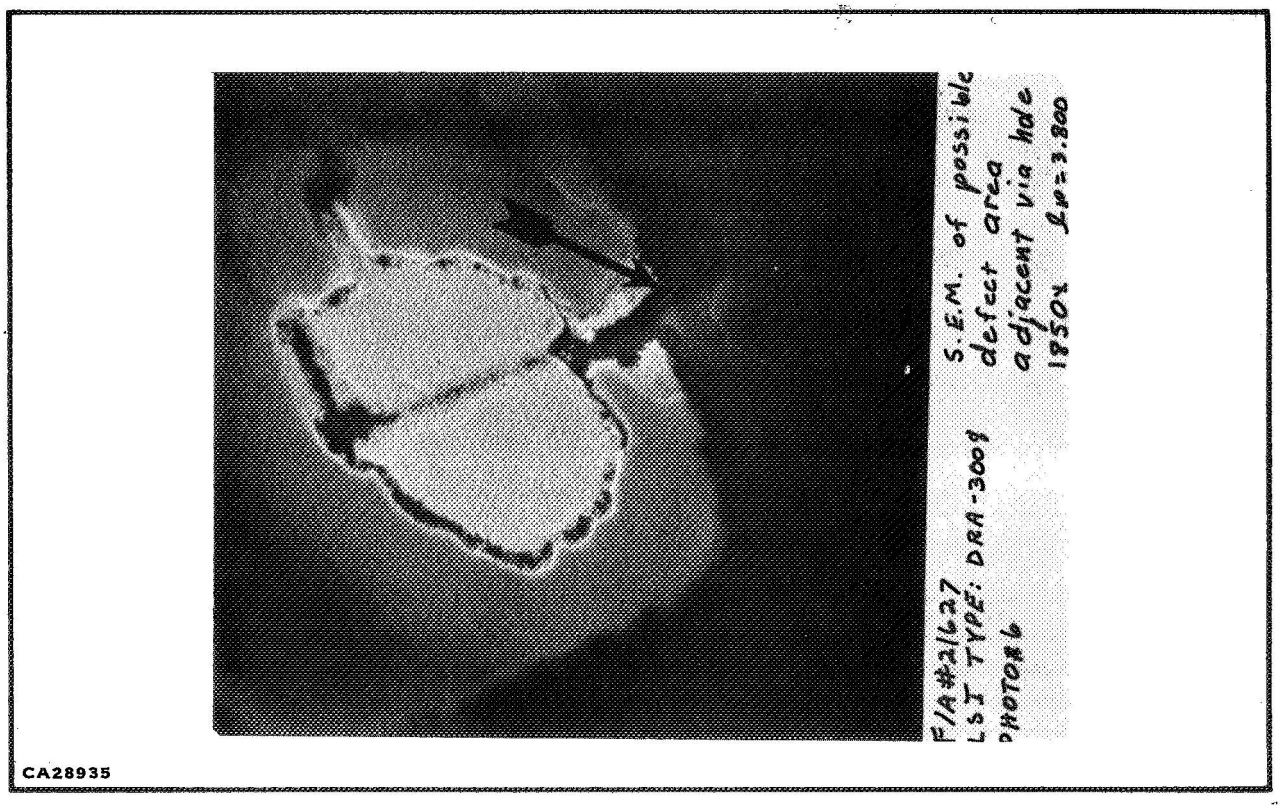


Figure 26. Scanning Electron Micrograph of Defective Via (1850X)

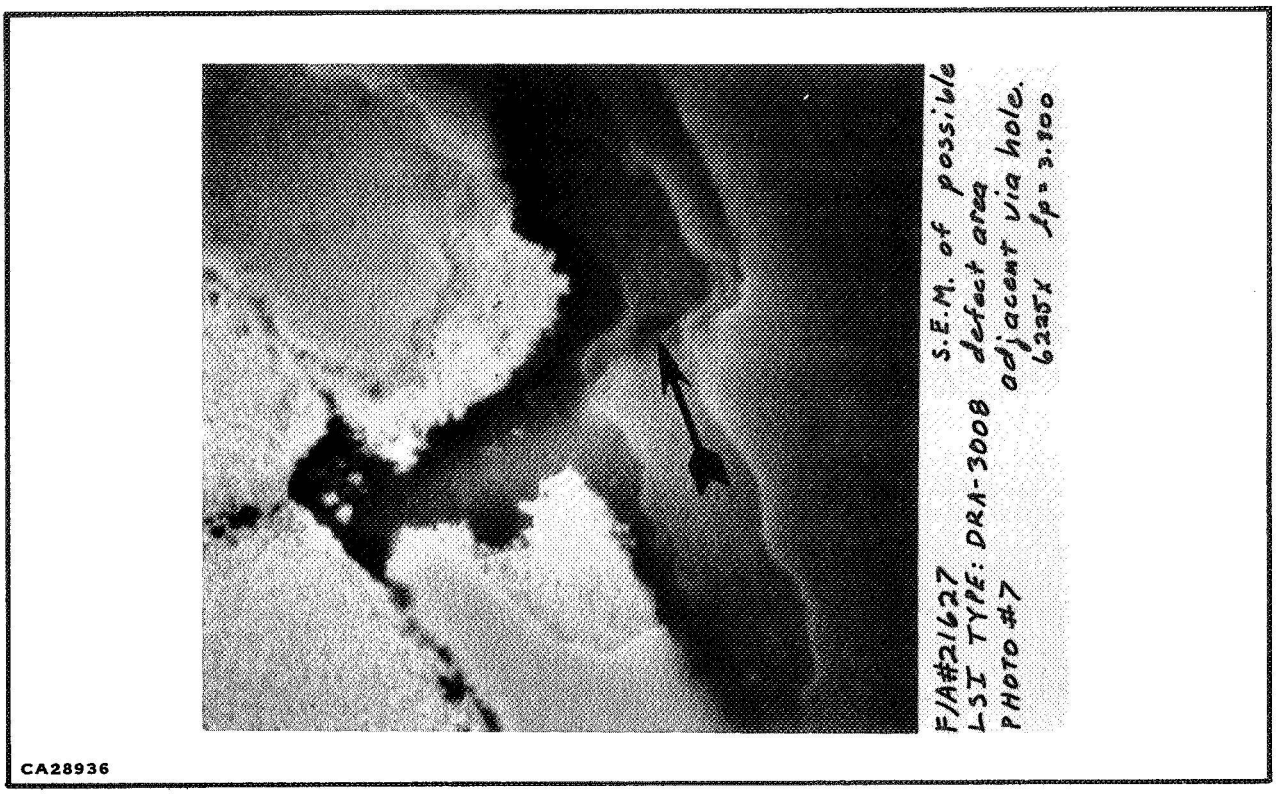


Figure 27. Scanning Electron Micrograph of Defective Via (6225X)

Further discussion of this particular failure mechanism and possible metal system changes to reduce the occurrence of M-L shorts is presented in Section III.

- DRA-3008, SN 2313 – This device was determined to be a functional failure at the 1000-hour test point. The unit was decapped, the defect was traced to a gate interconnect (utilizing the SATS tester), and the device was sent to the failure-analysis laboratory to determine the cause of failure. The failure-analysis laboratory was unable to verify the failure (using digital voltmeter analysis of the area in question) and returned the unit to Houston. Retests on the functional tester in Houston also were unable to detect a failure.

  The believed area of fault was visually examined and no visual anomaly, though capable of causing the failure, was detected. The fault is believed to have been multilevel short to ground; in some cases, this type of short is quite easy to clear. Measuring input/output breakdowns on the curve tracer (if sufficient current limiting is not observed) can sometimes open this type of short to ground, thereby eliminating the failure.

Several multilevel processing improvements are under development; they are discussed in Section III. Until a more reproducible multilevel system is established, several screening methods, visual and electrical, should be implemented to screen current-process LSI/DRA devices for high-reliability applications. Several possible methods are discussed in Section IV. The economic impact of these screens is not fully known at present, but, with a further enhanced M-L process, their effect on yield and, therefore, cost should be minimal.

SECTION III

DESIGN ANALYSIS OF CURRENT PRODUCT

A. METALLIZATIONS

An analysis of TI discretionary routed LSI metallization must include the following areas.

- First-level metal
- Second-level metal
- Third-level metal
- Feedthroughs in multilevel metal

Each of these is discussed in subsequent paragraphs; geometries and characteristics of the "L" slice (NAND gates and J-K master-slave flip-flops) are given. This could be extended to all other slice types by revising the first-level metal worst-case widths and, therefore, circuit currents because all deposition thicknesses remain constant.

1. First Metal

The maximum design current density for first-level metal on the "L" slice occurs at the output (A_{out}) of the 1-input gate. At this point, we have 0.6-mil metal width.

A current maximum occurs when A_{out} is driving 10 TTL loads, (array design practices limit outputs to 10 TTL normalized loads), which is a maximum of 16.0 mA.

At first metal, thicknesses of each successive layer for the "sandwich" structure are as follows:

Aluminum	500 Å
Molybdenum	2000 Å
Gold	9000 Å
Molybdenum	750 Å

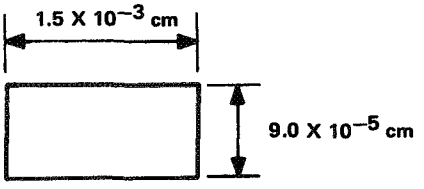
Comparing the resistivities of molybdenum to gold, it is seen that

$$\rho_{moly} \approx 5.7 \times 10^{-6}\ \Omega\text{-cm}$$

$$\rho_{gold} \approx 2.44 \times 10^{-6}\ \Omega\text{-cm}$$

which indicates that the majority of the current conducted will be carried by the gold metallization. Current-carrying capabilities will be analyzed assuming that only the gold metal is a current carrier.

The cross section of first metal is as shown below (gold only):



Therefore, we have a cross-sectional area of:

$$\text{Area} = (1.5 \times 10^{-3})(9.0 \times 10^{-5}) = 13.6 \times 10^{-8}\ \text{cm}^2$$

and a resultant current density (J) of:

$$J = \frac{16 \times 10^{-3}\ \text{A}}{13.6 \times 10^{-8}\ \text{cm}^2} = 1.17 \times 10^{5}\ \text{A/cm}^2$$

or

$$J = 117{,}200\ \text{A/cm}^2$$

2. Second Metal

Second-level metal lines are 3.0 mils wide and have 12,500 Å of gold. These second-level metal lines can, at most, carry 16.0 mA (the same as first-level metal signal pins) and, obviously, current densities here are not critical.

Also on the second-metal level are V_{CC} interconnection bus lines; these lines are 11.0 mils wide. An absolute maximum of 10 J-K flip-flops can be interconnected by a V_{CC} line. This represents a maximum current of 400.0 mA. This worst-case current would yield a current density of:

$$J = \frac{400 \times 10^{-3}\ A}{(11.0 \times 10^{-3}\ \text{in.})(2.54\ \text{cm/in.})(12{,}500\ \text{Å})(1 \times 10^{-8}\ \text{cm/Å})}$$

$$J = 114{,}531\ A/cm^2$$

3. Third Metal

Third-level metal is signal carrying, as is second metal, and, therefore, subject to the same current densities as signal lines on second metal.

4. Feedthroughs

Of final interest is the typical current density seen at feedthroughs between metallization layers.

The feedthrough configuration is as shown in Figure 28.

The smallest cross-sectional current-carrying area is at the base of the sloping metal from third to second level where the via diameter is 1.0 mil. Therefore, the circumference is:

$$C = 7.98 \times 10^{-3}\ \text{cm.}$$

The metal thickness of 12,500 Å of gold yields a cross-sectional current-carrying area of:

$$\text{Area} = 1.0 \times 10^{-6}\ cm^2$$

and current density:

$$J = \frac{16\ \text{mA}}{1.0 \times 10^{-8}\ cm^2}$$

$$J = 1{,}600{,}000\ A/cm^2$$

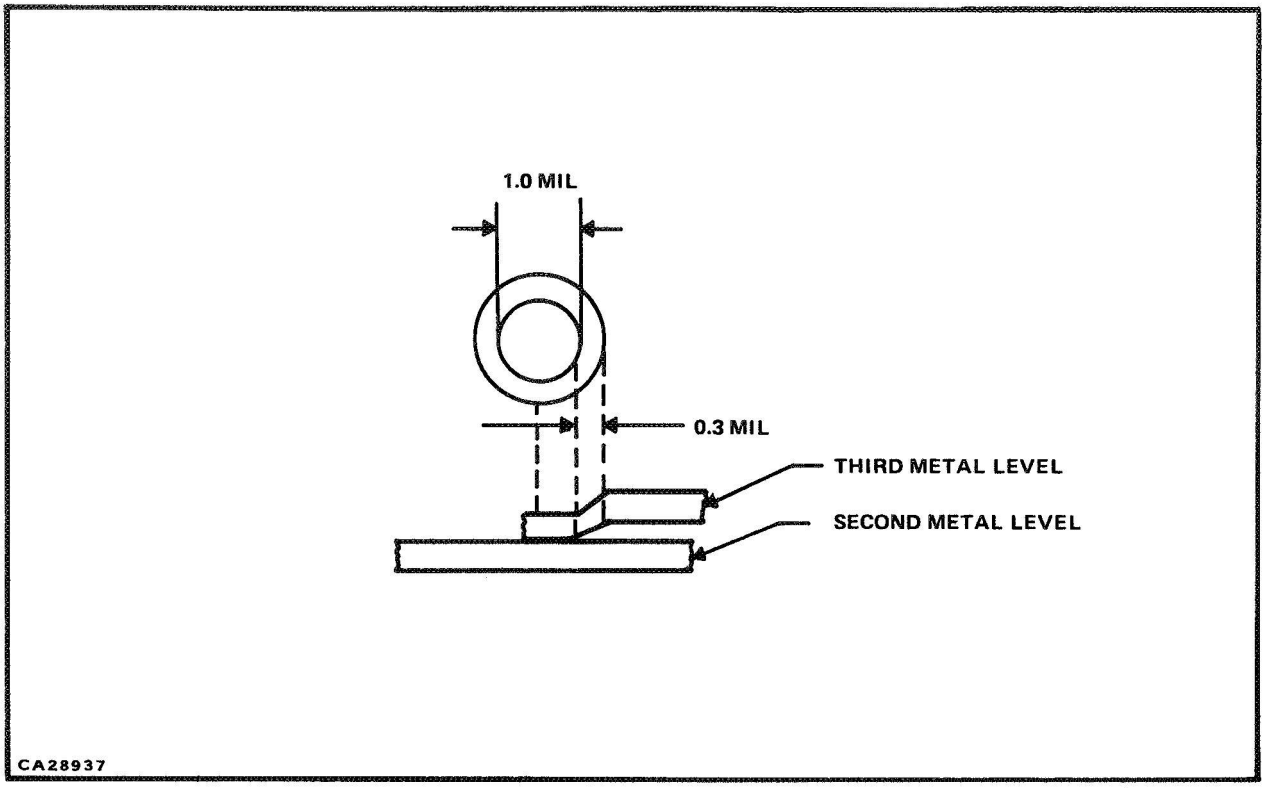


Figure 28. Feedthrough Cross Section

5. Summary

Tests performed on molybdenum-gold metallization systems have shown this metal system capable of carrying 2.5 X 10^6 A/cm^2 with no resultant metal migration problems.[1]

As can be seen for each of the above conditions, the design current densities are well within material limitations for a reliable metallization system.

Even anticipating metallization faults (voids, over-etch, masking faults, non-uniform deposition) and if the manufacturing operations have even limited control (that is, if the unit's metallization cross section is only 10% of design limits), the resultant current densities will still remain within accepted reliability standards.

[1] RADC, "Reliability of Thin-Film Multilayer Connections," Technical Report RADC-TR-69-344, RCA Laboratories (December 1969).

B. INSULATIONS

The TI multilevel insulator system has a cross section as shown in Figure 29.

The dielectric constant and dielectric strength of amorphous SiO_2 are as follows:[2]

Relative dielectric constant $\approx$ 3.8

Dielectric strength $\approx 5 \times 10^6$ V/cm

From a reliability viewpoint, the dielectric strength of the passivation layers is of particular interest. There will be a maximum voltage across the multilevel insulator of 5.5 volts; this is operation under maximum V_{CC} conditions.

Hence, we have an electric-field intensity, E, of

$$E = 5.5 \text{ V}/(22.0) \times 10^{-5} \text{ cm}$$

$$E = 2.5 \times 10^4 \text{ V/cm}$$

This value is well within the dielectric strength of the SiO_2 insulator.

The electric-field intensity shown above is for the nominal coverage of oxide over parallel metal levels. However, the worst-case distance between metal lines would occur at an oxide step, as showr in the micrograph of Figure 30.

For this closer spacing over an oxide step, we have a separation of approximately 1.57×10^{-4} cm and an electric-field intensity of

$$E = \frac{5.5}{1.57 \times 10^{-4}} = 3.5 \times 10^4 \text{ V/cm}$$

This value of E is still two orders of magnitude less than the critical value of 5×10^6 V/cm.

This cursory examination of design conditions for TI LSI has centered on the multilevel technology because the initial slice processing is essentially the well-proven TTL manufacturing process.

In summary, it has been shown that the LSI design for the multilevel interconnections is well within conservative engineering limits.

---

[2] T. R. Myers, Technical Monograph 69-2, IIT Research Institute, Chicago, Illinois (September 1969), p. 8.

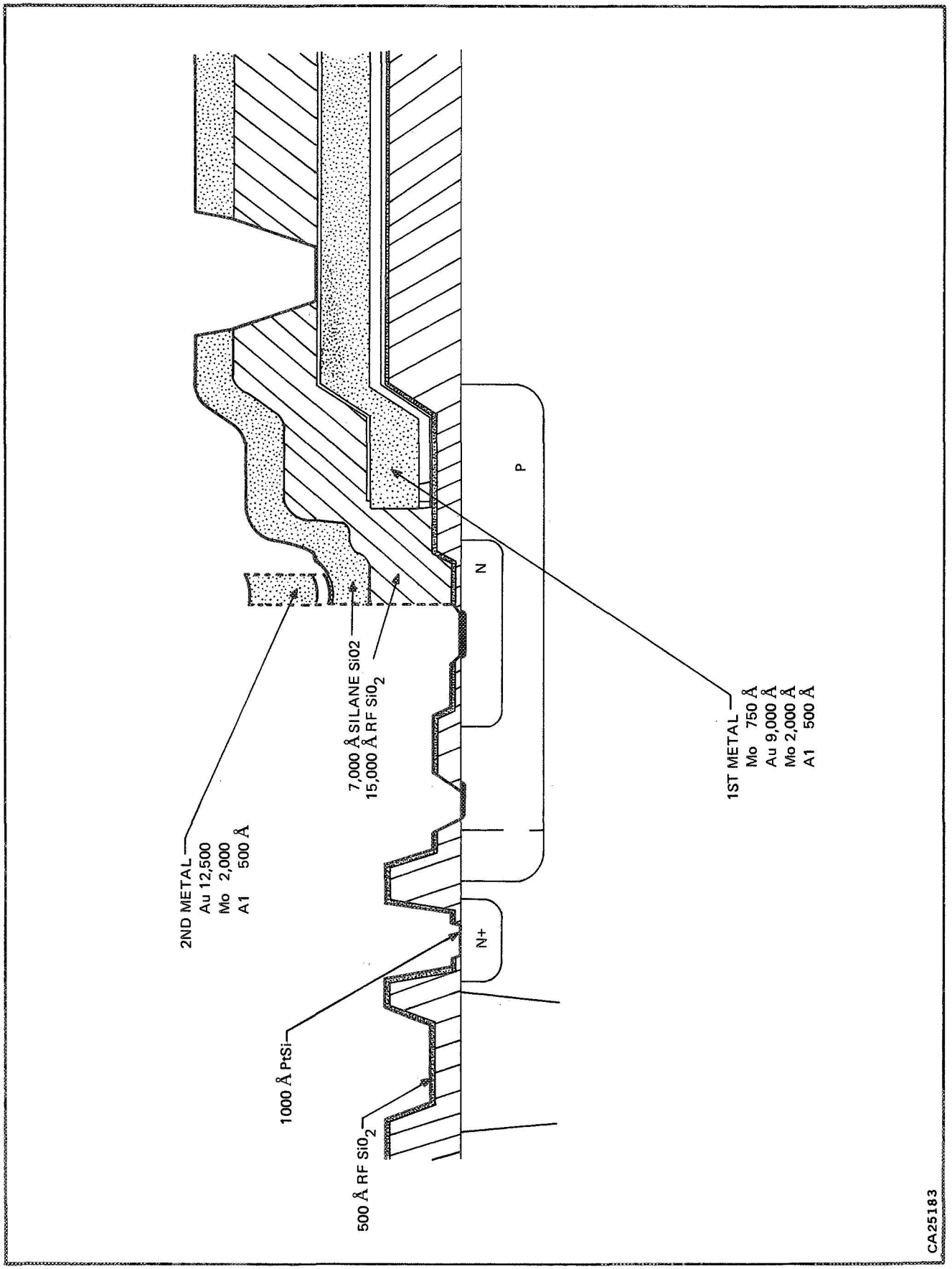


Figure 29. Multilevel Cross Section

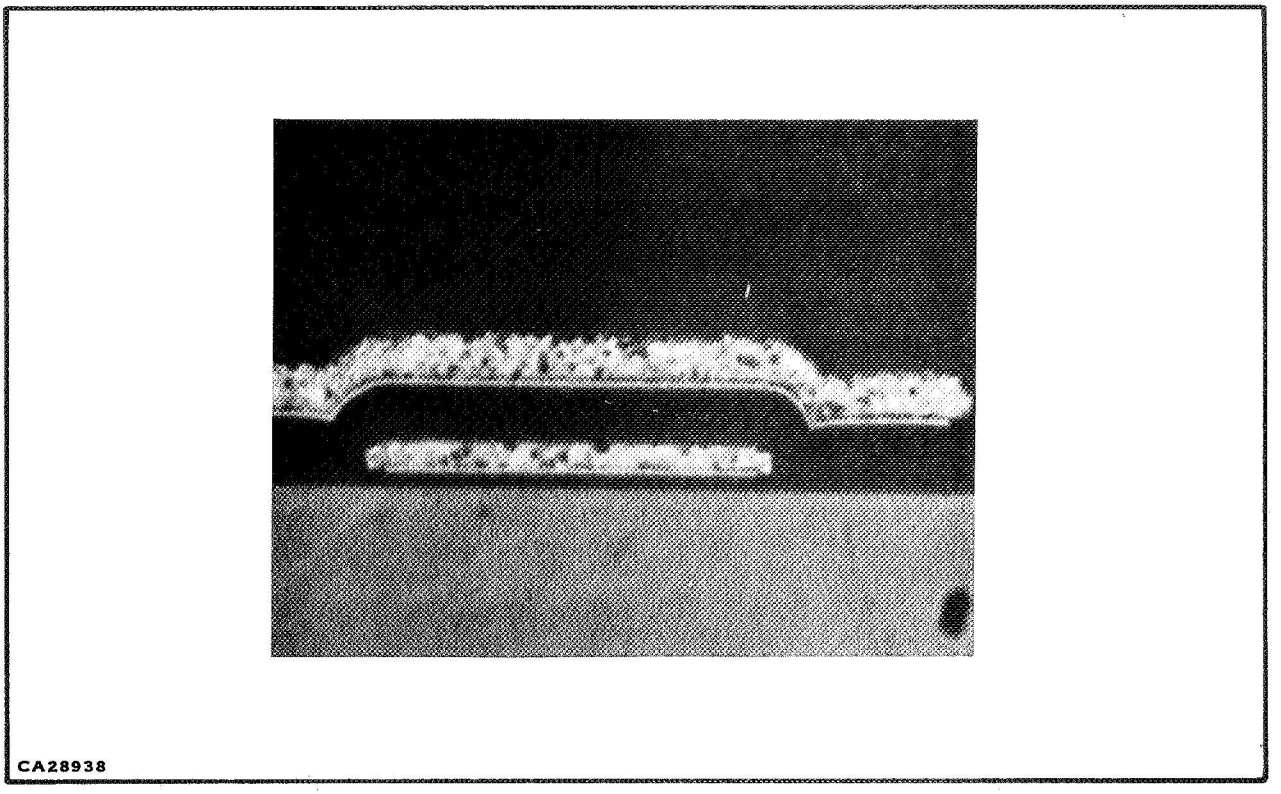


Figure 30. Scanning Electron Micrograph of Metal Crossover

The above examination is centered on reliability analysis of the completed multilevel metal/oxide system, not on processing problems associated with manufacture. Several product reliability hazards are inherent in the multilevel system presently being used. Notable are:

- Via runout, shown in Figure 31. Second-level metal under vias from second to third metal is necessary to ensure that the oxide etch that cuts these vias does not contact passivation between second metal and first metal. In this instance, a multilevel short would occur between the second to third metal via and the first-level metal if the etching process continued long enough to reach first metal. Even if an M-L short is not present during processing, the thin oxide that could result at the via is a potential reliability hazard during life (see failure analysis of DRA-3008, No. 2005, Section IV-B-1-b).

  If the etching procedure is not complete (to avoid over-etch), the possibility of open vias, due to incomplete oxide removal, exists.

  Via etch times, rates, and characteristics are, therefore, quite critical due to the uneven underlying topography and possible misalignment of vias during the masking operation.

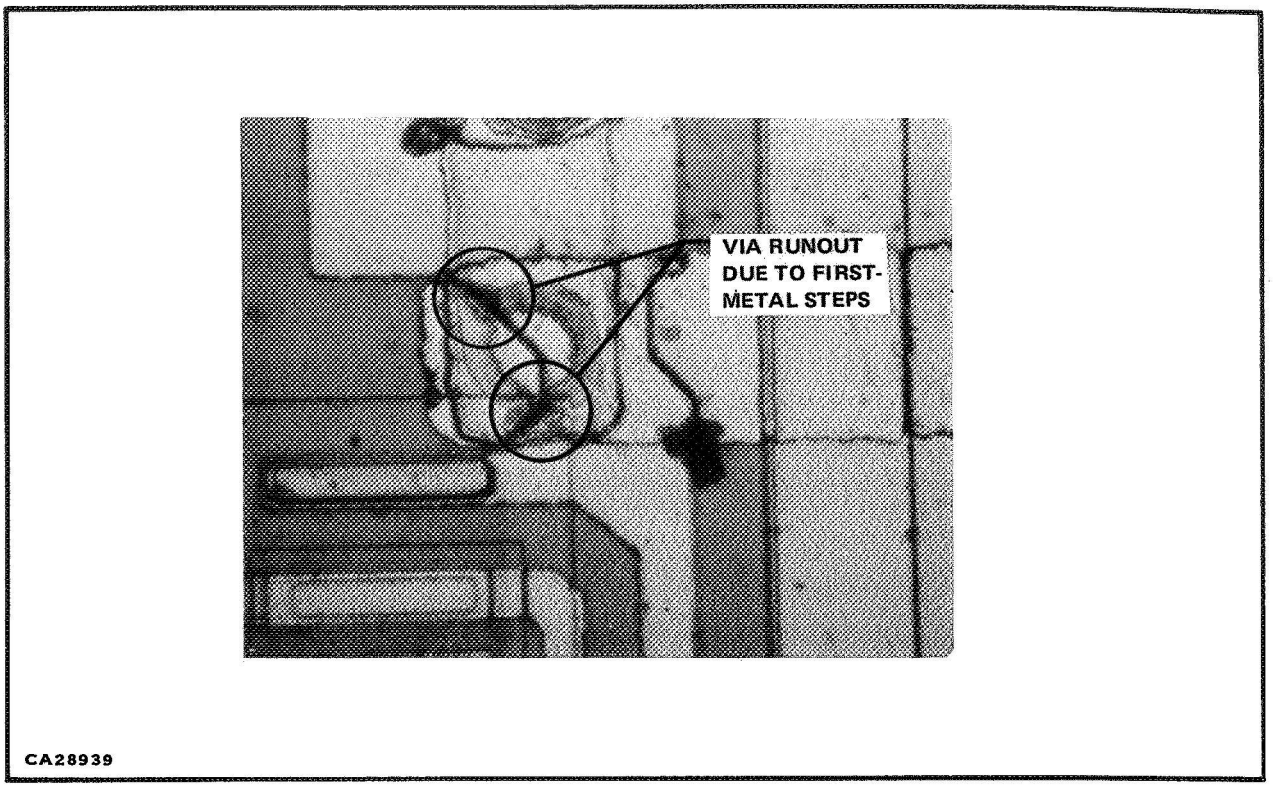


Figure 31. Via Runout (oxide via cut between 2nd and 3rd metal) at Oxide Steps Resulting from 1st-Level Metal Interconnect

Since this run-out via problem tends to manifest itself as lot oriented, strict process controls can minimize its impact. That is, a tightening of controls used in the oxide deposition and removal steps can reduce the frequency of occurrence.

There are also several quality control inspections that could be implemented to further control the problem. Documentation of testing at functional test could give a quantitative measure of the number of defective vias on a given slice. This quantitative measure of via integrity could be correlated with the visual inspection of the slice at this test station (or at a previous QC inspection). The data from each of these stations could be analyzed to establish a realistic maximum number of via electrical faults (due to runout) that could be tolerated.

- Figure 32 illustrates a hazard that can occur in the molybdenum-gold metal system if the process is not rigidly controlled. Arrow "1" shows an "open" in a second-metal conductor that can potentially occur over sharp-edged underlying metal films. However, this potential open has been shown to occur only infrequently. A more prevalent hazard is shown at "2" in Figure 32; this shows the difficult edge that must be covered by second-to-third-level insulating oxide when underlying metal layers have been processed to yield sharp edges. If the underlying metal and subsequent oxide-processing steps are not strictly controlled, multilevel shorts can occur due to inadequate oxide coverage.

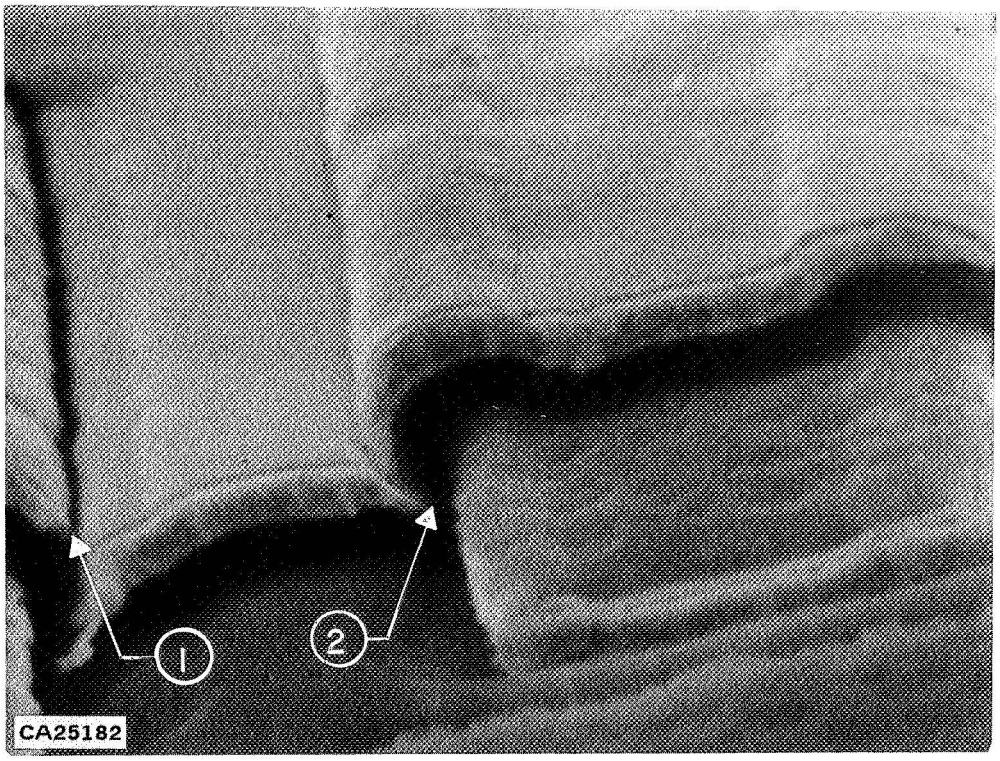


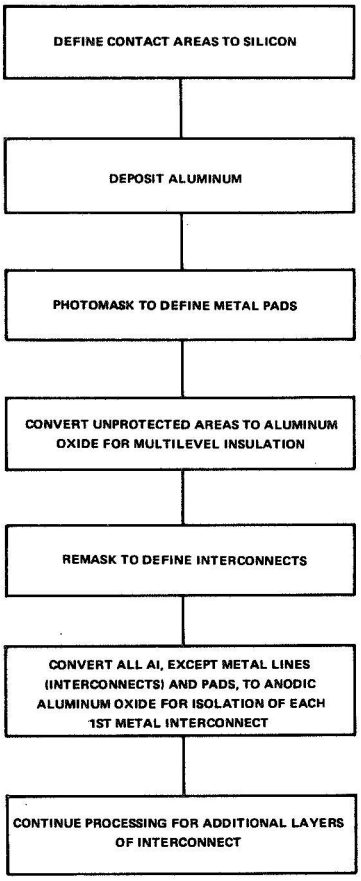
Figure 32. Potential Hazard in Molybdenum-Gold Metal System

The two problems discussed above can be controlled by meticulous care in the manufacturing process. However, as these impact the yield of a three-level metal system, they also affect cost and reliability.

To further alleviate the potential problem of sharp-edged Mo-Au metal lines (as well as provide more gradual steps over which to place multilevel vias), several new metal systems are currently being investigated.

Although the investigation has not yet produced functioning arrays of great complexity, much hope is held for the utilization of anodized aluminum as a multilevel metal/insulator system.

In this contemplated process,* metal-line definition is accomplished by converting aluminum to an anodic aluminum-oxide dielectric. The processing of a level occurs in the sequence shown on the accompanying diagram.



The primary advantage of this processing technique is the elimination of sharp-edged contours that must be crossed by subsequent passivation and metal layers. Figure 33 shows the relatively flat surface possible for two-level anodized-aluminum interconnects.

In summary, the currently utilized M-L metal system is adequate for processing complex arrays, but current developments indicate that superior systems are likely to be developed which will simplify processing and enhance reliability.

*Initial work carried out under Contract No. N00019-70-C-0487 by Texas Instruments Incorporated for Naval Air Systems Command, Dept. of the Navy, Washington, D.C.

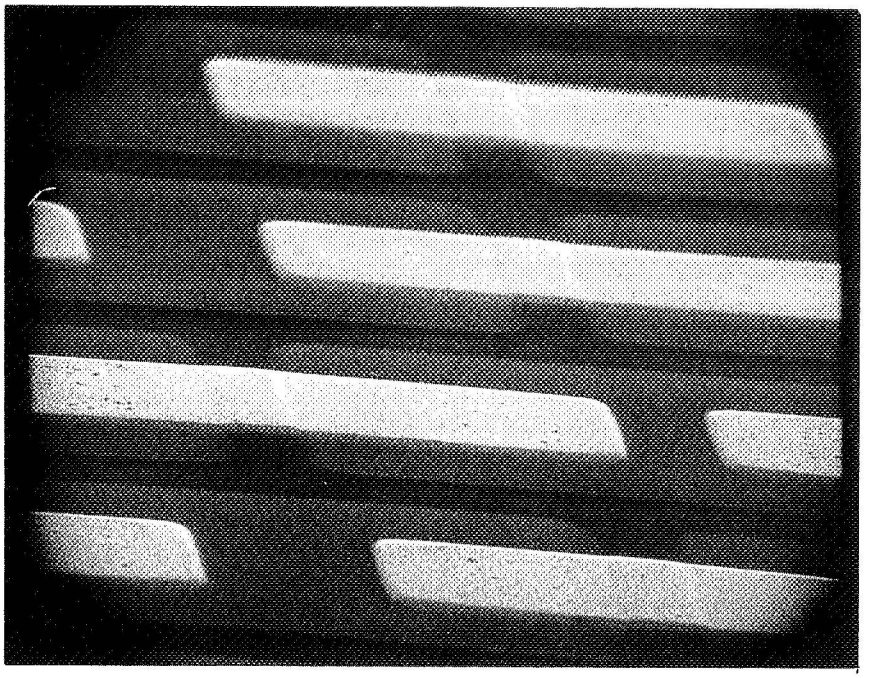


Figure 33. Two-Level Structure – Anodic Process

C. LSI PACKAGING CAPABILITIES

The environmental testing performed in conjunction with Contract NAS8-21319 has shown that the package developed for full-slice bipolar LSI is adequate to provide array operation under most expected aerospace applications. The summary of test results in Section II indicates that several conclusions are valid.

- The epoxy slice-mounting technique provides a resilient mount for the brittle silicon slice (≈ 12 mils thick) that eliminates slice-cracking problems inherent in mounting a 1-1/2 inch silicon slice to ceramic. The thermal shock/cycling test results show that the epoxy mount will not induce slice cracks previously seen when gold alloy and/or glass frit mounts were used.

- Gold-wire to gold-metal thermocompression bonding techniques are adequate for the LSI multilevel system; however, tighter and possibly innovative (i.e., infrared bonding monitors) bonding screens as well as perhaps operator controls were shown to be necessary and are currently being implemented.

- The hermetically sealed package shown in Figure 34 has proven to be quite satisfactory for full-slice LSI. Thermal shock tests, useful for seal integrity, failed to cause loss of hermeticity when stressed to MIL-STD-883, Method 1011,

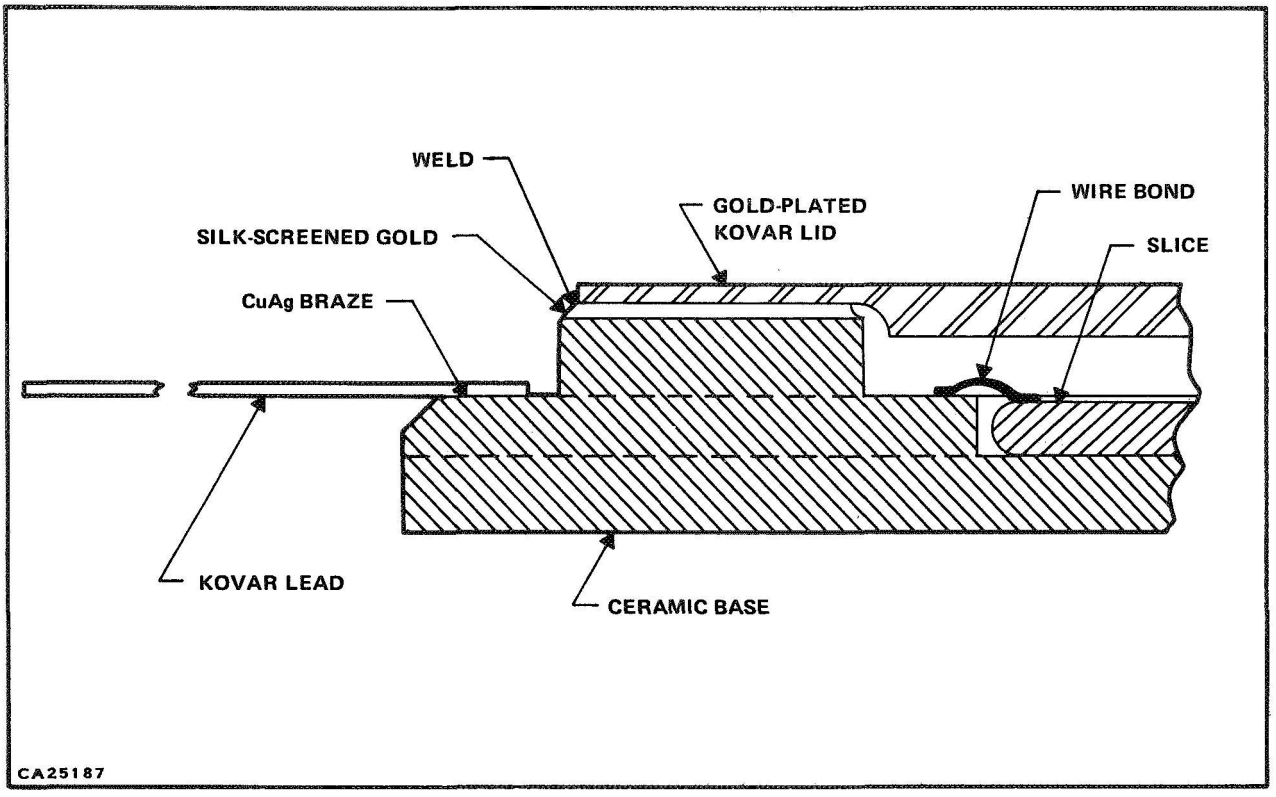


Figure 34. LSI Hermetically Sealed Package Construction

Condition C, for five cycles (after previous thermal shock stressing). During thermal shock stressing, no loss of hermeticity was seen up to and including temperature cycling through MIL-STD-883, Method 1010, Condition D. Final package failure was due to base ceramic crack, not loss of lid hermeticity.

- The external wire bonding, utilizing 1.5-mil gold wire, has proven to be quite reliable. Since cavity size does not restrict bond wire or pad placement, 1-1/2-mil wire can be used. To accommodate the larger ball size inherent in using 1.5-mil wire, the external bonding pads on the slice are approximately 10 mils square. Using this large pad and ball, therefore increasing the cross-sectional bond area between pad and ball, better (and more repeatable) bonds can be made.

- The Sylgard used to insulate repair bonds that now must be made on the surface of the slice (1-mil gold wire is used) appears to yield some added protection from moisture environments, such as would be experienced with a nonhermetic (epoxy) sealed package. However, the Sylgard does produce stresses on bond wires under thermally changing environments; hence, care must be taken in selecting a Sylgard compound and in assuring repeatability of application procedure and integrity of materials.

Additionally, since thermal stresses are transmitted to the bond wires, bond repeatability must be ensured to minimize discrepant bonds. One-hundred-percent screening is performed on each array under temperature-cycling environment to ensure the integrity of wire bonds.

- Extension of current discretionary routed technology to larger-diameter wafers and, therefore, greater-potential complexities for an LSI array necessitates a re-evaluation of packaging constraints for more complex arrays.

  Pin Limitations – As LSI complexities continually increase the difficulty of partitioning a system, remembering constraints such as device testing, manual interface with completed systems, etc. also increases. Even as LSI decreases system "pin" count (or logic-to-package pin ratio), the pin count on ever-increasingly complex LSI must rise, although at a decreasing rate when compared to logic complexity. When full-slice LSI advances, for example, to two-inch slices, a larger package and probably pin count will be necessary. The packaging configuration chosen by TI (see Figure 34) is capable of being expanded from a device cavity, as well as lead complement standpoint. Since the array is mounted to a printed wiring board in the same manner as a conventional flat pack, the increasing number of leads will not increase the difficulty of registration with drilled holes that would be experienced if a dual in-line pin configuration were used.

  In addition, the flat pack/ribbon lead package allows reliable and controllable reflow-solder techniques to be used to mount the array to the printed wiring board. Registration and mounting of 156 leads of a dual in-line or post-through-ceramic package and other solder techniques would not be as repeatable.

  Cavity Size – An increase of basic slice diameter (now 1.5 inches) would necessitate enlargement of the cavity for the two-inch slice. As the cavity was enlarged, a simple increase in header size and seal-ring diameter could yield the same reliable package seal. As the diameter of the lid would have to be increased, provisions would need to be made to ensure adequate structural rigidity of the lid.

  Power – As LSI device complexity increases, the power that must be dissipated by the package also increases. TI's discretionary routing technology allows the master slice to be designed using low-power TTL cells if advantageous. However, most current devices use standard TTL cells. A typical 400-gate equivalent device dissipates $\approx$ 3.5 watts at V_{CC} = 5.0 volts and 25°C T_A. The

thermal rise of the current package is to ≈ 143°C when operating at +125°C, T_A, with no heat sink. If significantly greater complexity devices are manufactured, adequate heat sinking will be necessary for the arrays when being operated at elevated ambient temperatures. A heat-sink plate can be readily applied to the flat ceramic base of the package to provide a thermal system of adequately low thermal resistance for complexities anticipated in the near future.

SECTION IV

RECOMMENDATION AND GUIDELINES FOR DESIGN, PROCUREMENT, AND USAGE OF BIPOLAR LSI IN HIGH-RELIABILITY APPLICATIONS

A. SCOPE

This section gives the results of tests summarized in the previous sections of this report. The section presents information made available by this contract effort; therefore, the recommendations are based upon Texas Instruments discretionary routing technique for producing bipolar arrays.

B. ELECTRICAL TESTS

1. Functional Testing

a. General

As the state of the semiconductor art produces increasingly complex devices, the problems associated with final electrical test of arrays increase dramatically. Even though the array user usually demands only a certain function (therefore, buying to a black-box specification, he only cares that, from the external pins, the array functions in his system), this in itself presents difficult testing problems when the current complexities of LSI devices are considered.

This black-box concept usually necessitates a functional-only final test for electrical acceptance. In many cases, however, device complexities preclude even this 100% (of all logic combinations) functional test. For example, consider a device with 30 inputs; this complexity is well within current capabilities for several different technological approaches to LSI. With 30 inputs, there are approximately 10^9 different combinations possible for the binary inputs anticipated. Assuming a test rate of 10 tests/microsecond, 2.75 hours are still required to exhaustively exercise the inputs to the device. Because dedicating a computer to testing an array for 2.75 hours is unrealistic, an alternate approach to array testing must be considered. Also, even if all possible input combinations could be applied, if some sequential logic elements were employed in the array, the sequence of the input patterns (this governs the state of the sequential logic) must be analyzed to ensure adequate testing of the sequential elements.

b. Methods of Test-Sequence Generation

To functionally test an array and yet not randomly input patterns and check for correct output conditions, a test approach for generating the input sequence must be established. Several basic assumptions are integral to the determination of functional faults in random logic arrays. Faults are:

- Logical nature (1 is interpreted as 0 or vice versa).
- Permanent (not intermittent) during test application.
- Represented by each connection being shorted to power or open, stuck at 1, or stuck at 0. Stuck at 0 is considered the same as shorted to ground.

Utilizing these concepts, several basic approaches are applicable to the testing of logic arrays. The approaches, with appropriate comments, are as follows:

- Random Exercise and Physical Comparison – A known good array and that under test are tested simultaneously with identical inputs applied to each. If outputs are not identical, the test array is assumed faulty.
- Physical Replacement – The array under test replaces a known good array in a known good machine. The machine is then operated to determine that it still functions properly.
- Simulated Replacement – Simulate good machine and array interfaces in an operating sequence; then, apply these input patterns to the test array.
- Random Exercise and Simulated Comparison – Simulate a good array with random inputs; then, apply the same inputs to test array to see if outputs agree.
- Deterministic/Algorithmic Approach – Propagate the possible fault to an output pin. Initial set-up conditions must be such that, if D represents stuck at 1, a zero should be placed on the line in question. Subsequent inputs are used to propagate the fault represented by D to an output pin for comparison to wanted data.
- Physical Fault Insertion – Using predetermined test sequences, insert faults physically into an otherwise good machine. Apply the test sequences to see if the tests detect the faults.
- Simulated Fault Insertion – Analogous to physical fault insertion, except that the faults are not physically inserted into a good machine, but rather into a simulated model of the good machine.

TI has chosen the simulated-fault method for functional testing of LSI arrays; the basics of this method are discussed in the following paragraphs.

c. Simulated-Fault Method

The simulated-fault method uses large-scale digital computers to simulate the operation of the logic for all possible logical faults. The good logical design and each fault are simulated separately; then, a test schedule is chosen so that the good device will perform differently from any of the possible faulty devices. Successful completion of this test sequence assures that the device under test is the good one, and does not contain any logical faults.

Faults simulated are:

- Any gate output shorted to power or shorted to ground.
- Any gate input shorted to power or shorted to ground.
- Any signal path open.

Where two or more faults are logically indistinguishable from one another (such as the input to an inverter shorted to ground, and the output shorted to power), they are simulated as one fault.

Figure 35 shows commonly used fault models for a NAND gate. This type of fault model is expanded for use with other logic cells. Utilizing these fault models for functional stuck-at-1 or 0 failures, a test sequence can be generated.

The computer procedure used to choose the test sequence follows:

- Choose an input pattern and apply it to all devices.
- Simulate the behavior of the good device and of each faulty device under the input pattern.
- If the behavior of the good device is different from that of one or more of the faulty devices, the pattern is acceptable. If not, go to procedure 5.
- Record the output pattern of the good device and of the distinguishable faulty devices.
- Change the input pattern and go back to procedure 1.
- The goal is a sequence of input and output patterns so that the output of each faulty device is different from the good device at least once.

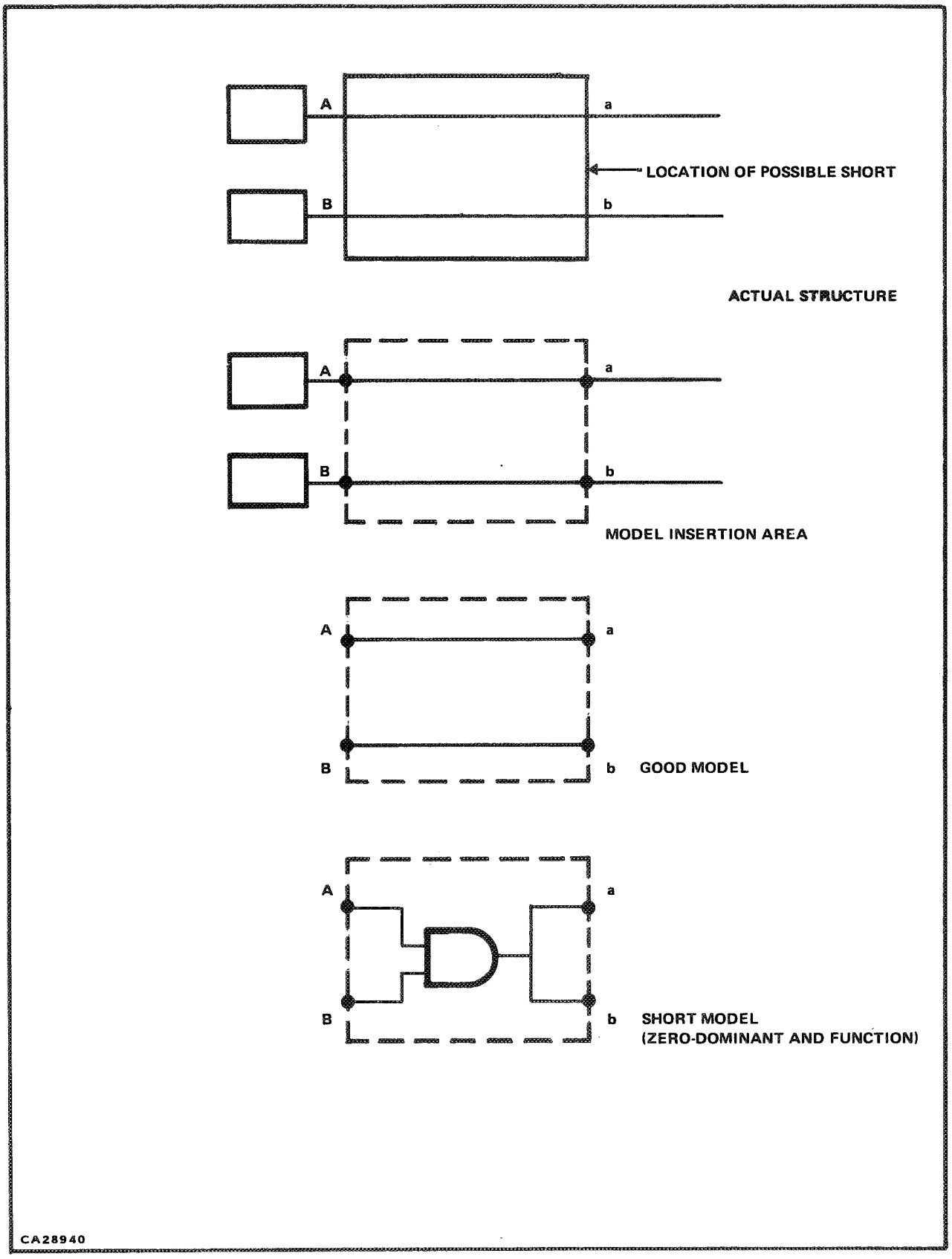


Figure 35. Signal-to-Signal Short Model

The simulated fault method of logical testing offers several advantages from the user's point of view. They are:

- The complete array test sequence can be specified by the manufacturer.
- User-generated tests can be validated with respect to accuracy of input-output patterns.
- User-generated tests can be graded with regard to completeness of test relative to the TI fault models for cells. This will show the user the percentage of I/O connections (internal to array and external) that has been exercised to ensure that connections are not stuck at 1 or 0.

d. Limitations of Procedures

No functional testing procedure tests a random logic array under 100 percent of the possible logical combinations.

For example, if we assume a 15-bit register of flip-flops, each flip-flop with 4 inputs – J, K, preset, clear – (the clock has been omitted since it normally appears to all flip-flops simultaneously) each cell or flip-flop has 2^4 possible combinations of inputs.

Since we have 15 total "bits" of sequential logic, we have $(2^4)^{15} = 2^{60}$ possible combinations of conditions, or 1.153×10^{18} possible combinations.

Testing at a fast 10-MHz rate, we have

$$\frac{1.153 \times 10^{18} \text{ tests}}{1.0 \times 10^{7} \text{ tests/sec}}$$

$$1.153 \times 10^{11} \text{ seconds to test}$$

$$\frac{1.153 \times 10^{11} \text{ sec}}{8.64 \times 10^{4} \text{ sec/day}}$$

We would need $0.1334 \times 10^7 = 1.334 \times 10^6$ days to test.

To avoid the unrealistically high test time necessary to exercise the array through all possible logical combinations, an alternate approach must be taken to effect a functional test. As discussed in the previous section, TI has chosen the fault-simulation approach to LSI array testing. Several basic problems and potential aids in solving these problems are discussed in subsequent paragraphs.

Logic-simulation techniques must completely define the state of each array (both good and with each fault inserted) to determine a test sequence that will exercise each node of the logic to ensure no stuck-at-1 or 0 conditions. If the logic designer has designed-in numerous feedback loops from and to sequential logic cells within the array (and limited external access to these cells), defining the state of these cells can be difficult and time consuming. To alleviate this problem, comprehensive interaction between the logic designer and those responsible for testing the completed array must be maintained. In many cases, the partitioning of the system to minimize pin/package count is performed irrespective of testing that must be accomplished on the final arrays. Often, limited concessions in pin count (i.e., by bringing to external pins clear inputs to flip-flops) can dramatically decrease software-simulation problems associated with array testing.

The logic testing described in Section II was based upon detection of single faults, either to ground or to power. An additional fault model that could be considered to more completely test an array would be fault modeling, including signal-to-signal short diagnosis (see Figure 35).

The inclusions of signal-to-signal faults, however, would greatly increase the complexity of the software necessary to test an array. For example, using a typical 250-gate array:

Item	Single-Fault Model	Addition of Signal-to-Signal Faults
No. of faults	300	32,000
Simulation words	10 X 125	1000 X 125
No. of simulations	1	1000

The addition of signal-to-signal fault modeling substantially increases not only the complexity of the simulation program that determines the selection of input test patterns, but also the running time and complexity of the actual testing sequence.

TI's experience in its bipolar LSI program has shown that the single-fault modeling approach provides testing results capable of producing arrays which operate consistently in a system environment.

2. Parametric Testing

a. Switching Time and Data Rate

In using the input combinations derived to ensure that the logic of the array is consistent with the design logic, the user must define methods and constraints of applying and measuring the ones and zeros of input combinations as well as outputs of the array.

Design characteristics of TI's bipolar LSI arrays (as well as others) parallel those of established families, such as TTL. Functional testing of completed arrays should utilize the testing principles that have been proven effective in other technologies (testing for this contract has shown these tests consistent with LSI arrays). In most cases, established guard-banded limits on parameters are effective in eliminating marginal units susceptible to failure by parameter degradation.

The methods of performing functional tests and the parametric considerations involved are discussed in subsequent paragraphs.

- Basic considerations dictate that, for TI's bipolar LSI, input and output parameters be checked to determine compatibility with external TTL elements that would typically be required to interface with the array. Table V indicates parameters always accessible for inputs and outputs of completed arrays that should be checked at final test. The parameters shown above are particularly good indicators of array degradation with time and, as such, should be performed before and after burn-in testing to monitor device characteristics with respect to time.

Table V. Parameters for Array Inputs/Outputs

Test No.	Parameter Measured	Significance
1	O-level input currents on accessible inputs.	Indicates integrity of input resistor of cell. Changes indicate diffusion or metallization anomalies at input transistor or in M-L metal.
2	Output short-circuit current with output at 1 level (for accessible outputs).	Indicates h_{fe} of drive transistor. Lower drive capability could indicate marginal performance at low temperatures. Also indicates integrity of M-L metal and feedthroughs when carrying high currents.
3	1-level input current.	Abnormally high input currents can indicate contaminated passivation layers and anomalies in input transistors.
4	V_{out} for O-level output at maximum TTL specified load of 16mA.	An increase in V_{out} with life can indicate degradation of h_{fe} or significant shifts in resistor values.

- Characterization of bipolar LSI devices, both at the cell and array levels, has indicated that the tests of Table VI are valuable indicators of manufacturing consistency and quality. The tests, as outlined, should be performed at the cell level (prior to interconnect) as well as at the array level where possible. In most cases, the tests shown are sufficient to guarantee array operation over the specified temperature range ($T_A = -55$ to Max, with Max determined by complexity, power dissipation, and package of a particular array, Max = 125°C T_A for TTL).
- The tests reported in Table VI are intended to duplicate, at the cell level, the potential worst-case fan-in and fan-out, and V_{cc} levels for cells interconnected in a system. For example, the test labeled "V_{on}" checks the output voltage of a gate to the data-sheet limit (0.4 volt) with $V_{cc} = 3.75$ volts and sunk current of 31 mA. This test is more severe than what should be seen as worst case in a system environment ($V_{cc} = 4.5$ V, $I_{sink} = 16$ mA). This type of testing should be done both at a cell level and on the array level; the accept/reject criteria must be determined to fit the logic design of the array to be tested. For example, if an array pin input goes to five gate inputs internally, the input $I_{in(1)}$ current limit should comprehend the increased current due to the multiple inputs.

b. Data Rate/Frequency of Test

The data presented in Section IV-B-2 show that, within a given slice, the gate and flip-flop transfer characteristics of the electrically good cells are quite uniform, which is to be expected since the delay times are primarily a function of device geometries and diffusion concentrations.

At probe test, the TTL cells are tested to ensure functionality to established input/output conditions. In addition, certain tests are performed to ensure that the diffusion (i.e., transistor parameters) characteristics, also checked before metallization, remain within established limits. Tests such as I_{os}, $V_{out(0)}$ (load of 10), which monitor the h_{fe} characteristics of the cell output and drive transistors, can be used to verify the switching characteristics of the cell. That is, experience and design analysis show that TTL switching speeds are predominantly a function of h_{fe} (as well as resistor values) of the transistors and dc tests that verify the integrity of the diffusion operation can ensure that device transfer characteristics will consistently fall within acceptable limits.

An additional negative consideration in attempts to utilize switching times as an indicator of device reliability is the inherent difficulty in reproducibly measuring switching times that, for bipolar cells, fall below the 10-ns range. Measurements in this range typically are only accurate to ±10%, and slight fixturing changes cause even greater inaccuracies. When measuring delay at the cell level, probe capacitances become quite significant in the measurements.

Table VI. Bipolar LSI Test Conditions (@ 25°C)

Test	V_{CC}(volts)	Inputs	Limit Parameters	Forcing Condition	Comments
$I_{IN(1)}$	5.5	6 V, GND	$I_{IN(1)} < 20\ \mu A$	6 volts on one input	Untested inputs to GND.
B_{VI}	5.25	1.00 mA, GND	$V_{IN} \geq 5.5$ volts	1.0 mA	Unused inputs to GND.
$I_{IN(0)}$	5.5	0.4 V, 2.4 V	I_{IN} (@ 0.4 V) ≤ -1.44 mA	0.4 volts	Input at –55 volts to be <1.6 mA.
V_{ON}	3.75	2.4 V, GND	$V_{OUT(0)} \leq 0.90$ volts	31 mA (sink at output)	Check output transistor for adequate drive at low temp.
V_{ON}	4.50	0.8, 1.7 V	$V_{OUT(0)} \leq 0.40$ volts	20 mA (sink at output)	Drive capabilities over temperature range.
$V_{OFF(MIN)}$	4.50	0.8, 1.7	$V_{OUT} \geq 2.55$ volts	–0.8 mA (out of input)	1. Noise-margin capability over temperature range.
$V_{OFF(MAX)}$	4.75	2.4 V, GND	$V_{OUT} < 4.0$ volts	+40 μA	2. Force outputs for $V_{OUT(1)}$.
$I_{OS(MAX)}$	5.5	2.4 V, GND	$I_{OUT} < -49.5$ mA	Short output to 0.0 volts	1. Minimum value of output resistor. 2. Max. value of output resistor. 3. Operation over temp. range.
$I_{OS(MIN)}$	5.5	2.4 V, GND	$I_{OUT} > -20.8$ mA		
$I_{CC(0)}$	5.5	4.5 V, GND	$I_{CC} < 19.8$ mA	V_{CC} voltage	Guard-band temperature operation.
$I_{CC(1)}$	5.5	4.5 V, GND	$I_{CC} < 7.2$ mA	V_{CC} voltage	

Therefore, switching-time measurements, both at probe and after cell interconnect, are not particularly valuable indicators of device reliability per se. For the reasons mentioned above, the major consideration in testing speed for bipolar LSI should remain concerned with the maximum anticipated logic complexity and its associated test complexity. The maximum data rate must be great enough to allow a reasonable test time for the functional tests.

Although performing 100% switching testing (either at array or cell level) does not appear to be useful from a reliability viewpoint, a sampling test of completed array-switching characteristics for system compatibility is useful. Analysis of the array logic design to yield the worst-case delay path and subsequent testing of that path are normally sufficient to ensure array delays consistent with the system implementation.

3. Temperature Testing

Table VI shows typical parametric testing that should be performed at 25°C to determine array characteristics under extended temperature conditions. For most cases, the testing indicated will ensure no failures due to parametric degradation at temperature extremes, but this is not true for isolated functional failures. For example, although an output may pass the I_{OS} test at 25°C with a metal line, with thin or minimum coverage at an oxide step, this same device could fail when the metal line becomes an open at temperature extremes. In many cases, a nonoperating thermal cycling test would not detect these potential device failures.

In the more mature technologies, where design and manufacturing constraints are well established (and a parametric data base exists), testing at 25°C is much more indicative of performance over the recommended temperature range. However, the normally limited throughput of high-reliability LSI dictates that all devices should be screened at temperature extremes to ensure there are no design or assembly flaws which relate to the mechanical (viz., metallization, packaging) aspects of the device.

4. Array Testing at Temperature Extremes

The testing of LSI bipolar arrays at temperature extremes can prove effective in determining the integrity of LSI arrays. Temperature-testing data can provide valuable information in two areas of LSI testing:

- Investigating device integrity as a function of temperature at time "zero" (before life test or usage).
- Providing conditions for investigation of various parameters under worst-case conditions.

These two usages are explained in the following paragraphs.

- Investigating Device Integrity from a Functional-Mechanical Standpoint

  The fabrication of bipolar LSI arrays has introduced many new considerations into the reliability evaluation of microcircuits; one of these is new schemes of interconnecting and packaging multicell LSI systems. The mechanical (packaging, metallizations, etc.) integrity of these arrays is substantially different from the established integrity of TTL-type devices and, for this reason, the devices should be subjected to temperature testing that is not as critical as for established technologies.

  To amplify, a large amount of statistical information is available for TTL devices, based on high-volume production over many years. These statistical data enable parameter characterization of TTL devices at probe (@ 25°C) that can predict temperature operation by guard banding parameter limits.

  Much LSI technology (viz., TI's LSI discretionary routed arrays) is based upon the established TTL technology. Hence, full utilization is made of information resulting from TTL production experience. Wafer probe on LSI/DRA units, therefore, can isolate cells that are not only functional, but capable of operation over the full temperature range of −55° to +125°C. However, after cell characteristics are defined, subsequent operations can jeopardize the array integrity as a function of temperature. For example, experience on this contract has shown the necessarily different-from-normal bonding methods and screens to be insufficiently defined to ensure a repeatably reliable wire bond.

  Although this processing flaw was detectable by utilizing nonoperating thermal screens (temperature shock and cycling), production experience has shown that some intermittent array failures can be screened with high-temperature final testing.

  In defining the integrity of a Sylgard (high-purity junction-coating resin) material to encapsulate repair bonding wires, temperature-cycling testing showed no adverse effects on array electrical characteristics at 25°C. Subsequent testing at +125°C, however, showed intermittent failures that were traced to Sylgard expansion pulling up ball bonds. The encapsulating material was changed to eliminate these temperature-sensitive failures.

  By extending this case experience to other design conditions, such as multilevel feedthroughs, clearing of multilevel metal shorts, or ROM programming by capacitive discharge, we can see that all these unique fabrication methods (or designs) can have intermittent failure mechanisms which could be a function of temperature and, therefore, would not show up during nonoperating temperature testing, followed by electrical testing at 25°C.

- Parameter Investigation Prior to Usage or Life Test

  Parametric characterization of LSI devices can be effectively utilized in determining their long-term reliability. As has been the procedure in testing several gate complexity devices, evaluation of LSI devices at temperature extremes is useful in supplying worst-case conditions to the device to be evaluated. Evaluation under worst-case conditions, before and after a burn-in period, amplifies device anomalies and can detect failure-prone devices.

5. Test Cells

a. General

Test cells have two distinct areas of applicability with respect to bipolar LSI reliability evaluation. They are:

- Test devices can and should be used in initial evaluation of device capabilities from an environmental-stress viewpoint.
- Test cells on each device have limited applicability in defining lot/processing-oriented problems in bipolar LSI.

Test cells and devices that fit into these two categories, as well as their usefulness, are described in the following paragraphs.

b. Test Arrays for Environmental Stress Evaluation

As demonstrated by the environmental test program for this contract, test devices can be of great value in determining environmental capabilities of an LSI design. A test device is particularly valuable in permitting evaluation of environmental capabilities (and inherent device weaknesses) prior to committal of large funds to a custom array design. Moreover, the same test array can be utilized after initial qualification of device capabilities to monitor the repeatability of the manufacturing operation on a lot-by-lot basis. That is, each identifiable lot can be evaluated for mechanical integrity (multilevels and packaging) by destructively testing the monitor device.

The structure of the test device for an environmental test and/or process monitor of multilevel metal bipolar LSI should include several test cells. They are:

- Series vias and multilevel metal runs over typical first-level contours (to simulate the cross section oxide step conditions present in active arrays) to test for via and metal integrity over oxide steps. The total number of crossovers and vias of the pattern should approximate the total typical for an array of the complexity to be manufactured.

- Since the discretionary routing scheme of multilevel interconnects on a wafer has not advanced to where no repairs are necessary after interconnection, a portion of the test vehicle should be evaluated for repair-procedure integrity. The pattern would typically involve opening second- and third-level interconnects through capacitive discharge and using wire-bonding techniques to repair the opened signal/power path. Bond-wire lengths and placements should be designed to duplicate typical repair procedures on active arrays.
- Wafer attach, external ball bonding (from the slice to the package), and package sealing should be consistent with typical manufacturing procedures. Testing will, therefore, yield information not only on slice characteristics, but on packaging (wafer mount, hermetic seal) integrity.

c. Test Cells on Active Arrays

The results of test-cell testing for this program indicate that isolated faults normally associated with discretionary routed (three-level) metal will typically not be evidenced.

The test cells employed typically perform a function of monitoring only general multilevel integrity; cell characteristics are fully defined at wafer probe prior to multilevel interconnection. Test cells on first metal would typically not add significantly to wafer-characterization data already available (and inherent) in separation of good from bad cells.

The cell-probe tests (structured to follow Table VI) can make available, by data logging when necessary, information to fully characterize cell parameters, i.e., BV_{ebo}, resistor values, h_{fe} of critical transistors, etc. Application of multilevel metal to the characterized wafer introduces a single major failure mechanism – multilevel shorts due to oxide faults (introduced by various processing anomalies, such as run-out vias, preferential oxide etch along oxide steps).

Typically, these multilevel defects occur as isolated failures, and infrequently over the area of the slice. For multilevel test sites to help define the reliability of the completed LSI array, an unrealistically high percentage of multilevel real estate would need to be committed to them. An alternate and preferable approach to determining the reliability characteristics of multilevel metal LSI devices would be to maintain comprehensive records on the magnitude and nature of multilevel repairs necessary to effect a functioning array. Normally, the amount of rework necessary can be correlated to the quality and ultimate reliability of the completed array. User experience with manufactured arrays should be used to determine the relationship between array quality levels, amount of necessary rework, and acceptable system reliability.

Although test elements used to define reliability concerned with isolated defects (M-L shorts) do not appear to be valuable, several on the slice could be useful for destructive test-wafer evaluation; that is, evaluation of wafer characteristics typically uniform over a slice. A typical cell, to be destructively tested to identify M-L characteristics, could include:

1) Several multilevel runs at right angles to each other to be used for:

   - C-V analysis to evaluate oxide stability
   - Voltage stressing to destruction for analysis of oxide integrity over metal steps

   A data base would need to be established to determine applicable delta limits for dielectric strength and statistical variation of fault density within the oxides.

2) A series of multilevel vias on second and third metal (total number should at least equal 100) to characterize M-L vias. The tests on series vias should include:

   - Average via resistance
   - Destructively test vias with increasing current stress until failure occurs. A standard test procedure should be developed that indicates true current-carrying capabilities and does not induce failures through increasing metal temperatures.

In implementation of any testing (on a test site per slice basis), the data must be evaluated carefully to ensure that levels of tests are indicative of the quality of devices. The analysis must include consideration of the possibility of discrete processing flaws inherent in any batch-processing operation. Visual examination prior to testing should be performed to criteria used over the remainder of the slice to help evaluate the applicability of various visual-inspection criteria.

C. PROCUREMENT RECOMMENDATIONS FOR LSI

Generally, these procurement guidelines should be performed in the order specified in the following paragraphs to ensure reliability results consistent with anticipated program needs.

1) Initial goals for system design should be translated into technology needs. For example, system speed, power, and size requirements should be translated into performance needs for componentry; that is, the system should be implemented with CMOS, TTL, low-power TTL, bipolar/LSI, etc. Reliability Engineering interface is necessary at this point to ensure that reliability aspects are fully comprehended in this system decision.

2) Based on the above decision, survey technological approaches capable of meeting system needs to determine processing limitations that could affect reliability of the system. For example, if LSI/DRA were chosen for system implementation, particular emphasis must be placed on evaluation of the multilevel interconnection system. If MOS were used, the technology involved should be reviewed and studied in detail.

3) Based on the detailed list of manufacturing characteristics derived for the above action, a preliminary manufacturing (primarily packaging and metallization) test program should be implemented to determine the various device's capability to meet needed system environmental/reliability requirements.

   This preliminary evaluation could be most cost effective when several products appear capable of meeting requirements, if all are evaluated utilizing test devices rather than functioning array. Large start-up and design costs associated with a custom array can be delayed until a preliminary environmental strength/stress capability study showed the device design to be capable of meeting anticipated system requirements.

4) The reliability evaluation of action 3, above, is meant only to uncover design limitations concerned with the mechanical attributes of the devices. Again, prior to committal of a system to partitioning and custom device design by a particular manufacturer, electrically similar (at least utilizing similar basic "cells") devices should be subjected to electrical characterization for evaluation of electrical stability with respect to time on operating life test. This evaluation again will enable the reliability activity to assess the long-term integrity of the technology before large investments are made to commit a design to a particular vendor's custom-design group.

5) Concurrent with the evaluations of a given technology mentioned above, the reliability activity must interface with the system-design group to ensure design and partitioning consistent with reliability concepts concerning electrical testing.

   - Each array (subsystem) must be structured so that adequate testing of array logic can be effected, remembering difficulties concerning functional testing discussed previously.

   - A sufficient sampling of inputs/outputs of each cell type should be available for sample parametric testing at the array level.

   - Test cells (several mentioned previously, to include diffusion, registration, alignment, and metallization) should be specified in each array design, where applicable, to enhance and simplify reliability analysis of the arrays.

6) Initial parts, usually procured to populate a prototype system, often are accepted with little or no Quality Control involvement and/or screening. Rather, these "prototype" parts should be screened to those limits shown to be effective in the analysis of design weaknesses by action 3, above. Screening limits should purposefully be somewhat less stringent than the operating system parts, but should be sufficiently stringent to point out potential device quality, reliability, and yield (as it affects reproducibility) problems. Analysis of test results should be directed toward establishment of process capabilities and development of meaningful controls for the production units.

7) Based on knowledge generated by action in 3 and 6, above, the final reliability screening specification can be intelligently negotiated with system-operating conditions considered, and not based solely upon broad application of general MIL-STD procurement specifications; in various cases (viz., internal visual examinations as applied to multilevel metal LSI or screening levels meant for SSI complexity devices that are not consistent with true LSI packages or processes) strict application of a MIL-STD has limited usefulness. The added base of knowledge prior to production of complex and expensive devices for the actual system will also be useful to ascertain the degree of repeatability for a given manufacturing operation. With LSI complexities increasing and device numbers necessary to populate a system dwindling, the repeatability information generated by lot-acceptance concepts is not as readily available.

8) After system implementation, some device failures are still likely. Added responsibility must be placed on the reliability engineer to ensure timely and accurate analysis of all failures. Although analysis becomes increasingly complex, it must also become increasingly accurate since fewer parts will be available for examination.

   Since the analysis of LSI system failures must supplant information usually available as a result of device and/or lot qualification for SSI/MSI systems, accurate documentation of system-operating conditions and testing must be maintained. Each field failure must be well documented to provide an adequate data base to supplement necessarily limited device life-test results.