N71-29904

NASA TECHNICAL MEMORANDUM

NASA TM X-2314

NASA TM X-2314

A DIGITAL REGULATED SOLAR ARRAY POWER MODULE

by James E. Triner

Lewis Research Center

Cleveland, Ohio 44135

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • JULY 1971

1. Report No.
NASA TM X-2314

2. Government Accession No.

3. Recipient's Catalog No.

4. Title and Subtitle
A DIGITAL REGULATED SOLAR ARRAY POWER MODULE

5. Report Date
July 1971

6. Performing Organization Code

7. Author(s)
James E. Triner

8. Performing Organization Report No.
E-6215

10. Work Unit No.
120-26

9. Performing Organization Name and Address
Lewis Research Center
National Aeronautics and Space Administration
Cleveland, Ohio 44135

11. Contract or Grant No.

13. Type of Report and Period Covered
Technical Memorandum

12. Sponsoring Agency Name and Address
National Aeronautics and Space Administration
Washington, D.C. 20546

14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract
A concept for regulating the power developed on a solar array at the source (i.e., on the array) was experimentally investigated. This concept permits the power developed on the array to be delivered directly to an electrical load at the voltage or current required by the load. In the particular concept investigated, regulation was achieved by controlling the power output of array segments arranged in series and in a weighted binary fashion. The power output of an array segment could be removed from the series by shorting switches.

17. Key Words (Suggested by Author(s))
Power supplies; Electric batteries; Power supply circuits; Current regulators; Voltage regulators; Switching circuits; Photo transistors; Photo diodes

18. Distribution Statement
Unclassified - unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	19	$3.00

*For sale by the National Technical Information Service, Springfield, Virginia 22151

A DIGITAL REGULATED SOLAR ARRAY POWER MODULE

by James E. Triner

Lewis Research Center

SUMMARY

A concept for regulating the power developed on a solar array at the source (i.e., on the array) was experimentally investigated. This concept permits the power developed on the array to be delivered directly to an electrical load at the voltage or current required by the load. In the particular concept investigated, regulation was achieved by controlling the power output of array segments arranged in series and in a weighted binary fashion. The power output of an array segment could be removed from the series by shorting switches.

The regulation obtained experimentally met the design goal of 0.1 percent regulation for a 1000-volt solar array module. The regulation was insensitive to array lighting and thermal variations. No major switching transients were observed. Worst-case power dissipations for the switching circuitry was 450 milliwatt. Because of equipment limits, the regulation demonstration was confined to a range of voltage from 500 to 755 volts and a range of current from 0 to 40 milliamperes.

INTRODUCTION

Solar arrays using silicon solar cells are essentially the exclusive source of electrical power for Earth satellites. The silicon cells used on these arrays are inherently low-voltage devices. The anticipated advent of satellites incorporating ion thrustors and high frequency electron tubes (traveling wave tubes, etc.) has created a need for dc power supplies with 1000- to 16 000-volt outputs. The present thrustors require from 1000 to 5000 volts dc at the accelerator electrodes. The near future tubes may require up to 16 000 volts dc.

Conventional solar arrays are wired to deliver their dc power at less than 100 volts. The high-voltage requirements noted previously are met with low-voltage solar arrays by transforming the low voltage into high voltage with heavy and complex power conditioning equipment, which typically weighs 33-66 kg/kW (15 to 30 lb/kW).

Since the dc power requirements are expected to be met by solar arrays, a departure from the conventional method of developing conditioned solar array power may be desirable. In this regard, it appears desirable and feasible to

(1) Develop solar array power at the voltage levels required by the major using loads

(2) Provide on the array itself, the regulation required by the major using dc loads

Such a high-voltage solar array (with integrated dc power conditioning equipment and capable of delivering discrete voltage levels from 1000 to 16 000 V to a using load) should reduce the complexity and weight and increase the overall reliability of the total power system. On a system basis a weight savings of 22 to 44 kg/kW (10 to 20 lb/kW) should be achievable using integrated solar array technology.

The technology necessary to design the high-voltage solar array described here does not now exist. To obtain the technology to design such arrays, research and development effort is necessary in the areas of (1) operating high-voltage solar arrays in a space environment, (2) providing power regulation and switching integral with the array (3) developing deployable large area array configurations.

Studies were performed (refs. 1 and 2) on the feasibility of operating a high-voltage solar array (area (1)) in a space environment. The results of these studies indicate that the high-voltage solar array concept is practical. Experimental verification of these study results is underway. The array deployment techniques (area (3)) being developed by a number of organizations are adaptable to either the low- or high-voltage array configurations.

The purpose of this report is to present preliminary evaluations of the concept to regulate solar array power (area (2)) and to demonstrate the performance characteristics and capabilities of one type of electronic circuit involved. The experimental evaluation of the solar array regulation concept was performed on a 755-volt, 50-milliampere solar array module. A binary coded decimal up-down counter and digital clock were used to supply control logic to the regulator system.

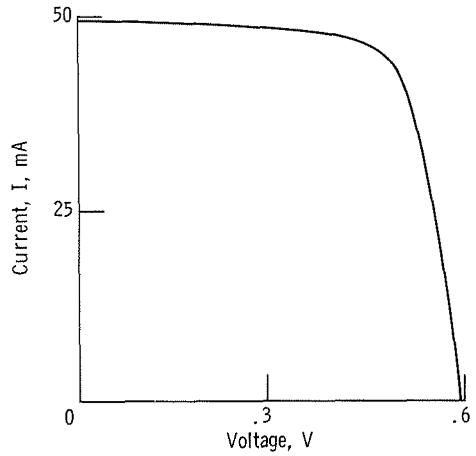
The electronic circuitry developed for this particular regulating scheme could be applied to systems with voltage ranges from 1000 to 16 000 volts and a voltage variation equal to or less than 0.1 percent. A similar type voltage regulation scheme could be developed with a digital computer system supplying the control logic.

REGULATING CONCEPT

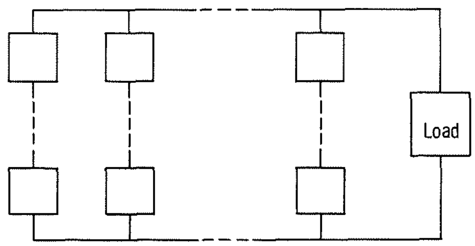
In a power system there are three basic subsystems. They are (1) the power source (2) a conditioning network and (3) the load which determines the size and complexity of the power source and the conditioning network.

The power source for most spacecraft is obtained by direct conversion of solar energy into electrical power by solar cells. Figure 1(a) shows the current-voltage characteristics of a single 1- by 2-centimeter n-on-p silicon solar cell. Such solar cells (or other size cells) can be connected electrically in series, parallel combinations to satisfy the power requirement of a load. As an example, the load and the solar array configuration (1 by 2 cm cells) needed to supply the load is shown in figure 1(b). Unfortunately most spacecraft loads are more demanding than indicated in figure 1(b). Most loads require regulated power (i.e., constant voltage, constant current, constant power, or some stipulated variation of these quantities). In addition, the output of solar cells is affected by temperature, light intensity, radiation degradation, etc. Thus, the requirement for a conditioning network.

The conditioning network for this investigation is a voltage regulator. Although this concept is applicable to a variety of voltage levels, the one selected for this investigation was 755 volts. The same concept may be used for current regulation as well. The concept evaluated has been given the name integral power conditioning because the voltage is controlled by controlling the number of cells on the array that deliver power



(a) Current-voltage characteristic of 1- by 2-centimeter silicon solar cell.



(b) MxN solar cell matrix.

Figure 1. - Characteristic solar cell power sources.

to the load. In developing the integral power conditioning concept, it was assumed that a digital computer would be on the spacecraft and would provide the logic for control of the system. Such a logic system, however, is not a necessary part of the integral power conditioning as will be noted later.

The requirements for the conditioning network are as follows:

(1) High circuit reliability.

(2) Ability to switch power to the load when required.

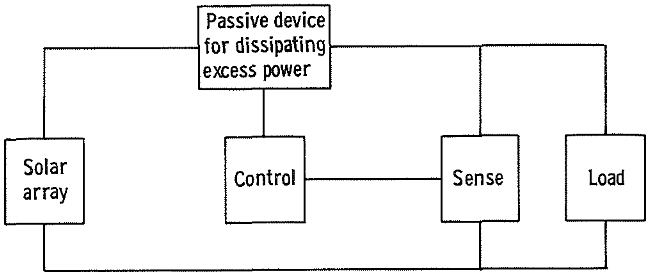
(3) Precise current or voltage regulation.

(4) Isolation of high-voltage power from the low-voltage control logic of the computer.

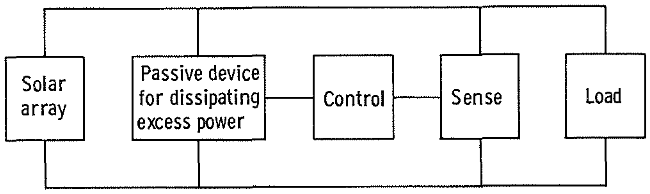
(5) Acceptable control logic in a digital form.

(6) Ability to perform the conditioning integral with the solar array.

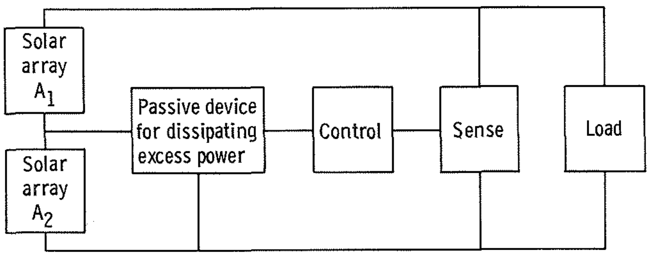
Conventional regulating concepts are the series regulator, the shunt regulator, and the partial shunt regulator. The schematic of each of the above mentioned regulators is shown in figure 2. The main disadvantage of the first two of these regulators is that they require large power dissipation elements. This can best be seen by examining



(a) Series regulator.

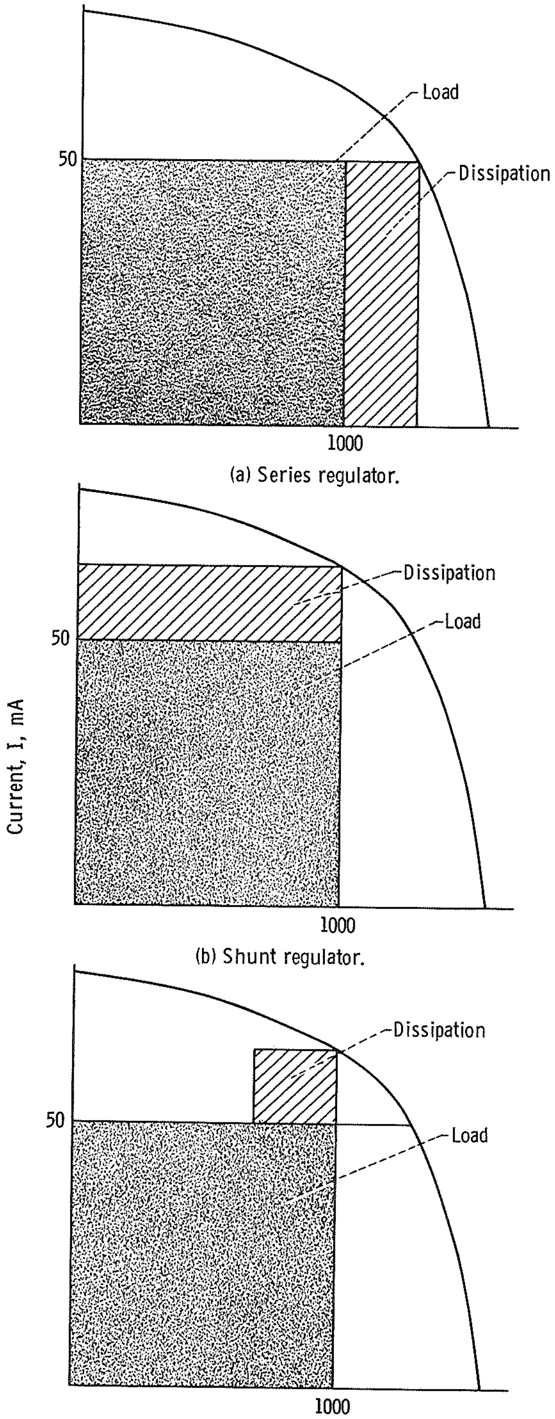


(b) Shunt regulator.



(c) Partial shunt regulator.

Figure 2. - Conventional regulator systems.



(a) Series regulator.

(b) Shunt regulator.

(c) Partial shunt regulator.

Figure 3. - Power dissipation in conventional regulator systems.

the regulation situation for an example load requiring a constant 1000-volt dc source of power at a nominal current value of 50 milliampere. Figures 3(a) and (b) show the power dissipation curves for the series and shunt conventional regulator systems. The current-voltage characteristic of the solar array required to supply the load and the amount of power which must be dissipated by the passive element of the voltage regulator configurations (shown in fig. 2) is a large percentage of the total solar array power output. The partial shunt regulator has considerably lower power dissipation as shown in figure 3(c). The digital regulator described next takes advantage of this approach to lowering power dissipation.

Sufficient power to the load with an allowance for power variation of solar cells can be obtained by series connecting solar cells for voltage and parallel connecting solar cells for current. The design of this digital regulator is based on a weighted binary number system. The solar cells in the series string are grouped into voltage increments (binary submodules) that correspond to the weighted binary system, that is, $2^0, 2^1, \ldots, 2^n$. Each weighted voltage increment (binary submodule) is provided with a shorting switch. When the switch is open, the submodule voltage and power are part of the series string. When the switch is closed, the submodule voltage and power are not part of the series string. A schematic diagram of the digital system is shown in figure 4. The output of each binary submodule can exist in either the on state (voltage added to the series string) or in the off state (voltage not added to the series string). The on state and the off state correspond in the logic system to a one-level or a zero-level condition,

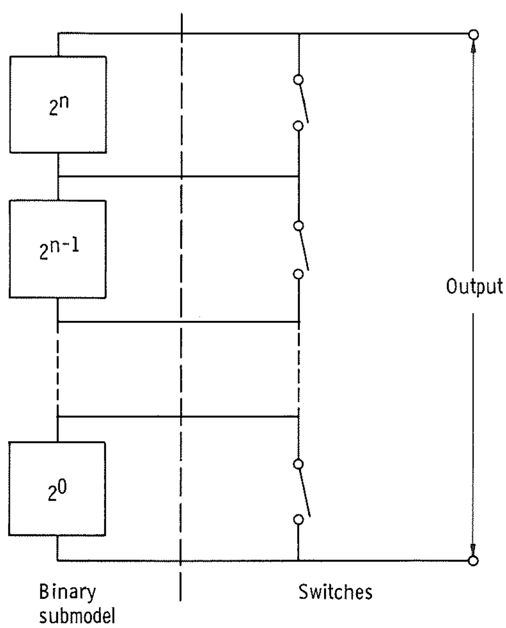
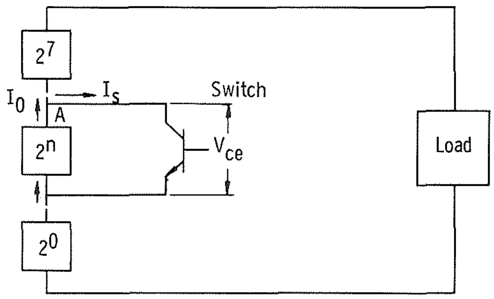


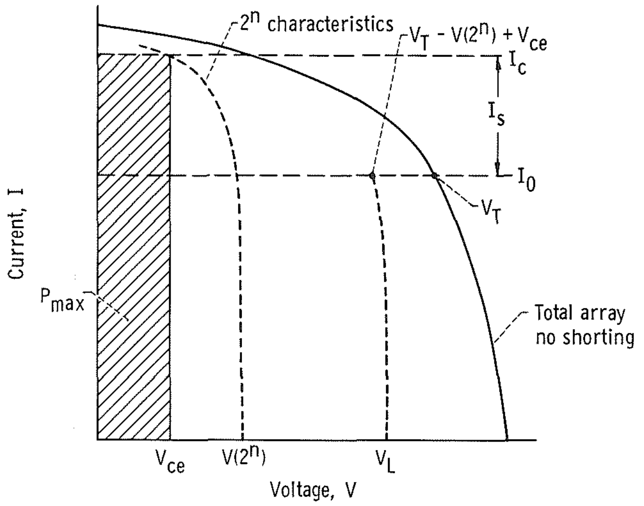
Figure 4. - Binary subsections of regulated solar array section.

respectively. Using this technique, the power of the solar array can be conditioned to the power requirements of a load by setting the logic levels of each of the (2^n) submodules. Power is dissipated within the shorting switch (neglecting leakage currents) only when the binary submodule is shorted. The power dissipated by the switch is dependent on the load configuration. The worst-case power dissipation within the switch occurs when the switch is closed and the load current is near zero. Then essentially full short circuit current of the solar cell flows through the shorting switch. Figure 5 shows this power dissipation characteristic of the shorting switch. This power dissipation is less than 5 milliwatts for a typical switch shorting a submodule consisting of a string of 1- by 2-centimeter solar cells in series when under light load or no load conditions. For a single-string (1- by 2-cm solar cells) eight-bit digital regulator, therefore, the



Summing currents at point A

$I_s = I_c - I_0$
$I_s \approx I_{sc} - I_0$ for $V_{ce} \ll V_{oc}(2^n)$
$I_{s,max} \approx I_{sc}$
$P_{max} \approx I_{sc}V_{ce}$



(b) Current-voltage characteristics for Z^n cell block.

Figure 5. - Power dissipation of submodule switch.

maximum power dissipated would be 40 milliwatts when the eight switches are closed and there is no current to the load.

The digital concept also has the capability of satisfying the conditioning network requirements noted earlier. Power can be switched to a load when it is required. Voltage regultion to practically any precision desired is obtainable by selecting the proper voltage increment for the least significant binary bit. Computer control logic terminals can be programmed directly to supply the required control logic. Optoelectronic coupling (as will be described subsequently) can be used to isolate low voltage logic signals from the high voltage solar array. Preliminary studies indicate that a reliability of 0.999 can be achieved using present day state-of-the-art technology. Through the use of microcircuit technology the complete regulator control circuitry could be placed on a single chip, and also, the low-power dissipation within the switch makes integration of the entire regulator (control circuitry and switches) on an array substrate possible.

In order to evaluate the performance of such a digital system one was built in breadboard form and tested. The following two sections describe the digital system and the experimental evaluation of the system.

DESCRIPTION OF EXPERIMENT

The concept of digital regulation on a high voltage solar array was experimentally investigated using a 755 volt, 50 millampere test array. A block diagram of the entire

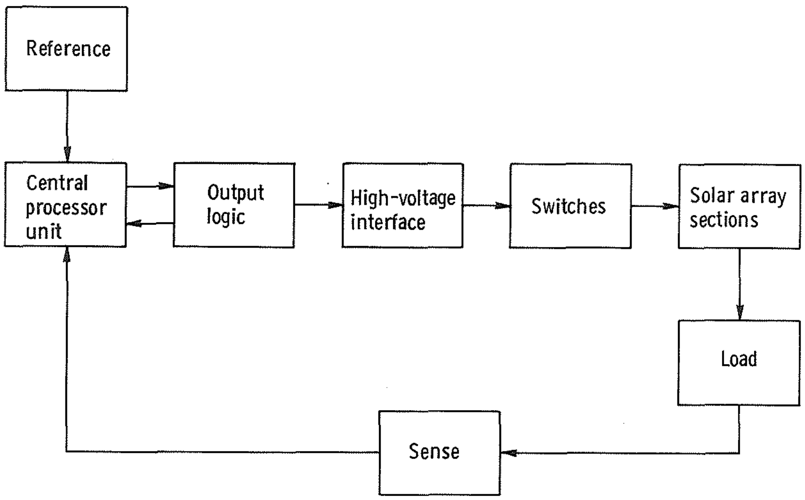


Figure 6. - Closed-loop digital regulator system.

system is shown in figure 6. The three major design aspects of the experiment are

(1) Binary submodule switching system

(2) Control logic circuitry

(3) High voltage interface

Binary Switching of High Voltage Solar Array

The test array was divided into two sections, a 500-volt unregulated section and a 255-volt regulated section. The binary submodule switching system was incorporated on the 255-volt section of the array. The 255-volt regulated section of the solar array module was tapped at voltage levels equivalent to the binary weighted system (i.e., 2^0, 2^1, . . ., 2^7). A variable voltage from 0 to 255 volts in 1-volt increments is obtainable with this binary voltage tap configuration. The unregulated 500-volt solar array section was placed in series with the 255-volt regulated solar array section for a total array output capability of 755 volts at 50 milliamperes. Thus, 34 percent of the total 755-volt array was controllable by shorting out binary subsections of the 255-volt solar array section. Regulation of 0.175 percent was obtained with this arrangement. Figure 7 shows the test configuration. Such a test configuration can be replicated in parallel to obtain greater current output. However, the test configuration shown in figure 7 represented the maximum capabilities for experimentation in terms of available solar cells at the time the investigation was conducted.

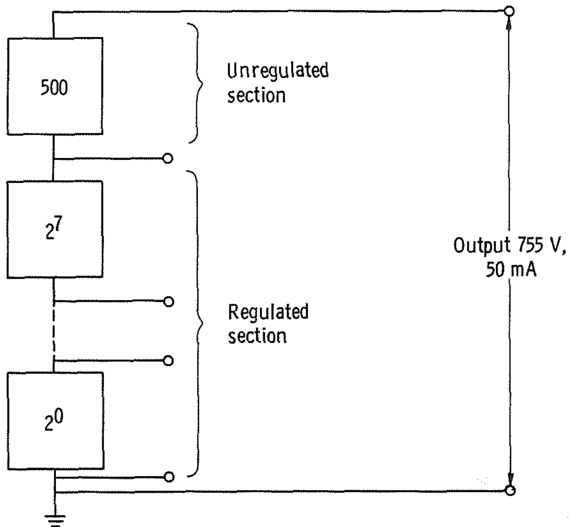
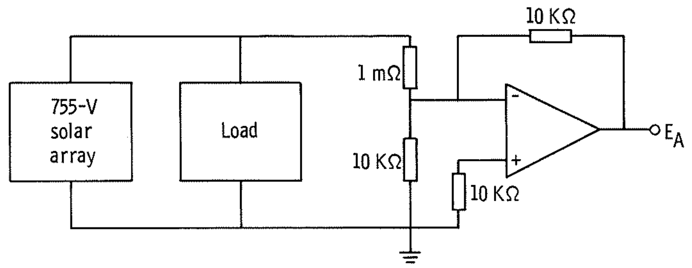


Figure 7. - Layout of high-voltage solar array sections.

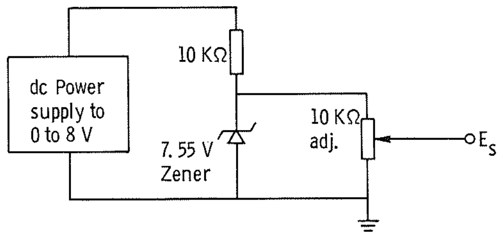
Control Logic Circuits

The control logic circuits for the 255-volt section of the array will be discussed as four subtopics. They are the solar array output sensing network, the central processor, the processor output logic, and the drive circuitry.

Input-output sensing. - The schematics showing how the two analog inputs are generated, the solar array reference voltage and the standard reference voltage are shown in figure 8. The output voltage of the solar array is measured across 100:1 re-



(a) Solar array reference voltage sense network.



(b) Standard reference supply.

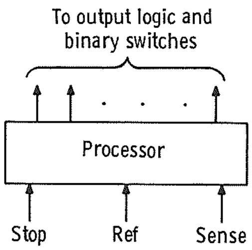
Figure 8. - Analog inputs to central processor unit.

sistive divider network. (See fig. 8(a).) The input to the divider network is 1 megohm. Therefore, there is no loading of the solar array by the sensing network. A unity gain operational amplifier is used to buffer this sensed output voltage from the subsequent circuitry. The output of the operational amplifier is 0 to 7.55 volts which is proportional to the total solar array output (0 to 755 V dc) and will be referred to as the solar array reference voltage E_A. The standard reference voltage E_S (see fig. 8(b)) is continuously adjustable from 5 to 8 volts. This corresponds to a solar array output variation of 500 to 755 volts dc. The solar array reference voltage E_A is compared with the standard reference E_S in the central processor unit. When a null voltage ($E_A - E_S = 0$) is across the analog inputs of the central processor unit the desired set point output voltage of the solar array is obtained.

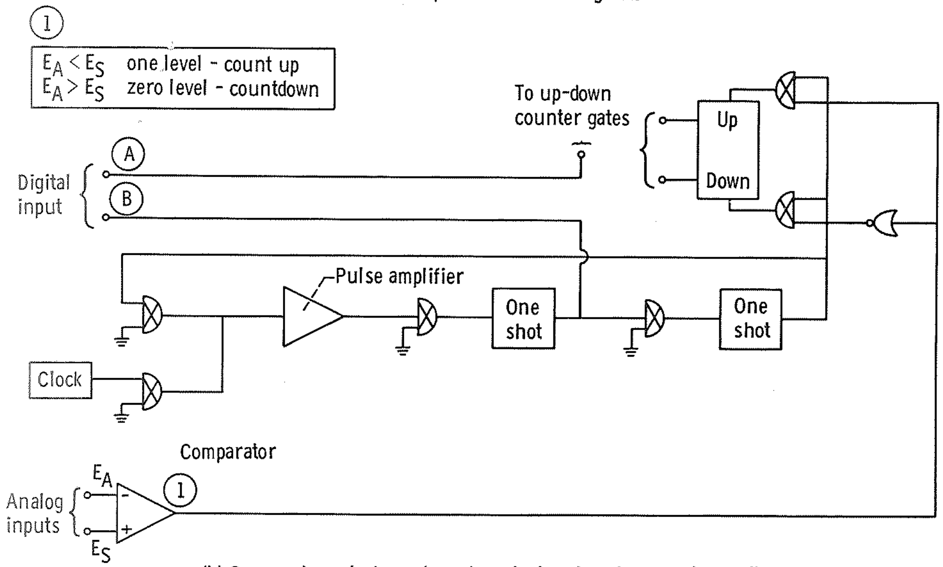
Central processor unit. - The intelligence of the digital regulator is performed by the central processor unit. In an actual spacecraft application this function would be achieved using an on-board digital computer. For this experiment, the central processor unit is a binary coded decimal up-down counter, a high speed comparator, and a digital clock. The processing unit accepts two analog inputs. A block diagram of the central processor unit is shown in figure 9(a). The processor determines whether the array voltage is greater than or less than the reference voltage. When the difference between array voltage and reference voltage exceeds a certain deadband, the processor is activated to seek a null voltage.

The null voltage is obtained in the following manner. Figure 9(b) shows the high-speed comparator, the digital clock, and the up-down counter input logic gates. The two reference voltages E_A and E_S (see fig. 9(b)) are inputs to the negative and positive inputs of a high-speed comparator. The output of the comparator is either a logic one level or a logic zero level. An E_A is greater than E_S results in a zero level on the comparator output. The input gate of the up-down counter which sets the counter in either an up count mode or a down count mode represented as a one level or a zero level, respectively, senses the output of the high-speed comparator. If a one level is present at the input gate the counter is advanced at a predetermined clock rate bit by bit until the desired switch combination is achieved on the array. The reverse situation occurs when a zero level input is present at the up-down counter input gate.

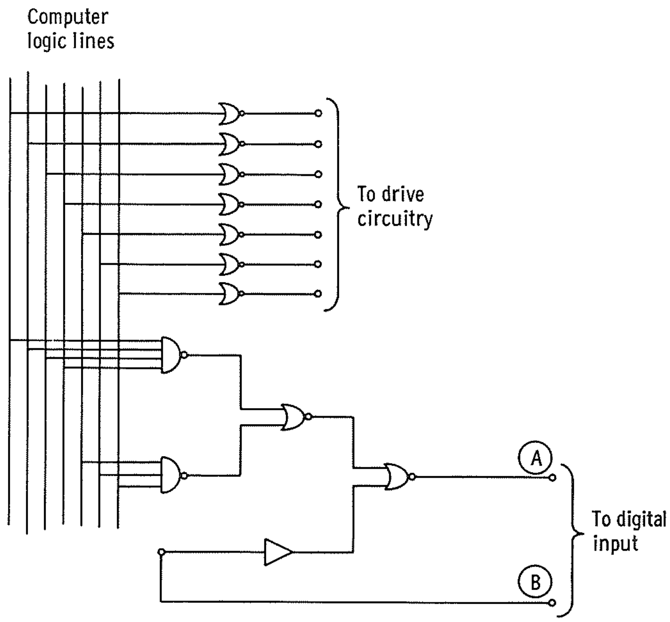
The third input to the processor is the digital input. This input in obtained from the output logic of the processor unit as shown in figure 9(c). By design the output voltage of the array was controlled within 1 volt of the desired voltage output. Therefore, the seven output bits (2^1 - 2^7) of the central processing unit are sensed to determine when they are on. The output bits are sensed through the use of a four-input NAND gate and a three-input NAND gate. These two gates are NORED together and along with the inverted digital clock pulse are sensed by the NOR gate of the shutdown logic. When the control capabilities of the 255-volt section are exceeded (i.e., when all switches are open and the load current demand exceeds array capabilities) the clock input gate of the up-down counter stops the clock pulses from reaching the clocked gate of the counter. Therefore, the counter is halted and the processor does not continue to search for a null input from the analog inputs. The output logic bits are coupled to the binary switch drive circuitry through NOR gates. These buffer the output logic from the drive circuitry.



(a) Central processor block diagram.



(b) Comparator, clock, and up-down logic gates of processing unit.



(c) Shutdown logic.

Figure 9. - Central processing unit.

High Voltage Interface

The processing unit operates at low-voltage (0 to 3 V), but its logic output signals must operate switches on the array that can be at high voltage. It is desirable to isolate the high voltage on the array from the low-voltage control logic of the processing unit. This is accomplished by using optoelectronic coupling between the output logic gates of the processor and the switch device circuitry on the array. In this experiment an optoelectronic device capable of withstanding 500 volts dc was used to provide isolation between the high voltage on the array and the low-voltage control logic. Figure 10 shows a simple binary switch section with optoelectronic coupling.

A detailed drawing of the complete closed-loop control system is shown in figure 11. The experimental results and performance of the system are discussed in the next section.

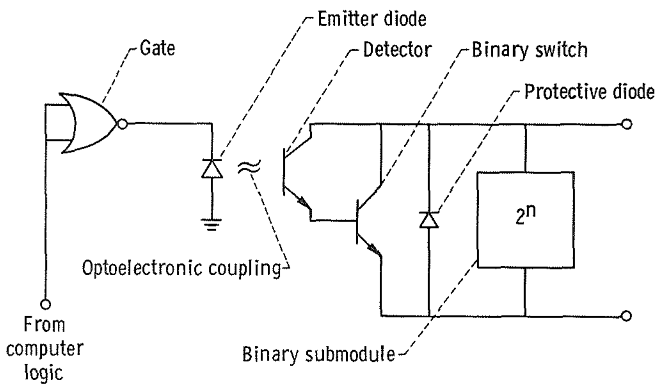


Figure 10. - Single binary subsection and switch drive circuitry.

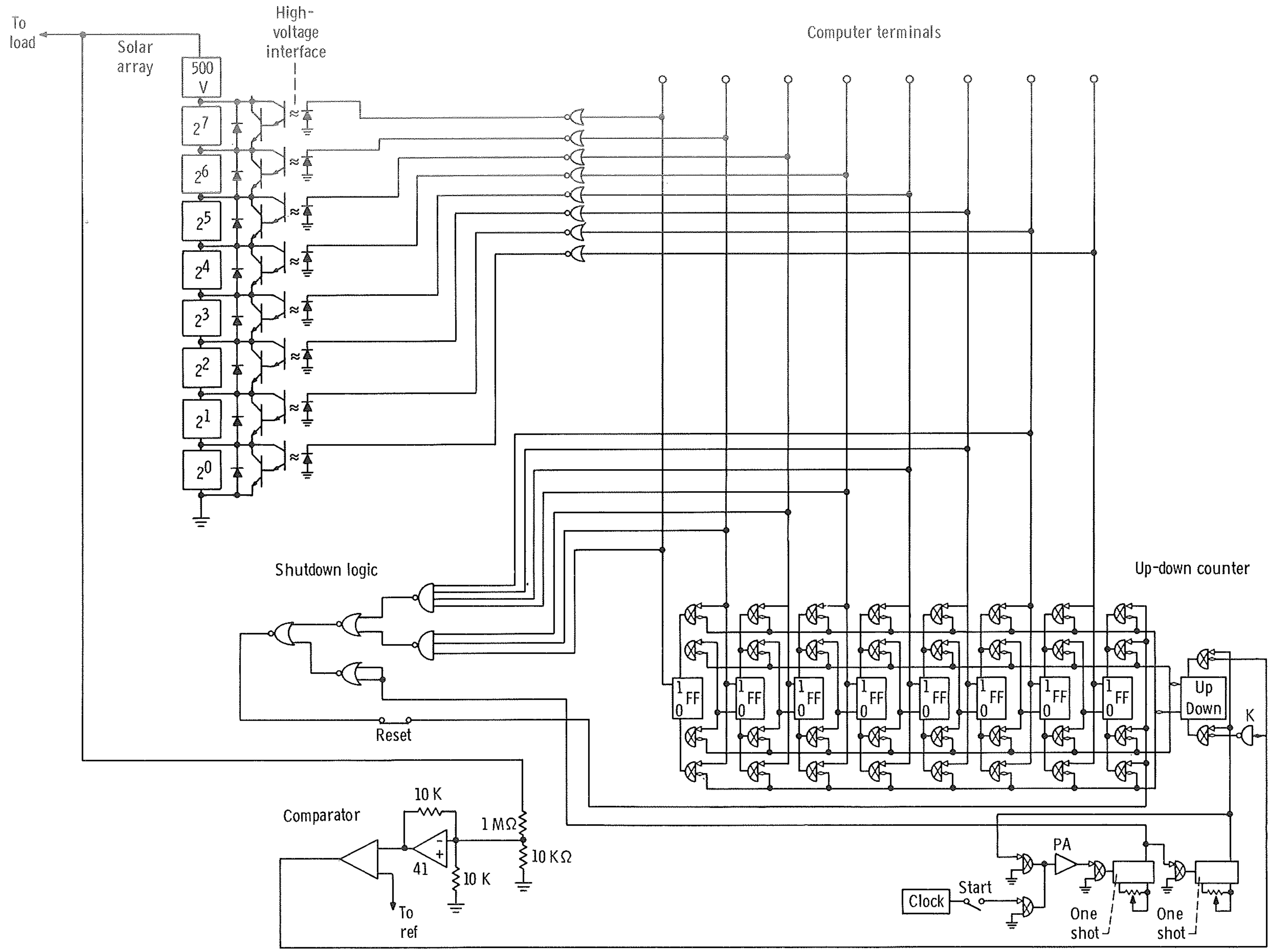


Figure 11. - Digital regulated high-voltage solar array module.

EXPERIMENTAL RESULTS AND DISCUSSION

The operation of the digital regulated solar array module is affected by both the physical operating condition and the actual circuitry which controls the operation of the regulator.

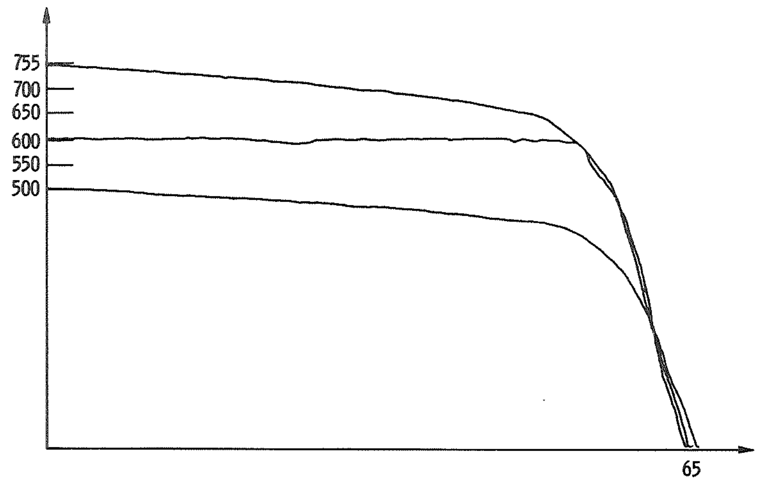
Two physical operating conditions that affect the solar array regulator performance are (1) the temperature of the solar cells and the uniformity of the temperature from cell to cell, and (2) the illumination intensity and its uniformity. Both conditions are critical to the output of the solar cells. In the experimental setup, the array was illuminated by a 15 000-watt light bank and also by placing the array in direct sunlight. Light bank illumination was uniform to ±10 percent at a light intensity capable of producing an output from the solar cells equivalent to 140 milliwatts per square centimeter AMO solar intensity. The light bank produced temperature variations of approximately 5.5° K (10° F) over the solar array. Another characteristic of the light bank was that a large portion of the output was in the infrared region of the spectrum, thus producing operating array temperatures of $330.4 \pm 5.5^{\circ}$ K ($135^{\circ} \pm 10^{\circ}$ F). These temperature variations and light intensity variations experienced with the light bank were not present under sunlight exposure.

Figure 12 shows the regulation characteristics of the system at 610 volts under both illumination conditions. These results demonstrate that the ability to regulate was not affected by the illumination intensity variation and temperature variations experienced with the light bank.

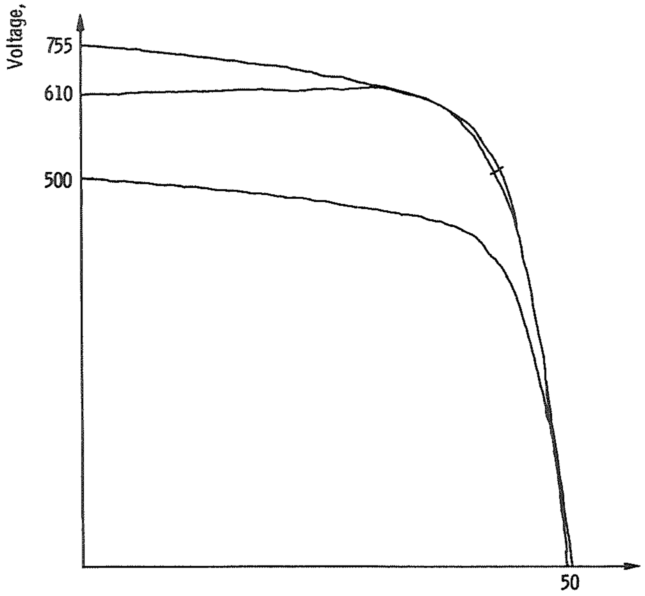
Four conditions that affect the output characteristics of the binary elements are (1) intrinsic solar cell characteristics, (2) ambient operating temperature of the cells, (3) illumination of the cells, and (4) intrinsic characteristics of switches. Even though these conditions were present, a voltage regulation (from 500 to 755 volts in steps of 50 volts over the full-current capabilities for that particular voltage range) of 0.175 percent was achieved. The operational characteristics of the high voltage solar array module are shown in figure 13.

One significant feature of this regulator system is the very low power dissipated in the switch circuits of the regulator system under full regulation conditions. Power dissipation within the binary switches was 40 milliwatts. The control logic and high voltage interface power dissipation was 410 milliwatts. Therefore, no special provisions were required on the solar array to dissipate the heat (450 mW) generated by the regulator system.

The high-voltage interface between the array and the logic was bridged using the TIXL103 optically coupled isolator which has a 500-volt isolation rating. This rated isolation is peculiar, of course, to this particular device. Higher-volt isolation can be obtained easily using the light emitting diode and photo detector as coupled devices.



(a) Regulation at 610 volts of HUSA module under artificial illumination.



(b) Regulation of HUSA module under direct sunlight illumination.

Figure 12. - Regulation characteristics of HSA module.

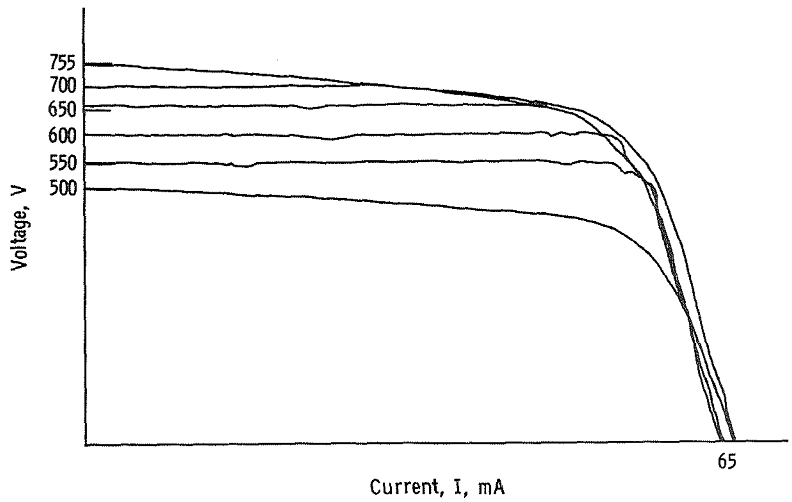


Figure 13. - Regulation characteristics of HUSA module over entire range of regulating capabilities.

In general, the system performance is compatible both with a digital control system integral with the solar array or with an external digital computer system. A high-voltage solar array regulation scheme can more easily meet power requirements than conventional power conditioning. Overall system efficiency for a high voltage solar array is higher than conventional power conditioning.

SUMMARY OF RESULTS

The results of a preliminary experimental investigation of digital solar array regulation electronics were as follows:

1. The design goal for voltage regulation with the digital controlled high voltage solar array regulator was 0.1 percent for a 1000-volt solar array. The voltage regulation obtained for the digital regulated 755-volt solar array module was 0.175 percent for a minimum bit size of 1 volt. This is equivalent to a regulation of 0.132 percent on a 1000-volt solar array module. These results demonstrate that the 0.1 percent goal can be easily achieved by reducing the minimum bit size and by employing more sophisticated experimental facilities.
2. No major switching transients were observed.
3. The worst case power dissipation of the switching regulator is 450 milliwatt.
4. Regulation was provided over the full current capability of the solar array.
5. The ability to regulate was not affected by the moderate nonuniform lighting of

the solar array and solar array temperature variations present in the experiment.

6. The binary submodules need not be exact weighted binary bits to achieve the desired regulation.

7. Switching of the binary submodules can be achieved by driving a Darlington configured binary submodule switch directly from a light emitting diode.

8. Power dissipation within the binary submodule switch was approximately 50 milliwatts. Therefore, no special provisions would be required on a solar array to dissipate the heat generated by the binary submodule switch in the on state.

9. The gain achievable with the diode/transistor coupling approach would permit the light emitting diodes to be driven directly from computer output terminals.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, March 31, 1971,
120-26.

REFERENCES

1. Springgate, W. F.; and Oman, Henry: High Voltage Solar Array Study. Rep. D2-121734-1, Boeing Co. (NASA CR-72674), 1969.

2. Knauer, W. Bayless, J. R.; Todd, G. T.; and Ward, J. W.: High Voltage Solar Array Study. Hughes Research Labs. (NASA CR-72675), May 1970.

NASA-Langley, 1971 —— 10 E-6215

"The aeronautical and space activities of the United States shall be conducted so as to contribute . . . to the expansion of human knowledge of phenomena in the atmosphere and space. The Administration shall provide for the widest practicable and appropriate dissemination of information concerning its activities and the results thereof."

—NATIONAL AERONAUTICS AND SPACE ACT OF 1958

NASA SCIENTIFIC AND TECHNICAL PUBLICATIONS

TECHNICAL REPORTS: Scientific and technical information considered important, complete, and a lasting contribution to existing knowledge.

TECHNICAL NOTES: Information less broad in scope but nevertheless of importance as a contribution to existing knowledge.

TECHNICAL MEMORANDUMS: Information receiving limited distribution because of preliminary data, security classification, or other reasons.

CONTRACTOR REPORTS: Scientific and technical information generated under a NASA contract or grant and considered an important contribution to existing knowledge.

TECHNICAL TRANSLATIONS: Information published in a foreign language considered to merit NASA distribution in English.

SPECIAL PUBLICATIONS: Information derived from or of value to NASA activities. Publications include conference proceedings, monographs, data compilations, handbooks, sourcebooks, and special bibliographies.

TECHNOLOGY UTILIZATION PUBLICATIONS: Information on technology used by NASA that may be of particular interest in commercial and other non-aerospace applications. Publications include Tech Briefs, Technology Utilization Reports and Technology Surveys.

Details on the availability of these publications may be obtained from:

SCIENTIFIC AND TECHNICAL INFORMATION OFFICE

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Washington, D.C. 20546