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JUNCTION TRANSISTOR SYNCHRONOUS RECTIFICATION

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GSFC
GODDARD SPACE FLIGHT CENTER
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ABSTRACT

Higher efficiency and reliability are needed in the rectification used to produce low output voltages. To this end, the application of driven synchronous rectifier circuits is investigated. One reliability problem of such circuits, the "double-on" resulting from storage time, is illustrated for low output voltages obtained from rectification of the square-wave outputs of low input voltage converters. A comparison of the rectification efficiency and reliability of driven transistor synchronous rectifiers with that of barrier diodes indicates that the choice of rectifiers in low output voltage applications is dependent on both the source and output voltage levels of the application.

JUNCTION TRANSISTOR SYNCHRONOUS RECTIFICATION

INTRODUCTION

The use of Schottky-barrier low-resistivity metal-to-silicon junction techniques as well as the use of transistors driven as synchronous rectifiers have enabled substantial reduction of rectification losses (1). Industry efforts to improve low output voltage rectification efficiency have focused principally on power-diode development.

For the low output voltage requirements contemplated for new integrated-circuit applications, rectification efficiency and reliability improvement is needed. To this end, circuit approaches that use driven transistor synchronous rectification were investigated, and such devices were developed at Goddard Space Flight Center (GSFC). This report presents the major results obtained from the development and utilization of driven transistor synchronous rectification of square-wave inverter outputs generated by low input/low output voltage converters.

BACKGROUND

Diode Rectification

From Figure 1, an approximation of the diode-rectification efficiency η is

$$\eta = \frac{V_O}{V_{IN}} = \frac{1}{1 + V_D/V_O}, \qquad (1)$$

neglecting other losses. For low output voltages, V_D is the significant efficiency-reducing factor: As V_D is minimized, η is maximized.

Synchronous Rectification

Figure 2 illustrates full-wave, transistor synchronous rectification stages which are voltage driven from the output transformer of a dc-to-square-wave-ac inverter (2, 3). The long storage time inherent in the low-saturation-resistance transistors of the synchronous rectifiers produce the familiar "double-on" condition which can result in abnormally high inverter switchover current transients as illustrated in Figure 3. The double-on condition reduces both reliability and efficiency. In this circuit arrangement, because there is no crossover speedup forcing provision, the rise and fall times are slow, which results in reduced efficiency and increased output ripple. Also, the diode voltage drop varies with load, which causes poor regulation.

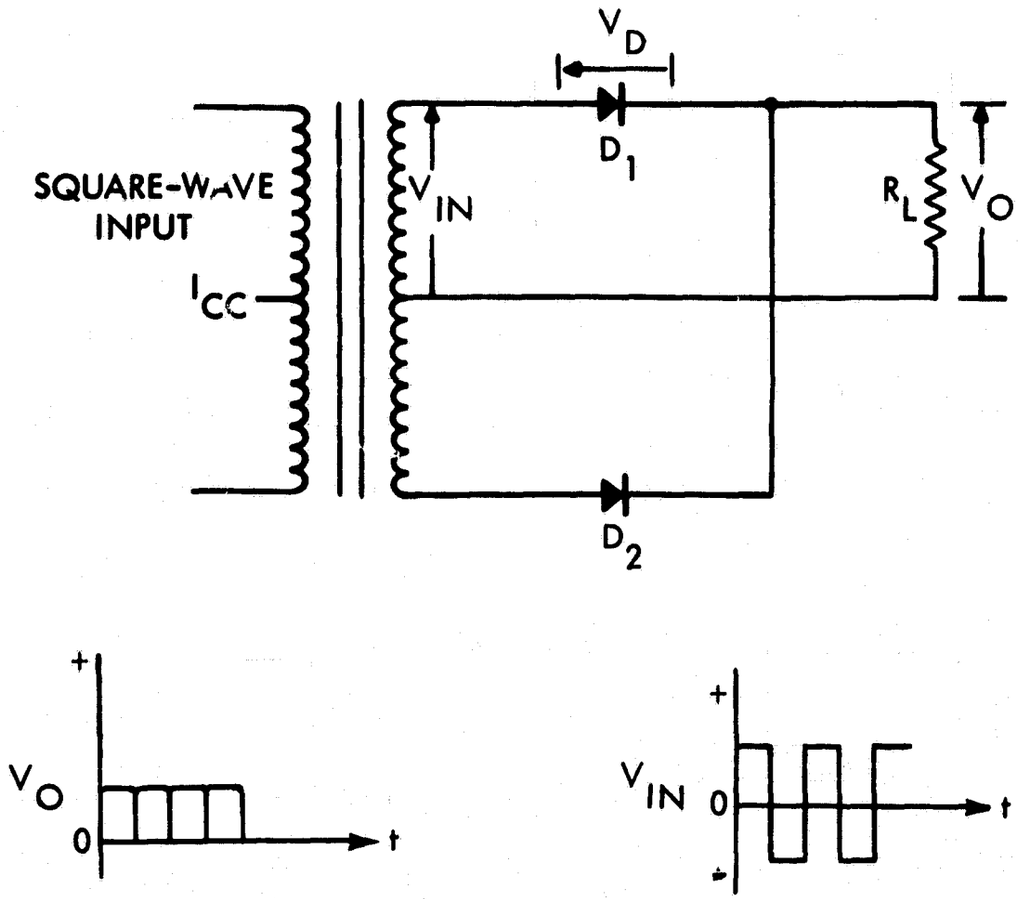
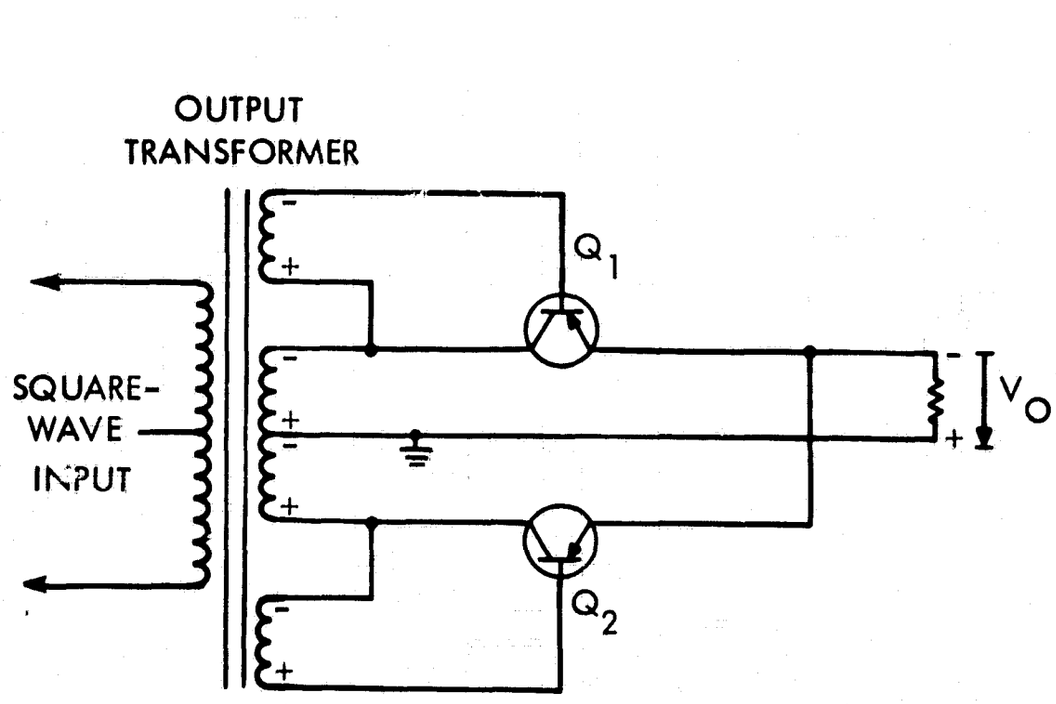


Figure 1. Full-wave rectification with diodes.

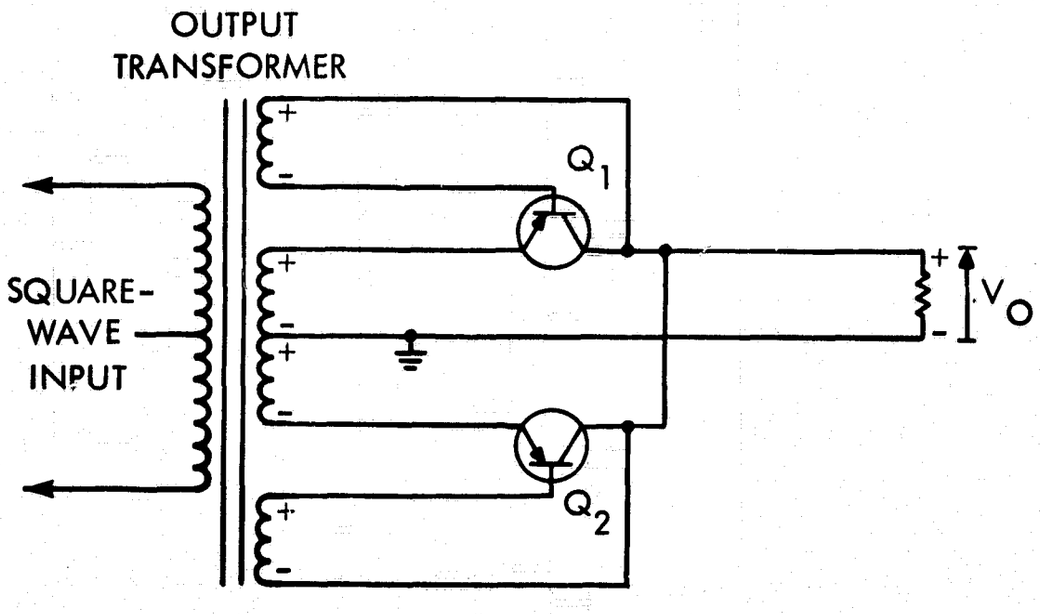
Recent Developments

The development at GSFC of an inverter with the means for base-current shaping for sweeping charge carriers from the base region (4, 5) has enabled the development and application of an effective base drive for transistor synchronous rectification. This drive technique resolves several efficiency/reliability problem areas, particularly the double-on overlap, thereby making the transistor synchronous rectification approach reliable for low output voltage rectification requirements where high efficiency and reliability are needed.

Figure 4 is a schematic of a dc-to-dc converter developed at GSFC (4, 5). The positive current-feedback drive circuit provides a load-related inverter drive throughout the major portion of the inverter cycle. The negative voltage feedback V_{N_5} saturates the saturable reactor (SR) and recycles the inverter. The uniqueness of this inverter circuit lies in the inclusion of the inductor L in the frequency-determining loop. The complex action resulting from including L in the loop is analyzed in References (4) and (5). Briefly,

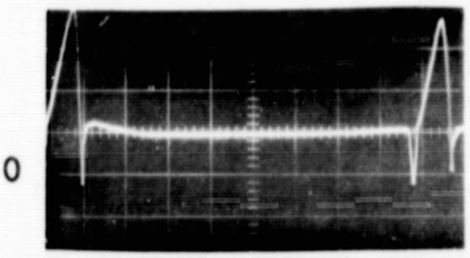


(a) NEGATIVE OUTPUT



(b) POSITIVE OUTPUT

Figure 2. Full-wave driven transistor synchronous rectification. (Polarities are shown for half cycle when Q_1 is conducting; for other half cycle, polarities reverse, and Q_2 conducts.)



2N1100 DRIVEN TRANSISTOR RECTIFIER

Figure 3. Inverter input current transient resulting from "double-on" rectifier condition (10-A/cm vertical and 100-μs/cm horizontal displacement).

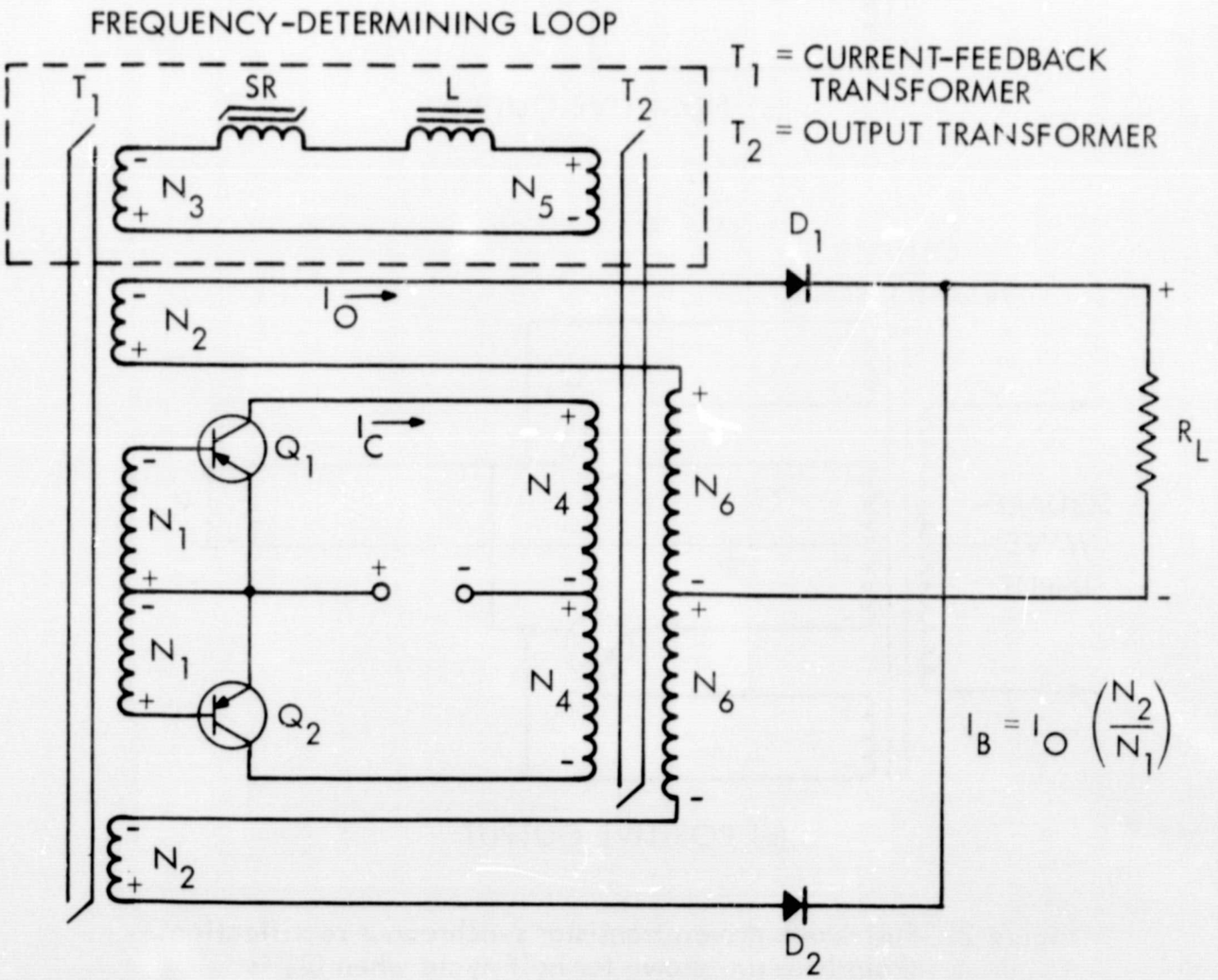


Figure 4. Inverter with means for base-current shaping for sweeping charge carriers from base region (5). (Polarities are shown for half cycle when Q_1 and D_1 are conducting; for other half cycle, polarities reverse, and Q_2 and D_2 conduct.)

the load-related shaping of the base current by the inverter transistors Q_1 and Q_2 is generated by current sharing with the frequency-determining loop, which is also coupled to the base-driving, current-feedback transformer. This shaping results in an efficient and reliable inverter switchover with the following unique characteristics:

1. The shaping results in the separation and control of the base-current reduction (switching-off transistor) and base-current overdrive (switching-on transistor) to separate time intervals. The initiation of switchover occurs only after stored base charges are minimized and conditions for switching are optimized. Fall time is rapid.

2. The base current of the switching-off transistor is reduced in a controlled manner, and as a function of load prior to switch-over initiation, to a minimal value at the instant of switchover. There is a minimal storage time existent at switchover which reduces the storage-time-overlap (double-on) problem of the push-pull inverters.

3. An overdrive occurs after switchover, resulting in a rapid rise time for the switching-on transistor. The overdrive current of the switching-on transistor is a function of load current (the peak value is twice the normal load-related drive).

Overall inverter-circuit reliability is enhanced by the use of load-side current feedback. This provides the efficiency advantages of load-related current feedback without the catastrophic possibilities of output transformer saturation.

GENERATION/UTILIZATION OF THE NEW TRANSISTOR SYNCHRONOUS RECTIFIER BASE DRIVE

In Figure 4, the square-wave-ac-to-dc rectification employed diode rectifiers D_1 and D_2. The replacement of the diode rectifiers with transistor synchronous rectifiers that are base driven by the inverter current-feedback transformer T_1 is illustrated in Figure 5. The rectifier drive windings N_7 are placed on the inverter current-feedback transformer rather than on the output transformer (see Figure 2) as was done previously. Using the voltages induced in the N_7 windings for driving the transistor synchronous rectifiers has several advantages.

In Figure 5, note that the inverter-transistor (Q_1 or Q_2) emitter-base voltage V_{EB} is determined by the load-side current-feedback drive. The N_7 winding voltage used to drive the transistor rectifier is related to the V_{EB} -established N_1 winding voltage by the turns ratio:

$$V_{N_7} = V_{N_1}\left(\frac{N_7}{N_1}\right) \qquad (2)$$

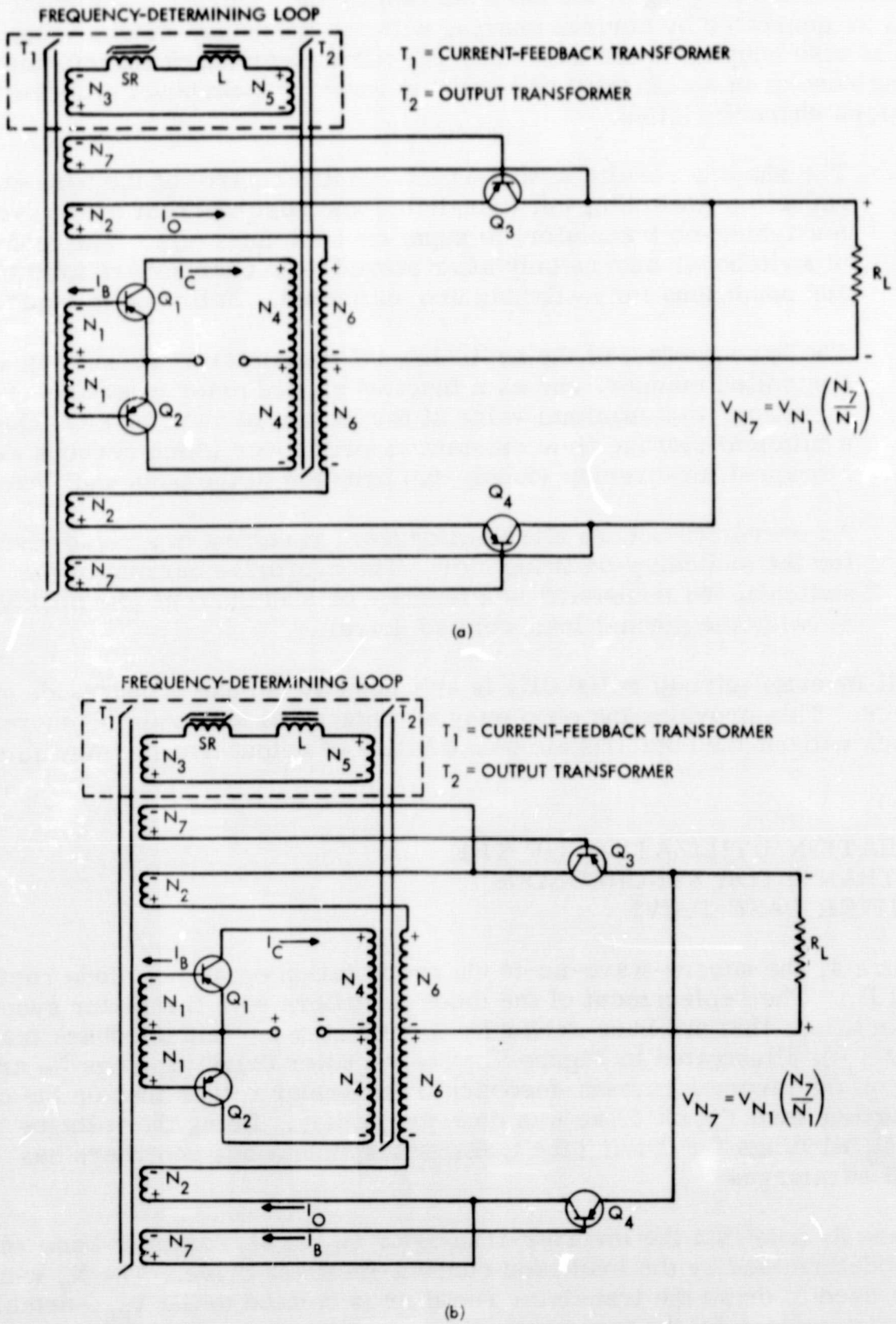


Figure 5. New base drive for driven transistor rectification. [Part (a): Polarities are shown for half cycle when Q_1 and Q_3 are conducting; for other half cycle, polarities reverse, and Q_2 and Q_4 conduct. Part (b): Polarities are shown for half cycle when Q_1 and Q_4 are conducting; for other half cycle, polarities reverse, and Q_2 and Q_3 conduct.]

From Eq. 2 it is seen that the synchronous rectifier base drive level can be nondissipatively adjusted by changing the turns ratio.

The synchronous rectifier drive voltage V_{N_7} is also related to the output load since V_{EB} is determined by load current feedback. This load-related rectifier drive voltage causes the rectifier drive to increase with increased load. Thus, an optimum rectifier load-to-base current ratio is maintained for static and dynamic load changes. This conserves rectifier drive power while reducing rectifier conduction losses.

A beginning and end of the inverter half-cycle shaping of the rectifier-base drive current is generated by the frequency-determining-loop action of the inverter (4, 5). The typical load-related overdrive (switching-on transistor rectifier) and drive reduction (switching-off transistor rectifier) are illustrated in Figure 6. This shaping of the transistor synchronous rectifier drive shortens the rectifier rise and fall times, and essentially eliminates the rectifier storage-time (double-on) problem and thus improves reliability and efficiency.

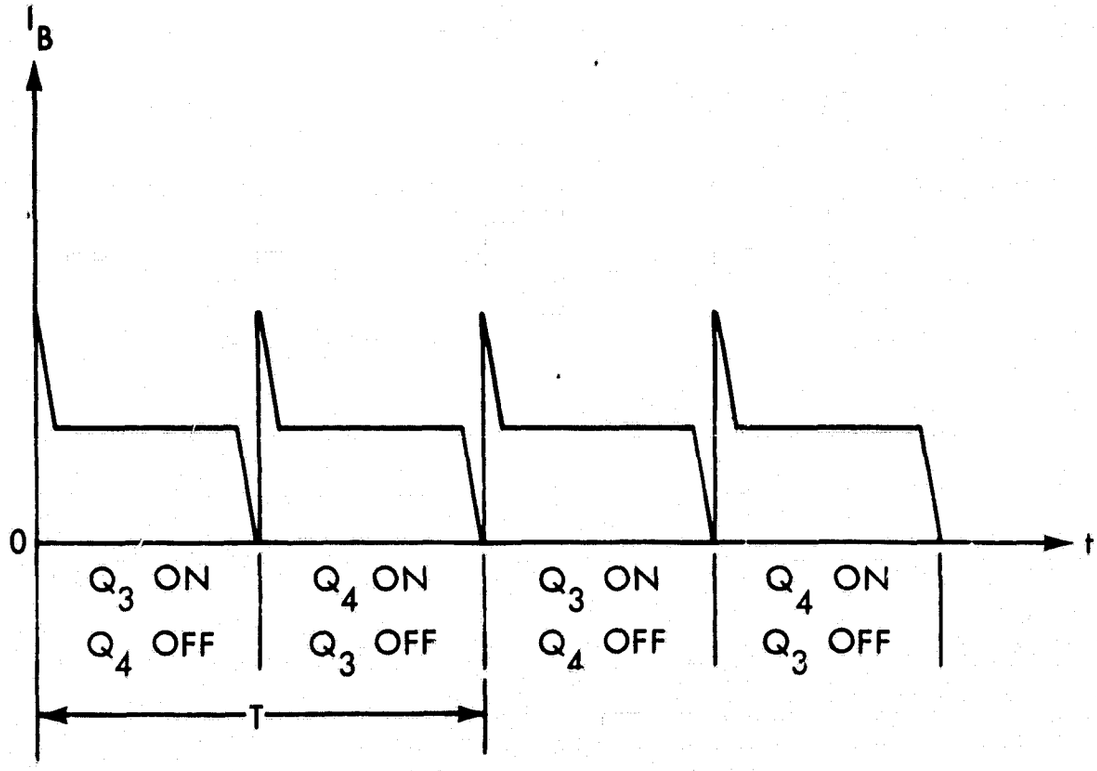


Figure 6. Load-related synchronous rectifier base current I_B (of Q_3 or Q_4).

Inverter-Transistor Base-Current and Transistor Synchronous Rectifier Base-Current Interrelations

Substitution of rectifier diodes for the transistor rectifiers (as shown in Figure 4) simplifies the situation; then, the inverter-transistor base current is

$$I_{B(INV)} = I_O \left(\frac{N_2}{N_1}\right) . \qquad (3)$$

The current feedback $I_{B(INV)}$ is both a function of and limited by the output load.

When the transistor rectifiers are substituted back into the circuit (Figure 5), the flow of the transistor synchronous rectifier base current $I_{B(RECT)}$ results in a reduction of the value of $I_{B(INV)}$ given in Eq. 3 because the total feedback current is both load determined and load limited. Since $I_{B(RECT)}$ subtracts from $I_{B(INV)}$, it is necessary to alter concurrently the N_2/N_1 ratio (Eq. 3) and the N_7/N_1 ratio (Eq. 2) to maintain the optimum I_C/I_B ratio of both the inverter and rectifier transistors. Adjusting N_2/N_1 increases the total feedback current to the value needed to supply the additional rectifier drive power and maintain the inverter drive power at its proper level. Adjusting N_7/N_1 sets the voltage transformation ratio so that the optimum rectifier I_C/I_B ratio is obtained. With proper N_2/N_1 and N_7/N_1 ratios, an optimum drive of the inverter and rectifier bases is maintained for both static and dynamic output-loading conditions. It is important to note that an improper design that gives insufficient inverter-base drive will result in failure of the circuit to start and run.

Cut-Off Condition of Driven Transistor Synchronous Rectifiers

As shown by the dashed lines in Figure 7, the cutoff transistor Q_2 operates in an inverted mode (the physical emitter becomes the electrical collector, and the physical collector becomes the electrical emitter), but Q_2 remains nonconducting because of the off-biasing polarity. Bright states (6), "A transistor, when used in the inverted connection, has a room-temperature leakage current at cut-off which is an order of magnitude lower than that of the normal connection." Thus, the driven synchronous rectifier can be operated hotter, thereby reducing thermal runaway problems. From Figure 7, it is also noted that a transistor with a reverse emitter-base voltage rating $V_{EB_{REV}}$ (min) $> V_O + V_{IN} + V_{DRIVE}$ is needed to avoid breakdown.

The use of base-driven transistor synchronous rectification for the higher voltage applications is limited by the emitter-base voltage requirement.

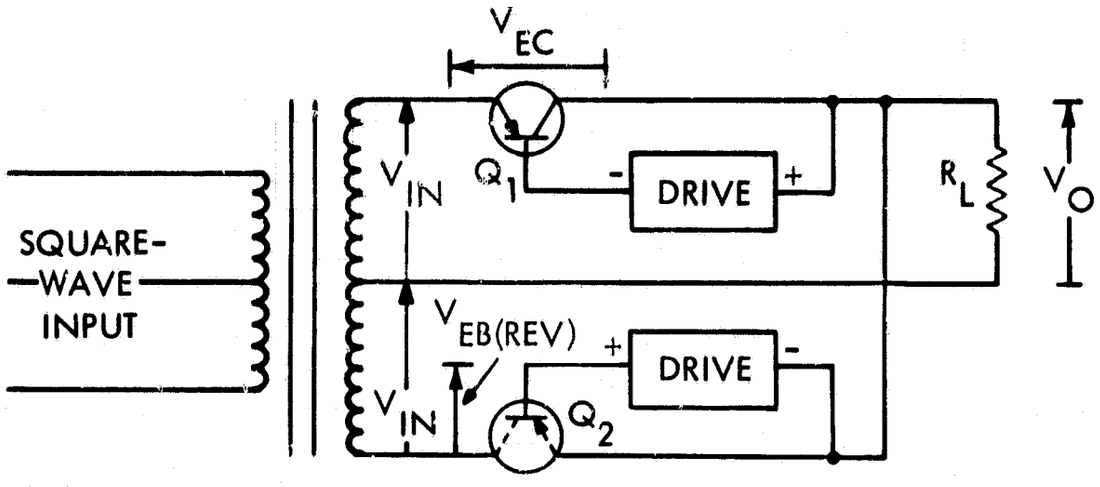


Figure 7. Inverted operation of the off transistor in driven transistor synchronous rectification.

A symmetrical transistor appears desirable for driven transistor synchronous rectifier applications. Increased storage time to achieve higher voltage ratings of such symmetrical transistors can be handled efficiently and reliably by the load-related drive-shaping technique.

TEST PROCEDURE AND RESULTS

A low input voltage inverter and driven synchronous rectifier low output voltage circuit, shown in Figure 8, was developed. The N_6 windings were wound on the output transformer T_2 to obtain a square-wave output of approximately 5 V peak. The N_7 windings for the synchronous rectifier base drive were wound on the current transformer T_1. The N_2/N_1 and N_7/N_1 ratios were adjusted for favorable drive conditions for the inverter and rectifier transistors. For each test, the rectified dc output was adjusted by varying the output load and inverter input voltage. The leakage losses of the cutoff transistor or diode were not included, as they were small enough to neglect. The test conditions were $I_0 = 5$ A and $V_0 \approx 5$ V for test 1, and $I_0 = 10$ A and $V_0 \approx 5$ V for test 2.

For each test, the power out P_0 and the synchronous rectifier collector-emitter dissipation P_{CE} were measured directly with a pulse power monitor (PPM).* The base-winding (N_7) power was calculated from voltage and current measurements. Some of the typical data obtained for the synchronous rectifier operation (with 2N2732 germanium transistors) are illustrated by Figures 9 through 14.

*Model PM-5003, Ohio Semitronics, Inc.

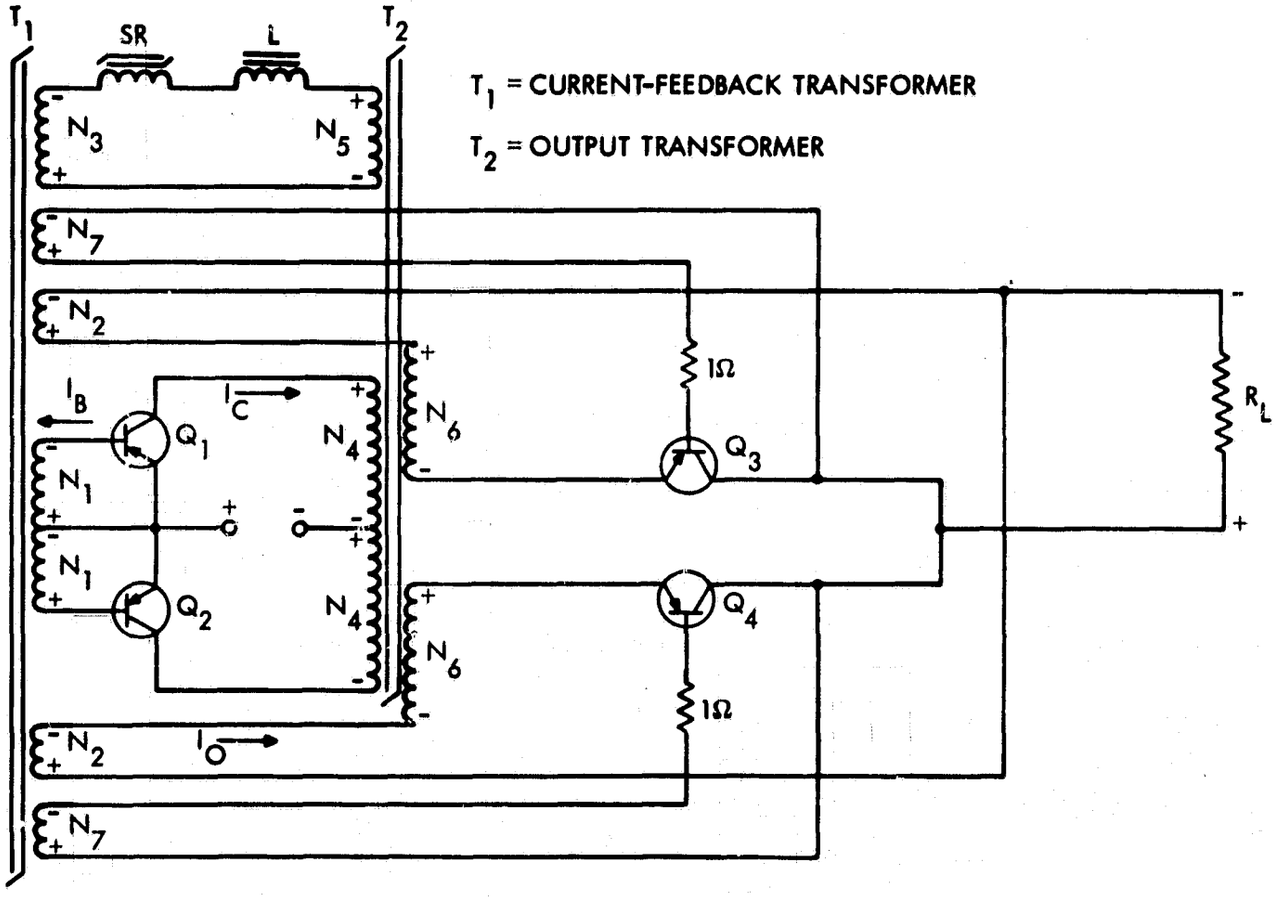


Figure 8. Circuit for transistor synchronous rectification efficiency measurements.

The synchronous rectifier rectification efficiency η was calculated from

$$\eta = \frac{P_O}{P_O + P_B + P_{CE}}, \tag{4}$$

where P_{CE} is the collector-emitter dissipation and P_O is the power out, both measured by the PPM, and P_B is the base-winding drive power (from voltage/current measurements). Table 1 shows the base-driven 2N2732 synchronous rectifier test results.

Table 1

Rectifier Test Results

Test	I_O (A)	P_O (W)	P_{CE} (W)	P_B (W)	η (%)
1	5	27.6	0.48	0.13	97.8
2	10	54.0	1.4	0.24	97.0

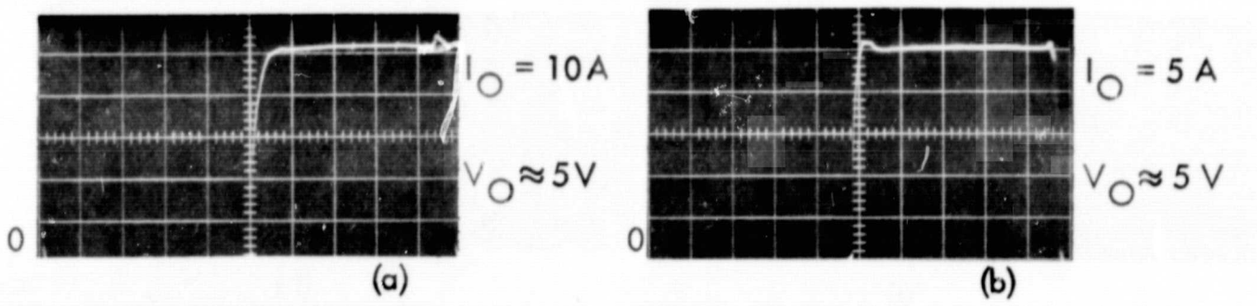


Figure 9. Conducting half-cycle input voltages (1-V/cm vertical and 0.1-ms/cm horizontal displacement).

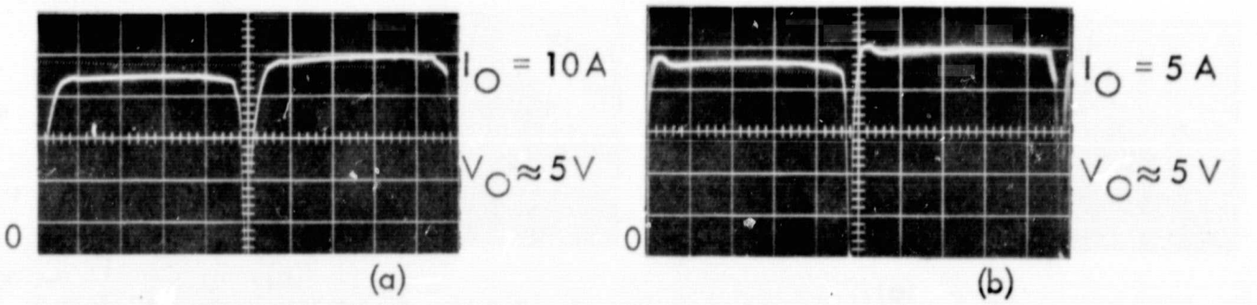


Figure 10. Rectified output voltages (1-V/cm vertical and 0.1-ms/cm horizontal displacement).

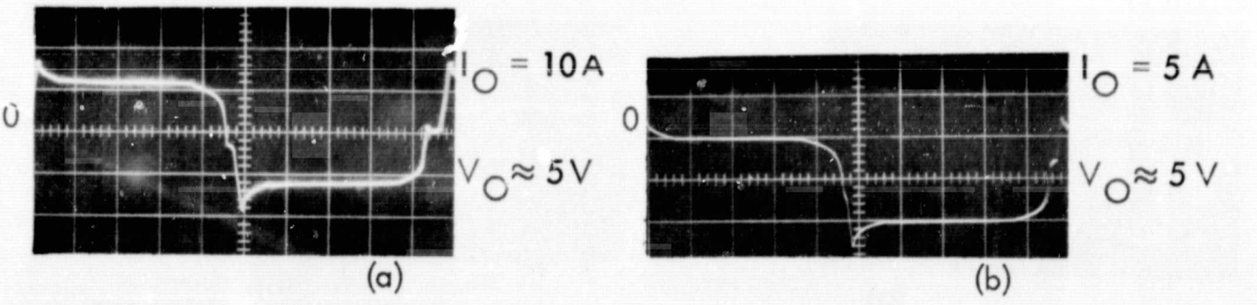


Figure 11. Drive-winding voltages (0.5-V/cm vertical and 0.1-ms/cm horizontal displacement).

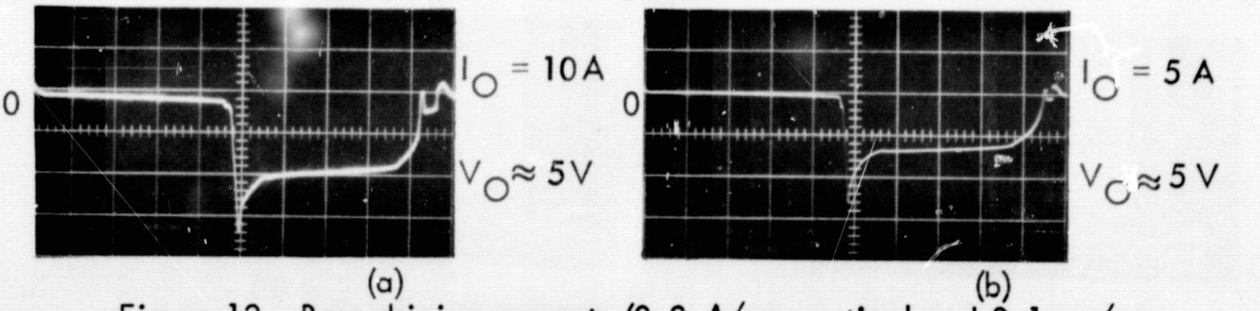


Figure 12. Base driving currents (0.2-A/cm vertical and 0.1-ms/cm horizontal displacement).

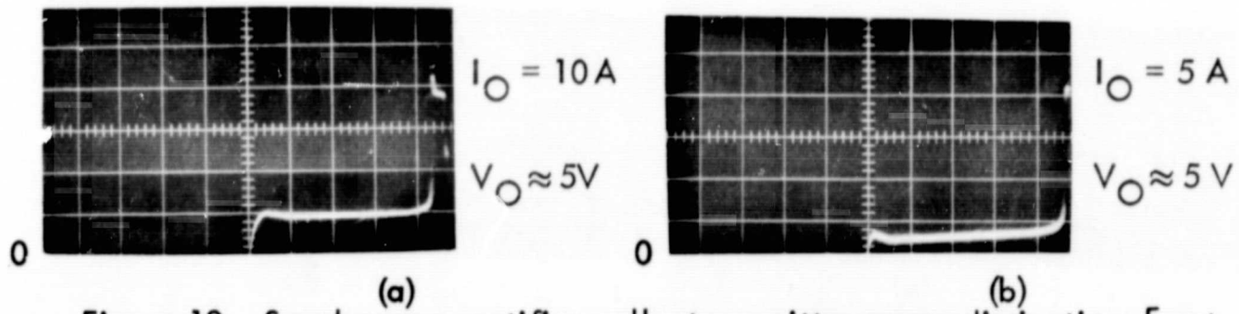


Figure 13. Synchronous rectifier collector-emitter power dissipations [part (a), 1.2-W/cm vertical and 0.1-ms/cm horizontal displacement; part (b), 0.6-W/cm vertical and 0.1-ms/cm horizontal displacement].

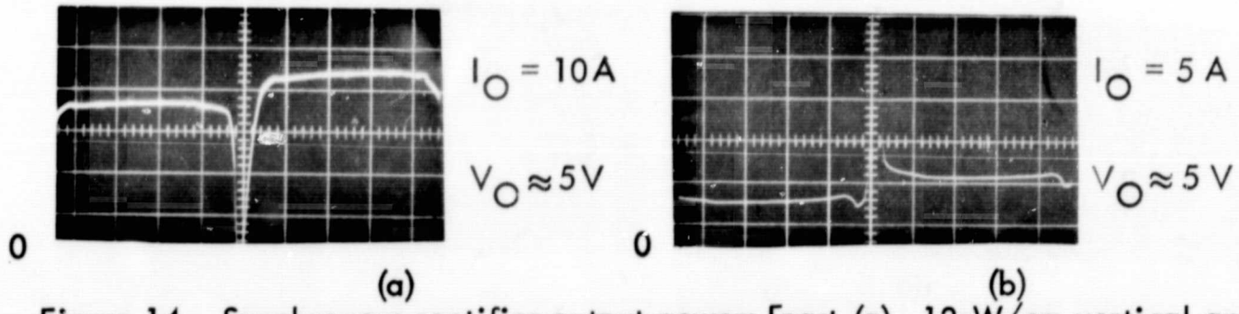


Figure 14. Synchronous rectifier output powers [part (a), 12-W/cm vertical and 0.1-ms/cm horizontal displacement; part (b), 6-W/cm vertical and 0.1-ms/cm horizontal displacement].

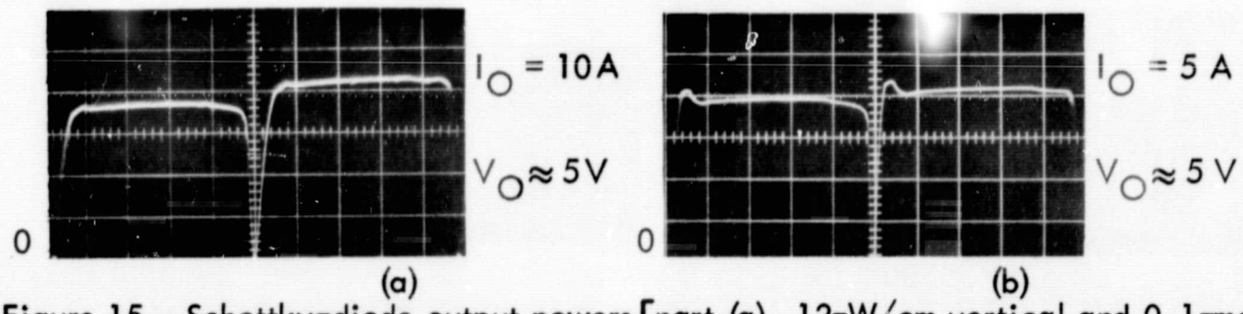


Figure 15. Schottky-diode output powers [part (a), 12-W/cm vertical and 0.1-ms/cm horizontal displacement; part (b), 6-W/cm vertical and 0.1-ms/cm horizontal displacement].

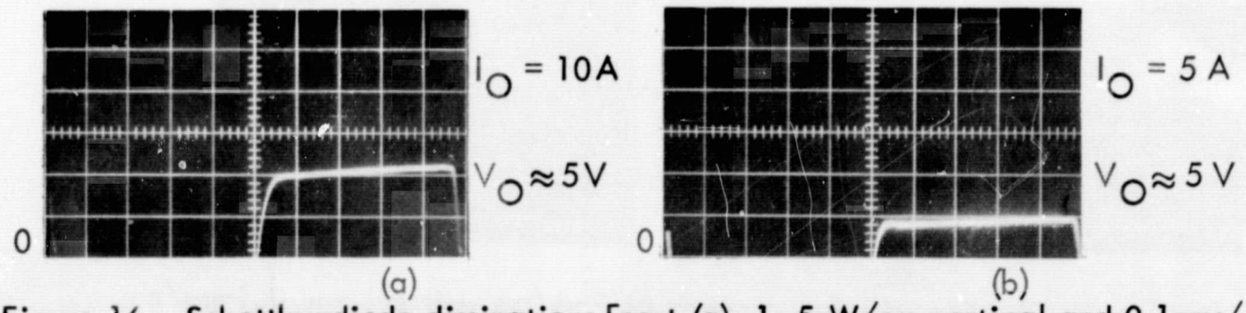


Figure 16. Schottky-diode dissipations [part (a), 1.5-W/cm vertical and 0.1-ms/cm horizontal displacement; part (b), 1.2-W/cm vertical and 0.1-ms/cm horizontal displacement].

Newly available Schottky hot-carrier power rectifier diodes* were subjected to approximately the same operating conditions as the synchronous rectifiers. The diodes were substituted for the transistors in the circuit of Figure 8, with the N7 drive-windings open circuited. Some of the typical data for the power diodes are illustrated in Figures 15 and 16. The power-diode rectifier efficiencies were calculated from

$$\eta = \frac{P_O}{P_O + P_D} ,$$

where P_O and the diode dissipation P_D were both measured by PPM. The results of the power-diode rectifier efficiency measurements are shown in Table 2.

Table 2

Rectifier Efficiency Measurements

Test	I_O (A)	P_O (W)	P_D (W)	η (%)
1	5	25.8	1.2	95.5
2	10	51.6	3.0	94.5

CONCLUSIONS

The driven transistor synchronous rectifier has both a low forward drop when conducting and low leakage when cut off. For very low output voltage requirements, very low saturation voltage transistors are available which can further improve efficiency.

For the case of low output voltage requirements where a low input voltage converter is used (Figure 5), the load-related storage-time-compensated base drive for transistor synchronous rectification has provided improved reliability and efficiency. Demonstrated total dissipations $P_{CE} + P_B$ were approximately half that of the most efficient low voltage power diodes avaible.

Where adequately rated transistors are available, some improvements of rectification efficiency and reliability at moderately high output voltages is possible using the new load-related, storage-time-compensated driven synchronous rectifier technique.

*Motorola, MBD 5500A

For the case of low output voltage requirements from moderately high voltage sources where a step-down output transformer-rectifier combination is employed, the use of the new barrier-type power diodes yields higher reliability than the use of a voltage-driven transistor synchronous rectifier (Figure 2) and provides for a simplification of the basic circuit.

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