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An Overview of Associative or Content-Addressable Memory Systems and a KWIC Index to the Literature

by

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An Overview of Associative or Content-Addressable Memory Systems and a KWIC Index to the Literature 1956-1970

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Abstract

This bibliography of associative or content-addressable memory systems covers the literature from approximately 1956 through 1970. A brief overview of the literature referencing pertinent articles is provided. The overview is current to approximately 1969 when it was written. In addition, the bibliography is presented as a Key Word In Context Index (KWIC).** Areas discussed in the overview are applications, hardware implementation, computer organizations with associative memories, and software aspects.

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1. Introduction

Content-addressable and associative memory systems have been under active investigation since 1956. Work in this field received its impetus from the efforts of Slade and McMahon [SMTC57] who described cryogenic catalog memory cell designs. Such memories have been referred to variously as catalog memories [SMTC57], associative memories [KPAM61], parallel-search memories [FAAF62], content-addressable memories [FRCA63], and data-addressed memories [NFAC62].

The International Federation of Information Processing Society Glossary defines an associative store as, "a <u>store</u> whose <u>registers</u> are not identified by their name or position but by their <u>content</u>."* In explaining the definition by an example, the glossary further notes that the retrieval of any one item in such a store would be accomplished by searching all registers in parallel to retrieve the relevant data by a content search with but a single operation. An excellent survey of associative memory technology has been provided by Hanlon [HACA66]. This overview emphasizes work accomplished subsequent to Hanlon's article.

An associative processor consists of an associative memory and additional hardware to permit manipulation of the data in the memory store.

Typical elements of an associative processor are:

- 1. The memory array which provides the data storage itself.
- 2. <u>The comparand register</u> which contains the data to be compared against the contents of the memory array for searches; may provide a shifting register for some input/output operations; and can play an intermediate role in the transfer of data between the memory array and a general

^{*}Joint Technical Committee on Terminology. <u>IFIP-ICC Vocabulary of Information</u> <u>Processing</u>. Amsterdam: North Holland Publishing Company, 1966.

purpose computer depending upon the configuration in which the processor is employed.

- 3. <u>The mask register</u> which is used to contain data specifying portions of words for operations involving only word portions.
- <u>The resolver</u> which is used to determine the location of response bitsin the response store.
- 5. <u>The search logic</u> which causes the search commands received by the memory to be executed properly. Search operations are generally accomplished in a bit serial, word parallel fashion starting at the most significant bit.
- <u>The response store</u> which receives vectors indicating which data satisfy a given search criterion and which can execute logical operations, such as shifting and Boolean operations on these vectors.

For example, an associative processor, developed by the Goodyear Aerospace Corporation, The Goodyear Associative Processor [BDPP66], has the elements described above. Fuller and his associates [BCS066] propose that in addition to a parallel read operation, associative memories have a multi-write capability to enter words in parallel into the associative processor's memory array.

2. Applications of Associative Memories

The importance of a content-addressable memory lies not only in the ability to search the memory by content, but to do so in parallel within approximately the same amount of time that would be required to access a single memory element in today's digital computers. Because of this capability, numerous speculative articles have been written specifying the various fields of application in which such memories could be applied. Some of the application areas proposed have been for sorting [SLAM62]; pattern recognition [USPD59, MDTL61, YYPR66]; solution of partial differential equations [BBP062]; radartrack correlation [JKTT62, KAA068]; path finding in graphs [CBPF68]; document retrieval [CBDA62, YYAC66]; machine translation [BTAC66, HJAC67]; relational data searches [SLAS66, SLAS67, LSAP65]; question-answering systems [ASTA67]; data storage and retrieval systems [GMA066, FBS065, DGAS66]; chemical substructure searching [ACAM68] and numerous other applications (see [EFSA63] and [GJTF62] for several applications of associative processings).

With the exception of a very limited number of areas, as noted by Hanlon [HACA66], "...the superiority of the content-addressable memory or associative processor is only implied, not proved." For a number of applications developed since Hanlon completed his survey, small associative memories do not appear particularly advantageous. Applications of this type include: (1) formatted file problems [GMA066, FBS065]; (2) dictionarý look-up for translation efforts [BTAC66]; (3) automatic abstracting problems [GRHA66]; and (4) for use with compilers [PCAM67]. In both [DGAS66] and [FBS065], a specific associative processor integrated with a second generation computer environment was postulated. Machine coding was generated in each instance. Although some advantage could be shown for an associative memory configuration, the cost differential and actual time saved would not make the approach worth the effort. The compiler study [PCAM67], concluded that the input/output for memory loads was excessive in the use of a small associative memory for compilation.

When originally conceived, associative memories were thought of as devices to permit the easy manipulation of large masses of data. More recently they have been thought of as devices to aid in the control functions associated with a data processor. Chu [CYA065] proposed an associative memory to assist in dynamic storage allocation problems. A small associative memory can be used to keep a map of memory and of program locations to assist in dynamic storage allocation. The IBM 360 series [BGM064] contains a small associative memory used in this way. Green et al. [GMA066] note that a small associative memory might be used to store queued requests for input/output devices such as discs and drums so that the requests could be retrieved in a sequence that would minimize access time or latency time. Prywess has made a similar observation. Gunderson et al. [GFAT66] have been studying the use of associative memories for other control functions within a multi-processor computer organization. Bird, et al. [BCS066] have used an associative memory to scan the output of drum tracks in parallel for a fixed-field formatted file application. That is, the associative memory was used as a filter between the drum and the central processor.

3. Associative Memory Implementations and Computer Organizations

Although several individuals speculated as early as 1961 that large associative memories would be available [MTSC61, RJCM61], no such memories appear to be imminent. To implement an associative or content-addressable memory, a considerable amount of logic at each cell is required. To achieve complicated cell circuit designs at a reasonable cost, researchers believed that cryogenic or superconductive technology developments were required.

There have been several different approaches towards hardware elements for associative memories. These fall in the areas of cryoelectrics, magnetics, and tunnel diodes.

3.1 Cryoelectrics

Work in crycelectrics was perhaps the first area investigated. Such investigators as Slade [SATW59, SMTC57]; Seeber [SLAM62, SLAL63, SRAS60, SRCA60, SRSM61]; Newhouse and Fruin [NFAC62]; Davies [DPAP64, DPDF63]; Mann and Rogers [MRAC62], discuss various implementations of cryoelectric memories. The latter report upon experimental work in which small arrays of cells were utilized, and have also described a bit logic for "between limits" retrieval. As more complicated operations are specified, the number of cryotrons per cell becomes large. Newhouse and Fruin [NFAC62] claimed the feasibility of a 300,000 bit (approximately 8,000 word) memory in 162 although their experiment was conducted on a three-word module consisting of 81 crossed-fil croyotons. Although technological developments in evaporation and insulation of films promised the realization of larger arrays than those envisioned by Newhouse and Fruin, no such developments have taken place. Indeed, interest in cryogenic devices for associative memories appears to be waning, while interest in other areas appears to be developing. Abrons and Burns [ABSM64] consider the development stages in applying superconductive devices and review superconductive memories. Burns [BLCR65] is developing a large superconductive random access memory using batch fabrication techniques based on the RCA superconductive continuous sheet memory. The approach shows promise for random-access memories in the range of 10^7 bits and potentially for a 10^9 bit size.

3.2 Magnetics

Because magnetic devices appeared to promise earlier realization of an 🕓 associative memory than did a crycelectric memory, many such devices have been Consideration has been given to magnetic cores [HSS064, KPAM61; developed. MPAM61]; transfluxors [LSAM63]; biax cores [CMAM64]; and multi-aperture logic elements [RCAP64] among several magnetic techniques. Due to the high power dissipation and high cost associated with the magnetic approach, the memories are necessarily small and have limited extendability in that they cannot store large data files. A magnetic film approach, which permits an associative memory using non-destructive readout, has been reported by Joseph and Kaplan Kaplan has estimated [KAAS63, JKTT62] that with bi-core thin-film [JKTT62]. elements, a 10,000 word associative memory is feasible. The Goodyear Aerospace Corporation [GRAH64, BDPP66] was funded by Rome Air Development Center [AF 30 [602-3549] to construct a 2048 word associative processor, The Goodyear Association Processor (GAP). GAP is constructed using the BILOC elements to hold each bit. The memory consists of two 1024 word memories of 48 bits per word that share common logic. Green, et al [GMA066] analyze the cost of magnetic memory elements and alternative logic for associative processors such as GAP. These estimates include the relative costs for the basic associative memory array, the logic required to drive the memory, and the response stores required to manipulate the output of a series of search requests submitted to the processor.

Other devices have been used for associative memories. A memory organization

using tunnel diodes is described by Fuller [FRCA63]. These memories seem to hold some promise. Some other devices used for memory arrays are laminated ferrites [WMWN63], magnetic films [RCAP64], and solenoid arrays [PGAS64].

3.3 Associative Memory Organizations in Computer Systems

In considering associative memories, it is important to view them in the context in which they are to be employed, rather than as abstract entities. Thus, one must investigate such memories within the context of a general purpose computing system. Fuller [FRCA63] performed one such investigation in which the content-addressable memory was used as a special purpose device with little logic. Dugan, et al [DGAS66] consider several possible ways in which an associative memory may be connected and configured with a general purpose computer. These are:

- Peripheral Device connected on a normal transfer channel in the same manner as a disc or drum.
- (2) <u>Multiprocessor</u> a device that has its own instruction repertoire and can operate simultaneously with a central processor.
- (3) <u>Integrated</u> the associative memory is embedded as a part of core memory and can operate upon data both in an associative manner and in a conventional manner.
- (4) <u>Special I/O Search Controller</u> the associative memory is used to coordinate, control, and optimize search operations employing peripheral devices and thereby to assist the overall computation process by decreasing the imbalance between memory speeds.

With each of the above configurations, variants are possible with alternative logic mechanizations of the associative memory. The alternatives range from devices capable of elementary searches on equality, less than or equal,

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greater than or equal, maximum, minimum, etc., to devices that contain full parallel hardware, thereby permitting complex operations and extending the memory to have the capabilities of a processor.

In addition to the above interfaces, a number of designers have considered associative processors. One development in this regard is the Associative Store Processor (ASP) [LSAP65, SLAS66, SLAS67], described by Love, Savitt and Troop. The ASP machine organization provides the parallel search facilities of an associative memory plus inter-cell communication. The dominant element in the ASP machine organization is the context-addressed memory. This memory stores both data and programs and is intended to provide the ability to identify, in parallel, unknown items by specifying the context of relations in which the unknowns appear. A relatively small read-only memory is employed to store a micro-program for executing ASP instructions. However, the ASP machine organization has not reached a hardware implementation stage. An interpreter [SLAS68] has been implemented for the IBM 360 family of computers to simulate a portion of the ASP system.

The ILLIAC IV [BCIL68, KAA068, IUIL67], which is an outgrowth of the Solomon Computer [SBTS63, SBTS62, CGTS65], should provide extensive parallel processing capability. The ILLIAC IV is currently being implemented for the University of Illinois by the Burroughs Corporation. As noted in [BCIL68] "The nucleus of the system is the ILLIAC IV array, a matrix of 256 identical processing units, configured into four identical quadrants, each having 64 processing units under the direction of a common control unit. These array elements perform the computational tasks for the system." Each of the 256 processing elements has 2048 words of 64 bit memory. Associative processing is accomplished by performing search operations when the elements of the search field are in the same relative position in each processor. The cycle time is 240 nanoseconds. The processing elements have a 32 bit mode where each quadrant could be considered as 128 parallel operating units. The processing elements can communicate data to form neighboring processing elements by means of routing instructions.

The complete ILLIAC IV system for the University of Illinois includes a B6500 computer to perform input/output operations and compilation, and contains an operating system. A 10^9 bit, head-per-track disk file with a 40 millisecond rotation speed provides an effective transfer rate of 10^9 bits/ second. Westlund [WGAT68] has developed a timing simulator for the ILLIAC IV. The simulator, written in ALGOL, is implemented on the Burroughs B5500.

Kisylia [KAAA68] proposes an associative memory processor with distributed logic. His work is based upon the organization proposed by Lee and Paull [LPAC63]. The modification made by Kisylia lies in the construction of the memory cell and in the various modes of local communication each cell enjoys with its neighbors. Processing may take place simultaneously on three distinct levels in the machine. The hardware organization has not been implemented.

Murtha [MJHP66] has written a comprehensive and thorough article on highly parallel processing systems in which he describes associative memories and associative processors. Both hardware and software technical details of a large number of parallel processors are covered. In addition, he explains how an associative memory cell operates and describes the inter-communicating cell developed by Lee [LCIC62]. Murtha notes that, "...Probably the most ambitious hardware development is a cryogenic processor being built by Texas Instruments. It will have 5000 words of 65 bits each with a parallel read cycle time of about 10 μ sec. It is expected to be operating in the fall of 1966." As of the time period covered by this article, this author is not aware

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that the memory has been delivered to the sponsors, Rome Air Development Center (RADC).

Knapp [KMRP67] describes work sponsored by the Rome Air Development Center (RADC) in associative memory technology. In 1967 RADC was sponsoring the following hardware associative memory developments: an Associative List Selector (ALS) that implements a fast hash addressing scheme, is under development by Goodyear Aerospace Corporation [GBAL66]; a 120-bit 2350 cryotion associative processor plane is being fabricated by Texas Instruments, Incorporated [PJFA65, RGCA64]; a breadboard model of an associative memory that uses ferroelectric and photoconductor elements has been developed by the Marquardt Corporation [HBED66, HBAT65]; techniques for fabricating distributive logic and memory networks using monolithic chips, wafers and individual minature component elements are under development by the Westinghouse Aerospace Division [TRFT66]; and an associative memory array using enhancement insulated-gate complementary, thin-film field-effect transistor has been developed and partially tested by RCA under Contract AF30(602)-2718.

All of the above hardware organizations have permitted both the reading and the writing of data from and to an associative memory. Fixed or semipermanent stores have been used as content-addressable memories. Goldberg and Green [GGLF61] have reported upon a fixed content-addressable memory that involves the use of permanent wiring of information in an array of linear cores. Lewin, et al [LBFR65] have developed a fixed content-addressable memory where electronic punched cards are used as the storage medium. Lewis [LMAS65] has written a thorough survey of fixed memories for both content and conventional memories. Read-only memories are useful when one has encyclopedic information not subject to change, but they are not useful when the data base is subject to change.

3.4 Software Simulation of Associative Memories

In addition to the simulation of an associative processor, ASP [SLAS68], attempts have been made to simulate associative memory properties via software techniques. Feldman [FJA065], using a hash code to access entries in a table, basically simulates the exact match capabilities of an associative memory. The data accessed is organized in a ring data structure. His approach is very useful for systems that do not require the full capabilities of an associative memory (i.e., the ability to interrogate the entire memory on any combination of bits within a word, rather than on only an exact match). Rovner [RPAI66] has modified the hash code concept to organize the data where it exceeds the capacity of core. In this modification a two-level data store consisting of core and drum is required. Rovner develops a scheme for a paged software-simulated associative memory. Again, only the exact match is considered. Hilbing [HFTA68] also considers paged associative memory systems. Ash, et al [ASTA67] have used Feldman's approach to organize data for a question-answering system under development. The system is called TRAMPS. Rovner and Feldman [RFTL68, FRAA68] have developed an associative language called LEAP to facilitate programming their simulated associative processor. LEAP is an extension of ALGOL to include associations, sets and a number of auxiliary constructs. LEAP is a family of languages; each language adds a different set of features, to the ALGOL base. Forms of LEAP contain matrix operations, property sets, and on-line graphics [FRAA68, RPAA68]. Gall and Brotherton [BGAL66], describe an Associative List Selector (ALS) hardware device with capabilities similar to those of the associative memory that Rovner and Feldman are working out through a software simulation. The ALS is a hardware implementation of hash addressing to give a fast search capability on equality.

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4. Software Studies

The area of software for associative memories has by and large been neglected. Falkoff [FAAF62], using Iverson's notation, has developed numerous algorithms for associative memories. Estrin and Fuller [EFAF63] have also described algorithms for associative memories. They further note that content-addressable memories are more flexible than list structures since, within a list structure, data is ordered with respect to predecessors and successors of elements on a list. However, in a content-addressable memory, data sets are unordered. Lewin [LMR062] has developed an elegant technique requiring two sense outputs for each digit of the word and requiring 2m-1 cycles for the complete readout of m words that match the interrogation bit configuration. The time is a function of the number of multiple matches and is not a function of the size of the associative store. A new proof of Lewin's result has been developed by Wolinsky [WAAS68].

Dugan, et al [DGAS66] note that several macro type instructions are required for dealing with several classes of data in an associative memory. They describe a routine called SPO that saves all response stores and status (busy) bits and "deactivates" that AM segment not defined by SPO. Other macros noted were NGT (to find the value of a data word from a list which is next greater than the comparand), AND (to find the conjunction of two lists of data words), and an executive type routine, DISPATCHER, that handles the problem of data loads to the associative memory. They note that programming for associative memories is "difficult to learn because associative configurations are conceptually different from other configurations". Green, et al [GMA066] expand upon the implications of associative processing for programmers reported by Dugan.

There are several hardware features that could help the software manipulative

problem. Bird, et al [BCSO66] note that a multi-write capability that permits one to write simultaneously into memory registers is important for associative manipulation. Dugan, et al [DGAS66] note that the ability to retain and to manipulate tag bits in a word and to perform indirect addressing or index modifications of associative instructions for associative memory locations are important hardware features required by software personnel.

5. Summary

Associative memory hardware technology has not yet come of age. After more than twelve years of effort in the field, only experimental hardware or small memories exist. Simulation solutions have yet to include the full capability of associative memories. Software studies indicate that programming associative memories is complex and that much more work is required in this area. Although the associative property is useful, manipulating associatively stored data may be complex.

Two application areas that look promising for associative memories are those of control operations and question-answering systems. A survey of question-answering systems is provided by Simmons [SRAE65]. More recent work is provided in [KCNL68, WWPS68, SBAC68, GRTU68].

No one has yet completed a study that conclusively shows that associative memories or processors in a computer environment are clearly better than a conventional memory. For the types of problems he considers, Feldman [FJA065] notes that a simulation of an associative memory on conventional hardware is competitive with the hardware approach.

It is clear that the promise of associative or content-addressable memories has not materialized. Much work remains to be done to achieve large data stores of associative memories. The software approaches to achieve associative capabilities will become increasingly important as associative hardware continues to remain limited. More quantitative studies, rather than speculative studies, are required to determine the precise advantages or disadvantages of associative memory technology.

As may be seen from the size of this bibliography, the literature in associative memory technology continues to grow rapidly. It is hoped that future studies will provide further insight into the prospects for this technology.

Preface to KWIC* Index

The bibliography consists of two parts. The first part is the Key Word In Context (KWIC) Index which lists the titles sorted according to index words selected from the title. Preceding each title is a six-character code. The coding scheme (devised by the late H. P. Luhn who developed one of the first KWIC indexes) is composed by taking the first character of the author's last name, the first character of his first name, the first character of the first and second words of the title, and the date of the article. A slight modification of the code applies for multiple authors, corporate authors and other non-standard situations. The second part of the bibliography consists of the citations themselves sorted according to the coding scheme. In addition to the citation, the computer review number is provided whenever the article has been reviewed in Computing Reviews. The citation appears only once in the second part of the bibliography even though there may be multiple authors. References in the text are specified in terms of the code.

The bibliography has been accumulated over several years starting in 1963. Among the journals covered in the bibliography are the Joint Computer Conferences, Association for Computing Machinery publications and Defense Documentation Center publications. Other journals have also been searched in accumulating the bibliography. Two searches of the Defense Documentation Center holdings were requested: search control No. 001550 and 101547 October 7, 1968. Wherever possible, patents concerning associative memory developments have been included.

^{*}The Key Word In Context Index (KWIC) program used was developed by Mr. J. Gary Augustson and Mr. Arnold Miller of the University of Maryland Computer Science Center for the UNIVAC 1108 computer.

			+++++KUTA TNREY++++
NAAT65	REASONANT	ABSORPTION	NON-DESTRUCTIVE READ-OUT TECHNIQUE.=A THIN MAGNETIC FILM COMPUTER NEMORY USING
PSAA67	, AN	ABSTRACT	PARALLEL PROCESSING SYSTEM.=
CRAM69	CIATIVE MEMORY	ACCEPTORS	#ASS0
FRVT69	OPOLOGY RANDOM	ACCESS	MEMORY OFGANIZATIONS=VARIABLE T
WRAT	MULTIPLE-WORD	ACCESS	MEMORIFS.=A TRANSISTOR-TUNNEL DIODE CELL FOR ASSOCIATIVE MEMORIES AND
NECS67	LLS FOR RANDOM	ACCESS	MEMOPIES.=CRYOTRON STORAGE CF
FRVT69	OPOLOGY RANDOM	ACCESS	MEMORY ORGANIZATIONS.=VARIABLE T
NH1062	OF STOPAGE AND	ACCESS	TECHNIQUES SUITABLE FOR USE IN LARGE-CAPACITY DIGITAL MEMORIES, =INVESTIGATION
MSF161	STOPAGE AND	ACCESS	TECHNICUES = FUNDAMENTAL INVESTIGATION OF DIGITAL COMPUTER
LAAA61	REDUCE THE	ACCESS	TIME FOR INSTRUCTIONS IN LOOPS. = AN APPLICATION FOR A SMALL, FAST ASSOCIATIVE M
HGOR57	QUASI-RANDOM	ACCESS	MEMORY SYSTEM .=
BLCR65	LECTRIC RANDOM	ACCESS	MEMORY. PHASE 3.=CRYOE
BACR66	LECTRIC RANDOM	ACCESS	MEMORY - PHASE 3.=CRYOF
NDCS65	ING FOR RANDOM	ACCESS	MEMORIES. = CONTINUOUS SHEFT SENS
BBCR64	LECTRIC RANDOM	ACCESS	MEMORY, PHASE 2 10 (9) BIT MEMORY.=CRYOE
NVCA65	CRYOGENICS -	ACHIEVEMENT	AND POTENTIAL .=
FRAL67		ACHIEVING	LARGE SCALE COMPUTING CAPARI ITTES THROUGH ASSOCIATIVE PARALLEL PROCESSING
FRAL		ACHIEVING	LARGE COMPUTING CAPABILITIES THROUGH ASSOCIATIVE PARALLEL PROCESSING.=
SDAL		ACHIEVING	LARGE COMPUTING CAPABILITIES THROUGH AN ARRAY COMPUTER.=
GJBT60	SIMULTANEOUS	ACTION	BRINARY TESTS FOR TWO TERMINAL
BRAA69	EALIZATION FOR	ACTIVE	SONAP SIGNAL PROCESSING. AN ASSOCIATIVE MEMORY PARALLEL DELTIC R
MEN067	MS - CYCLIC TO	ACYCLIC	GRAPH TRANSFORMATIONS. =MODELS OF COMPUTATIONAL SYSTE
KMSP64	HASIS ON	ADAPTATION	TO USE THROUGH MAN-MACHINE INTERACTION SOME PROBLEMS IN INFORMATION SCIENCE W
NCAT63		ADAPTIVE	THRESHOLD LOGIC.=
ACTC65	CTION OF AN	ADAPTIVE	MAN-MACHINE ASSOCIATIVE MEMORY FOR INFORMATION RETRIEVAL - TOWARDS CONTROLIED E
KMAM62		ADAPTIVE	MFCHANISMS IN DIGITAL ' CONCEPT ' PROCESSING. =
WDCA68	Y DESIGN USING	ADAPTIVE	AND ASSOCIATIVE TECHNIQUES.=COMPUTER=AIDED STRATEG
EVCA62	CORRECTION AND	ADDENDUM	=COSPEC
YYAN66	A NONBULK	ADDITION	TECHNIQUE FOR ASSOCIATIVE PROCESSORS.=
ISSB56	SOPTING BY	ADDRESS	CALCULATION. =
SGA064	ASSOCIATIVELY	ADDRESS	DISTPIBUTED MEMORY.=APPLICATION OF AN
FESA63	NS FOR CONTENT	ADPRESSABLE	MEMORIES=SOME APPLICATIO
PEAI69	RATORY CONTENT	ADDRESSABLE	MEMORY SYSTEM. = AN IMPROVED FIELD-CONTROLLED POLARIZATION-TRANSFER DEVICE AND T
FRCA63	CONTENT	ADDRESSABLE	MEMORY SYSTEMS.=
LCCA68	CONTENT	ADDRESSABLE	AND DISTRIBUTED LOGIC MEMORIFS. =
НЈАС67	A CONTENT	ADDRESSABLE	MEMORY WITH APPLICATIONS TO MACHINE TRANSLATION.=
LPAC64	A CONTENT	ADDRESSABLE	DISTPIPUTED LOGIC MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=
BRCAG6	CONTENT	ADDRESSABLE	MEMORY .=
BKCA66	CONTENT	ADDRESSABLE	MEMORY
BRCA67	CONTENT	ADDRESSABLE	
SLPC65	ANEL : CONTENT	ADORESSABLE	MFMORIES.==
LPAC63	A CONTENT	ADDRESSABLE	DISTRIBUTED LOGIC MEMORY WITH APPLICATION TO INFORMATION RETRIEVAL.=
COCA65	CONTENT	AUPRESSABLE	MEMORY SYSTEMS CONCEPTS.=
Інтабе	TAG	ADDRESSED	MEMORY.=
LSAM63	GNETIC CONTENT	ADDRESSED	MEMORY.=ALL MA
GJAI63	INTRINSICALLY	ADDRESSED	PROCESSING SYSTEM. = AN
GECA67	CONTENT	AUPRESSED	MEMORY.=
SKCA67	CONTENT	ADPRESSED	MEMORY.=
NFAC62	CRYOGENIC DATA	ADDRESSED	MEMORY _= A
LMROA2	FROM A CONTENT	ADDRESSED	MEMOPY.=RETRIEVAL OF ORDERED LISTS
NFDA62	DATA	AUPRESSED	MEMORY USING THIN-FILM CRYOTRONS.=
EFMA64	NULTIPLE	ADDRESSING	FOR FIXED-TAG ASSOCIATIVE MEMORIES.=
RRTA67	CIATIVE MEMORY	ADDRESSING	=TRANSLATED ASSO
NAAN62	E OF SCRAMELED	AUDRESSING	FOR ASSOCIATIVE MEMORIES.=A NOTE ON THE US
РНСА62	CONTENT	ADDRESSING	AND INFORMATION RETRIEVAL.=
PGAS64	NG CORFELATION	ADDRESSING	=A SENTPERMANENT MEMORY UTILIZI

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Ertag9	THE	ADVANCED	AVIONICS DIGITAL COMPUTER.=
18AP62	R THE STUDY OF	ADVANCED	INFORMATION RETRIEVAL TECHNICUES = A PROPOSAL FO
GJTF62	TECHNIQUES FOR	ADVANCED	INFORMATION PROCESSING SYSTEM. = TECHNI
GAAG67	.'	ADVANCED	GENERAL -PURPOSE COMPLITER ORGANIZATIONS -
JH\$068	STUDY OF	ADVANCED	ASSOCIATIVE PROCESSOR TECHNICIES INTERIN PERAPE -
RDAC66	•	ADVANCED	COMPUTER ORGANIZATION STUDY -
PSED68	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE REMORTES -ELEMENT D
BTAC66		ADVANCED	COMPUTER ORGANIZATION -
HBED66	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES SELEMENT D
HHED67	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES HELEMENT D
BGED67	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES. = FIEMENT D
BFAC62		ADVANCED	
KBAI67		ADVANCES	IN MEMORY TECHNOLOGY.=
GJCD67	E FOR COMPUTER	AIDED	DESIGN : A SURVEY ECOMPOUND DATA STRUCTUR
NwTA68-	E PROCESSOR IN	AIPCRAFT	CONFLICT DETECTION. THE ASSOCIATIV
RBAB67	OLIC AND	ALGEBRAIC	MANIPULATION TA BRIFE SUBVEY OF COMPLITED LANGUAGES FOR CANE
FRAA69	AN	ALGOL	PASED ASSOCIATIVE LANGUAGE=
FRAA68	AN	ALGOL-BASED	ASSOCIATIVE LANGUAGE =
₩ĸCR68	IC PROGRAMMING	ALGORITHM	ANNUAL PROBRESS DEPORT -CELLINAR REALTATION OF THE DUMAN
LCAA61	AN	ALGORITHM	FOR PATH CONNECTIONS AND ITE ADDITIONS -
RRAA64	A	ALGORITHM	FOR CONCURRENT RANDOM WALKS ON WIGHLY RADALLEL MACHINES
ASAM67	ATH CONNECTION	AL GORITHM	TA MODIFICATION OF IFFE P
NRPC69	STRUCTURES AND	ALGORITHMS	FOR LOCIC DESIGN PROBLEMS=PAGALLEL COMPLETING
FAAF62		ALGORITHMS	FOR PARALLEL SEARCH MEMORIES =
SJAI64	•	ALGORITHMS	IN PARALLEL COMPUTATION. =
MYSA69	AGE ALLOCATION	ALGORITHYS	IN THE TRANSULL COMPLLER STOR
EFAF63		ALGORITHMS	FOR CONTENT-ADDRESSABLE VEMORY ORGANIZATION -
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WCAM69	ASSOCIATIVE	MEMORY	
WCAM69	ASSOCIATIVE	MEMORY	
GKAC67	ONTINUCUS ETLM	MEMORY	DEVICE 340002/ Device 240002/
HHCS68	AN ASSOCIATIVE	MEMORY	FOR A THE CONCIDENT PULSESEA C
CCAM65	ASSOCIATIVE	MEMORY	FOR A TIME-SHARED PROCESSOR, =CONTROL STORAGE USF IN IMPLEMENTING
KUSA47			COMPUTER STSTEM : DESCRIPTION AND SELECTED NAVAL APPLICATIONS,=
004620	TENT ADDDERGED	MEMORI	CELLS=SUPERCONDUCTIVE C
828059	FD ACCACTANTUR	MEMORY	SYSTEM.=A GLASS DELAY LINE CON
	ED ASSOCIATIVE	MEMORY	=SILICON-ON-SAPPHIRE COMPLEMENTARY MOS CIRCUITS FOR HIGH SPE
KAP A67	·	MEMORY	ALLOCATION FOR MULTIPROCESSORS=
	ATIVE	MEMORY	AND PARALLEL PROCESSING=ON A COMPUTER LANGUAGE WHICH SIMULATES ASSOCI
NIAM69	SS ASSOCIATIVE .	MEMORY	#A MULTIACCE
PFA169	NT ADDRESSABLE	MEMORY	SYSTEM.=AN IMPROVED FIELD-CONTROLLED POLARIZATION-TRANSFER DEVICE AND THE OPER
FGLI68	AM-ADDRESSABLE	MEMORY	=LOW TEMPERATURE BE
FRVT69	RANDOM ACCESS	MEMORY	ORGANIZATIONS.=VARIABLE TOPOLOGY
BRAA69	AN ASSOCIATIVE	MEMORY	PARALLEL DELTIC REALIZATION FOR ACTIVE SONAR SIGNAL PROCESSING TAN ASS
GHSM66	SPACEBORNE	MEMORY	ORGANIZATION.=
SLRA69	GE ASSOCIATIVE	MEMORY	WITH ORDERED RETRIEVAL.==RAN
FkVT69	RANDOM ACCESS	MEMORY	ORGANIZATIONS=VARIABLE TOPOLOGY
WLAM70	ÅSSOCIATIVE	MEMORY	MODEL S=
LGTA69	ASSOCIATIVE	MEMORY	ETHE ARCHITECTURE OF A LARGE DISTRIBUTED LAGIC
KBA167	ADVÁNCES IN	MEMORY	TECHNOLOGY.
Ft₃UM	HÉ ASSOCIATIVE	MEMORY	PARALEE PROCESSING LANGUAGE, ANODI-IT TUSEDIS MANUAL FOR T
SJDL69	TRIBUTED LOGIC	MEMORY	COMPUTED FOR PROCESS CANNOLADE AMPTEMIL. OSER'S MANUAL FUR I
CRAM69	ASSOCIATIVE	MEMORY	
LFAS69	OF LOCK-ASIDE	MEMORY	
YYAC66	AR ASSOCIATIVE	NEMORY	
YYAC66	IC ASSOCIATIVE	NEMODY	
FWAM64	ASSOCIATIVE	NEMORY	CREATION RETRIEVAL.=A CRYOGEN
IVAI67	OR ASSOCIATIVE	NEMORY	
R1AM67	ASSOCIATIVE	' MCMORY	STSTEM WITH TUO NANOSECOND CYCLE TIME, TAN INTEGRATED MOS TRANSIST
RPAS62	1 2 ASSACTATIVE	MEMORY	FUR COLLECTION AND DISPLAY SYSTEM.=
DGTM62		MENORY	=A SEMANTICAL
CATAZO		MEMORY	=THE MULTI-LIST TY
	CALC CONCENTS	MEMORY	=THE ORGANIZATION OF A MULTILIST-TY
	CALE CRYDGENIC	MEMORY	=DESIGN OF A LARGE S
SUMMOU	STRUCTION OF A	MEMORY	DEVICE.=A NEW PRINCIPLE FOR THE CON
СПАМББ	- ASSOCIATIVE	MEMORY	ASSEMPLER,=AMDRIVE* AND CODAP
LPACA4	TRIBUTED LOGIC	MEMORY	WITH APPLICATIONS TO INFORMATION RETRIEVAL.==A CONTENT ADDRESSABLE DIS
RIMO67	M ASSOCIATIVE	MEMORY	=METHODS OF SFLECTING A MULTIVALENT ANSWER FRO
FRCA63	NT ADDRESSABLE	MEMORY	SYSTEMS.=CONTE
SHAP61	ED ASSOCIATIVE	NEMORY	FOR USE IN COMPTLING = A PROGRAMM
CHDI63	AN ASSOCIATIVE	MEMORY	DIMENSIONING IN
SNTW66	E CRYOFLECTRIC	MEMORY	SYSTEMS THREE WID
FCAM61	ASSOCIATIVE	MEMORY	APPLICATIONS FOR INTELL GENCE DATA PROCESSING -
CBPF68	TH ASSOCIATIVE	MEMORY	PATH FINDING WI
BvM066	R ASSOCIATIVE	MEMORY	INT TODELING OF A MEMORY SUCTEM INCLUDING A RUFER
SSTF60	YOTRON CATALOG	MEMORY	THIN TIM OF A WEMORY SYSTEM INCLUDING A BUFFE
FTAM68	IC ASSOCIATIVE	MEMORY	
RCAP64	AN ASSOCIATIVE	NEMORY	
SoTR68	UPERCONDUCTING	NEMORY	CELL A DESERVICE A PROPAL FOR
NMCA65	TENT-ADDRESSED	MEMORY	VELL - A PERSISTUTRON - IN A MEMORY MATRIX. THE RELIABILITY OF OPERATING A S
AMGE62	IC ASSOCIATIVE	NEMODY	CIDENT PAGNETORESISTIVE READONIO OF MAGNETIC THIN FILMS.=CON
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SAAD64	OF ASSOCIATIVE	MEMORIES	FROM A DEVICE POINT OF VIEW-SA DISCUSSION
CVTU67	IN ASSOCIATIVE	MEMORIES	THE USE OF CODES, MOUTON AND OPPER RETRIEVAL I
WAED64	V SEARCH	MEMORIES	TOALERE DETERMINATION AND ORDERED RETUINED
BRCA67	NT ADDRESSABLE	MEMORIES	HUNTE HUNTEN
WMWN63	W IN COMPUTER	NEMORIES	TN NUCLEAR PHYSICS.=
BCAM67	ASSUCIATIVE	NEMORIES	
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DORMAN	MAGNETIC FILM	MEMORIES	=PLATED WIRE
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SHAP68	SE OF NODIFIED	MEMORIES	=ASSOCIATIVE PROCESSING FOR GENERAL PURPOSE COMPUTERS THROUGH THE O
BGED67	ED ASSOCIATIVE	MEMORIES	=ELEMENT DEVELOPMENT FOR ADVANC
PSED68	ED ASSOCIATIVE	MEMORIES	=ELEMENT DEVELOPMENT FOR ADVANC
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RDAM65	ASSOCIATIVE	MEMORIES	AND INFORMATION RETRIEVAL. =
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APCM63	CRYOELECTRIC	MEMORIES	= ```
AHSA63	VE ASSOCIATIVE	MEMORIES	=SUPFRCONDUCTI
AHTB65	WORK-ORGANIZED	MEMORIES	=THE BRIDGE CELL - A NEW SUPFRCONDUCTIVE MEMORY CELL FOR RANDOM-ACCESS
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RPAG69	TENT-ADDRESSED	MEMORY	SYSTEMEA GLASS DELAT LINE CON
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TFAM68	IC ASSOCIATIVE	MEMORY	CHARACTER THE EMENTATION AND CHARACTERISTICS.=
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TRCA64	ER ASSOCIATIVE	MEMORY	FINAL REPORT.=COMPUT
SUASER	E SELE-SORTING	MEMORY	REVISED_=ASSOCIATIV
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HRIT63	ING THE SEARCH	MEMORY	WITH THE USQ-20 COMPUTER.=INTEGRAT
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EPCA43	NT-ADDRESSABLE	MEMORY	SYSTEMS = CONTE
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NAATAS	ETLM COMPLETER	MEMORY	USING & REASONANT ABSORPTION NON-DESTRUCTIVE READ-OUT TECHNIQUE. A THIN MAGNET
GEAMA 7	ASSOCIATIVE	MEMORY	
HLOPE7	-RANDON ACCESS	MEMORY	SYSTEM = GUAST
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TOTAZE	TAG ANNRESEEN	MEMORY	
1 42 425	ON ACCOUNTSSED	NEMORY	
	00 ACCOCIATIVE	NEMODY	WITH LOOP NANOSECONDE CYCLE TIME ZAN INTEGRATED MOS TRANSIST
1147	ACCACTATIVE	MEMORY	CACLEN - CACLENERS ALONG ALONG THE MAN MALEDUALES AND HANDED.
	ACCACIATIVE	MEMORY	
104060	ACCARTATIC		
IBAMAD	43300141114C	R C PIVA I	

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18CM65	CRYOGENIC	MEMORY	SYSTEM.=
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IHLM60	LOGICAL	MEMORY	STUDY.=
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EFAF63	NT-ADDRESSABLE	MEMORY	
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BFOT	AN ASSOCIATIVE	NEMORY	TON THE POLITION OF ALLOCATION, EAPPLICATION OF CON
BCAM65	ASSOCIATIVE	MEMORY	CIDCUTE
BUPP66	ASSOCIATIVE	NEMORY	
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FWAM64	ASSOCIATIVE	MEMORY	
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ABCACH	TC ACCOCIATIVE	NCMORY	TECHNIC CONCOLS STUDI.ª
RICALL	TC ASSOCIATIVE	MEMORY	
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YYAC66	IC ASSOCIATIVE	MEMORY	SYSTEM FOR INFORMATION RETRIEVAL. #A CRYOGEN
SLAM62	ASSOCIATIVE	MEMORY	WITH ORDERED RETRIEVAL
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PGML62	ED ASSOCIATIVE	MEMORY	=MULTI-LIST ORGANIZ
CWCA66	NT-ADDRESSABLE	MEMORY	TECHNIQUES.=CONTE
CWCA65	NT-ADDRESSABLE	MEMORY	TECHNIQUES.=CONTE
RPAI66	ASSOCIATIVE	MEMORY	SYSTEM TAN INVESTIGATION INTO PAGING A SOFTWARE-SIMULATED
RHTW68	2D CORE SEARCH	MEMORY	
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BACC61	UPERCONDUCTIVE	MEMORY	=COINCIDENT CURRENT S
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BCAL63	Y CRYOFLECTRIC	MEMORY	WITH CAVITY SENSING TA LARGE CAPACIT
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KMAH65	OVEN READ ONLY	MEMORY	=A HIGH-SPEED, W
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FETM60	TRIE	MEMORY	
LPAC63	TRIBUTED LOGIC	MEMORY	WITH APPLICATION TO INFORMATION RETRIEVAL =A CONTENT ADDRESSABLE DIS
SAAC62	A CRYOTRON	MEMORY	CELL.=
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