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An Overview of Associative or Content-Addressable Memory Systems and a KWIC Index to the Literature

by

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Abstract

This bibliography of associative or content-addressable memory systems covers the literature from approximately 1956 through 1970. A brief overview of the literature referencing pertinent articles is provided. The overview is current to approximately 1969 when it was written. In addition, the bibliography is presented as a Key Word In Context Index (KWIC).** Areas discussed in the overview are applications, hardware implementation, computer organizations with associative memories, and software aspects.

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1. Introduction

Content-addressable and associative memory systems have been under active investigation since 1956. Work in this field received its impetus from the efforts of Slade and McMahon [SMTC57] who described cryogenic catalog memory cell designs. Such memories have been referred to variously as catalog memories [SMTC57], associative memories [KPAM61], parallel-search memories [FAAF62], content-addressable memories [FRCA63], and data-addressed memories [NFAC62].

The International Federation of Information Processing Society Glossary defines an associative store as, "a store whose registers are not identified by their name or position but by their content."* In explaining the definition by an example, the glossary further notes that the retrieval of any one item in such a store would be accomplished by searching all registers in parallel to retrieve the relevant data by a content search with but a single operation. An excellent survey of associative memory technology has been provided by Hanlon [HACA66]. This overview emphasizes work accomplished subsequent to Hanlon's article.

An associative processor consists of an associative memory and additional hardware to permit manipulation of the data in the memory store.

Typical elements of an associative processor are:

1. The memory array which provides the data storage itself.
2. The comparand register which contains the data to be compared against the contents of the memory array for searches; may provide a shifting register for some input/output operations; and can play an intermediate role in the transfer of data between the memory array and a general

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*Joint Technical Committee on Terminology. IFIP-ICC Vocabulary of Information Processing. Amsterdam: North Holland Publishing Company, 1966.

purpose computer depending upon the configuration in which the processor is employed.

3. The mask register which is used to contain data specifying portions of words for operations involving only word portions.
4. The resolver which is used to determine the location of response bits in the response store.
5. The search logic which causes the search commands received by the memory to be executed properly. Search operations are generally accomplished in a bit serial, word parallel fashion starting at the most significant bit.
6. The response store which receives vectors indicating which data satisfy a given search criterion and which can execute logical operations, such as shifting and Boolean operations on these vectors.

For example, an associative processor, developed by the Goodyear Aerospace Corporation, The Goodyear Associative Processor [BDPP66], has the elements described above. Fuller and his associates [BCS066] propose that in addition to a parallel read operation, associative memories have a multi-write capability to enter words in parallel into the associative processor's memory array.

2. Applications of Associative Memories

The importance of a content-addressable memory lies not only in the ability to search the memory by content, but to do so in parallel within approximately the same amount of time that would be required to access a single memory element in today's digital computers. Because of this capability, numerous speculative articles have been written specifying the various fields of application in which such memories could be applied. Some of the application areas proposed have been for sorting [SLAM62]; pattern recognition [USPD59, MDTL61, YYPR66]; solution of partial differential equations [BBPO62]; radar-track correlation [JKTT62, KAAO68]; path finding in graphs [CBPF68]; document retrieval [CBDA62, YYAC66]; machine translation [BTAC66, HJAC67]; relational data searches [SLAS66, SLAS67, LSAP65]; question-answering systems [ASTA67]; data storage and retrieval systems [GMAO66, FBSO65, DGAS66]; chemical substructure searching [ACAM68] and numerous other applications (see [EFSA63] and [GJTF62] for several applications of associative processings).

With the exception of a very limited number of areas, as noted by Hanlon [HACA66], "...the superiority of the content-addressable memory or associative processor is only implied, not proved." For a number of applications developed since Hanlon completed his survey, small associative memories do not appear particularly advantageous. Applications of this type include: (1) formatted file problems [GMAO66, FBSO65]; (2) dictionary look-up for translation efforts [BTAC66]; (3) automatic abstracting problems [GRHA66]; and (4) for use with compilers [PCAM67]. In both [DGAS66] and [FBSO65], a specific associative processor integrated with a second generation computer environment was postulated. Machine coding was generated in each instance. Although some advantage could be shown for an associative memory configuration, the cost differential and actual time saved would not make the approach worth

the effort. The compiler study [PCAM67], concluded that the input/output for memory loads was excessive in the use of a small associative memory for compilation.

When originally conceived, associative memories were thought of as devices to permit the easy manipulation of large masses of data. More recently they have been thought of as devices to aid in the control functions associated with a data processor. Chu [CYA065] proposed an associative memory to assist in dynamic storage allocation problems. A small associative memory can be used to keep a map of memory and of program locations to assist in dynamic storage allocation. The IBM 360 series [BGM064] contains a small associative memory used in this way. Green et al. [GMA066] note that a small associative memory might be used to store queued requests for input/output devices such as discs and drums so that the requests could be retrieved in a sequence that would minimize access time or latency time. Prywess has made a similar observation. Gunderson et al. [GFAT66] have been studying the use of associative memories for other control functions within a multi-processor computer organization. Bird, et al. [BCS066] have used an associative memory to scan the output of drum tracks in parallel for a fixed-field formatted file application. That is, the associative memory was used as a filter between the drum and the central processor.

3. Associative Memory Implementations and Computer Organizations

Although several individuals speculated as early as 1961 that large associative memories would be available [MTSC61, RJCM61], no such memories appear to be imminent. To implement an associative or content-addressable memory, a considerable amount of logic at each cell is required. To achieve complicated cell circuit designs at a reasonable cost, researchers believed that cryogenic or superconductive technology developments were required.

There have been several different approaches towards hardware elements for associative memories. These fall in the areas of cryoelectrics, magnetics, and tunnel diodes.

3.1 Cryoelectrics

Work in cryoelectrics was perhaps the first area investigated. Such investigators as Slade [SATW59, SMTC57]; Seeber [SLAM62, SLAL63, SRAS60, SRCA60, SRSM61]; Newhouse and Fruin [NFAC62]; Davies [DPAP64, DPDF63]; Mann and Rogers [MRAC62], discuss various implementations of cryoelectric memories. The latter report upon experimental work in which small arrays of cells were utilized, and have also described a bit logic for "between limits" retrieval. As more complicated operations are specified, the number of cryotrons per cell becomes large. Newhouse and Fruin [NFAC62] claimed the feasibility of a 300,000 bit (approximately 8,000 word) memory in 162 although their experiment was conducted on a three-word module consisting of 81 crossed-fil croyotons. Although technological developments in evaporation and insulation of films promised the realization of larger arrays than those envisioned by Newhouse and Fruin, no such developments have taken place. Indeed, interest in cryogenic devices for associative memories appears to be waning, while interest in other areas appears to be developing. Ahrons and Burns [ABSM64] consider the development stages in applying superconductive devices and review superconductive

memories. Burns [BLCR65] is developing a large superconductive random access memory using batch fabrication techniques based on the RCA superconductive continuous sheet memory. The approach shows promise for random-access memories in the range of 10^7 bits and potentially for a 10^9 bit size.

3.2 Magnetics

Because magnetic devices appeared to promise earlier realization of an associative memory than did a cryoelectric memory, many such devices have been developed. Consideration has been given to magnetic cores [HSSO64, KPAM61, MPAM61]; transfluxors [LSAM63]; biax cores [CMAM64]; and multi-aperture logic elements [RCAP64] among several magnetic techniques. Due to the high power dissipation and high cost associated with the magnetic approach, the memories are necessarily small and have limited extendability in that they cannot store large data files. A magnetic film approach, which permits an associative memory using non-destructive readout, has been reported by Joseph and Kaplan [JKTT62]. Kaplan has estimated [KAAS63, JKTT62] that with bi-core thin-film elements, a 10,000 word associative memory is feasible. The Goodyear Aerospace Corporation [GRAH64, BDPP66] was funded by Rome Air Development Center [AF 30 [602-3549] to construct a 2048 word associative processor, The Goodyear Association Processor (GAP). GAP is constructed using the BILOC elements to hold each bit. The memory consists of two 1024 word memories of 48 bits per word that share common logic. Green, et al [GMAO66] analyze the cost of magnetic memory elements and alternative logic for associative processors such as GAP. These estimates include the relative costs for the basic associative memory array, the logic required to drive the memory, and the response stores required to manipulate the output of a series of search requests submitted to the processor.

Other devices have been used for associative memories. A memory organization

using tunnel diodes is described by Fuller [FRCA63]. These memories seem to hold some promise. Some other devices used for memory arrays are laminated ferrites [WMWN63], magnetic films [RCAP64], and solenoid arrays [PGAS64].

3.3 Associative Memory Organizations in Computer Systems

In considering associative memories, it is important to view them in the context in which they are to be employed, rather than as abstract entities. Thus, one must investigate such memories within the context of a general purpose computing system. Fuller [FRCA63] performed one such investigation in which the content-addressable memory was used as a special purpose device with little logic. Dugan, et al [DGAS66] consider several possible ways in which an associative memory may be connected and configured with a general purpose computer. These are:

(1) Peripheral Device - connected on a normal transfer channel in the same manner as a disc or drum.

(2) Multiprocessor - a device that has its own instruction repertoire and can operate simultaneously with a central processor.

(3) Integrated - the associative memory is embedded as a part of core memory and can operate upon data both in an associative manner and in a conventional manner.

(4) Special I/O Search Controller - the associative memory is used to coordinate, control, and optimize search operations employing peripheral devices and thereby to assist the overall computation process by decreasing the imbalance between memory speeds.

With each of the above configurations, variants are possible with alternative logic mechanizations of the associative memory. The alternatives range from devices capable of elementary searches on equality, less than or equal,

greater than or equal, maximum, minimum, etc., to devices that contain full parallel hardware, thereby permitting complex operations and extending the memory to have the capabilities of a processor.

In addition to the above interfaces, a number of designers have considered associative processors. One development in this regard is the Associative Store Processor (ASP) [LSAP65, SLAS66, SLAS67], described by Love, Savitt and Troop. The ASP machine organization provides the parallel search facilities of an associative memory plus inter-cell communication. The dominant element in the ASP machine organization is the context-addressed memory. This memory stores both data and programs and is intended to provide the ability to identify, in parallel, unknown items by specifying the context of relations in which the unknowns appear. A relatively small read-only memory is employed to store a micro-program for executing ASP instructions. However, the ASP machine organization has not reached a hardware implementation stage. An interpreter [SLAS68] has been implemented for the IBM 360 family of computers to simulate a portion of the ASP system.

The ILLIAC IV [BCIL68, KAA068, IUIL67], which is an outgrowth of the Solomon Computer [SBTS63, SBTS62, CGTS65], should provide extensive parallel processing capability. The ILLIAC IV is currently being implemented for the University of Illinois by the Burroughs Corporation. As noted in [BCIL68] "The nucleus of the system is the ILLIAC IV array, a matrix of 256 identical processing units, configured into four identical quadrants, each having 64 processing units under the direction of a common control unit. These array elements perform the computational tasks for the system." Each of the 256 processing elements has 2048 words of 64 bit memory. Associative processing is accomplished by performing search operations when the elements of the search field are in the same relative position in each processor. The cycle

time is 240 nanoseconds. The processing elements have a 32 bit mode where each quadrant could be considered as 128 parallel operating units. The processing elements can communicate data to form neighboring processing elements by means of routing instructions.

The complete ILLIAC IV system for the University of Illinois includes a B6500 computer to perform input/output operations and compilation, and contains an operating system. A 10^9 bit, head-per-track disk file with a 40 millisecond rotation speed provides an effective transfer rate of 10^9 bits/second. Westlund [WGAT68] has developed a timing simulator for the ILLIAC IV. The simulator, written in ALGOL, is implemented on the Burroughs B5500.

Kisylia [KAAA68] proposes an associative memory processor with distributed logic. His work is based upon the organization proposed by Lee and Paull [LPAC63]. The modification made by Kisylia lies in the construction of the memory cell and in the various modes of local communication each cell enjoys with its neighbors. Processing may take place simultaneously on three distinct levels in the machine. The hardware organization has not been implemented.

Murtha [MJHP66] has written a comprehensive and thorough article on highly parallel processing systems in which he describes associative memories and associative processors. Both hardware and software technical details of a large number of parallel processors are covered. In addition, he explains how an associative memory cell operates and describes the inter-communicating cell developed by Lee [LCIC62]. Murtha notes that, "...Probably the most ambitious hardware development is a cryogenic processor being built by Texas Instruments. It will have 5000 words of 65 bits each with a parallel read cycle time of about 10 μsec. It is expected to be operating in the fall of 1966." As of the time period covered by this article, this author is not aware

that the memory has been delivered to the sponsors, Rome Air Development Center (RADC).

Knapp [KMRP67] describes work sponsored by the Rome Air Development Center (RADC) in associative memory technology. In 1967 RADC was sponsoring the following hardware associative memory developments: an Associative List Selector (ALS) that implements a fast hash addressing scheme, is under development by Goodyear Aerospace Corporation [GBAL66]; a 120-bit 2350 cryotion associative processor plane is being fabricated by Texas Instruments, Incorporated [PJFA65, RGCA64]; a breadboard model of an associative memory that uses ferroelectric and photoconductor elements has been developed by the Marquardt Corporation [HBED66, HBAT65]; techniques for fabricating distributive logic and memory networks using monolithic chips, wafers and individual minature component elements are under development by the Westinghouse Aerospace Division [TRFT66]; and an associative memory array using enhancement insulated-gate complementary, thin-film field-effect transistor has been developed and partially tested by RCA under Contract AF30(602)-2718.

All of the above hardware organizations have permitted both the reading and the writing of data from and to an associative memory. Fixed or semi-permanent stores have been used as content-addressable memories. Goldberg and Green [GGLF61] have reported upon a fixed content-addressable memory that involves the use of permanent wiring of information in an array of linear cores. Lewin, et al [LBFR65] have developed a fixed content-addressable memory where electronic punched cards are used as the storage medium. Lewis [LMAS65] has written a thorough survey of fixed memories for both content and conventional memories. Read-only memories are useful when one has encyclopedic information not subject to change, but they are not useful when the data base is subject to change.

3.4 Software Simulation of Associative Memories

In addition to the simulation of an associative processor, ASP [SLAS68], attempts have been made to simulate associative memory properties via software techniques. Feldman [FJA065], using a hash code to access entries in a table, basically simulates the exact match capabilities of an associative memory. The data accessed is organized in a ring data structure. His approach is very useful for systems that do not require the full capabilities of an associative memory (i.e., the ability to interrogate the entire memory on any combination of bits within a word, rather than on only an exact match). Rovner [RPAI66] has modified the hash code concept to organize the data where it exceeds the capacity of core. In this modification a two-level data store consisting of core and drum is required. Rovner develops a scheme for a paged software-simulated associative memory. Again, only the exact match is considered. Hilbing [HFTA68] also considers paged associative memory systems. Ash, et al [ASTA67] have used Feldman's approach to organize data for a question-answering system under development. The system is called TRAMPS. Rovner and Feldman [RFTL68, FRAA68] have developed an associative language called LEAP to facilitate programming their simulated associative processor. LEAP is an extension of ALGOL to include associations, sets and a number of auxiliary constructs. LEAP is a family of languages; each language adds a different set of features, to the ALGOL base. Forms of LEAP contain matrix operations, property sets, and on-line graphics [FRAA68, RPAA68]. Gall and Brotherton [BGAL66], describe an Associative List Selector (ALS) hardware device with capabilities similar to those of the associative memory that Rovner and Feldman are working out through a software simulation. The ALS is a hardware implementation of hash addressing to give a fast search capability on equality.

4. Software Studies

The area of software for associative memories has by and large been neglected. Falkoff [FAAF62], using Iverson's notation, has developed numerous algorithms for associative memories. Estrin and Fuller [EFAF63] have also described algorithms for associative memories. They further note that content-addressable memories are more flexible than list structures since, within a list structure, data is ordered with respect to predecessors and successors of elements on a list. However, in a content-addressable memory, data sets are unordered. Lewin [LMR062] has developed an elegant technique requiring two sense outputs for each digit of the word and requiring 2m-1 cycles for the complete readout of m words that match the interrogation bit configuration. The time is a function of the number of multiple matches and is not a function of the size of the associative store. A new proof of Lewin's result has been developed by Wolinsky [WAAS68].

Dugan, et al [DGAS66] note that several macro type instructions are required for dealing with several classes of data in an associative memory. They describe a routine called SPO that saves all response stores and status (busy) bits and "deactivates" that AM segment not defined by SPO. Other macros noted were NGT (to find the value of a data word from a list which is next greater than the comparand), AND (to find the conjunction of two lists of data words), and an executive type routine, DISPATCHER, that handles the problem of data loads to the associative memory. They note that programming for associative memories is "difficult to learn because associative configurations are conceptually different from other configurations". Green, et al [GMA066] expand upon the implications of associative processing for programmers reported by Dugan.

There are several hardware features that could help the software manipulative

problem. Bird, et al [BCSO66] note that a multi-write capability that permits one to write simultaneously into memory registers is important for associative manipulation. Dugan, et al [DGAS66] note that the ability to retain and to manipulate tag bits in a word and to perform indirect addressing or index modifications of associative instructions for associative memory locations are important hardware features required by software personnel.

5. Summary

Associative memory hardware technology has not yet come of age. After more than twelve years of effort in the field, only experimental hardware or small memories exist. Simulation solutions have yet to include the full capability of associative memories. Software studies indicate that programming associative memories is complex and that much more work is required in this area. Although the associative property is useful, manipulating associatively stored data may be complex.

Two application areas that look promising for associative memories are those of control operations and question-answering systems. A survey of question-answering systems is provided by Simmons [SRAE65]. More recent work is provided in [KCNL68, WWPS68, SBAC68, GRTU68].

No one has yet completed a study that conclusively shows that associative memories or processors in a computer environment are clearly better than a conventional memory. For the types of problems he considers, Feldman [FJA065] notes that a simulation of an associative memory on conventional hardware is competitive with the hardware approach.

It is clear that the promise of associative or content-addressable memories has not materialized. Much work remains to be done to achieve large data stores of associative memories. The software approaches to achieve associative capabilities will become increasingly important as associative hardware continues to remain limited. More quantitative studies, rather than speculative studies, are required to determine the precise advantages or disadvantages of associative memory technology.

As may be seen from the size of this bibliography, the literature in associative memory technology continues to grow rapidly. It is hoped that future studies will provide further insight into the prospects for this technology.

Preface to KWIC* Index

The bibliography consists of two parts. The first part is the Key Word In Context (KWIC) Index which lists the titles sorted according to index words selected from the title. Preceding each title is a six-character code. The coding scheme (devised by the late H. P. Luhn who developed one of the first KWIC indexes) is composed by taking the first character of the author's last name, the first character of his first name, the first character of the first and second words of the title, and the date of the article. A slight modification of the code applies for multiple authors, corporate authors and other non-standard situations. The second part of the bibliography consists of the citations themselves sorted according to the coding scheme. In addition to the citation, the computer review number is provided whenever the article has been reviewed in Computing Reviews. The citation appears only once in the second part of the bibliography even though there may be multiple authors. References in the text are specified in terms of the code.

The bibliography has been accumulated over several years starting in 1963. Among the journals covered in the bibliography are the Joint Computer Conferences, Association for Computing Machinery publications and Defense Documentation Center publications. Other journals have also been searched in accumulating the bibliography. Two searches of the Defense Documentation Center holdings were requested: search control No. 001550 and 101547 October 7, 1968. Wherever possible, patents concerning associative memory developments have been included.

*The Key Word In Context Index (KWIC) program used was developed by Mr. J. Gary Augustson and Mr. Arnold Miller of the University of Maryland Computer Science Center for the UNIVAC 1108 computer.

****KWIC INDEX****

NAAT65	REASONANT	ABSORPTION	NON-DESTRUCTIVE READ-OUT TECHNIQUE.=A THIN MAGNETIC FILM COMPUTER MEMORY USING
PSAA67	AN	ABSTRACT	PARALLEL PROCESSING SYSTEM.=
CRAM69	CIATIVE MEMORY	ACCEPTORS	=ASSO
FRVT69	OPOLOGY RANDOM	ACCESS	MEMORY ORGANIZATIONS=VARIABLE T
WRAT	MULTIPLE-WORD	ACCESS	MEMORIES.=A TRANSISTOR-TUNNEL DIODE CELL FOR ASSOCIATIVE MEMORIES AND
NECS67	LLS FOR RANDOM	ACCESS	MEMORIES.=CRYOTRON STORAGE CE
FRVT69	OPOLOGY RANDOM	ACCESS	MEMORY ORGANIZATIONS.=VARIABLE T
MHIO62	OF STORAGE AND	ACCESS	TECHNIQUES SUITABLE FOR USE IN LARGE-CAPACITY DIGITAL MEMORIES. =INVESTIGATION
NSFI61	STORAGE AND	ACCESS	TECHNIQUES.=FUNDAMENTAL INVESTIGATION OF DIGITAL COMPUTER
LAAA61	REDUCE THE	ACCESS	TIME FOR INSTRUCTIONS IN LOOPS.=AN APPLICATION FOR A SMALL, FAST ASSOCIATIVE M
HGGR67	QUASI-RANDOM	ACCESS	MEMORY SYSTEM.=
BLCR65	LECTRIC RANDOM	ACCESS	MEMORY, PHASE 3.=CRYOE
BACR66	LECTRIC RANDOM	ACCESS	MEMORY - PHASE 3.=CRYOE
NDCS65	ING FOR RANDOM	ACCESS	MEMORIES.=CONTINUOUS SHEET SENS
BBCR64	LECTRIC RANDOM	ACCESS	MEMORY, PHASE 2 10 (9) BIT MEMORY.=CRYOE
NVCA65	CRYOGENICS -	ACHIEVEMENT	AND POTENTIAL.=
FRAL67		ACHIEVING	LARGE SCALE COMPUTING CAPABILITIES THROUGH ASSOCIATIVE PARALLEL PROCESSING=
FRAL		ACHIEVING	LARGE COMPUTING CAPABILITIES THROUGH ASSOCIATIVE PARALLEL PROCESSING.=
SDAL		ACHIEVING	LARGE COMPUTING CAPABILITIES THROUGH AN ARRAY COMPUTER.=
GJBT60	, SIMULTANEOUS	ACTION	=BINARY TESTS FOR TWO TERMINAL
BRAA69	EALIZATION FOR	ACTIVE	SONAR SIGNAL PROCESSING.=AN ASSOCIATIVE MEMORY PARALLEL DELTIC R
MEMO67	MS - CYCLIC TO	ACYCLIC	GRAPH TRANSFORMATIONS.=MODELS OF COMPUTATIONAL SYSTE
KMSP64	HASIS ON	ADAPTATION	TO USE THROUGH MAN-MACHINE INTERACTION.=SOME PROBLEMS IN INFORMATION SCIENCE W
MCAT63		ADAPTIVE	THRESHOLD LOGIC.=
ACTC65	CTION OF AN	ADAPTIVE	MAN-MACHINE ASSOCIATIVE MEMORY FOR INFORMATION RETRIEVAL.=TOWARDS CONTROLLED E
KMAM62		ADAPTIVE	MECHANISMS IN DIGITAL ' CONCEPT ' PROCESSING. =
WDCA68	Y DESIGN USING	ADAPTIVE	AND ASSOCIATIVE TECHNIQUES.=COMPUTER-AIDED STRATEG
EVCA62	CORRECTION AND	ADDENDUM	=CORREC
YYAN66	A NONBULK	ADDITION	TECHNIQUE FOR ASSOCIATIVE PROCESSORS.=
ISSB56	SORTING BY	ADDRESS	CALCULATION.=
SGAO64	ASSOCIATIVELY	ADDRESS	DISTRIBUTED MEMORY.=APPLICATION OF AN
FESA63	NS FOR CONTENT	ADDRESSABLE	MEMORIES=SOME APPLICATIO=
PRAI69	RATORY CONTENT	ADDRESSABLE	MEMORY SYSTEM.=AN IMPROVED FIELD-CONTROLLED POLARIZATION-TRANSFER DEVICE AND T
FRCA63	CONTENT	ADDRESSABLE	MEMORY SYSTEMS.=
LCCA68	CONTENT	ADDRESSABLE	AND DISTRIBUTED LOGIC MEMORIES. =
HJAC67	A CONTENT	ADDRESSABLE	MEMORY WITH APPLICATIONS TO MACHINE TRANSLATION.=
LPAC64	A CONTENT	ADDRESSABLE	DISTRIBUTED LOGIC MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=
BRCA66	CONTENT	ADDRESSABLE	MEMORY.=
BRCA66	CONTENT	ADDRESSABLE	MEMORY.=
BRCA67	CONTENT	ADDRESSABLE	MEMORIES.=
SLPC65	ANEL : CONTENT	ADDRESSABLE	MEMORIES.=P
LPAC63	A CONTENT	ADDRESSABLE	DISTRIBUTED LOGIC MEMORY WITH APPLICATION TO INFORMATION RETRIEVAL.=
CDCA65	CONTENT	ADDRESSABLE	MEMORY SYSTEMS CONCEPTS.=
IBTA66	TAG	ADDRESSED	MEMORY.=
LSAM63	GNETIC CONTENT	ADDRESSED	MEMORY.=ALL MA
GJAI63	INTRINSICALLY	ADDRESSED	PROCESSING SYSTEM.=AN
GECA67	CONTENT	ADDRESSED	MEMORY.=
SRCA67	CONTENT	ADDRESSED	MEMORY.=
NFAC62	CRYOGENIC DATA	ADDRESSED	MEMORY.=A
LMRO62	FROM A CONTENT	ADDRESSED	MEMORY.=RETRIEVAL OF ORDERED LISTS
NFDA62	DATA	ADDRESSED	MEMORY USING THIN-FILM CRYOTRONS.=
EFMA64	MULTIPLE	ADDRESSING	FOR FIXED-TAG ASSOCIATIVE MEMORIES.=
RRTA67	CIATIVE MEMORY	ADDRESSING	=TRANSLATED ASSO
NAAN62	E OF SCRAMBLED	ADDRESSING	FOR ASSOCIATIVE MEMORIES.=A NOTE ON THE US
PHCA62	CONTENT	ADDRESSING	AND INFORMATION RETRIEVAL.=
PGAS64	NG CORRELATION	ADDRESSING	=A SEMIPERMANENT MEMORY UTILIZI

ERTA69	THE	ADVANCED	AVIONICS DIGITAL COMPUTER.=
IBAP62	R THE STUDY OF	ADVANCED	INFORMATION RETRIEVAL TECHNIQUES.=A PROPOSAL FO
GJTF62	TECHNIQUES FOR	ADVANCED	INFORMATION PROCESSING SYSTEM.=TECHNI
GAAG67		ADVANCED	GENERAL-PURPOSE COMPUTER ORGANIZATIONS.=
JHSO68	STUDY OF	ADVANCED	ASSOCIATIVE PROCESSOR TECHNIQUES INTERIM REPORT.=
RDAC66		ADVANCED	COMPUTER ORGANIZATION STUDY.=
PSED68	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES.=ELEMENT D
BTAC66		ADVANCED	COMPUTER ORGANIZATION.=
HBED66	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES.=ELEMENT D
HHED67	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES.=ELEMENT D
BGED67	EVELOPMENT FOR	ADVANCED	ASSOCIATIVE MEMORIES.=ELEMENT D
BFAC62		ADVANCED	COMPUTER ORGANIZATION-ADDRESSING.=
KBAI67		ADVANCES	IN MEMORY TECHNOLOGY.=
GJCD67	E FOR COMPUTER	AIDED	DESIGN : A SURVEY.=COMPOUND DATA STRUCTUR
MWTA68	E PROCESSOR IN	AIRCRAFT	CONFLICT DETECTION.=THE ASSOCIATIV
RBAB67	OLIC AND	ALGEBRAIC	MANIPULATION.=A BRIEF SURVEY OF COMPUTER LANGUAGES FOR SYMB
FRAA69	AN	ALGOL	BASED ASSOCIATIVE LANGUAGE=
FRAA68	AN	ALGOL-BASED	ASSOCIATIVE LANGUAGE.=
MRCR68	IC PROGRAMMING	ALGORITHM	ANNUAL PROGRESS REPORT.=CELLULAR REALIZATION OF THE DYNAM
LCAA61	AN	ALGORITHM	FOR PATH CONNECTIONS AND ITS APPLICATIONS.=
RRAA64	A	ALGORITHM	FOR CONCURRENT RANDOM WALKS ON HIGHLY PARALLEL MACHINES.=
ASAM67	ATH CONNECTION	ALGORITHM	=A MODIFICATION OF LEE'S P
MRPC69	STRUCTURES AND	ALGORITHMS	FOR LOGIC DESIGN PROBLEMS=PARALLEL COMPUTING
FAAF62		ALGORITHMS	FOR PARALLEL SEARCH MEMORIES.=
SJAI64		ALGORITHMS	IN PARALLEL COMPUTATION.=
MYSA69	AGE ALLOCATION	ALGORITHMS	IN THE TRANQUIL COMPILER.=STOR
EFAF63		ALGORITHMS	FOR CONTENT-ADDRESSABLE MEMORY ORGANIZATION.=
RWAM63	CIATIVE MEMORY	ALGORITHMS	AND THEIR CRYOGENIC IMPLEMENTATION.=ASSO
RJAF64		ALGORITHMS	FOR COMPLEX SEARCHES.=
FAAF62		ALGORITHMS	FOR PARALLEL SEARCH MEMORIES.=
RAMA67	MEMORY	ALLOCATION	FOR MULTIPROCESSORS=
MYSA69	STORAGE	ALLOCATION	ALGORITHMS IN THE TRANQUIL COMPILER.=
CYAO65	YNAMIC STORAGE	ALLOCATION	=APPLICATION OF CONTENT-ADDRESSED MEMORY FOR D
RHOT69	LEMENTATION OF	AMBIT/G	: A GRAPHICAL PROGRAMMING LANGUAGE.=ON THE IMP
RPAA68	AN	AMBIT/G	PROGRAMMING LANGUAGE IMPLEMENTATION.=
CDAM66		AMDRIVE*	AND CODAP - ASSOCIATIVE MEMORY ASSEMBLER.=
FNUM	SING LANGUAGE,	AMPPL-II	=USER'S MANUAL FOR THE ASSOCIATIVE MEMORY, PARALLEL PROCES
FMOA69	LLEL LANGUAGE,	AMPPL-II	=ON A NEW TOOL IN ARTIFICIAL INTELLIGENCE RESEARCH : AN ASSOCIATIVE MEMORY, PA
BHAM65	E MEMORY USING	ANALOG	SUMMING TECHNIQUE.=ASSOCIATIV
WDPN64	) APPLICATIONS	ANALYSES	=PARALLEL NETWORK COMPUTER (SOLOMON
VITA69	THE	ANALYSIS	OF THE CRYOTRONIC ASSOCIATIVE ELEMENT CONTROLLED BY MONOPOLAR CURRENTS.=
BWAA69		ANALYSIS	AND SYNTHESIS OF CONTROL MECHANISMS FOR PARALLEL PROCESSES.=
HFTA68	THE	ANALYSIS	OF STRATEGIES FOR PAGING A LARGE ASSOCIATIVE DATA STRUCTURE.=
BAAO66		ANALYSIS	OF PROGRAMS FOR PARALLEL PROCESSING.=
GRPS63	EM SEARCH TIME	ANALYSIS	=PRELIMINARY SYST
FRAA64	AN	ANALYSIS	OF THE MULTIPLE INSTANTANEOUS RESPONSE FILE.=
GMAO66		ANALYSIS	OF SMALL ASSOCIATIVE MEMORIES FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=
GMAO66		ANALYSIS	OF SMALL ASSOCIATIVE MEMORIES FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=
ENAO65		ANALYSIS	OF THE CRYOGENIC CONTINUOUS FILM MEMORY.=
RPMP63	L PULSE-HEIGHT	ANALYZER	APPLICATION OF AN ASSOCIATIVE PROGRAMMED COMPUTER.=MULTIDIMENSIONA
SBDR65	NG MEGACHANNEL	ANALYZER	THROUGH ASSOCIATIVE PROGRAMMING OF A SMALL COMPUTER.=DIRECT-RECORDI
BHIL65	ESCRIPTION AND	ANNOTATED	BIBLIOGRAPHY.=ILLIAC-II - A SHORT D
ABAS64		ANNUAL	SUMMARY REPORT OF INVESTIGATION IN DIGITAL TECHNOLOGY RESEARCH.=
MRCR68	NG ALGORITHM,	ANNUAL	PROGRESS REPORT.=CELLULAR REALIZATION OF THE DYNAMIC PROGRAMMI
RIMO67	A MULTIVALENT	ANSWER	FROM ASSOCIATIVE MEMORY.=METHODS OF SELECTING
GYOR65	ULTI-COMPONENT	ANSWER	FROM ASSOCIATIVE MEMORY.=ORDERED RETRIEVAL OF A M
BHAM62	Y USE OF	ANTENNA	PROPAGATION CONCEPTS.=A MACHINE FOR PERFORMING VISUAL RECOGNITION B

YHD064	NSE FILE : THE	AN/GSQ-81	DOCUMENT DATA INDEXING SET.=DEVELOPMENT OF A MULTIPLE INSTANTANEOUS RESPO
DBAP67		APL	- ASSOCIATIVE PROGRAMMING LANGUAGE USER'S MANUAL.=
DGAA66		APL	- A LANGUAGE FOR ASSOCIATIVE DATA HANDLING IN PL/I.=
RFST64	DETERMINE THE	APPLICABILITY	OF THE SOLOMON COMPUTER TO COMMAND AND CONTROL.=STUDY TO
RFST64	DETERMINE THE	APPLICABILITY	OF THE SOLOMON COMPUTER TO COMMAND AND CONTROL. VOLUME I. INFORMATION STORAGE,
KAA069		APPLICATION	OF ILLIAC-IV TO URBAN DEFENSE RADAR PROBLEM.=
SEAA61	PROCEDURE WITH	APPLICATION	TO PARALLEL PROGRAMMING.=AN AUTOMATIC SEQUENCING
KJA063		APPLICATION	OF A PARALLEL-SEARCH MEMORY.=
KDIL68	V SOFTWARE AND	APPLICATION	PROGRAMMING.=ILLIAC-I
RPMP63	EIGHT ANALYZER	APPLICATION	OF AN ASSOCIATIVE PROGRAMMED COMPUTER.=MULTIDIMENSIONAL PULSE-H
LAAA61	AN	APPLICATION	FOR A SMALL, FAST ASSOCIATIVE MEMORY TO REDUCE THE ACCESS TIME FOR INSTRUCTION
CMS064	CIATIVE MEMORY	APPLICATION	=STUDY OF ASSO
CCA0		APPLICATION	OF ASSOCIATIVE MEMORIES TO THE WEAPON ASSIGNMENT PROBLEM OF NTDS.=
CYA065		APPLICATION	OF CONTENT-ADDRESSED MEMORY FOR DYNAMIC STORAGE ALLOCATION.=
HRA0		APPLICATION	OF CRYOGENIC TECHNIQUES TO COMPUTER TECHNOLOGY.=
NBAI60	YOTRON AND ITS	APPLICATION	TO DIGITAL COMPUTERS.=AN IMPROVED FILM CR
KAA068		APPLICATION	OF ILLIAC-IV TO URBAN DEFENSE RADAR PROBLEM.=
LPAC63	Y WITH	APPLICATION	TO INFORMATION RETRIEVAL.=A CONTENT ADDRESSABLE DISTRIBUTED LOGIC MEMOR
NBTC60	YOTRON AND ITS	APPLICATION	TO DIGITAL COMPUTERS.=THE CROSSED-FILM CR
SGA064		APPLICATION	OF AN ASSOCIATIVELY ADDRESS DISTRIBUTED MEMORY.=
FBAA65	PROCESSOR WITH	APPLICATION	TO PICTURE PROCESSING.=AN ASSOCIATIVE PARALLEL
CWA067		APPLICATION	OF PARALLEL PROCESSING TO NUMERICAL WEATHER PREDICTION.=
HIPP70	HNOLOGIES, AND	APPLICATIONS	=PARALLEL PROCESSOR SYSTEMS, TEC
FESA63	SOME	APPLICATIONS	FOR CONTENT ADDRESSABLE MEMORIES=
CCAM65	SELECTED NAVAL	APPLICATIONS	=ASSOCIATIVE MEMORY COMPUTER SYSTEM : DESCRIPTION AND
FCAM61	CIATIVE MEMORY	APPLICATIONS	FOR INTELLIGENCE DATA PROCESSING.=ASSO
LCAA61	CTIONS AND ITS	APPLICATIONS	=AN ALGORITHM FOR PATH CONNE
AEA062		APPLICATIONS	OF CRYOTRONS TO THE HIGH-SPEED COMPUTER.=
IBS063	STUDY OF THE	APPLICATIONS	OF PARALLEL SEARCH MEMORIES.=
HJAC67	LE MEMORY WITH	APPLICATIONS	TO MACHINE TRANSLATION.=A CONTENT ADDRESSAB
LPAC64	Y WITH	APPLICATIONS	TO INFORMATION RETRIEVAL.=A CONTENT ADDRESSABLE DISTRIBUTED LOGIC MEMOR
CJOA67	GANIZATION AND	APPLICATIONS	OF ASSOCIATIVE FILE PROCESSORS.=OR
FJAM61	CIATIVE MEMORY	APPLICATIONS	IN INTELLIGENCE DATA PROCESSING.=ASSO
GAA063		APPLICATIONS	OF PARALLEL SEARCH MEMORIES.=
YCAM66	TEMS AND THEIR	APPLICATIONS	TO PICTURE AND ARITHMETIC PROCESSES.=ASSOCIATIVE MEMORY SYS
VRPF67	E OF CRYOGENIC	APPLICATIONS	=PREDICTIONS FOR FUTUR
SEAC64	Y WITH	APPLICATIONS	TO INFORMATION RETRIEVAL.=A CONTENT-ADDRESSABLE DISTRIBUTED LOGIC MEMOR
PJST66	TECHNOLOGY AND	APPLICATIONS	=SUPERCONDUCTING THIN-FILM
WDPN64	ER (SOLOMON)	APPLICATIONS	ANALYSES.=PARALLEL NETWORK COMPUT
HPAM65	SELECTED NAVAL	APPLICATIONS	=ASSOCIATIVE MEMORY COMPUTER SYSTEM DESCRIPTION AND
EFSA63	SOME	APPLICATIONS	FOR CONTENT-ADDRESSABLE MEMORIES.=
LSAP66	PROCESSING AS	APPLIED	TO MULTI-PREFORMED BEAM SONAR SYSTEMS.=ASSOCIATIVE PARALLEL
NVAS64		APPLIED	SUPERCONDUCTIVITY.=
ADAD61	A DELAY LINE	APPROACH	TO ASSOCIATIVE MEMORY.=
SDAP67	LLEL COMPUTING	APPROACH	TO DIGITAL SIMULATION.=A PARA
STGS68	TIVE MEMORY	APPROACH	=GRAPHICAL SYSTEMS COMMUNICATIONS : AN ASSOCIA
PJAA65	AN	APPROACH	TO PARALLEL PROCESSING.=
HTSO69	LLEL PROCESSOR	APPROACHES	AND TECHNIQUES.=SURVEY OF PARA
CAOT68	CE OF DISCRETE	APPROXIMATIONS	TO THE NAVIER STOKES EQUATIONS.=ON THE CONVERGEN
HJAU69	F EXECUTING AN	ARBITRARY	NUMBER OF SUB-PROGRAMS SIMULTANEOUSLY.=A UNIVERSAL COMPUTER, CAPABLE O
LGTA70	THE	ARCHITECTURE	OF A LARGE ASSOCIATIVE PROCESSOR=
LGTA69	THE	ARCHITECTURE	OF A LARGE DISTRIBUTED LOGIC ASSOCIATIVE PROCESSOR=
LGTA69	THE	ARCHITECTURE	OF A LARGE DISTRIBUTED LOGIC, ASSOCIATIVE MEMORY=
DJPG68	TER	ARCHITECTURE	=PROGRAMMING GENERALITY, PARALLELISM AND COMPU
LWSA68	SOME	ARGUMENTS	FAVORING NON-CONVENTIONAL TYPES OF COMPUTERS.=
YCAM66	TO PICTURE AND	ARITHMETIC	PROCESSES.=ASSOCIATIVE MEMORY SYSTEMS AND THEIR APPLICATIONS
BBCO68	COMPILATION OF	ARITHMETIC	EXPRESSIONS FOR PARALLEL COMPUTATIONS.=COMPIL

HMCS60	OTRON STORAGE,	ARITHMETIC	AND LOGICAL CIRCUITS.=CRY
PAAC70	OUGH	ARRAY	ORGANIZATION=ASSOCIATIVE CAPABILITIES FOR MASS STORAGE THR
KRMA62	MEMORY	ARRAY	SEARCHING SYSTEM.=
SDAL	IES THROUGH AN	ARRAY	COMPUTER.=ACHIEVING LARGE COMPUTING CAPABILIT
SSCO65	GANIZATION FOR	ARRAY	PROCESSING.=COMPUTER OR
KWCL69	OGIC-IN-MEMORY	ARRAYS	=CELLULAR L
KLCI68	NTERCONNECTION	ARRAYS	=CELLULAR I
HFIA61	ITERATIVE	ARRAYS	OF LOGIC CIRCUITS.=
EKPO67	ES OF CELLULAR	ARRAYS	FOR LOGIC AND STORAGE.=PROPERTI
LBFA63	ANIC DIODE	ARRAYS	=FIXED ASSOCIATIVE MEMORY USING EVAPORATED ORG
WPST66	: SELECTED	ARTICLES	=SCIENTIFIC TECHNICAL INFORMATION NO. 6, 1964
SJPD64	TE THE PATTERN	ARTICULATION	UNIT OF ILLIAC-III.=PROGRAM DESCRIPTION OF PAX AN IBM 7090 PROGRAM TO SIMULA
SJUM64	E THE PATTERN	ARTICULATION	UNIT OF ILLIAC-III.=USER'S MANUAL FOR PAX AN IBM 7090 PROGRAM TO SIMULAT
FMOA69	A NEW TOOL IN	ARTIFICIAL	INTELLIGENCE RESEARCH : AN ASSOCIATIVE MEMORY, PARALLEL LANGUAGE, AMPPL-II.=ON
GLRM69	IV ASSEMBLER	ASK	=REFERENCE MANUAL FOR ILLIAC-
AWAC68	OMPILER FOR AN	ASSOCIATIVE	OBJECT MACHINE=A C
LHTA69	THE	ASP	- DYNABIT SYSTEM : AN ASSOCIATIVE PROCESSOR USING BULK STORAGE.=
LRAU68		ASP	USERS MANUAL . ASSOCIATION-STORING PROCESSOR INTERPRETER PROGRAM.=
LGAS68		ASP	- A RING IMPLEMENTED ASSOCIATIVE STRUCTURE PACKAGE.=
SLAS67		ASP	: A NEW CONCEPT IN LANGUAGE AND MACHINE ORGANIZATION.=
SLAS68		ASP	USER'S MANUAL ASSOCIATION-STORING PROCESSOR INTERPRETER PROGRAM.=
MTCA60	COMBINATORIAL	ASPECTS	OF INFORMATION RETRIEVAL.=
FJAO65		ASPECTS	OF ASSOCIATIVE PROCESSING.=
SRSA65	D RETRIEVAL OF	ASPECTS	OF MEANING IN DIRECTED GRAPH STRUCTURES.=STORAGE AN
GMEA65	ND THEORETICAL	ASPECTS	OF THE SUPERCONDUCTING CONTINUOUS FILM STORE.=EXPERIMENTAL A
GLRM69	FOR ILLIAC-IV	ASSEMBLER	ASK.=REFERENCE MANUAL
CDAM66	CIATIVE MEMORY	ASSEMBLER	=AMDRIVE* AND CODAP - ASSO
CCAO	TO THE WEAPON	ASSIGNMENT	PROBLEM OF NTDS.=APPLICATION OF ASSOCIATIVE MEMORIES
TRAO63		ASSIGNMENT	OF INVENTORY OF A VARIABLE STRUCTURE COMPUTER.=
MDTA66	THE AUTOMATIC	ASSIGNMENT	AND SEQUENCING OF COMPUTATIONS ON PARALLEL PROCESSOR SYSTEMS.=
BGAL66		ASSOCIATED	LIST SELECTOR =
FTAP65	EN PLATED-WIRE	ASSOCIATED	MEMORY.=A WOV
SHRO63	E ELEMENTS AND	ASSOCIATED	CIRCUITS.=RESEARCH ON BIAX TYP
SLAS68		ASSOCIATION	STORING PROCESSOR INTERPRETIVE PROGRAM - PROGRAM LOGIC MANUAL.
RRAS69		ASSOCIATION	STORING PROCESSOR INTERPRETIVE PROGRAM - PROGRAM LOGIC MANUAL.
KAAA68	AN	ASSOCIATION	PROCESSOR FOR INFORMATION RETRIEVAL.=
SMMO64	DO STATISTICAL	ASSOCIATION	PROCESSING.=MEMORY ORGANIZATION OF A 7090 TO
SLAS67		ASSOCIATION	STORING PROCESSOR.=
LRAU68	SERS MANUAL .	ASSOCIATION-STORING	PROCESSOR INTERPRETER PROGRAM.=ASP U
SLAS68	P USER'S MANUAL	ASSOCIATION-STORING	PROCESSOR INTERPRETER PROGRAM.=AS
SLAS66		ASSOCIATION-STORING	PROCESSOR STUDY.=
ASTA69	N INTERPRETIVE	ASSOCIATIVE	PROCESSOR WITH DEDUCTIVE CAPABILITIES=TRAMP: A
ACAM68		ASSOCIATIVE	MEMORY INVESTIGATIONS : SUBSTRUCTURE SEARCHING AND DATA ORGANIZATION =
FRAL67	THROUGH	ASSOCIATIVE	PARALLEL PROCESSING=ACHIEVING LARGE SCALE COMPUTING CAPABILITIES
WMAP69		ASSOCIATIVE	PARALLEL PROCESSING FOR THE FAST FOURIER TRANSFORM.=
WLAS70	AN	ASSOCIATIVE	MEMORY USING LARGE SCALE INTEGRATION =
TFAM68	A MAGNETIC	ASSOCIATIVE	MEMORY=
LGTA69	TRIBUTED LOGIC	ASSOCIATIVE	PROCESSOR=THE ARCHITECTURE OF A LARGE DIS
WAUI69	SIFICATION FOR	ASSOCIATIVE	MEMORIES=UNIFIED INTERVAL CLASSIFICATION AND UNIFIED 3-CLAS
GKAC	IVE	ASSOCIATIVE	MEMORIES=A CONTINOUS FILM MEMORY CELL FOR SUPERCONDUCT
GHAM68	PROCESSOR WITH	ASSOCIATIVE	CONTROL =A MULTI
SDAP71		ASSOCIATIVE	PROCESSING OF LINE DRAWINGS=
GDAH69		ASSOCIATIVE	HOLOGRAPHIC MEMORIES=
LGTA70	URE OF A LARGE	ASSOCIATIVE	PROCESSOR=THE ARCHITECT
KKAI69	AN INTEGRATED	ASSOCIATIVE	STORAGE SYSTEM =
MJAO69	AN OVERVIEW OF	ASSOCIATIVE	MEMORY OR CONTENT-ADDRESSABLE MEMORY SYSTEMS AND A KWIC INDEX TO THE LITERATUR
BCSO69	HIGH SPEED	ASSOCIATIVE	MEMORY=SILICON-ON-SAPPHIRE COMPLEMENTARY MOS CIRCUITS FOR

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IBAM65                    ASSOCIATIVE    MEMORY.=
IBAM66                    ASSOCIATIVE    MEMORY.=
DPAP64                    ASSOCIATIVE    PROCESSORS.=
CJRO64   ARCH ON FERRET   ASSOCIATIVE    MEMORY.=RESE
IBAM66                    ASSOCIATIVE    MEMORY SYSTEM.=
FKAL     LITIES THROUGH   ASSOCIATIVE     PARALLEL PROCESSING.=ACHIEVING LARGE COMPUTING CAPABI
WAAS68   HEOREM FOR       ASSOCIATIVE    MEMORIES.=A SIMPLE PROOF OF LEWIN'S ORDERED-RETRIEVAL T
RWAM63                    ASSOCIATIVE    MEMORY ALGORITHMS AND THEIR CRYOGENIC IMPLEMENTATION.=
STFS61   OR A CRYOGENIC   ASSOCIATIVE    MEMORY.=FEASIBILITY STUDY F
ASTA67   MEMORY WITH AN   ASSOCIATIVE    BASE.=TRAMP : A RELATIONAL
RPAI66   ATED             ASSOCIATIVE    MEMORY SYSTEM.=AN INVESTIGATION INTO PAGING A SOFTWARE-SIMUL
YCAM66                    ASSOCIATIVE    MEMORY SYSTEMS AND THEIR APPLICATIONS TO PICTURE AND ARITHMETIC PROCESSES.=
CVTU67   -OUT-OF-N ' IN   ASSOCIATIVE    MEMORIES.=THE USE OF CODES ' M
SAAD64    DISCUSSION OF   ASSOCIATIVE    MEMORIES FROM A DEVICE POINT OF VIEW.=A
RDAM67                    ASSOCIATIVE    MEMORY CELL.=
WDCA68    AND             ASSOCIATIVE    TECHNIQUES.=COMPUTER-AIDED STRATEGY DESIGN USING ADAPTIVE
ACTC65   VE MAN-MACHINE   ASSOCIATIVE    MEMORY FOR INFORMATION RETRIEVAL.=TOWARDS CONTROLLED EXPERIMENTS IN THE CONSTR
PSED68   T FOR ADVANCED   ASSOCIATIVE    MEMORIES.=ELEMENT DEVELOPMEN
STCA64        COMPUTER    ASSOCIATIVE    MEMORY STUDY.=
YYAC66   POINT CELLULAR   ASSOCIATIVE    MEMORY.=A CUT
STSP65   SEMI-PERMANENT   ASSOCIATIVE    STORE.=SEMI-P
SLAM62                    ASSOCIATIVE    MEMORY WITH ORDERED RETRIEVAL.=
ADAD61   NE APPROACH TO   ASSOCIATIVE    MEMORY.=A DELAY LI
SGAM63   L MODEL FOR AN   ASSOCIATIVE    MEMORY.=A MATHEMATICA
RRTA67       TRANSLATED   ASSOCIATIVE    MEMORY ADDRESSING.=
AKAI68    AN INTEGRATED   ASSOCIATIVE    MEMORY MATRIX.=
YFCA62      CIRCULATING   ASSOCIATIVE    MEMORIES.=
PGML62   LIST ORGANIZED   ASSOCIATIVE    MEMORY.=MULTI-
AKAM68                    ASSOCIATIVE    MEMORY IN LARGE COMPUTER SYSTEM.=
CVOR67   FROM A DECIMAL   ASSOCIATIVE    MEMORY.=ORDERED RETRIEVAL
PGTO62   ULTI-LIST TYPE   ASSOCIATIVE    MEMORY.=THE ORGANIZATION OF A M
BCAM67                    ASSOCIATIVE    MEMORIES IN NUCLEAR PHYSICS.=
TRCA64        COMPUTER    ASSOCIATIVE    MEMORY STUDY.=
PWDO64   IGN OF A FULLY   ASSOCIATIVE    CRYOGENIC DATA PROCESSOR.=DES
BRAL68   LY-DISTRIBUTED   ASSOCIATIVE    MEMORY NETWORK.=A LOCAL
SWAM63                    ASSOCIATIVE    MEMORY TECHNIQUES FOR LARGE DATA PRO
YCPR66   OGNITION BY AN   ASSOCIATIVE    MEMORY.=PATTERN REC
YTAC67      A CRYOGENIC   ASSOCIATIVE    MEMORY.=
WROA64            ON AN   ASSOCIATIVE    MEMORY FOR NEBULA COMPUTER.=
RFAA67              AN    ASSOCIATIVE    PROCESSING SYSTEM FOR CONVENTIONAL DIGITAL COMPUTERS.=
RCAM66                    ASSOCIATIVE    MEMORY.=
PGAR63   ARALLEL SEARCH   ASSOCIATIVE     MEMORY.=A READ-ONLY MULTI-MEGABIT P
RJCA64        CRYOGENIC   ASSOCIATIVE    MEMORY RESEARCH.=
PLTM61   , PART 1 : THE   ASSOCIATIVE    MEMORY.=THE MULTI-LIST SYSTEM
YCAS64   DY OF CRYOTRON   ASSOCIATIVE    MEMORY IN DIGITAL SYSTEMS.=A STU
RDAM65                    ASSOCIATIVE    MEMORIES AND INFORMATION RETRIEVAL. =
SRCA60        CRYOGENIC   ASSOCIATIVE    MEMORY.=
SRSM61   LATION WITH AN   ASSOCIATIVE    MEMORY.=SYMBOL MANIPU
YYPR66   ITION USING AN   ASSOCIATIVE    MEMORY.=PATTERN RECOGN
SIAL63                    ASSOCIATIVE    LOGIC FOR HIGHLY PARALLEL SYSTEMS.=
SRAS67                    ASSOCIATIVE    SEARCH MEMORY STUDY.=
SHAP68                    ASSOCIATIVE    PROCESSING FOR GENERAL PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES.
RRAO62   NIZATION OF AN   ASSOCIATIVE    CRYOGENIC COMPUTER.=AN ORGA
GMAO66   LYSIS OF SMALL   ASSOCIATIVE    MEMORIES FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=ANA
YYAC66      A CRYOGENIC   ASSOCIATIVE    MEMORY SYSTEM FOR INFORMATION RETRIEVAL.=
BGED67   T FOR ADVANCED   ASSOCIATIVE    MEMORIES.=ELEMENT DEVELOPMEN
ABCA64        CRYOGENIC   ASSOCIATIVE    MEMORY TECHNIQUES.=
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DPDF63	DESIGN FOR AN	ASSOCIATIVE	COMPUTER.=
IBAM66		ASSOCIATIVE	MEMORY.=
FRAP67		ASSOCIATIVE	PARALLEL PROCESSING.=
IBAM67		ASSOCIATIVE	MEMORY.=
IBAM65		ASSOCIATIVE	MEMORY SYSTEM.=
CMSO64	STUDY OF	ASSOCIATIVE	MEMORY APPLICATION.=
CCSO64	VESTIGATION ON	ASSOCIATIVE	MEMORIES.=SUMMARY OF IN
EFMA64	FOR FIXED-TAG	ASSOCIATIVE	MEMORIES.=MULTIPLE ADDRE
BCAM66		ASSOCIATIVE	MEMORY.=
IYAI	MOS TRANSISTOR	ASSOCIATIVE	MEMORY WITH 100-NANOSECONDS CYCLE TIME.=AN INTEGRATED
CATK62	3-K BIT	ASSOCIATIVE	MEMORY WORKS AT ROOM TEMPERATURE.=
GRHA66	HYBRID	ASSOCIATIVE	COMPUTER STUDY.=
GYCR65	FROM	ASSOCIATIVE	MEMORY.=ORDERED RETRIEVAL OF A MULTI-COMPONENT ANSWER
BJAS61	ANENT MAGNETIC	ASSOCIATIVE	MEMORY AND CODE CONVERTER.=A SEMI-PERM
GEAM67		ASSOCIATIVE	MEMORY.=
IKAH66	150-NANOSECOND	ASSOCIATIVE	MEMORY USING INTEGRATED MOS TRANSISTORS.=A
HPEC	N CRITERIA FOR	ASSOCIATIVE	MEMORIES.=EVALUATIO
FAPS60	SYSTEM USING	ASSOCIATIVE	STORAGE.=PROGRAM SEQUENCE CONTROL IN A MULTIPROCESSING
IBAM65		ASSOCIATIVE	MEMORY.=
BDPP66	WORD	ASSOCIATIVE	MEMORY.=PRELIMINARY PROGRAMMING MANUAL FOR RADC 2048
INAP64		ASSOCIATIVE	PROCESSOR STUDY FOR RADC.=
FJAM61		ASSOCIATIVE	MEMORY APPLICATIONS IN INTELLIGENCE DATA PROCESSING.=
IBAA60	AN	ASSOCIATIVE	MEMORY USING SUPERCONDUCTIVE TECHNIQUES.=
HWSM66	LE RESPONSE IN	ASSOCIATIVE	MEMORIES AND READOUT OF THE DETECTOR MATRIX.=SIMULTANEOUS MULTIP
IBAM65		ASSOCIATIVE	MEMORY READOUT CIRCUIT.=
FSAP64		ASSOCIATIVE	PROCESSOR STUDY.=
FJAO65	ASPECTS OF	ASSOCIATIVE	PROCESSING.=
CCAO	APPLICATION OF	ASSOCIATIVE	MEMORIES TO THE WEAPON ASSIGNMENT PROBLEM OF NTDS.=APPLIC
HBSU64	OME USES OF AN	ASSOCIATIVE	MEMORY AS A REAL-TIME CONTROL.=S
DPAS62	UPERCONDUCTIVE	ASSOCIATIVE	MEMORY.=A S
JMOO64	RIEVAL FROM AN	ASSOCIATIVE	MEMORY.=ON ORDERED RET
GAAM67		ASSOCIATIVE	MEMORY.=
JKAM		ASSOCIATIVE	MEMORIES.=
GPAM		ASSOCIATIVE	MEMORY TECHNIQUES.=
CJOA67	PPLICATIONS OF	ASSOCIATIVE	FILE PROCESSORS.=ORGANIZATION AND A
IBAP64		ASSOCIATIVE	PROCESSOR.=
HBAT65		ASSOCIATIVE	TAG MEMORY.=
DGAS66	TY OF A HYBRID	ASSOCIATIVE	MEMORY PROCESSOR.=A STUDY OF THE UTILI
BFOT	UTONOMY FOR AN	ASSOCIATIVE	MEMORY.=ON THE EVOLUTION OF A
HAHA63	HUGHES	ASSOCIATIVE	MEMORY.=
FMOI61	ERATIONS IN AN	ASSOCIATIVE	MEMORY.=OP
DGAA66	A LANGUAGE FOR	ASSOCIATIVE	DATA HANDLING IN PL/I.=APL -
IBAP63		ASSOCIATIVE	PROCESSING TECHNIQUES.=
BECA67	CRYOGENIC	ASSOCIATIVE	MEMORY.=
BCSO66	STUDY OF	ASSOCIATIVE	PROCESSING TECHNIQUES.=
CKAT62	A TUNNEL DIODE	ASSOCIATIVE	MEMORY.=A TUNN
ICSO66	STUDY OF	ASSOCIATIVE	PROCESSING TECHNIQUES.=
ISSO64	SWITCHING FOR	ASSOCIATIVE	MEMORY SYSTEMS.=STUDY OF ELASTIC
FRO61	MATION WITH AN	ASSOCIATIVE	MEMORY.=RETRIEVAL OF INFOR
IIGS64	NERAL SURVEY :	ASSOCIATIVE	STORAGE FOR NUCLEAR PHYSICS.=GE
WAM64		ASSOCIATIVE	MEMORY.=
FAT66		ASSOCIATIVE	TECHNIQUES FOR CONTROL FUNCTIONS IN A MULTIPROCESSOR.=
JAH64	6-BIT MAGNETIC	ASSOCIATIVE	MEMORY.=A 128-WORD, 3
KAP67		ASSOCIATIVE	PARALLEL PROCESSING.=
ACOn2	ON OF NOTES ON	ASSOCIATIVE	MEMORY.=COLLECTI
PAM61	A MAGNETIC	ASSOCIATIVE	MEMORY.=
MLA62	FICATION OF AN	ASSOCIATIVE	MEMORY.=LOGICAL AND FUNCTIONAL SPECI

```
SLMF62    L SYSTEMS, AND    ASSOCIATIVE    LOGIC.=MASS FABRICATION, HIGHLY PARALLE
SRAP61      A PROGRAMMED    ASSOCIATIVE    MEMORY FOR USE IN COMPILING.=
YYAN66     TECHNIQUE FOR    ASSOCIATIVE    PROCESSORS.=A NONBULK ADDITION
AKAM68                      ASSOCIATIVE    MEMORIES IN LARGE COMPUTER SYSTEMS.=
SHAP69                      ASSOCIATIVE    PROCESSING FOR GENERAL PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES.
BGAM69    SSION ORIENTED    ASSOCIATIVE    PROCESSOR USING PLATED WIRE.=A MI
FTAA67                AN    ASSOCIATIVE    PROCESSOR.=
BRAS62    A SEMANTICALLY    ASSOCIATIVE    MEMORY. =A SEMA
PLFA66    WORD CRYOGENIC    ASSOCIATIVE     PROCESSOR.=FABRICATION AND TESTING OF 5000
PGTO62    MULTILIST-TYPE    ASSOCIATIVE    MEMORY.=THE ORGANIZATION OF A
RWRO64    H ON CRYOGENIC    ASSOCIATIVE    MEMORIES.=RESEARC
GPAP65                      ASSOCIATIVE    PROCESSING TECHNIQUES.=
FNUM      MANUAL FOR THE    ASSOCIATIVE    MEMORY, PARALLEL PROCESSING LANGUAGE, AMPPL-II.=USER'S
LACO62     FOR USE IN AN    ASSOCIATIVE    MEMORY.=CODING OF TREES
FTAM68        A MAGNETIC    ASSOCIATIVE    MEMORY.=
FRAA68    AN ALGOL-BASED    ASSOCIATIVE    LANGUAGE.=AN ALG
BVMO66    UDING A BUFFER    ASSOCIATIVE     MEMORY UNIT.=MODELING OF A MEMORY SYSTEM INCL
LESC63    OR CIRCUITS IN    ASSOCIATIVE    MEMORIES.=SEMI-CONDUCT
GGAP66    ORK PROCESSING    ASSOCIATIVE    MEMORY=A POSSIBLE MODEL OF A NETW
FRAP64                      ASSOCIATIVE    PROCESSOR STUDY.=
FTAA67                AN    ASSOCIATIVE    PROCESSOR.=
LAAM65                      ASSOCIATIVE    MEMORY WITH NEAREST MATCH.=
MRAC62    TWEEN LIMITS '    ASSOCIATIVE    MEMORY.=A CRYOGENIC ' BE
CBPF68    H FINDING WITH    ASSOCIATIVE.   MEMORY.=PAT
LAAA61     A SMALL, FAST    ASSOCIATIVE    MEMORY TO REDUCE THE ACCESS TIME FOR INSTRUCTIONS IN LOOPS.=AN APPLICATION FOR
BRTU68    SE OF MULTIPLE    ASSOCIATIVE    MEMORIES IN PROGRAMMING THE GROWING MACHINE.=THE U
LACA65          CRYOTRON    ASSOCIATIVE    MEMORY CELL.=
LSAP65                      ASSOCIATIVE    PROCESSING TECHNIQUES STUDY.=
GASO69    FECTIVENESS OF    ASSOCIATIVE    PROCESSOR IN AWACS.=STUDY OF MISSION EF
SRDR65    ALYZER THROUGH    ASSOCIATIVE     PROGRAMMING OF A SMALL COMPUTER.=DIRECT-RECORDING MEGACHANNEL AN
MBAM65                      ASSOCIATIVE    MEMORY STRUCTURE.=
LSAP66                      ASSOCIATIVE    PARALLEL PROCESSING AS APPLIED TO MULTI-PREFORMED BEAM SONAR SYSTEMS.=
MSUO64    ORY SYSTEMS AS    ASSOCIATIVE    MEMORIES FOR INTEGRATING STORAGE OF MULTIPARAMETER DATA BY AUTOMATIC DATA REDU
AFBI65    E CORE PER BIT    ASSOCIATIVE     ELEMENT.=BILOC - A HIGH SPEED NDRO ON
RPAA67                AN    ASSOCIATIVE    PROCESSING SYSTEM FOR CONVENTIONAL DIGITAL COMPUTERS=
CDAM66    E* AND CODAP -    ASSOCIATIVE    MEMORY ASSEMBLER.=AMDRIV
FTTS68    F A HIGH-SPEED    ASSOCIATIVE    PROCESSOR.=THE STRUCTURE O
LGAS68    NG IMPLEMENTED    ASSOCIATIVE    STRUCTURE PACKAGE.=ASP - A RT
FCDO68    OF PRIORITY IN    ASSOCIATIVE    MEMORIES.=DETERMINATION
MPAM61        A MAGNETIC    ASSOCIATIVE    MEMORY SYSTEM.=
KMRP67    DC PROGRAMS IN    ASSOCIATIVE    PROCESSING.=RA
LAAA63                AN    ASSOCIATIVE    LOCAL STORE.=
PIAM67                      ASSOCIATIVE    MEMORY FOR COLLECTION AND DISPLAY SYSTEM.=
RPMP63    ATION OF AN       ASSOCIATIVE    PROGRAMMED COMPUTER.=MULTIDIMENSIONAL PULSE-HEIGHT ANALYZER APPLIC
HETA68    PAGING A LARGE    ASSOCIATIVE     DATA STRUCTURE.=THE ANALYSIS OF STRATEGIES FOR
GAHO67    UCTIONS FOR       ASSOCIATIVE    MEMORY.=HANDBOOK OF OPERATING AND MAINTENANCE - INSTR
HAAP63    R THE STUDY OF    ASSOCIATIVE    PROCESSING TECHNIQUES.=A PROPOSAL FO
CRDA62     DIMENSION: AN    ASSOCIATIVE    MEMORY.=
GAAM67                      ASSOCIATIVE    MEMORY.=
IBAM66                      ASSOCIATIVE    MEMORY SYSTEM.=
IBHA64          HYBRID      ASSOCIATIVE    COMPUTER STUDY.=
BCAM65                      ASSOCIATIVE    MEMORY CIRCUIT.=
BPAS61                      ASSOCIATIVE    STORAGE TECHNIQUES.=
IBAM66                      ASSOCIATIVE    MEMORY SYSTEM.=
GBAL66                      ASSOCIATIVE    LIST SELECTOR.=
FKMO67    RGANIZATION IN    ASSOCIATIVE    PARALLEL PROCESSING.=MACHINE O
FBSO65          STUDY OF    ASSOCIATIVE    PROCESSING TECHNIQUES.=
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LGTA69	.	ASSOCIATIVE	MEMORY=THE ARCHITECTURE OF A LARGE DISTRIBUTED LOGIC
WCAC68	ILM DEVICE FOR	ASSOCIATIVE	MEMORIES.=A COUPLE MAGNETIC F
SPAF69	IGHLY PARALLEL	ASSOCIATIVE	PROCESSOR=A FAST, FLEXIBLE H
CRAM69		ASSOCIATIVE	MEMORY ACCEPTORS=
DSAT71		ASSOCIATIVE	TECHNIQUES IN THE SOLUTION OF DATA MANAGEMENT PROBLEMS=
FRAA69	AN ALGOL BASED	ASSOCIATIVE	LANGUAGE=AN ALG
RJTA69	THE	ASSOCIATIVE	PROCESSOR - A NEW COMPUTER RESOURCE=
WLAM70		ASSOCIATIVE	MEMORY MODELS=
FNOA67	HICH SIMULATES	ASSOCIATIVE	MEMORY AND PARALLEL PROCESSING=ON A COMPUTER LANGUAGE W
SAAS68	ILIARY STORAGE	ASSOCIATIVE	DATA STRUCTURE FOR PL/1=AUX
MZET68	ORTS TOWARD AN	ASSOCIATIVE	LEARNING INSTRUCTIONAL SYSTEM=EFF
PAAC70		ASSOCIATIVE	CAPABILITIES FOR MASS STORAGE THROUGH ARRAY ORGANIZATION=
NTAM69	A MULTIACCESS	ASSOCIATIVE	MEMORY=
SRAS60		ASSOCIATIVE	SELF-SORTING MEMORY REVISED.=
DBAP67	APL -	ASSOCIATIVE	PROGRAMMING LANGUAGE USER'S MANUAL.=
IBCA	CRYOGENIC	ASSOCIATIVE	MEMORY TECHNIQUES.=
VITA69	THE CRYOTRONIC	ASSOCIATIVE	ELEMENT CONTROLLED BY MONOPOLAR CURRENTS.=THE ANALYSIS OF
LMTF69	THIN FILM	ASSOCIATIVE	MEMORY.=
FMOA69	ARCH : AN	ASSOCIATIVE	MEMORY, PARALLEL LANGUAGE, AMPPL-II.=ON A NEW TOOL IN ARTIFICIAL INTELLIGENCE
RIMO67	NT ANSWER FROM	ASSOCIATIVE	MEMORY.=METHODS OF SELECTING A MULTIVALE
LHTA69	T SYSTEM : AN	ASSOCIATIVE	PROCESSOR USING BULK STORAGE.=THE ASP - DYNABI
BHAA62	AN	ASSOCIATIVE	MACHINE FOR DEALING WITH THE VISUAL FIELD AND SOME OF ITS BIOLOGICAL IMPLICATI
BPAH67	A HIGH-SPEED	ASSOCIATIVE	MEMORY.=
TRFS61	OR A CRYOGENIC	ASSOCIATIVE	MEMORY.=FEASIBILITY STUDY F
IYAI67	MOS TRANSISTOR	ASSOCIATIVE	MEMORY SYSTEM WITH 100 NANOSECOND CYCLE TIME.=AN INTEGRATED
RWDO65	IGN OF A FULLY	ASSOCIATIVE	CRYOGENIC DATA PROCESSOR.=DES
HIAA64	AN	ASSOCIATIVE	STORE FOR NUCLEAR PHYSICS.=
HMCS68	MPLEMENTING AN	ASSOCIATIVE	MEMORY FOR A TIME-SHARED PROCESSOR.=CONTROL STORAGE USE IN I
EETU67	THE USE OF	ASSOCIATIVE	PROCESSORS IN RADAR TRACKING AND CORRELATION.=
CCAM65		ASSOCIATIVE	MEMORY COMPUTER SYSTEM : DESCRIPTION AND SELECTED NAVAL APPLICATIONS.=
WCAM69		ASSOCIATIVE	MEMORY DEVICE 3466631.=
RMAM62		ASSOCIATIVE	MEMORIES AND THE ONE LEVEL STORE.=
BHAO66		ASSOCIATIVE	OR CONTENT-ADDRESSED STORES.=
RWSA67	SERIAL	ASSOCIATIVE	MEMORIES.=
WCAM69	,	ASSOCIATIVE	MEMORY DEVICE 3466632.=
TRCA64	COMPUTER	ASSOCIATIVE	MEMORY FINAL REPORT.=
CBDI63	NSIONING IN AN	ASSOCIATIVE	MEMORY. =DIME
RJRO63	H ON CRYOGENIC	ASSOCIATIVE	MEMORIES.=RESEARC
WRAT	DIODE CELL FOR	ASSOCIATIVE	MEMORIES AND MULTIPLE-WORD ACCESS MEMORIES.=A TRANSISTOR-TUNNEL
FHAP64		ASSOCIATIVE	PROCESSOR STUDY.=
GJAA69	AN	ASSOCIATIVE	HIGHLY-PARALLEL COMPUTER FOR RADAR DATA PROCESSING.=
FTAA69	AN	ASSOCIATIVE	PROCESSOR.=
NCAM64		ASSOCIATIVE	MEMORY SYSTEM IMPLEMENTATION AND CHARACTERISTICS.=
SLRA69	RANGE	ASSOCIATIVE	MEMORY WITH ORDERED RETRIEVAL.=
RJRO63	H ON CRYOGENIC	ASSOCIATIVE	MEMORIES.=RESEARC
FCAM61		ASSOCIATIVE	MEMORY APPLICATIONS FOR INTELLIGENCE DATA PROCESSING.=
NWTA68	THE	ASSOCIATIVE	PROCESSOR IN AIRCRAFT CONFLICT DETECTION.=
YYAC66	POINT CELLULAR	ASSOCIATIVE	MEMORY.=A CUT
FWAM64		ASSOCIATIVE	MEMORY.=
LESS63	SOLID STATE	ASSOCIATIVE	CELLS.=
PGTM62	ULTI-LIST TYPE	ASSOCIATIVE	MEMORY.=THE M
RCAP64	ROPOSAL FOR AN	ASSOCIATIVE	MEMORY USING MAGNETIC FILMS.=A P
BRAA69	AN	ASSOCIATIVE	MEMORY PARALLEL DELTIC REALIZATION FOR ACTIVE SONAR SIGNAL PROCESSING.=
RJRO63	H ON CRYOGENIC	ASSOCIATIVE	MEMORIES.=RESEARC
YYAG66	A-CRYOGENIC	ASSOCIATIVE	MEMORY FOR INFORMATION RETRIEVAL.=
HIPC68	PROCESSOR WITH	ASSOCIATIVE	CONTROL.=PAGE-CONTROL SCHEMES IN A MULTI
AMGE62	. E. CRYOGENIC	ASSOCIATIVE	MEMORY CIRCUIT DEVELOPED.=G

```
8B8C66 .                    BASING          CRYOGENIC COMPUTERS IN SPACE=

SSAM63                      ASSOCIATIVE     MEMORY COMPUTERS FROM THE PROGRAMMING POINT OF VIEW.=
PJFA65      G OF CRYOGENIC  ASSOCIATIVE     PROCESSOR PLANES.=FABRICATION AND TESTIN
STGS68      NICATIONS : AN  ASSOCIATIVE     MEMORY APPROACH.=GRAPHICAL SYSTEMS COMMU
LBFA63              FIXED   ASSOCIATIVE     MEMORY USING EVAPORATED ORGANIC DIODE ARRAYS.=
SLAS67                      ASSOCIATIVE     STORING PROCESSOR.=
SRAS60                      ASSOCIATIVE     SELF-SORTING MEMORY.=
HHED67      T FOR ADVANCED  ASSOCIATIVE     MEMORIES.=ELEMENT DEVELOPMEN
JHSO68      DY OF ADVANCED  ASSOCIATIVE     PROCESSOR TECHNIQUES INTERIM REPORT.=STU
GRHA66              HYBRID  ASSOCIATIVE     COMPUTER STUDY.=
RGCA64           CRYOGENIC  ASSOCIATIVE     PROCESSOR PLANE TEST AND EVALUATION.=
PCAM67                      ASSOCIATIVE     MEMORY COMPILER TECHNIQUES STUDY.=
PJFA67      WORD CRYOGENIC  ASSOCIATIVE      PROCESSOR.=FABRICATION AND TESTING OF 5000
MHRM64      ESPONSES IN AN  ASSOCIATIVE     MEMORY.=RESOLVING MULTIPLE R
TPAS67                      ASSOCIATIVE     STORE.=
TRAC67                      ASSOCIATIVE     COMPUTER.=
TRAM67                      ASSOCIATIVE     MEMORY SYSTEM.=
GMAO66      LYSIS OF SMALL  ASSOCIATIVE     MEMORIES FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=ANA
GGAT67                      ASSOCIATIVE     TECHNIQUES FOR CONTROL FUNCTIONS IN A MULTI-PROCESSOR SIMULATION INVESTIGATION
TRAM66                      ASSOCIATIVE     MEMORY.=
HBED66      T FOR ADVANCED  ASSOCIATIVE     MEMORIES.=ELEMENT DEVELOPMEN
RJCA64           CRYOGENIC  ASSOCIATIVE     MEMORY TECHNIQUES.=
BRCA63           CRYOGENIC  ASSOCIATIVE     PROCESSOR.=
HPAM65                      ASSOCIATIVE     MEMORY COMPUTER SYSTEM DESCRIPTION AND SELECTED NAVAL APPLICATIONS.=
NAAN62      ADDRESSING FOR  ASSOCIATIVE      MEMORIES.=A NOTE ON THE USE OF SCRAMBLED
HACA66      DDRESSABLE AND  ASSOCIATIVE     MEMORY SYSTEMS - A SURVEY.=CONTENT-A
FBAA65                 AN   ASSOCIATIVE     PARALLEL PROCESSOR WITH APPLICATION TO PICTURE PROCESSING.=
EDAA64                 AN   ASSOCIATIVE     PROCESSOR.=
CRAP64      ROPOSAL FOR AN  ASSOCIATIVE     MEMORY USING MAGNETIC FILMS.=A P
CBSA63      IZABLE FORM OF  ASSOCIATIVE     MEMORY.=SHIEF: A REAL
CAAM63                      ASSOCIATIVE     MEMORIES.=
LEAT63                      ASSOCIATIVE     TECHNIQUES WITH COMPLEMENTING FLIP-FLOP.=
ARCO65      PER-CONDUCTIVE  ASSOCIATIV      MEMORIES.=CALCULATIONS OF SPEED OF LADDER NETWORK FOR SU
AJSO62      EARCH ON RANGE  ASSOCIATIV      MEMORY.=S
AJEO61       SYSTEMS USING  ASSOCIATIV      MEMORIES.=EVALUATION OF
ARSA63      UPERCONDUCTIVE  ASSOCIATIVE     MEMORIES.=S
CYAD65      UCTIVE-READOUT  ASSOCIATIVE     MEMORY.=A DESTR
CMAM64                      ASSOCIATIVE     MEMORY SYSTEM IMPLEMENTATION AND CHARACTERISTICS.=
BHAM65                      ASSOCIATIVE     MEMORY USING ANALOG SUMMING TECHNIQUE.=
BBSO64      OF A CRYOGENIC  ASSOCIATIVE     PROCESSOR.=STRUCTURE
SGAO64      LICATION OF AN  ASSOCIATIVELY   ADDRESS DISTRIBUTED MEMORY.=APP
SLAS66                      ASSOCIATIVE-STORING PROCESSOR STUDY.=
SJAO68                      ASYNCHRONOUS    OPERATION OF AN ITERATIVELY STRUCTURED GENERAL-PURPOSE DIGITAL COMPUTER=
DFTA61                 THE  ATLAS           COMPUTER.=
SHTC62      OL UNIT OF THE  ATLAS           COMPUTER.=THE CENTRAL CONTR
SJAT64                      AT-1            PARALLEL COMPUTER - SECOND PRELIMINARY VERSION.=
SEAA61                 AN   AUTOMATIC       SEQUENCING PROCEDURE WITH APPLICATION TO PARALLEL PROGRAMMING.=
MSUO64      AMETER DATA BY  AUTOMATIC       DATA REDUCTION.=USE OF STANDARD MEMORY SYSTEMS AS ASSOCIATIVE MEMORIES FOR INT
HSAP60                      AUTOMATIC       PARALLEL PROCESSING.=
LPAS63                      AUTOMATIC       STRATIFICATION OF INFORMATION.=
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GPAI66		AUTOMATIC	INTRODUCTION OF INFORMATION INTO A REMOTE-ACCESS SYSTEM : A PHYSICS LIBRARY CA
MDTA66	THE	AUTOMATIC	ASSIGNMENT AND SEQUENCING OF COMPUTATIONS ON PARALLEL PROCESSOR SYSTEMS.=
BFOT	E EVOLUTION OF	AUTONOMY	FOR AN ASSOCIATIVE MEMORY.=ON TH
SAAS68		AUXILIARY	STORAGE ASSOCIATIVE DATA STRUCTURE FOR PL/1=
ERTA69	THE ADVANCED	AVIONICS	DIGITAL COMPUTER.=
GAS069	PROCESSOR IN	AWACS	=STUDY OF MISSION EFFECTIVENESS OF ASSOCIATIVE
IBSS64	VEILLANCE DATA	BASE	REPRESENTATION AS TEST VEHICLE.=SEA SUR
ASTA67	AN ASSOCIATIVE	BASE	=TRAMP : A RELATIONAL MEMORY WITH
BBBC66		BASING	CRYOGENIC COMPUTERS IN SPACE=
TRFT66	TECHNIQUES FOR	BATCH	FABRICATION OF DISTRIBUTED LOGIC NETWORKS.=FABRICATION
CBEO65	S OF THE DLM, /	BATCH-FABRICATABLE	PARALLEL COMPUTER.=ECONOMIC
BDTB67	THE	BBN	940 LISP SYSTEM.=
LSAP66	ULTI-PREFORMED	BEAM	SONAR SYSTEMS.=ASSOCIATIVE PARALLEL PROCESSING AS APPLIED TO M
FGLT68	OW TEMPERATURE	BEAM-ADDRESSABLE	MEMORY.=L
TKAT61	ELEMENT USING	BIAS	RESTORATION.=A TOROIDAL NONDESTRUCTIVE MEMORY
MRHS66	HIGH-SPEED	BIAX	MEMORIES.=
HJBP64		BIAX	PERCEPTRON.=
SHRO63	RESEARCH ON	BIAX	TYPE ELEMENTS AND ASSOCIATED CIRCUITS.=
PCAT64	A 10MO NDRO	BIAX	MEMORY OF 1024 WORD, 48 BIT PER WORD CAPACITY.=
NKPM65	MODEL FOR THE	BIAX	=PHENOMENOLOGICAL
WWBH59		BIAX	HIGH-SPEED MAGNETIC COMPUTER ELEMENT.=
BHIL65	AND ANNOTATED	BIBLIOGRAPHY	=ILLIAC-II - A SHORT DESCRIPTION
AFBI65		BILOC	- A HIGH SPEED NDRO ONE CORE PER BIT ASSOCIATIVE ELEMENT.=
GJBT60		BINARY	TESTS FOR TWO TERMINAL, SIMULTANEOUS ACTION.=
BHAA62	ND SOME OF ITS	BIOLOGICAL	IMPLICATIONS.=AN ASSOCIATIVE MACHINE FOR DEALING WITH THE VISUAL FIELD A
RDBD67		BIT	DRIVER=
AFBI65	O ONE CORE PER	BIT	ASSOCIATIVE ELEMENT.=BILOC - A HIGH SPEED NDR
CATK62	3-K	BIT	ASSOCIATIVE MEMORY WORKS AT ROOM TEMPERATURE.=
CSPW67	PLATED WIRE	BIT	STEERING FOR LOGIC AND STORAGE.=
BBCR64	ASE 2 10 (9)	BIT	MEMORY.=CRYOELECTRIC RANDOM ACCESS MEMORY; PR
PCAT64	1024 WORD, 48	BIT	PER WORD CAPACITY.=A 10MO NDRO BIAX MEMORY OF
CWPW67	MEMORIES WITH	BIT-STEERING	TECHNIQUE.=PLATED WIRE CONTENT-ADDRESSABLE
ARTB65	THE	BRIDGE	CELL - A NEW SUPERCONDUCTIVE MEMORY CELL FOR RANDOM-ACCESS WORK-ORGANIZED MEMO
RBAB67	A	BRIEF	SURVEY OF COMPUTER LANGUAGES FOR SYMBOLIC AND ALGEBRAIC MANIPULATION.=
FKBD67		BROOKHAVEN	DIGITAL COMMUNICATIONS NETWORK =
CCPR	ON PROCESS FOR	BUBBLE	CHAMBER PICTURES.=PATTERN RECOGNITI
BVMO66	EM INCLUDING A	BUFFER	ASSOCIATIVE MEMORY UNIT.=MODELING OF A MEMORY SYST
BSLS68	MODEL	BUILDING	SIMULATION AND EVALUATION.=LARGE SCALE INFORMATION PROCESSING SYSTEMS :
LHTA69	OCESSOR USING	BULK	STORAGE.=THE ASP - DYNABIT SYSTEM : AN ASSOCIATIVE PR
CGBP65		BULK	PROCESSING IN DISTRIBUTED LOGIC MEMORY.=
ISSB66	ING BY ADDRESS	CALCULATION	=SORT
MPAD69	FOR SCIENTIFIC	CALCULATIONS	=A DESIGN FOR A FAST COMPUTER
ARCO65		CALCULATIONS	OF SPEED OF LADDER NETWORK FOR SUPER-CONDUCTIVE ASSOCIATIVE MEMORIES.=
PAAC70	ASSOCIATIVE	CAPABILITIES	FOR MASS STORAGE THROUGH ARRAY ORGANIZATION=
FRAL67	CALE COMPUTING	CAPABILITIES	THROUGH ASSOCIATIVE PARALLEL PROCESSING=ACHIEVING LARGE S
ASTA69	DEDUCTIVE	CAPABILITIES	=TRAMP: AN INTERPRETIVE ASSOCIATIVE PROCESSOR WITH
FRAL	ARGE COMPUTING	CAPABILITIES	THROUGH ASSOCIATIVE PARALLEL PROCESSING.=ACHIEVING L
SDAL	ARGE COMPUTING	CAPABILITIES	THROUGH AN ARRAY COMPUTER.=ACHIEVING L
RJMM63	TIC MEMORIES -	CAPABILITIES	AND LIMITATIONS.=MAGNE
HJAU59	RSAL COMPUTER,	CAPABLE	OF EXECUTING AN ARBITRARY NUMBER OF SUB-PROGRAMS SIMULTANEOUSLY.=A UNIVE
MYSP61	ENT STORAGE BY	CAPACITIVE	COUPLING.=SEMI-PERMAN
FHCC61	CARD	CAPACITOR	- A SEMI-PERMANENT, READ ONLY MEMORY.=
KASC67	SMALL	CAPACITY	THIN CYLINDRICAL MAGNETIC FILM STORAGE SYSTEMS.=
PCAT64	PER WORD	CAPACITY	=A 10MO NDRO BIAX MEMORY OF 1024 WORD, 48 BIT
BCAL63	A LARGE	CAPACITY	CRYOELECTRIC MEMORY WITH CAVITY SENSING.=
FHCC61		CARD	CAPACITOR - A SEMI-PERMANENT, READ ONLY MEMORY.=
SSTF60	FILM CRYOTRON	CATALOG	MEMORY.=THIN

SSTF60	-FILM CRYOTRON	CATALOG	MEMORY.=THIN
SMTC67	THE CRYOTRON	CATALOG	MEMORY SYSTEM.=
GPAI66	HYSICS LIBRARY	CATALOG	=AUTOMATIC INTRODUCTION OF INFORMATION INTO A REMOTE-ACCESS SYSTEM : A P
BSCS65		CAVITY	SENSING OF CRYOELECTRIC MEMORY PLANES.=
BCAL63	IC MEMORY WITH	CAVITY	SENSING.=A LARGE CAPACITY CRYOELECTR
GKAC	US FILM MEMORY	CELL	FOR SUPERCONDUCTIVE ASSOCIATIVE MEMORIES=A CONTINO
WRAT	R-TUNNEL DIODE	CELL	FOR ASSOCIATIVE MEMORIES AND MULTIPLE-WORD ACCESS MEMORIES.=A TRANSISTO
SOTR68	DUCTING MEMORY	CELL	- A PERSISTOTRON - IN A MEMORY MATRIX. =THE RELIABILITY OF OPERATING A SUPERCO
BBOO64	US FILM MEMORY	CELL	=OPERATION OF THE CRYOGENIC CONTINUO
LACA65	CIATIVE MEMORY	CELL	=CRYOTRON ASSO
RDAM67	CIATIVE MEMORY	CELL	=ASSO
SAAC62	RYOTRON MEMORY	CELL	=A C
ARTB65	THE BRIDGE	CELL	- A NEW SUPERCONDUCTIVE MEMORY CELL FOR RANDOM-ACCESS WORK-ORGANIZED MEMORIES.
ARTB65	DUCTIVE MEMORY	CELL	FOR RANDOM-ACCESS WORK-ORGANIZED MEMORIES.=THE BRIDGE CELL - A NEW SUPERCON
GLAI65	AN IMPROVED	CELL	MEMORY.=
KHSA67	US FILM MEMORY	CELLS	=SUPERCONDUCTIVE CONTINUO
LESS63	TE ASSOCIATIVE	CELLS	=SOLID STA
NECS67	YOTRON STORAGE	CELLS	FOR RANDOM ACCESS MEMORIES.=CR
LCIC62	RCOMMUNICATING	CELLS	BASIS FOR A DISTURBED LOGIC COMPUTER.=INTE
KWCL69		CELLULAR	LOGIC-IN-MEMORY ARRAYS=
KLCI68		CELLULAR	INTERCONNECTION ARRAYS=
MSCL64		CELLULAR	LINEAR-INPUT LOGIC.=
YYAC66	A CUTPOINT	CELLULAR	ASSOCIATIVE MEMORY.=
MRCC64	CUTPOINT	CELLULAR	LOGIC.=
MRCR68		CELLULAR	REALIZATION OF THE DYNAMIC PROGRAMMING ALGORITHM, ANNUAL PROGRESS REPORT.=
LCSO68	SYNTHESIS OF A	CELLULAR	COMPUTER. =SYNTHE
EKPO67	PROPERTIES OF	CELLULAR	ARRAYS FOR LOGIC AND STORAGE.=
YYAC66	A CUTPOINT	CELLULAR	ASSOCIATIVE MEMORY.=
ETTO68	THEORY OF	CELLULAR	LOGIC NETWORKS AND MACHINES.=
SHTC62	THE	CENTRAL	CONTROL UNIT OF THE ATLAS COMPUTER.=
CCPR	ESS FOR BUBBLE	CHAMBER	PICTURES.=PATTERN RECOGNITION PROC
MCAM64	EMENTATION AND	CHARACTERISTICS	=ASSOCIATIVE MEMORY SYSTEM IMPL
BCIL69	IAC-IV SYSTEMS	CHARACTERISTICS	AND PROGRAMMING MANUAL.=ILL
BCIL68	C-IV : SYSTEMS	CHARACTERISTICS	AND PROGRAMMING MANUAL.=ILLIA
CMCO60		CHARACTERISTICS	OF FILM CRYOTRONS.=
HLSC65	SWITCHING	CHARACTERISTICS	OF CROSSED-FILM CRYOTRON CIRCUITS.=
CMAM64		CHARACTERISTICS	=ASSOCIATIVE MEMORY SYSTEM IMPLEMENTATION AND
HJIC65	UIT COMPUTERS	CHARACTERIZATION	AND RESUME.=ITERATIVE CIRC
GVTP61	L MACHINES IN	CHEMISTRY	=THE PROSPECTS FOR THE UTILIZATION OF INFORMATIONAL-LOGICA
HJIC65	ITERATIVE	CIRCUIT	COMPUTERS CHARACTERIZATION AND RESUME.=
ACII65	AN INTERACTIVE	CIRCUIT	STORED PROGRAM PARALLEL PROCESSOR.=INVESTIGATIONS INTO THE THEORY OF
AMGE62	CIATIVE MEMORY	CIRCUIT	DEVELOPED.=G. E. CRYOGENIC ASSO
NGSA63	SYSTEM AND	CIRCUIT	DESIGNS FOR THE TOBERMORY PERCEPTION.=
IBAM65	MEMORY READOUT	CIRCUIT	=ASSOCIATIVE
BCAM65	CIATIVE MEMORY	CIRCUIT	=ASSO
HJOI60	ON ITERATIVE	CIRCUIT	COMPUTER CONSTRUCTED OF MICROELECTRONIC COMPONENTS AND SYSTEM.=
BCSO69	PLEMENTARY MOS	CIRCUITS	FOR HIGH SPEED ASSOCIATIVE MEMORY=SILICON-ON-SAPPHIRE COM
HFIA61	RRAYS OF LOGIC	CIRCUITS	=ITERATIVE A
LESC63	SEMI-CONDUCTOR	CIRCUITS	IN ASSOCIATIVE MEMORIES.=SEMI-C
YTSD64	RYOGENIC LOGIC	CIRCUITS	=SYSTEMATIC DESIGN OF C
SHRO63	AND ASSOCIATED	CIRCUITS	=RESEARCH ON BIAX TYPE ELEMENTS
SHMA64	MEMORY AND	CIRCUITS	THEREFOR.=
WBCA63	S AND CRYOTRON	CIRCUITS	A REVIEW.=CRYOTRON
NVSC61	UPERCONDUCTING	CIRCUITS	FOR COMPUTING MACHINES.=S
HLSC65	OTRON	CIRCUITS	=SWITCHING CHARACTERISTICS OF CROSSED-FILM CRY
FOAH66	ECHNOLOGY: I -	CIRCUITS	AND DEVICES.=A HYBRID CRYOTRON T
HMCS60	IC AND LOGICAL	CIRCUITS	=CRYOTRON STORAGE, ARITHMET

YFCA62		CIRCULATING	ASSOCIATIVE MEMORIES.=
WAUI69	IFIED INTERVAL	CLASSIFICATION	AND UNIFIED 3-CLASSIFICATION FOR ASSOCIATIVE MEMORIES=UN
CDAM66	AMDRIVE* AND	CODAP	-ASSOCIATIVE MEMORY ASSEMBLER.=
MRMC63	OMPARATORS AND	CODE	CONVERTERS. =MAGNETIC C
BJAS61	IVE MEMORY AND	CODE	CONVERTER.=A SEMI-PERMANENT MAGNETIC ASSOCIAT
CVTU67	THE USE OF	CODES	' M-OUT-OF-N ' IN ASSOCIATIVE MEMORIES.=
LACO62		CODING	OF TREES FOR USE IN AN ASSOCIATIVE MEMORY.=
GKAC67	EN BY MULTIPLE	COINCIDENT	PULSES=A CONTINUOUS FILM MEMORY DRIV
BACC61		COINCIDENT	CURRENT SUPERCONDUCTIVE MEMORY.=
PTAM67	IVE MEMORY FOR	COLLECTION	AND DISPLAY SYSTEM.=ASSOCIAT
GACO62		COLLECTION	OF NOTES ON ASSOCIATIVE MEMORY.=
NTCA60		COMBINATORIAL	ASPECTS OF INFORMATION|RETRIEVAL.=
RFST64	ON COMPUTER TO	COMMAND	AND CONTROL. VOLUME I. INFORMATION STORAGE, RETRIEVAL AND COMMUNICATION SYSTEM
RFST64	ON COMPUTER TO	COMMAND	AND CONTROL.=STUDY TO DETERMINE THE APPLICABILITY OF THE SOLOM
SHCO67		COMMENT	ON ' CONTENT-ADDRESSED MEMORY USING MAGNETO- OR ELECTRO-OPTICAL INTERROGATION.
SISA63	HINE GRAPHICAL	COMMUNICATION	SYSTEM.=SKETCHPAD, A MAN-MAC
RLGC64	GRAPHICAL	COMMUNICATION	AND CONTROL.LANGUAGES.=
RFST64	RETRIEVAL AND	COMMUNICATION	SYSTEM CONTROL.=STUDY TO DETERMINE THE APPLICABILITY OF THE SOLOMON COMPUTER T
FKBD67	KHAVEN DIGITAL	COMMUNICATIONS	NETWORK =BROO
STGS68	PHICAL SYSTEMS	COMMUNICATIONS	: AN ASSOCIATIVE MEMORY APPROACH.=GRA
MRMC63	MAGNETIC	COMPARATORS	AND CODE CONVERTERS. =
BRAC64	A	COMPARISON	OF LIST PROCESSING LANGUAGES.=
BBCO68		COMPILATION	OF ARITHMETIC EXPRESSIONS FOR PARALLEL COMPUTATIONS.=
AWAC68	A	COMPILER	FOR AN ASOCIATIVE ORJECT MACHINE=
MYSA69	N THE TRANQUIL	COMPILER	=STORAGE ALLOCATION ALGORITHMS I
WDSA64	ION TO DEVELOP	COMPILER	TECHNIQUES REQUIRED FOR PROGRAMMING THE PARALLEL NETWORK COMPUTER.=STUDY AND I
PCAM67	CIATIVE MEMORY	COMPILER	TECHNIQUES STUDY.=ASSO
SRAP61	ORY FOR USE IN	COMPILING	=A PROGRAMMED ASSOCIATIVE MEM
BSSO69	ON-ON-SAPPHIRE	COMPLEMENTARY	MOS CIRCUITS FOR HIGH SPEED ASSOCIATIVE MEMORY=SILIC
LEAT63	ECHNIQUES WITH	COMPLEMENTING	FLIP-FLOP.=ASSOCIATIVE T
RJAF64	ALGORITHMS FOR	COMPLEX	SEARCHES.=ALGORI
MKES67	IC SOLID STATE	COMPONENTS	PART 4.=ELECTRON
HJOI60	ICROELECTRONIC	COMPONENTS	AND SYSTEM.=ON ITERATIVE CIRCUIT COMPUTER CONSTRUCTED OF M
GJCD67		COMPOUND	DATA STRUCTURE FOR COMPUTER AIDED DESIGN : A SURVEY.=
SJAI64	MS IN PARALLEL	COMPUTATION	=ALGORITH
EVOO62	COMPUTER FOR	COMPUTATION	OF EIGENVALUES AND EIGENVECTORS OF REAL SYMMETRIC MATRICES.=ORGANIZATION OF A
MEMO67	MODELS OF	COMPUTATIONAL	SYSTEMS - CYCLIC TO ACYCLIC GRAPH TRANSFORMATIONS.=
ADAM69	L FOR PARALLEL	COMPUTATIONS	=A MODE
BBCO68	ALLEL	COMPUTATIONS	=COMPILATION OF ARITHMETIC EXPRESSIONS FOR PAR
RBAG67	L FOR PARALLEL	COMPUTATIONS	=A GRAPH MODE
MDTA66	SEQUENCING OF	COMPUTATIONS	ON PARALLEL PROCESSOR SYSTEMS.=THE AUTOMATIC ASSIGNMENT AND
KMPO66	FOR PARRALLEL	COMPUTATIONS	DETERMINACY, TERMINATION, QUEUEING.=PROPERTIES OF A MODEL
WDCA68		COMPUTER-AIDED	STRATEGY DESIGN USING ADAPTIVE AND ASSOCIATIVE TECHNIQUES.=
WICA68	DATA STRUCTURE	CONCEPT	BASED ON RINGS=CYLINDERS-A
SLAS67	ASP : A NEW	CONCEPT	IN LANGUAGE AND MACHINE ORGANIZATION.=
KMAM62	S IN DIGITAL '	CONCEPT	' PROCESSING. =ADAPTIVE MECHANISM
BHAM62	PROPAGATION	CONCEPTS	=A MACHINE FOR PERFORMING VISUAL RECOGNITION BY USE OF ANTENNA
CDCA65	MEMORY SYSTEMS	CONCEPTS	=CONTENT ADDRESSABLE
LMAS66	MINARY RESULTS	CONCERNING	PARALLEL PROCESSING AND PARALLEL PROCESSORS.=A SURVEY OF PROBLEMS AND PRELI
SDSS65	N PARALLEL AND	CONCURRENT	COMPUTER SYSTEMS=SPECIAL SESSION O
RKAA64	ALGORITHM FOR	CONCURRENT	RANDOM WALKS ON HIGHLY PARALLEL MACHINES.=A
VEMR61	EMPLOYING ONE	CONDUCTIVE	PATH PER FILE ITEM.=MAGNETIC REALIZATION FOR MIRF
MWTA68	OR IN AIRCRAFT	CONFLICT	DETECTION.=THE ASSOCIATIVE PROCESS
ASAM67	OF LEE'S PATH	CONNECTION	ALGORITHM.=A MODIFICATION
LCAA61	RITHM FOR PATH	CONNECTIONS	AND ITS APPLICATIONS.=AN ALGO
JEMH69	OMPUTER SYSTEM	CONSIDERATIONS	=MEMORY HIERARCHY - C
NRSS69	SOME SOFTWARE	CONSIDERATIONS	IN UTILIZATION OF A NETWORK OF COMPUTERS.=

```
SPPA63          ING AND DESIGN      CONSIDERATIONS      OF A HIGHLY PARALLEL COMPUTER.=PROGRAMM
BCCI62                              CONSIDERATIONS      IN THE DESIGN OF A COMPUTER WITH HIGH LOGIC-TO-MEMORY SPEED RATIO.=
HJOI60          RCUIT COMPUTER      CONSTRUCTED         OF MICROELECTRONIC COMPONENTS AND SYSTEM.=ON ITERATIVE CI
SGAN60          NCIPLE FOR THE      CONSTRUCTION        OF A MEMORY DEVICE.=A NEW PRI
ACTC65          RIMENTS IN THE      CONSTRUCTION        OF AN ADAPTIVE MAN-MACHINE ASSOCIATIVE MEMORY FOR INFORMATION RETRIEVAL.=TOWAR
FESA63          PLICATIONS FOR      CONTENT             ADDRESSABLE MEMORIES=SOME AP
PFAI69          HE EXPLORATORY      CONTENT             ADDRESSABLE MEMORY SYSTEM.=AN IMPROVED FIELD-CONTROLLED POLARIZATION-TRANSFER
FRCA63                              CONTENT             ADDRESSABLE MEMORY SYSTEMS.=
LCCA68                              CONTENT             ADDRESSABLE AND DISTRIBUTED LOGIC MEMORIES. =
LSAM63            ALL MAGNETIC      CONTENT             ADDRESSED MEMORY.=
LPAC64                    A         CONTENT             ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVA
HJAC67                    A         CONTENT             ADDRESSABLE MEMORY WITH APPLICATIONS TO MACHINE TRANSLATION.=
BRCA67                              CONTENT             ADDRESSABLE MEMORIES.=
BRCA66                              CONTENT             ADDRESSABLE MEMORY.=
GECA67                              CONTENT             ADDRESSED MEMORY.=
BRCA66                              CONTENT             ADDRESSABLE MEMORY.=
SLPC65                PANEL :       CONTENT             ADDRESSABLE MEMORIES.=
SRCA67                              CONTENT             ADDRESSED MEMORY.=
WDHS64            HIGH-SPEED,       CONTENT             SEARCH IN A LARGE, ROTATING, MASS MEMORY.=
PHCA62                              CONTENT             ADDRESSING AND INFORMATION RETRIEVAL.=
LPAC63                    A         CONTENT             ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH APPLICATION TO INFORMATION RETRIEVAL
CDCA65                              CONTENT             ADDRESSABLE MEMORY SYSTEMS CONCEPTS.=
LMRO62          D LISTS FROM A      CONTENT             ADDRESSED MEMORY.=RETRIEVAL OF ORDERE
EJIP70          ING WITH QUEUED     CONTENT-ADDRESSABLE MEMORIES=INTERRUPT PROCESS
MJAO69          ATIVE MEMORY OR     CONTENT-ADDRESSABLE MEMORY SYSTEMS AND A KWIC INDEX TO THE LITERATURE 1956-1970=AN OVERVIEW OF A
SBCA66                              CONTENT-ADDRESSABLE PROGRAMMING TECHNIQUES.=
CWPW67              PLATED WIRE     CONTENT-ADDRESSABLE MEMORIES WITH BIT-STEERING TECHNIQUE.=
EFAF63           ALGORITHMS FOR     CONTENT-ADDRESSABLE MEMORY ORGANIZATION.=
FRCA63                              CONTENT-ADDRESSABLE MEMORY SYSTEMS.=
BRCA67                              CONTENT-ADDRESSABLE MEMORY.=
RPDA68                              CONTENT-ADDRESSABLE MEMORY SYSTEM.=DESIGN AND EVALUATION OF A GLASS DELAY LINE
RPEO67          UATION OF THREE     CONTENT-ADDRESSABLE MEMORY SYSTEMS USING GLASS DELAY LINES.=EVAL
RRTC64              TRANSFLUXOR     CONTENT-ADDRESSABLE MEMORY.=
SFAC64                    A         CONTENT-ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=
CWCA65                              CONTENT-ADDRESSABLE MEMORY TECHNIQUES.=
CWCA66                              CONTENT-ADDRESSABLE MEMORY TECHNIQUES.=
CWCA65                              CONTENT-ADDRESSABLE MEMORY TECHNIQUES.=
TRTC62                    TRUE      CONTENT-ADDRESSABLE MEMORY.=
CRCA67                              CONTENT-ADDRESSABLE MEMORY TECHNIQUES.=
EFSA63          PPLICATIONS FOR     CONTENT-ADDRESSABLE MEMORIES.=SOME A
ERCA64                              CONTENT-ADDRESSABLE DISTRIBUTED-LOGIC MEMORIES.=
HACA66                              CONTENT-ADDRESSABLE AND ASSOCIATIVE MEMORY SYSTEMS - A SURVEY.=
RPAG69          ASS DELAY LINE      CONTENT-ADDRESSED MEMORY SYSTEM=A GL
SWAS68          NTIALLY HOMING      CONTENT-ADDRESSED MEMORY MODEL.=A SEQUE
RPAG69          ASS DELAY LINE      CONTENT-ADDRESSED MEMORY SYSTEM.=A GL
BHAO66          ASSOCIATIVE OR      CONTENT-ADDRESSED STORES.=ASSOCI
NMCA65                              CONTENT-ADDRESSED MEMORY USING MAGNETORESISTIVE READOUT OF MAGNETIC THIN FILMS.=
CYAO65          APPLICATION OF      CONTENT-ADDRESSED MEMORY FOR DYNAMIC STORAGE ALLOCATION.=APPLIC
RCCA66                              CONTENT-ADDRESSED MEMORY.=
SHCA66                              CONTENT-ADDRESSED MEMORY USING MAGNETO- OR ELECTRO-OPTICAL INTERROGATION.=
SHCO67            COMMENT ON '      CONTENT-ADDRESSED MEMORY USING MAGNETO- OR ELECTRO-OPTICAL INTERROGATION.'=
CSDT66          F A DELAY-LINE      CONTENT-ADDRESSED MEMORY.=DESIGN TECHNIQUES O
GKAC                      A         CONTINOUS           FILM MEMORY CELL FOR SUPERCONDUCTIVE ASSOCIATIVE MEMORIES=
GKAW            UPERCONDUCTING      CONTINUOUS          FILM MEMORY=A WORD-ORGANIZED S
KHSA67          UPERCONDUCTIVE      CONTINUOUS          FILM MEMORY CELLS=S
GKAC67                    A         CONTINUOUS          FILM MEMORY DRIVEN BY MULTIPLE COINCIDENT PULSES=
BBOO64           THE CRYOGENIC      CONTINUOUS          FILM MEMORY CELL.=OPERATION OF
```

```
BLCS60                      CONTINUOUS      SHEET SUPERCONDUCTING MEMORY.=
NDCS65                      CONTINUOUS      SHEET SENSING FOR RANDOM ACCESS MEMORIES.=
ENAO65    THE CRYOGENIC     CONTINUOUS      FILM MEMORY.=ANALYSIS OF
GMEA65   UPERCONDUCTING     CONTINUOUS      FILM STORE.=EXPERIMENTAL AND THEORETICAL ASPECTS OF THE S
SJDL69   ER FOR PROCESS     CONTROL         =DISTRIBUTED LOGIC MEMORY COMPUT
GHAM68   TH ASSOCIATIVE     CONTROL          =A MULTIPROCESSOR WI
BMAA69   D SYNTHESIS OF     CONTROL         MECHANISMS FOR PARALLEL PROCESSES.=ANALYSIS AN
HHCS68                      CONTROL         STORAGE USE IN IMPLEMENTING AN ASSOCIATIVE MEMORY FOR A TIME-SHARED PROCESSOR.
HTPC68    ASSOCIATIVE       CONTROL         =PAGE-CONTROL SCHEMES IN A MULTIPROCESSOR WITH
HBSU64   AS A REAL-TIME     CONTROL         =SOME USES OF AN ASSOCIATIVE MEMORY
GFAT66   TECHNIQUES FOR     CONTROL         FUNCTIONS IN A MULTIPROCESSOR.=ASSOCIATIVE
FAPS60   OGRAM SEQUENCE     CONTROL         IN A MULTIPROCESSING SYSTEM USING ASSOCIATIVE STORAGE.=PR
HHAD63      A DIRECTORY     CONTROL         SYSTEM FOR MULTIPROGRAMMING.=
SHTC62      THE CENTRAL     CONTROL         UNIT OF THE ATLAS COMPUTER.=
RFST64   TO COMMAND AND     CONTROL         =STUDY TO DETERMINE THE APPLICABILITY OF THE SOLOMON COMPUTER
RFST64   TO COMMAND AND     CONTROL          VOLUME I. INFORMATION STORAGE, RETRIEVAL AND COMMUNICATION SYSTEM CONTROL.=ST
GGAT67   TECHNIQUES FOR     CONTROL         FUNCTIONS IN A MULTI-PROCESSOR SIMULATION INVESTIGATION.=ASSOCIATIVE
RLGC64   MUNICATION AND     CONTROL         LANGUAGES.=GRAPHICAL COM
RFST64   ICATION SYSTEM     CONTROL         =STUDY TO DETERMINE THE APPLICABILITY OF THE SOLOMON COMPUTER TO COMMAND AND C
AETF61   FORMULATION OF     CONTROL         SYSTEM OPTIMIZATION PROBLEMS.=THE FIXED-PLUS-VARIABLE COMPUTER SYSTEM IN DYNAM
VITA69   EMENT             CONTROLLED      BY MONOPOLAR CURRENTS.=THE ANALYSIS OF THE CRYOTRONIC ASSOCIATIVE EL
ACTC65          TOWARDS     CONTROLLED      EXPERIMENTS IN THE CONSTRUCTION OF AN ADAPTIVE MAN-MACHINE ASSOCIATIVE MEMORY
RPAA67   ING SYSTEM FOR     CONVENTIONAL    DIGITAL COMPUTERS=AN ASSOCIATIVE PROCESS
RFAA67   ING SYSTEM FOR     CONVENTIONAL    DIGITAL COMPUTERS.=AN ASSOCIATIVE PROCESS
CAOT68          ON THE      CONVERGENCE     OF DISCRETE APPROXIMATIONS TO THE NAVIER STOKES EQUATIONS.=
BJAS61   AND CODE           CONVERTER       =A SEMI-PERMANENT MAGNETIC ASSOCIATIVE MEMORY
NRMC63   ATORS AND CODE     CONVERTERS       =MAGNETIC COMPAR
AFBI65   SPEED NDRO ONE     CORE            PER BIT ASSOCIATIVE ELEMENT.=BILOC - A HIGH
RHTW68          2-1/2D      CORE            SEARCH MEMORY.=
EVCA62                      CORRECTION      AND ADDENDUM.=
EETU67   ACKING AND         CORRELATION     =THE USE OF ASSOCIATIVE PROCESSORS IN RADAR TR
JKTT62     TARGET TRACK     CORRELATION     WITH A SEARCH MEMORY.=
PGAS64   MORY UTILIZING     CORRELATION     ADDRESSING.=A SEMIPERMANENT ME
WCAC68              A       COUPLE          MAGNETIC FILM DEVICE FOR ASSOCIATIVE MEMORIES.=
MYSP61    BY CAPACITIVE     COUPLING        =SEMI-PERMANENT STORAGE
HPEC         EVALUATION     CRITERIA        FOR ASSOCIATIVE MEMORIES.=
NBTC60              THE     CROSSED-FILM    CRYOTRON AND ITS APPLICATION TO DIGITAL COMPUTERS.=
HISC65   ACTERISTICS OF     CROSSED-FILM    CRYOTRON CIRCUITS.=SWITCHING CHAR
SNTW66       THREE-WIRE     CRYOELECTRIC    MEMORY SYSTEMS.=
BSCS65   ITY SENSING OF     CRYOELECTRIC    MEMORY PLANES.=CAV
CGMM66   NG METHODS FOR     CRYOELECTRIC    MEMORIES.=MANUFACTURI
BBCR64                J     CRYOELECTRIC    RANDOM ACCESS MEMORY, PHASE 2 10 ( 9 ) BIT MEMORY.=
BACM63                .     CRYOELECTRIC    MEMORIES.=
BACR64                      CRYOELECTRIC    RECEIVER TECHNIQUES.=
BACR66                .     CRYOELECTRIC    RANDOM ACCESS MEMORY - PHASE 3.=
CGMM67   NG METHODS FOR     CRYOELECTRIC    MEMORIES.=MANUFACTURI
BLCR65                      CRYOELECTRIC    RANDOM ACCESS MEMORY, PHASE 3.=
ARCM63                .     CRYOELECTRIC    MEMORIES.=
BCAL63   LARGE CAPACITY     CRYOELECTRIC    MEMORY WITH CAVITY SENSING.=A
BLCM64                      CRYOELECTRIC    MEMORIES.=
CLAC67              A       CRYOELECTRIC    DISTRIBUTED LOGIC MEMORY.=
PJPD68   PROCESSING VIA     CRYOELECTRICS   =PARALLEL DATA
MNAN68            A NEW     CRYOGENIC       MEMORY SYSTEM=
BBBC66          BASING      CRYOGENIC       COMPUTERS IN SPACE=
RJRO63       RESEARCH ON    CRYOGENIC       ASSOCIATIVE MEMORIES.=
YYAC66              A       CRYOGENIC       ASSOCIATIVE MEMORY FOR INFORMATION RETRIEVAL.=
PWDO68   LY ASSOCIATIVE     CRYOGENIC       DATA PROCESSOR.=DESIGN OF A FUL
```

TRFS61	TY STUDY FOR A	CRYOGENIC	ASSOCIATIVE MEMORY.=FEASIBILI
GMAC60	A	CRYOGENIC	MULTIPLE INSTANTANEOUS RESPONSE FILE.=
PJFA66	G OF 5000 WORD	CRYOGENIC	ASSOCIATIVE PROCESSOR.=FABRICATION AND TESTIN
IBCA		CRYOGENIC	ASSOCIATIVE MEMORY TECHNIQUES.=
RJRO63	RESEARCH ON	CRYOGENIC	ASSOCIATIVE MEMORIES.=
RWRO64	RESEARCH ON	CRYOGENIC	ASSOCIATIVE MEMORIES.=
RJRO63	RESEARCH ON	CRYOGENIC	ASSOCIATIVE MEMORIES.=
BBOO64	ERATION OF THE	CRYOGENIC	CONTINUOUS FILM MEMORY CELL.=OP
MRAC62	A	CRYOGENIC	' BETWEEN LIMITS ' ASSOCIATIVE MEMORY.=
YDDO61	A LARGE SCALE	CRYOGENIC	MEMORY.=DESIGN OF
AMGE62	G. E.	CRYOGENIC	ASSOCIATIVE MEMORY CIRCUIT DEVELOPED.=
GECM65		CRYOGENIC	MEMORY.=
GECA67		CRYOGENIC	ASSOCIATIVE MEMORY.=
GECM65		CRYOGENIC	MEMORY.=
IBCM65		CRYOGENIC	MEMORY SYSTEM.=
HHCM64		CRYOGENIC	MEMORY SYSTEMS.=
VRPF67	FOR FUTURE OF	CRYOGENIC	APPLICATIONS.=PREDICTIONS
RJCA64		CRYOGENIC	ASSOCIATIVE MEMORY RESEARCH.=
BLDO62	A LARGE-SCALE	CRYOGENIC	MEMORY SYSTEM.=DESIGN OF
YTAC67	A	CRYOGENIC	ASSOCIATIVE MEMORY.=
YTSD64	ATIC DESIGN OF	CRYOGENIC	LOGIC CIRCUITS.=SYSTEM
RWAM63	THMS AND THEIR	CRYOGENIC	IMPLEMENTATION.=ASSOCIATIVE MEMORY ALGORI
SRCA60		CRYOGENIC	ASSOCIATIVE MEMORY.=
STFS61	TY STUDY FOR A	CRYOGENIC	ASSOCIATIVE MEMORY.=FEASIBILI
PWDO64	LY ASSOCIATIVE	CRYOGENIC	DATA PROCESSOR.=DESIGN OF A FUL
YYAC66	A	CRYOGENIC	ASSOCIATIVE MEMORY SYSTEM FOR INFORMATION RETRIEVAL.=
RJCA64		CRYOGENIC	ASSOCIATIVE MEMORY TECHNIQUES.=
MHCR66		CRYOGENIC	RESEARCH.=
RGCA64		CRYOGENIC	ASSOCIATIVE PROCESSOR PLANE TEST AND EVALUATION.=
PFCT63		CRYOGENIC	TUBE FITTING.=
PJFA65	AND TESTING OF	CRYOGENIC	ASSOCIATIVE PROCESSOR PLANES.=FABRICATION
BRCA63		CRYOGENIC	ASSOCIATIVE PROCESSOR.=
PJND66	EVELOPMENTS IN	CRYOGENIC	DEVICES.=NEW D
ABCA64		CRYOGENIC	ASSOCIATIVE MEMORY TECHNIQUES.=
BBPO66	A SPACE-BASED	CRYOGENIC	COMPUTER.=PROSPECTS OF
PJFA67	G OF 5000 WORD	CRYOGENIC	ASSOCIATIVE PROCESSOR.=FABRICATION AND TESTIN
NFAC62	A	CRYOGENIC	DATA ADDRESSED MEMORY.=
RRAO62	AN ASSOCIATIVE	CRYOGENIC	COMPUTER.=AN ORGANIZATION OF
HRAO	APPLICATION OF	CRYOGENIC	TECHNIQUES TO COMPUTER TECHNOLOGY.=APPLIC
ENAO65	NALYSIS OF THE	CRYOGENIC	CONTINUOUS FILM MEMORY.=A
BBSO64	STRUCTURE OF A	CRYOGENIC	ASSOCIATIVE PROCESSOR.=STRUCT
RICM65		CRYOGENICS	MEMORY PLANE INTERCONNECTION TECHNIQUES.=
NVCA65		CRYOGENICS	- ACHIEVEMENT AND POTENTIAL.=
SSTF60	THIN FILM	CRYOTRON	CATALOG MEMORY.=
NECS67		CRYOTRON	STORAGE CELLS FOR RANDOM ACCESS MEMORIES.=
LACA65		CRYOTRON	ASSOCIATIVE MEMORY CELL.=
RDTD66	ESIGN OF LARGE	CRYOTRON	MEMORIES.=THE D
SATW59	THE WOVEN	CRYOTRON	MEMORY. =
YCAS64	A STUDY OF	CRYOTRON	ASSOCIATIVE MEMORY IN DIGITAL SYSTEMS.=
RJCR64		CRYOTRON	RESEARCH.=
SAAC62	A	CRYOTRON	MEMORY CELL.=
SMTC57	THE	CRYOTRON	CATALOG MEMORY SYSTEM.=
SSTF60	THIN-FILM	CRYOTRON	CATALOG MEMORY.=
WBCA63	CRYOTRONS AND	CRYOTRON	CIRCUITS, A REVIEW.=
PECM57		CRYOTRON	MEMORY SYSTEMS.=
LICL66		CRYOTRON	LOGIC STUDIES.=
HMCS60		CRYOTRON	STORAGE, ARITHMETIC AND LOGICAL CIRCUITS.=

FOAH66	A HYBRID	CRYOTRON	TECHNOLOGY: I - CIRCUITS AND DEVICES.=
NBTC60	E CROSSED-FILM	CRYOTRON	AND ITS APPLICATION TO DIGITAL COMPUTERS.=TH
BJCC63		CRYOTRON	COMPUTER TECHNIQUES.=
NBAI60	IMPROVED FILM	CRYOTRON	AND ITS APPLICATION TO DIGITAL COMPUTERS.=AN
HLSC65	F CROSSED-FILM	CRYOTRON	CIRCUITS.=SWITCHING CHARACTERISTICS O
AOAH66	1 HYBRID	CRYOTRON	TECHNOLOGY: 2 - FABRICATION.=
VITA69	NALYSIS OF THE	CRYOTRONIC	ASSOCIATIVE ELEMENT CONTROLLED BY MONOPOLAR CURRENTS.=THE A
IWTC62	THE CASE FOR	CRYOTRONICS	?.=
AEAO62	PPLICATIONS OF	CRYOTRONS	TO THE HIGH-SPEED COMPUTER.=A
CMCO60	ISTICS OF FILM	CRYOTRONS	=CHARACTER
SSTF60	THIN-FILM	CRYOTRONS	=
WBCA63		CRYOTRONS	AND CRYOTRON CIRCUITS, A REVIEW.=
NFDA62	SING THIN-FILM	CRYOTRONS	=DATA ADDRESSED MEMORY U
BACC61	COINCIDENT	CURRENT	SUPERCONDUCTIVE MEMORY.=
VITA69	D BY MONOPOLAR	CURRENTS	=THE ANALYSIS OF THE CRYOTRONIC ASSOCIATIVE ELEMENT CONTROLLE
YYAC66	A	CUTPOINT	CELLULAR ASSOCIATIVE MEMORY.=
NRCC64		CUTPOINT	CELLULAR LOGIC.=
YYAC66	A	CUTPOINT	CELLULAR ASSOCIATIVE MEMORY.=
IYAI67	100 NANOSECOND	CYCLE	TIME.=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMORY SYSTEM WITH
IYAI	00-NANOSECONDS	CYCLE	TIME.=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMORY WITH 1
MEMO67	ONAL SYSTEMS -	CYCLIC	TO ACYCLIC GRAPH TRANSFORMATIONS.=MODELS OF COMPUTATI
WTCA68		CYLINDERS-A	DATA STRUCTURE CONCEPT BASED ON RINGS=
KASC67	CAPACITY THIN	CYLINDRICAL	MAGNETIC FILM STORAGE SYSTEMS.=SMALL
BHAA62	VE MACHINE FOR	DEALING	WITH THE VISUAL FIELD AND SOME OF ITS BIOLOGICAL IMPLICATIONS.=AN ASSOCIATI
CVOR67	TRIEVAL FROM A	DECIMAL	ASSOCIATIVE MEMORY.=ORDERED PE
ASTA69	WITH	DEDUCTIVE	CAPABILITIES=TRAMP: AN INTERPRETIVE ASSOCIATIVE PROCESSOR
KAAO69	AC-IV TO URBAN	DEFENSE	RADAR PROBLEM.=APPLICATION OF ILLI
KAAO68	AC-IV TO URBAN	DEFENSE	RADAR PROBLEM.=APPLICATION OF ILLI
CSDT66	ECHNIQUES OF A	DELAY-LINE	CONTENT-ADDRESSED MEMORY.=DESIGN T
BKAA69	EMORY PARALLEL	DELTIC	REALIZATION FOR ACTIVE SONAR SIGNAL PROCESSING.=AN ASSOCIATIVE M
AGAD69	A	DESCRIPTION	OF THE ILLIAC-IV OPERATING SYSTEM.=
CCAM65	PUTER SYSTEM :	DESCRIPTION	AND SELECTED NAVAL APPLICATIONS.=ASSOCIATIVE MEMORY COM
BHIL65	C-II - A SHORT	DESCRIPTION	AND ANNOTATED BIBLIOGRAPHY.=ILLIA
KKAP66	A PROGRAMMERS	DESCRIPTION	OF L6.=
SJPD64	PROGRAM	DESCRIPTION	OF PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC
HPAM65	OMPUTER SYSTEM	DESCRIPTION	AND SELECTED NAVAL APPLICATIONS.=ASSOCIATIVE MEMORY C
BHAT67	EXTRACTING NEW	DESCRIPTORS	OF SHAPES.=A TRANSFORMATION FOR
RSHD69	HARDWARE	DESIGN	REFLECTING SOFTWARE REQUIREMENTS=
NRPC69	FOR LOGIC	DESIGN	PROBLEMS=PARALLEL COMPUTING STRUCTURES AND ALGORITHMS
NPAD69	A	DESIGN	FOR A FAST COMPUTER FOR SCIENTIFIC CALCULATIONS=
PWDO65		DESIGN	OF A FULLY ASSOCIATIVE CRYOGENIC DATA PROCESSOR.=
GHOT	ON THE	DESIGN	OF A MULTI-LIST INFORMATION PROCESSING SYSTEM=
KWTD69	THE	DESIGN	OF A HIGHLY PARALLEL COMPUTER ORGANIZATION.=
HMTM60	I PERCEPTION -	DESIGN	AND PERFORMANCE.=THE MARK
CCTL61	THE LOGICAL	DESIGN	OF A HOLLAND MACHINE.=
MBDO		DESIGN	OF A PATTERN RECOGNITION DIGITAL COMPUTER - PART 1 : GENERAL INTRODUCTION.=
SPPA62	AL AND LOGICAL	DESIGN	OF A HIGHLY PARALLEL COMPUTER.=PHYSIC
RDTD66	THE	DESIGN	OF LARGE CRYOTRON MEMORIES.=
YDDO61		DESIGN	OF A LARGE SCALE CRYOGENIC MEMORY.=
BJTL68	THE LOGICAL	DESIGN	OF THE NEBULA COMPUTER.=
GPIO62	ES AND MACHINE	DESIGN	=INTERACTIONS OF COMPUTER LANGUAG
DPDF63		DESIGN	FOR AN ASSOCIATIVE COMPUTER.=
BEDO61		DESIGN	OF A FIXED-PLUS-VARIABLE STRUCTURE COMPUTER FOR THE SOLUTION OF A DIFFUSION EQ
YTSD64	SYSTEMATIC	DESIGN	OF CRYOGENIC LOGIC CIRCUITS.=
BCCI62	RATIONS IN THE	DESIGN	OF A COMPUTER WITH HIGH LOGIC-TO-MEMORY SPEED RATIO.=CONSIDE
WDCA68	AIDED STRATEGY	DESIGN	USING ADAPTIVE AND ASSOCIATIVE TECHNIQUES.=COMPUTER=
GJCD67	COMPUTER AIDED	DESIGN	: A SURVEY.=COMPOUND DATA STRUCTURE FOR

```
RPDA68                          DESIGN          AND EVALUATION OF A GLASS DELAY LINE CONTENT-ADDRESSABLE MEMORY SYSTEM.=
SPPA63  ROGRAMMING AND          DESIGN          CONSIDERATIONS OF A HIGHLY PARALLEL COMPUTER.=P
YHDO64                  J       DESIGN          OF AN EXPERIMENTAL MULTIPLE INSTANTANEOUS RESPONSE FILE.=
SDSD64          SYSTEM          DESIGN          OF A SEARCH MEMORY.=
BLDO62                          DESIGN          OF A LARGE-SCALE CRYOGENIC MEMORY SYSTEM.=
JSTD62              THE         DESIGN          OF A 4096 WORD ONE MICROSECOND MAGNETIC FILM STORE.=
PWDO64                          DESIGN          OF A FULLY ASSOCIATIVE CRYOGENIC DATA PROCESSOR.=
RCMF61  IC FILM MEMORY          DESIGN          =MAGNET
MIRA68  REQUIRED TO             DESIGN          AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS.=RESEARCH AND DEVELOPMENT OF TH
CSDT66                          DESIGN          TECHNIQUES OF A DELAY-LINE CONTENT-ADDRESSED MEMORY.=
CMAM63  OCESSOR SYSTEM          DESIGN          =A MULTIPR
NGSA63  EM AND CIRCUIT          DESIGNS         FOR THE TOBERMORY PERCEPTION.=SYST
CYAD65                  A       DESTRUCTIVE-READOUT ASSOCIATIVE MEMORY.=
MWTA68  CRAFT CONFLICT          DETECTION       =THE ASSOCIATIVE PROCESSOR IN AIR
WHPF63  RED SEQUENTIAL          DETECTION       OF SIMULTANEOUS MULTIPLE RESPONSES.=PROPOSAL FOR ORDE
USPD59          PATTERN         DETECTION       AND RECOGNITION.=
HWSM66  READOUT OF THE          DETECTOR        MATRIX.=SIMULTANEOUS MULTIPLE RESPONSE IN ASSOCIATIVE MEMORIES AND
KMPO66  ONS:                    DETERMINACY      TERMINATION, QUEUEING.=PROPERTIES OF A MODEL FOR PARRALLEL COMPUTATI
FCDO68                          DETERMINATION   OF PRIORITY IN ASSOCIATIVE MEMORIES.=
WAED64          EXTREME         DETERMINATION   AND ORDERED RETRIEVAL IN SEARCH MEMORIES.=
RFST64          STUDY TO        DETERMINE       THE APPLICABILITY OF THE SOLOMON COMPUTER TO COMMAND AND CONTROL. VOLUME I. IN
RFST64          STUDY TO        DETERMINE       THE APPLICABILITY OF THE SOLOMON COMPUTER TO COMMAND AND CONTROL.=
WDSA64  VESTIGATION TO          DEVELOP         COMPILER TECHNIQUES REQUIRED FOR PROGRAMMING THE PARALLEL NETWORK COMPUTER.=ST
AMGE62  MEMORY CIRCUIT          DEVELOPED       =G. F. CRYOGENIC ASSOCIATIVE
YHDO64                          DEVELOPMENT     OF A MULTIPLE INSTANTANEOUS RESPONSE FILE : THE AN/GSQ-81 DOCUMENT DATA INDEXI
MIRA68    RESEARCH AND          DEVELOPMENT     OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER
PSED68          ELEMENT         DEVELOPMENT     FOR ADVANCED ASSOCIATIVE MEMORIES.=
HRED66          ELEMENT         DEVELOPMENT     FOR ADVANCED ASSOCIATIVE MEMORIES.=
HHED67          ELEMENT         DEVELOPMENT     FOR ADVANCED ASSOCIATIVE MEMORIES.=
BGED67          ELEMENT         DEVELOPMENT     FOR ADVANCED ASSOCIATIVE MEMORIES.=
CSSI63   OF NEW MEMORY          DEVELOPMENTS    =SYSTEMS IMPLICATIONS
YDRD61          RECENT          DEVELOPMENTS    IN HIGH-SPEED SUPERCONDUCTING DEVICES.=
RJCM62  OSSIBLE FUTURE          DEVELOPMENTS    =COMPUTER MEMORIES - P
RJND66              NEW         DEVELOPMENTS    IN CRYOGENIC DEVICES.=
SGAN60  ON OF A MEMORY          DEVICE          =A NEW PRINCIPLE FOR THE CONSTRUCTI
PFAI69  ATION-TRANSFER          DEVICE           AND THE OPERATING FEATURES OF THE EXPLORATORY CONTENT ADDRESSABLE MEMORY SYST
WCAC68   MAGNETIC FILM          DEVICE          FOR ASSOCIATIVE MEMORIES.=A COUPLE
WCAM69  CIATIVE MEMORY          DEVICE          3466632.=ASSO
WCAM69  CIATIVE MEMORY          DEVICE          3466631.=ASSO
SAAD64  EMORIES FROM A          DEVICE          POINT OF VIEW.=A DISCUSSION OF ASSOCIATIVE M
KPTR63  MANENT STORAGE          DEVICE          =THE ROPE MEMORY - A PER
SASS62  ES AND STORAGE          DEVICES         =SUPERCONDUCTIVE SWITCH
BDMA    MAGNETIC LOGIC          DEVICES         =MULTI-APERTURE
YDRD61  UPERCONDUCTING          DEVICES         =RECENT DEVELOPMENTS IN HIGH-SPEED S
OJSF63          DISPLAY         DEVICES         =SWITCHING FUNCTIONS FOR SIMPLIFIED DATA RETRIEVAL AND
PJND66  S IN CRYOGENIC          DEVICES         =NEW DEVELOPMENT
FOAH66  - CIRCUITS AND          DEVICES         =A HYBRID CRYOTRON TECHNOLOGY: I
MYDS68                          DIAGNOSTIC      SEQUENCE GENERATOR FOR ILLIAC-IV PROCESSING ELEMENT.=
KKDT68                          DIAGNOSTIC      TEST PATTERNS AND SEQUENCES FOR ILLIAC-IV PROCESSING ELEMENT.=
BBPO62  ABOLIC PARTIAL          DIFFERENTIAL    EQUATIONS.=PROPERTIES OF A VARIABLE STRUCTURE COMPUTER SYSTEM IN THE SOLUTION
BEDO61   SOLUTION OF A          DIFFUSION       EQUATION.=DESIGN OF A FIXED-PLUS-VARIABLE STRUCTURE COMPUTER FOR THE
SJAI68  ENERAL-PURPOSE          DIGITAL          COMPUTER=AN ITERATIVELY STRUCTURED G
FKBD67      BROOKHAVEN          DIGITAL         COMMUNICATIONS NETWORK =
SJAO68  ENERAL-PURPOSE          DIGITAL         COMPUTER=ASYNCHRONOUS OPERATION OF AN ITERATIVELY STRUCTURED G
ERTA69  ANCED AVIONICS          DIGITAL         COMPUTER.=THE ADV
MBDO    RN RECOGNITION          DIGITAL         COMPUTER - PART 1 : GENERAL INTRODUCTION.=DESIGN OF A PATTE
RPAA67  R CONVENTIONAL          DIGITAL          COMPUTERS=AN ASSOCIATIVE PROCESSING SYSTEM FO
```

ARAS64	VESTIGATION IN	DIGITAL	TECHNOLOGY RESEARCH.=ANNUAL SUMMARY REPORT OF IN
MHIO62	LARGE-CAPACITY	DIGITAL	MEMORIES. =INVESTIGATION OF STORAGE AND ACCESS TECHNIQUES SUITABLE FOR USE IN
MSFI61	VESTIGATION OF	DIGITAL	COMPUTER STORAGE AND ACCESS TECHNIQUES.=FUNDAMENTAL IN
GHAN61	UIREMENTS OF A	DIGITAL	COMPUTER FOR THE MANIPULATION OF LIST STRUCTURES.=A NOTE ON THE SYSTEM REQ
CELA62	ABLE STRUCTURE	DIGITAL	COMPUTER.=LOGARITHMIC AND EXPONENTIAL FUNCTION EVALUATION IN A VARI
EGDT64	.	DIGITAL	TECHNOLOGY RESEARCH.=
SJAI66	ELY STRUCTURED	DIGITAL	COMPUTER.=AN ITERATIV
SDAP67	NG APPROACH TO	DIGITAL	SIMULATION.=A PARALLEL COMPUTI
RFAA67	R CONVENTIONAL	DIGITAL	COMPUTERS.=AN ASSOCIATIVE PROCESSING SYSTEM FO
YCAS64	TIVE MEMORY IN	DIGITAL	SYSTEMS.=A STUDY OF CRYOTRON ASSOCIA
WTSA60	NUAL REPORT ON	DIGITAL	COMPUTER SYSTEMS STUDIES.=SEMI-AN
KMAM62	MECHANISMS IN	DIGITAL	' CONCEPT ' PROCESSING. =ADAPTIVE
NBAI60	APPLICATION TO	DIGITAL	COMPUTERS.=AN IMPROVED FILM CRYOTRON AND ITS
NBTC60	APPLICATION TO	DIGITAL	COMPUTERS.=THE CROSSED-FILM CRYOTRON AND ITS
BRNA66	NEBULA: A	DIGITAL	COMPUTER USING A 20 MC GLASS DELAY LINE MEMORY.=
NSND62	NANOPHILE	DIGITAL	ORGANIZATIONS.=
CBDA62		DIMENSION	AN ASSOCIATIVE MEMORY.=
CBDI63		DIMENSIONING	IN AN ASSOCIATIVE MEMORY. =
WRAT	NSISTOR-TUNNEL	DIODE	CELL FOR ASSOCIATIVE MEMORIES AND MULTIPLE-WORD ACCESS MEMORIES.=A TRA
CRAT62	A TUNNEL	DIODE	ASSOCIATIVE MEMORY.=
LBFA63	ORATED ORGANIC	DIODE	ARRAYS.=FIXED ASSOCIATIVE MEMORY USING EVAP
T1HS61	RY USES TUNNEL	DIODES	=HIGH-SPEED MEMO
BKSA68	A COMPUTER FOR	DIRECT	EXECUTION OF LIST PROCESSING LANGUAGE=STUDY OF
SRSA65	OF MEANING IN	DIRECTED	GRAPH STRUCTURES.=STORAGE AND RETRIEVAL OF ASPECTS
HHAD63	A	DIRECTORY	CONTROL SYSTEM FOR MULTIPROGRAMMING.=
BKDO65		DIRECTORY	ORGANIZATION FOR A STORAGE SYSTEM.=
SBDR65		DIRECT-RECORDING	MEGACHANNEL ANALYZER THROUGH ASSOCIATIVE PROGRAMMING OF A SMALL COMPUTER.=
RDSO68	OLUTION OF THE	DIRICHLET	PROBLEM ON A SIMULATED PARALLEL PROCESSING SYSTEM.=S
CAOT68	CONVERGENCE OF	DISCRETE	APPROXIMATIONS TO THE NAVIER STOKES EQUATIONS.=ON THE
SAAD64	A	DISCUSSION	OF ASSOCIATIVE MEMORIES FROM A DEVICE POINT OF VIEW.=
PTAM67	COLLECTION AND	DISPLAY	SYSTEM.=ASSOCIATIVE MEMORY FOR
OJSF63	EVAL AND	DISPLAY	DEVICES.=SWITCHING FUNCTIONS FOR SIMPLIFIED DATA RETRI
LGTA69	URE OF A LARGE	DISTRIBUTED	LOGIC. ASSOCIATIVE MEMORY=THE ARCHITECT
LGTA69	URE OF A LARGE	DISTRIBUTED	LOGIC ASSOCIATIVE PROCESSOR=THE ARCHITECT
SJDL69		DISTRIBUTED	LOGIC MEMORY COMPUTER FOR PROCESS CONTROL=
TRFT66	FABRICATION OF	DISTRIBUTED	LOGIC NETWORKS.=FABRICATION TECHNIQUES FOR BATCH
LCCA68	DDRESSABLE AND	DISTRIBUTED	LOGIC MEMORIES. =CONTENT A
LPAC64	NT ADDRESSABLE	DISTRIBUTED	LOGIC MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=A CONTE
SEAC64	NT-ADDRESSABLE	DISTRIBUTED	LOGIC MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=A CONTE
SGAO64	TIVELY ADDRESS	DISTRIBUTED	MEMORY.=APPLICATION OF AN ASSOCIA
CIAC67	A CRYOELECTRIC	DISTRIBUTED	LOGIC MEMORY.=A CRYO
CGBP65	PROCESSING IN	DISTRIBUTED	LOGIC MEMORY.=BULK
LPAC63	NT ADDRESSABLE	DISTRIBUTED	LOGIC MEMORY WITH APPLICATION TO INFORMATION RETRIEVAL.=A CONTE
ERCA64	NT-ADDRESSABLE	DISTRIBUTED-LOGIC	MEMORIES.=CONTE
LCIC62	S, BASIS FOR A	DISTURBED	LOGIC COMPUTER.=INTERCOMMUNICATING CELL
CHEO65	ONOMICS OF THE	DLM	A BATCH-FABRICATABLE PARALLEL COMPUTER.=EC
YHDO64	THE AN/GSQ-81	DOCUMENT	DATA INDEXING SET.=DEVELOPMENT OF A MULTIPLE INSTANTANEOUS RESPONSE FILE :
GVRO64	R MEMORIES FOR	DOCUMENT	PROCESSING.=REQUIREMENTS OF FUTURE COMPUTE
SDAP71	ESSING OF LINE	DRAWINGS	=ASSOCIATIVE PROC
GKAC67	US FILM MEMORY	DRIVEN	BY MULTIPLE COINCIDENT PULSES=A CONTINUO
RDBD67	BIT	DRIVER	=
LHTA69	THE ASP -	DYNABIT	SYSTEM : AN ASSOCIATIVE PROCESSOR USING BULK STORAGE.=
NHCR68	IZATION OF THE	DYNAMIC	PROGRAMMING ALGORITHM, ANNUAL PROGRESS REPORT.=CELLULAR REAL
CYAO65	SED MEMORY FOR	DYNAMIC	STORAGE ALLOCATION.=APPLICATION OF CONTENT-ADDRES
AETF61	UTER SYSTEM IN	DYNAMIC	PROGRAMMING FORMULATION OF CONTROL SYSTEM OPTIMIZATION PROBLEMS.=THE FIXED-PL
CHEO65		ECONOMICS	OF THE DLM, A BATCH-FABRICATABLE PARALLEL COMPUTER.=
BEAE63	LUATION OF THE	EFFECTIVENESS	OF PARALLEL PROCESSING.=AN EVA

PFAI69	EATURES OF THE	EXPLORATORY	CONTENT ADDRESSABLE MEMORY SYSTEM.=AN IMPROVED FIELD-CONTROLLED POLARIZATION-T
CFLA62	OGARITHMIC AND	EXPONENTIAL	FUNCTION EVALUATION IN A VARIABLE STRUCTURE DIGITAL COMPUTER.=L
REPE69	PARALLELISM	EXPOSURE	AND EXPLOITATION.=
BBC068	OF ARITHMETIC	EXPRESSIONS	FOR PARALLEL COMPUTATIONS.=COMPILATION
BHAT67	SFORMATION FOR	EXTRACTING	NEW DESCRIPTORS OF SHAPES.=A TRAN
WAED64		EXTREME	DETERMINATION AND ORDERED RETRIEVAL IN SEARCH MEMORIES.=
MIRA68	DESIGN AND	FABRICATE	ULTRAHIGH-SPEED COMPUTER SYSTEMS.=RESEARCH AND DEVELOPMENT OF THE TECHNOLOGIES
PJFA66		FABRICATION	AND TESTING OF 5000 WORD CRYOGENIC ASSOCIATIVE PROCESSOR.=
NBHS	WO-DIMENSIONAL	FABRICATION	=HIGH-SPEED SUPERCONDUCTIVE SWITCHING ELEMENT SUITABLE FOR T
SLMF62	MASS	FABRICATION	HIGHLY PARALLEL SYSTEMS, AND ASSOCIATIVE LOGIC.=
TRFT66	QUES FOR BATCH	FABRICATION	OF DISTRIBUTED LOGIC NETWORKS.=FABRICATION TECHNI
TRFT66		FABRICATION	TECHNIQUES FOR BATCH FABRICATION OF DISTRIBUTED LOGIC NETWORKS.=
PJFA67		FABRICATION	AND TESTING OF 5000 WORD CRYOGENIC ASSOCIATIVE PROCESSOR.=
PJFA65		FABRICATION	AND TESTING OF CRYOGENIC ASSOCIATIVE PROCESSOR PLANES.=
AOAH66	ECHNOLOGY: 2 -	FABRICATION	=1 HYBRID CRYOTRON T
WRAP65	ROBLEM SOLVING	FACILITY	=A P
CWSO	STEM OPERATION	FACTORS	=SY
MPAD69	A DESIGN FOR A	FAST	COMPUTER FOR SCIENTIFIC CALCULATIONS=A DESI
SPAF69	A	FAST	FLEXIBLE HIGHLY PARALLEL ASSOCIATIVE PROCESSOR=
WMAP69	ESSING FOR THE	FAST	FOURIER TRANSFORM.=ASSOCIATIVE PARALLEL PROC
LAAA61	N FOR A SMALL,	FAST	ASSOCIATIVE MEMORY TO REDUCE THE ACCESS TIME FOR INSTRUCTIONS IN LOOPS.=AN APP
LWSA68	SOME ARGUMENTS	FAVORING	NON-CONVENTIONAL TYPES OF COMPUTERS.=SOME A
TRFS61		FEASIBILITY	STUDY FOR A CRYOGENIC ASSOCIATIVE MEMORY.=
STFS61		FEASIBILITY	STUDY FOR A CRYOGENIC ASSOCIATIVE MEMORY.=
PFAI69	THE OPERATING	FEATURES	OF THE EXPLORATORY CONTENT ADDRESSABLE MEMORY SYSTEM.=AN IMPROVED FIELD-CONTRO
CJRO64	RESEARCH ON	FERRET	ASSOCIATIVE MEMORY.=
RWFM68		FERRITE	MEMORY SYSTEMS.=
SRLF63	LAMINATED	FERRITE	MEMORY.=
BHAA62	ITH THE VISUAL	FIELD	AND SOME OF ITS BIOLOGICAL IMPLICATIONS.=AN ASSOCIATIVE MACHINE FOR DEALING W
VVPO58	ON OF MAGNETIC	FIELDS	THROUGH THIN SUPERCONDUCTING FILMS.=PENETRATI
PFAI69	AN IMPROVED	FIELD-CONTROLLED	POLARIZATION-TRANSFER DEVICE AND THE OPERATING FEATURES OF THE EXPLORATORY CON
YHDO64	NEOUS RESPONSE	FILE	: THE AN/GSQ-81 DOCUMENT DATA INDEXING SET.=DEVELOPMENT OF A MULTIPLE INSTANTA
GMAC60	NEOUS RESPONSE	FILE	=A CRYOGENIC MULTIPLE INSTANTA
MSFO67		FILE	ORGANIZATION AND DATA MANAGEMENT. =
LWAM	A MULTIPLE	FILE	ORGANIZATION FOR INFORMATION RETRIEVAL SYSTEMS.=
HCMR61	FLUX PATH PER	FILE	ITEM.=MAGNETIC REALIZATIONS FOR MIRF EMPLOYING ONE
GGMI61	NEOUS RESPONSE	FILE	=MULTIPLE INSTANTA
FKAA64	NEOUS RESPONSE	FILE	=AN ANALYSIS OF THE MULTIPLE INSTANTA
YHDO64	OUS RESPONSE	FILE	=DESIGN OF AN EXPERIMENTAL MULTIPLE INSTANTANE
CJOA67	OF ASSOCIATIVE	FILE	PROCESSORS.=ORGANIZATION AND APPLICATIONS
VEMR61	CTIVE PATH PER	FILE	ITEM.=MAGNETIC REALIZATION FOR MIRF EMPLOYING ONE CONDU
FGAM61	LEL SEARCH	FILE	=A METHOD FOR RESOLVING MULTIPLE RESPONSES IN A PARAL
GFLT61	GEST WORD IN A	FILE	USING A MODIFIED MEMORY.=LOCATING THE LAR
NJMI61	NEOUS RESPONSE	FILE	).=MIRF (MULTIPLE INSTANTA
GGLF62	LARGE	FILES	FOR INFORMATION RETRIEVAL BASED ON SIMULTANEOUS INTERROGATION OF ALL ITEMS.=
GHLF61	LARGE	FILES	FOR INFORMATION RETRIEVAL BASED ON SIMULTANEOUS INTERROGATION OF ALL ITEMS.=
GKAC	A CONTINOUS	FILM	MEMORY CELL FOR SUPERCONDUCTIVE ASSOCIATIVE MEMORIES=
KHSA67	IVE CONTINUOUS	FILM	MEMORY CELLS=SUPERCONDUCT
GKAW	ING CONTINUOUS	FILM	MEMORY=A WORD-ORGANIZED SUPERCONDUCT
LMTF69	THIN	FILM	ASSOCIATIVE MEMORY.=
SSTF60	THIN	FILM	CRYOTRON CATALOG MEMORY.=
GKAC67	A CONTINUOUS	FILM	MEMORY DRIVEN BY MULTIPLE COINCIDENT PULSES=
PZMF68	MAGNETIC	FILM	MEMORY SYSTEMS.=
WCAC68	OUPLE MAGNETIC	FILM	DEVICE FOR ASSOCIATIVE MEMORIES.=A C
WAAT65	THIN MAGNETIC	FILM	COMPUTER MEMORY USING A REASONANT ABSORPTION NON-DESTRUCTIVE READ-OUT TECHNIQU
BBOO64	NIC CONTINUOUS	FILM	MEMORY CELL.=OPERATION OF THE CRYOGE
DPPW64	WIRE MAGNETIC	FILM	MEMORIES.=PLATED

GASO69	UDY OF MISSION	EFFECTIVENESS	OF ASSOCIATIVE PROCESSOR IN AWACS.=ST
CRIO63	NCE OF THERMAL	EFFECTS	ON THE OPERATING SPEED OF SUPERCONDUCTING COMPUTER ELEMENTS.=INFLUE
NZET68		EFFORTS	TOWARD AN ASSOCIATIVE LEARNING INSTRUCTIONAL SYSTEM=
EVOO62	COMPUTATION OF	EIGENVALUES	AND EIGENVECTORS OF REAL SYMMETRIC MATRICES.=ORGANIZATION OF A ' FIXED-PLUS-VA
EVOO62	IGENVALUES AND	EIGENVECTORS	OF REAL SYMMETRIC MATRICES.=ORGANIZATION OF A ' FIXED-PLUS-VARIABLE ' STRUCTUR
HSSO64	STUDY OF	ELASTIC	SWITCHING FOR ASSOCIATIVE MEMORY SYSTEMS.=
SKES60		ELASTIC	SWITCHING PROPERTIES OF SOME SQUARE LOOP MATERIALS IN TOROIDAL STRUCTURES.=
LTEM60		ELECTRODEPOSITED	MEMORY ELEMENTS FOR A NON-DESTRUCTIVE MEMORY.=
RDFH65	E HARDWARE FOR	ELECTRONIC	INFORMATION-HANDLING SYSTEMS.=FUTUR
NKES67		ELECTRONIC	SOLID STATE COMPONENTS, PART 4.=
SHCO67	AGNETO- OR	ELECTRO-OPTICAL	INTERROGATION.'=COMMENT ON ' CONTENT-ADDRESSED MEMORY USING M
SHCA66	NG MAGNETO- OR	ELECTRO-OPTICAL	INTERROGATION.=CONTENT-ADDRESSED MEMORY USI
VITA69	IC ASSOCIATIVE	ELEMENT	CONTROLLED BY MONOPOLAR CURRENTS.=THE ANALYSIS OF THE CRYOTRON
DRTI69	-IV PROCESSING	ELEMENT	=THE ILLIAC
ABHS	TIVE SWITCHING	ELEMENT	SUITABLE FOR TWO-DIMENSIONAL FABRICATION.=HIGH-SPEED SUPERCONDUC
DRTI69	-IV PROCESSING	ELEMENT	=THE ILLIAC
AFBI65	SOCIATIVE	ELEMENT	=BILOC - A HIGH SPEED NDRO ONE CORE PER BIT AS
NYDS68	ROCESSING	ELEMENT	=DIAGNOSTIC SEQUENCE GENERATOR FOR ILLIAC-IV P
TKAT61	RUCTIVE MEMORY	ELEMENT	USING BIAS RESTORATION.=A TOROIDAL NONDEST
BDNM60	MAGNETIC LOGIC	ELEMENT	=NEW MULTI-APERTURE
HHED67		ELEMENT	DEVELOPMENT FOR ADVANCED ASSOCIATIVE MEMORIES.=
BGED67		ELEMENT	DEVELOPMENT FOR ADVANCED ASSOCIATIVE MEMORIES.=
HBED66		ELEMENT	DEVELOPMENT FOR ADVANCED ASSOCIATIVE MEMORIES.=
KKDT68	PROCESSING	ELEMENT	=DIAGNOSTIC TEST PATTERNS AND SEQUENCES FOR ILLIAC-IV
PSED68		ELEMENT	DEVELOPMENT FOR ADVANCED ASSOCIATIVE MEMORIES.=
WWBH59	NETIC COMPUTER	ELEMENT	=BIAX HIGH-SPEED MAG
FSGO62	LIZATION OF AN	ELEMENTARY	PERCEIVING AND MEMORIZING MACHINE.=GENERA
NSAM63	IZATION FOR AN	ELEMENTARY	LIST PROCESSING COMPUTER.=A MEMORY ORGAN
NHRO64	TURE COMPUTING	ELEMENTS	=RESEARCH ON LOW TEMPERA
LTEM60	POSITED MEMORY	ELEMENTS	FOR A NON-DESTRUCTIVE MEMORY.=ELECTRODE
SHRO63	H ON BIAX TYPE	ELEMENTS	AND ASSOCIATED CIRCUITS.=RESEARC
CRIO63	CTING COMPUTER	ELEMENTS	=INFLUENCE OF THERMAL EFFECTS ON THE OPERATING SPEED OF SUPERCONDU
KMSP64	N SCIENCE WITH	EMPHASIS	ON ADAPTATION TO USE THROUGH MAN-MACHINE INTERACTION.=SOME PROBLEMS IN INFORMA
HCMR61	TIONS FOR MIRF	EMPLOYING	ONE FLUX PATH PER FILE ITEM.=MAGNETIC REALIZA
VEMR61	ATION FOR MIRF	EMPLOYING	ONE CONDUCTIVE PATH PER FILE ITEM.=MAGNETIC REALIZ
BEDO61	OF A DIFFUSION	EQUATION	=DESIGN OF A FIXED-PLUS-VARIABLE STRUCTURE COMPUTER FOR THE SOLUTION
CAOT68	NAVIER STOKES	EQUATIONS	=ON THE CONVERGENCE OF DISCRETE APPROXIMATIONS TO THE
BBPO62	L DIFFERENTIAL	EQUATIONS	=PROPERTIES OF A VARIABLE STRUCTURE COMPUTER SYSTEM IN THE SOLUTION OF PARABOL
BHPA69	REPARATION AND	EVALUATION	OF COMPUTER PROGRAMS FOR PARALLEL PROCESSING SYSTEMS.=P
BSLS68	SIMULATION AND	EVALUATION	=LARGE SCALE INFORMATION PROCESSING SYSTEMS : MODEL BUILDING,
BEAE63	AN	EVALUATION	OF THE EFFECTIVENESS OF PARALLEL PROCESSING.=
HPEC		EVALUATION	CRITERIA FOR ASSOCIATIVE MEMORIES.=
CELA62	NTIAL FUNCTION	EVALUATION	IN A VARIABLE STRUCTURE DIGITAL COMPUTER.=LOGARITHMIC AND EXPONE
RPDA68	DESIGN AND	EVALUATION	OF A GLASS DELAY LINE CONTENT-ADDRESSABLE MEMORY SYSTEM.=
RPEO67		EVALUATION	OF THREE CONTENT-ADDRESSABLE MEMORY SYSTEMS USING GLASS DELAY LINES.=
RGCA64	PLANE TEST AND	EVALUATION	=CRYOGENIC ASSOCIATIVE PROCESSOR
AJEO61		EVALUATION	OF SYSTEMS USING ASSOCIATIVE MEMORIES.=
LBFA63	E MEMORY USING	EVAPORATED	ORGANIC DIODE ARRAYS.=FIXED ASSOCIATIV
KMEO67		EVOLUTION	OF COMPUTER SYSTEMS TO PERFORM PARALLEL PROCESSING.=
BFOT	ON THE	EVOLUTION	OF AUTONOMY FOR AN ASSOCIATIVE MEMORY.=
HJAU59	ER, CAPABLE OF	EXECUTING	AN ARBITRARY NUMBER OF SUB-PROGRAMS SIMULTANEOUSLY.=A UNIVERSAL COMPUT
BKSA68	TER FOR DIRECT	EXECUTION	OF LIST PROCESSING LANGUAGE=STUDY OF A COMPU
LPAE65	AN	EXPERIMENTAL	SYNTAX-DIRECTED DATA STRUCTURE LANGUAGE.=
YHDO64	DESIGN OF AN	EXPERIMENTAL	MULTIPLE INSTANTANEOUS RESPONSE FILE.=
GMEA65		EXPERIMENTAL	AND THEORETICAL ASPECTS OF THE SUPERCONDUCTING CONTINUOUS FILM STORE.=
ACTC65	RDS CONTROLLED	EXPERIMENTS	IN THE CONSTRUCTION OF AN ADAPTIVE MAN-MACHINE ASSOCIATIVE MEMORY FOR INFORMAT
REPE69	M EXPOSURE AND	EXPLOITATION	=PARALLELIS

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GAAG67          ADVANCED        GENERAL-PURPOSE  COMPUTER ORGANIZATIONS.=
CETN62          THE NEXT        GENERATION       OF COMPUTERS.=
RJMI65      ENT AND FUTURE      GENERATIONS      OF COMPUTERS.=MEMORIES IN PRES
MYDS68      OSTIC SEQUENCE      GENERATOR        FOR ILLIAC-IV PROCESSING ELEMENT.=DIAGN
RPAG69              A           GLASS            DELAY LINE CONTENT-ADDRESSED MEMORY SYSTEM=
RPAG69              A           GLASS            DELAY LINE CONTENT-ADDRESSED MEMORY SYSTEM.=
RPDA68      VALUATION OF A      GLASS            DELAY LINE CONTENT-ADDRESSABLE MEMORY SYSTEM.=DESIGN AND E
RPEO67       SYSTEMS USING      GLASS            DELAY LINES.=EVALUATION OF THREE CONTENT-ADDRESSABLE MEMORY
BRNA66       USING A 20 MC      GLASS            DELAY LINE MEMORY.=NEBULA: A DIGITAL COMPUTER
LDGL69                          GLYPNIR          : A LIST PROCESSING LANGUAGE FOR ILLIAC-IV.=
SHGP68                          GRAPH            PROPERTY RECOGNITION MACHINES.=
SRSA65      N DIRECTED          GRAPH            STRUCTURES.=STORAGE AND RETRIEVAL OF ASPECTS OF MEANING I
RBAG67              A           GRAPH            MODEL FOR PARALLEL COMPUTATIONS.=
MEMO67      LIC TO ACYCLIC      GRAPH             TRANSFORMATIONS.=MODELS OF COMPUTATIONAL SYSTEMS - CYC
RHOT69      OF AMBIT/G : A      GRAPHICAL        PROGRAMMING LANGUAGE.=ON THE IMPLEMENTATION
SISA63       A MAN-MACHINE      GRAPHICAL        COMMUNICATION SYSTEM.=SKETCHPAD,
RIGC64                          GRAPHICAL        COMMUNICATION AND CONTROL.LANGUAGES.=
STGS68                          GRAPHICAL        SYSTEMS COMMUNICATIONS : AN ASSOCIATIVE MEMORY APPROACH.=
SCTP65      UPERCONDUCTIVE      GROUND           PLANE.=THE PERSISTATRON UTILIZING A S
BRTU68      ROGRAMMING THE      GROWING          MACHINE.=THE USE OF MULTIPLE ASSOCIATIVE MEMORIES IN P
GAHO67                          HANDBOOK         OF OPERATING AND MAINTENANCE - INSTRUCTIONS FOR ASSOCIATIVE MEMORY.=
DGAA66      SOCIATIVE DATA      HANDLING         IN PL/I.=APL - A LANGUAGE FOR AS
RSHD69                          HARDWARE         DESIGN REFLECTING SOFTWARE REQUIREMENTS=
RDFH65              FUTURE      HARDWARE         FOR ELECTRONIC INFORMATION-HANDLING SYSTEMS.=
GRAH64              A           HARDWARE         INTEGRATED GENERAL PURPOSE COMPUTER SEARCH MEMORY.=
JEMH69              MEMORY      HIERARCHY        - COMPUTER SYSTEM CONSIDERATIONS.=
BLAR70              SIMILAR     HIGH             LEVEL LANGUAGE=A RING PROCESSING PACKAGE FOR USE WITH FORTRAN OR A
BSSO69      S FOR               HIGH             SPEED ASSOCIATIVE MEMORY=SILICON-ON-SAPPHIRE COMPLEMENTARY MOS CIRCUIT
AFBI65          BILOC - A       HIGH             SPEED NDRO ONE CORE PER BIT ASSOCIATIVE ELEMENT.=
BCCI62       COMPUTER WITH      HIGH              LOGIC-TO-MEMORY SPEED RATIO.=CONSIDERATIONS IN THE DESIGN OF A
SPAF69      FAST, FLEXIBLE      HIGHLY           PARALLEL ASSOCIATIVE PROCESSOR=A
KWTD69      HE DESIGN OF A      HIGHLY            PARALLEL COMPUTER ORGANIZATION.=T
SLMF62      S FABRICATION,      HIGHLY           PARALLEL SYSTEMS, AND ASSOCIATIVE LOGIC.=MAS
MJHP66                          HIGHLY           PARALLEL INFORMATION PROCESSING SYSTEMS. =
MAOP60       PROGRAMMING A      HIGHLY           PARALLEL MACHINE TO BE AN INTELLIGENT TECHNICIAN.=ON
SPPA62      AL DESIGN OF A      HIGHLY           PARALLEL COMPUTER.=PHYSICAL AND LOGIC
RRAA64      ANDOM WALKS ON      HIGHLY           PARALLEL MACHINES.=A ALGORITHM FOR CONCURRENT R
CWHP62                          HIGHLY           PARALLEL MACHINES.=
SPPA63      DERATIONS OF A      HIGHLY           PARALLEL COMPUTER.=PROGRAMMING AND DESIGN CONSI
SLAL63      TIVE LOGIC FOR      HIGHLY           PARALLEL SYSTEMS.=ASSOCIA
GJAA69      N ASSOCIATIVE,      HIGHLY-PARALLEL  COMPUTER FOR RADAR DATA PROCESSING.=A
NBHS                            HIGH-SPEED       SUPERCONDUCTIVE SWITCHING ELEMENT SUITABLE FOR TWO-DIMENSIONAL FABRICATION.=
BPAH67              A           HIGH-SPEED       ASSOCIATIVE MEMORY.=
AFAO62      YOTRONS TO THE      HIGH-SPEED       COMPUTER.=APPLICATIONS OF CR
FITS68      STRUCTURE OF A      HIGH-SPEED       ASSOCIATIVE PROCESSOR.=THE
MRHS66                          HIGH-SPEED       BIAX MEMORIES.=
WDHS64                          HIGH-SPEED        CONTENT SEARCH IN A LARGE, ROTATING, MASS MEMORY.=
YDRD61      EVELOPMENTS IN      HIGH-SPEED       SUPERCONDUCTING DEVICES.=RECENT D
WWBH59              BIAX        HIGH-SPEED       MAGNETIC COMPUTER ELEMENT.=
TIHS61                          HIGH-SPEED       MEMORY USES TUNNEL DIODES.=
KMAH65              A           HIGH-SPEED        WOVEN READ ONLY MEMORY.=
CCTL61      AL DESIGN OF A      HOLLAND          MACHINE.=THE LOGIC
CWAM63          A MODIFIED      HOLLAND          MACHINE.=
GOAH69        ASSOCIATIVE       HOLOGRAPHIC      MEMORIES=
SWAS68      A SEQUENTIALLY      HOMING           CONTENT-ADDRESSED MEMORY MODEL.=A SEQU
HAHA63                          HUGHES           ASSOCIATIVE MEMORY.=
IBHA64-                         HYBRID           ASSOCIATIVE COMPUTER STUDY.=
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KASC67      RICAL MAGNETIC     FILM                STORAGE SYSTEMS.=SMALL CAPACITY THIN CYLIND
CMCO60      ACTERISTICS OF     FILM                CRYOTRONS.=CHAR..
JSTD62      ECOND MAGNETIC     FILM                 STORE.=THE DESIGN OF A 4096 WORD ONE MICROS
RCMF61           MAGNETIC      FILM                MEMORY DESIGN.=
ENAO65      NIC CONTINUOUS     FILM                MEMORY.=ANALYSIS OF THE CRYOGE
GMEA65      ING CONTINUOUS     FILM                STORE.=EXPERIMENTAL AND THEORETICAL ASPECTS OF THE SUPERCONDUCT
NBAI60         AN IMPROVED     FILM                CRYOTRON AND ITS APPLICATION TO DIGITAL COMPUTERS.=
RCAP64      USING MAGNETIC     FILMS               =A PROPOSAL FOR AN ASSOCIATIVE MEMORY
NMCA65       MAGNETIC THIN     FILMS               =CONTENT-ADDRESSED MEMORY USING MAGNETORESISTIVE READOUT OF
GPNR67       THIN MAGNETIC     FILMS               =NONDESTRUCTIVE READOUT ( NDRO ) FROM
VVPO58      UPERCONDUCTING     FILMS               =PENETRATION OF MAGNETIC FIELDS THROUGH THIN S
CRAP64      USING MAGNETIC     FILMS               =A PROPOSAL FOR AN ASSOCIATIVE MEMORY
TRCA64      CIATIVE MEMORY     FINAL               REPORT.=COMPUTER ASSO
CBPF68               PATH      FINDING             WITH ASSOCIATIVE MEMORY.=
PFCT63      CRYOGENIC TUBE     FITTING             =CRYOGE
LBFR65                         FIXED               RESISTOR-CARD MEMORY.=
EGO060       SYSTEMS - THE     FIXED               PLUS VARIABLE STRUCTURE COMPUTER.=ORGANIZATION OF COMPUTER
LBFA63                         FIXED               ASSOCIATIVE MEMORY USING EVAPORATED ORGANIC DIODE ARRAYS.=
BEDO61          DESIGN OF A    FIXED-PLUS-VARIABLE STRUCTURE COMPUTER FOR THE SOLUTION OF A DIFFUSION EQUATION.=
AETF61               THE       FIXED-PLUS-VARIABLE COMPUTER SYSTEM IN DYNAMIC PROGRAMMING FORMULATION OF CONTROL SYSTEM OPTIMIZ
EVO062      NIZATION OF A '    FIXED-PLUS-VARIABLE ' STRUCTURE COMPUTER FOR COMPUTATION OF EIGENVALUES AND EIGENVECTORS OF REAL
EFMA64      ADDRESSING FOR     FIXED-TAG           ASSOCIATIVE MEMORIES.=MULTIPLE
SPAF69            A FAST,      FLEXIBLE            HIGHLY-PARALLEL ASSOCIATIVE PROCESSOR=
LEAT63       COMPLEMENTING     FLIP-FLOP           =ASSOCIATIVE TECHNIQUES WITH
HCMR61       EMPLOYING ONE     FLUX                PATH PER FILE ITEM.=MAGNETIC REALIZATIONS FOR MIRF
CHSA63      : A REALIZABLE     FORM                OF ASSOCIATIVE MEMORY.=SHIEF
AETF61          PROGRAMMING    FORMULATION         OF CONTROL SYSTEM OPTIMIZATION PROBLEMS.=THE FIXED-PLUS-VARIABLE COMPUTER SYST
BLAR70      E FOR USE WITH     FORTRAN             OR A SIMILAR HIGH LEVEL LANGUAGE=A RING PROCESSING PACKAG
GHAF60                  A      FORTRAN-COMPILED    LIST PROCESSING LANGUAGE.=
WMAP69      G FOR THE FAST     FOURIER             TRANSFORM.=ASSOCIATIVE PARALLEL PROCESSIN
PWDO65          DESIGN OF A    FULLY               ASSOCIATIVE CRYOGENIC DATA PROCESSOR.=
PWDO64          DESIGN OF A    FULLY               ASSOCIATIVE CRYOGENIC DATA PROCESSOR.=
CFLA62      ND EXPONENTIAL     FUNCTION            EVALUATION IN A VARIABLE STRUCTURE DIGITAL COMPUTER.=LOGARITHMIC A
FMLA62          LOGICAL AND    FUNCTIONAL          SPECIFICATION OF AN ASSOCIATIVE MEMORY.=
GEAT66      ES FOR CONTROL     FUNCTIONS           IN A MULTIPROCESSOR.=ASSOCIATIVE TECHNIQU
GGAT67      ES FOR CONTROL     FUNCTIONS           IN A MULTI-PROCESSOR SIMULATION INVESTIGATION.=ASSOCIATIVE TECHNIQU
OJSF63           SWITCHING     FUNCTIONS           FOR SIMPLIFIED DATA RETRIEVAL AND DISPLAY DEVICES.=
MSFI61                         FUNDAMENTAL         INVESTIGATION OF DIGITAL COMPUTER STORAGE AND ACCESS TECHNIQUES.=
HLPA66          PRESENT AND    FUTURE              STATE-OF-THE-ART IN COMPUTER MEMORIES.=
GVRO64      EQUIREMENTS OF     FUTURE              COMPUTER MEMORIES FOR DOCUMENT PROCESSING.=R
VRPF67      REDICTIONS FOR     FUTURE              OF CRYOGENIC APPLICATIONS.=P
RDFH65                         FUTURE              HARDWARE FOR ELECTRONIC INFORMATION-HANDLING SYSTEMS.=
RJCM62      IES - POSSIBLE     FUTURE              DEVELOPMENTS.=COMPUTER MEMOR
RJMI65      IN PRESENT AND     FUTURE              GENERATIONS OF COMPUTERS.=MEMORIES
EKLS63      SYSTEMS OF THE     FUTURE              =LARGE SCALE COMPUTING
EPAP67      TING MACHINE '     GAMMA-BARABAN       '.=A PARALLEL MACHINE SIMULATOR BASED ON THE SEQUENTIALLY OPERA
SHAP69      PROCESSING FOR     GENERAL             PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES.=ASSOCIATIVE
MBDO        TER - PART 1 :     GENERAL             INTRODUCTION.=DESIGN OF A PATTERN RECOGNITION DIGITAL COMPU
HIGS64                         GENERAL             SURVEY : ASSOCIATIVE STORAGE FOR NUCLEAR PHYSICS.=
SHAP68      PROCESSING FOR     GENERAL             PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES.=ASSOCIATIVE
PSUO66      MULTIWRITE FOR     GENERAL             PROGRAMMABILITY OF SEARCH MEMORIES.=USE OF
GRAH64      ARE INTEGRATED     GENERAL             PURPOSE COMPUTER SEARCH MEMORY.=A HARDW
KAAS63      UBSYSTEM FOR A     GENERAL             PURPOSE COMPUTER.=A SEARCH MEMORY S
DJPG68          PROGRAMMING    GENERALITY           PARALLELISM AND COMPUTER ARCHITECTURE.=
FSGO62                         GENERALIZATION      OF AN ELEMENTARY PERCEIVING AND MEMORIZING MACHINE.=
SJAI68      ELY STRUCTURED     GENERAL-PURPOSE     DIGITAL COMPUTER=AN ITERATIV
SJAO68      CTURED             GENERAL-PURPOSE     DIGITAL COMPUTER=ASYNCHRONOUS OPERATION OF AN ITERATIVELY STRU
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GRHA66                          HYPRID          ASSOCIATIVE COMPUTER STUDY.=
DGAS66  E UTILITY OF A          HYBRID          ASSOCIATIVE MEMORY PROCESSOR.=A STUDY OF TH
GRHA66                          HYBRID          ASSOCIATIVE COMPUTER STUDY.=
FOAH66                  A       HYBRID          CRYOTRON TECHNOLOGY: I - CIRCUITS AND DEVICES.=
AOAH66                  1       HYBRID          CRYOTRON TECHNOLOGY: 2 - FABRICATION.=
BMAH62                  A       HYPOTHETICAL    MACHINE FOR SYNTAX TESTS.=
SRII67                          ILLIAC          IV-ROUTE TO PARALLEL COMPUTERS=
BHIL65                          ILLIAC-II       - A SHORT DESCRIPTION AND ANNOTATED BIBLIOGRAPHY.=
SJUM64  LATION UNIT OF          ILLIAC-III      =USER'S MANUAL FOR PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICU
SJPD64  LATION UNIT OF          ILLIAC-III      =PROGRAM DESCRIPTION OF PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICU
MBTI63  ION COMPUTER -          ILLIAC-III      =THE ILLINOIS PATTERN RECOGNIT
MRIL65                          ILLIAC-III       A PROCESSOR OF VISUAL INFORMATION.=
LDGL69  G LANGUAGE FOR          ILLIAC-IV       =GLYPNIR : A LIST PROCESSIN
8BTI68                  THE     ILLIAC-IV       COMPUTER.=
DRTI69                  THE     ILLIAC-IV       PROCESSING ELEMENT.=
KAAO69  APPLICATION OF          ILLIAC-IV       TO URBAN DEFENSE RADAR PROBLEM.=APPLIC
AKSS69  ESSING VIA THE          ILLIAC-IV       COMPUTER.=SEISMIC SIGNAL PROC
BCIL69                          ILLIAC-IV       SYSTEMS CHARACTERISTICS AND PROGRAMMING MANUAL.=
GDAM69  -ASSEMBLER FOR          ILLIAC-IV       =A MACRO
DRTI69                  THE     ILLIAC-IV       PROCESSING ELEMENT.=
GLRM69  NCE MANUAL FOR          ILLIAC-IV       ASSEMBLER ASK.=REFERE
AGAD69  RIPTION OF THE          ILLIAC-IV       OPERATING SYSTEM.=A DESC
KDIL68                          ILLIAC-IV       SOFTWARE AND APPLICATION PROGRAMMING.=
WGAT68  G SIMULATOR OF          ILLIAC-IV       =A TIMIN
BCIL68                          ILLIAC-IV       : SYSTEMS CHARACTERISTICS AND PROGRAMMING MANUAL.=
MYDS68   GENERATOR FOR          ILLIAC-IV       PROCESSING ELEMENT.=DIAGNOSTIC SEQUENCE
BGTI68                  THE     ILLIAC-IV       COMPUTER.=
MYSM68  X INVERSION ON          ILLIAC-IV       =SPARSE MATRI
IUIL67                          ILLIAC-IV       =
KKOT68   SEQUENCES FOR          ILLIAC-IV        PROCESSING ELEMENT.=DIAGNOSTIC TEST PATTERNS AND
CFLP68  LEMENTATION IN          ILLIAC-IV        I : REVISED SIMPLEX METHOD.=LINEAR PROGRAMMING IMP
KAAO68  APPLICATION OF          ILLIAC-IV       TO URBAN DEFENSE RADAR PROBLEM.=APPLIC
BRTP69  IVERSITY OF             ILLINOIS        PROGRAMMING MANUAL.=THE PAX-2 PICTURE PROCESSING SYSTEM AT THE UN
MBTI63                  THE     ILLINOIS        PATTERN RECOGNITION COMPUTER - ILLIAC-III.=
RHOT69                  ON THE  IMPLEMENTATION  OF AMBIT/G : A GRAPHICAL PROGRAMMING LANGUAGE.=
MCAM64   MEMORY SYSTEM          IMPLEMENTATION  AND CHARACTERISTICS.=ASSOCIATIVE
RPAA68  MMING LANGUAGE          IMPLEMENTATION  =AN AMBIT/G PROGRA
SSSO64  -                       IMPLEMENTATION  AND TECHNIQUES.=SURVEY OF PRESENT AND POTENTIAL SEARCH MEMORY
CFLP68  AR PROGRAMMING          IMPLEMENTATION  IN ILLIAC-IV. I : REVISED SIMPLEX METHOD.=LINE
RWAM63  ENIC                    IMPLEMENTATION  =ASSOCIATIVE MEMORY ALGORITHMS AND THEIR CRYOG
CMAM64   MEMORY SYSTEM          IMPLEMENTATION  AND CHARACTERISTICS.=ASSOCIATIVE
LGAS68    ASP - A RING          IMPLEMENTED     ASSOCIATIVE STRUCTURE PACKAGE.=
HHCS68  STORAGE USE IN          IMPLEMENTING    AN ASSOCIATIVE MEMORY FOR A TIME-SHARED PROCESSOR.=CONTROL
BHAA62  ITS BIOLOGICAL          IMPLICATIONS    =AN ASSOCIATIVE MACHINE FOR DEALING WITH THE VISUAL FIELD AND SOME OF
CSSI63         SYSTEMS          IMPLICATIONS    OF NEW MEMORY DEVELOPMENTS.=
PFAI69                  AN      IMPROVED        FIELD-CONTROLLED POLARIZATION-TRANSFER DEVICE AND THE OPERATING FEATURES OF TH
NBAI60                  AN      IMPROVED        FILM CRYOTRON AND ITS APPLICATION TO DIGITAL COMPUTERS.=
GLAI65                  AN      IMPROVED        CELL MEMORY.=
RMSI66      SCHEDULING          INDEPENDENT     TASKS ON PARALLEL PROCESSORS.=
MJAO69  EMS AND A KWIC          INDEX           TO THE LITERATURE 1956-1970=AN OVERVIEW OF ASSOCIATIVE MEMORY OR CONTENT-ADDRE
YHDO64   DOCUMENT DATA          INDEXING        SET.=DEVELOPMENT OF A MULTIPLE INSTANTANEOUS RESPONSE FILE : THE AN/GSQ-81
CRIO63                          INFLUENCE       OF THERMAL EFFECTS ON THE OPERATING SPEED OF SUPERCONDUCTING COMPUTER ELEMENTS
YYAC66  IVE MEMORY FOR          INFORMATION     RETRIEVAL.=A CRYOGENIC ASSOCIAT
GHOT    F A MULTI-LIST          INFORMATION     PROCESSING SYSTEM=ON THE DESIGN O
LPAC64  PPLICATIONS TO          INFORMATION     RETRIEVAL.=A CONTENT ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH A
MJHP66  IGHLY PARALLEL          INFORMATION     PROCESSING SYSTEMS. =H
MTCA60  IAL ASPECTS OF          INFORMATION     RETRIEVAL.=COMBINATOR
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BeLS68          LARGE SCALE     INFORMATION     PROCESSING SYSTEMS : MODEL BUILDING, SIMULATION AND EVALUATION.=
KAAA68          PROCESSOR FOR   INFORMATION     RETRIEVAL.=AN ASSOCIATION
HAST63          STRUCTURE AND   INFORMATION      RETRIEVAL.=SOME THEORIZING ON MEMORY
GJTF62          S FOR ADVANCED  INFORMATION     PROCESSING SYSTEM.=TECHNIQUE
LPAS63,         ATIFICATION OF  INFORMATION     =AUTOMATIC STR
IBAP62          DY OF ADVANCED  INFORMATION     RETRIEVAL TECHNIQUES.=A PROPOSAL FOR THE STU
LwAM            GANIZATION FOR  INFORMATION     RETRIEVAL SYSTEMS.=A MULTIPLE FILE OR
MRIL65          SSOR OF VISUAL  INFORMATION     =ILLIAC-III: A PROCE
GGLF62          ARGE FILES FOR  INFORMATION     RETRIEVAL BASED ON SIMULTANEOUS INTEROGATION OF ALL ITEMS.=L
GHLF61          ARGE FILES FOR  INFORMATION     RETRIEVAL BASED ON SIMULTANEOUS INTERROGATION OF ALL ITEMS.=L
FERO61            RETRIEVAL OF  INFORMATION     WITH AN ASSOCIATIVE MEMORY.=
MJTS64          H MEMORY IN AN  INFORMATION     RETRIEVAL SYSTEM.=THE SEARC
DGTS64          URE OF ON-LINE  INFORMATION     PROCESSING SYSTEMS,=THE STRUCT
ACTC65          IVE MEMORY FOR  INFORMATION      RETRIEVAL.=TOWARDS CONTROLLED EXPERIMENTS IN THE CONSTRUCTION OF AN ADAPTIVE
SFAC64          PPLICATIONS TO  INFORMATION     RETRIEVAL.=A CONTENT-ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH A
KMSP64          ME PROBLEMS IN  INFORMATION     SCIENCE WITH EMPHASIS ON ADAPTATION TO USE THROUGH MAN-MACHINE INTERACTION.=SO
GPAI66          NTRODUCTION OF  INFORMATION     INTO A REMOTE-ACCESS SYSTEM : A PHYSICS LIBRARY CATALOG.=AUTOMATIC I
RDAM65          E MEMORIES AND  INFORMATION     RETRIEVAL. =ASSOCIATIV
WPST66          IFIC TECHNICAL  INFORMATION     NO. 6, 1964 : SELECTED ARTICLES.=SCIENT
YYAC66          ORY SYSTEM FOR  INFORMATION      RETRIEVAL.=A CRYOGENIC ASSOCIATIVE MEM
PHCA62          ADDRESSING AND  INFORMATION     RETRIEVAL.=CONTENT
GHMM68          ICAL MODELS OF  INFORMATION     SYSTEMS.=MATHEMAT
RFST64          L.  VOLUME I.   INFORMATION     STORAGE, RETRIEVAL AND COMMUNICATION SYSTEM CONTROL.=STUDY TO DETERMINE THE AP
NTAI60          NTRODUCTION TO  INFORMATION     PROCESSING LANGUAGE - V.=AN I
LPAC63          APPLICATION TO  INFORMATION     RETRIEVAL.=A CONTENT ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH
NAIP61                          INFORMATION     PROCESSING LANGUAGE - V MANUAL.=
AMIP62                          INFORMATION     PROCESSING BY DATA INTERROGATION.=
GVTP61           UTILIZATION OF INFORMATIONAL-LOGICAL MACHINES IN CHEMISTRY.=THE PROSPECTS FOR THE
RDFH65           FOR ELECTRONIC INFORMATION-HANDLING SYSTEMS.=FUTURE HARDWARE.
YHDO64           OF A MULTIPLE  INSTANTANEOUS    RESPONSE FILE : THE AN/GSQ-81 DOCUMENT DATA INDEXING SET.=DEVELOPMENT
GMAC60          GENIC MULTIPLE  INSTANTANEOUS    RESPONSE FILE.=A CRYO
GGMI61               MULTIPLE   INSTANTANEOUS    RESPONSE FILE.=
FRAA64          F THE MULTIPLE  INSTANTANEOUS    RESPONSE FILE.=AN ANALYSIS O
YHDO64          ENTAL MULTIPLE  INSTANTANEOUS    RESPONSE FILE.=DESIGN OF AN EXPERIM
NJMI61          IRF ( MULTIPLE  INSTANTANEOUS    RESPONSE FILE ).=M
FPAM69              A MULTIPLE  INSTRUCTION      STREAM PROCESSOR WITH SHARED RESOURCES.=
MZET68          ATIVE LEARNING  INSTRUCTIONAL    SYSTEM=EFFORTS TOWARD AN ASSOCI
GAHO67           MAINTENANCE -  INSTRUCTIONS     FOR ASSOCIATIVE MEMORY.=HANDBOOK OF OPERATING AND
LAAA61          CCESS TIME FOR  INSTRUCTIONS     IN LOOPS.=AN APPLICATION FOR A SMALL, FAST ASSOCIATIVE MEMORY TO REDUCE THE A
KKAI69                     AN   INTEGRATED      ASSOCIATIVE STORAGE SYSTEM =
IYAI67                     AN   INTEGRATED      MOS TRANSISTOR ASSOCIATIVE MEMORY SYSTEM WITH 100 NANOSECOND CYCLE TIME.=
IKAH66          E MEMORY USING  INTEGRATED      MOS TRANSISTORS.=A 150-NANOSECOND ASSOCIATIV
IYAI                       AN   INTEGRATED      MOS TRANSISTOR ASSOCIATIVE MEMORY WITH 100-NANOSECONDS CYCLE TIME.=
AKAI68                     AN   INTEGRATED      ASSOCIATIVE MEMORY MATRIX.=
RJIM65                          INTEGRATED      MAGNETIC AND SUPERCONDUCTIVE MEMORIES : A SURVEY OF TECHNIQUES, RESULTS AND PR
GRAH64              A HARDWARE  INTEGRATED      GENERAL PURPOSE COMPUTER SEARCH MEMORY.=
MSUO64           MEMORIES FOR   INTEGRATING     STORAGE OF MULTIPARAMETER DATA BY AUTOMATIC DATA REDUCTION.=USE OF STANDARD ME
HRIT63                          INTEGRATING     THE SEARCH MEMORY WITH THE USQ-20 COMPUTER.=
WLAS70          NG LARGE SCALE  INTEGRATION     =AN ASSOCIATIVE MEMORY USI
FMOA69           IN ARTIFICIAL  INTELLIGENCE    RESEARCH : AN ASSOCIATIVE MEMORY, PARALLEL LANGUAGE, AMPPL-II.=ON A NEW TOOL
FCAM61          PLICATIONS FOR  INTELLIGENCE    DATA PROCESSING.=ASSOCIATIVE MEMORY AP
FJAM61          PPLICATIONS IN  INTELLIGENCE    DATA PROCESSING.=ASSOCIATIVE MEMORY A
NAOP60          E AN            INTELLIGENT     TECHNICIAN.=ON PROGRAMMING A HIGHLY PARALLEL MACHINE TO B
GRRO67             RESEARCH ON  INTELLIGENT     QUESTION-ANSWERING SYSTEM.=
RSIB69                          INTERACTION     BETWEEN LSI AND PARALLEL PROCESSING.=
KMSP64          GH-MAN-MACHINE  INTERACTION     =SOME PROBLEMS IN INFORMATION SCIENCE WITH EMPHASIS ON ADAPTATION TO USE THROU
GPIO62                          INTERACTIONS    OF COMPUTER LANGUAGES AND MACHINE DESIGN.=
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ACII65	E THEORY OF AN	INTERACTIVE	CIRCUIT STORED PROGRAM PARALLEL PROCESSOR.=INVESTIGATIONS INTO TH
LCIC62		INTERCOMMUNICATING	CELLS, BASIS FOR A DISTURBED LOGIC COMPUTER.=
KLCI68	, CELLULAR	INTERCONNECTION	ARRAYS=
RLCM65	S MEMORY PLANE	INTERCONNECTION	TECHNIQUES.=CRYOGENIC
JKMC63	MAN-COMPUTER	INTERFACE	STUDY.=
JHSO68	SOR TECHNIQUES	INTERIM	REPORT.=STUDY OF ADVANCED ASSOCIATIVE PROCES
SAPO59	EEDINGS OF THE	INTERNATIONAL	SYMPOSIUM ON THE THEORY OF SWITCHING, APRIL, 1957.=PROC
GGLF62	N SIMULTANEOUS	INTEROGATION	OF ALL ITEMS.=LARGE FILES FOR INFORMATION RETRIEVAL BASED O
LRAU68	ESSOR	INTERPRETER	PROGRAM.=ASP USERS MANUAL , ASSOCIATION-STORING PROC
SLAS68	RING PROCESSOR	INTERPRETER	PROGRAM.=ASP USER'S MANUAL ASSOCIATION-STO
ASTA69	TRAMP: AN	INTERPRETIVE	ASSOCIATIVE PROCESSOR WITH DEDUCTIVE CAPABILITIES=
SLAS68	RING PROCESSOR	INTERPRETIVE	PROGRAM - PROGRAM LOGIC MANUAL.=ASSOCIATION STO
RRAS69	RING PROCESSOR	INTERPRETIVE	PROGRAM - PROGRAM LOGIC MANUAL.=ASSOCIATION STO
GHLF61	N SIMULTANEOUS	INTERROGATION	OF ALL ITEMS.=LARGE FILES FOR INFORMATION RETRIEVAL BASED O
SHCA66	ECTRO-OPTICAL	INTERROGATION	=CONTENT-ADDRESSED MEMORY USING MAGNETO- OR EL
SHCO67	LECTRO-OPTICAL	INTERROGATION	'=COMMENT ON ' CONTENT-ADDRESSED MEMORY USING MAGNETO- OR E
AMIP62	ESSING BY DATA	INTERROGATION	=INFORMATION PROC
EJIP70		INTERRUPT	PROCESSING WITH QUEUED CONTENT-ADDRESSABLE MEMORIES=
WAUI69	UNIFIED	INTERVAL	CLASSIFICATION AND UNIFIED 3-CLASSIFICATION FOR ASSOCIATIVE MEMORIES=
GJAI63	AN	INTRINSICALLY	ADDRESSED PROCESSING SYSTEM.=
MBDO	RT 1 : GENERAL	INTRODUCTION	=DESIGN OF A PATTERN RECOGNITION DIGITAL COMPUTER - PA
HGIT64		INTRODUCTION	TO SEARCH MEMORIES.=
GPAI66	AUTOMATIC	INTRODUCTION	OF INFORMATION INTO A REMOTE-ACCESS SYSTEM : A PHYSICS LIBRARY CATALOG.=
NTAI60	AN	INTRODUCTION	TO INFORMATION PROCESSING LANGUAGE - V.=
TRAO63	ASSIGNMENT OF	INVENTORY	OF A VARIABLE STRUCTURE COMPUTER.=
EDMI68	MATRIX	INVERSION	AND ITERATIVE REFINEMENT.=
MYSM68	SPARSE MATRIX	INVERSION	ON ILLIAC-IV.=
MHIO62		INVESTIGATION	OF STORAGE AND ACCESS TECHNIQUES SUITABLE FOR USE IN LARGE-CAPACITY DIGITAL ME
ABAS64	MARY REPORT OF	INVESTIGATION	IN DIGITAL TECHNOLOGY RESEARCH.=ANNUAL SUM
MSFI61	FUNDAMENTAL	INVESTIGATION	OF DIGITAL COMPUTER STORAGE AND ACCESS TECHNIQUES.=
HWIO61		INVESTIGATION	OF WOVEN-SCREEN MEMORY TECHNIQUES.=
CCSO64	SUMMARY OF	INVESTIGATION	ON ASSOCIATIVE MEMORIES.=
WDSA64	STUDY AND	INVESTIGATION	TO DEVELOP COMPILER TECHNIQUES REQUIRED FOR PROGRAMMING THE PARALLEL NETWORK C
RPAI66	AN	INVESTIGATION	INTO PAGING A SOFTWARE-SIMULATED ASSOCIATIVE MEMORY SYSTEM.=
GGAT67	SOR SIMULATION	INVESTIGATION	=ASSOCIATIVE TECHNIQUES FOR CONTROL FUNCTIONS IN A MULTI-PROCES
ACAM68	CIATIVE MEMORY	INVESTIGATIONS	: SUBSTRUCTURE SEARCHING AND DATA ORGANIZATION.=ASSO
ACII65		INVESTIGATIONS	INTO THE THEORY OF AN INTERACTIVE CIRCUIT STORED PROGRAM PARALLEL PROCESSOR.=
HFIA61		ITERATIVE	ARRAYS OF LOGIC CIRCUITS.=
HJIC65		ITERATIVE	CIRCUIT COMPUTERS CHARACTERIZATION AND RESUME.=
EDMI68	INVERSION AND	ITERATIVE	REFINEMENT.=MATRIX
HJOI60	ON	ITERATIVE	CIRCUIT COMPUTER CONSTRUCTED OF MICROELECTRONIC COMPONENTS AND SYSTEM.=
SJAO68	PERATION OF AN	ITERATIVELY	STRUCTURED GENERAL-PURPOSE DIGITAL COMPUTER=ASYNCHRONOUS O
SJAI68	AN	ITERATIVELY	STRUCTURED GENERAL-PURPOSE DIGITAL COMPUTER=
SJAI66	AN	ITERATIVELY	STRUCTURED DIGITAL COMPUTER.=
SRII67	ILLIAC	IV-ROUTE	TO PARALLEL COMPUTERS=
BTAM71	A MULTIPLEXED	I/O	SYSTEM FOR REAL TIME COMPUTERS =
MJAO69	SYSTEMS AND A	KWIC	INDEX TO THE LITERATURE 1956-1970=AN OVERVIEW OF ASSOCIATIVE MEMORY OR CONTENT
ARCO65	NS OF SPEED OF	LADDER	NETWORK FOR SUPER-CONDUCTIVE ASSOCIATIVE MEMORIES.=CALCULATIO
SRLF63		LAMINATED	FERRITE MEMORY.=
BLAR70	LAR HIGH LEVEL	LANGUAGE	=A RING PROCESSING PACKAGE FOR USE WITH FORTRAN OR A SIMI
BKSA68	PROCESSING	LANGUAGE	=STUDY OF A COMPUTER FOR DIRECT EXECUTION OF LIST
FRAA69	ED ASSOCIATIVE	LANGUAGE	=AN ALGOL BAS
FNOA67	ON A COMPUTER	LANGUAGE	WHICH SIMULATES ASSOCIATIVE MEMORY AND PARALLEL PROCESSING=
RHOT69	L PROGRAMMING	LANGUAGE	=ON THE IMPLEMENTATION OF AMBIT/G : A GRAPHICA
LDGL69	IST PROCESSING	LANGUAGE	FOR ILLIAC-IV.=GLYPNIR : A L
FNUM	PROCESSING	LANGUAGE	AMPPL-II.=USER'S MANUAL FOR THE ASSOCIATIVE MEMORY, PARALLEL
RFTL68	THE LEAP	LANGUAGE	AND DATA STRUCTURE.=

FMOA69	MORY, PARALLEL	LANGUAGE	AMPPL-II.=ON A NEW TOOL IN ARTIFICIAL INTELLIGENCE RESEARCH : AN ASSOCIATIVE
DBAP67	VE PROGRAMMING	LANGUAGE	USER'S MANUAL.=APL - ASSOCIATI
LPAE65	DATA STRUCTURE	LANGUAGE	=AN EXPERIMENTAL SYNTAX-DIRECTED
RPAA68	/G PROGRAMMING	LANGUAGE	IMPLEMENTATION.=AN AMBIT
FRAA68	ED ASSOCIATIVE	LANGUAGE	=AN ALGOL-BAS
FGSN64	G MANIPULATION	LANGUAGE	=SNOROL : A STRIN
NRAP64	A PROGRAMMING	LANGUAGE	FOR THE PARALLEL PROCESSING OF PICTURES.=
DGAA66	APL - A	LANGUAGE	FOR ASSOCIATIVE DATA HANDLING IN PL/I.=
RFTL68	THE LEAP	LANGUAGE	AND DATA STRUCTURE.=
RGLD64		LANGUAGE	DATA PROCESSING WITH SEARCH MEMORIES.=
SLAS67	NEW CONCEPT IN	LANGUAGE	AND MACHINE ORGANIZATION.=ASP : A
APTL66	2 PROGRAMMING	LANGUAGE	AND SYSTEM.=THE LISP
NAIP61	ION PROCESSING	LANGUAGE	- V MANUAL.=INFORMAT
NTAI60	ION PROCESSING	LANGUAGE	- V.=AN INTRODUCTION TO INFORMAT
GHAF60	IST PROCESSING	LANGUAGE	=A FORTRAN-COMPILED L
GPIO62	NS OF COMPUTER	LANGUAGES	AND MACHINE DESIGN.=INTERACTIO
CGAT61	ESSING NATURAL	LANGUAGES	=A TABLE LOOK-UP MACHINE FOR PROC
BRCL64	IST PROCESSING	LANGUAGES	=COMPUTER L
RRAB67	EY OF COMPUTER	LANGUAGES	FOR SYMBOLIC AND ALGEBRAIC MANIPULATION.=A BRIEF SURV
RLGC64	ON AND CONTROL	LANGUAGES	=GRAPHICAL COMMUNICATI
GBCL61	COMPUTER	LANGUAGES	FOR SYMBOL MANIPULATION.=
BRAC64	IST PROCESSING	LANGUAGES	=A COMPARISON OF I
FRAL67	ACHIEVING	LARGE	SCALE COMPUTING CAPABILITIES THROUGH ASSOCIATIVE PARALLEL PROCESSING=
LGTA69	HITECTURE OF A	LARGE	DISTRIBUTED LOGIC, ASSOCIATIVE MEMORY=THE ARC
WLAS70	E MEMORY USING	LARGE	SCALE INTEGRATION =AN ASSOCIATIV
LGTA70	HITECTURE OF A	LARGE	ASSOCIATIVE PROCESSOR=THE ARC
AKAM68	VE MEMORIES IN	LARGE	COMPUTER SYSTEMS.=ASSOCIATI
LGTA69	HITECTURE OF A	LARGE	DISTRIBUTED LOGIC ASSOCIATIVE PROCESSOR=THE ARC
HFTA68	S FOR PAGING A	LARGE	ASSOCIATIVE DATA STRUCTURE.=THE ANALYSIS OF STRATEGIE
YDDO61	DESIGN OF A	LARGE	SCALE CRYOGENIC MEMORY.=
BSLS68		LARGE	SCALE INFORMATION PROCESSING SYSTEMS : MODEL BUILDING, SIMULATION AND EVALUATI
RDTD66	THE DESIGN OF	LARGE	CRYOTRON MEMORIES.=
GHLF61		LARGE	FILES FOR INFORMATION RETRIEVAL BASED ON SIMULTANEOUS INTERROGATION OF ALL ITE
GGLF62		LARGE	FILES FOR INFORMATION RETRIEVAL BASED ON SIMULTANEOUS INTEROGATION OF ALL ITEM
FRAL	ACHIEVING	LARGE	COMPUTING CAPABILITIES THROUGH ASSOCIATIVE PARALLEL PROCESSING.=
LROO62	RGANIZATION OF	LARGE	MEMORY SYSTEMS. =O
SDAL	ACHIEVING	LARGE	COMPUTING CAPABILITIES THROUGH AN ARRAY COMPUTER.=
AKAM68	TIVE MEMORY IN	LARGE	COMPUTER SYSTEM.=ASSOCIA
WDHS64	NT SEARCH IN A	LARGE	ROTATING, MASS MEMORY.=HIGH-SPEED, CONTE
SWAM63	TECHNIQUES FOR	LARGE	DATA PROCESSORS.=ASSOCIATIVE MEMORY
SJLP66		LARGE	PARALLEL COMPUTERS.=
BCAL63	A	LARGE	CAPACITY CRYOELECTRIC MEMORY WITH CAVITY SENSING.=
EKLS63		LARGE	SCALE COMPUTING SYSTEMS OF THE FUTURE.=
GELT61	LOCATING THE	LARGEST	WORD IN A FILE USING A MODIFIED MEMORY.=
MHIO62	BLE FOR USE IN	LARGE-CAPACITY	DIGITAL MEMORIES, =INVESTIGATION OF STORAGE AND ACCESS TECHNIQUES SUITA
YMLC62		LARGE-CAPACITY	MEMORY TECHNIQUES FOR COMPUTING.=
BLDO62	DESIGN OF A	LARGE-SCALE	CRYOGENIC MEMORY SYSTEM.=
RFTL68	THE	LEAP	LANGUAGE AND DATA STRUCTURE.=
RFTL68	THE	LEAP	LANGUAGE AND DATA STRUCTURE.=
N7ET68	AN ASSOCIATIVE	LEARNING	INSTRUCTIONAL SYSTEM=EFFORTS TOWARD
ASAM67	ODIFICATION OF	LEE'S	PATH CONNECTION ALGORITHM.=A M
BLAR70	SIMILAR HIGH	LEVEL	LANGUAGE=A RING PROCESSING PACKAGE FOR USE WITH FORTRAN OR A
RMAM62	ES AND THE ONE	LEVEL	STORE.=ASSOCIATIVE MEMORI
WAAS68	IMPLE PROOF OF	LEWIN'S	ORDERED-RETRIEVAL THEOREM FOR ASSOCIATIVE MEMORIES.=A S
GPAI66	EM : A PHYSICS	LIBRARY-	CATALOG.=AUTOMATIC INTRODUCTION OF INFORMATION INTO A REMOTE-ACCESS SYST
IBLP60		LIGHTNING	PROJECT.=
RJMM63	PABILITIES AND	LIMITATIONS	=MAGNETIC MEMORIES - CA

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MRAC62          ENIC ' BETWEEN      LIMITS          ' ASSOCIATIVE MEMORY.=A CRYOG
RPAG69           A GLASS DELAY      LINE            CONTENT-ADDRESSED MEMORY SYSTEM=
SDAP71           PROCESSING OF      LINE            DRAWINGS=ASSOCIATIVE
RPAG69           A GLASS DELAY      LINE            CONTENT-ADDRESSED MEMORY SYSTEM.=
RPDA68           A GLASS DELAY      LINE             CONTENT-ADDRESSABLE MEMORY SYSTEM.=DESIGN AND EVALUATION OF
ADAD61                A DELAY       LINE            APPROACH TO ASSOCIATIVE MEMORY.=
BRNA66          MC GLASS DELAY      LINE             MEMORY.=NEBULA: A DIGITAL COMPUTER USING A 20
CFLP68                              LINEAR          PROGRAMMING IMPLEMENTATION IN ILLIAC-IV. I : REVISED SIMPLEX METHOD.=
MSCL64                CELLULAR      LINEAR-INPUT    LOGIC.=
RPEO67          NG GLASS DELAY      LINES           =EVALUATION OF THREE CONTENT-ADDRESSABLE MEMORY SYSTEMS USI
MJLI62                              LISP            1.5 PROCESSING MANUAL.=
BDTB67             THE BBN 940      LISP            SYSTEM.=
APTL66                     THE      LISP            2 PROGRAMMING LANGUAGE AND SYSTEM.=
LDGL69             GLYPNIR : A      LIST            PROCESSING LANGUAGE FOR ILLIAC-IV.=
BGAL66              ASSOCIATED      LIST            SELECTOR =
BKSA68          T EXECUTION OF      LIST             PROCESSING LANGUAGE=STUDY OF A COMPUTER FOR DIREC
GBAL66             ASSOCIATIVE      LIST            SELECTOR.=
FJLP67                              LIST            PROCESSING.=
GHAN61          ANIPULATION OF      LIST            STRUCTURES.=A NOTE ON THE SYSTEM REQUIREMENTS OF A DIGITAL COMPUTER FOR THE M
WJSL63               SYMMETRIC      LIST            PROCESSOR.=
CGLP68                              LIST            PROCESSING RESEARCH TECHNIQUES.=
CJLP67                              LIST            PROCESSING RESEARCH TECHNIQUES.=
BRCL64                 COMPUTER     LIST            PROCESSING LANGUAGES.=
MSAM63           AN ELEMENTARY      LIST            PROCESSING COMPUTER.=A MEMORY ORGANIZATION FOR
BRAC64           COMPARISON OF      LIST            PROCESSING LANGUAGES.=A
GHAF60          RTRAN-COMPILED      LIST            PROCESSING LANGUAGE.=A FO
LMRO62          VAL OF ORDERED      LISTS           FROM A CONTENT ADDRESSED MEMORY.=RETRIE
MJAO69          C INDEX TO THE      LITERATURE      1956-1970=AN OVERVIEW OF ASSOCIATIVE MEMORY OR CONTENT-ADDRESSABLE MEMORY SYST
LAAA63          AN ASSOCIATIVE      LOCAL           STORE.=AN ASS
BRAL68                       A      LOCALLY-DISTRIBUTED ASSOCIATIVE MEMORY NETWORK.=
GELT61                              LOCATING        THE LARGEST WORD IN A FILE USING A MODIFIED MEMORY.=
CFLA62                              LOGARITHMIC     AND EXPONENTIAL FUNCTION EVALUATION IN A VARIABLE STRUCTURE DIGITAL COMPUTER.=
LGTA69          GE DISTRIBUTED      LOGIC            ASSOCIATIVE MEMORY=THE ARCHITECTURE OF A LAR
MRPC69          ALGORITHMS FOR      LOGIC            DESIGN PROBLEMS=PARALLEL COMPUTING STRUCTURES AND
MRTS69              THE SYSTEM      LOGIC           AND USAGE RECORDER=
HHSL69              STRUCTURED      LOGIC           =
SLMF62          D ASSOCIATIVE       LOGIC           =MASS FABRICATION, HIGHLY PARALLEL SYSTEMS, AN
MSCL64          R LINEAR-INPUT      LOGIC           =CELLULA
SJDL69             DISTRIBUTED      LOGIC           MEMORY COMPUTER FOR PROCESS CONTROL=
HFIA61          TIVE ARRAYS OF      LOGIC           CIRCUITS.=ITERA
LGTA69          GE DISTRIBUTED      LOGIC           ASSOCIATIVE PROCESSOR=THE ARCHITECTURE OF A LAR
RRAS69          GRAM - PROGRAM      LOGIC           MANUAL.=ASSOCIATION STORING PROCESSOR INTERPRETIVE PRO
LPAC64          LE DISTRIBUTED      LOGIC           MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=A CONTENT ADDRESSAB
TRFT66          F DISTRIBUTED       LOGIC           NETWORKS.=FABRICATION TECHNIQUES FOR BATCH FABRICATION O
SLAS68          GRAM - PROGRAM      LOGIC           MANUAL.=ASSOCIATION STORING PROCESSOR INTERPRETIVE PRO
LCCA68          ND DISTRIBUTED      LOGIC           MEMORIES. =CONTENT ADDRESSABLE A
MRCC64          POINT CELLULAR      LOGIC           =CUT
EKPO67          LAR ARRAYS FOR      LOGIC           AND STORAGE.=PROPERTIES OF CELLU
MCAT63          TIVE THRESHOLD      LOGIC           =ADAP
SEAC64          LE DISTRIBUTED      LOGIC           MEMORY WITH APPLICATIONS TO INFORMATION RETRIEVAL.=A CONTENT-ADDRESSAB
CSPW67          T STEERING FOR      LOGIC           AND STORAGE.=PLATED WIRE BI
BDMA            RTURE MAGNETIC      LOGIC           DEVICES.=MULTI-APE
BDNM60          RTURE MAGNETIC      LOGIC           ELEMENT.=NEW MULTI-APE
YTSD64          N OF CRYOGENIC      LOGIC           CIRCUITS.=SYSTEMATIC DESIG
LICL66               CRYOTRON       LOGIC           STUDIES.=
ETTO68          RY OF CELLULAR      LOGIC           NETWORKS AND MACHINES.=THEO
OWLA                LOOK AHEAD      LOGIC           SIMPLIFIED.=
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LPAC63	LE DISTRIBUTED	LOGIC	MEMORY WITH APPLICATION TO INFORMATION RETRIEVAL.=A CONTENT ADDRESSAB
LCIC62	OR A DISTURBED	LOGIC	COMPUTER.=INTERCOMMUNICATING CELLS, BASIS F
SLAL63	ASSOCIATIVE	LOGIC	FOR HIGHLY PARALLEL SYSTEMS.=
CLAC67	IC DISTRIBUTED	LOGIC	MEMORY.=A CRYOELECTR
CGBP65	IN DISTRIBUTED	LOGIC	MEMORY.=BULK PROCESSING
BJTL68	THE	LOGICAL	DESIGN OF THE NEBULA COMPUTER.=
CCTL61	THE	LOGICAL	DESIGN OF A HOLLAND MACHINE.=
SPPA62	PHYSICAL AND	LOGICAL	DESIGN OF A HIGHLY PARALLEL COMPUTER.=
MDTL61	TENTATIVE	LOGICAL	REALIZATION OF A PATTERN RECOGNITION COMPUTER.=
FMLA62		LOGICAL	AND FUNCTIONAL SPECIFICATION OF AN ASSOCIATIVE MEMORY.=
IBLM60		LOGICAL	MEMORY STUDY.=
HMCS60	ARITHMETIC AND	LOGICAL	CIRCUITS.=CRYOTRON STORAGE,
KWCL69	CELLULAR	LOGIC-IN-MEMORY	ARRAYS=
BCCI62	TH HIGH	LOGIC-TO-MEMORY	SPEED RATIO.=CONSIDERATIONS IN THE DESIGN OF A COMPUTER WI
KGTL	TABLE	LOOKUP	PROCEDURES IN DATA PROCESSING.=
KNTL62	TABLE	LOOKUP	STUDY MODEL.=
GJTL62	TABLE	LOOKUP	COMPUTERS.=
LFAS69	A STUDY OF	LOOK-ASIDE	MEMORY.=
CGAT61	A TABLE	LOOK-UP	MACHINE FOR PROCESSING NATURAL LANGUAGES.=
SKES60	OF SOME SQUARE	LOOP	MATERIALS IN TOROIDAL STRUCTURES.=ELASTIC SWITCHING PROPERTIES
LAAA61	NSTRUCTIONS IN	LOOPS	=AN APPLICATION FOR A SMALL, FAST ASSOCIATIVE MEMORY TO REDUCE THE ACCESS TIME
FGLT68		LOW	TEMPERATURE BEAM-ADDRESSABLE MEMORY.=
MHRO64	RESEARCH ON	LOW	TEMPERATURE COMPUTING ELEMENTS.=
RSIB69	ACTION BETWEEN	LSI	AND PARALLEL PROCESSING.=INTER
KKAP66	DESCRIPTION OF	L6	=A PROGRAMMERS
AWAC68	CIATIVE OBJECT	MACHINE	=A COMPILER FOR AN ASOO
BHAA62	AN ASSOCIATIVE	MACHINE	FOR DEALING WITH THE VISUAL FIELD AND SOME OF ITS BIOLOGICAL IMPLICATIONS.=AN
BHAM62	A	MACHINE	FOR PERFORMING VISUAL RECOGNITION BY USE OF ANTENNA PROPAGATION CONCEPTS.=
CCTL61	N OF A HOLLAND	MACHINE	=THE LOGICAL DESIG
NAOP60	IGHLY PARALLEL	MACHINE	TO BE AN INTELLIGENT TECHNICIAN.=ON PROGRAMMING A H
BRTU68	NG THE GROWING	MACHINE	=THE USE OF MULTIPLE ASSOCIATIVE MEMORIES IN PROGRAMMI
HJAC67	PPLICATIONS TO	MACHINE	TRANSLATION.=A CONTENT ADDRESSABLE MEMORY WITH A
FRMO67		MACHINE	ORGANIZATION IN ASSOCIATIVE PARALLEL PROCESSING.=
GPIO62	LANGUAGES AND	MACHINE	DESIGN.=INTERACTIONS OF COMPUTER
FSGO62	D MEMORIZING	MACHINE	=GENERALIZATION OF AN ELEMENTARY PERCEIVING AN
CGAT61	TABLE LOOK-UP	MACHINE	FOR PROCESSING NATURAL LANGUAGES.=A
EPAP67	A PARALLEL	MACHINE	SIMULATOR BASED ON THE SEQUENTIALLY OPERATING MACHINE ' GAMMA-BARABAN '.=
SIAS67	N LANGUAGE AND	MACHINE	ORGANIZATION.=ASP : A NEW CONCEPT I
EPAP67	OPERATING	MACHINE	' GAMMA-BARABAN '.=A PARALLEL MACHINE SIMULATOR BASED ON THE SEQUENTIALLY
CWAM63	DIFIED HOLLAND	MACHINE	=A MO
BMAH62	A HYPOTHETICAL	MACHINE	FOR SYNTAX TESTS.=A HYPO
SHGP68	TY RECOGNITION	MACHINES	=GRAPH PROPER
RRAA64	GHLY PARALLEL	MACHINES	=A ALGORITHM FOR CONCURRENT RANDOM WALKS ON HI
GVTP61	IONAL-LOGICAL	MACHINES	IN CHEMISTRY.=THE PROSPECTS FOR THE UTILIZATION OF INFORMAT
CWHP62	IGHLY PARALLEL	MACHINES	=H
BRPI68	ROGRAMS AND IN	MACHINES	=PARALLELISM IN COMPUTER P
ETTO68	C NETWORKS AND	MACHINES	=THEORY OF CELLULAR LOGI
NVSC61	FOR COMPUTING	MACHINES	=SUPERCONDUCTING CIRCUITS
GDAM69	A	MACRO-ASSEMBLER	FOR ILLIAC-IV.=
JFAM68	A	MAGNETIC	ASSOCIATIVE MEMORY=
WCAC68	A COUPLE	MAGNETIC	FILM DEVICE FOR ASSOCIATIVE MEMORIES.=
PZMF68		MAGNETIC	FILM MEMORY SYSTEMS.=
GPNR67	RO) FROM THIN	MAGNETIC	FILMS.=NONDESTRUCTIVE READOUT (ND
RCAP64	E MEMORY USING	MAGNETIC	FILMS.=A PROPOSAL FOR AN ASSOCIATIV
FTAM68	A	MAGNETIC	ASSOCIATIVE MEMORY.=
MRMC63		MAGNETIC	COMPARATORS AND CODE CONVERTERS. =
NMCA65	VE READOUT OF	MAGNETIC	THIN FILMS.=CONTENT-ADDRESSED MEMORY USING MAGNETORESISTI

MAAT65	A THIN	MAGNETIC	FILM COMPUTER MEMORY USING A REASONANT ABSORPTION NON-DESTRUCTIVE READ-OUT TEC
KASC67	IN CYLINDRICAL	MAGNETIC	FILM STORAGE SYSTEMS.=SMALL CAPACITY TH
KPAM61	A	MAGNETIC	ASSOCIATIVE MEMORY.=
KJAH64	8-WORD, 36-BIT	MAGNETIC	ASSOCIATIVE MEMORY.=A 12
HCMR61		MAGNETIC	REALIZATIONS FOR MIRF EMPLOYING ONE FLUX PATH PER FILE ITEM.=
LSAM63	ALL	MAGNETIC	CONTENT ADDRESSED MEMORY.=
MPAM61	A	MAGNETIC	ASSOCIATIVE MEMORY SYSTEM.=
VVPO58	PENETRATION OF	MAGNETIC	FIELDS THROUGH THIN SUPERCONDUCTING FILMS.=PENETR
BDMA	MULTI-APERTURE	MAGNETIC	LOGIC DEVICES.=MULTI-
BJAS61	SEMI-PERMANENT	MAGNETIC	ASSOCIATIVE MEMORY AND CODE CONVERTER.=A
JSTD62	NE MICROSECOND	MAGNETIC	FILM STORE.=THE DESIGN OF A 4096 WORD O
DPPW64	. PLATED WIRE	MAGNETIC	FILM MEMORIES.=
BDNM60	MULTI-APERTURE	MAGNETIC	LOGIC ELEMENT.=NEW
VEMR61		MAGNETIC	REALIZATION FOR MIRF EMPLOYING ONE CONDUCTIVE PATH PER FILE ITEM.=
WW8H59	IAX HIGH-SPEED	MAGNETIC	COMPUTER ELEMENT.=B
RJIM65	INTEGRATED	MAGNETIC	AND SUPERCONDUCTIVE MEMORIES : A SURVEY OF TECHNIQUES, RESULTS AND PROSPECTS.=
RJMM63		MAGNETIC	MEMORIES - CAPABILITIES AND LIMITATIONS.=
CRAP64	E MEMORY USING	MAGNETIC	FILMS.=A PROPOSAL FOR AN ASSOCIATIV
RCMF61		MAGNETIC	FILM MEMORY DESIGN.=
NMCA65	D MEMORY USING	MAGNETORESISTIVE	READOUT OF MAGNETIC THIN FILMS.=CONTENT-ADDRESSE
SHCA66	D MEMORY USING	MAGNETO-	OR ELECTRO-OPTICAL INTERROGATION.=CONTENT-ADDRESSE
SHCO67	D MEMORY USING	MAGNETO-	OR ELECTRO-OPTICAL INTERROGATION.'=COMMENT ON ' CONTENT-ADDRESSE
GAHO67	OPERATING AND	MAINTENANCE	- INSTRUCTIONS FOR ASSOCIATIVE MEMORY.=HANDBOOK OF
BLAT63	ND	MAINTENANCE	=A TREE STRUCTURE SYSTEM FOR SORTING, SEARCH A
DSAT71	LUTION OF DATA	MANAGEMENT	PROBLEMS=ASSOCIATIVE TECHNIQUES IN THE SO
MSFO67	ATION AND DATA	MANAGEMENT	=FILE ORGANIZ
FGSN64	BOL : A STRING	MANIPULATION	LANGUAGE.=SNO
GHAN61	MPUTER FOR THE	MANIPULATION	OF LIST STRUCTURES.=A NOTE ON THE SYSTEM REQUIREMENTS OF A DIGITAL CO
RBAB67	ALGEBRAIC	MANIPULATION	=A BRIEF SURVEY OF COMPUTER LANGUAGES FOR SYMBOLIC AND
SRSM61	SYMBOL	MANIPULATION	WITH AN ASSOCIATIVE MEMORY.=
GBCL61	GES FOR SYMBOL	MANIPULATION	=COMPUTER LANGUA
GLRM69	REFERENCE	MANUAL	FOR ILLIAC-IV ASSEMBLER ASK.=
BRTP69	IS PROGRAMMING	MANUAL	=THE PAX-2 PICTURE PROCESSING SYSTEM AT THE UNIVERSITY OF ILLINO
DBAP67	ANGUAGE USER'S	MANUAL	=APL - ASSOCIATIVE PROGRAMMING L
FNUM	USER'S	MANUAL	FOR THE ASSOCIATIVE MEMORY, PARALLEL PROCESSING LANGUAGE, AMPPL-II.=
BCIL69	ND PROGRAMMING	MANUAL	=ILLIAC-IV SYSTEMS CHARACTERISTICS A
LRAU68	ASP USERS	MANUAL	' ASSOCIATION-STORING PROCESSOR INTERPRETER PROGRAM.=
SLAS68	PROGRAM LOGIC	MANUAL	=ASSOCIATION STORING PROCESSOR INTERPRETIVE PROGRAM -
BCIL68	ND PROGRAMMING	MANUAL	=ILLIAC-IV : SYSTEMS CHARACTERISTICS A
SJUM64	USER'S	MANUAL	FOR PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIA
RBAS69	PROGRAM LOGIC	MANUAL	=ASSOCIATION STORING PROCESSOR INTERPRETIVE PROGRAM -
MJLI62	1.5 PROCESSING	MANUAL	=LISP
BDPP66	RY PROGRAMMING	MANUAL	FOR RADC 2048 WORD ASSOCIATIVE MEMORY.=PRELIMINA
NE*167	*1	MANUAL	=
SIAS68	ASP USER'S	MANUAL	ASSOCIATION-STORING PROCESSOR INTERPRETER PROGRAM.=
NAIP61	G LANGUAGE - V	MANUAL	=INFORMATION PROCESSIN
CGMM66		MANUFACTURING	METHODS FOR CRYOELECTRIC MEMORIES.=
CGMM67		MANUFACTURING	METHODS FOR CRYOELECTRIC MEMORIES.=
PNMC66		MAN-COMPUTER	PROBLEM SOLVING WITH MULTILIST.=
JKMC63		MAN-COMPUTER	INTERFACE STUDY.=
ACTC65	AN ADAPTIVE	MAN-MACHINE	ASSOCIATIVE MEMORY FOR INFORMATION RETRIEVAL.=TOWARDS CONTROLLED EXPERIMENTS I
SISA63	SKETCHPAD, A	MAN-MACHINE	GRAPHICAL COMMUNICATION SYSTEM.=
KMSP64	TO USE THROUGH	MAN-MACHINE	INTERACTION.=SOME PROBLEMS IN INFORMATION SCIENCE WITH EMPHASIS ON ADAPTATION
HMTM60	THE	MARK	I PERCEPTION - DESIGN AND PERFORMANCE.=
PAAC70	PABILITIES FOR	MASS	STORAGE THROUGH ARRAY ORGANIZATION=ASSOCIATIVE CA
HLRA63	AND SURVEY OF	MASS	MEMORIES.=REVIEW
SLMF62		MASS	FABRICATION, HIGHLY PARALLEL SYSTEMS, AND ASSOCIATIVE LOGIC.=

WDHS64	RGE, ROTATING,	MASS	MEMORY.=HIGH-SPFFD, CONTENT SEARCH IN A LA
LAAM65	Y WITH NEAREST	MATCH	=ASSOCIATIVE MEMOR
SKES60	ME SQUARE LOOP	MATERIALS	IN TOROIDAL STRUCTURES.=ELASTIC SWITCHING PROPERTIES OF SO
SGAM63	A	MATHEMATICAL	MODEL FOR AN ASSOCIATIVE MEMORY.=
GHMM68		MATHEMATICAL	MODELS OF INFORMATION SYSTEMS.=
EVO062	REAL SYMMETRIC	MATRICES	=ORGANIZATION OF A ' FIXED-PLUS-VARIABLE ' STRUCTURE COMPUTER FOR COMPUTATION
SOTR68	- IN A MEMORY	MATRIX	=THE RELIABILITY OF OPERATING A SUPERCONDUCTING MEMORY CELL - A PERSISTOTRON
TSSM68	SPARSE	MATRIX	MULTIPLICATION.=
MYSM68	SPARSE	MATRIX	INVERSION ON ILLIAC-IV.=
EDMI68		MATRIX	INVERSION AND ITERATIVE REFINEMENT.=
FKTP64	EN WIRE MEMORY	MATRIX	=THE PLATED-WOV
HWSM66	F THE DETECTOR	MATRIX	=SIMULTANEOUS MULTIPLE RESPONSE IN ASSOCIATIVE MEMORIES AND READOUT O
AKAI68	CIATIVE MEMORY	MATRIX	=AN INTEGRATED ASSO
SRSA65	OF ASPECTS OF	MEANING	IN DIRECTED GRAPH STRUCTURES.=STORAGE AND RETRIEVAL
BMAA69	SIS OF CONTROL	MECHANISMS	FOR PARALLEL PROCESSES.=ANALYSIS AND SYNTHE
KMAM62	ADAPTIVE	MECHANISMS	IN DIGITAL ' CONCEPT ' PROCESSING. =
HMAP63	GANIZATION AND	MECHANIZATIONS	=A PARALLEL COMPUTER OR
SBDR65	RECT-RECORDING	MEGACHANNEL	ANALYZER THROUGH ASSOCIATIVE PROGRAMMING OF A SMALL COMPUTER.=DI
WAUI69	OR ASSOCIATIVE	MEMORIES	=UNIFIED INTERVAL CLASSIFICATION AND UNIFIED 3-CLASSIFICATION F
AKAM68	ASSOCIATIVE	MEMORIES	IN LARGE COMPUTER SYSTEMS.=
FFSA63	NT ADDRESSABLE	MEMORIES	=SOME APPLICATIONS FOR CONTE
SHAP69	SE OF MODIFIED	MEMORIES	=ASSOCIATIVE PROCESSING FOR GENERAL PURPOSE COMPUTERS THROUGH THE U
WCAC68	OR ASSOCIATIVE	MEMORIES	=A COUPLE MAGNETIC FILM DEVICE F
GKAC	ASSOCIATIVE	MEMORIES	=A CONTINOUS FILM MEMORY CELL FOR SUPERCONDUCTIVE
GDAH69	VE HOLOGRAPHIC	MEMORIES	=ASSOCIATI
EJIP70	.ESSABLE	MEMORIES	=INTERRUPT PROCESSING WITH QUEUED CONTENT-ADDR
HLRA63	SURVEY OF MASS	MEMORIES	=REVIEW AND
RWSA67	AL ASSOCIATIVE	MEMORIES	=SERI
CWPW67	NT-ADDRESSABLE	MEMORIES	WITH BIT-STEERING TECHNIQUE.=PLATED WIRE CONTE
RMAM62	ASSOCIATIVE	MEMORIES	AND THE ONE LEVEL STORE.=
RDTD66	LARGE CRYOTRON	MEMORIES	=THE DESIGN OF
BRTU68	LE ASSOCIATIVE	MEMORIES	IN PROGRAMMING THE GROWING MACHINE.=THE USE OF MULTIP
RJRO63	IC ASSOCIATIVE	MEMORIES	=RESEARCH ON CRYOGEN
LCCA68	TRIBUTED LOGIC	MEMORIES	=CONTENT ADDRESSABLE AND DIS
HLPA66	RT IN COMPUTER	MEMORIES	=PRESENT AND FUTURE STATE-OF-THE-A
WRAT	OR ASSOCIATIVE	MEMORIES	AND MULTIPLE-WORD ACCESS MEMORIES.=A TRANSISTOR-TUNNEL DIODE CELL F
NECS67	RANDOM ACCESS	MEMORIES	=CRYOTRON STORAGE CELLS FOR
RWRO64	IC ASSOCIATIVE	MEMORIES	=RESEARCH ON CRYOGEN
WRAT	LE-WORD ACCESS	MEMORIES	=A TRANSISTOR-TUNNEL DIODE CELL FOR ASSOCIATIVE MEMORIES AND MULTIP
FCDO68	IN ASSOCIATIVE	MEMORIES	=DETERMINATION OF PRIORITY
ARSM63	UPERCONDUCTIVE	MEMORIES	=S
RJRO63	IC ASSOCIATIVE	MEMORIES	=RESEARCH ON CRYOGEN
FAAF62	ARALLEL SEARCH	MEMORIES	=ALGORITHMS FOR P
RJRO63	IC ASSOCIATIVE	MEMORIES	=RESEARCH ON CRYOGEN
IHSO63	ARALLEL SEARCH	MEMORIES	=STUDY OF THE APPLICATIONS OF P
MSUO64	AS ASSOCIATIVE	MEMORIES	FOR INTEGRATING STORAGE OF MULTIPARAMETER DATA BY AUTOMATIC DATA REDUCTION.=US
HGIT64	TION TO SEARCH	MEMORIES	=INTRODUC
GAAO63	ARALLEL SEARCH	MEMORIES	=APPLICATIONS OF P
HPEC	OR ASSOCIATIVE	MEMORIES	=EVALUATION CRITERIA F
EFMA64	AG ASSOCIATIVE	MEMORIES	=MULTIPLE ADDRESSING FOR FIXED-T
GVRO64	UTURE COMPUTER	MEMORIES	FOR DOCUMENT PROCESSING.=REQUIREMENTS OF F
MHIO62	PACITY DIGITAL	MEMORIES	=INVESTIGATION OF STORAGE AND ACCESS TECHNIQUES SUITABLE FOR USE IN LARGE-CA
LFSC63	IN ASSOCIATIVE	MEMORIES	=SEMI-CONDUCTOR CIRCUITS
JKAM	ASSOCIATIVE	MEMORIES	=
HWSM66	IN ASSOCIATIVE	MEMORIES	AND READOUT OF THE DETECTOR MATRIX.=SIMULTANEOUS MULTIPLE RESPONSE
MRHS66	IGH-SPEED BIAX	MEMORIES	=H
WAAS68	ASSOCIATIVE	MEMORIES	=A SIMPLE PROOF OF LEWIN'S ORDERED-RETRIEVAL THEOREM FOR

GKAC	CONTINOUS FILM	MEMORY	CELL FOR SUPERCONDUCTIVE ASSOCIATIVE MEMORIES=A
LMTF69	LM ASSOCIATIVE	MEMORY	=THIN FI
GKAW	ONTINUOUS FILM	MEMORY	=A WORD-ORGANIZED SUPERCONDUCTING C
JEMH69		MEMORY	HIERARCHY - COMPUTER SYSTEM CONSIDERATIONS.=
MNAN68	NEW CRYOGENIC	MEMORY	SYSTEM=A
WCAM69	ASSOCIATIVE	MEMORY	DEVICE 3466631.=
WCAM69	ASSOCIATIVE	MEMORY	DEVICE 3466632.=
GKAC67	ONTINUOUS FILM	MEMORY	DRIVEN BY MULTIPLE COINCIDENT PULSES=A C
HHCS68	AN ASSOCIATIVE	MEMORY	FOR A TIME-SHARED PROCESSOR.=CONTROL STORAGE USE IN IMPLEMENTING
CCAM65	ASSOCIATIVE	MEMORY	COMPUTER SYSTEM : DESCRIPTION AND SELECTED NAVAL APPLICATIONS.=
KHSA67	ONTINUOUS FILM	MEMORY	CELLS=SUPERCONDUCTIVE C
RPAG69	TENT-ADDRESSED	MEMORY	SYSTEM.=A GLASS DELAY LINE CON
BCSO69	ED ASSOCIATIVE	MEMORY	=SILICON-ON-SAPPHIRE COMPLEMENTARY MOS CIRCUITS FOR HIGH SPE
RAMA67		MEMORY	ALLOCATION FOR MULTIPROCESSORS=
FNOA67	ATIVE	MEMORY	AND PARALLEL PROCESSING=ON A COMPUTER LANGUAGE WHICH SIMULATES ASSOCI
NTAM69	SS ASSOCIATIVE	MEMORY	=A MULTIACCE
PEAI69	NT ADDRESSABLE	MEMORY	SYSTEM.=AN IMPROVED FIELD-CONTROLLED POLARIZATION-TRANSFER DEVICE AND THE OPER
FGLT68	AM-ADDRESSABLE	MEMORY	=LOW TEMPERATURE BE
FRVT69	RANDOM ACCESS	MEMORY	ORGANIZATIONS.=VARIABLE TOPOLOGY
BRAA69	AN ASSOCIATIVE	MEMORY	PARALLEL DELTIC REALIZATION FOR ACTIVE SONAR SIGNAL PROCESSING.=AN ASS
GHSM66	SPACEBORNE	MEMORY	ORGANIZATION.=
SLRA69	GE ASSOCIATIVE	MEMORY	WITH ORDERED RETRIEVAL.=RAN
FKVT69	RANDOM ACCESS	MEMORY	ORGANIZATIONS=VARIABLE TOPOLOGY
WLAM70	ASSOCIATIVE	MEMORY	MODELS=
LGTA69	ASSOCIATIVE	MEMORY	=THE ARCHITECTURE OF A LARGE DISTRIBUTED LOGIC.
KBAI67	ADVANCES IN	MEMORY	TECHNOLOGY.=
FNUM	HE ASSOCIATIVE	MEMORY	PARALLEL PROCESSING LANGUAGE, AMPPL-II.=USER'S MANUAL FOR T
SJDL69	TRIBUTED LOGIC	MEMORY	COMPUTER FOR PROCESS CONTROL=DIS
CRAM69	ASSOCIATIVE	MEMORY	ACCEPTORS=
LFAS69	OF LOOK-ASIDE	MEMORY	=A STUDY
YYAC66	AR ASSOCIATIVE	MEMORY	=A CUTPOINT CELLUL
YYAC66	IC ASSOCIATIVE	MEMORY	FOR INFORMATION RETRIEVAL.=A CRYOGEN
FWAM64	ASSOCIATIVE	MEMORY	=
IYAI67	OR ASSOCIATIVE	MEMORY	SYSTEM WITH 100 NANOSECOND CYCLE TIME.=AN INTEGRATED MOS TRANSIST
RIAM67	ASSOCIATIVE	MEMORY	FOR COLLECTION AND DISPLAY SYSTEM.=
BRAS62	LY ASSOCIATIVE	MEMORY	=A SEMANTICAL
PGTM62	PE ASSOCIATIVE	MEMORY	=THE MULTI-LIST TY
PGTO62	PE ASSOCIATIVE	MEMORY	=THE ORGANIZATION OF A MULTILIST-TY
YDDO61	CALE CRYOGENIC	MEMORY	=DESIGN OF A LARGE S
SGAN60	STRUCTION OF A	MEMORY	DEVICE.=A NEW PRINCIPLE FOR THE CON
CDAM66	- ASSOCIATIVE	MEMORY	ASSEMBLER.=AMDRIVE* AND CODAP
LPAC64	TRIBUTED LOGIC	MEMORY	WITH APPLICATIONS TO INFORMATION RETRIEVAL.=A CONTENT ADDRESSABLE DIS
RIMO67	M ASSOCIATIVE	MEMORY	=METHODS OF SELECTING A MULTIVALENT ANSWER FRO
FRCA63	NT ADDRESSABLE	MEMORY	SYSTEMS.=CONTE
SHAP61	ED ASSOCIATIVE	MEMORY	FOR USE IN COMPILING.=A PROGRAMM
CHDI63	AN ASSOCIATIVE	MEMORY	=DIMENSIONING IN
SNTW66	E CRYOELECTRIC	MEMORY	SYSTEMS.=THREE-WIR
FCAM61	ASSOCIATIVE	MEMORY	APPLICATIONS FOR INTELLIGENCE DATA PROCESSING.=
CBPF68	TH ASSOCIATIVE	MEMORY	=PATH FINDING WI
BVMO66	R ASSOCIATIVE	MEMORY	UNIT.=MODELING OF A MEMORY SYSTEM INCLUDING A BUFFE
SSTF60	YOTRON CATALOG	MEMORY	=THIN FILM CR
FTAM68	IC ASSOCIATIVE	MEMORY	=A MAGNET
RCAP64	AN ASSOCIATIVE	MEMORY	USING MAGNETIC FILMS.=A PROPOSAL FOR
SOTR68	UPERCONDUCTING	MEMORY	CELL - A PERSISTOTRON - IN A MEMORY MATRIX. =THE RELIABILITY OF OPERATING A S
NMCA65	TENT-ADDRESSED	MEMORY	USING MAGNETORESISTIVE READOUT OF MAGNETIC THIN FILMS.=CON
AMGE62	IC ASSOCIATIVE	MEMORY	CIRCUIT DEVELOPED.=G. E. CRYOGEN
SOTR68	STOTRON - IN A	MEMORY	MATRIX. =THE RELIABILITY OF OPERATING A SUPERCONDUCTING MEMORY CELL - A PERSI

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SAAD64   OF ASSOCIATIVE   MEMORIES   FROM A DEVICE POINT OF VIEW.=A DISCUSSION
CVTU67   IN ASSOCIATIVE   MEMORIES   =THE USE OF CODES ' M-OUT-OF-N '
WAED64   N SEARCH         MEMORIES   =EXTREME DETERMINATION AND ORDERED RETRIEVAL I
BRCA67   NT ADDRESSABLE   MEMORIES   =CONTE
WMWN63   EW IN COMPUTER   MEMORIES   =WHAT'S N
BCAM67     ASSOCIATIVE    MEMORIES   IN NUCLEAR PHYSICS.=
YFCA62   NG ASSOCIATIVE   MEMORIES   =CIRCULATI
CCAO     OF ASSOCIATIVE   MEMORIES   TO THE WEAPON ASSIGNMENT PROBLEM OF NTDS.=APPLICATION
DPPW64    MAGNETIC FILM   MEMORIES   =PLATED WIRE
SLPC65   NT ADDRESSABLE   MEMORIES   =PANEL : CONTE
CCSO64   ON ASSOCIATIVE   MEMORIES   =SUMMARY OF INVESTIGATION
CGMM66   R CRYOELECTRIC   MEMORIES   =MANUFACTURING METHODS FO
GMAO66   LL ASSOCIATIVE   MEMORIES   FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=ANALYSIS OF SMA
SHAP68   SE OF MODIFIED   MEMORIES   =ASSOCIATIVE PROCESSING FOR GENERAL PURPOSE COMPUTERS THROUGH THE U
BGED67   ED ASSOCIATIVE   MEMORIES   =ELEMENT DEVELOPMENT FOR ADVANC
PSED68   ED ASSOCIATIVE   MEMORIES   =ELEMENT DEVELOPMENT FOR ADVANC
CGMM67   R CRYOELECTRIC   MEMORIES   =MANUFACTURING METHODS FO
BACM63     CRYOELECTRIC   MEMORIES   =
RDAM65     ASSOCIATIVE    MEMORIES   AND INFORMATION RETRIEVAL. =
RJIM65   UPERCONDUCTIVE   MEMORIES   : A SURVEY OF TECHNIQUES, RESULTS AND PROSPECTS.=INTEGRATED MAGNETIC AND S
NAAN62    ASSOCIATIVE     MEMORIES   =A NOTE ON THE USE OF SCRAMBLED ADDRESSING FOR
GMAO66   LL ASSOCIATIVE   MEMORIES   FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=ANALYSIS OF SMA
HHED67   ED ASSOCIATIVE   MEMORIES   =ELEMENT DEVELOPMENT FOR ADVANC
RJAS62   EY OF COMPUTER   MEMORIES   =A SURV
HHED66   ED ASSOCIATIVE   MEMORIES   =ELEMENT DEVELOPMENT FOR ADVANC
RGLD64   NG WITH SEARCH   MEMORIES   =LANGUAGE DATA PROCESSI
RJNT64   DS IN COMPUTER   MEMORIES   =NEW TREN
PSUO66    OF SEARCH       MEMORIES   =USE OF MULTIWRITE FOR GENERAL PROGRAMMABILITY
RJCM62       COMPUTER     MEMORIES   - POSSIBLE FUTURE DEVELOPMENTS.=
LMAS65   Y OF READ ONLY   MEMORIES   =A SURVE
FAAF62   ARALLEL SEARCH   MEMORIES   =ALGORITHMS FOR P
EFSA63   NT-ADDRESSABLE   MEMORIES   =SOME APPLICATIONS FOR CONTE
ERCA64   TRIBUTED-LOGIC   MEMORIES   =CONTENT-ADDRESSABLE DIS
CAAM63     ASSOCIATIVE    MEMORIES   =
NDCS65    RANDOM ACCESS   MEMORIES   =CONTINUOUS SHEET SENSING FOR
RJCM61       COMPUTER     MEMORIES   - A SURVEY OF THE STATE-OF-THE-ART.=
RJMI65                    MEMORIES   IN PRESENT AND FUTURE GENERATIONS OF COMPUTERS.=
RJMM63       MAGNETIC     MEMORIES   - CAPABILITIES AND LIMITATIONS.=
ARCO65   VE ASSOCIATIVE   MEMORIES   =CALCULATIONS OF SPEED OF LADDER NETWORK FOR SUPER-CONDUCTI
AJEO61   NG ASSOCIATIVE   MEMORIES   =EVALUATION OF SYSTEMS USI
ARCM63     CRYOELECTRIC   MEMORIES   =
ARSA63   VE ASSOCIATIVE   MEMORIES   =SUPERCONDUCTI
ARTB65   WORK-ORGANIZED   MEMORIES   =THE BRIDGE CELL - A NEW SUPERCONDUCTIVE MEMORY CELL FOR RANDOM-ACCESS
ABSM64   UPERCONDUCTIVE   MEMORIES   =S
BLCM64     CRYOELECTRIC   MEMORIES   =
FSGO62   PERCEIVING AND   MEMORIZING   MACHINE.=GENERALIZATION OF AN ELEMENTARY
WLAS70   AN ASSOCIATIVE   MEMORY       USING LARGE SCALE INTEGRATION =AN ASS
MJAO69   OF ASSOCIATIVE   MEMORY       OR CONTENT-ADDRESSABLE MEMORY SYSTEMS AND A KWIC INDEX TO THE LITERATURE 1956-
RPAG69   TENT-ADDRESSED   MEMORY       SYSTEM=A GLASS DELAY LINE CON
MJAO69   ADDRESSABLE      MEMORY       SYSTEMS AND A KWIC INDEX TO THE LITERATURE 1956-1970=AN OVERVIEW OF ASSOCIATIV
ACAM68     ASSOCIATIVE    MEMORY       INVESTIGATIONS : SUBSTRUCTURE SEARCHING AND DATA ORGANIZATION.=
FWOA69     ASSOCIATIVE    MEMORY        PARALLEL LANGUAGE, AMPPL-II.=ON A NEW TOOL IN ARTIFICIAL INTELLIGENCE RESEARC
SWAS68   TENT-ADDRESSED   MEMORY       MODEL.=A SEQUENTIALLY HOMING CON
TFAM68   IC ASSOCIATIVE   MEMORY       =A MAGNET
NCAM64     ASSOCIATIVE    MEMORY       SYSTEM IMPLEMENTATION AND CHARACTERISTICS.=
RWFM68        FERRITE     MEMORY       SYSTEMS.=
P7MF68    MAGNETIC FILM   MEMORY       SYSTEMS.=
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BH0064    ONTINUOUS FILM    MEMORY    CELL.=OPERATION OF THE CRYOGENIC C
GGAP66    NG ASSOCIATIVE    MEMORY    =A POSSIBLE MODEL OF A NETWORK PROCESSI
TRCA64    ER ASSOCIATIVE    MEMORY    FINAL REPORT.=COMPUT
SRAS60    E SELF-SORTING    MEMORY    REVISED.=ASSOCIATIV
CSSI63    CATIONS OF NEW    MEMORY    DEVELOPMENTS.=SYSTEMS IMPLI
BPAH67    ED ASSOCIATIVE    MEMORY    =A HIGH-SPE
TRFS61    IC ASSOCIATIVE    MEMORY    =FEASIBILITY STUDY FOR A CRYOGEN
GAH067       ASSOCIATIVE    MEMORY    =HANDBOOK OF OPERATING AND MAINTENANCE - INSTRUCTIONS FOR
IBCA      IC ASSOCIATIVE    MEMORY    TECHNIQUES.=CRYOGEN
BVM066     MODELING OF A    MEMORY    SYSTEM INCLUDING A BUFFER ASSOCIATIVE MEMORY UNIT.=
IBAM66       ASSOCIATIVE    MEMORY    =
LBFR65     RESISTOR-CARD    MEMORY    =FIXED
KJA063    ARALLEL-SEARCH    MEMORY    =APPLICATION OF A P
LSAM63    TENT ADDRESSED    MEMORY    =ALL MAGNETIC CON
KJAH64    IC ASSOCIATIVE    MEMORY    =A 128-WORD, 36-BIT MAGNET
KPAM61    IC ASSOCIATIVE    MEMORY    =A MAGNET
KRMA62                      MEMORY    ARRAY SEARCHING SYSTEM.=
HBSU64    AN ASSOCIATIVE    MEMORY    AS A REAL-TIME CONTROL.=SOME USES OF
KSTA64    NTATIVE SEARCH    MEMORY    =THEORY AND ORGANIZATION OF A REPRESE
HAST63     THEORIZING ON    MEMORY    STRUCTURE AND INFORMATION RETRIEVAL.=SOME
GFCA67    IC ASSOCIATIVE    MEMORY    =CRYOGEN
IBMS66                      MEMORY    SYSTEM.=
MJTS64        THE SEARCH    MEMORY    IN AN INFORMATION RETRIEVAL SYSTEM.=
JM0064    AN ASSOCIATIVE    MEMORY    =ON ORDERED RETRIEVAL FROM
IBAM66       ASSOCIATIVE    MEMORY    SYSTEM.=
HSSO64    OR ASSOCIATIVE    MEMORY    SYSTEMS.=STUDY OF ELASTIC SWITCHING F
LAAA61    ST ASSOCIATIVE    MEMORY    TO REDUCE THE ACCESS TIME FOR INSTRUCTIONS IN LOOPS.=AN APPLICATION FOR A SMAL
MRAC62     ' ASSOCIATIVE    MEMORY    =A CRYOGENIC ' BETWEEN LIMITS
JKTT62     WITH A SEARCH    MEMORY    =TARGET TRACK CORRELATION
GPAM         ASSOCIATIVE    MEMORY    TECHNIQUES.=
GAC062    ON ASSOCIATIVE    MEMORY    =COLLECTION OF NOTES
FKTP64    TED-WOVEN WIRE    MEMORY    MATRIX.=THE PLA
FTAP65    IRE ASSOCIATED    MEMORY    =A WOVEN PLATED-W
LAC062    AN ASSOCIATIVE    MEMORY    =CODING OF TREES FOR USE IN
HRIT63    ING THE SEARCH    MEMORY    WITH THE USQ-20 COMPUTER.=INTEGRAT
MSU064    SE OF STANDARD    MEMORY    SYSTEMS AS ASSOCIATIVE MEMORIES FOR INTEGRATING STORAGE OF MULTIPARAMETER DATA
IBAM66       ASSOCIATIVE    MEMORY    =
HUAC67    NT ADDRESSABLE    MEMORY    WITH APPLICATIONS TO MACHINE TRANSLATION.=A CONTE
IBAM67       ASSOCIATIVE    MEMORY    =
GECA67    TENT ADDRESSED    MEMORY    =CON
GYOR65       ASSOCIATIVE    MEMORY    =ORDERED RETRIEVAL OF A MULTI-COMPONENT ANSWER FROM
LAAM65       ASSOCIATIVE    MEMORY    WITH NEAREST MATCH.=
FRCA63    NT-ADDRESSABLE    MEMORY    SYSTEMS.=CONTE
HHCM64         CRYOGENIC    MEMORY    SYSTEMS.=
IKAH66    ND ASSOCIATIVE    MEMORY    USING INTEGRATED MOS TRANSISTORS.=A 150-NANOSECO
IBAM65       ASSOCIATIVE    MEMORY    =
HWI061    F WOVEN-SCREEN    MEMORY    TECHNIQUES.=INVESTIGATION O
MAAT65     FILM COMPUTER    MEMORY    USING A REASONANT ABSORPTION NON-DESTRUCTIVE READ-OUT TECHNIQUE.=A THIN MAGNET
GEAM67       ASSOCIATIVE    MEMORY    =
HGQR57    -RANDOM ACCESS    MEMORY    SYSTEM.=QUASI
HAHA63    ES ASSOCIATIVE    MEMORY    =HUGH
IBTA66     TAG ADDRESSED    MEMORY    =
LACA65    ON ASSOCIATIVE    MEMORY    CELL.=CRYOTR
IYAI      OR ASSOCIATIVE    MEMORY    WITH 100-NANOSECONDS CYCLE TIME.=AN INTEGRATED MOS TRANSIST
IBAM66       ASSOCIATIVE    MEMORY    SYSTEM.=
IBAM65       ASSOCIATIVE    MEMORY    SYSTEM.=
IBAM66       ASSOCIATIVE    MEMORY    SYSTEM.=
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IBAM65	ASSOCIATIVE	MEMORY	READOUT CIRCUIT.=
LTEM60	ECTRODEPOSITED	MEMORY	ELEMENTS FOR A NON-DESTRUCTIVE MEMORY.=EL
HBAT65	SSOCIATIVE TAG	MEMORY	=A
IBCM65	CRYOGENIC	MEMORY	SYSTEM.=
MPAM61	IC ASSOCIATIVE	MEMORY	SYSTEM.=A MAGNET
IBAA60	AN ASSOCIATIVE	MEMORY	USING SUPERCONDUCTIVE TECHNIQUES.=AN ASS
GAAM67	ASSOCIATIVE	MEMORY	=
LRO062	ATION OF LARGE	MEMORY	SYSTEMS. =ORGANIZ
IBLM60	LOGICAL	MEMORY	STUDY.=
IBAM65	ASSOCIATIVE	MEMORY	=
MBAM65	ASSOCIATIVE	MEMORY	STRUCTURE.=
GAAM67	ASSOCIATIVE	MEMORY	=
LTEM60	STRUCTIVE	MEMORY	=ELECTRODEPOSITED MEMORY ELEMENTS FOR A NON-DE
BRCA66	NT ADDRESSABLE	MEMORY	=CONTE
SHCA66	TENT-ADDRESSED	MEMORY	USING MAGNETO- OR ELECTRO-OPTICAL INTERROGATION.=CON
TKAT61	NONDESTRUCTIVE	MEMORY	ELEMENT USING BIAS RESTORATION.=A TOROIDAL
EFAF63	NT-ADDRESSABLE	MEMORY	ORGANIZATION.=ALGORITHMS FOR CONTE
YYPR66	AN ASSOCIATIVE	MEMORY	=PATTERN RECOGNITION USING
CJTF67	UPERCONDUCTION	MEMORY	=TRAPPED-FLUX S
CYAO65	TENT-ADDRESSED	MEMORY	FOR DYNAMIC STORAGE ALLOCATION.=APPLICATION OF CON
BFOT	AN ASSOCIATIVE	MEMORY	=ON THE EVOLUTION OF AUTONOMY FOR
BCAM65	ASSOCIATIVE	MEMORY	CIRCUIT.=
BUPP66	ASSOCIATIVE	MEMORY	=PRELIMINARY PROGRAMMING MANUAL FOR RADC 2048 WORD
YTAC67	IC ASSOCIATIVE	MEMORY	=A CRYOGEN
SFAC64	TRIBUTED LOGIC	MEMORY	WITH APPLICATIONS TO INFORMATION RETRIEVAL.=A CONTENT-ADDRESSABLE DIS
SSSO64	TENTIAL SEARCH	MEMORY	- IMPLEMENTATION AND TECHNIQUES.=SURVEY OF PRESENT AND PO
CATK62	IT ASSOCIATIVE	MEMORY	WORKS AT ROOM TEMPERATURE.=3-K B
YCAS64	ON ASSOCIATIVE	MEMORY	IN DIGITAL SYSTEMS.=A STUDY OF CRYOTR
BJAS61	IC ASSOCIATIVE	MEMORY	AND CODE CONVERTER.=A SEMI-PERMANENT MAGNET
SWAM63	ASSOCIATIVE	MEMORY	TECHNIQUES FOR LARGE DATA PROCESSORS.=
BCAM66	ASSOCIATIVE	MEMORY	=
DPAS62	VE ASSOCIATIVE	MEMORY	=A SUPERCONDUCTI
BSCS65	F CRYOELECTRIC	MEMORY	PLANES.=CAVITY SENSING O
SHCO67	TENT-ADDRESSED	MEMORY	USING MAGNETO- OR ELECTRO-OPTICAL INTERROGATION.'=COMMENT ON ' CON
GECM65	CRYOGENIC	MEMORY	=
SRCA67	TENT ADDRESSED	MEMORY	=CON
ADAD61	TO ASSOCIATIVE	MEMORY	=A DELAY LINE APPROACH
FJAM61	ASSOCIATIVE	MEMORY	APPLICATIONS IN INTELLIGENCE DATA PROCESSING.=
WDHS64	NG, MASS	MEMORY	=HIGH-SPEED, CONTENT SEARCH IN A LARGE, ROTATI
BLDO62	CALE CRYOGENIC	MEMORY	SYSTEM.=DESIGN OF A LARGE-S
DBAS66	ID ASSOCIATIVE	MEMORY	PROCESSOR.=A STUDY OF THE UTILITY OF A HYBR
AKAM68	ASSOCIATIVE	MEMORY	IN LARGE COMPUTER SYSTEM.=
AKAI68	ED ASSOCIATIVE	MEMORY	MATRIX.=AN INTEGRAT
YMLC62	LARGE-CAPACITY	MEMORY	TECHNIQUES FOR COMPUTING.=LARGE-
BRCA66	NT ADDRESSABLE	MEMORY	=CONTE
WRDA64	AN ASSOCIATIVE	MEMORY	FOR NEBULA COMPUTER.=ON
BRAL68	ED ASSOCIATIVE	MEMORY	NETWORK.=A LOCALLY-DISTRIBUT
TRCA64	ER ASSOCIATIVE	MEMORY	STUDY.=COMPUT
CRAT62	DE ASSOCIATIVE	MEMORY	=A TUNNEL DIO
CMSO64	OF ASSOCIATIVE	MEMORY	APPLICATION.=STUDY
YCPR66	AN ASSOCIATIVE	MEMORY	=PATTERN RECOGNITION BY
FMOI61	AN ASSOCIATIVE	MEMORY	=OPERATIONS IN
YYAC66	AR ASSOCIATIVE	MEMORY	=A CUTPOINT CELLUL
CHDA62	AN ASSOCIATIVE	MEMORY	=DIMENSION:
BRCA67	NT-ADDRESSABLE	MEMORY	=CONTE
CJRO64	ET ASSOCIATIVE	MEMORY	=RESEARCH ON FERR
FMLA62	SOCIATIVE	MEMORY	=LOGICAL AND FUNCTIONAL SPECIFICATION OF AN AS

```
ASTA67    : A RELATIONAL    MEMORY    WITH AN ASSOCIATIVE BASE.=TRAMP
YCAM66     ASSOCIATIVE      MEMORY    SYSTEMS AND THEIR APPLICATIONS TO PICTURE AND ARITHMETIC PROCESSES.=
STFS61    IC ASSOCIATIVE    MEMORY    =FEASIBILITY STUDY FOR A CRYOGEN
GECM65        CRYOGENIC     MEMORY    =
FHCC61    ENT, READ ONLY    MEMORY    =CARD CAPACITOR - A SEMI-PERMAN
CVOR67    AL ASSOCIATIVE    MEMORY    =ORDERED RETRIEVAL FROM A DECIM
RPDA68    NT-ADDRESSABLE    MEMORY    SYSTEM.=DESIGN AND EVALUATION OF A GLASS DELAY LINE CONTE
ACTC65    NE ASSOCIATIVE    MEMORY    FOR INFORMATION RETRIEVAL.=TOWARDS CONTROLLED EXPERIMENTS IN THE CONSTRUCTION
FERO61    AN ASSOCIATIVE    MEMORY    =RETRIEVAL OF INFORMATION WITH.
BLCS60    UPERCONDUCTING    MEMORY    =CONTINUOUS SHEET S
FWAM64       ASSOCIATIVE    MEMORY    =
RCAM66       ASSOCIATIVE    MEMORY    =
BBCR64     RANDOM ACCESS    MEMORY     PHASE 2 10 ( 9 ) BIT MEMORY.=CRYOELECTRIC
RPEO67    NT-ADDRESSABLE    MEMORY    SYSTEMS USING GLASS DELAY LINES.=EVALUATION OF THREE CONTE
CWCA65    NT-ADDRESSABLE    MEMORY    TECHNIQUES.=CONTE
SGAM63    AN ASSOCIATIVE    MEMORY    =A MATHEMATICAL MODEL FOR
HPAM65       ASSOCIATIVE    MEMORY    COMPUTER SYSTEM DESCRIPTION AND SELECTED NAVAL APPLICATIONS.=
SRSM61    AN ASSOCIATIVE    MEMORY    =SYMBOL MANIPULATION WITH
RLCM65        CRYOGENICS    MEMORY    PLANE INTERCONNECTION TECHNIQUES.=
STCA64    ER ASSOCIATIVE    MEMORY    STUDY.=COMPUT
SGAM63       ASSOCIATIVE    MEMORY    COMPUTERS FROM THE PROGRAMMING POINT OF VIEW.=
SDSD64    GN OF A SEARCH    MEMORY    =SYSTEM DESI
MSAM63              A       MEMORY    ORGANIZATION FOR AN ELEMENTARY LIST PROCESSING COMPUTER.=
PCAM67     ASSOCIATIVE      MEMORY    COMPILER TECHNIQUES STUDY.=
ABCA64    IC ASSOCIATIVE    MEMORY    TECHNIQUES.=CRYOGEN
RJCA64    IC ASSOCIATIVE    MEMORY    RESEARCH.=CRYOGEN
SMMO64                      MEMORY    ORGANIZATION OF A 7090 TO DO STATISTICAL ASSOCIATION PROCESSING.=
RRTC64    NT-ADDRESSABLE    MEMORY    =TRANSFLUXOR CONTE
RWAM63       ASSOCIATIVE    MEMORY    ALGORITHMS AND THEIR CRYOGENIC IMPLEMENTATION.=
CRCA67    NT-ADDRESSABLE    MEMORY    TECHNIQUES.=CONTE
BACR66     RANDOM ACCESS    MEMORY    - PHASE 3.=CRYOELECTRIC
BBCR64     ( 9 ) BIT        MEMORY    =CRYOELECTRIC RANDOM ACCESS MEMORY, PHASE 2 10
SRLF63    INATED FERRITE    MEMORY    =LAM
BLCR65     RANDOM ACCESS    MEMORY     PHASE 3.=CRYOELECTRIC
PITM61    HE ASSOCIATIVE    MEMORY    =THE MULTI-LIST SYSTEM, PART 1 : T
PGAR63    OCIATIVE          MEMORY    =A READ-ONLY MULTI-MEGABIT PARALLEL SEARCH ASS
STGS68    AN ASSOCIATIVE    MEMORY     APPROACH.=GRAPHICAL SYSTEMS COMMUNICATIONS :
SATW59    WOVEN CRYOTRON    MEMORY     =THE
RRTA67    ED ASSOCIATIVE    MEMORY    ADDRESSING.=TRANSLAT
PGTO62    PE ASSOCIATIVE    MEMORY    =THE ORGANIZATION OF A MULTI-LIST TY
SHTA62     TAG-ADDRESSED    MEMORY    =
YYAC66    IC ASSOCIATIVE    MEMORY    SYSTEM FOR INFORMATION RETRIEVAL.=A CRYOGEN
SLAM62       ASSOCIATIVE    MEMORY    WITH ORDERED RETRIEVAL.=
PECM57          CRYOTRON    MEMORY    SYSTEMS.=
SRCA60    IC ASSOCIATIVE    MEMORY    =CRYOGEN
RCCA66    TENT-ADDRESSED    MEMORY    =CON
PGML62    ED ASSOCIATIVE    MEMORY    =MULTI-LIST ORGANIZ
CWCA66    NT-ADDRESSABLE    MEMORY    TECHNIQUES.=CONTE
CWCA65    NT-ADDRESSABLE    MEMORY    TECHNIQUES.=CONTE
RPAI66       ASSOCIATIVE    MEMORY    SYSTEM.=AN INVESTIGATION INTO PAGING A SOFTWARE-SIMULATED
RHTW68    2D CORE SEARCH    MEMORY    =2-1/
RDAM67       ASSOCIATIVE    MEMORY    CELL.=
SHMA64                      MEMORY    AND CIRCUITS THEREFOR.=
RCMF61     MAGNETIC FILM    MEMORY    DESIGN.=
TRAM67       ASSOCIATIVE    MEMORY    SYSTEM.=
BACC61    UPERCONDUCTIVE    MEMORY    =COINCIDENT CURRENT S
TRAM66       ASSOCIATIVE    MEMORY    =
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BCAL63	Y CRYOELECTRIC	MEMORY	WITH CAVITY SENSING.=A LARGE CAPACIT
NFAC62	DATA ADDRESSED	MEMORY	=A CRYOGENIC
TRTC62	NT-ADDRESSABLE	MEMORY	=TRUE CONTE
CMAM64	ASSOCIATIVE	MEMORY	SYSTEM IMPLEMENTATION AND CHARACTERISTICS.=
TGHT63	O QUIZ A WHOLE	MEMORY	AT ONCE.=HOW T
RJCA64	IC ASSOCIATIVE	MEMORY	TECHNIQUES.=CRYOGEN
KPTR63	THE ROPE	MEMORY	- A PERMANENT STORAGE DEVICE.=
CDCA65	NT ADDRESSABLE	MEMORY	SYSTEMS CONCEPTS.=CONTE
LMRO62	TENT ADDRESSED	MEMORY	=RETRIEVAL OF ORDERED LISTS FROM A CON
BHAM65	ASSOCIATIVE	MEMORY	USING ANALOG SUMMING TECHNIQUE.=
BRNA66	S DELAY LINE	MEMORY	=NEBULA: A DIGITAL COMPUTER USING A 20 MC GLAS
WMTM63	TAG	MEMORY	=
ARTB65	UPERCONDUCTIVE	MEMORY	CELL FOR RANDOM-ACCESS WORK-ORGANIZED MEMORIES.=THE BRIDGE CELL - A NEW S
PCAT64	10MO NDRO BIAX	MEMORY	OF 1024 WORD, 48 BIT PER WORD CAPACITY.=A
AJSO62	GE ASSOCIATIVE	MEMORY	=SEARCH ON RAN
TIHS61	HIGH-SPEED	MEMORY	USES TUNNEL DIODES.=
LBFA63	ED ASSOCIATIVE	MEMORY	USING EVAPORATED ORGANIC DIODE ARRAYS.=FIX
KMAH65	OVEN READ ONLY	MEMORY	=A HIGH-SPEED, W
PGAS64	SEMIPERMANENT	MEMORY	UTILIZING CORRELATION ADDRESSING.=A
SMTC57	YOTRON CATALOG	MEMORY	SYSTEM.=THE CR
MHRM64	AN ASSOCIATIVE	MEMORY	=RESOLVING MULTIPLE RESPONSES IN
KAAS63	A SEARCH	MEMORY	SUBSYSTEM FOR A GENERAL PURPOSE COMPUTER.=
CGBP65	TRIBUTED LOGIC	MEMORY	=BULK PROCESSING IN DIS
SSTF60	YOTRON CATALOG	MEMORY	=THIN-FILM CR
SRAS60	E SELF-SORTING	MEMORY	=ASSOCIATIV
CYAD65	UT ASSOCIATIVE	MEMORY	=A DESTRUCTIVE-READO
CRAP64	AN ASSOCIATIVE	MEMORY	USING MAGNETIC FILMS.=A PROPOSAL FOR
CLAC67	TRIBUTED LOGIC	MEMORY	=A CRYOELECTRIC DIS
CRSA63	OF ASSOCIATIVE	MEMORY	=SHIFT: A REALIZABLE FORM
CSDT66	TENT-ADDRESSED	MEMORY	=DESIGN TECHNIQUES OF A DELAY-LINE CON
ENAO65	ONTINUOUS FILM	MEMORY	=ANALYSIS OF THE CRYOGENIC C
NFDA62	DATA ADDRESSED	MEMORY	USING THIN-FILM CRYOTRONS.=DATA A
FETM60	TRIE	MEMORY	=
LPAC63	TRIBUTED LOGIC	MEMORY	WITH APPLICATION TO INFORMATION RETRIEVAL.=A CONTENT ADDRESSABLE DIS
SAAC62	A CRYOTRON	MEMORY	CELL.=
GIAI65	IMPROVED CELL	MEMORY	=AN
GRAH64	R SEARCH	MEMORY	=A HARDWARE INTEGRATED GENERAL PURPOSE COMPUTE
SWSA63	TREE ORIENTED	MEMORY	SYSTEM.=STORAGE AND SEARCH PROPERTIES OF A
RRAT63	OSECOND SEARCH	MEMORY	=A 300 NAN
GFLT61	ODIFIED	MEMORY	=LOCATING THE LARGEST WORD IN A FILE USING A M
SRAS67	CIATIVE SEARCH	MEMORY	STUDY.=ASSO
SGAO64	SS DISTRIBUTED	MEMORY	=APPLICATION OF AN ASSOCIATIVELY ADDRE
HACA66	ND ASSOCIATIVE	MEMORY	SYSTEMS - A SURVEY.=CONTENT-ADDRESSABLE A
CFLP68	EVISED SIMPLEX	METHOD	=LINEAR PROGRAMMING IMPLEMENTATION IN ILLIAC-IV, I : R
FGAM61	A	METHOD	FOR RESOLVING MULTIPLE RESPONSES IN A PARALLEL SEARCH FILE.=
RIMO67		METHODS	OF SELECTING A MULTIVALENT ANSWER FROM ASSOCIATIVE MEMORY.=
CGMM66	MANUFACTURING	METHODS	FOR CRYOELECTRIC MEMORIES.=
CGMM67	MANUFACTURING	METHODS	FOR CRYOELECTRIC MEMORIES.=
MRSO67	SURVEY OF	MICROCELLULAR	RESEARCH.=
HJOI60	CONSTRUCTED OF	MICROELECTRONIC	COMPONENTS AND SYSTEM.=ON ITERATIVE CIRCUIT COMPUTER
JSTD62	4096 WORD ONE	MICROSECOND	MAGNETIC FILM STORE.=THE DESIGN OF A
HCMR61	ALIZATIONS FOR	MIRF	EMPLOYING ONE FLUX PATH PER FILE ITEM.=MAGNETIC RE
VEMR61	EALIZATION FOR	MIRF	EMPLOYING ONE CONDUCTIVE PATH PER FILE ITEM.=MAGNETIC R
NJMI61		MIRF	(MULTIPLE INSTANTANEOUS RESPONSE FILE).=
BGAM69	A	MISSION	ORIENTED ASSOCIATIVE PROCESSOR USING PLATED WIRE.=
GASO69	STUDY OF	MISSION	EFFECTIVENESS OF ASSOCIATIVE PROCESSOR IN AWACS.=
SWAS68	DRESSED MEMORY	MODEL	=A SEQUENTIALLY HOMING CONTENT-AD

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ADAM69                  A       MODEL           FOR PARALLEL COMPUTATIONS.=
KNTL62      E LOOKUP STUDY      MODEL           =TARL
GGAP66          A POSSIBLE      MODEL           OF A NETWORK PROCESSING ASSOCIATIVE MEMORY=
BSLS68      ING SYSTEMS :       MODEL            BUILDING, SIMULATION AND EVALUATION.=LARGE SCALE INFORMATION PROCESS
SGAM63      A MATHEMATICAL      MODEL           FOR AN ASSOCIATIVE MEMORY.=A MATH
RBAG67            A GRAPH       MODEL           FOR PARALLEL COMPUTATIONS.=
NKPM65      ENOMENOLOGICAL      MODEL           FOR THE BIAX.=PH
KMPO66      ROPERTIES OF A      MODEL           FOR PARRALLEL COMPUTATIONS: DETERMINACY, TERMINATION, QUEUEING.=P
BVMO66                          MODELING        OF A MEMORY SYSTEM INCLUDING A BUFFER ASSOCIATIVE MEMORY UNIT.=
WLAM70      CIATIVE MEMORY      MODELS          =ASSO
GHMM68        MATHEMATICAL      MODELS          OF INFORMATION SYSTEMS.=
MEMO67                          MODELS          OF COMPUTATIONAL SYSTEMS - CYCLIC TO ACYCLIC GRAPH TRANSFORMATIONS.=
ASAM67                  A       MODIFICATION    OF LEE'S PATH CONNECTION ALGORITHM.=
SHAP69      UGH THE USE OF      MODIFIED        MEMORIES.=ASSOCIATIVE PROCESSING FOR GENERAL PURPOSE COMPUTERS THRO
SHAP68      UGH THE USE OF      MODIFIED        MEMORIES.=ASSOCIATIVE PROCESSING FOR GENERAL PURPOSE COMPUTERS THRO
CWAM63                  A       MODIFIED        HOLLAND MACHINE.=
GELT61      A FILE USING A      MODIFIED         MEMORY.=LOCATING THE LARGEST WORD IN
VITA69       CONTROLLED BY      MONOPOLAR       CURRENTS.=THE ANALYSIS OF THE CRYOTRONIC ASSOCIATIVE ELEMENT
BSSO69       COMPLEMENTARY      MOS             CIRCUITS FOR HIGH SPEED ASSOCIATIVE MEMORY=SILICON-ON-SAPPHIRE
IYAI67       AN INTEGRATED      MOS             TRANSISTOR ASSOCIATIVE MEMORY SYSTEM WITH 100 NANOSECOND CYCLE TIME.=
IYAI         AN INTEGRATED      MOS             TRANSISTOR ASSOCIATIVE MEMORY WITH 100-NANOSECONDS CYCLE TIME.=
IKAH66      ING INTEGRATED      MOS              TRANSISTORS.=A 150-NANOSECOND ASSOCIATIVE MEMORY US
NTAM69                  A       MULTIACCESS     ASSOCIATIVE MEMORY=
RPMP63                          MULTIDIMENSIONAL PULSE-HEIGHT ANALYZER APPLICATION OF AN ASSOCIATIVE PROGRAMMED COMPUTER.=
PNMC66      M SOLVING WITH      MULTILIST       =MAN-COMPUTER PROBLE
PGTO62      ANIZATION OF A      MULTILIST-TYPE  ASSOCIATIVE MEMORY.=THE ORG
MSUO64      ING STORAGE OF      MULTIPARAMETER  DATA BY AUTOMATIC DATA REDUCTION.=USE OF STANDARD MEMORY SYSTEMS AS ASSOCIATI
FPAM69                  A       MULTIPLE        INSTRUCTION STREAM PROCESSOR WITH SHARED RESOURCES.=
GKAC67      MORY DRIVEN BY      MULTIPLE        COINCIDENT PULSES=A CONTINUOUS FILM ME
YHDO64      VELOPMENT OF A      MULTIPLE        INSTANTANEOUS RESPONSE FILE : THE AN/GSQ-81 DOCUMENT DATA INDEXING SET.=DE
GMAC60         A CRYOGENIC      MULTIPLE        INSTANTANEOUS RESPONSE FILE.=
BRTU68          THE USE OF      MULTIPLE        ASSOCIATIVE MEMORIES IN PROGRAMMING THE GROWING MACHINE.=
GGMI61                          MULTIPLE        INSTANTANEOUS RESPONSE FILE.=
HWSM66        SIMULTANEOUS      MULTIPLE        RESPONSE IN ASSOCIATIVE MEMORIES AND READOUT OF THE DETECTOR MATRIX.=
LWAM                .     A     MULTIPLE        FILE ORGANIZATION FOR INFORMATION RETRIEVAL SYSTEMS.=
EFMA64                          MULTIPLE        ADDRESSING FOR FIXED-TAG ASSOCIATIVE MEMORIES.=
YHDO64      N EXPERIMENTAL      MULTIPLE        INSTANTANEOUS RESPONSE FILE.=DESIGN OF A
FRAA64      NALYSIS OF THE      MULTIPLE        INSTANTANEOUS RESPONSE FILE.=AN A
WDMP64                          MULTIPLE        PROCESSING TECHNIQUES.=
FGAM61       FOR RESOLVING      MULTIPLE        RESPONSES IN A PARALLEL SEARCH FILE.=A METHOD
WHPF63      SIMULTANEOUS        MULTIPLE        RESPONSES.=PROPOSAL FOR ORDERED SEQUENTIAL DETECTION OF
MHRM64           RESOLVING      MULTIPLE        RESPONSES IN AN ASSOCIATIVE MEMORY.=
NJNI61              MIRF (      MULTIPLE        INSTANTANEOUS RESPONSE FILE ).=
BIAM71                  A       MULTIPLEXED     I/O SYSTEM FOR REAL TIME COMPUTERS =
WRAT        E MEMORIES AND      MULTIPLE-WORD   ACCESS MEMORIES.=A TRANSISTOR-TUNNEL DIODE CELL FOR ASSOCIATIV
TSSM68       SPARSE MATRIX      MULTIPLICATION  =
FAPS60      E CONTROL IN A      MULTIPROCESSING SYSTEM USING ASSOCIATIVE STORAGE.=PROGRAM SEQUENC
GHAM68                  A       MULTIPROCESSOR  WITH ASSOCIATIVE CONTROL =
HTPC68      L SCHEMES IN A      MULTIPROCESSOR  WITH ASSOCIATIVE CONTROL.=PAGE-CONTRO
GFAT66      IN A                MULTIPROCESSOR  =ASSOCIATIVE TECHNIQUES FOR CONTROL FUNCTIONS ,
CMAM63                  A       MULTIPROCESSOR  SYSTEM DESIGN.=
RAMA67      ALLOCATION FOR      MULTIPROCESSORS =MEMORY
HHAD63      ROL SYSTEM FOR      MULTIPROGRAMMING =A DIRECTORY CONT
BGNO64                          MULTISYSTEM     ORGANIZATION.=
RIMO67      OF SELECTING A      MULTIVALENT     ANSWER FROM ASSOCIATIVE MEMORY.=METHODS
PSUO66              USE OF      MULTIWRITE      FOR GENERAL PROGRAMMABILITY OF SEARCH MEMORIES.=
BDNM60                NEW       MULTI-APERTURE  MAGNETIC LOGIC ELEMENT.=
```

BDMA		MULTI-APERTURE	MAGNETIC LOGIC DEVICES.=
GYOR65	RETRIEVAL OF A	MULTI-COMPONENT	ANSWER FROM ASSOCIATIVE MEMORY.=ORDERED
PGTM63	THE	MULTI-LIST	SYSTEM FOR REAL-TIME STORAGE AND RETRIEVAL.=
PGTM62	THE	MULTI-LIST	TYPE ASSOCIATIVE MEMORY.=
GHOT	HE DESIGN OF A	MULTI-LIST	INFORMATION PROCESSING SYSTEM=ON T
GPTM61	THE	MULTI-LIST	SYSTEM TECHNICAL REPORT NO. 1.=
PGML62		MULTI-LIST	ORGANIZED ASSOCIATIVE MEMORY.=
PGTM61	THE	MULTI-LIST	SYSTEM TECHNICAL REPORT NUMBER 1.=
PGTO62	ANIZATION OF A	MULTI-LIST	TYPE ASSOCIATIVE MEMORY.=THE ORG
PLTM61	THE	MULTI-LIST	SYSTEM, PART 1 : THE ASSOCIATIVE MEMORY.=
PGTM62	THE	MULTI-LIST	SYSTEM FOR THE REAL-TIME SOFTWARE AND RETRIEVAL.=
PGAR63	A READ-ONLY	MULTI-MEGABIT	PARALLEL SEARCH ASSOCIATIVE MEMORY.=
LSAP66		MULTI-PREFORMED	BEAM SONAR SYSTEMS.=ASSOCIATIVE PARALLEL PROCESSING AS APPLIED TO
GGAT67	N A	MULTI-PROCESSOR	SIMULATION INVESTIGATION.=ASSOCIATIVE TECHNIQUES FOR CONTROL FUNCTIONS I
CVTU67	USE OF CODES '	M-OUT-OF-N	' IN ASSOCIATIVE MEMORIES.=THE
NSND62		NANOPHILE	DIGITAL ORGANIZATIONS.=
NSOT63	ORGANIZING THE	NANOPHILE	COMPUTERS.=ORGANI
IYAI67	YSTEM WITH 100	NANOSECOND	CYCLE TIME.=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMORY S
RBAT63	A 300	NANOSECOND	SEARCH MEMORY.=
CGAT61	FOR PROCESSING	NATURAL	LANGUAGES.=A TABLE LOOK-UP MACHINE
CCAM65	SELECTED	NAVAL	APPLICATIONS.=ASSOCIATIVE MEMORY COMPUTER SYSTEM : DESCRIPTION AND
HPAM65	N AND SELECTED	NAVAL	APPLICATIONS.=ASSOCIATIVE MEMORY COMPUTER SYSTEM DESCRIPTIO
CAOT68	MATIONS TO THE	NAVIER	STOKES EQUATIONS.=ON THE CONVERGENCE OF DISCRETE APPROXI
GPNR67	TIVE READOUT (	NDRO	) FROM THIN MAGNETIC FILMS.=NONDESTRUC
AFBI65	- A HIGH SPEED	NDRO	ONE CORE PER BIT ASSOCIATIVE ELEMENT.=BILOC
PCAT64	A 10MO	NDRO	BIAX MEMORY OF 1024 WORD, 48 BIT PER WORD CAPACITY.=
LAAM65	VE MEMORY WITH	NEAREST	MATCH.=ASSOCIATI
BJTL68	DESIGN OF THE	NEBULA	COMPUTER.=THE LOGICAL
WROA64	IVE MEMORY FOR	NEBULA	COMPUTER.=ON AN ASSOCIAT
NWPR66	REPORT ON THE	NEBULA	COMPUTER.=PROGRESS
BRNA66		NEBULA	A DIGITAL COMPUTER USING A 20 MC GLASS DELAY LINE MEMORY.=
BCPR67	REPORT ON THE	NEBULA	COMPUTER.=PROGRESS
FKBD67	COMMUNICATIONS	NETWORK	=BROOKHAVEN DIGITAL
NRSS69	ILIZATION OF A	NETWORK	OF COMPUTERS.=SOME SOFTWARE CONSIDERATIONS IN UT
GGAP66	BLE MODEL OF A	NETWORK	PROCESSING ASSOCIATIVE MEMORY=A POSSI
WESO62	LOMON PARALLEL	NETWORK	PROCESSOR.=SO
BRAL68	CIATIVE MEMORY	NETWORK	=A LOCALLY-DISTRIBUTED ASSO
WDPN64	PARALLEL	NETWORK	COMPUTER (SOLOMON) APPLICATIONS ANALYSES.=
WDSA64	G THE PARALLEL	NETWORK	COMPUTER.=STUDY AND INVESTIGATION TO DEVELOP COMPILER TECHNIQUES REQUIRED FOR
WDPN64	PARALLEL	NETWORK	COMPUTER (SOLOMON).=
WDPN64	PARALLEL	NETWORK	COMPUTER (SOLOMON).=
ARCO65	PEED OF LADDER	NETWORK	FOR SUPER-CONDUCTIVE ASSOCIATIVE MEMORIES.=CALCULATIONS OF S
TRFT66	RIBUTED LOGIC	NETWORKS	=FABRICATION TECHNIQUES FOR BATCH FABRICATION OF DIST
ETTO68	CELLULAR LOGIC	NETWORKS	AND MACHINES.=THEORY OF
CFTN62	THE	NEXT	GENERATION OF COMPUTERS.=
YYAN66	A	NONBULK	ADDITION TECHNIQUE FOR ASSOCIATIVE PROCESSORS.=
GPNR67		NONDESTRUCTIVE	READOUT (NDRO) FROM THIN MAGNETIC FILMS.=
TKAT61	A TOROIDAL	NONDESTRUCTIVE	MEMORY ELEMENT USING BIAS RESTORATION.=
LWSA68	MENTS FAVORING	NON-CONVENTIONAL	TYPES OF COMPUTERS.=SOME ARGU
MAAT65	ABSORPTION	NON-DESTRUCTIVE	READ-OUT TECHNIQUE.=A THIN MAGNETIC FILM COMPUTER MEMORY USING A REASONANT
LTEM60	ELEMENTS FOR A	NON-DESTRUCTIVE	MEMORY.=ELECTRODEPOSITED MEMORY
CYAP67	ING STUDY OF A	NON-NUMERICAL	PROCESSOR.=A PROGRAMM
CCAO	ENT PROBLEM OF	NTDS	=APPLICATION OF ASSOCIATIVE MEMORIES TO THE WEAPON ASSIGNM
HIAA64	TIVE STORE FOR	NUCLEAR	PHYSICS.=AN ASSOCIA
HIGS64	VE STORAGE FOR	NUCLEAR	PHYSICS.=GENERAL SURVEY : ASSOCIATI
BCAM67	VE MEMORIES IN	NUCLEAR	PHYSICS.=ASSOCIATI
PGTM61	CHNICAL REPORT	NUMBER	1.=THE MULTI-LIST SYSTEM TE

HJAU69	ARBITRARY	NUMBER	OF SUB-PROGRAMS SIMULTANEOUSLY.=A UNIVERSAL COMPUTER, CAPABLE OF EXECUTING AN
CWA067	PROCESSING TO	NUMERICAL	WEATHER PREDICTION.=APPLICATION OF PARALLEL
AWAC68	AN ASOCIATIVE	OBJECT	MACHINE=A COMPILER FOR
KEOL62		ONE-LEVEL	STORAGE SYSTEM.=
DGTS64	E STRUCTURE OF	ON-LINE	INFORMATION PROCESSING SYSTEMS.=TH
JLO061	ON	OPERAND	STRUCTURE, REPRESENTATION, STORAGE AND SEARCH.=
AGAD69	THE ILLIAC-IV	OPERATING	SYSTEM.=A DESCRIPTION OF
PFAI69	VICE AND THE	OPERATING	FEATURES OF THE EXPLORATORY CONTENT ADDRESSABLE MEMORY SYSTEM.=AN IMPROVED FIE
SOTR68	RELIABILITY OF	OPERATING	A SUPERCONDUCTING MEMORY CELL - A PERSISTOTRON - IN A MEMORY MATRIX. =THE
GAHO67	HANDBOOK OF	OPERATING	AND MAINTENANCE - INSTRUCTIONS FOR ASSOCIATIVE MEMORY.=
CRIO63	EFFECTS ON THE	OPERATING	SPEED OF SUPERCONDUCTING COMPUTER ELEMENTS.=INFLUENCE OF THERMAL
EPAP67	ENTIALLY	OPERATING	MACHINE ' GAMMA-BARABAN '.=A PARALLEL MACHINE SIMULATOR BASED ON THE SEQU
SJA068	ASYNCHRONOUS	OPERATION	OF AN ITERATIVELY STRUCTURED GENERAL-PURPOSE DIGITAL COMPUTER=
BBO064		OPERATION	OF THE CRYOGENIC CONTINUOUS FILM MEMORY CELL.=
CWSO	SYSTEM	OPERATION	FACTORS.=
FMOI61		OPERATIONS	IN AN ASSOCIATIVE MEMORY.=
AETF61	CONTROL SYSTEM	OPTIMIZATION	PROBLEMS.=THE FIXED-PLUS-VARIABLE COMPUTER SYSTEM IN DYNAMIC PROGRAMMING FORM
SLRA69	VE MEMORY WITH	ORDERED	RETRIEVAL.=RANGE ASSOCIATI
JMO064	ON	ORDERED	RETRIEVAL FROM AN ASSOCIATIVE MEMORY.=
GYOR65		ORDERED	RETRIEVAL OF A MULTI-COMPONENT ANSWER FROM ASSOCIATIVE MEMORY.=
CVOR67		ORDERED	RETRIEVAL FROM A DECIMAL ASSOCIATIVE MEMORY.=
WAED64	ERMINATION AND	ORDERED	RETRIEVAL IN SEARCH MEMORIES.=EXTREME DET
SLAM62	VE MEMORY WITH	ORDERED	RETRIEVAL.=ASSOCIATI
WHPF63	PROPOSAL FOR	ORDERED	SEQUENTIAL DETECTION OF SIMULTANEOUS MULTIPLE RESPONSES.=
LMRO62	RETRIEVAL OF	ORDERED	LISTS FROM A CONTENT ADDRESSED MEMORY.=
WAAS68	OOF OF LEWIN'S	ORDERED-RETRIEVAL	THEOREM FOR ASSOCIATIVE MEMORIES.=A SIMPLE PR
LBFA63	ING EVAPORATED	ORGANIC	DIODE ARRAYS.=FIXED ASSOCIATIVE MEMORY US
ACAM68	HING AND DATA	ORGANIZATION	=ASSOCIATIVE MEMORY INVESTIGATIONS : SUBSTRUCTURE SEARC
PAAC70	ARRAY	ORGANIZATION	=ASSOCIATIVE CAPABILITIES FOR MASS STORAGE THROUGH
KWTD69	ALLEL COMPUTER	ORGANIZATION	=THE DESIGN OF A HIGHLY PAR
GHSM66	CEBORNE MEMORY	ORGANIZATION	=SPA
BKP163	OP ON COMPUTER	ORGANIZATION	=PROCEEDINGS 1962 WORKSH
PGTO62	THE	ORGANIZATION	OF A MULTILIST-TYPE ASSOCIATIVE MEMORY.=
LWAM	MULTIPLE FILE	ORGANIZATION	FOR INFORMATION RETRIEVAL SYSTEMS.=A
MSFO67	, FILE	ORGANIZATION	AND DATA MANAGEMENT. =
KSTA64	THEORY AND	ORGANIZATION	OF A REPRESENTATIVE SEARCH MEMORY.=
LRO062		ORGANIZATION	OF LARGE MEMORY SYSTEMS. =
FRMO67	MACHINE	ORGANIZATION	IN ASSOCIATIVE PARALLEL PROCESSING.=
EFAF63	ESSABLE MEMORY	ORGANIZATION	=ALGORITHMS FOR CONTENT-ADDR
BGMO64	MULTISYSTEM	ORGANIZATION	=
CJOA67		ORGANIZATION	AND APPLICATIONS OF ASSOCIATIVE FILE PROCESSORS.=
PGTO62	THE	ORGANIZATION	OF A MULTI-LIST TYPE ASSOCIATIVE MEMORY.=
SMMO64	MEMORY	ORGANIZATION	OF A 7090 TO DO STATISTICAL ASSOCIATION PROCESSING.=
MSAM63	A MEMORY	ORGANIZATION	FOR AN ELEMENTARY LIST PROCESSING COMPUTER.=
RDAC66	ANCED COMPUTER	ORGANIZATION	STUDY.=ADV
SLAS67	GE AND MACHINE	ORGANIZATION	=ASP : A NEW CONCEPT IN LANGUA
BTAC66	ANCED COMPUTER	ORGANIZATION	=ADV
BKDO65	DIRECTORY	ORGANIZATION	FOR A STORAGE SYSTEM.=
SSCO65	COMPUTER	ORGANIZATION	FOR ARRAY PROCESSING.=
RRAO62	AN	ORGANIZATION	OF AN ASSOCIATIVE CRYOGENIC COMPUTER.=
EGO060		ORGANIZATION	OF COMPUTER SYSTEMS - THE FIXED PLUS VARIABLE STRUCTURE COMPUTER.=
EVO062		ORGANIZATION	OF A ' FIXED-PLUS-VARIABLE ' STRUCTURE COMPUTER FOR COMPUTATION OF EIGENVALUES
HMAP63	ALLEL COMPUTER	ORGANIZATION	AND MECHANIZATIONS.=A PAR
FRVT69	ACCESS MEMORY	ORGANIZATIONS	=VARIABLE TOPOLOGY RANDOM
FRVT69	ACCESS MEMORY	ORGANIZATIONS	=VARIABLE TOPOLOGY RANDOM
GAAG67	RPOSE COMPUTER	ORGANIZATIONS	=ADVANCED GENERAL-PU
NSND62	OPHILE DIGITAL	ORGANIZATIONS	=NAN

```
BFAC62        VANCED COMPUTER   ORGANIZATION-ADDRESSING.=AD
PGML62            MULTI-LIST    ORGANIZED          ASSOCIATIVE MEMORY.=
NSOT63                          ORGANIZING         THE NANOPHILE COMPUTERS.=
BGAM69             A MISSION    ORIENTED           ASSOCIATIVE PROCESSOR USING PLATED WIRE.=
SWSA63        TIES OF A TREE    ORIENTED           MEMORY SYSTEM.=STORAGE AND SEARCH PROPER
USAC58            A COMPUTER    ORIENTED           TOWARDS PROBLEMS.=
SWOP69                          ORTHOGONAL         PROCESSING.=
NJAO69                     AN   OVERVIEW           OF ASSOCIATIVE MEMORY OR CONTENT-ADDRESSABLE MEMORY SYSTEMS AND A KWIC INDEX T
BLAR70        ING PROCESSING    PACKAGE            FOR USE WITH FORTRAN OR A SIMILAR HIGH LEVEL LANGUAGE=A R
LGAS68        TIVE STRUCTURE    PACKAGE            =ASP - A RING IMPLEMENTED ASSOCIA
HTPC68                          PAGE-CONTROL       SCHEMES IN A MULTIPROCESSOR WITH ASSOCIATIVE CONTROL.=
HFTA68        STRATEGIES FOR    PAGING             A LARGE ASSOCIATIVE DATA STRUCTURE.=THE ANALYSIS OF
RPAI66        STIGATION INTO    PAGING             A SOFTWARE-SIMULATED ASSOCIATIVE MEMORY SYSTEM.=AN INVE
SIPC65                          PANEL              : CONTENT ADDRESSABLE MEMORIES.=
BBPO62           SOLUTION OF    PARABOLIC          PARTIAL DIFFERENTIAL EQUATIONS.=PROPERTIES OF A VARIABLE STRUCTURE COMPUTER SY
FRAL67           ASSOCIATIVE    PARALLEL           PROCESSING=ACHIEVING LARGE SCALE COMPUTING CAPABILITIES THROUGH
FNOA67            MEMORY AND    PARALLEL           PROCESSING=ON A COMPUTER LANGUAGE WHICH SIMULATES ASSOCIATIVE
RSIB69        ETWEEN LSI AND    PARALLEL           PROCESSING.=INTERACTION B
ASII65        STORED PROGRAM    PARALLEL           PROCESSOR.=INVESTIGATIONS INTO THE THEORY OF AN INTERACTIVE CIRCUIT
SPAF69        LEXIBLE HIGHLY    PARALLEL           ASSOCIATIVE PROCESSOR=A FAST, F
SDSS65        IAL SESSION ON    PARALLEL           AND CONCURRENT COMPUTER SYSTEMS=SPEC
HTPP70                          PARALLEL           PROCESSOR SYSTEMS, TECHNOLOGIES, AND APPLICATIONS=
SRII67        AC IV-ROUTE TO    PARALLEL           COMPUTERS=ILLI
CHPP69                          PARALLEL           PROCESSING FOR PHASED-ARRAY RADARS.=
BRAA69        CIATIVE MEMORY    PARALLEL           DELTIC REALIZATION FOR ACTIVE SONAR SIGNAL PROCESSING.=AN ASSO
ADAM69           A MODEL FOR    PARALLEL           COMPUTATIONS.=
HTSO69             SURVEY OF    PARALLEL           PROCESSOR APPROACHES AND TECHNIQUES.=
NRPC69                          PARALLEL           COMPUTING STRUCTURES AND ALGORITHMS FOR LOGIC DESIGN PROBLEMS=
GHRA69        RESENTATION OF    PARALLEL           PROCESSABLE STREAMS IN COMPUTER PROGRAMS.=RECOGNITION AND REP
WMAP69           ASSOCIATIVE    PARALLEL           PROCESSING FOR THE FAST FOURIER TRANSFORM.=
PJPD68                          PARALLEL           DATA PROCESSING VIA CRYOELECTRICS.=
BRPA69        R PROGRAMS FOR    PARALLEL           PROCESSING SYSTEMS.=PREPARATION AND EVALUATION OF COMPUTE
BMAA69        MECHANISMS FOR    PARALLEL            PROCESSES.=ANALYSIS AND SYNTHESIS OF CONTROL .
KWTD69        N OF A HIGHLY     PARALLEL           COMPUTER ORGANIZATION.=THE DESIG
FNOA69        IATIVE MEMORY,    PARALLEL           LANGUAGE, AMPPL-II.=ON A NEW TOOL IN ARTIFICIAL INTELLIGENCE RESEARCH : AN ASS
FAAF62        ALGORITHMS FOR    PARALLEL           SEARCH MEMORIES.=ALGORI
SFAA61        ATION TO          PARALLEL           PROGRAMMING.=AN AUTOMATIC SEQUENCING PROCEDURE WITH APPLIC
NRAP64        NGUAGE FOR THE    PARALLEL           PROCESSING OF PICTURES.=A PROGRAMMING LA
LMAS66        PROCESSING AND    PARALLEL           PROCESSORS.=A SURVEY OF PROBLEMS AND PRELIMINARY RESULTS CONCERNING PARALLEL
RMSI66        NDENT TASKS ON    PARALLEL           PROCESSORS.=SCHEDULING INDEPE
LMAS66        CONCERNING        PARALLEL           PROCESSING AND PARALLEL PROCESSORS.=A SURVEY OF PROBLEMS AND PRELIMINARY RESUL
FNUM          IATIVE MEMORY,    PARALLEL            PROCESSING LANGUAGE, AMPPL-II.=USER'S MANUAL FOR THE ASSOC
NAOP60        MMING A HIGHLY    PARALLEL           MACHINE TO BE AN INTELLIGENT TECHNICIAN.=ON PROGRA
SLMF62        CATION, HIGHLY    PARALLEL           SYSTEMS, AND ASSOCIATIVE LOGIC.=MASS FABRI
BEAE63        FECTIVENESS OF    PARALLEL           PROCESSING.=AN EVALUATION OF THE EF
KMEO67        EMS TO PERFORM    PARALLEL           PROCESSING.=EVOLUTION OF COMPUTER SYST
HSAP60             AUTOMATIC    PARALLEL           PROCESSING.=
EBPP63                          PARALLEL           PROCESSING IN A RESTRUCTURABLE COMPUTER SYSTEM.=
SPPA62        GN OF A HIGHLY    PARALLEL           COMPUTER.=PHYSICAL AND LOGICAL DESI
NJHP66              HIGHLY      PARALLEL           INFORMATION PROCESSING SYSTEMS. =
LSAP66           ASSOCIATIVE    PARALLEL           PROCESSING AS APPLIED TO MULTI-PREFORMED BEAM SONAR SYSTEMS.=
SJAI64         ALGORITHMS IN    PARALLEL           COMPUTATION.=
IRSO63        PPLICATIONS OF    PARALLEL           SEARCH MEMORIES.=STUDY OF THE A
SJAT64                  AT-1    PARALLEL           COMPUTER - SECOND PRELIMINARY VERSION.=
RRAA64        ALKS ON HIGHLY    PARALLEL            MACHINES.=A ALGORITHM FOR CONCURRENT RANDOM W
WESO62              SOLOMON     PARALLEL           NETWORK PROCESSOR.=
BAAO66        F PROGRAMS FOR    PARALLEL           PROCESSING.=ANALYSIS O
```

GAA063	PPLICATIONS OF	PARALLEL	SEARCH MEMORIES.=A
AJPS65	STRUCTURES FOR	PARALLEL	PROCESSING.=PROGRAM
FRAL	H ASSOCIATIVE	PARALLEL	PROCESSING.=ACHIEVING LARGE COMPUTING CAPABILITIES THROUG
SPPA63	NS OF A HIGHLY	PARALLEL	COMPUTER.=PROGRAMMING AND DESIGN CONSIDERATIO
BBCO68	XPRESSIONS FOR	PARALLEL	COMPUTATIONS.=COMPILATION OF ARITHMETIC E
RDSO68	ON A SIMULATED	PARALLEL	PROCESSING SYSTEM.=SOLUTION OF THE DIRICHLET PROBLEM
FRMO67	IN ASSOCIATIVE	PARALLEL	PROCESSING.=MACHINE ORGANIZATION
FRAP67	ASSOCIATIVE	PARALLEL	PROCESSING.=
CWHP62	HIGHLY	PARALLEL	MACHINES.=
CHEO65	H-FABRICATABLE	PARALLEL	COMPUTER.=ECONOMICS OF THE DLM, A BATC
PJAA65	AN APPROACH TO	PARALLEL	PROCESSING.=AN APP
WDPN64		PARALLEL	NETWORK COMPUTER (SOLOMON) APPLICATIONS ANALYSES.=
FRAP67	ASSOCIATIVE	PARALLEL	PROCESSING.=
KMPP66		PARALLEL	PROCESSING COMPUTER SYSTEM.=
RJAC67	ROGRAMMING FOR	PARALLEL	PROCESSORS.=A CASE STUDY IN P
PSAA67	AN ABSTRACT	PARALLEL	PROCESSING SYSTEM.=
RRAG67	RAPH MODEL FOR	PARALLEL	COMPUTATIONS.=A G
EPAP67	A	PARALLEL	MACHINE SIMULATOR BASED ON THE SEQUENTIALLY OPERATING MACHINE ' GAMMA-BARABAN
SDAP67	A	PARALLEL	COMPUTING APPROACH TO DIGITAL SIMULATION.=
PGAR63	MULTI-MEGABIT	PARALLEL	SEARCH ASSOCIATIVE MEMORY.=A READ-ONLY
WDSA64	ROGRAMMING THE	PARALLEL	NETWORK COMPUTER.=STUDY AND INVESTIGATION TO DEVELOP COMPILER TECHNIQUES REQUI
MDTA66	MPUTATIONS ON	PARALLEL	PROCESSOR SYSTEMS.=THE AUTOMATIC ASSIGNMENT AND SEQUENCING OF CO
CWAO67	APPLICATION OF	PARALLEL	PROCESSING TO NUMERICAL WEATHER PREDICTION.=APPLIC.
SJLP66	LARGE	PARALLEL	COMPUTERS.=
RMAP63	A	PARALLEL	COMPUTER ORGANIZATION AND MECHANIZATIONS.=
FGAM61	RESPONSES IN A	PARALLEL	SEARCH FILE.=A METHOD FOR RESOLVING MULTIPLE
FAAF62	ALGORITHMS FOR	PARALLEL	SEARCH MEMORIES.=ALGORI
FRAA65	AN ASSOCIATIVE	PARALLEL	PROCESSOR WITH APPLICATION TO PICTURE PROCESSING.=AN ASS
SLAL63	GIC FOR HIGHLY	PARALLEL	SYSTEMS.=ASSOCIATIVE LO
WDPN64		PARALLEL	NETWORK COMPUTER (SOLOMON).=
SWPC60		PARALLEL	COMPUTING WITH VERTICAL DATA.=
WDPN64		PARALLEL	NETWORK COMPUTER (SOLOMON).=
REPE69		PARALLELISM	EXPOSURE AND EXPLOITATION.=
DJPG68	NG GENERALITY,	PARALLELISM	AND COMPUTER ARCHITECTURE.=PROGRAMMI
BRPI68		PARALLELISM	IN COMPUTER PROGRAMS AND IN MACHINES.=
BBON62	OF THE SOLOMON	PARALLEL-PROCESSING	COMPUTER.=ON THE USE
KJAO63	PLICATION OF A	PARALLEL-SEARCH	MEMORY.=AP
KMPO66	OF A MODEL FOR	PARRALLEL	COMPUTATIONS: DETERMINACY, TERMINATION, QUEUEING.=PROPERTIES
BHPO62	N OF PARABOLIC	PARTIAL	DIFFERENTIAL EQUATIONS.=PROPERTIES OF A VARIABLE STRUCTURE COMPUTER SYSTEM IN
SDUS66	US	PATENT	NO.3287703.=
CBPF68		PATH	FINDING WITH ASSOCIATIVE MEMORY.=
HCMR61	OYING ONE FLUX	PATH	PER FILE ITEM.=MAGNETIC REALIZATIONS FOR MIRF EMPL
LCAA61	ALGORITHM FOR	PATH	CONNECTIONS AND ITS APPLICATIONS.=AN
VFMR61	ONE CONDUCTIVE	PATH	PER FILE ITEM.=MAGNETIC REALIZATION FOR MIRF EMPLOYING
ASAM67	ATION OF LEE'S	PATH	CONNECTION ALGORITHM.=A MODIFIC
SJPD64	SIMULATE THE	PATTERN	ARTICULATION UNIT OF ILLIAC-III.=PROGRAM DESCRIPTION OF PAX AN IBM 7090 PROGRA
SJUM64	SIMULATE THE	PATTERN	ARTICULATION UNIT OF ILLIAC-III.=USER'S MANUAL FOR PAX AN IBM 7090 PROGRAM TO
MDTL61	ALIZATION OF A	PATTERN	RECOGNITION COMPUTER.=TENTATIVE LOGICAL RE
MBDO	DESIGN OF A	PATTERN	RECOGNITION DIGITAL COMPUTER - PART 1 : GENERAL INTRODUCTION.=
MBTI63	THE ILLINOIS	PATTERN	RECOGNITION COMPUTER - ILLIAC-III.=
YYPR66		PATTERN	RECOGNITION USING AN ASSOCIATIVE MEMORY.=
YCPR66		PATTERN	RECOGNITION BY AN ASSOCIATIVE MEMORY.=
CCPR		PATTERN	RECOGNITION PROCESS FOR BUBBLE CHAMBER PICTURES.=
USPD59		PATTERN	DETECTION AND RECOGNITION.=
KKDT68	IAGNOSTIC TEST	PATTERNS	AND SEQUENCES FOR ILLIAC-IV PROCESSING ELEMENT.=D
SJPD64	DESCRIPTION OF	PAX	AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=
SJUM64	R'S MANUAL FOR	PAX	AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=

BRTP69	THE	PAX-2	PICTURE PROCESSING SYSTEM AT THE UNIVERSITY OF ILLINOIS PROGRAMMING MANUAL.=
VVPO58		PENETRATION	OF MAGNETIC FIELDS THROUGH THIN SUPERCONDUCTING FILMS.=
FSGO62	AN ELEMENTARY	PERCEIVING	AND MEMORIZING MACHINE.=GENERALIZATION OF
HMTM60	THE MARK I	PERCEPTION	- DESIGN AND PERFORMANCE.=
NGSA63	THE TOBERMORY	PERCEPTION	=SYSTEM AND CIRCUIT DESIGNS FOR
HJBP64	BIAX	PERCEPTRON	=
KMEO67	TER SYSTEMS TO	PERFORM	PARALLEL PROCESSING.=EVOLUTION OF COMPU
HMTM60	N - DESIGN AND	PERFORMANCE	=THE MARK I PERCEPTIO
BHAM62	A MACHINE FOR	PERFORMING	VISUAL RECOGNITION BY USE OF ANTENNA PROPAGATION CONCEPTS.=
KPTR63	PE MEMORY - A	PERMANENT	STORAGE DEVICE.=THE RO
SCTP65	THE	PERSISTATRON	UTILIZING A SUPERCONDUCTIVE GROUND PLANE.=
SOTR68	EMORY CELL - A	PERSISTOTRON	- IN A MEMORY MATRIX. =THE RELIABILITY OF OPERATING A SUPERCONDUCTING M
BBCR64	ACCESS MEMORY,	PHASE	2 10 (9) BIT MEMORY.=CRYOELECTRIC RANDOM
BLCR65	ACCESS MEMORY,	PHASE	3.=CRYOELECTRIC RANDOM
BACR66	CCESS MEMORY -	PHASE	3.=CRYOELECTRIC RANDOM A
CHPP69	PROCESSING FOR	PHASED-ARRAY	RADARS.=PARALLEL
NKPM65		PHENOMENOLOGICAL	MODEL FOR THE BIAX.=
SPPA62		PHYSICAL	AND LOGICAL DESIGN OF A HIGHLY PARALLEL COMPUTER.=
HIAA64	RE FOR NUCLEAR	PHYSICS	=AN ASSOCIATIVE STO
HIGS64	GE FOR NUCLEAR	PHYSICS	=GENERAL SURVEY : ASSOCIATIVE STORA
BCAM67	IES IN NUCLEAR	PHYSICS	=ASSOCIATIVE MEMOR
GPAI66	SS SYSTEM : A	PHYSICS	LIBRARY CATALOG.=AUTOMATIC INTRODUCTION OF INFORMATION INTO A REMOTE-ACCE
BRTP69	THE PAX-2	PICTURE	PROCESSING SYSTEM AT THE UNIVERSITY OF ILLINOIS PROGRAMMING MANUAL.=
YCAM66	PPLICATIONS TO	PICTURE	AND ARITHMETIC PROCESSES.=ASSOCIATIVE MEMORY SYSTEMS AND THEIR A
FBAA65	ATION TO	PICTURE	PROCESSING.=AN ASSOCIATIVE PARALLEL PROCESSOR WITH APPLIC
NRAP64	SSING OF	PICTURES	=A PROGRAMMING LANGUAGE FOR THE PARALLEL PROCE
CCPR	BUBBLE CHAMBER	PICTURES	=PATTERN RECOGNITION PROCESS FOR
SHAP69	A	PIPELINE	PUSH-DOWN STACK COMPUTER.=
SCTP65	DUCTIVE GROUND	PLANE	=THE PERSISTATRON UTILIZING A SUPERCON
RLCM65	OGENICS MEMORY	PLANE	INTERCONNECTION TECHNIQUES.=CRY
RGCA64	TIVE PROCESSOR	PLANE	TEST AND EVALUATION.=CRYOGENIC ASSOCIA
BSCS65	LECTRIC MEMORY	PLANES	=CAVITY SENSING OF CRYOE
PUFA65	IVE PROCESSOR	PLANES	=FABRICATION AND TESTING OF CRYOGENIC ASSOCIAT
BGAM69	ROCESSOR USING	PLATED	WIRE.=A MISSION ORIENTED ASSOCIATIVE P
CWPW67		PLATED	WIRE CONTENT-ADDRESSABLE MEMORIES WITH BIT-STEERING TECHNIQUE.=
CSPW67		PLATED	WIRE BIT STEERING FOR LOGIC AND STORAGE.=
DPPW64		PLATED	WIRE MAGNETIC FILM MEMORIES.=
FTAP65	A WOVEN	PLATED-WIRE	ASSOCIATED MEMORY.=
FKTP64	THE	PLATED-WOVEN	WIRE MEMORY MATRIX.=
DGAA66	TA HANDLING IN	PL/I	=APL - A LANGUAGE FOR ASSOCIATIVE DA
SAAS68	STRUCTURE FOR	PL/1	=AUXILIARY STORAGE ASSOCIATIVE DATA
SSAM63	HE PROGRAMMING	POINT	OF VIEW.=ASSOCIATIVE MEMORY COMPUTERS FROM T
SAAD64	FROM A DEVICE	POINT	OF VIEW.=A DISCUSSION OF ASSOCIATIVE MEMORIES
PFAI69	IELD-CONTROLLED	POLARIZATION-TRANSFER	DEVICE AND THE OPERATING FEATURES OF THE EXPLORATORY CONTENT ADDRESSABLE M
GGAP66	A	POSSIBLE	MODEL OF A NETWORK PROCESSING ASSOCIATIVE MEMORY=
RJCM62	TER MEMORIES -	POSSIBLE	FUTURE DEVELOPMENTS.=COMPU
SSSO64	OF PRESENT AND	POTENTIAL	SEARCH MEMORY - IMPLEMENTATION AND TECHNIQUES.=SURVEY
NVCA65	CHIEVEMENT AND	POTENTIAL	=CRYOGENICS - A
CWAO67	AL WEATHER	PREDICTION	=APPLICATION OF PARALLEL PROCESSING TO NUMERIC
VNPF67		PREDICTIONS	FOR FUTURE OF CRYOGENIC APPLICATIONS.=
LMAS66	F PROBLEMS AND	PRELIMINARY	RESULTS CONCERNING PARALLEL PROCESSING AND PARALLEL PROCESSORS.=A SURVEY O
SJAT64	PUTER - SECOND	PRELIMINARY	VERSION.=AT-1 PARALLEL COM
GRPS63		PRELIMINARY	SYSTEM SEARCH TIME ANALYSIS.=
BUPP66		PRELIMINARY	PROGRAMMING MANUAL FOR RADC 2048 WORD ASSOCIATIVE MEMORY.=
SBTS63	N COMPUTER - A	PRELIMINARY	REPORT.=THE SOLOMO
BWPA69		PREPARATION	AND EVALUATION OF COMPUTER PROGRAMS FOR PARALLEL PROCESSING SYSTEMS.=
HLPA66		PRESENT	AND FUTURE STATE-OF-THE-ART IN COMPUTER MEMORIES.=

SSSO64	SURVEY OF	PRESENT	AND POTENTIAL SEARCH MEMORY - IMPLEMENTATION AND TECHNIQUES.=
RJMI65	MEMORIES IN	PRESENT	AND FUTURE GENERATIONS OF COMPUTERS.=
SGAN60	A NEW	PRINCIPLE	FOR THE CONSTRUCTION OF A MEMORY DEVICE.=
FCDO68	TERMINATION OF	PRIORITY	IN ASSOCIATIVE MEMORIES.=DE
KAAO69	DEFENSE RADAR	PROBLEM	=APPLICATION OF ILLIAC-IV TO URBAN
PNMC66	MAN-COMPUTER	PROBLEM	SOLVING WITH MULTILIST.=
CCAO	PON ASSIGNMENT	PROBLEM	OF NTDS.=APPLICATION OF ASSOCIATIVE MEMORIES TO THE WEA
RDSO68	THE DIRICHLET	PROBLEM	ON A SIMULATED PARALLEL PROCESSING SYSTEM.=SOLUTION OF
WRAP65	A	PROBLEM	SOLVING FACILITY.=
KAAO68	DEFENSE RADAR	PROBLEM	=APPLICATION OF ILLIAC-IV TO URBAN
PUAS65	FOR REAL-TIME	PROBLEM	SOLVING.=A STORAGE AND RETRIEVAL SYSTEM
MRPC69	IC DESIGN	PROBLEMS	=PARALLEL COMPUTING STRUCTURES AND ALGORITHMS FOR LOG
DSAT71	A MANAGEMENT	PROBLEMS	=ASSOCIATIVE TECHNIQUES IN THE SOLUTION OF DAT
LMAS66	A SURVEY OF	PROBLEMS	AND PRELIMINARY RESULTS CONCERNING PARALLEL PROCESSING AND PARALLEL PROCESSORS
KMSP64	SOME	PROBLEMS	IN INFORMATION SCIENCE WITH EMPHASIS ON ADAPTATION TO USE THROUGH MAN-MACHINE
AETF61	IMIZATION	PROBLEMS	=THE FIXED-PLUS-VARIABLE COMPUTER SYSTEM IN DYNAMIC PROGRAMMING FORMULATION OF
USAC58	IENTED TOWARDS	PROBLEMS	=A COMPUTER OR
SEAA61	TIC SEQUENCING	PROCEDURE	WITH APPLICATION TO PARALLEL PROGRAMMING.=AN AUTOMA
KGTL	TABLE LOOKUP	PROCEDURES	IN DATA PROCESSING.=
BKP163		PROCEEDINGS	1962 WORKSHOP ON COMPUTER ORGANIZATION.=
SAPO59		PROCEEDINGS	OF THE INTERNATIONAL SYMPOSIUM ON THE THEORY OF SWITCHING, APRIL, 1957.=
SJDL69	Y COMPUTER FOR	PROCESS	CONTROL=DISTRIBUTED LOGIC MEMOR
CCPR	RN RECOGNITION	PROCESS	FOR BUBBLE CHAMBER PICTURES.=PATTE
GRRA69	ON OF PARALLEL	PROCESSABLE	STREAMS IN COMPUTER PROGRAMS.=RECOGNITION AND REPRESENTATI
BMAA69	FOR PARALLEL	PROCESSES	=ANALYSIS AND SYNTHESIS OF CONTROL MECHANISMS
YCAM66	AND ARITHMETIC	PROCESSES	=ASSOCIATIVE MEMORY SYSTEMS AND THEIR APPLICATIONS TO PICTURE
SHAP69	ASSOCIATIVE	PROCESSING	FOR GENERAL PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES.=
AKSS69	SEISMIC SIGNAL	PROCESSING	VIA THE ILLIAC-IV COMPUTER.=SEISMI
PJPD68	PARALLEL DATA	PROCESSING	VIA CRYOELECTRICS.=
BKSA68	IST	PROCESSING	LANGUAGE=STUDY OF A COMPUTER FOR DIRECT EXECUTION OF L
DRTI69	THE ILLIAC-IV	PROCESSING	ELEMENT.=
SDAP71	ASSOCIATIVE	PROCESSING	OF LINE DRAWINGS=
FRAL67	ATIVE PARALLEL	PROCESSING	=ACHIEVING LARGE SCALE COMPUTING CAPABILITIES THROUGH ASSOCI
BLAR70	A RING	PROCESSING	PACKAGE FOR USE WITH FORTRAN OR A SIMILAR HIGH LEVEL LANGUAGE=
SWOP69	ORTHOGONAL	PROCESSING	=
RSIB69	I AND PARALLEL	PROCESSING	=INTERACTION BETWEEN LS
BRPA69	S FOR PARALLEL	PROCESSING	SYSTEMS.=PREPARATION AND EVALUATION OF COMPUTER PROGRAM
DRTI69	THE ILLIAC-IV	PROCESSING	ELEMENT.=
BRTP69	PAX-2 PICTURE	PROCESSING	SYSTEM AT THE UNIVERSITY OF ILLINOIS PROGRAMMING MANUAL.=THE
EJIP70	INTERRUPT	PROCESSING	WITH QUEUED CONTENT-ADDRESSABLE MEMORIES=
FNOA67	Y AND PARALLEL	PROCESSING	=ON A COMPUTER LANGUAGE WHICH SIMULATES ASSOCIATIVE MEMOR
WMAP69	ATIVE PARALLEL	PROCESSING	FOR THE FAST FOURIER TRANSFORM.=ASSOCI
LMAS66	G PARALLEL	PROCESSING	AND PARALLEL PROCESSORS.=A SURVEY OF PROBLEMS AND PRELIMINARY RESULTS CONCERNI
MYDS68	FOR ILLIAC-IV	PROCESSING	ELEMENT.=DIAGNOSTIC SEQUENCE GENERATOR
BRAA69	E SONAR SIGNAL	PROCESSING	=AN ASSOCIATIVE MEMORY PARALLEL DELTIC REALIZATION FOR ACTIV
KMEO67	RFORM PARALLEL	PROCESSING	=EVOLUTION OF COMPUTER SYSTEMS TO PE
BEAE63	SS OF PARALLEL	PROCESSING	=AN EVALUATION OF THE EFFECTIVENE
NRAP64	R THE PARALLEL	PROCESSING	OF PICTURES.=A PROGRAMMING LANGUAGE FO
GJAA69	RADAR DATA	PROCESSING	=AN ASSOCIATIVE, HIGHLY-PARALLEL COMPUTER FOR
KMRP67	IN ASSOCIATIVE	PROCESSING	=RADC PROGRAMS
CHPP69	PARALLEL	PROCESSING	FOR PHASED-ARRAY RADARS.=
GGAP66	L OF A NETWORK	PROCESSING	ASSOCIATIVE MEMORY=A POSSIBLE MODE
LDGL69	YPNIR : A LIST	PROCESSING	LANGUAGE FOR ILLIAC-IV.=GL
FNUM	ALLEL	PROCESSING	LANGUAGE, AMPPL-II.=USER'S MANUAL FOR THE ASSOCIATIVE MEMORY, PAR
GPAP65	ASSOCIATIVE	PROCESSING	TECHNIQUES.=
RPAA67	AN ASSOCIATIVE	PROCESSING	SYSTEM FOR CONVENTIONAL DIGITAL COMPUTERS=AN ASS
GHOT	ST INFORMATION	PROCESSING	SYSTEM=ON THE DESIGN OF A MULTI-LI

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KGTL        EDURES IN DATA    PROCESSING    =TABLE LOOKUP PROC
FCAM61      NCE DATA          PROCESSING    =ASSOCIATIVE MEMORY APPLICATIONS FOR INTFLLIGE
BSLS68      LE INFORMATION    PROCESSING    SYSTEMS : MODEL BUILDING, SIMULATION AND EVALUATION.=LARGE SCA
AJPS65      S FOR PARALLEL    PROCESSING    =PROGRAM STRUCTURE
HAAP63      OF ASSOCIATIVE    PROCESSING     TECHNIQUES.=A PROPOSAL FOR THE STUDY
HSAP60      MATIC PARALLEL    PROCESSING    =AUTO
GVRO64      DOCUMENT          PROCESSING    =REQUIREMENTS OF FUTURE COMPUTER MEMORIES FOR
LSAP65         ASSOCIATIVE    PROCESSING    TECHNIQUES STUDY.=
EBPP63            PARALLEL    PROCESSING    IN A RESTRUCTURABLE COMPUTER SYSTEM.=
GJAI63      ALLY ADDRESSED    PROCESSING    SYSTEM.=AN INTRINSIC
MJLI62            LISP 1.5    PROCESSING    MANUAL.=
BAAO66      S FOR PARALLEL    PROCESSING    =ANALYSIS OF PROGRAM
GJTF62      ED INFORMATION    PROCESSING    SYSTEM.=TECHNIQUES FOR ADVANC
MJHP66      EL INFORMATION    PROCESSING    SYSTEMS, =HIGHLY PARALL
I8AP63         ASSOCIATIVE    PROCESSING    TECHNIQUES.=
LSAP66      ATIVE PARALLEL    PROCESSING    AS APPLIED TO MULTI-PREFORMED BEAM SONAR SYSTEMS.=ASSOCI
FRAP67      ATIVE PARALLEL    PROCESSING    =ASSOCI
FJLP67               LIST     PROCESSING    =
BCSO66      OF ASSOCIATIVE    PROCESSING    TECHNIQUES.=STUDY
CGLP68               LIST     PROCESSING    RESEARCH TECHNIQUES.=
DGTS64      NE INFORMATION    PROCESSING    SYSTEMS.=THE STRUCTURE OF ON-LI
BRCL64       COMPUTER LIST    PROCESSING    LANGUAGES.=
PJAA65      CH TO PARALLEL    PROCESSING    =AN APPROA
RDSO68      TED PARALLEL      PROCESSING    SYSTEM.=SOLUTION OF THE DIRICHLET PROBLEM ON A SIMULA
BCSO66      OF ASSOCIATIVE    PROCESSING    TECHNIQUES.=STUDY
FBSO65      OF ASSOCIATIVE    PROCESSING    TECHNIQUES.=STUDY
CGAT61      UP MACHINE FOR    PROCESSING    NATURAL LANGUAGES.=A TABLE LOOK-
CJLP67               LIST     PROCESSING    RESEARCH TECHNIQUES.=
KMAM62      AL ' CONCEPT '    PROCESSING     =ADAPTIVE MECHANISMS IN DIGIT
FRMO67      ATIVE PARALLEL    PROCESSING    =MACHINE ORGANIZATION IN ASSOCI
FRAP67      ATIVE PARALLEL    PROCESSING    =ASSOCI
FRAL        TIVE  PARALLEL    PROCESSING    =ACHIEVING LARGE COMPUTING CAPABILITIES THROUGH ASSOCIA
FJAO65      OF ASSOCIATIVE    PROCESSING    =ASPECTS
FJAM61      CE DATA           PROCESSING    =ASSOCIATIVE MEMORY APPLICATIONS IN INTELLIGEN
MSAM63      LEMENTARY LIST    PROCESSING     COMPUTER.=A MEMORY ORGANIZATION FOR AN E
KKDT68      LIAC-IV           PROCESSING    ELEMENT.=DIAGNOSTIC TEST PATTERNS AND SEQUENCES FOR IL
KMPP66            PARALLEL    PROCESSING    COMPUTER SYSTEM.=
RGLD64       LANGUAGE DATA    PROCESSING    WITH SEARCH MEMORIES.=
PSAA67      TRACT PARALLEL    PROCESSING    SYSTEM.=AN ARS
SMMO64      AL ASSOCIATION    PROCESSING    =MEMORY ORGANIZATION OF A 7090 TO DO STATISTIC
WDMP64            MULTIPLE    PROCESSING    TECHNIQUES.=
RFAA67      AN ASSOCIATIVE    PROCESSING    SYSTEM FOR CONVENTIONAL DIGITAL COMPUTERS.=AN ASS
SHAP68         ASSOCIATIVE    PROCESSING    FOR GENERAL PURPOSE COMPUTERS THROUGH THE USE OF MODIFIED MEMORIES.=
BRAC64      ARISON OF LIST    PROCESSING    LANGUAGES.=A COMP
CWAO67      ON OF PARALLEL    PROCESSING    TO NUMERICAL WEATHER PREDICTION.=APPLICATI
NAIP61         INFORMATION    PROCESSING    LANGUAGE - V MANUAL.=
AMIP62         INFORMATION    PROCESSING    BY DATA INTERROGATION.=
SSCO65      TION FOR ARRAY    PROCESSING    =COMPUTER ORGANIZA
NIAI60      TO INFORMATION    PROCESSING    LANGUAGE - V.=AN INTRODUCTION
CGBP65               BULK     PROCESSING    IN DISTRIBUTED LOGIC MEMORY.=
FBAA65            PICTURE     PROCESSING    =AN ASSOCIATIVE PARALLEL PROCESSOR WITH APPLICATION TO
GHAF60      -COMPILED LIST    PROCESSING    LANGUAGE.=A FORTRAN
HHCS68       A TIME-SHARED    PROCESSOR     =CONTROL STORAGE USE IN IMPLEMENTING AN ASSOCIATIVE MEMORY FOR
HTPP70            PARALLEL    PROCESSOR     SYSTEMS, TECHNOLOGIES, AND APPLICATIONS=
LGTA69       ASSOCIATIVE      PROCESSOR     =THE ARCHITECTURE OF A LARGE DISTRIBUTED LOGIC
ASII65      OGRAM PARALLEL    PROCESSOR     =INVESTIGATIONS INTO THE THEORY OF AN INTERACTIVE CIRCUIT STORED PR
LHTA69      AN ASSOCIATIVE    PROCESSOR     USING BULK STORAGE.=THE ASP - DYNABIT SYSTEM :
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LRAU68	IATION-STORING	PROCESSOR	INTERPRETER PROGRAM.=ASP USERS MANUAL . ASSOC
SPAF69	EL ASSOCIATIVE	PROCESSOR	=A FAST, FLEXIBLE HIGHLY PARALL
RJTA69	HE ASSOCIATIVE	PROCESSOR	- A NEW COMPUTER RESOURCE=T
LGTA70	GE ASSOCIATIVE	PROCESSOR	=THE ARCHITECTURE OF A LAR
ASTA69	VE ASSOCIATIVE	PROCESSOR	WITH DEDUCTIVE CAPABILITIES=TRAMP: AN INTERPRETI
FPAM69	RUCTION STREAM	PROCESSOR	WITH SHARED RESOURCES.=A MULTIPLE INST
PJFA66	C ASSOCIATIVE	PROCESSOR	=FABRICATION AND TESTING OF 5000 WORD CRYOGENI
RRAS69	IATION STORING	PROCESSOR	INTERPRETIVE PROGRAM - PROGRAM LOGIC MANUAL.=ASSOC
FTTS68	ED ASSOCIATIVE	PROCESSOR	=THE STRUCTURE OF A HIGH-SPE
PWDO65	CRYOGENIC DATA	PROCESSOR	=DESIGN OF A FULLY ASSOCIATIVE
BGAM69	ED ASSOCIATIVE	PROCESSOR	USING PLATED WIRE.=A MISSION ORIENT
GAS069	OF ASSOCIATIVE	PROCESSOR	IN AWACS.=STUDY OF MISSION EFFECTIVENESS
MWTA68	HE ASSOCIATIVE	PROCESSOR	IN AIRCRAFT CONFLICT DETECTION.=T
FTAA67	AN ASSOCIATIVE	PROCESSOR	=AN ASS
FTAA69	AN ASSOCIATIVE	PROCESSOR	=AN ASS
FTAA67	AN ASSOCIATIVE	PROCESSOR	=AN ASS
FBAP64	ASSOCIATIVE	PROCESSOR	STUDY.=
HTS069	EY OF PARALLEL	PROCESSOR	APPROACHES AND TECHNIQUES.=SURV
SLAS68	IATION STORING	PROCESSOR	INTERPRETIVE PROGRAM - PROGRAM LOGIC MANUAL.=ASSOC
NRIL65	ILLIAC-III: A	PROCESSOR	OF VISUAL INFORMATION.=
WES062	RALLEL NETWORK	PROCESSOR	=SOLOMON PA
INAP64	ASSOCIATIVE	PROCESSOR	STUDY FOR RADC.=
IRAP64	ASSOCIATIVE	PROCESSOR	=
CYAP67	NON-NUMERICAL	PROCESSOR	=A PROGRAMMING STUDY OF A
KAAA68	AN ASSOCIATION	PROCESSOR	FOR INFORMATION RETRIEVAL.=AN ASS
FRAP64	ASSOCIATIVE	PROCESSOR	STUDY.=
DGAS66	E MEMORY	PROCESSOR	=A STUDY OF THE UTILITY OF A HYBRID ASSOCIATIV
FSAP64	ASSOCIATIVE	PROCESSOR	STUDY.=
WJSL63	SYMMETRIC LIST	PROCESSOR	=SYMMET
SLAS67	IATION STORING	PROCESSOR	=ASSOC
PJFA65	IC ASSOCIATIVE	PROCESSOR	PLANES.=FABRICATION AND TESTING OF CRYOGEN
JHS068	ED ASSOCIATIVE	PROCESSOR	TECHNIQUES INTERIM REPORT.=STUDY OF ADVANC
MDTA66	S ON PARALLEL	PROCESSOR	SYSTEMS.=THE AUTOMATIC ASSIGNMENT AND SEQUENCING OF COMPUTATION
SLAS66	IATIVE-STORING	PROCESSOR	STUDY.=ASSOC
SLAS66	IATION-STORING	PROCESSOR	STUDY.=ASSOC
SLAS68	IATION-STORING	PROCESSOR	INTERPRETER PROGRAM.=ASP USER'S MANUAL ASSOC
PWDO64	CRYOGENIC DATA	PROCESSOR	=DESIGN OF A FULLY ASSOCIATIVE
FBAA65	ATIVE PARALLEL	PROCESSOR	WITH APPLICATION TO PICTURE PROCESSING.=AN ASSOCI
EDAA64	AN ASSOCIATIVE	PROCESSOR	=AN ASS
RGCA64	IC ASSOCIATIVE	PROCESSOR	PLANE TEST AND EVALUATION.=CRYOGEN
SLAS67	IATIVE STORING	PROCESSOR	=ASSOC
PJFA67	C ASSOCIATIVE	PROCESSOR	=FABRICATION AND TESTING OF 5000 WORD CRYOGENI
BRCA63	IC ASSOCIATIVE	PROCESSOR	=CRYOGEN
BRS064	IC ASSOCIATIVE	PROCESSOR	=STRUCTURE OF A CRYOGEN
RMSI66	KS ON PARALLEL	PROCESSORS	=SCHEDULING INDEPENDENT TAS
LMAS66	G AND PARALLEL	PROCESSORS	=A SURVEY OF PROBLEMS AND PRELIMINARY RESULTS CONCERNING PARALLEL PROCESSIN
EETU67	OF ASSOCIATIVE	PROCESSORS	IN RADAR TRACKING AND CORRELATION.=THE USE
YYAN66	OR ASSOCIATIVE	PROCESSORS	=A NONBULK ADDITION TECHNIQUE F
CJOA67	FILE	PROCESSORS	=ORGANIZATION AND APPLICATIONS OF ASSOCIATIVE
DPAP64	ASSOCIATIVE	PROCESSORS	=
SWAM63	FOR LARGE DATA	PROCESSORS	=ASSOCIATIVE MEMORY TECHNIQUES
RJAC67	G FOR PARALLEL	PROCESSORS	=A CASE STUDY IN PROGRAMMIN
ASII65	CUIT STORED	PROGRAM	PARALLEL PROCESSOR.=INVESTIGATIONS INTO THE THEORY OF AN INTERACTIVE CIR
LRAU68	INTERPRETER	PROGRAM	=ASP USERS MANUAL . ASSOCIATION-STORING PROCESSOR
RRAS69	R INTERPRETIVE	PROGRAM	- PROGRAM LOGIC MANUAL.=ASSOCIATION STORING PROCESSO
RRAS69	TIVE PROGRAM -	PROGRAM	LOGIC MANUAL.=ASSOCIATION STORING PROCESSOR INTERPRE
SJPD64		PROGRAM	DESCRIPTION OF PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICULATION UN

SJPD64	AN IBM 7090	PROGRAM	TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=PROGRAM DESCRIPTION O
SJUM64	X AN IBM 7090	PROGRAM	TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=USER'S MANUAL FOR PA
SLAS68	R INTERPRETIVE	PROGRAM	- PROGRAM LOGIC MANUAL.=ASSOCIATION STORING PROCESSO
SIAS68	TIVE PROGRAM -	PROGRAM	LOGIC MANUAL.=ASSOCIATION STORING PROCESSOR INTERPRE
AJPS65		PROGRAM	STRUCTURES FOR PARALLEL PROCESSING.=
FAPS60		PROGRAM	SEQUENCE CONTROL IN A MULTIPROCESSING SYSTEM USING ASSOCIATIVE STORAGE.=
SLAS68	OR INTERPRETER	PROGRAM	=ASP USER'S MANUAL ASSOCIATION-STORING PROCESS
PSU066	TE FOR GENERAL	PROGRAMMABILITY	OF SEARCH MEMORIES.=USE OF MULTIWRI
SRAP61	A	PROGRAMMED	ASSOCIATIVE MEMORY FOR USE IN COMPILING.=
RPMP63	ASSOCIATIVE	PROGRAMMED	COMPUTER.=MULTIDIMENSIONAL PULSE-HEIGHT ANALYZER APPLICATION OF AN
KKAP66	A	PROGRAMMERS	DESCRIPTION OF L6.=
BRTP69	OF ILLINOIS	PROGRAMMING	MANUAL.=THE PAX-2 PICTURE PROCESSING SYSTEM AT THE UNIVERSITY
BCIL69	CTERISTICS AND	PROGRAMMING	MANUAL.=ILLIAC-IV SYSTEMS CHARA
DBAP67	- ASSOCIATIVE	PROGRAMMING	LANGUAGE USER'S MANUAL.=APL
RPAA68	AN AMBIT/G	PROGRAMMING	LANGUAGE IMPLEMENTATION.=
SBDR65	ASSOCIATIVE	PROGRAMMING	OF A SMALL COMPUTER.=DIRECT-RECORDING MEGACHANNEL ANALYZER THROUGH
SEAA61	PARALLEL	PROGRAMMING	=AN AUTOMATIC SEQUENCING PROCEDURE WITH APPLICATION TO
SBCA66	NT-ADDRESSABLE	PROGRAMMING	TECHNIQUES.=CONTE
NAOP60	ON	PROGRAMMING	A HIGHLY PARALLEL MACHINE TO BE AN INTELLIGENT TECHNICIAN.=
RHOT69	: A GRAPHICAL	PROGRAMMING	LANGUAGE.=ON THE IMPLEMENTATION OF AMBIT/G
KDIL68	ND APPLICATION	PROGRAMMING	=ILLIAC-IV SOFTWARE A
BCIL68	CTERISTICS AND	PROGRAMMING	MANUAL.=ILLIAC-IV : SYSTEMS CHARA
NRAP64	A	PROGRAMMING	LANGUAGE FOR THE PARALLEL PROCESSING OF PICTURES.=
CYAP67	A	PROGRAMMING	STUDY OF A NON-NUMERICAL PROCESSOR.=
MHCR68	OF THE DYNAMIC	PROGRAMMING	ALGORITHM, ANNUAL PROGRESS REPORT.=CELLULAR REALIZATION
BRTU68	VE MEMORIES IN	PROGRAMMING	THE GROWING MACHINE.=THE USE OF MULTIPLE ASSOCIATI
DJPG68		PROGRAMMING	GENERALITY, PARALLELISM AND COMPUTER ARCHITECTURE.=
BUPP66	PRELIMINARY	PROGRAMMING	MANUAL FOR RADC 2048 WORD ASSOCIATIVE MEMORY.=
RJAC67	CASE STUDY IN	PROGRAMMING	FOR PARALLEL PROCESSORS.=A
WDSA64	REQUIRED FOR	PROGRAMMING	THE PARALLEL NETWORK COMPUTER.=STUDY AND INVESTIGATION TO DEVELOP COMPILER TEC
CFLP68	LINEAR	PROGRAMMING	IMPLEMENTATION IN ILLIAC-IV. I : REVISED SIMPLEX METHOD.=
SPPA63		PROGRAMMING	AND DESIGN CONSIDERATIONS OF A HIGHLY PARALLEL COMPUTER.=
SSAM63	UTERS FROM THE	PROGRAMMING	POINT OF VIEW.=ASSOCIATIVE MEMORY COMP
APTL66	THE LISP 2	PROGRAMMING	LANGUAGE AND SYSTEM.=
AETF61	NAMIC	PROGRAMMING	FORMULATION OF CONTROL SYSTEM OPTIMIZATION PROBLEMS.=THE FIXED-PLUS-VARIABLE C
BRPA69	ON OF COMPUTER	PROGRAMS	FOR PARALLEL PROCESSING SYSTEMS.=PREPARATION AND EVALUATI
GRRA69	MS IN COMPUTER	PROGRAMS	=RECOGNITION AND REPRESENTATION OF PARALLEL PROCESSABLE STREA
BAAO66	ANALYSIS OF	PROGRAMS	FOR PARALLEL PROCESSING.=
KMRP67	RADC	PROGRAMS	IN ASSOCIATIVE PROCESSING.=
BRPI68	SM IN COMPUTER	PROGRAMS	AND IN MACHINES.=PARALLELI
MHCR68	RITHM, ANNUAL	PROGRESS	REPORT.=CELLULAR REALIZATION OF THE DYNAMIC PROGRAMMING ALGO
NWPR66		PROGRESS	REPORT ON THE NEBULA COMPUTER.=
IUQT67	ERLY TECHNICAL	PROGRESS	REPORT, APRIL, MAY, JUNE, 1967=QUART
IUQT65	ERLY TECHNICAL	PROGRESS	REPORT FOR OCTOBER, NOVEMBER, DECEMBER, 1965.=QUART
BCPR67		PROGRESS	REPORT ON THE NEBULA COMPUTER.=
IBLP60	LIGHTNING	PROJECT	=
WAAS68	A SIMPLE	PROOF	OF LEWIN'S ORDERED-RETRIEVAL THEOREM FOR ASSOCIATIVE MEMORIES.=
BHAM62	ANTENNA	PROPAGATION	CONCEPTS.=A MACHINE FOR PERFORMING VISUAL RECOGNITION BY USE OF
BHPO62		PROPERTIES	OF A VARIABLE STRUCTURE COMPUTER SYSTEM IN THE SOLUTION OF PARABOLIC PARTIAL D
EKPO67		PROPERTIES	OF CELLULAR ARRAYS FOR LOGIC AND STORAGE.=
SKES60	STIC SWITCHING	PROPERTIES	OF SOME SQUARE LOOP MATERIALS IN TOROIDAL STRUCTURES.=ELA
KMPO66		PROPERTIES	OF A MODEL FOR PARRALLEL COMPUTATIONS: DETERMINACY, TERMINATION, QUEUEING.=
SWSA63	AGE AND SEARCH	PROPERTIES	OF A TREE ORIENTED MEMORY SYSTEM.=STOR
SHGP68	GRAPH	PROPERTY	RECOGNITION MACHINES.=
RCAP64	A	PROPOSAL	FOR AN ASSOCIATIVE MEMORY USING MAGNETIC FILMS.=
IBAP62	A	PROPOSAL	FOR THE STUDY OF ADVANCED INFORMATION RETRIEVAL TECHNIQUES.=
HAAP63	A	PROPOSAL	FOR THE STUDY OF ASSOCIATIVE PROCESSING TECHNIQUES.=

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WHPF63                          PROPOSAL          FOR ORDERED SEQUENTIAL DETECTION OF SIMULTANEOUS MULTIPLE RESPONSES.=
CRAP64                    A     PROPOSAL          FOR AN ASSOCIATIVE MEMORY USING MAGNETIC FILMS.=
GWTP61                  THE     PROSPECTS         FOR THE UTILIZATION OF INFORMATIONAL-LOGICAL MACHINES IN CHEMISTRY.=
BBPO66                          PROSPECTS         OF A SPACE-BASED CRYOGENIC COMPUTER.=
RJIM65  S, RESULTS AND          PROSPECTS         =INTEGRATED MAGNETIC AND SUPERCONDUCTIVE MEMORIES : A SURVEY OF TECHNIQUE
GKAC67  OINCIDENT               PULSES            =A CONTINUOUS FILM MEMORY DRIVEN BY MULTIPLE C
RPMP63  LTIDIMENSIONAL          PULSE-HEIGHT      ANALYZER APPLICATION OF AN ASSOCIATIVE PROGRAMMED COMPUTER,=MU
SHAP69      A PIPELINE          PUSH-DOWN         STACK COMPUTER,=
HGQR67                          QUASI-RANDOM      ACCESS MEMORY SYSTEM,=
GRRO67   ON INTELLIGENT         QUESTION-ANSWERING SYSTEM,=RESEARCH
EJIP70  ROCESSING WITH          QUEUED            CONTENT-ADDRESSABLE MEMORIES=INTERRUPT P
KMPO66  , TERMINATION,          QUEUEING          =PROPERTIES OF A MODEL FOR PARRALLEL COMPUTATIONS: DETERMINACY
TGHT63          HOW TO          QUIZ              A WHOLE MEMORY AT ONCE,=
EETU67   PROCESSORS IN          RADAR             TRACKING AND CORRELATION,=THE USE OF ASSOCIATIVE
GJAA69  L COMPUTER FOR          RADAR             DATA PROCESSING,=AN ASSOCIATIVE, HIGHLY-PARALLE
KAAO69   URBAN DEFENSE          RADAR             PROBLEM,=APPLICATION OF ILLIAC-IV TO
KAAO68   URBAN DEFENSE          RADAR             PROBLEM,=APPLICATION OF ILLIAC-IV TO
CHPP69  R PHASED-ARRAY          RADARS            =PARALLEL PROCESSING FO
KMRP67                          RADC              PROGRAMS IN ASSOCIATIVE PROCESSING,=
INAP64  SSOR STUDY FOR          RADC              =ASSOCIATIVE PROCE
BDPP66  ING MANUAL FOR          RADC              2048 WORD ASSOCIATIVE MEMORY,=PRELIMINARY PROGRAMM
FRVT69  IABLE TOPOLOGY          RANDOM            ACCESS MEMORY ORGANIZATIONS,=VAR
FRVT69  IABLE TOPOLOGY          RANDOM            ACCESS MEMORY ORGANIZATIONS=VAR
NFCS67  RAGE CELLS FOR          RANDOM            ACCESS MEMORIES,=CRYOTRON STO
RRAA64  FOR CONCURRENT          RANDOM            WALKS ON HIGHLY PARALLEL MACHINES,=A ALGORITHM
BRCR64    CRYOELECTRIC          RANDOM            ACCESS MEMORY, PHASE 2 10 ( 9 ) BIT MEMORY,=
BICR65    CRYOELECTRIC          RANDOM            ACCESS MEMORY, PHASE 3,=
NDCS65  ET SENSING FOR          RANDOM            ACCESS MEMORIES,=CONTINUOUS SHE
BACR66    CRYOELECTRIC          RANDOM            ACCESS MEMORY - PHASE 3,=
ARTB65  Y CELL FOR              RANDOM-ACCESS     WORK-ORGANIZED MEMORIES,=THE BRIDGE CELL - A NEW SUPERCONDUCTIVE MEMOR
SLRA69                          RANGE             ASSOCIATIVE MEMORY WITH ORDERED RETRIEVAL,=
AJSO62       SEARCH ON          RANGE             ASSOCIATIVE MEMORY,=
BCCI62  O-MEMORY SPEED          RATIO             =CONSIDERATIONS IN THE DESIGN OF A COMPUTER WITH HIGH LOGIC-T
FHCC61  EMI-PERMANENT,          READ              ONLY MEMORY,=CARD CAPACITOR - A S
KMAH65  H-SPEED, WOVEN          READ              ONLY MEMORY,=A HIG
LMAS65     A SURVEY OF          READ              ONLY MEMORIES,=
GPNR67  NONDESTRUCTIVE          READOUT           ( NDRO ) FROM THIN MAGNETIC FILMS,=NONDES
NMCA65  GNETORESISTIVE          READOUT           OF MAGNETIC THIN FILMS,=CONTENT-ADDRESSED MEMORY USING MA
HWSM66   MEMORIES AND           READOUT           OF THE DETECTOR MATRIX,=SIMULTANEOUS MULTIPLE RESPONSE IN ASSOCIATIVE
IBAM65  CIATIVE MEMORY          READOUT           CIRCUIT,=ASSO
PGAR63            A             READ-ONLY         MULTI-MEGABIT PARALLEL SEARCH ASSOCIATIVE MEMORY,=
MAAT65  ON-DESTRUCTIVE          READ-OUT          TECHNIQUE,=A THIN MAGNETIC FILM COMPUTER MEMORY USING A REASONANT ABSORPTION N
BTAM71  I/O SYSTEM FOR          REAL              TIME COMPUTERS =A MULTIPLEXED
EVOO62  IGENVECTORS OF          REAL              SYMMETRIC MATRICES,=ORGANIZATION OF A ' FIXED-PLUS-VARIABLE ' STRUCTURE COMPUT
CRSA63       SHIEF: A           REALIZABLE        FORM OF ASSOCIATIVE MEMORY,=
BRAA69  ARALLEL DELTIC          REALIZATION       FOR ACTIVE SONAR SIGNAL PROCESSING,=AN ASSOCIATIVE MEMORY P
MRCR68       CELLULAR           REALIZATION       OF THE DYNAMIC PROGRAMMING ALGORITHM, ANNUAL PROGRESS REPORT,=
MDTL61  TATIVE LOGICAL          REALIZATION       OF A PATTERN RECOGNITION COMPUTER,=TEN
VEMR61       MAGNETIC           REALIZATION       FOR MIRF EMPLOYING ONE CONDUCTIVE PATH PER FILE ITEM,=
HCMR61       MAGNETIC           REALIZATIONS      FOR MIRF EMPLOYING ONE FLUX PATH PER FILE ITEM,=
PGTM63  IST SYSTEM FOR          REAL-TIME         STORAGE AND RETRIEVAL,=THE MULTI-L
HBSU64  VE MEMORY AS A          REAL-TIME         CONTROL,=SOME USES OF AN ASSOCIATI
PGTM62  SYSTEM FOR THE          REAL-TIME         SOFTWARE AND RETRIEVAL,=THE MULTI-LIST
PUAS65  VAL SYSTEM FOR          REAL-TIME         PROBLEM SOLVING,=A STORAGE AND RETRIE
MAAT65  MEMORY USING A          REASONANT          ABSORPTION NON-DESTRUCTIVE READ-OUT TECHNIQUE,=A THIN MAGNETIC FILM COMPUTER
BACR64    CRYOELECTRIC          RECEIVER          TECHNIQUES,=
YORD61                          RECENT            DEVELOPMENTS IN HIGH-SPEED SUPERCONDUCTING DEVICES,=
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BHAM62	FORMING VISUAL	RECOGNITION	BY USE OF ANTENNA PROPAGATION CONCEPTS.=A MACHINE FOR PER
SHGP68	GRAPH PROPERTY	RECOGNITION	MACHINES.=GRAPH
GRRA69		RECOGNITION	AND REPRESENTATION OF PARALLEL PROCESSABLE STREAMS IN COMPUTER PROGRAMS.=
MDTL61	N OF A PATTERN	RECOGNITION	COMPUTER.=TENTATIVE LOGICAL REALIZATIO
MBDO	N OF A PATTERN	RECOGNITION	DIGITAL COMPUTER - PART 1 : GENERAL INTRODUCTION.=DESIG
MRTI63	LINOIS PATTERN	RECOGNITION	COMPUTER - ILLIAC-III.=THE IL
YYPR66	PATTERN	RECOGNITION	USING AN ASSOCIATIVE MEMORY.=
YCPR66	PATTERN	RECOGNITION	BY AN ASSOCIATIVE MEMORY.=
CCPR	PATTERN	RECOGNITION	PROCESS FOR BUBBLE CHAMBER PICTURES.=
USPD69	DETECTION AND	RECOGNITION	=PATTERN
MRTS69	OGIC AND USAGE	RECORDER	=THE SYSTEM L
LAAA61	MEMORY TO	REDUCE	THE ACCESS TIME FOR INSTRUCTIONS IN LOOPS.=AN APPLICATION FOR A SMALL, FAST AS
MSUO64	AUTOMATIC DATA	REDUCTION	=USE OF STANDARD MEMORY SYSTEMS AS ASSOCIATIVE MEMORIES FOR INTEGRATING STORAG
GLRM69	(	REFERENCE	MANUAL FOR ILLIAC-IV ASSEMBLER ASK.=
EDMI68	AND ITERATIVE	REFINEMENT	=MATRIX INVERSION
RSHD69	ARDWARE DESIGN	REFLECTING	SOFTWARE REQUIREMENTS=H
ASTA67	TRAMP : A	RELATIONAL	MEMORY WITH AN ASSOCIATIVE BASE.=
SOTR68	THE	RELIABILITY	OF OPERATING A SUPERCONDUCTING MEMORY CELL - A PERSISTOTRON - IN A MEMORY MATR
GPAI66	RMATION INTO A	REMOTE-ACCESS	SYSTEM : A PHYSICS LIBRARY CATALOG.=AUTOMATIC INTRODUCTION OF INFO
JLOO61	AND STRUCTURE,	REPRESENTATION	STORAGE AND SEARCH.=ON OPER
GWRA69	ECOGNITION AND	REPRESENTATION	OF PARALLEL PROCESSABLE STREAMS IN COMPUTER PROGRAMS.=R
IBSS64	ANCE DATA BASE	REPRESENTATION	AS TEST VEHICLE.=SEA SURVEILL
KSTA64	ANIZATION OF A	REPRESENTATIVE	SEARCH MEMORY.=THEORY AND ORG
WDSA64	ECHNIQUES	REQUIRED	FOR PROGRAMMING THE PARALLEL NETWORK COMPUTER.=STUDY AND INVESTIGATION TO DEVE
MIRA68	E TECHNOLOGIES	REQUIRED	TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS.=RESEARCH AND DEVELOP
RSHD69	CTING SOFTWARE	REQUIREMENTS	=HARDWARE DESIGN REFLE
GVRO64		REQUIREMENTS	OF FUTURE COMPUTER MEMORIES FOR DOCUMENT PROCESSING.=.
GHAN61	ON THE SYSTEM	REQUIREMENTS	OF A DIGITAL COMPUTER FOR THE MANIPULATION OF LIST STRUCTURES.=A NOTE
IUCS66	MPUTER SYSTEMS	RESEARCH	=CO
RJRO63		RESEARCH	ON CRYOGENIC ASSOCIATIVE MEMORIES.=
RWRO64		RESEARCH	ON CRYOGENIC ASSOCIATIVE MEMORIES.=
RJRO63		RESEARCH	ON CRYOGENIC ASSOCIATIVE MEMORIES.=
FMOA69	L INTELLIGENCE	RESEARCH	: AN ASSOCIATIVE MEMORY, PARALLEL LANGUAGE, AMPPL-II.=ON A NEW TOOL IN ARTIFIC
RJRO63		RESEARCH	ON CRYOGENIC ASSOCIATIVE MEMORIES.=
ABAS64	TAL TECHNOLOGY	RESEARCH	=ANNUAL SUMMARY REPORT OF INVESTIGATION IN DIGI
NHRO64		RESEARCH	ON LOW TEMPERATURE COMPUTING ELEMENTS.=
EGDT64	TAL TECHNOLOGY	RESEARCH	=DIGI
CGLP68	IST PROCESSING	RESEARCH	TECHNIQUES.=L
CJRO64		RESEARCH	ON FERRET ASSOCIATIVE MEMORY.=
CJLP67	IST PROCESSING	RESEARCH	TECHNIQUES.=L
NHCR66	CRYOGENIC	RESEARCH	=
SHRO63		RESEARCH	ON BIAX TYPE ELEMENTS AND ASSOCIATED CIRCUITS.=
GRRO67		RESEARCH	ON INTELLIGENT QUESTION-ANSWERING SYSTEM.=
RJCA64	CIATIVE MEMORY	RESEARCH	=CRYOGENIC ASSO
RJCR64	CRYOTRON	RESEARCH	=
MRSO67	MICROCELLULAR	RESEARCH	=SURVEY OF
MTRA68		RESEARCH	AND DEVELOPMENT OF THE TECHNOLOGIES REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH
LBFR65	FIXED	RESISTOR-CARD	MEMORY.=
FGAM61	A METHOD FOR	RESOLVING	MULTIPLE RESPONSES IN A PARALLEL SEARCH FILE.=
MHRM64		RESOLVING	MULTIPLE RESPONSES IN AN ASSOCIATIVE MEMORY.=
RJTA69	A NEW COMPUTER	RESOURCE	=THE ASSOCIATIVE PROCESSOR -
FPAM69	SHARED	RESOURCES	=A MULTIPLE INSTRUCTION STREAM PROCESSOR WITH
GMAC60	INSTANTANEOUS	RESPONSE	FILE.=A CRYOGENIC MULTIPLE
YHDO64	INSTANTANEOUS	RESPONSE	FILE : THE AN/GSQ-81 DOCUMENT DATA INDEXING SET.=DEVELOPMENT OF A MULTIPLE
HWSM66	NEOUS MULTIPLE	RESPONSE	IN ASSOCIATIVE MEMORIES AND READOUT OF THE DETECTOR MATRIX.=SIMULTA
FRAA64	INSTANTANEOUS	RESPONSE	FILE.=AN ANALYSIS OF THE MULTIPLE
GGMI61	INSTANTANEOUS	RESPONSE	FILE.=MULTIPLE

YHDO64	INSTANTANEOUS	RESPONSE	FILE.=DESIGN OF AN EXPERIMENTAL MULTIPLE
NJMI61	INSTANTANEOUS	RESPONSE	FILE).=MIRF (MULTIPLE
MHRM64	LVING MULTIPLE	RESPONSES	IN AN ASSOCIATIVE MEMORY.=RESO
WHPF63	OUS MULTIPLE	RESPONSES	=PROPOSAL FOR ORDERED SEQUENTIAL DETECTION OF SIMULTANE
FGAM61	LVING MULTIPLE	RESPONSES	IN A PARALLEL SEARCH FILE.=A METHOD FOR RESO
TKAT61	G BIAS	RESTORATION	=A TOROIDAL NONDESTRUCTIVE MEMORY ELEMENT USIN
ERPP63	ROCESSING IN A	RESTRUCTURABLE	COMPUTER SYSTEM.=PARALLEL P
LMAS66	ND PRELIMINARY	RESULTS	CONCERNING PARALLEL PROCESSING AND PARALLEL PROCESSORS.=A SURVEY OF PROBLEMS A
RJIM65	OF TECHNIQUES,	RESULTS	AND PROSPECTS.=INTEGRATED MAGNETIC AND SUPERCONDUCTIVE MEMORIES : A SURVEY
HJIC65	AND	RESUME	=ITERATIVE, CIRCUIT COMPUTERS CHARACTERIZATION
YYAC66	OR INFORMATION	RETRIEVAL	=A CRYOGENIC ASSOCIATIVE MEMORY F
LPAC64	TO INFORMATION	RETRIEVAL	=A CONTENT ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH APPLICATIONS
PGTM63	ME STORAGE AND	RETRIEVAL	=THE MULTI-LIST SYSTEM FOR REAL-TI
SLRA69	Y WITH ORDERED	RETRIEVAL	=RANGE ASSOCIATIVE MEMOR
HAST63	MATION	RETRIEVAL	=SOME THEORIZING ON MEMORY STRUCTURE AND INFOR
JMOO64	ON ORDERED	RETRIEVAL	FROM AN ASSOCIATIVE MEMORY.=
MTCA60	OF INFORMATION	RETRIEVAL	=COMBINATORIAL ASPECTS
KAAA68	OR INFORMATION	RETRIEVAL	=AN ASSOCIATION PROCESSOR F
MJTS64	AN INFORMATION	RETRIEVAL	SYSTEM.=THE SEARCH MEMORY IN
IBAP62	ED INFORMATION	RETRIEVAL	TECHNIQUES.=A PROPOSAL FOR THE STUDY OF ADVANC
LWAM	OR INFORMATION	RETRIEVAL	SYSTEMS.=A MULTIPLE FILE ORGANIZATION F
GYOR65	ORDERED	RETRIEVAL	OF A MULTI-COMPONENT ANSWER FROM ASSOCIATIVE MEMORY.=
WAED64	ON AND ORDERED	RETRIEVAL	IN SEARCH MEMORIES.=EXTREME DETERMINATI
CVOR67	ORDERED	RETRIEVAL	FROM A DECIMAL ASSOCIATIVE MEMORY.=
GGLF62	OR INFORMATION	RETRIEVAL	BASED ON SIMULTANEOUS INTERROGATION OF ALL ITEMS.=LARGE FILES F
GHLF61	OR INFORMATION	RETRIEVAL	BASED ON SIMULTANEOUS INTERROGATION OF ALL ITEMS.=LARGE FILES F
FERO61		RETRIEVAL	OF INFORMATION WITH AN ASSOCIATIVE MEMORY.=
ACTC65	NFORMATION	RETRIEVAL	=TOWARDS CONTROLLED EXPERIMENTS IN THE CONSTRUCTION OF AN ADAPTIVE MAN-MACHINE
OJSF63	IMPLIFIED DATA	RETRIEVAL	AND DISPLAY DEVICES.=SWITCHING FUNCTIONS FOR S
SEAC64	TO INFORMATION	RETRIEVAL	=A CONTENT-ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH APPLICATIONS
PHCA62	ND INFORMATION	RETRIEVAL	=CONTENT ADDRESSING A
GMAO66	TA STORAGE AND	RETRIEVAL	SYSTEMS.=ANALYSIS OF SMALL ASSOCIATIVE MEMORIES FOR DA
PGTM62	ARE AND	RETRIEVAL	=THE MULTI-LIST SYSTEM FOR THE REAL-TIME SOFTW
SLAM62	Y WITH ORDERED	RETRIEVAL	=ASSOCIATIVE MEMOR
RDAM65	ND INFORMATION	RETRIEVAL	=ASSOCIATIVE MEMORIES A
RFST64	ON STORAGE,	RETRIEVAL	AND COMMUNICATION SYSTEM CONTROL.=STUDY TO DETERMINE THE APPLICABILITY OF THE
SRSA65	STORAGE AND	RETRIEVAL	OF ASPECTS OF MEANING IN DIRECTED GRAPH STRUCTURES.=
PUAS65	A STORAGE AND	RETRIEVAL	SYSTEM FOR REAL-TIME PROBLEM SOLVING.=
YYAC66	ORMATION	RETRIEVAL	=A CRYOGENIC ASSOCIATIVE MEMORY SYSTEM FOR INF
LPAC63	TO INFORMATION	RETRIEVAL	=A CONTENT ADDRESSABLE DISTRIBUTED LOGIC MEMORY WITH APPLICATION
GMAO66	TA STORAGE AND	RETRIEVAL	SYSTEMS.=ANALYSIS OF SMALL ASSOCIATIVE MEMORIES FOR DA
LMRO62		RETRIEVAL	OF ORDERED LISTS FROM A CONTENT ADDRESSED MEMORY.=
HLRA63		REVIEW	AND SURVEY OF MASS MEMORIES.=
WBCA63	ON CIRCUITS, A	REVIEW	=CRYOTRONS AND CRYOTR
SRAS60	SORTING MEMORY	REVISED	=ASSOCIATIVE SELF=
CFLP68	ILLIAC-IV. I :	REVISED	SIMPLEX METHOD.=LINEAR PROGRAMMING IMPLEMENTATION IN
BLAR70	A	RING	PROCESSING PACKAGE FOR USE WITH FORTRAN OR A SIMILAR HIGH LEVEL LANGUAGE=
LGAS68	ASP - A	RING	IMPLEMENTED ASSOCIATIVE STRUCTURE PACKAGE.=
WTCA68	NCEPT BASED ON	RINGS	=CYLINDERS-A DATA STRUCTURE CO
CATK62	EMORY WORKS AT	ROOM	TEMPERATURE.=3-K BIT ASSOCIATIVE M
KPTR63	THE	ROPE	MEMORY - A PERMANENT STORAGE DEVICE.=
WDHS64	CH IN A LARGE,	ROTATING	MASS MEMORY.=HIGH-SPEED, CONTENT SEAR
WLAS70	RY USING LARGE	SCALE	INTEGRATION =AN ASSOCIATIVE MEMO
FWAL67	CHIEVING LARGE	SCALE	COMPUTING CAPABILITIES THROUGH ASSOCIATIVE PARALLEL PROCESSING=A
YDDO61	IGN OF A LARGE	SCALE	CRYOGENIC MEMORY.=DES
BSLS68	LARGE	SCALE	INFORMATION PROCESSING SYSTEMS : MODEL BUILDING, SIMULATION AND EVALUATION.=
EKLS63	LARGE	SCALE	COMPUTING SYSTEMS OF THE FUTURE.=

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RMSI66                          SCHEDULING      INDEPENDENT TASKS ON PARALLEL PROCESSORS.=
HTPC68      PAGE-CONTROL        SCHEMES         IN A MULTIPROCESSOR WITH ASSOCIATIVE CONTROL.=
KWSP64    IN INFORMATION        SCIENCE         WITH EMPHASIS ON ADAPTATION TO USE THROUGH MAN-MACHINE INTERACTION.=SOME PROBL
MPAD69    T COMPUTER FOR        SCIENTIFIC      CALCULATIONS=A DESIGN FOR A FAS
WPST66                          SCIENTIFIC      TECHNICAL INFORMATION NO. 6, 1964 : SELECTED ARTICLES.=
NAAN62     ION THE USE OF       SCRAMBLED       ADDRESSING FOR ASSOCIATIVE MEMORIES.=A NOTE
IBSS64                          SEA             SURVEILLANCE DATA BASE REPRESENTATION AS TEST VEHICLE.=
JLOO61    N, STORAGE AND        SEARCH          =ON OPERAND STRUCTURE, REPRESENTATIO
FAAF62    S FOR PARALLEL        SEARCH          MEMORIES.=ALGORITHM
JKTT62    ELATION WITH A        SEARCH          MEMORY.=TARGET TRACK CORR
HGIT64    NTRODUCTION TO        SEARCH          MEMORIES.=I
MJTS64              THE         SEARCH          MEMORY IN AN INFORMATION RETRIEVAL SYSTEM.=
KSTA64    REPRESENTATIVE        SEARCH          MEMORY.=THEORY AND ORGANIZATION OF A
HRIT63    NTEGRATING THE        SEARCH          MEMORY WITH THE USQ-20 COMPUTER.=I
IBSO63    NS OF PARALLEL        SEARCH          MEMORIES.=STUDY OF THE APPLICATIO
GRPS63    IMINARY SYSTEM        SEARCH          TIME ANALYSIS.=PREL
BLAT63    M FOR SORTING,        SEARCH          AND MAINTENANCE.=A TREE STRUCTURE SYSTE
WAED64    D RETRIEVAL IN        SEARCH           MEMORIES.=EXTREME DETERMINATION AND ORDERE
GAAO63    NS OF PARALLEL        SEARCH          MEMORIES.=APPLICATIO
WDHS64    SPEED, CONTENT        SEARCH          IN A LARGE, ROTATING, MASS MEMORY.=HIGH-
SDSD64    EM DESIGN OF A        SEARCH          MEMORY.=SYST
RGLD64    ROCESSING WITH        SEARCH          MEMORIES.=LANGUAGE DATA P
SSSO64     AND POTENTIAL        SEARCH          MEMORY - IMPLEMENTATION AND TECHNIQUES.=SURVEY OF PRESENT
PGAR63    GABIT PARALLEL        SEARCH          ASSOCIATIVE MEMORY.=A READ-ONLY MULTI-ME
RHTW68       2-1/2D CORE        SEARCH          MEMORY.=
AJSO62                          SEARCH          ON RANGE ASSOCIATIVE MEMORY.=
SWSA63       STORAGE AND        SEARCH          PROPERTIES OF A TREE ORIENTED MEMORY SYSTEM.=
KAAS63                A         SEARCH          MEMORY SUBSYSTEM FOR A GENERAL PURPOSE COMPUTER.=
RBAT63    300 NANOSECOND        SEARCH          MEMORY.=A
PSUO66    RAMMABILITY OF        SEARCH           MEMORIES.=USE OF MULTIWRITE FOR GENERAL PROG
FGAM61    A PARALLEL            SEARCH          FILE.=A METHOD FOR RESOLVING MULTIPLE RESPONSES IN
FAAF62    S FOR PARALLEL        SEARCH          MEMORIES.=ALGORITHM
GRAH64    RPOSE COMPUTER        SEARCH           MEMORY.=A HARDWARE INTEGRATED GENERAL PU
SRAS67       ASSOCIATIVE        SEARCH          MEMORY STUDY.=
RJAF64    MS FOR COMPLEX        SEARCHES        =ALGORITH
ACAM68    : SUBSTRUCTURE        SEARCHING        AND DATA ORGANIZATION.=ASSOCIATIVE MEMORY INVESTIGATIONS
KRMA62      MEMORY ARRAY        SEARCHING       SYSTEM.=
AKSS69                          SEISMIC         SIGNAL PROCESSING VIA THE ILLIAC-IV COMPUTER.=
CCAM65    ION AND               SELECTED        NAVAL APPLICATIONS.=ASSOCIATIVE MEMORY COMPUTER SYSTEM : DESCRIPT
WPST66     NO. 6, 1964 :        SELECTED         ARTICLES.=SCIENTIFIC TECHNICAL INFORMATION
HPAM65    ESCRIPTION AND        SELECTED        NAVAL APPLICATIONS.=ASSOCIATIVE MEMORY COMPUTER SYSTEM D
RTMO67        METHODS OF        SELECTING       A MULTIVALENT ANSWER FROM ASSOCIATIVE MEMORY.=
BGAL66    SSOCIATED LIST        SELECTOR         =A
GBAL66    SOCIATIVE LIST        SELECTOR        =AS
SRAS60       ASSOCIATIVE        SELF-SORTING    MEMORY REVISED.=
SRAS60       ASSOCIATIVE        SELF-SORTING    MEMORY.=
BRAS62                A         SEMANTICALLY    ASSOCIATIVE MEMORY. =
PGAS64                A         SEMIPERMANENT   MEMORY UTILIZING CORRELATION ADDRESSING.=
WTSA60                          SEMI-ANNUAL     REPORT ON DIGITAL COMPUTER SYSTEMS STUDIES.=
LFSC63                          SEMI-CONDUCTOR  CIRCUITS IN ASSOCIATIVE MEMORIES.=
MYSP61                          SEMI-PERMANENT  STORAGE BY CAPACITIVE COUPLING.=
BJAS61                A         SEMI-PERMANENT  MAGNETIC ASSOCIATIVE MEMORY AND CODE CONVERTER.=
FHCC61     CAPACITOR - A        SEMI-PERMANENT   READ ONLY MEMORY.=CARD
STSP65                          SEMI-PERMANENT  ASSOCIATIVE STORE.=
BSCS65          CAVITY          SENSING         OF CRYOELECTRIC MEMORY PLANES.=
NDCS65    NTINUOUS SHEET        SENSING         FOR RANDOM ACCESS MEMORIES.=CO
BCAL63    RY WITH CAVITY        SENSING         =A LARGE CAPACITY CRYOELECTRIC MEMO
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NYDS68          DIAGNOSTIC      SEQUENCE        GENERATOR FOR ILLIAC-IV PROCESSING ELEMENT.=
FAPS60             PROGRAM      SEQUENCE        CONTROL IN A MULTIPROCESSING SYSTEM USING ASSOCIATIVE STORAGE.=
KKDT68  T PATTERNS AND          SEQUENCES       FOR ILLIAC-IV PROCESSING ELEMENT.=DIAGNOSTIC TES
SFAA61    AN AUTOMATIC          SEQUENCING      PROCEDURE WITH APPLICATION TO PARALLEL PROGRAMMING.=
MDTA66  ASSIGNMENT AND          SEQUENCING      OF COMPUTATIONS ON PARALLEL PROCESSOR SYSTEMS.=THE AUTOMATIC
WHPF63  AL FOR ORDERED          SEQUENTIAL      DETECTION OF SIMULTANEOUS MULTIPLE RESPONSES.=PROPOS
SWAS68                A         SEQUENTIALLY    HOMING CONTENT-ADDRESSED MEMORY MODEL.=
EPAP67  R BASED ON THE          SEQUENTIALLY     OPERATING MACHINE ' GAMMA-BARABAN '.=A PARALLEL MACHINE SIMULATO
RWSA67                          SERIAL          ASSOCIATIVE MEMORIES.=
SDSS65             SPECIAL      SESSION         ON PARALLEL AND CONCURRENT COMPUTER SYSTEMS=
YHDO64   DATA INDEXING          SET             =DEVELOPMENT OF A MULTIPLE INSTANTANEOUS RESPONSE FILE : THE AN/GSQ-81 DOCUMEN
BHAT67  RS OF                   SHAPES          =A TRANSFORMATION FOR EXTRACTING NEW DESCRIPTO
FPAM69  PROCESSOR WITH          SHARED           RESOURCES.=A MULTIPLE INSTRUCTION STREAM
BLCS60      CONTINUOUS          SHEET           SUPERCONDUCTING MEMORY.=
NDCS65      CONTINUOUS          SHEET           SENSING FOR RANDOM ACCESS MEMORIES.=
CHSA63                          SHIEF            A REALIZABLE FORM OF ASSOCIATIVE MEMORY.=
BHIL65   ILLIAC-II - A          SHORT           DESCRIPTION AND ANNOTATED BIBLIOGRAPHY.=
AKSS69             SEISMIC      SIGNAL          PROCESSING VIA THE ILLIAC-IV COMPUTER.=
BKAA69  R ACTIVE SONAR          SIGNAL          PROCESSING.=AN ASSOCIATIVE MEMORY PARALLEL DELTIC REALIZATION FO
BKSO69                          SILICON-ON-SAPPHIRE COMPLEMENTARY MOS CIRCUITS FOR HIGH SPEED ASSOCIATIVE MEMORY=
BLAR70  N OR A                  SIMILAR         HIGH LEVEL LANGUAGE=A RING PROCESSING PACKAGE FOR USE WITH FORTRA
WAAS68                A         SIMPLE          PROOF OF LEWIN'S ORDERED-RETRIEVAL THEOREM FOR ASSOCIATIVE MEMORIES.=
CFLP68  V. I : REVISED          SIMPLEX         METHOD.=LINEAR PROGRAMMING IMPLEMENTATION IN ILLIAC-I
OJSF63   FUNCTIONS FOR          SIMPLIFIED      DATA RETRIEVAL AND DISPLAY DEVICES.=SWITCHING
OWLA    OK AHEAD LOGIC          SIMPLIFIED      =LO
SJPD64  GRAM TO                 SIMULATE        THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=PROGRAM DESCRIPTION OF PAX AN IBM
SJUM64  090 PROGRAM TO          SIMULATE        THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=USER'S MANUAL FOR PAX AN IBM 7
RDSO68  T PROBLEM ON A          SIMULATED       PARALLEL PROCESSING SYSTEM.=SOLUTION OF THE DIRICHLE
FNOA67  LANGUAGE WHICH          SIMULATES       ASSOCIATIVE MEMORY AND PARALLEL PROCESSING=ON A COMPUTER
BSLS68       BUILDING.          SIMULATION      AND EVALUATION.=LARGE SCALE INFORMATION PROCESSING SYSTEMS : MODEL
SDAP67  ACH TO DIGITAL          SIMULATION      =A PARALLEL COMPUTING APPRO
GGAT67  ULTI-PROCESSOR          SIMULATION      INVESTIGATION.=ASSOCIATIVE TECHNIQUES FOR CONTROL FUNCTIONS IN A M
WGAT68         A TIMING         SIMULATOR       OF ILLIAC-IV.=
EPAP67  RALLEL MACHINE          SIMULATOR       BASED ON THE SEQUENTIALLY OPERATING MACHINE ' GAMMA-BARABAN '.=A PA
HWSM66                          SIMULTANEOUS    MULTIPLE RESPONSE IN ASSOCIATIVE MEMORIES AND READOUT OF THE DETECTOR MATRIX.=
GHLF61  IEVAL BASED ON          SIMULTANEOUS    INTERROGATION OF ALL ITEMS.=LARGE FILES FOR INFORMATION RETR
GGLF62  IEVAL BASED ON          SIMULTANEOUS    INTEROGATION OF ALL ITEMS.=LARGE FILES FOR INFORMATION RETR
GJBT60   TWO TERMINAL,          SIMULTANEOUS    ACTION.=BINARY TESTS FOR
WHPF63  L DETECTION OF          SIMULTANEOUS     MULTIPLE RESPONSES.=PROPOSAL FOR ORDERED SEQUENTIA
HJAU69  F SUB-PROGRAMS          SIMULTANEOUSLY  =A UNIVERSAL COMPUTER, CAPABLE OF EXECUTING AN ARBITRARY NUMBER O
SISA63                          SKETCHPAD        A MAN-MACHINE GRAPHICAL COMMUNICATION SYSTEM.=
SRDR65  OGRAMMING OF A          SMALL           COMPUTER.=DIRECT-RECORDING MEGACHANNEL ANALYZER THROUGH ASSOCIATIVE PR
KASC67                          SMALL           CAPACITY THIN CYLINDRICAL MAGNETIC FILM STORAGE SYSTEMS.=
LAAA61  LICATION FOR A          SMALL            FAST ASSOCIATIVE MEMORY TO REDUCE THE ACCESS TIME FOR INSTRUCTIONS IN LOOPS.=
GMAO66     ANALYSIS OF          SMALL           ASSOCIATIVE MEMORIES FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=
GMAO66     ANALYSIS OF          SMALL           ASSOCIATIVE MEMORIES FOR DATA STORAGE AND RETRIEVAL SYSTEMS.=
FGSN64                          SNOBOL          : A STRING MANIPULATION LANGUAGE.=
RSHD69  IGN REFLECTING          SOFTWARE        REQUIREMENTS=HARDWARE DES
NRSS69             SOME         SOFTWARE        CONSIDERATIONS IN UTILIZATION OF A NETWORK OF COMPUTERS.=
KDIL68       ILLIAC-IV          SOFTWARE        AND APPLICATION PROGRAMMING.=
PGTM62   THE REAL-TIME          SOFTWARE        AND RETRIEVAL.=THE MULTI-LIST SYSTEM FOR
RPAI66  N INTO PAGING A         SOFTWARE-SIMULATED ASSOCIATIVE MEMORY SYSTEM.=AN INVESTIGATIO
LESS63                          SOLID           STATE ASSOCIATIVE CELLS.=
MKES67      ELECTRONIC          SOLID           STATE COMPONENTS. PART 4.=
GMTS63             THE          SOLOMON         COMPUTER.=
WESO62                          SOLOMON         PARALLEL NETWORK PROCESSOR.=
CGTS65             THE          SOLOMON         2 COMPUTING SYSTEM.=
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RFST64  ABILITY OF THE     SOLOMON          COMPUTER TO COMMAND AND CONTROL. VOLUME I. INFORMATION STORAGE, RETRIEVAL AND
SBTS62            THE      SOLOMON          COMPUTER.=
SBTS63            THE      SOLOMON          COMPUTER - A PRELIMINARY REPORT.=
RFST64  ABILITY OF THE     SOLOMON          COMPUTER TO COMMAND AND CONTROL.=STUDY TO DETERMINE THE APPLIC
WDPN64  ORK COMPUTER (     SOLOMON          ) APPLICATIONS ANALYSES.=PARALLEL NETW
WDPN64  ORK COMPUTER (     SOLOMON          ).=PARALLEL NETW
WDPN64  ORK COMPUTER (     SOLOMON          ).=PARALLEL NETW
GMTS63            THE      SOLOMON          COMPUTER.=
BBON62  THE USE OF THE     SOLOMON          PARALLEL-PROCESSING COMPUTER.=ON
DSAT71  HNIQUES IN THE     SOLUTION         OF DATA MANAGEMENT PROBLEMS=ASSOCIATIVE TEC
BBP062  YSTEM IN THE       SOLUTION         OF PARABOLIC PARTIAL DIFFERENTIAL EQUATIONS.=PROPERTIES OF A VARIABLE STRUCTUR
RDS068                     SOLUTION         OF THE DIRICHLET PROBLEM ON A SIMULATED PARALLEL PROCESSING SYSTEM.=
BED061  PUTER FOR THE      SOLUTION         OF A DIFFUSION EQUATION.=DESIGN OF A FIXED-PLUS-VARIABLE STRUCTURE COM
PNMC66  MPUTER PROBLEM     SOLVING          WITH MULTILIST.=MAN-CO
PHAS65  PROBLEM            SOLVING          =A STORAGE AND RETRIEVAL SYSTEM FOR REAL-TIME
WRAP65       A PROBLEM     SOLVING          FACILITY.=
BRAA69  ION FOR ACTIVE     SONAR            SIGNAL PROCESSING.=AN ASSOCIATIVE MEMORY PARALLEL DELTIC REALIZAT
LSAP66  PREFORMED BEAM     SONAR            SYSTEMS.=ASSOCIATIVE PARALLEL PROCESSING AS APPLIED TO MULTI-
ISSB56                     SORTING          BY ADDRESS CALCULATION.=
BLAT63  URE SYSTEM FOR     SORTING           SEARCH AND MAINTENANCE.=A TREE STRUCT
BRBC66  C COMPUTERS IN     SPACE            =RASING CRYOGENI
GHSM66                     SPACEBORNE       MEMORY ORGANIZATION.=
BBP066  PROSPECTS OF A     SPACE-BASED      CRYOGENIC COMPUTER.=PROSPE
NYSM68                     SPARSE           MATRIX INVERSION ON ILLIAC-IV.=
ISSM68                     SPARSE           MATRIX MULTIPLICATION.=
SDSS65                     SPECIAL          SESSION ON PARALLEL AND CONCURRENT COMPUTER SYSTEMS=
FMLA62  AND FUNCTIONAL     SPECIFICATION    OF AN ASSOCIATIVE MEMORY.=LOGICAL
BRSO69            HIGH     SPEED            ASSOCIATIVE MEMORY=SILICON-ON-SAPPHIRE COMPLEMENTARY MOS CIRCUITS FOR
AFBI65  BILOC - A HIGH     SPEED            NDRO ONE CORE PER BIT ASSOCIATIVE ELEMENT.=BILOC
BCCI62  OGIC-TO-MEMORY     SPEED            RATIO.=CONSIDERATIONS IN THE DESIGN OF A COMPUTER WITH HIGH L
CRIO63   THE OPERATING     SPEED            OF SUPERCONDUCTING COMPUTER ELEMENTS.=INFLUENCE OF THERMAL EFFECTS ON
ARCO65  ALCULATIONS OF     SPEED            OF LADDER NETWORK FOR SUPER-CONDUCTIVE ASSOCIATIVE MEMORIES.=C
SKES60  ERTIES OF SOME     SQUARE           LOOP MATERIALS IN TOROIDAL STRUCTURES.=ELASTIC SWITCHING PROP
SHAP69  LINE PUSH-DOWN     STACK            COMPUTER.=A PIPE
NSU064          USE OF     STANDARD         MEMORY SYSTEMS AS ASSOCIATIVE MEMORIES FOR INTEGRATING STORAGE OF MULTIPARAMET
LESS63            SOLID    STATE            ASSOCIATIVE CELLS.=
NKES67  ECTRONIC SOLID     STATE            COMPONENTS, PART 4.=FL
HIPA66  ENT AND FUTURE     STATE-OF-THE-ART IN COMPUTER MEMORIES.=PRES
RJCM61   SURVEY OF THE     STATE-OF-THE-ART =COMPUTER MEMORIES - A
SMMO64  F A 7090 TO DO     STATISTICAL      ASSOCIATION PROCESSING.=MEMORY ORGANIZATION O
CSPW67  LATED WIRE BIT     STEERING         FOR LOGIC AND STORAGE.=P
CAOT68   TO THE NAVIER     STOKES           EQUATIONS.=ON THE CONVERGENCE OF DISCRETE APPROXIMATIONS
PAAC70  ITIES FOR MASS     STORAGE          THROUGH ARRAY ORGANIZATION=ASSOCIATIVE CAPABIL
LHTA69  OR USING  BULK     STORAGE          =THE ASP - DYNABIT SYSTEM : AN ASSOCIATIVE PROCESS
SAAS68       AUXILIARY     STORAGE          ASSOCIATIVE DATA STRUCTURE FOR PL/1=
KKAI69  ED ASSOCIATIVE     STORAGE          SYSTEM =AN INTEGRAT
SASS62  E SWITCHES AND     STORAGE          DEVICES.=SUPERCONDUCTIV
PGTM63   FOR REAL-TIME     STORAGE          AND RETRIEVAL.=THE MULTI-LIST SYSTEM
JL0061  EPRESENTATION,     STORAGE          AND SEARCH.=ON OPERAND STRUCTURE, R
HHCS68         CONTROL     STORAGE          USE IN IMPLEMENTING AN ASSOCIATIVE MEMORY FOR A TIME-SHARED PROCESSOR.=
NFCS67        CRYOTRON     STORAGE          CELLS FOR RANDOM ACCESS MEMORIES.=
MSFI61  GITAL COMPUTER     STORAGE          AND ACCESS TECHNIQUES.=FUNDAMENTAL INVESTIGATION OF DI
NSU064  R  INTEGRATING     STORAGE          OF MULTIPARAMETER DATA BY AUTOMATIC DATA REDUCTION.=USE OF STANDARD MEMORY SYS
NYSA69                     STORAGE          ALLOCATION ALGORITHMS IN THE TRANQUIL COMPILER.=
NYSP61  SEMI-PERMANENT     STORAGE          BY CAPACITIVE COUPLING.=SEMI-P
NHIO62  VESTIGATION OF     STORAGE          AND ACCESS TECHNIQUES SUITABLE FOR USE IN LARGE-CAPACITY DIGITAL MEMORIES. =IN
HIGS64   : ASSOCIATIVE     STORAGE          FOR NUCLEAR PHYSICS.=GENERAL SURVEY
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KASC67          MAGNETIC FILM     STORAGE          SYSTEMS.=SMALL CAPACITY THIN CYLINDRICAL
FAPS60        G  ASSOCIATIVE      STORAGE         =PROGRAM SEQUENCE CONTROL IN A MULTIPROCESSING SYSTEM USIN
BPAS61           ASSOCIATIVE      STORAGE         TECHNIQUES.=
EKPO67          FOR LOGIC AND     STORAGE         =PROPERTIES OF CELLULAR ARRAYS
CSPW67          FOR LOGIC AND     STORAGE         =PLATED WIRE BIT STEERING
CYAO65        RY FOR DYNAMIC      STORAGE         ALLOCATION.=APPLICATION OF CONTENT-ADDRESSED MEMO
RFST64        .  INFORMATION      STORAGE          RETRIEVAL AND COMMUNICATION SYSTEM CONTROL.=STUDY TO DETERMINE THE APPLICABIL
SRSA65                            STORAGE         AND RETRIEVAL OF ASPECTS OF MEANING IN DIRECTED GRAPH STRUCTURES.=
GMAO66        ORIES FOR DATA      STORAGE         AND RETRIEVAL SYSTEMS.=ANALYSIS OF SMALL ASSOCIATIVE MEM
PUAS65                  A         STORAGE         AND RETRIEVAL SYSTEM FOR REAL-TIME PROBLEM SOLVING.=
HMCS60            CRYOTRON        STORAGE          ARITHMETIC AND LOGICAL CIRCUITS.=
KEOL62          ONE-LEVEL         STORAGE         SYSTEM.=
KPTR63        -  A PERMANENT      STORAGE         DEVICE.=THE ROPE MEMORY
GMAO66        ORIES FOR DATA      STORAGE         AND RETRIEVAL SYSTEMS.=ANALYSIS OF SMALL ASSOCIATIVE MEM
SWSA63                            STORAGE         AND SEARCH PROPERTIES OF A TREE ORIENTED MEMORY SYSTEM.=
BKDO65        NIZATION FOR A      STORAGE         SYSTEM.=DIRECTORY ORGA
RMAM62         THE ONE LEVEL      STORE           =ASSOCIATIVE MEMORIES AND
HIAA64        AN ASSOCIATIVE      STORE           FOR NUCLEAR PHYSICS.=AN ASS
LAAA63        OCIATIVE LOCAL      STORE           =AN ASS
JSTD62        NETIC FILM          STORE           =THE DESIGN OF A 4096 WORD ONE MICROSECOND MAG
STSP65        NT ASSOCIATIVE      STORE           =SEMI-PERMANE
TPAS67           ASSOCIATIVE      STORE           =
GMEA65        ONTINUOUS FILM      STORE           =EXPERIMENTAL AND THEORETICAL ASPECTS OF THE SUPERCONDUCTING C
ASII65        IVE CIRCUIT         STORED          PROGRAM PARALLEL PROCESSOR.=INVESTIGATIONS INTO THE THEORY OF AN INTERACT
BHAO66        TENT-ADDRESSED      STORES          =ASSOCIATIVE OR CON
RRAS69           ASSOCIATION      STORING         PROCESSOR INTERPRETIVE PROGRAM - PROGRAM LOGIC MANUAL.=
SLAS68           ASSOCIATION      STORING         PROCESSOR INTERPRETIVE PROGRAM - PROGRAM LOGIC MANUAL.=
SLAS67           ASSOCIATION      STORING         PROCESSOR.=
SLAS67           ASSOCIATIVE      STORING         PROCESSOR.=
HFTA68        HE ANALYSIS OF      STRATEGIES      FOR PAGING A LARGE ASSOCIATIVE DATA STRUCTURE.=T
WDCA68        COMPUTER-AIDED      STRATEGY        DESIGN USING ADAPTIVE AND ASSOCIATIVE TECHNIQUES.=COMPUT
LPAS63             AUTOMATIC      STRATIFICATION  OF INFORMATION.=
FPAM69        LE INSTRUCTION      STREAM          PROCESSOR WITH SHARED RESOURCES.=A MULTIP
GRRA69        OCESSABLE           STREAMS         IN COMPUTER PROGRAMS.=RECOGNITION AND REPRESENTATION OF PARALLEL PR
FGSN64            SNOBOL : A      STRING          MANIPULATION LANGUAGE.=
RFTL68        GUAGE AND DATA      STRUCTURE       =THE LEAP LAN
SAAS68        SOCIATIVE DATA      STRUCTURE       FOR PL/1=AUXILIARY STORAGE AS
WICA68        LINDERS-A DATA      STRUCTURE       CONCEPT BASED ON RINGS=CY
FITS68                   THE      STRUCTURE       OF A HIGH-SPEED ASSOCIATIVE PROCESSOR.=
JLO061            ON OPERAND      STRUCTURE        REPRESENTATION, STORAGE AND SEARCH.=
HAST63        ZING ON MEMORY      STRUCTURE       AND INFORMATION RETRIEVAL.=SOME THEORI
LGAS68        ED ASSOCIATIVE      STRUCTURE       PACKAGE.=ASP - A RING IMPLEMENT
HFTA68        CIATIVE   DATA      STRUCTURE       =THE ANALYSIS OF STRATEGIES FOR PAGING A LARGE ASSO
MBAM65        CIATIVE MEMORY      STRUCTURE       =ASSO
LPAE65        -DIRECTED DATA      STRUCTURE       LANGUAGE.=AN EXPERIMENTAL SYNTAX
RFTL68        GUAGE AND DATA      STRUCTURE       =THE LEAP LAN
GJCD67         COMPOUND DATA      STRUCTURE       FOR COMPUTER AIDED DESIGN : A SURVEY.=
BLAT63               A TREE       STRUCTURE       SYSTEM FOR SORTING, SEARCH AND MAINTENANCE.=
OGTS64                  THE       STRUCTURE       OF ON-LINE INFORMATION PROCESSING SYSTEMS.=
CFLA62             VARIABLE       STRUCTURE       DIGITAL COMPUTER.=LOGARITHMIC AND EXPONENTIAL FUNCTION EVALUATION IN A
BEDO61        -PLUS-VARIABLE      STRUCTURE       COMPUTER FOR THE SOLUTION OF A DIFFUSION EQUATION.=DESIGN OF A FIXED
EGVS64             VARIABLE       STRUCTURE       COMPUTER SYSTEM.=
BBPO62         OF A VARIABLE      STRUCTURE       COMPUTER SYSTEM IN THE SOLUTION OF PARABOLIC PARTIAL DIFFERENTIAL EQUATIONS.=P
TRAO63         OF A VARIABLE      STRUCTURE       COMPUTER.=ASSIGNMENT OF INVENTORY
BRSO64                            STRUCTURE       OF A CRYOGENIC ASSOCIATIVE PROCESSOR.=
EVDO62        LUS-VARIABLE '      STRUCTURE        COMPUTER FOR COMPUTATION OF EIGENVALUES AND EIGENVECTORS OF REAL SYMMETRIC MA
EGDO60        PLUS VARIABLE       STRUCTURE       COMPUTER.=ORGANIZATION OF COMPUTER SYSTEMS - THE FIXED
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SJAI68	AN ITERATIVELY	STRUCTURED	GENERAL-PURPOSE DIGITAL COMPUTER=AN ITE
HHSL69		STRUCTURED	LOGIC=
SJAO68	AN ITERATIVELY	STRUCTURED	GENERAL-PURPOSE DIGITAL COMPUTER=ASYNCHRONOUS OPERATION OF
SJAI66	AN ITERATIVELY	STRUCTURED	DIGITAL COMPUTER.=AN ITE
MRPC69	LLEL COMPUTING	STRUCTURES	AND ALGORITHMS FOR LOGIC DESIGN PROBLEMS=PARA
AJPS65	PROGRAM	STRUCTURES	FOR PARALLEL PROCESSING.=
GHAN61	LATION OF LIST	STRUCTURES	=A NOTE ON THE SYSTEM REQUIREMENTS OF A DIGITAL COMPUTER FOR THE MANIPU
SKES60	S IN TOROIDAL	STRUCTURES	=ELASTIC SWITCHING PROPERTIES OF SOME SQUARE LOOP MATERIAL
SRSA65	CTED GRAPH	STRUCTURES	=STORAGE AND RETRIEVAL OF ASPECTS OF MEANING IN DIRE
WISA60	MPUTER SYSTEMS	STUDIES	=SEMI-ANNUAL REPORT ON DIGITAL CO
LICL66	CRYOTRON LOGIC	STUDIES	=CRYOTR
BKSA68		STUDY	OF A COMPUTER FOR DIRECT EXECUTION OF LIST PROCESSING LANGUAGE=
LFAS69	A	STUDY	OF LOOK-ASIDE MEMORY.=
TRFS61	FEASIBILITY	STUDY	FOR A CRYOGENIC ASSOCIATIVE MEMORY.=
FRAP64	TIVE PROCESSOR	STUDY	=ASSOCIA
KNTL62	TABLE LOOKUP	STUDY	MODEL.=
GASO69		STUDY	OF MISSION EFFECTIVENESS OF ASSOCIATIVE PROCESSOR IN AWACS.=
HAAP63	OPOSAL FOR THE	STUDY	OF ASSOCIATIVE PROCESSING TECHNIQUES.=A PR
INAP64	TIVE PROCESSOR	STUDY	FOR RADC.=ASSOCIA
JKMC63	UTER INTERFACE	STUDY	=MAN-COMP
IRAP62	OPOSAL FOR THE	STUDY	OF ADVANCED INFORMATION RETRIEVAL TECHNIQUES.=A PR
FRAP64	TIVE PROCESSOR	STUDY	=ASSOCIA
HSSO64		STUDY	OF ELASTIC SWITCHING FOR ASSOCIATIVE MEMORY SYSTEMS.=
IRSO63		STUDY	OF THE APPLICATIONS OF PARALLEL SEARCH MEMORIES.=
IRHA64	ATIVE COMPUTER	STUDY	=HYBRID ASSOCI
CYAP67	A PROGRAMMING	STUDY	OF A NON-NUMERICAL PROCESSOR.=
LSAP65	ING TECHNIQUES	STUDY	=ASSOCIATIVE PROCESS
IRLM60	LOGICAL MEMORY	STUDY	=LOGICA
FRSO65		STUDY	OF ASSOCIATIVE PROCESSING TECHNIQUES.=
DGAS66	A	STUDY	OF THE UTILITY OF A HYBRID ASSOCIATIVE MEMORY PROCESSOR.=
FSAP64	TIVE PROCESSOR	STUDY	=ASSOCIA
CMSO64		STUDY	OF ASSOCIATIVE MEMORY APPLICATION.=
BCSO66		STUDY	OF ASSOCIATIVE PROCESSING TECHNIQUES.=
BCSO66		STUDY	OF ASSOCIATIVE PROCESSING TECHNIQUES.=
GRHA66	ATIVE COMPUTER	STUDY	=HYBRID ASSOCI
WDSA64		STUDY	AND INVESTIGATION TO DEVELOP COMPILER TECHNIQUES REQUIRED FOR PROGRAMMING THE
RFST64		STUDY	TO DETERMINE THE APPLICABILITY OF THE SOLOMON COMPUTER TO COMMAND AND CONTROL.
YCAS64	A	STUDY	OF CRYOTRON ASSOCIATIVE MEMORY IN DIGITAL SYSTEMS.=
JHSO68		STUDY	OF ADVANCED ASSOCIATIVE PROCESSOR TECHNIQUES INTERIM REPORT.=
RDAC66	R ORGANIZATION	STUDY	=ADVANCED COMPUTE
RJAC67	A CASE	STUDY	IN PROGRAMMING FOR PARALLEL PROCESSORS.=
TRCA64	CIATIVE MEMORY	STUDY	=COMPUTER ASSO
SLAS66	RING PROCESSOR	STUDY	=ASSOCIATIVE-STO
STFS61	FEASIBILITY	STUDY	FOR A CRYOGENIC ASSOCIATIVE MEMORY.=
STCA64	CIATIVE MEMORY	STUDY	=COMPUTER ASSO
RFST64		STUDY	TO DETERMINE THE APPLICABILITY OF THE SOLOMON COMPUTER TO COMMAND AND CONTROL.
PCAM67	LER TECHNIQUES	STUDY	=ASSOCIATIVE MEMORY COMPI
SRAS67	SEARCH MEMORY	STUDY	=ASSOCIATIVE
SLAS66	RING PROCESSOR	STUDY	=ASSOCIATION-STO
GRHA66	ATIVE COMPUTER	STUDY	=HYBRID ASSOCI
ACAM68	VESTIGATIONS :	SUBSTRUCTURE	SEARCHING AND DATA ORGANIZATION.=ASSOCIATIVE MEMORY IN
KAAS63	SEARCH MEMORY	SUBSYSTEM	FOR A GENERAL PURPOSE COMPUTER.=A
HJAU59	NUMBER OF	SUB-PROGRAMS	SIMULTANEOUSLY.=A UNIVERSAL COMPUTER, CAPABLE OF EXECUTING AN ARBITRARY
NRHS	TCHING ELEMENT	SUITABLE	FOR TWO-DIMENSIONAL FABRICATION.=HIGH-SPEED SUPERCONDUCTIVE SWI
MHIO62	ESS TECHNIQUES	SUITABLE	FOR USE IN LARGE-CAPACITY DIGITAL MEMORIES. =INVESTIGATION OF STORAGE AND ACC
ABAS64	ANNUAL	SUMMARY	REPORT OF INVESTIGATION IN DIGITAL TECHNOLOGY RESEARCH.=
CCSO64		SUMMARY	OF INVESTIGATION ON ASSOCIATIVE MEMORIES.=

BHAM65	Y USING ANALOG,	SUMMING	TECHNIQUE.=ASSOCIATIVE MEMOR
GKAW	WORD-ORGANIZED	SUPERCONDUCTING	CONTINUOUS FILM MEMORY=A
SOTR68	OF OPERATING A	SUPERCONDUCTING	MEMORY CELL - A PERSISTOTRON - IN A MEMORY MATRIX. =THE RELIABILITY
IKSC61		SUPERCONDUCTING	COMPUTERS.=
BLCS60	NTINUOUS SHEET	SUPERCONDUCTING	MEMORY.=CO
VVPO68	S THROUGH THIN	SUPERCONDUCTING	FILMS.=PENETRATION OF MAGNETIC FIELD
YDRD61	IN HIGH-SPEED	SUPERCONDUCTING	DEVICES.=RECENT DEVELOPMENTS
PJST66		SUPERCONDUCTING	THIN-FILM TECHNOLOGY AND APPLICATIONS.=
LASC61		SUPERCONDUCTING	COMPUTERS.=
GMEA65	ASPECTS OF THE	SUPERCONDUCTING	CONTINUOUS FILM STORE.=EXPERIMENTAL AND THEORETICAL
NVSC61		SUPERCONDUCTING	CIRCUITS FOR COMPUTING MACHINES.=
CKIO63	SPEED OF	SUPERCONDUCTING	COMPUTER ELEMENTS.=INFLUENCE OF THERMAL EFFECTS ON THE OPERATING
CJTF57	TRAPPED-FLUX	SUPERCONDUCTION	MEMORY.=
GKAC	EMORY CELL FOR	SUPERCONDUCTIVE	ASSOCIATIVE MEMORIES=A CONTINOUS FILM M
KHSA67		SUPERCONDUCTIVE	CONTINUOUS FILM MEMORY CELLS=
ARSM63		SUPERCONDUCTIVE	MEMORIES.=
NBHS	HIGH-SPEED	SUPERCONDUCTIVE	SWITCHING ELEMENT SUITABLE FOR TWO-DIMENSIONAL FABRICATION.=
SASS62		SUPERCONDUCTIVE	SWITCHES AND STORAGE DEVICES.=
IBAA60	E MEMORY USING	SUPERCONDUCTIVE	TECHNIQUES.=AN ASSOCIATIV
DPAS62	A	SUPERCONDUCTIVE	ASSOCIATIVE MEMORY.=
RJIM65	D MAGNETIC AND	SUPERCONDUCTIVE	MEMORIES : A SURVEY OF TECHNIQUES, RESULTS AND PROSPECTS.=INTEGRATE
SCTP65	ON UTILIZING A	SUPERCONDUCTIVE	GROUND PLANE.=THE PERSISTATR
BACC61	CIDENT CURRENT	SUPERCONDUCTIVE	MEMORY.=COIN
MTSC61		SUPERCONDUCTIVE	COMPUTERS - COMMONPLACE IN TEN YEARS ?.=
ARSA63		SUPERCONDUCTIVE	ASSOCIATIVE MEMORIES.=
ABSM64		SUPERCONDUCTIVE	MEMORIES.=
ARTB65	E CELL - A NEW	SUPERCONDUCTIVE	MEMORY CELL FOR RANDOM-ACCESS WORK-ORGANIZED MEMORIES.=THE BRIDG
NVAS64	APPLIED	SUPERCONDUCTIVITY	=
ARCO65	ER NETWORK FOR	SUPER-CONDUCTIVE	ASSOCIATIVE MEMORIES.=CALCULATIONS OF SPEED OF LAND
IRSS64	SEA	SURVEILLANCE	DATA BASE REPRESENTATION AS TEST VEHICLE.=
HLRA63	REVIEW AND	SURVEY	OF MASS MEMORIES.=
HTSO69		SURVEY	OF PARALLEL PROCESSOR APPROACHES AND TECHNIQUES.=
LMAS66	A	SURVEY	OF PROBLEMS AND PRELIMINARY RESULTS CONCERNING PARALLEL PROCESSING AND PARALLE
HTGS64	GENERAL	SURVEY	: ASSOCIATIVE STORAGE FOR NUCLEAR PHYSICS.=
GJCD67	SIGN : A	SURVEY	=COMPOUND DATA STRUCTURE FOR COMPUTER AIDED DE
RBAB67	A BRIEF	SURVEY	OF COMPUTER LANGUAGES FOR SYMBOLIC AND ALGEBRAIC MANIPULATION.=
RJIM65	E MEMORIES : A	SURVEY	OF TECHNIQUES, RESULTS AND PROSPECTS.=INTEGRATED MAGNETIC AND SUPERCONDUCTIV
RJAS62	A	SURVEY	OF COMPUTER MEMORIES.=
SSSO64		SURVEY	OF PRESENT AND POTENTIAL SEARCH MEMORY - IMPLEMENTATION AND TECHNIQUES.=
LMAS65	A	SURVEY	OF READ ONLY MEMORIES.=
MRSO67		SURVEY	OF MICROCELLULAR RESEARCH.=
RJCM61	R MEMORIES - A	SURVEY	OF THE STATE-OF-THE-ART.=COMPUTE
HACA66	STEMS - A	SURVEY	=CONTENT-ADDRESSABLE AND ASSOCIATIVE MEMORY SY
SASS62	UPERCONDUCTIVE	SWITCHES	AND STORAGE DEVICES.=S
NBHS	UPERCONDUCTIVE	SWITCHING	ELEMENT SUITABLE FOR TWO-DIMENSIONAL FABRICATION.=HIGH-SPEED S
HSSO64	UDY OF ELASTIC	SWITCHING	FOR ASSOCIATIVE MEMORY SYSTEMS.=ST
SAPO59	THE THEORY OF	SWITCHING	APRIL, 1957.=PROCEEDINGS OF THE INTERNATIONAL SYMPOSIUM ON
SKES60	ELASTIC	SWITCHING	PROPERTIES OF SOME SQUARE LOOP MATERIALS IN TOROIDAL STRUCTURES.=
OJSF63		SWITCHING	FUNCTIONS FOR SIMPLIFIED DATA RETRIEVAL AND DISPLAY DEVICES.=
HLSC65		SWITCHING	CHARACTERISTICS OF CROSSED-FILM CRYOTRON CIRCUITS.=
SRSM61		SYMBOL	MANIPULATION WITH AN ASSOCIATIVE MEMORY.=
GRCL61	LANGUAGES FOR	SYMBOL	MANIPULATION.=COMPUTER
RBAB67	LANGUAGES FOR	SYMBOLIC	AND ALGEBRAIC MANIPULATION.=A BRIEF SURVEY OF COMPUTER
WJSL63		SYMMETRIC	LIST PROCESSOR.=
EWOO62	ECTORS OF REAL	SYMMETRIC	MATRICES.=ORGANIZATION OF A ' FIXED-PLUS-VARIABLE ' STRUCTURE COMPUTER FOR COM
SAPO59	INTERNATIONAL	SYMPOSIUM	ON THE THEORY OF SWITCHING, APRIL, 1957.=PROCEEDINGS OF THE
BMAH62	AL MACHINE FOR	SYNTAX	TESTS.=A HYPOTHETIC

LPAF65	N EXPERIMENTAL	SYNTAX DIRECTED	DATA STRUCTURE LANGUAGE A
LCS			
BMAA69	ANALYSIS AND	SYNTHESIS	OF CONTROL MECHANISMS FOR PARALLEL PROCESSES.=
KGTL		TABLE	LOOKUP PROCEDURES IN DATA PROCESSING.=
KNTL62		TABLE	LOOKUP STUDY MODEL.=
GJTL62		TABLE	LOOKUP COMPUTERS.=
CGAT61	A	TABLE	LOOK-UP MACHINE FOR PROCESSING NATURAL LANGUAGES.=
IBTA66		TAG	ADDRESSED MEMORY.=
HBAT65	ASSOCIATIVE	TAG	MEMORY.=
WMTM63		TAG	MEMORY.=
SHTA62		TAG-ADDRESSED	MEMORY.=
JKTT62		TARGET	TRACK CORRELATION WITH A SEARCH MEMORY.=
RMSI66	NG INDEPENDENT	TASKS	ON PARALLEL PROCESSORS.=SCHEDULI
GPTM61	TI-LIST SYSTEM	TECHNICAL	REPORT NO. 1.=THE MUL
IIIQT65	QUARTERLY	TECHNICAL	PROGRESS REPORT FOR OCTOBER, NOVEMBER, DECEMBER, 1965.=
PGTM61	TI-LIST SYSTEM	TECHNICAL	REPORT NUMBER 1.=THE MUL
WPST66	SCIENTIFIC	TECHNICAL	INFORMATION NO. 6, 1964 : SELECTED ARTICLES.=
IIIQT67	QUARTERLY	TECHNICAL	PROGRESS REPORT, APRIL, MAY, JUNE, 1967=
NAOP60	INTELLIGENT	TECHNICIAN	=ON PROGRAMMING A HIGHLY PARALLEL MACHINE TO BE AN
YYAN66	NBULK ADDITION	TECHNIQUE	FOR ASSOCIATIVE PROCESSORS.=A NO
CWPW67	BIT-STEERING	TECHNIQUE	=PLATED WIRE CONTENT-ADDRESSABLE MEMORIES WITH
MAAT65	CTIVE READ-OUT	TECHNIQUE	=A THIN MAGNETIC FILM COMPUTER MEMORY USING A REASONANT ABSORPTION NON-DESTRU
BHAM65	ANALOG SUMMING	TECHNIQUE	=ASSOCIATIVE MEMORY USING
OSAT71	ASSOCIATIVE	TECHNIQUES	IN THE SOLUTION OF DATA MANAGEMENT PROBLEMS=
GPAP65	IVE PROCESSING	TECHNIQUES	=ASSOCIAT
HTSO69	APPROACHES AND	TECHNIQUES	=SURVEY OF PARALLEL PROCESSOR
SBCA66	LE PROGRAMMING	TECHNIQUES	=CONTENT-ADDRESSAB
IBCA	CIATIVE MEMORY	TECHNIQUES	=CRYOGENIC ASSO
HWIO61	-SCREEN MEMORY	TECHNIQUES	=INVESTIGATION OF WOVEN
MHIO62	AGE AND ACCESS	TECHNIQUES	SUITABLE FOR USE IN LARGE-CAPACITY DIGITAL MEMORIES. =INVESTIGATION OF STOR
TRFT66	FABRICATION	TECHNIQUES	FOR BATCH FABRICATION OF DISTRIBUTED LOGIC NETWORKS.=
IBAP62	ION RETRIEVAL	TECHNIQUES	=A PROPOSAL FOR THE STUDY OF ADVANCED INFORMAT
IBAP63	IVE PROCESSING	TECHNIQUES	=ASSOCIAT
HAAP63	SSING	TECHNIQUES	=A PROPOSAL FOR THE STUDY OF ASSOCIATIVE PROCE
MSFI61	E AND ACCESS	TECHNIQUES	=FUNDAMENTAL INVESTIGATION OF DIGITAL COMPUTER STORAG
IBAA60	UPERCONDUCTIVE	TECHNIQUES	=AN ASSOCIATIVE MEMORY USING S
LSAP65	IVE PROCESSING	TECHNIQUES	STUDY.=ASSOCIAT
CGLP68	SSING RESEARCH	TECHNIQUES	=LIST PROCE
GPAM	CIATIVE MEMORY	TECHNIQUES	=ASSO
BCSO66	IVE PROCESSING	TECHNIQUES	=STUDY OF ASSOCIAT
GFAT66	ASSOCIATIVE	TECHNIQUES	FOR CONTROL FUNCTIONS IN A MULTIPROCESSOR.=
FBSO65	IVE PROCESSING	TECHNIQUES	=STUDY OF ASSOCIAT
BPAS61	IATIVE STORAGE	TECHNIQUES	=ASSOC
GJTF62		TECHNIQUES	FOR ADVANCED INFORMATION PROCESSING SYSTEM.=
CJLP67	SSING RESEARCH	TECHNIQUES	=LIST PROCE
BCSO66	IVE PROCESSING	TECHNIQUES	=STUDY OF ASSOCIAT
WDCA68	ASSOCIATIVE	TECHNIQUES	=COMPUTER-AIDED STRATEGY DESIGN USING ADAPTIVE AND
BACR64	CTRIC RECEIVER	TECHNIQUES	=CRYOELE
RJIM65	: A SURVEY OF	TECHNIQUES	RESULTS AND PROSPECTS.=INTEGRATED MAGNETIC AND SUPERCONDUCTIVE MEMORIES
SWAM63	CIATIVE MEMORY	TECHNIQUES	FOR LARGE DATA PROCESSORS.=ASSO
YMLC62	APACITY MEMORY	TECHNIQUES	FOR COMPUTING.=LARGE-C
GGAT67	ASSOCIATIVE	TECHNIQUES	FOR CONTROL FUNCTIONS IN A MULTI-PROCESSOR SIMULATION INVESTIGATION.=
SSSO64	EMENTATION AND	TECHNIQUES	=SURVEY OF PRESENT AND POTENTIAL SEARCH MEMORY - IMPL
RLCM65	NTERCONNECTION	TECHNIQUES	=CRYOGENICS MEMORY PLANE I
JHSO68	TIVE PROCESSOR	TECHNIQUES	INTERIM REPORT.=STUDY OF ADVANCED ASSOCIA
WDSA64	VELOP COMPILER	TECHNIQUES	REQUIRED FOR PROGRAMMING THE PARALLEL NETWORK COMPUTER.=STUDY AND INVESTIGATI
HRAO	N OF CRYOGENIC	TECHNIQUES	TO COMPUTER TECHNOLOGY.=APPLICATIO

WDMP64	PLE PROCESSING	TECHNIQUES	=MULTI
BJCC63	OTRON COMPUTER	TECHNIQUES	=CRY
CWCA66	ESSABLE MEMORY	TECHNIQUES	=CONTENT-ADDR
PCAM67	EMORY COMPILER	TECHNIQUES	STUDY.=ASSOCIATIVE M
CWCA65	ESSABLE MEMORY	TECHNIQUES	=CONTENT-ADDR
RJCA64	CIATIVE MEMORY	TECHNIQUES	=CRYOGENIC ASSO
CRCA67	ESSABLE MEMORY	TECHNIQUES	=CONTENT-ADDR
ABCA64	CIATIVE MEMORY.	TECHNIQUES	=CRYOGENIC ASSO
LEAT63	ASSOCIATIVE	TECHNIQUES	WITH COMPLEMENTING FLIP-FLOP.=
CSDT66	DESIGN	TECHNIQUES	OF A DELAY-LINE CONTENT-ADDRESSED MEMORY.=
CWCA65	ESSABLE MEMORY	TECHNIQUES	=CONTENT-ADDR
HTPP70	ESSOR SYSTEMS,	TECHNOLOGIES	AND APPLICATIONS=PARALLEL PROC
MIRA68	LOPMENT OF THE	TECHNOLOGIES	REQUIRED TO DESIGN AND FABRICATE ULTRAHIGH-SPEED COMPUTER SYSTEMS.=RESEARCH AN
KBAI67	NCES IN MEMORY	TECHNOLOGY	=ADVA
ABAS64	ION IN DIGITAL	TECHNOLOGY	RESEARCH.=ANNUAL SUMMARY REPORT OF INVESTIGAT
EGDT64	DIGITAL	TECHNOLOGY	RESEARCH.=
PJST66	TING THIN-FILM	TECHNOLOGY	AND APPLICATIONS.=SUPERCONDUC
HHAO	ES TO COMPUTER	TECHNOLOGY	=APPLICATION OF CRYOGENIC TECHNIQU
AOAH66	YBRID CRYOTRON	TECHNOLOGY	2 - FABRICATION.=1 H
FOAH66	YBRID CRYOTRON	TECHNOLOGY	I - CIRCUITS AND DEVICES.=A H
FGLT68	LOW	TEMPERATURE	BEAM-ADDRESSABLE MEMORY.=
MHRO64	ESEARCH ON LOW	TEMPERATURE	COMPUTING ELEMENTS.=R
CATK62	WORKS AT ROOM	TEMPERATURE	=3-K BIT ASSOCIATIVE MEMORY
MDTL61		TENTATIVE	LOGICAL REALIZATION OF A PATTERN RECOGNITION COMPUTER.=
GJBT60	TESTS FOR TWO	TERMINAL	SIMULTANEOUS ACTION.=BINARY
KMPO66	DETERMINACY,	TERMINATION	QUEUEING.=PROPERTIES OF A MODEL FOR PARRALLEL COMPUTATIONS:
IRSS64	RESENTATION AS	TEST	VEHICLE.=SEA SURVEILLANCE DATA BASE REP
RGCA64	ROCESSOR PLANE	TEST	AND EVALUATION.=CRYOGENIC ASSOCIATIVE P
KKDT68	DIAGNOSTIC	TEST	PATTERNS AND SEQUENCES FOR ILLIAC-IV PROCESSING ELEMENT.=
PJFA66	ABRICATION AND	TESTING	OF 5000 WORD CRYOGENIC ASSOCIATIVE PROCESSOR.=F
PJFA67	ABRICATION AND	TESTING	OF 5000 WORD CRYOGENIC ASSOCIATIVE PROCESSOR.=F
PJFA65	ABRICATION AND	TESTING	OF CRYOGENIC ASSOCIATIVE PROCESSOR PLANES.=F
GJBT60	BINARY	TESTS	FOR TWO TERMINAL, SIMULTANEOUS ACTION.=
BMAH62	INE FOR SYNTAX	TESTS	=A HYPOTHETICAL MACH
WAAS68	ERED-RETRIEVAL	THEOREM	FOR ASSOCIATIVE MEMORIES.=A SIMPLE PROOF OF LEWIN'S ORD
GMEA65	PERIMENTAL AND	THEORETICAL	ASPECTS OF THE SUPERCONDUCTING CONTINUOUS FILM STORE.=EX
HAST63	SOME	THEORIZING	ON MEMORY STRUCTURE AND INFORMATION RETRIEVAL.=
ASII65	TIONS INTO THE	THEORY	OF AN INTERACTIVE CIRCUIT STORED PROGRAM PARALLEL PROCESSOR.=INVESTIGA
KSTA64		THEORY	AND ORGANIZATION OF A REPRESENTATIVE SEARCH MEMORY.=
SAPO69	MPOSIUM ON THE	THEORY	OF SWITCHING, APRIL, 1957.=PROCEEDINGS OF THE INTERNATIONAL SY
EITO68		THEORY	OF CELLULAR LOGIC NETWORKS AND MACHINES.=
SHMA64	Y AND CIRCUITS	THEREFOR	=MEMOR
CRIO63	INFLUENCE OF	THERMAL	EFFECTS ON THE OPERATING SPEED OF SUPERCONDUCTING COMPUTER ELEMENTS.=
LMTF69		THIN	FILM ASSOCIATIVE MEMORY.=
NMCA65	T OF MAGNETIC	THIN	FILMS.=CONTENT-ADDRESSED MEMORY USING MAGNETORESISTIVE READOU
SSTF60		THIN	FILM CRYOTRON CATALOG MEMORY.=
GPNR67	(NDRO) FROM	THIN	MAGNETIC FILMS.=NONDESTRUCTIVE READOUT
MAAT65	A	THIN	MAGNETIC FILM COMPUTER MEMORY USING A REASONANT ABSORPTION NON-DESTRUCTIVE REA
KASC67	SMALL CAPACITY	THIN	CYLINDRICAL MAGNETIC FILM STORAGE SYSTEMS.=SMALL
VVPO58	FIELDS THROUGH	THIN	SUPERCONDUCTING FILMS.=PENETRATION OF MAGNETIC,
PJST66	UPERCONDUCTING	THIN-FILM	TECHNOLOGY AND APPLICATIONS.=S
SSTF60		THIN-FILM	CRYOTRONS.=
SSTF60		THIN-FILM	CRYOTRON CATALOG MEMORY.=
NEDA62	D MEMORY USING	THIN-FILM	CRYOTRONS.=DATA ADDRESSE
SNTW66		THREE-WIRE	CRYOELECTRIC MEMORY SYSTEMS.=
MCAT63	ADAPTIVE	THRESHOLD	LOGIC.=
PAAC70	R MASS STORAGE	THROUGH	ARRAY ORGANIZATION=ASSOCIATIVE CAPABILITIES FO

FRALA7	G CAPABILITIES	THROUGH	ASSOCIATIVE PARALLEL PROCESSING=ACHIEVING LARGE SCALE COMPUTIN
SHAP69	POSE COMPUTERS	THROUGH	THE USE OF MODIFIED MEMORIES.=ASSOCIATIVE PROCESSING FOR GENERAL PUR
SRDR65	ANNEL ANALYZER	THROUGH	ASSOCIATIVE PROGRAMMING OF A SMALL COMPUTER.=DIRECT-RECORDING MEGACH
KMSP64	PTATION TO USE	THROUGH	MAN-MACHINE INTERACTION.=SOME PROBLEMS IN INFORMATION SCIENCE WITH EMPHASIS ON
FRAL	G CAPABILITIES	THROUGH	ASSOCIATIVE PARALLEL PROCESSING.=ACHIEVING LARGE COMPUTIN
SDAL	G CAPABILITIES	THROUGH	AN ARRAY COMPUTER.=ACHIEVING LARGE COMPUTIN
SHAP68	MPUTERS	THROUGH	THE USE OF MODIFIED MEMORIES.=ASSOCIATIVE PROCESSING FOR GENERAL PURPOSE CO
VVPO58	AGNETIC FIELDS	THROUGH	THIN SUPERCONDUCTING FILMS.=PENETRATION OF M
BTAM71	YSTEM FOR REAL	TIME	COMPUTERS =A MULTIPLEXED I/O S
IYAI67	NOSECOND CYCLE	TIME	=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMORY SYSTEM WITH 100 NA
IYAI	OSECONDS CYCLE	TIME	=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMORY WITH 100-NAN
LAAA61	UCE THE ACCESS	TIME	FOR INSTRUCTIONS IN LOOPS.=AN APPLICATION FOR A SMALL, FAST ASSOCIATIVE MEMORY
GRPS63	SYSTEM SEARCH	TIME	ANALYSIS.=PRELIMINARY
HHCS68	MEMORY FOR A	TIME-SHARED	PROCESSOR.=CONTROL STORAGE USE IN IMPLEMENTING AN ASSOCIATIVE
WGAT68	A	TIMING	SIMULATOR OF ILLIAC-IV.=
NGSA63	ESIGNS FOR THE	TOBERMORY	PERCEPTION.=SYSTEM AND CIRCUIT D
FRVT69	VARIABLE	TOPOLOGY	RANDOM ACCESS MEMORY ORGANIZATIONS=
FRVT69	VARIABLE	TOPOLOGY	RANDOM ACCESS MEMORY ORGANIZATIONS.=
TKAT61	A	TOROIDAL	NONDESTRUCTIVE MEMORY ELEMENT USING BIAS RESTORATION.=
SKES60	MATERIALS IN	TOPOIDAL	STRUCTURES.=ELASTIC SWITCHING PROPERTIES OF SOME SQUARE LOOP
JKTT62	TARGET	TRACK	CORRELATION WITH A SEARCH MEMORY.=
EETU67	SSORS IN RADAR	TRACKING	AND CORRELATION.=THE USE OF ASSOCIATIVE PROCE
HMAT63	A	TRAINABLE	WEATHER-FORECASTING SYSTEM.=
ASTA69		TRAMP	AN INTERPRETIVE ASSOCIATIVE PROCESSOR WITH DEDUCTIVE CAPABILITIES=
ASTA67		TRAMP	: A RELATIONAL MEMORY WITH AN ASSOCIATIVE BASE.=
NYSA69	ORITHMS IN THE	TRANQUIL	COMPILER.=STORAGE ALLOCATION ALG
RRTC64		TRANSFLUXOR	CONTENT-ADDRESSABLE MEMORY.=
WMAP69	E FAST FOURIER	TRANSFORM	=ASSOCIATIVE PARALLEL PROCESSING FOR TH
BHAT67	A	TRANSFORMATION	FOR EXTRACTING NEW DESCRIPTORS OF SHAPES.=
NEMO67	CYCLIC GRAPH	TRANSFORMATIONS	=MODELS OF COMPUTATIONAL SYSTEMS - CYCLIC TO A
IYAI67	INTEGRATED MOS	TRANSISTOR	ASSOCIATIVE MEMORY SYSTEM WITH 100 NANOSECOND CYCLE TIME.=AN
IYAI	INTEGRATED MOS	TRANSISTOR	ASSOCIATIVE MEMORY WITH 100-NANOSECONDS CYCLE TIME.=AN
IKAH66	EGRATED MOS	TRANSISTORS	=A 150-NANOSECOND ASSOCIATIVE MEMORY USING INT
WRAT	A	TRANSISTOR-TUNNEL	DIODE CELL FOR ASSOCIATIVE MEMORIES AND MULTIPLE-WORD ACCESS MEMORIES.=
RRTA67		TRANSLATED	ASSOCIATIVE MEMORY ADDRESSING.=
HJAC67	S TO MACHINE	TRANSLATION	=A CONTENT ADDRESSABLE MEMORY WITH APPLICATION
CJTF67		TRAPPED-FLUX	SUPERCONDUCTION MEMORY.=
BIAT63	A	TREE	STRUCTURE SYSTEM FOR SORTING, SEARCH AND MAINTENANCE.=
SWSA63	ROPERTIES OF A	TREE	ORIENTED MEMORY SYSTEM.=STORAGE AND SEARCH P
LACO62	CODING OF	TREES	FOR USE IN AN ASSOCIATIVE MEMORY.=
RJNT64	NEW	TRENDS	IN COMPUTER MEMORIES.=
FETM60		TRIE	MEMORY.=
TRTC62		TRUE	CONTENT-ADDRESSABLE MEMORY.=
PFCT63	CRYOGENIC	TUBE	FITTING.=
CRAT62	A	TUNNEL	DIODE ASSOCIATIVE MEMORY.=
TIHS61	ED MEMORY USES	TUNNEL	DIODES.=HIGH-SPE
NRHS	SUITABLE FOR	TWO-DIMENSIONAL	FABRICATION.=HIGH-SPEED SUPERCONDUCTIVE SWITCHING ELEMENT
PGTM62	THE MULTI-LIST	TYPE	ASSOCIATIVE MEMORY.=THE MU
SHRO63	SEARCH ON BIAX	TYPE	ELEMENTS AND ASSOCIATED CIRCUITS.=RE
PGTO62	F A MULTI-LIST	TYPE	ASSOCIATIVE MEMORY.=THE ORGANIZATION O
LWSA68	N-CONVENTIONAL	TYPES	OF COMPUTERS.=SOME ARGUMENTS FAVORING NO
MIRA68	AND FABRICATE	ULTRAHIGH-SPEED	COMPUTER SYSTEMS.=RESEARCH AND DEVELOPMENT OF THE TECHNOLOGIES REQUIRED TO DES
SDUS67		UNCONVENTIAL	SYSTEMS.=
WAUI69	SIFICATION AND	UNIFIED	3-CLASSIFICATION FOR ASSOCIATIVE MEMORIES=UNIFIED INTERVAL CLAS
WAUI69		UNIFIED	INTERVAL CLASSIFICATION AND UNIFIED 3-CLASSIFICATION FOR ASSOCIATIVE MEMORIES=
SJPD64	N ARTICULATION	UNIT	OF ILLIAC-III.=PROGRAM DESCRIPTION OF PAX AN IBM 7090 PROGRAM TO SIMULATE THE
BVMO66	IATIVE MEMORY	UNIT	=MODELING OF A MEMORY SYSTEM INCLUDING A BUFFER ASSOC

SJUM64	N ARTICULATION	UNIT	OF ILLIAC-III.=USER'S MANUAL FOR PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTE
SHTC62	ENTRAL CONTROL	UNIT	OF THE ATLAS COMPUTER.=THE C
HJAU59	A	UNIVERSAL	COMPUTER, CAPABLE OF EXECUTING AN ARBITRARY NUMBER OF SUB-PROGRAMS SIMULTANEOU
BRTP69	SYSTEM AT THE	UNIVERSITY	OF ILLINOIS PROGRAMMING MANUAL.=THE PAX-2 PICTURE PROCESSING
KAA069	F ILLIAC-IV TO	URBAN	DEFENSE RADAR PROBLEM.=APPLICATION O
KAA068	F ILLIAC-IV TO	URBAN	DEFENSE RADAR PROBLEM.=APPLICATION O
MRTS69	STEM LOGIC AND	USAGE	RECORDER=THE SY
OBAP67	MMING LANGUAGE	USER'S	MANUAL.=APL - ASSOCIATIVE PROGRA
FNUM		USER'S	MANUAL FOR THE ASSOCIATIVE MEMORY, PARALLEL PROCESSING LANGUAGE, AMPPL-II.=
SJUM64		USER'S	MANUAL FOR PAX AN IBM 7090 PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT O
SLAS68	ASP	USER'S	MANUAL ASSOCIATION-STORING PROCESSOR INTERPRETER PROGRAM.=
HRIT63	EMORY WITH THE	USQ-20	COMPUTER.=INTEGRATING THE SEARCH M
DGAS66	A STUDY OF THE	UTILITY	OF A HYBRID ASSOCIATIVE MEMORY PROCESSOR.=A STUD
NRSS69	SIDERATIONS IN	UTILIZATION	OF A NETWORK OF COMPUTERS.=SOME SOFTWARE CON
GVTP61	SPECTS FOR THE	UTILIZATION	OF INFORMATIONAL-LOGICAL MACHINES IN CHEMISTRY.=THE PRO
SCTP65	E PERSISTATRON	UTILIZING	A SUPERCONDUCTIVE GROUND PLANE.=TH
PGAS64	RMANENT MEMORY	UTILIZING	CORRELATION ADDRESSING.=A SEMIPE
FRVT69		VARIABLE	TOPOLOGY RANDOM ACCESS MEMORY ORGANIZATIONS=
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EGVS64		VARIABLE	STRUCTURE COMPUTER SYSTEM.=
BBP062	ROPERTIES OF A	VARIABLE	STRUCTURE COMPUTER SYSTEM IN THE SOLUTION OF PARABOLIC PARTIAL DIFFERENTIAL EQ
CFLA62	ON IN A	VARIABLE	STRUCTURE DIGITAL COMPUTER.=LOGARITHMIC AND EXPONENTIAL FUNCTION EVALUATI
TRA063	INVENTORY OF A	VARIABLE	STRUCTURE COMPUTER.=ASSIGNMENT OF
EG0060	THE FIXED PLUS	VARIABLE	STRUCTURE COMPUTER.=ORGANIZATION OF COMPUTER SYSTEMS -
IRSS64	TATION AS TEST	VEHICLE	=SEA SURVEILLANCE DATA BASE PRESEN
SJAT64	ND PRELIMINARY	VERSION	=AT-1 PARALLEL COMPUTER - SECO
SWPC60	COMPUTING WITH	VERTICAL	DATA.=PARALLEL
SAAD64	EVICE POINT OF	VIEW	=A DISCUSSION OF ASSOCIATIVE MEMORIES FROM A D
SSAM63	MING POINT OF'	VIEW	=ASSOCIATIVE MEMORY COMPUTERS FROM THE PROGRAM
BHAA62	ALING WITH THE	VISUAL	FIELD AND SOME OF ITS BIOLOGICAL IMPLICATIONS.=AN ASSOCIATIVE MACHINE FOR DE
BHAM62	FOR PERFORMING	VISUAL	RECOGNITION BY USE OF ANTENNA PROPAGATION CONCEPTS.=A MACHINE
MRIL65	A PROCESSOR OF	VISUAL	INFORMATION.=ILLIAC-III:
RFST64	AND CONTROL.	VOLUME	I. INFORMATION STORAGE, RETRIEVAL AND COMMUNICATION SYSTEM CONTROL.=STUDY TO D
RRAA64	CURRENT RANDOM	WALKS	ON HIGHLY PARALLEL MACHINES.=A ALGORITHM FOR CON
CCA0	EMORIES TO THE	WEAPON	ASSIGNMENT PROBLEM OF NTDS.=APPLICATION OF ASSOCIATIVE M
CWA067	G TO NUMERICAL	WEATHER	PREDICTION.=APPLICATION OF PARALLEL PROCESSIN
HMAT63	A TRAINABLE	WEATHER-FORECASTING SYSTEM.=	
CWPW67	PLATED	WIRE	CONTENT-ADDRESSABLE MEMORIES WITH BIT-STEERING TECHNIQUE.=
BGAM69	R USING PLATED	WIRE	=A MISSION ORIENTED ASSOCIATIVE PROCESSO
FKTP64	E PLATED-WOVEN	WIRE	MEMORY MATRIX.=TH
DPPW64	PLATED	WIRE	MAGNETIC FILM MEMORIES.=
CSPW67	PLATED	WIRE	BIT STEERING FOR LOGIC AND STORAGE.=
PJFA66	ESTING OF 5000	WORD	CRYOGENIC ASSOCIATIVE PROCESSOR.=FABRICATION AND T
BDPP66	FOR RADC 2048	WORD	ASSOCIATIVE MEMORY.=PRELIMINARY PROGRAMMING MANUAL
WSTD62	SIGN OF A 4096	WORD	ONE MICROSECOND MAGNETIC FILM STORE.=THE DE
PCAT64	MEMORY OF 1024	WORD	48 BIT PER WORD CAPACITY.=A 10MO NDRO BIAX
PJFA67	ESTING OF 5000	WORD	CRYOGENIC ASSOCIATIVE PROCESSOR.=FABRICATION AND T
PCAT64	RD, 48 BIT PER	WORD	CAPACITY.=A 10MO NDRO BIAX MEMORY OF 1024 WO
GELT61	NG THE LARGEST	WORD	IN A FILE USING A MODIFIED MEMORY.=LOCATI
GKAW	A	WORD-ORGANIZED	SUPERCONDUCTING CONTINUOUS FILM MEMORY=
CATK62	CIATIVE MEMORY	WORKS	AT ROOM TEMPERATURE.=3-K BIT ASSO
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ANT865	RANDOM-ACCESS	WORK-ORGANIZED	MEMORIES.=THE BRIDGE CELL - A NEW SUPERCONDUCTIVE MEMORY CELL FOR
FTAP65	A	WOVEN	PLATED-WIRE ASSOCIATED MEMORY.=
SATW59	THE	WOVEN	CRYOTRON MEMORY. =
KMAH65	A HIGH-SPEED,	WOVEN	READ ONLY MEMORY.=
HWIO61	VESTIGATION OF	WOVEN-SCREEN	MEMORY TECHNIQUES.=IN

WTSC61	UNFLAGE AN TEN	YEARS	?.=SUPERCONDUCTIVE COMPUTERS - COMM
BBCR64	EMORY, PHASE 2	10	(9) BIT MEMORY.=CRYOELECTRIC RANDOM ACCESS M
PCAT64	A	10MO	NDRO BIAX MEMORY OF 1024 WORD, 48 BIT PER WORD CAPACITY.=
IYAI67	RY SYSTEM WITH	100	NANOSECOND CYCLE TIME.=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMO
IYAI	RY WITH	100-NANOSECONDS	CYCLE TIME.=AN INTEGRATED MOS TRANSISTOR ASSOCIATIVE MEMO
PCAT64	BIAX MEMORY OF	1024	WORD, 48 BIT PER WORD CAPACITY.=A 10MO NDRO
KJAH64	A	128-WORD	36-BIT MAGNETIC ASSOCIATIVE MEMORY.=
IKAH66	A	150-NANOSECOND	ASSOCIATIVE MEMORY USING INTEGRATED MOS TRANSISTORS.=
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WAUI69		3-CLASSIFICATION	FOR ASSOCIATIVE MEMORIES=UNIFIED INTERVAL CLASSIFICATION AND UNIFIED
CATK62		3-K	BIT ASSOCIATIVE MEMORY WORKS AT ROOM TEMPERATURE.=
RHAT63	A	300	NANOSECOND SEARCH MEMORY.=
SDUS66	US PATENT NO.	3287703	=.
WCAM69	MEMORY DEVICE	3466631	=ASSOCIATIVE
WCAM69	MEMORY DEVICE	3466632	=ASSOCIATIVE
KJAH64	A 128-WORD,	36-BIT	MAGNETIC ASSOCIATIVE MEMORY.=
JSTD62	HE DESIGN OF A	4096	WORD ONE MICROSECOND MAGNETIC FILM STORE.=T
PCAT64	OF 1024 WORD,	48	BIT PER WORD CAPACITY.=A 10MO NDRO BIAX MEMORY
PJFA66	AND TESTING OF	5000	WORD CRYOGENIC ASSOCIATIVE PROCESSOR.=FABRICATION
PJFA67	AND TESTING OF	5000	WORD CRYOGENIC ASSOCIATIVE PROCESSOR.=FABRICATION
SJUM64	OR PAX AN IBM	7090	PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=USER'S MANUAL
SJPD64	PAX AN IBM	7090	PROGRAM TO SIMULATE THE PATTERN ARTICULATION UNIT OF ILLIAC-III.=PROGRAM DESCR
SMMO64	ANIZATION OF A	7090	TO DO STATISTICAL ASSOCIATION PROCESSING.=MEMORY ORG
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