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OGO III DUST PARTICLE EXPERIMENT

Data Reduction and Analysis

FINAL REPORT

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by

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1. INTRODUCTION

The OGO III spacecraft contained an experiment (Experiment No. 16) to measure various physical parameters of picogram size dust particles in cis-lunar and near earth space. Information concerning the scientific objectives of the experiment, the basic sensors and detector array, the sensor calibration, electronic instrumentation, and experiment data are presented in this report - the final report on NASA contract with Temple University, NaS5-9352.

The OGO series dust particle experiment instrumentation was originally conceived in 1961 and resulted in an experiment on OGO I. The initial experimenters (1) participated in the first hypervelocity firings and calibration of the detectors. The electronic instrumentation was designed and fabricated by two industrial firms, and detailed information concerning the material presented in section five of the report is in the final reports from these two companies concerning the production of the OGO dust particle experiment units (2, 3). After the OGO I launch and flight several changes were made in the instrument to enhance the integrity of the experiment information. The report describes the OGO III instrument and measurements as interpreted by the final experimenters of record (4).

2. SCIENTIFIC OBJECTIVES

2.1 Historical Background

Since recorded time man has been interested in the solar system - moon, planets, meteorites and meteors at first. As science progressed the size of the bodies that could be detected became smaller and smaller until at the present time it is possible to detect particles much smaller than a picogram. The present investigation is in the picogram region. The first measurements of micrometeorites in space was made by Bohn and Nadig (5) in captured V-2 rockets flown at White Sands Proving Grounds, New Mexico, by the Air Force Cambridge Research Center. The detectors were made from ADP crystals and vacuum tubes were used for amplification. The first attempts were made in 1949; but the rocket failed, and it was not until 1950 that the first results were obtained. Essentially the same system, but using PZT detectors and transistorized electronics, was used in many Aerobee and other U.S.A. rockets. This same system was also used in Explorer I (6) and other satellites including OGO III, but with much more sophisticated electronic systems.

2.1 Cont.

Other systems of detection range from visual, photographic and radar to photometric observations of the zodiacal light not to mention various collection devices.

The OGO III measurements are mainly between 50,000 and 110,000 Km from the surface of earth and repeatedly sample the cis-lunar dust particle flux over a long period. These are the first such measurements since Pioneer I. (7)

2.2

Summary of Current Knowledge

Measurements from Mariner IV at 1 A.U. (12) and Pioneer I have shown a cumulative flux in cis-lunar space to be less than that in the vicinity of the earth. Prior to the OGO III measurement, the mass distribution of dust particles in the Earth-Moon system appeared as seen in Figure 1(8). Results of hypervelocity firings related to calibration of mic sensors (9) have indicated that the mass threshold sensitivities derived from early low velocity calibration efforts are in error. The most serious discrepancies affect the measurements from the experiments in the vicinity of the earth. These problems will be discussed later when the OGO III experiment measurement is presented. Thermal gradients in the sensors and/or mechanical package causing spurious noise pulses has been presented as a possible source of error in the data of near earth experiments (10). A further rigorous study of the thermal problem has been reported by Bohn, et al (11). Interpretation of the OGO III dust particle measurement, including consideration of the recent hypervelocity firings and thermal studies, is presented in section 6 of the report.

2.3

Information Desired in Geocentric and Cislunar Space

The mass distribution and orbits of picogram particles in cislunar space are necessary in order to determine (1) the degree of concentration of dust particles near the earth and (2) the extent to which lunar ejecta may serve as a source of near earth dust.

3. OGO III DUST PARTICLE TRIPLE COINCIDENCE TUBULAR DETECTOR

3.1 Basic Sensors

The basic sensor and detector array used in the OGO III dust particle experiment evolved from laboratory studies of microparticle hypervelocity impacts. A combination of acoustical and ionization sensors were

3.1 Cont.

first used on Mariner A. From this some of the instrumentation on OGO III was developed.

3.1.1 Thin Film Plasma Sensor

When a hypervelocity particle passes through a thin film a plasma is produced and a charge of either sign can be collected by a grid near by or a signal can be obtained by connecting a resistor and suitable voltage to the thin film, which is done in this case. A particle with diameter many times the thickness of the film can pass through it with little loss of velocity. However, depending upon its density composition and shape it may be fragmentized. It, nevertheless, will produce a signal at the front film.

3.1.2 Impact Plasma Sensor

This type of sensor is similar to the previous one. Here a hypervelocity particle produces a plasma upon impact on a metallic surface. A charge can then be collected producing a signal. The amplifiers associated with these plasma detectors must be very fast.

3.1.3 Impact Acoustical Sensor

An acoustical ceramic transducer (PZT) is cemented to the same metallic disk that serves as a source of impact plasma. An impacting particle will set up vibrations in the metallic disk which are then transmitted to the acoustical sensor.

3.2 Triple Coincidence Detector

The three sensors (Figure 2) are placed in a one inch diameter tube with the thin film plasma sensor 10 cm in front of the impact plate plasma sensor. A hypervelocity particle above threshold for the three detectors should produce three responses if it traverses the tube. This accounts for the name. Only triple responses are used as reliable data.

3.2.1 Time of Flight Measurements (TOF)

When a particle penetrates the front film a signal is produced to start a 2 mhz clock. If the particle now produces another signal at the other end of the tube, from either one of the two sensors, the clock will be stopped. The cycles from the clock will be transferred to the data shift register. From this information the TOF can be determined.

3.2.2 Energy Related Measurements

The amount of plasma produced by an impacting particle is energy dependent. By proper calibration the impact plasma pulse can be related to energy.

3.2.3 Impulse Related Measurements

A particle impinging upon an acoustical transducer will produce a response that is closely related to the momentum of the particle. We take it momentum dependent because we have no other definite data. In fact, over a small range, almost any scheme will work provided the proper constants are used.

4. CALIBRATION: LOW AND HYPERVELOCITY

Many studies (9) have been conducted on the response of various transducers when subjected to both high and low velocity impacts. In the present report we are interested in piezoelectric crystals and in thin films. The electrical response of PZT ceramic transducers, bonded to a metal plate, is to be determined as a function of impact parameters. It is generally agreed that for low velocities the response is proportional to the momentum transfer. Two studies (13, 14), however show that the response is linear for either elastic or inelastic impacts, but the inelastic impacts give three times the response for the same momentum transfer. The main question, however, is the behavior at hypervelocities.

4.1 Calibration Techniques

Most calibrations with microphones have been made using metal, glass, or plastic spheres at low velocities and metallic spheres at high velocities. In general the velocities are calculated from free fall data at low velocities and from electronic data at hypervelocities. The major hypervelocity work has used picogram dust particle electrostatic accelerators with 2 or 3 Mev Van de Graaffs providing the accelerating potential (15, 16).

4.1.2 Thin Film Hypervelocity Plasma Data

Charged carbonyl iron spheres, $r = 1\mu$, were accelerated to hypervelocities and impacted on the thin film sensor which had been placed in a small chamber and the appropriate bias voltages and amplifiers applied. The amplified sensor signal was displayed on an oscilloscope and photographed (Figure 3). Finally the calibration was made by firing at the completed experiment package. The thin

4.1.2 Cont.

film sensor produces a threshold signal from a particle with velocity of 5 Km/sec or greater and having a kinetic energy of 1 erg or greater. However, a particle of 1 erg energy but diameter approaching range of film thickness (velocity considerably above 5 Km/sec) will fragment or virtually explode upon impact.

4.1.3 Impact Plate Hypervelocity Plasma Data

This calibration was essentially the same as the previous one except that in this case a solid piece of metal was used for a plasma source at particle impact. The amplified sensor signal was displayed on an oscilloscope and photographed (Figure 4). The plasma created when the particle is stopped is greater than that resulting from the penetration of the thin film. A particle with kinetic energy of 0.3 ergs and velocity greater than 5 Km/sec was detectable by this sensor.

4.1.4 Acoustical Sensor

Many investigations and many results appear in the literature. It is generally agreed that the response of piezoelectric transducers is proportional to the total momentum transfer or depends upon some function of both mass and velocity, but always to obtain greater sensitivity as the velocity increases, than would be obtained by the momentum transfer. For example, McDonnell (14) finds that the sensitivity to microparticles at 2 Km/sec to 6 Km/sec is three times greater than would be estimated from low velocity calibrations.

Our calibrations show that the response increases with some function of velocity and possibly mass. The calibrations were made by using the electrostatic generator to accelerate the carbonyl iron particles. The results are shown in Figure 6. The sensor signal response (R_s), normalized to the incident particle momentum, is shown as a function of particle velocity. Below 5 Km/sec the response is quite linear with respect to the incident particle momentum. As hypervelocity threshold is reached and passed, the response over the range of data obtained from these firings is no longer linear with velocity. However, insufficient data are available to establish a function for the response. What is needed is extensive data over a large velocity range extending up to at least 20 Km/sec.

5. ELECTRONIC INSTRUMENTATION

5.1 Sensor Array Circuits

5.1.1 Qualitative Description of Four Tube Detector Array Circuits

The cosmic dust detection instrumentation consisted of four tubes oriented in different directions and each with sensors at both ends. Time-Of-Flight (TOF) measurements were possible with these two sensors. Each tube has a very thin film/grid at the front end through which the dust particles pass producing a plasma. This plasma is detected and amplified to produce a "start" signal for TOF measurements. At the back end of each tube a sensor is located to produce a "stop" signal. This same signal is also employed for energy analysis by integration of the ionization signal of the impacting particles. The "stop" and "start" signals are so named, because of their function with the electronic clock.

The TOF stop sensors of each of the four tubes are paralleled so that a particle signal detected in any tube can be processed by the same amplification circuitry. Each of the four sensor tubes employs separate start channel amplification circuitry to allow determination of which tube a hit occurs in. The TOF start and stop output signals are used for trigger purposes in the TOF measurement circuitry contained in an instrument separate from this sensor instrumentation.

The integrator circuitry provides integration of the ionization stop signal for A/D processing. The stop channel also provides an output stop trigger signal separate from the integrator output signal.

Four momentum sensors are employed and are arranged so that impact at the stop ionization sensor in any of the four sensor tubes enables momentum detection by the unified construction of the ionization TOF stop sensor and the momentum sensor. These four momentum sensors are connected in parallel and provide the signal to the single momentum amplifier (100 KC-tuned amplifier). This amplifier is arranged to provide two outputs from the momentum channel separated in gain by 20 DB. Each of these outputs is applied to separate high speed peak detectors (peak catch and stretch circuit) to enable A/D processing of the peak signals from both of these signal outputs of the momentum channel.

5.1.2 Start Channel TOF circuitry.

The start channel Time-Of-Flight (TOF) amplifier circuitry is shown in Figure 10. The high speed amplifiers for TOF START measurements are identical in configuration in channels A1 through A4 except for minor details of the -100 V sensor bias filtering, in channel A1 with respect to channels A2, A3, A4 which was done for AC common (ground) bus control purposes between channels.

The start sensor elements are biased at -100 V for purposes of charge collection. Each start amplifier input is a tightly coupled operational feedback input circuit to enable an output proportional to input signal current. The input circuit has a signal input and also a calibration input to allow calibration tests with GSE equipment and an in-flight calibration facility.

The sensor impedance is essentially capacitive only, since its shunt resistance is virtually infinite with respect to any other circuit impedances. The sensor capacitance is typically in the 12 pf to 20 pf range for a single such start sensor element.

The input signal from the sensor is in the positive direction and is thus positive phase at the output of the first feedback amplifier. This output is then injected as a current into the second of the feedback amplifiers. The output of the second amplifier drives an emitter follower (EF) with a positive phase voltage signal. This EF, in turn drives the output temperature compensated comparator/trigger stage which delivers an extremely high speed negative phased output trigger signal to the appropriate START logic circuitry in the TOF digital measurement system. Each of the four start channel outputs drive into separate logic inputs in the external TOF measurement system for purposes of tube identification of any particular hit.

5.1.3 STOP Channel TOF and B Plasma Integrator Circuitry

STOP channel Time-Of-Flight (TOF) trigger and integrator amplifier circuitry is shown in Figure 11. This amplifier channel employs the same basic philosophy of design as the start channel amplifiers but has certain exceptions that affect the exact configuration. Due to four parallel stop sensors connected in parallel at the input, the capacitance is sufficiently great so that a base feedback input circuit could not be used. Thus, a common base input stage with feedback to the emitter

5.1.3 Cont.

of the common base stage is used. This, in effect, becomes a three transistor feedback amplifier, but due to common base operation of the input stage, this added stage does not cause any phase-gain stability problems.

The amplifier has both a sensor signal input and a calibration input to allow calibration with GSE and an in-flight calibration system.

The output of the first feedback amplifier delivers a signal current output into the summing junction of the second feedback amplifier. It is necessary to obtain two output signals from this stop channel. One signal is a stop trigger output, and the other is an integrated output for A/D conversion purposes. These signals are isolated to prevent any interaction. The stop signal is fed directly to the TOF logic circuits.

The integrator capacitor peak voltage level is reached during the signal interval and is then discharged by R144, R145. This peak signal, decaying exponentially is fed to a specialized A/D converter which achieves logarithmic data expansion of lower level signals by virtue of this accurately controlled RC exponential discharge network. The RC decay time constant is 80 μ s, and is stable within $\pm 2\%$ over the thermal range from -40°C to $+70^{\circ}\text{C}$ with respect to a $+25^{\circ}\text{C}$ mean value.

5.1.4 Momentum Channel Amplifier and Peak Detector Circuitry

The momentum channel amplifier and peak detector circuitry is shown in Figure 9. The acoustical transducer (Mic) signal is fed to an amplifier employing tuned networks centered in frequency at 100 khz, the optimum sensor frequency. These tuned amplifier stages are properly unilateralized, insuring stable operation. The gain of the tuned stages is 60 db. The final amplifier stage is wide band with a gain of 20 db so that the total gain of 80 db.

The high gain output (80 DB) from the wide band amplifier is fed to the Level A peak detector circuitry. This peak catch and hold circuit is used to capture the peak level of the 100 khz damped wave and hold this level for A/D conversion.

The amplifier output immediately ahead of the 20 DB gain wide band amplifier (junction of R122 and D101) is the input signal source to the Level B peak detector

5.1.4 Cont.

circuitry. This peak detector circuitry is identical to that of Level A. It provides the Level B analog peak level output which is fed to an A/D as described for the Level A peak detector.

Four momentum sensors are employed, one in each sensor tube assembly. Each of these momentum sensors is mechanically coupled to the back surface of the sensor ionization plate. In this way the particle momentum is detected when a dust particle impacts on the stop sensor plate surface. All of these momentum sensors are connected in parallel. This provides an input to the momentum channel regardless of which tube sensor array receives a hit. Which tube receives a hit is determined by data coding using the four discrete start trigger amplifier outputs in an appropriate logic detection and storage system.

Since these four momentum sensors are paralleled, only one channel of momentum amplification is required. However, as already mentioned, two analog peak level outputs are employed, separated in gain by 20DB (the gain of the wide band output amplifier) to enable coverage of a greater dynamic signal range.

The peak detector circuits achieve extreme linearity and accuracy by employing a feedback technique for peak detection. Since simple diode-capacitor peak detection cannot be used for low level signals as the signal itself would be much less than required just to forward bias the peak detector diode.

This high accuracy method of peak detection functions as follows. The peak signal is applied to one of the inputs of a differential amplifier. The negative feedback on this amplifier is applied to the other differential input. The amplifier forward path includes a series diode-capacitor charge storage network. If the input swings positive, the amplifier will swing positive at its feedback base as the feedback action causes the signal at the anode of D107, D108 to rise sufficiently positive to provide the needed diode forward voltage so that the peak level storage capacitor can be charged through these diodes.

This charging of the peak storage capacitor causes the voltage level at the feedback base (Q107) to approach very close to the input signal level. The higher the loop gain, the more accurate this incremental follow-up

5.1.4 Cont.

between input and feedback base voltage. By virtue of the diode through which the peak storage capacitor is charged, it can be seen that when the peak is caught, if the input then swings back below its highest peak level, the feedback action will again seek to force the feedback base to follow and also swing down. This does not occur, for as the feedback attempts to force this action, the diode in series with the storage capacitor will be driven in the cut off direction. This then, in effect, traps the charge on the storage capacitor; and as a result, the feedback level at Q109 emitter will shift incrementally up virtually the exact amount the input signal shifts from its quiescent level to its most positive peak level.

The momentum system has facility for calibration signal injection from external GSE or an in-flight calibration system.

5.2 Logic, Power Supply, and Spacecraft Interface Circuits

5.2.1 Functional Description of Logic and Calibration Systems

The overall operation of the logic, starting with the output of the sensor electronics, can be divided into three parts (1) the first and second hits; (2) extra counts; and (3) telemetry. The first part describes the primary function of the experiment, i.e.: to measure four properties of the particle; the second part describes what happens if more than two hits occur during a readout period; the third part explains the telemetry operation.

If a particle has passed through the "A" film and is above the threshold, it enters the tube I.D. circuits where it identifies the tube and starts the Time of Flight measurement. Following the A plasma signal, the fast B plasma signal stops the Time of Flight measurement and stores the number of half microseconds in the Time of Flight Counter. During this time, the B analog and the mic signals have been analyzed by their respective pulse height analyzers (PHA) and stored there. When both PHA's have made their measurements, they each send an enabling pulse to the transfer pulse generator, which transfers the stored numbers to the shift register. The transfer pulse generator also pulses the shift 14 circuit which moves the first fourteen bits (the first hit) down to the second 14 bits in the shift register, thus clearing the first 14 bits for another hit. The second hit goes through the same process as the first except it is not shifted down the shift register.

5.2.1 Cont.

If more than two hits occur during a readout period, the A, B, and mic pulses enter the logic unit as before. The tube identification, the Time of Flight Counter and the mike and B PHA's all will contain a stored number. However, the transfer pulse generator has detected that it has transferred two hits already and now a transfer pulse goes only to the extra count logic. The extra count logic consists of eight bits with two bits assigned to each sensor tube. This immediately transfers the number of extra counts (up to 3) and the tube identification to two of the last eight bits of the shift register.

The spacecraft telemetry has two modes of operation as indicated by the Switch Signal: Equipment Group 1 (EG 1) and Equipment Group 2 (EG 2). Associated with each equipment group are the following signals from the spacecraft: four inhibit gates (each 9 bits long) and continuous shift pulses. The shift pulses are gated by the inhibit gates so that at each readout, four nine bit words are shifted serially into the telemetry system.

The interface circuits also supply resetting commands to clear the PHA's and inhibit signals to prevent any transfer of data during readout of old data. The output circuits which are designed to match the telemetry loads are also located here.

The system also contains an in-flight calibration circuit activated by ground command. When the calibrate signal is received by the experiment, a series of electrical signals are generated and fed to the sensors in the detector array simulating the detection of a dust particle. Once the calibrate sequence is initiated, a set of signals is supplied to each tube in the following order: +Y, +X, -X, +Z. The signals are supplied to one tube per readout, so that a complete calibration takes four readout periods. During the calibration sequence, the bias potential on each A plasma sensor is sampled and the information stored in the extra count binaries. This is done in order to determine whether the thin film and grid are shorted.

Spacecraft power consists of a widely varying battery voltage. The power supply accepts this voltage and runs it through a preregulator. The regulated output is then used to drive a converter which, in turn, supplies four regulators (+3, +7 and +12). An unregulated -100 volts supply is also generated to supply the sensor films.

5.2.2 OGO III Dust Particle Standard Logic Circuits

5.2.2.1 General

The major portion of the logic system consists of standard Modules. The basic design of these circuits is presented in the following sections. The individual component values are not given because they vary with function, loading, etc.

5.2.2.2 One Shot Multivibrator (Figure 24a)

The one shot multivibrator circuit depicted in Figure 24a is a standard monostable configuration. The one shot driven by the start and stop triggers have to be very fast, and the resistor and capacitor values for these modules are different in order to achieve the required high speed pulse.

5.2.2.3 Bistable Multivibrator (Figure 24b)

This module is a basic Eccles-Jordan Multivibrator providing two outputs. There are several minor variations made in this module depending on its use. However, the following basic operational functions hold for each module: A negative pulse on the set input causes output Q_1 to be positive; a negative pulse on the reset input causes Q_2 to be positive; a negative pulse on the toggle input causes the flip-flop to change states.

5.2.2.4 NAND Logic Gates (Figure 24c)

Given the following logic statements,

$$1. \text{ Output} = \overline{(A) \cdot (B) \cdot (C) \cdot (D) \cdot (E)}$$

$$2. \text{ Output} = \overline{A} + \overline{B} + \overline{C} + \overline{D} + \overline{E}$$

equation (1) states that the output will be in the "0" logic state when all the inputs are 1's, and equation (2) is the alternative statement that the output is in the "1" logic state if either or all of the inputs are 0's.

When any one of the inputs is at ground potential, the base of the first transistor is below the conduction point and the transistor is cut off. Therefore, there is no base drive to the second transistor, which is in a common emitter configuration, and the second transistor is cut off. The output collector sits at the B supply voltage.

5.2.2.4 Cont.

When all the inputs are positive with respect to the conduction point of the first transistor, the diodes in the input are back biased, and base drive is supplied to the first transistor through the base resistor from B plus. This saturates the transistor causing emitter current to flow, which, in turn, supplies base drive to the second transistor. This causes the second transistor to saturate, bringing the collector down from the B supply to the saturation voltage of the transistor, nominally, plus two tenths (0.2) of a volt positive with respect to ground. This step function, which is a negative going step, is the logic 0. When one of the inputs is grounded, it causes the output collector to return to the B supply creating a positive going step function, which is the logic 1.

This parallel NAND gate is identical in logic function to the NAND GATE. The difference is that the output of this module does not have its own load resistor but has its output connected in parallel to some other module, so that they share a load resistor. Two modules which are so connected essentially have their outputs "OR"ed together:

$$\text{Output} = (\bar{A}_1 + \bar{B}_1 + \bar{C}_1 \dots) (\bar{A}_2 + \bar{B}_2 + \bar{C}_2 \dots).$$

5.2.2.5 Ladder Driver (Figure 24d)

The ladder driver module is used in Mic Pulse Height and B Pulse Height Analyzers as a means of supplying different levels of voltage for comparison in the comparators that are part of the Pulse Height Analyzers.

When any of the inputs are at ground potential, the base of Q_1 is below the point of conduction and the transistor is cut off. Since Q_1 does not have a collector load resistor of its own, the collector of Q_1 is connected to an external resistor that is part of the ladder network. With Q_1 cut off, the collector sits at the supply voltage.

When all of the inputs are positive with respect to the conduction point of Q_1 , the input diodes (CR1, CR2, CR3) are back biased and base drive current flows through R3 saturating Q_1 causing the collector of the transistor Q_1 to sit at the saturation voltage of the transistor, nominally plus 0.2 volts.

5.2.2.5 Cont.

Because of the nature of the ladder network, the two (2) states of Q_1 (cut off or saturated) have the effect of switching the external collector resistor in or out of the ladder network circuit changing the voltage level in the ladder itself which in turn supplies the reference voltages used by the comparator to make comparisons with the incoming Mike or B signal.

5.2.2.6 Shift Pulse, TOF, and Transfer Pulse Drivers (Figure 24e)

These three modules are the interface driving circuits driving the appropriate data binaries in the shift register.

The TOF module supplies a negative pulse from one of two inputs. The two inputs are isolated by means of the diodes CR1 and CR2. Normally all transistors are cut off; a positive going waveform on either input will saturate all three transistors and produce a negative output pulse.

The shift pulse driver is a non-inverting module which produces negative output pulses. Normally all transistors are cut off. A negative pulse at the input saturates all three stages.

The transfer pulse driver is a non-inverting module which produces positive going pulses. Normally Q_1 and Q_2 are cut off. A positive pulse at the input saturates both transistors and produces a positive output pulse.

5.2.2.7 TOF and Shift Pulse Clocks (Figure 24f)

The 2 Mhz clock is an astable multivibrator whose frequency is controlled by two external capacitors. One capacitor is placed across Pins 8 and 12; the other capacitor is placed across Pins 6 and 11. RT1 and RT2 are sensors to stabilize the frequency in the presence of changing temperatures. The control lead is normally below zero volts and this stops the clock and holds Q_2 cut off and Q_1 saturated. When the control goes above +0.6 volts the clock starts with the saturation of Q_2 .

The 64 khz clock is also an astable multivibrator whose operation is identical to the 2 MC clock above. However, Q_3 in this module acts as an inverter and isolator for the clock output from Q_2 .

5.2.2.8 Comparator (Figure 24g)

This module consists of a difference amplifier followed by a stage of gain. The final output is fed back to increase the speed of switching. Q_1 contains a matched transistor pair which acts as the difference amplifier. An analog voltage is applied to input 1 and a staircase of voltage is applied to input 2. Prior to the appearance of the analog voltage the d-c biases are such that the right hand side of Q_1 is conducting; the resulting voltage drop across R_5 biases the left hand side of Q_1 to cut off. There will be a drop across R_2 so that the base of Q_2 is well below the emitter and Q_2 is saturated and the output is at a 1 state. The output is fed back through R_4 .

When an analog voltage on input 1 crosses threshold then Q_1 - left hand side - will conduct and the voltage across R_5 will increase and cut off the right hand side of Q_1 . The collector of Q_1 rises to $B+$ and cuts off Q_2 . The output falls to 0 and removes the feedback voltage which further drives the right hand side of Q_1 to cut off. In the system, the falling output voltage starts a staircase on input 2 and when the staircase equals the analog voltage the module switches back to its original state and stops the staircase. After the analog voltage returns to 0 the staircase is removed.

5.2.3 Logic Circuit Design Criteria

Reliability of circuits has been of prime importance in the design of this experiment. A number of basic tenets for achieving this goal apply:

1. Employ high quality, reliable components
2. Design with proper derating factors including deterioration of parameters
3. Manufacture with high workmanship standards including close supervision and inspection.

The Quality Assurance section of this report describes the precautions taken in an effort to secure reliable components and workmanship. The section describes the electrical design techniques.

All resistors are operated at less than one half of their rated power dissipation. The use of low power circuits has resulted in dissipation of less than 1 milliwatt for most of the resistors in the logic circuits.

5.2.3 Cont.

All capacitors are operated at less than 1/3 of rated voltage. The use of low voltage power supplies eases this problem considerably.

The use of low power, low voltage circuits has permitted deratings on semiconductor parameters of 2:1 and better. For example, the worst case of peak inverse voltage for four diodes occurs in the power supply and here the derating factor is 4:1. Elsewhere in the electronics the derating factor is higher.

Consistent with this aim for reliable circuits, worst case parameter values are incorporated into the design. Worst case parameters as given by manufacturers are derated even further; where no parameter value is given, tests are run to determine worst case values. In particular, digital circuits are sensitive to the value of saturated beta of the transistor; here the minimum low temperature value given by the manufacturer is divided by two and this value used in all calculations for circuit design. In this way a safety factor for aging is added. All circuit designs follow this approach and as a typical example of this technique, the following example of the design of the Nand gate is included.

Refer to Figure 24c for the schematic and observe that:

R1 = 160K
R2 = 43K
R3 = 47K
R4 = 18K

The specifications on Q_1 and Q_2 are:

1. Saturated beta at -55°C and 150 μa collector current shall be 20 or greater.
2. V_{ce} (saturated at 150 μa collector current and $+125^{\circ}\text{C}$ shall be less than 0.2v.
3. V_{be} (saturated conditions) for 150 μa collector current and -55°C shall be less than 0.8 volts.

Although these transistors will not be required to operate at -55°C or at $+125^{\circ}\text{C}$, the design has been taken at these limits and, in addition, the design includes five loads even though the system nowhere includes five

5.2.3 Cont.

loads. Let us, therefore, examine this Nand with 5 loads at -55°C . If this Nand is loaded with 5 Nands, then each Nand load will drive a load current into the Q_2 collector when the Nand output is at 0. This load current will be

$$I = \frac{3\text{v} - \text{collector saturation voltage} - \text{diode drop}}{160\text{K}}$$

let: collector saturation voltage = 0.1 v

diode drop = 0.6 v

$$I = \frac{3 - 0.1 - 0.6}{160\text{K}} = 14.4 \mu\text{a}$$

Five such loads will be 72 μa . However, we next examined five flip flop loads and found that this produced a greater momentary load. To trip a flip flop 43 μa must be drawn into Q_2 for each flip flop. Thus, 5 loads of this type equal a total load of $5 \times 43 = 215 \mu\text{a}$. When a Nand output goes to a 0 and trips 5 flip flops, the total current in Q_2 collector will be 215 μa plus its own saturation current. The collector saturation current is

$$\frac{3 - V_{ce} \text{ (saturated)}}{18\text{K}} = \frac{3 - 0.1}{18\text{K}} = 161 \mu\text{a}.$$

and total collector current = $215 + 161 = 376 \mu\text{a}$.

At -55°C the design must be such that Q_2 will saturate with this load. We now start at the front end of this circuit and calculate what drive is available at the base of Q_2 .

Assume that all Nand inputs are at 1 and the three diodes have just been back biased. Now R_1 supplies base drive to Q_1 which in turn supplies base drive to Q_2 . Worst case values of V_{be} for Q_1 and Q_2 are 0.8v. (but let us use 0.9v for additional safety factor). Thus, the base of Q_2 is at 0.9v and therefore the base of Q_1 is at 1.8 volts. The voltage across R_1 is $3 - 1.8 = 1.2$ volts. The current through R_1 , which is also the base drive for Q_1 is

$$\frac{1.2}{160\text{K}} = 7.5 \mu\text{a}.$$

5.2.3 Cont.

The beta of Q_1 for these conditions is no less than 14. However, we will use a beta of 7 to take care of aging. The collector current of Q_1 is

$$\text{base current} \times \text{beta} = 7.5 \times 7 = 52.5 \mu\text{a}.$$

The emitter current of Q_1 is the collector current + the base to emitter current and is $52.5 + 7.5 = 60 \mu\text{a}$. The 47K resistor with a drop of 0.9 volts across it loses $19 \mu\text{a}$ so that $60 - 19 = 41 \mu\text{a}$ are available at the base of Q_2 . The beta of Q_2 at $150 \mu\text{a}$ and 55°C is specified at 20. Divide this by 2 and use a beta of 10 (this value is safe because more than $150 \mu\text{a}$ will be flowing through Q_2).

The base drive is $41 \mu\text{a}$; the beta is 10 and thus the collector can saturate with $410 \mu\text{a}$ of current. But we have already shown that the maximum collector current is only 376 so that the design is indeed a worst case design.

At $+125^\circ\text{C}$ the worst case condition is when all inputs to the Nand are at 0 and we must examine the input to see if Q_1 and Q_2 will start to conduct: At this temperature collector saturation voltage is less than 0.3v. The diode drop is less than 0.5v so that the anode of a diode is $0.3 + 0.5 = 0.8\text{v}$. A worst case value for a base emitter junction at $+125^\circ\text{C}$ is 0.5 volts so that the base of Q_1 must rise to 1.0 volts for conduction to start but our calculations show that it can never exceed 0.8v under worst case conditions. Leakage measurements are made on all transistors at $+125^\circ\text{C}$ and the voltage drops due to leakage are negligible. High leakage is a cause for rejection of a transistor during heat soak.

Not all circuits are designed for 5 loads over so large a temperature range. However, all designs exceed the expected temperature range of operation and all designs include the safety factors demonstrated above. In this way the utmost in reliability has been included in the Dust Particle Measurement Instrument for OGO III.

5.2.4 Qualitative Description of A/D, Coincidence and Interface Circuitry

A qualitative description of the performance of the logic circuitry assumes that initially the telemetry system has just completed a readout of the experiment

5.2.4 Cont.

and all the multivibrators are in their initial states. In the following discussion, a 1 or up state corresponds to +3v for a gate or driver and to +2.4v for a multivibrator. A 0 or down state corresponds to +0.2v. A detectable hit now occurs and signals from the sensor electronics appear at J201 (Figure 12A). The waveforms and timing of these signals appear on Figure 12B,C. The A pulse lines are J201-1, J201-2, J201-3 and J201-5; one line from each sensor. These signals go to Z236, Z235, Z233, and Z231, respectively. These modules are one-shots and a pulse will appear on only one of the four inputs - this pulse then identifies the sensor where the input occurred. The output waveforms of these modules is shown in Figure 12C (a) and (b). The one shot outputs are coded into the two Nand gates contained in Z234 in the four following ways:

1. Neither gate is enabled.
2. One gate is enabled.
3. The other gate is enabled
4. Both gates enabled.

These gates will be enabled for 1200 μ s and the transfer of data occurs at 450 μ s so that the tube in which the hit occurs produces a unique output.

The negative-going pulse of each module is connected to the inputs of Z232, an AND gate, so that at the output of Z232 it appears again. This pulse drives Z252 which is a flip flop with one set line and two reset lines. On the leading/falling edge of this pulse, Q_2 of Z252 sets from a 0.2v level to +2.1v and this is coupled to Z253. (See Figure 18). Z253 is an astable multivibrator set at 2 MC. The rising voltage on the input immediately produces the first falling clock pulse (square waves) at Q_2 . This square wave drives the countdown chain consisting of six flip flops - Z257, Z254, Z258, Z255, Z259, and Z263. These six flip flops can count up to 64 pulses for a total T.O.F. of 31-1/2 μ s before being reset to their zero states.

The B plasma pulse resets Z252, the clock control module, thus stopping the clock. The time between the A and B pulse is stored in binary form in the six flip flops of the countdown chain. If, for any reason, a B pulse does not appear then the clock runs freely and fills the countdown chain. The 64th pulse will restore the flip flops to all zeros and at this time Q_1 of Z263 will fall from +2.4v to 0.2v. This falling edge drives a reset line of Z252 and this restores Z252- Q_2 to 0 and

5.2.4 Cont.

stops the clock. Propagation delays down the countdown chain may be such that the clock adds a count of one to the chain before it is stopped. In order to overcome this difficulty the falling edge at Z263-Q₁ is inverted by Z256 and a rising edge at Z256-Q₂ feeds Z251. This module is a driver which resets all the flip flops in the chain. This stops the clock and resets the chain to read a count of zero. This count is used to indicate an overrun condition - i.e., the time between A and B pulses was something greater than 31-1/2 μ s. There is no ambiguity because the design of the clock and clock control is such that even if A and B occurred simultaneously, the count in the chain would be one pulse.

In addition, the signal from Z232-Q₂ (Figure 17) also feeds to Z251. The trailing/rising edge of the signal will occur 1200 μ s after the A pulse and this rising edge also produces a negative going reset pulse from the driver Z251. (See Figure 18). This resets all the flip flops if they have not already been reset by an overrun action. The resetting action occurs well after the data stored in the countdown chain has been transferred out.

The B plasma analog signal is fed through the upper unit to the Power Supply Unit (Figure 12A) from which it goes to the comparator module Z121 (Figure 14A). The potentiometer R121 has been adjusted so if the pulse is greater than 50 mv, then the output of Z121, will change state (see BPHA waveforms Figure 14B,a). The leading/falling edge accomplishes two functions:

1. Z133, a 900 μ s one shot is started. (Figure 14B,b).
2. The negative transistion is inverted by Z123, a gate, and the resulting positive pulse is fed to Z126 to start this 64 KC clock (Figure 14B,c).

Z133-Q₂ supplies a positive voltage to the transfer pulse generator to permit a transfer pulse to occur if the Mic PHA also supplies a similar positive voltage. The falling edge of this pulse will later reset the BPHA flip flops after the data have been transferred out.

The 64 KC clock (Z126), now started, sends out a square wave to the two inputs of one half of the NAND gate in Z132; the two inputs of the other half are at the moment enabled (1 state). The inverted clock pulses now drive Z127, Z128 and Z131 - three flip flops are used to generate the non-linear staircase. Z130, Z124, Z125 and Z122 contain transistor switches and

5.2.4 Cont.

networks to produce the eight level staircase of voltage which is fed to the comparator Z121 (see Figure 14B,c). For each clock pulse the staircase steps up one step until the staircase voltage equals or exceeds the B analog signal. At this time the comparator (Z121) returns to its original state of +3v. This removes the positive voltage from the clock and stops it so that a digital number equivalent to the staircase step remains in the countdown chain. The staircase and flip flops will be reset by the falling edge of the one shot Z133.

If the B analog signal is above 5v, then the highest step, the seventh, will not cause the comparator to reset because this step is too small. The clock will not be stopped and an eighth clock pulse will then reset the chain and staircase to zero in the following manner. The output of the last flip flop in the chain (Z131) will now, for the first time, go to zero. This falling edge fires the 15 ms one shot Z129. The output goes from +3v to 0.2v, and this voltage is fed to Z132. Z132 is the gate which passes the clock pulses to the chain. When the one shot fires, (Z129), Z132 blocks any more pulses stopping the flip flop chain in its zero state. Thus, the zero state of the BPHA is reserved to indicate that the input B signal was above 5.0v. After the eighth clock pulse has reset the chain and staircase, the clock is reset as follows: C121 and R122 (Figure 14A) have a time constant such that, in less than 350 μ s, the varying voltage falls below the sustaining voltage, and the clock stops. The 15 ms one shot Z129 returns to its initial state 15 ms after the clock stops. The BPHA will now be ready for the next hit.

There are two signal outputs from the mic amplifier system. The most sensitive signal is the Mic Analog Low signal which is fed through J201-18 to the comparator Z202 (Figure 21A). The other signal, Mic Analog High, is derived from a point in the amplifier at which the gain is 1/10 that of the complete amplifier. This signal is fed through J201-17 to a second comparator, Z201 (Figure 21A). The relationship between these two signals is as follows:

For extremely small inputs to the sensor amplifiers (low momentum particles), both signals will be below 0.5v (comparator threshold). As the particle momentum increases, the Mic Low signal increases to a saturation value of 5.0v while the Mic High signal remains at 0.5v.

5.2.4 Cont.

Further increases in particle momentum cause the Mic High signal to increase from its threshold value of 0.5v until it also reaches a saturation voltage of 5.0v.

As the Mic Low signal increases to 0.5v it triggers the comparator Z202, whose output falls (Figure 21B,a) accomplishing the following three functions:

1. The output signal triggers Z214 (Figure 21B,e) the trailing edge of which initiates the transfer pulse.
2. The signal from Z214-Q₁ triggers the one shot Z213 (Figures 21A; 21B,f) which resets the flip flops Z207, Z208 and Z209 (Figure 21A) at the end of 100 ms.
3. The output signal also feeds a NAND gate, Z205, which produces a positive going output pulse.

The output of Z205 is coupled through C205 and R203 to Z204, the 64KC clock (see Figure 21B,b&c). The clock drives three flip flops (Z207, Z208, and Z209) which are arranged in a countdown chain. Z207-Q₂ and Z208-Q₂ drive Z206 which in turn drives Z203. Z206 and Z203 contain transistor drivers and resistor networks so that the output of Z203 produces a three step staircase which is fed to the comparator Z202 (Figure 21A and 21B,d).

Three cases are now obtained from the Mic amplifier output signal lines. The functioning of the Mic PHA for each case is explained below:

Case I: When the Mic amplifier output signal is such that only the Mic Low signal is affected, if one of the first three staircase steps is greater than or equal to the Mic Low signal, the comparator Z202-Q₂ will return to +3v when this step is reached and in doing so, will restore Z204 to initial conditions, stopping the clock. The binary number stored in Z207, Z208 and Z209 will be between 1 and 3 and will be transferred out later. The staircase will hold its position until reset.

Case II: Case II is that case where the Mic Low signal is saturated (5.0v) and the Mic High signal is varying with the momentum of the particle. It is pertinent at this time to examine Z210 and Z205.

5.2.4 Cont.

Z210 is a module holding two parallel NAND gates whose outputs are tied together and also tied to the output of Z205. Thus, there are three gates whose outputs are "OR"ed together to control the clock. During the first three staircase steps, Z205 is in control, and its output being UP started the clock; the other two outputs are also UP. When the fourth clock pulse occurs and sets Z207 and Z208 back to 0, it also sets the staircase to zero and places a 1 in Z209. The binary count is now 4. Z209-Q₁ now is at a 1 and is tied to two inputs of Z210. This releases one of the NANDS in Z210 so that it is controlled by the output of comparator Z201 which feeds another input of Z210. Since the first comparator Z202 could not make comparison during the first three steps, the input Mic signal must have reached 5.0 volts on Mic Low, and the second comparator Z201 is now examining the Mic High signal. The staircase is fed to the ladder input of Z201 from the ladder network Z203. Although the staircase is at its zero step, the staircase to Z201 is prebiased so that the zero step combines with the next three steps to form a total of four separate windows. The staircase can exceed the input Mic High signal in Z201 at any of the four possible levels. When this does occur, the output of Z201 returns from zero volts to three volts. Then the NAND gate in Z210, which is under the control of Z201, has its output go to 0.2v pulling the common output of Z205 and Z210 to this level. The common output of Z205 and Z210 is coupled through C205 and R203 to stop the clock at the proper time leaving a binary count in the chain and the staircase in the same position. This datum will later be transferred out and the flip flops reset by Z213-Q₂.

Case III. If a micrometeorite of large enough momentum is detected, then both Mic High and Mic Low will be signals of 5.0 volts, and none of the seven steps will make comparison. This leaves a binary seven in the chain, and the next clock pulse will restore the chain to zero count. Q₁ of Z209 falls to zero and triggers Z211, a 12 ms one shot. The output at Q₂ of Z211 controls the other half of Z210 so that when it goes from 0.2v to +2.4v the output of Z210 falls to zero and stops the clock. The count left in the chain to be transferred out will be a zero, a non-ambiguous count indicating a value of momentum higher than the highest staircase value. During the 12 ms that the one shot Z211 is holding the clock off, the Mic signals are decaying back to zero and the staircase is at a zero state. When the one shot

5.2.4 Cont.

releases, the common gate line at Z205 may rise and start the clock again if the Mic signals are still above threshold. The staircase then starts again, and will catch the signal at some level causing the comparator to reset and stop the clock. No transfer pulse occurs since the output of Z202 rises to a 1 state and, thus, does not trigger Z214. However, a binary count is stored in the countdown chain and this chain will be reset to zero when the 100 ms one shot (Z213) recovers.

The system has now stored, or is holding, the following information:

1. Tube identification coded on Z234.
2. T.O.F. held in six flip flops: Z257, Z254, Z258, Z255, Z259 and Z263.
3. B information held in three flip flops: Z127, Z128, and Z131.
4. Mic information held in three flip flops: Z207, Z208 and Z209.

Each of the above flip flops has its output tied to separate NAND gates. If the flip flop is in a 1 state, the gate is enabled, and a pulse can pass through. The gates are located as follows:

1. The two Tube I.D. gates are in the Dual NAND Z234. (Figure 17).
2. The six gates for T.O.F. are in Dual NANDS Z260, Z261 and Z262 (Figure 18).
3. The three BPHA gates are 1/2 of Z132 and Z134 (Figure 14A).
4. The three Mic PHA gates are Z215 and Z212 (Figure 21A).

It has already been noted that Z133-Q₂ in the BPHA supplies an enabling voltage for the transfer pulse. This voltage is fed to two inputs of (Figure 20) Z224 which is a dual NAND with a number of inhibiting voltages. If no inhibits are present and the two inputs are in a 1 state due to Z133, Z214, the 450 μ s one shot (Figure 21A) is started by the incoming Mic signals and Q₂ of Z214 feeds two more inputs of (Figure 20) Z224. The output of Z224 is normally at +3 volts; it falls to zero when Z214 triggers and returns to +3 when Z214 recovers at the end of 450 μ s. This return to +3v is coupled to the input of Z225 and produces a positive going pulse approximately 5 μ s wide at the output. This is the data transfer pulse, and it feeds all the gates mentioned above.

5.2.4 Cont.

When the transfer pulse appears at a gate, if the other input is in a 1 state, then a negative going pulse appears at the output of that gate - otherwise no pulse is generated. There are fourteen wires leaving the NAND gates - each one of which goes to a set line of a flip flop in the 36 bit storage register (Figure 22). This shift register will eventually hold all the data that are to be read out. If a set line receives a negative pulse as a result of a 1 in a data flip flop, a 1 is placed in that module. The following Table 2 shows the modules into which the data are transferred, as well as the type of data. The sequence starting from top is also the readout sequence.

<u>Data Transferred to Module</u>	<u>Data</u>	<u>Data Shifted to Module</u>
Z293	Most signif. tube ID bit	Z276
Z294	Least signif. tube ID bit	Z277
Z295	Most signif. T.O.F. bit	Z281
Z300		Z282
Z299		Z283
Z298		Z284
Z297		Z285
Z296	Least signif. T.O.F. bit	Z290
Z301	Most signif. BPHA bit	Z289
Z302		Z288
Z303	Least signif. BPHA bit	Z287
Z304	Most signif. Mic PHA bit	Z286
Z305		Z291
Z306	Least signif. Mic PHA bit	Z292

Table 2

Table 3 shows the Tube I.D. Code:

	<u>Most Significant Tube I.D. Bit</u>	<u>Least Significant Tube I.D. Bit</u>
Tube 1	0	0
Tube 2	0	1
Tube 3	1	0
Tube 4	1	1

Table 3

5.2.4 Cont.

The Transfer Pulse Driver Z225 (Figure 20) also feeds its pulse to Z222. Z221 and Z222 are two flip flops in a countdown chain and they count the number of transfer pulses that occur. The actual count occurs on the trailing edge of each transfer pulse.

The trailing edge of the transfer pulse toggles Z222 to a 0 and this falling voltage at Z222-Q₂ toggles Z106 (Figure 13). Z106-Q₁ goes to a 1 and, as in the Mic PHA and BPHA, this starts a 64KC clock, Z102. Each rising edge of the square wave from the output of Z102 is inverted by Z103 and each falling edge at the output of Z103 produces a negative pulse at the output of Z104. These pulses are counted in a chain of flip flops composed of Z105, Z108, Z109 and Z112.

When the count reaches 14 then Z108-Q₁, Z109-Q₁ and Z112-Q₁ are all in a 1 state for the first time. These signals drive Z107, a NAND gate, and at the count of 14 a negative pulse appears at its output. This triggers the 20 μ s one shot Z111. Z11-Q₂ falls from +3v to +0.2v for 20 μ s and then returns to +3v. The falling edge resets Z106-Q₁ to a 0 and stops the clock. Z111-Q₁ produces a positive pulse 20 μ s wide. The rising edge is inverted by a Z110, a DRIVER, and the negative output pulse from Z110 drives each flip flop in the countdown chain and resets them to their zero states.

Fourteen pulses have thus been generated at the output of Z104, and these pulses are the shift pulses for the entire 36 Bit Shift Register. At the end of 14 pulses, the data stored in the first 14 elements have been moved into the next 14 elements. The first 14 elements all now have zeroes in them and the data appear as shown in Table 5, in the right hand column.

After the various resetting actions have occurred, the system is ready for another hit. The longest dead time is the 100 ms reset one shot in the MIC PHA which allows the mic signals to return to their zero states. If another hit occurs prior to readout, the action of the various data taking circuits is identical to that described for the first hit. However, the transfer pulse, after transferring the data to the first 14 shift register elements again toggles Z222 at the trailing edge of the transfer pulse. Z222-Q₁ now goes from a 1 to a 0 and this toggles Z221. A count of 2 is now in the chain composed of Z221 and Z222. Since Z222-Q₂ produced a rising voltage, this time, it does not toggle Z106. Thus the 64KC clock Z102 will not start

5.2.4 Cont.

and there will not be another shift of 14 to the shift register. Data for two hits will thus be stored in the upper 28 elements. Lastly, Z221-Q₂ has just changed from a 1 to a 0 and Z221-Q₁ has changed from a 0 to a 1.

It will be recalled that Z224 is a dual module and the production of a transfer pulse by the half of Z224 which drives Z225-5 has been discussed. Z221-Q₂ until now was in a 1 state and enabled this half of the module. However, this voltage, at the end of two transfer pulses has gone to a 0 and prevents any further transfer pulses from occurring. If anymore hits occur, then the PHA's, T.O.F. and Tube I.D. circuits will operate as before, but since no transfer pulse can occur, these data do not get into the shift register and the internal resets will eventually wipe these data out.

The system does have the capability of storing, for each sensor tube, up to a maximum of three extra hits (i.e., hits which occur after the first two hits). Although no further transfer pulses can appear at Z224-12 because Z221-Q₂ is in a 0 state and inhibits this half of the NAND; Z221-5 is now in a 1 state and for the first time no longer inhibits the other half of Z224. Thus, when additional impacts occur the leading edge of Z214-Q₂ produces a negative going pulse at Z224 and drives Z226 at its input. Z226 produces a positive 90 μ s pulse and at the end of 90 μ s this pulse causes another 90 μ s pulse at Z223.

The following Table lists the modules involved in the Extra Count Circuits and shows to which sensor they correspond.

<u>A1 Circuits</u>	<u>A2 Circuits</u>	<u>A3 Circuits</u>	<u>A4 Circuits</u>
Z241	Z242	Z243	Z244
Z245	Z246	Z247	Z248
Z271	Z273	Z275	Z278
Z272	Z274	Z280	Z279

Table 4

Figure 19B and the following explanation shows how the A1 pulses produce extra counts. The explanation is identical for the other sensors. When an A1 pulse occurs, Z236 (Figure 17) produces a positive going pulse 1200 μ s wide which enables Z245 (Figure 19A). (If the hit occurred in another sensor, a similar enabling pulse would be generated by Z231, or Z233 or Z235 to drive the circuits corresponding to that sensor). The following

5.2.4 Cont.

explanation covers only the case in which an enabling pulse is present for A1 since, if there is no enabling pulse present, the pulses from Z226 and Z223 (Figure 20) would not get through the gates. Thus when an enabling pulse is present for A1, the pulse from Z226-Q₂ passes through Z245, is inverted, and sets Z271-Q₁ (Figure 22) to a 1. Z271-Q₂ falls from 1 to 0 triggering Z241, a 250 μ s one shot. Z241-Q₁ produces a negative going pulse which inhibits one half of Z245 so that when the positive pulse from Z223-Q₂ appears at an input of Z245, it does not get through. A single extra hit has now been counted. A 1 has been placed in Z271 while Z272 is still in a zero state. Z271 and Z272 are part of the 36 Bit Shift register, and if readout occurred, the data would indicate one extra hit in sensor A1.

If a second hit in sensor A1 occurs prior to readout, the pulse from Z226-Q₂ is inverted going through Z246 and tries to set Z271 to a 1. Since Z271 is already at a 1, there is no change in its state. Z241 does not trigger, and Z271-Q₁ and Z272-Q₂ are both in 1 states so that the pulse from Z223-Q₂ goes through Z245 and appears as a negative pulse at Z245-Q₂. This negative pulse resets Z271 to a 0 and sets Z272 to a 1 making the stored binary count 2.

If a third hit in sensor A1 occurs prior to readout, the pulse from Z226-Q₂ sets Z271 to a 1. Z271-Q₂ falls from 1 to 0 which triggers Z241-Q₁ to produce an inhibit at an input of Z245. In addition, Z272-Q₂ is also at 0 so that Z272 and Z241 both inhibit the pulse from Z223-Q₂ and prevent it from getting through to Z245. Z271-Q₁ and Z272-Q₁ are now both at 1, and the binary count is a 3.

If a fourth hit or any additional hits occurs in sensor A1 prior to readout, then Z226-Q₂ causes a set pulse at Z271 which has no effect since this module is already set to a 1. Z241 does not trigger again. The pulse from Z223-Q₂ does not get through Z245-Q₂ because Z272-Q₂ is at a 0. Thus, any additional extra hit causes no change in the stored 3. After readout, Z271 and Z272, as well as all other elements in the register, will be in a 0 state, and the process can begin again with new data.

Extra hits, if they occurred, are stored in Z271 through Z275 and Z278 through Z280. The first hit data will be stored in the modules listed on the right in Table 4 and the second hit data will be stored in the

5.2.4 Cont.

modules listed on the left hand side of Table 4. The final output of the 36 bit shift register appears at Z278-Q₁ and then goes to the inputs of Z146 and Z147. These two modules are output switches and produce the signals for the telemetry system. A nonreturn to zero (NRZ) is employed.

The experiment/spacecraft interface can now be described. As far as the experiment is concerned, there are two separate telemetry systems. They are called Equipment Group No. 1 (EG1) and Equipment Group No. 2 (EG2). These groups are non-synchronous; they supply the experiment with continuous shift pulses. When readout is required, the experiment also receives four gates. A DC voltage having two states, called Switch Signal, is supplied to the experiment, and its level indicates which EG is to be used. All of these signals are fed into Z151 (Figure 16) a resistor-capacitor network which shifts the levels of these signals so that they can be used by the 3-volt logic modules. Z151 also supplies the proper loads to the telemetry system.

The Switch Signal is fed to Z145 which produces a 1 and a 0 at its two outputs in order to gate all incoming and outgoing signals so that the proper EG is operating the experiment. When the Switch Signal is in the 0 state, EG1 is employed; when the Switch Signal is in the 1 state, EG2 is employed.

Z141 through Z144 (Figure 16) are Dual NANDS which select the gates that are to operate the readout. One half of Z141 accepts subcommutator word (SCW) 4 from EG1; the other half accepts SCW 4 from EG2. Z142 accepts SCW 5 from EG1 and EG2; Z143 accepts SCW 6 from EG1 and EG2, and Z144 accepts SCW 7 from EG1 and EG2. Each Dual NAND has its two outputs tied together so that each module forms an OR gate.

If the Switch Signal is in its 0 state, one output of Z145 will be a 1 and the other will be a 0. Since 0 inhibits a NAND gate, the 0 output of Z145 will inhibit all EG2 gates since it is applied to inputs of Z144, Z143, Z142, and Z141. The EG1 gates, however, will pass through inverted as they occur. Each EG1 gate is a positive pulse 9 shift pulses wide. Thus, the outputs of Z141 through Z144 are negative going pulses, and all four are applied to the gate Z150. The four SCW appear as four positive pulses serially on a single wire at the output of Z150.

5.2.4 Cont.

The output of Z150 drives both sides of Z101. Z101 is a Dual NAND one side of which receives shift pulses (positive going) from EG1 and the other side of which receives shift pulses from EG2. The two outputs of Z145 also feed each side of this module so that one EG group is inhibited - in this case, the output of Z145 which is 0 inhibits the shift pulses from EG2. Thus, as each positive going SCW appears at the output of Z150 and is applied to Z101, nine EG1 shift pulses pass through Z101. Z101 and Z103 also form an OR gate. A total of 36 negative going pulses appear at the outputs of Z101. These 36 pulses drive Z104 and appear as negative going pulses at the output. The four groups of nine pulses now drive the shift register and empty it of data leaving all elements in the 0 state. As noted before, the output of 36 Bit Shift Register is applied to Z146 and Z147. Output 1 of Z145 ("0") is applied to an input of Z147 holding its output, which drives EG2, at a 0 state. Output 2 of Z145 ("1") is applied to an input of Z146 and opens the EG1 data line. The four gates from Z150 are also applied to Z146 and Z147 so that, when a SCW is not present; the output line will be in a 0 state, which is an interface requirement.

If the Switch Signal is in a 1 state, the output states of Z145 are reversed so that now the EG2 shift pulses and inhibit gates pass through the system and the output of Z147 reads out the data while the output of Z146 is held at 0. It is to be noted that the 36 shift pulses are counted by Z105, Z108, Z109 and Z112 just as they were during the 14 bit shift after the first hit. At the end of the first 14 pulses, the automatic reset of these flip flops occurs and likewise at the end of the second 14. When readout is complete there will be a count of 8 left in the chain. However, the output of Z144 is a negative going pulse and drives the input of Z110. Thus, on the trailing/rising edge of this, the last SCW pulse, the Z110 output produces a negative pulse to reset the countdown chain.

All of the data have been read out and the experiment is now ready to accept new data.

There are two other functions to be described:

a. Inhibit During Readout

During readout data cannot be accepted into the system because attempting to transfer information

5.2.4 Cont.

into the 36 bit shift register while it is shifting would make both old and new data meaningless. To prevent read in during read-out, a 0 or negative going pulse is applied to two inputs of Z224. Z224 is the NAND module that passes the transfer pulse, and by holding two inputs at 0, the entire gate is inhibited. If a hit does occur, the various internal resetting actions will take place to wipe out this data, but no transfer of data is allowed to occur.

It remains then to generate a 0 during the readout interval and a 1 otherwise. This is done by Z148. Z148-Q₁ is normally at a 1. When the first telemetry gate (SCW 4) appears as a negative pulse at the output of Z141, the leading/negative edge is applied to Z148 to reset to a 0. The last gate (SCW 7) appears as a negative pulse at the output of Z144. It is inverted by Z149 so that the trailing/falling edge of the resultant positive pulse is applied to Z148 to set Q₁ back to a 1. Thus, Z148-Q₁ is a 0 during the entire readout interval and is used at Z224 to inhibit during readout.

b. Automatic Reset During Readout

There are two automatic reset mechanisms. The first occurs when the last gate (SCW 7) appears at the output of Z149 as a positive pulse. The trailing/falling edge is used to reset both binaries Z221 and Z222 to their zero states so that they can start to count transfer pulses again for new data.

The second action is necessary because it is possible that when the system is first turned on, or due to some noise that the countdown chains in either of the PHA's will have some number in them. The worst case is the number 7 in which case the staircases will be at their maximum amplitude so that, if a Mic or B signal appears and if that signal is smaller than the staircase voltage, the comparators will not trip and the data will be ignored. This fault could be a permanent one if a very large signal never appeared to start the PHA's, - for the

5.2.4 Cont.

staircases would remain up all the time. To eliminate this source of difficulty, the third gate (SCW 6), which appears at the output of Z143 as a negative going pulse, is connected to Z123. This pulse puts a 0 at two inputs of Z123 and the output of Z123 goes to a 1. As before, this starts the 64 KC clock, Z125, even though the comparator (Z121) output is also up. The clock fills up the countdown chain. On the next clock pulse, when the chain resets, the overrun one shot Z129 triggers and closes the gate Z132 so that no further clock pulses pass through. The action is identical to the case when a large B signal appears and causes overrun. The clock will stop when the start clock pulse decays due to C121 and R122. The one shot Z129 will recover after the clock stops. The countdown chain has been reset to all zeroes as desired. A similar action takes place in the Mic PHA, except that the second gate (SCW 5) is used when it appears as a 0 at the outputs of A142. This is tied to inputs of Z205 and Z210 and causes their outputs to go to a 1. The clock now starts and runs until the countdown chain falls back to zero, at which time the overrun one shot, Z211 (12 ms), stops the clock. The gate (SCW 5) releases and the one shot, Z211, recovers. The countdown chain has been reset to all zeroes. Both PHA's are thus reset to zero during readout, and at the end of readout they are ready for new data.

5.2.5 Power Supply Circuits

The power converter for the OGO III Dust Particle Measurement Instrument was designed to provide five experiment voltages and to meet the spacecraft payload requirements as defined in the Space Technology Laboratories Specification No. D-13356 Rev. A. "Specification Experiment Interfaces - OGO". The primary requirements are specified below as design goals.

Main Power:

1. Voltage: The experiment must operate at any input voltage from +23.5v to +33.5v.
2. Power: The total power must be less than 1.5 watts.

5.2.5 Cont.

3. Noise: The experiment must not generate noise greater than 20 mv p/p on the power input line.
4. Transients: The experiment must operate during and after a 10 ms 50v d-c pulse
5. Over Voltage: The experiment must not be damaged by application of any voltage from 0 to +42 for any time duration.

Power Synchronization:

1. Voltage: The synchronization signal will be a 4-7v p/p square wave.
2. Frequency: The frequency of this signal will be 2461 cps.
3. Noise: The experiment must not generate 10 mv p/p on the sync input line, or sync test line.

<u>Parameters</u>	<u>+3</u>	<u>+7</u>	<u>-7</u>	<u>-12</u>	<u>-100</u>	<u>Total</u>
Regulation	2%	2%	2%	2%	Unregulated	--
Current	53.0 ma	9.8 ma	21.0 ma	16.2 ma	0	--
Power	159.0 mw	68.5 mw	147 mw	195.0	0	569.5
Efficiency						35%

Table 5. Experiment Power Supply Requirements

The power converter consists of an input L-C filter, a pre-regulator, DC to DC converter, seven diode rectifiers, +7 volt regulator, -7 volt regulator and +12 volt regulator, +3 volt regulator, and a -100 volt filter. The payload battery source voltage is applied to an L-C filter network. The purpose of this network is to present inverter noise from entering the spacecraft via the experiment power line. The output of the L-C filter is applied to the pre-regulator module.

The pre-regulator module, Z161, serves the function of a reference and driver amplifier for an externally mounted power transistor, used as the series gate.

The output voltage drives DC/DC converter module, Z162. This module contains the active components used in the DC/DC converter. The module is utilized in

5.2.5 Cont.

conjunction with two transformers providing the frequency control and power transformation required to provide inputs to the rectifier and filter modules.

The DC to DC converter used the Jensen* circuit with an additional winding on the oscillating transformer to provide injection of a synchronizing signal. The sync signal is run through a saturating amplifier and driven into the sync winding. Sync is accomplished by the sync winding supplying the necessary volt-seconds to make the oscillator operate on frequency. The secondaries of the power transformer supply the operating voltages for six center tapped, full wave rectifiers and one full wave bridge, module Z163. The other rectifiers are mounted on the transformer, and drive respective filter capacitors which are located in the capacitor module, Z164. The potentials from the capacitor module are fed to various regulator modules. The output of each of these regulators is shunted with a capacitor in the capacitor module, Z164. The capacitors provide a low AC output impedance for the regulators. The various power busses are fed by Module Z164.

5.2.6 Description of Mechanical Package

The logic unit of the Dust Particle Measurement Instrument for OGO III is packaged into two housings fabricated from AZ31B magnesium. Magnesium was employed for weight reduction and for its good vibration dampening characteristics. The housings contain a built-in RF cavity and two cross member shear webs for internal rigidity. Relief cutouts were used wherever possible to reduce weight without sacrificing the strength of the housing. The two housings, when connected together, measure 6.50" x 6.30" x 3.24".

The modules used in the logic unit are point-to-point welded and of the cordwood type construction. Components are positioned between two mylar wafers with their bodies in close physical proximity with one another and their leads parallel. The component leads are connected by means of welding interconnecting nickel ribbon. Module lead out wires are brought out perpendicular to the body of the components. After an electrical check of the module, they are dip coated with epoxy in order to provide greater resistance to environmental effects such as shock and vibration. The epoxy also provides an efficient means of conductive heat removal. The average size of the modules are .600" x .400" x .650"

5.2.6 Cont.

and the average weight 3.85 grams. The logic unit utilizes 129 welded modules of approximately 30 different types.

A five layer all welded matrix was employed because welding forms a permanent connection, whereas soldering suffers the weakness of a separable connection. In addition, welding is a stable process, which permits repeatability and control during fabrication. Welding also assures the reliability of assembled electronic components, because heat is localized in the joining process and is less likely to induce thermal damage.

The five layer matrix consists of an epoxy glass support board .008" thick on which the modules are mounted. Underneath are two matrices, with an insulator between, which consists of two layers of wires at right angles to each other, separated by .007" mylar film. Welds are made through holes in the film in order to make connections between the perpendicular matrix wires. A module interconnection film (.007" mylar) is placed below the matrices. Module lead out wires are inserted through holes in the support board and protrude through mating holes in the interconnection film. Interconnecting ribbon is welded between the lead out wires and the circuit matrices. Excess wiring and lead materials are clipped out after welding. Eccofoam FPH (Emerson & Cuming) a high temperature polyurethane, rigid, foam-in-place resin was used to secure the electronics in each of the housings. This method was employed to maintain minimum weight and to meet the severe environmental requirements. The prototype unit weighed approximately 1269 grams; the first flight unit- 1241 grams and the second flight unit - 1201 grams.

5.2.7 Circuit Calibration Data

The actual calibration data show how closely the design goals were met. Figure 25 shows the variation in the T.O.F. measurements where the decimal number out is plotted against the input delay between the A and B signals in microseconds for three different temperatures. These data are also given in tabular form in Table 6.

The Mic PHA and BPHA calibrations are shown in Figure 26 for three different temperatures. The abscissa are the voltages measured on an oscilloscope calibrated with a digital voltmeter. The voltages at

5.2.7 Cont.

the base of the vertical steps are those causing the pulse height analyzer logic to advance to the next digital state. The Mic PHA calibration data for the three temperatures is set forth in Table 7.

Figure 27 shows a similar calibration for the B pulse height analyzer with the B PHA calibration data found in Table 8.

5.3 Environmental Testing

The instrumentation was designed and fabricated with a rigorous program of testing starting with individual components and continuing through modules, various subsystems and then the complete unit. The testing continued through integration on the spacecraft and included the environmental tests of the total spacecraft.

5.3.1 Experiment Instrumentation Testing Prior to Spacecraft Integration

The completed instrument was subjected to rigorous environmental testing to prove the complete design of the system with respect to the environmental specifications. Testing was performed at the two firms responsible for the instrument (2, 3). The successful passing of the final tests allowed the acceptance of the instrument by the experimenters. The units were then subjected to further acceptance testing by the OGO project integration group who by their acceptance qualified the units for acceptance on the spacecraft. The experiment instrumentation performed as required at all times and all apparent anomalies occurring during the tests were resolved as originating from sources external to the experiment or spacecraft. There were no component failures or measured shifts in calibration.

5.3.2 Spacecraft Testing Results

The following tests were performed with the equipment and spacecraft:

1. Functional - Primarily information fed from experiment to spacecraft was received and handled properly; also, experiment responded correctly to all spacecraft command and logic signals.

5.3.2 Cont.

2. Functional Testing during various environmental tests.
3. Experiment on and data being readout from the spacecraft with no external signal stimuli - closest approach to flight operation. Experiment tested by sending the in-flight calibrate command.

The experiment had a portable GSE unit which fed signals to the sensor electronics to simulate detection of particles. When this was attached and not shielded, noise was injected into the system. This was particularly true in the thermal-vacuum tests. The problem arose because the plasma amplifiers were very fast and rf fed into the system from external cables could trigger these amplifiers. Disconnect the GSE and only use the in-flight calibrate system to simulate the event. This was the only problem occurring during spacecraft testing and was not considered a problem for flight since the integrity of the system was violated only when external cables were connected and bathed in rf.

On the ground tests showed no spurious signals from any commands given to the spacecraft. Two experiments produced noise data in the experiment when they were turned on and off. Since this was always accomplished by ground command, these non events could always be eliminated.

Two noise tests were conducted to study the low level background noise count.

1. A three hour test where all spacecraft functions operated - result, no spurious events.
2. A fourteen hour quiet run where the complete electrically live spacecraft was operated and the data were monitored continuously. Results - no spurious events.

After launch, a question was raised concerning spurious counts probably coming from thermal gradients in the sensor (10). Because the tubular detector contained three independent sensors, no rigorous attempt was made to acoustically isolate the mic since coincidence of signals (mic and plasma) would identify the event. The details of thermal studies are given in the following section.

5.3.3 Noise Measurements and Studies

In any system it is desirable to know what the noise levels are, what the contributing factors are and

5.3.3 Cont.

how some of them can be eliminated or reduced. Some of these noises are due to electromagnetic interference, thermal creaks in the structure, the transducers or the electronics circuitry itself into which these noises are introduced.

5.3.3.1 Spacecraft

When the prototype unit was tested on the Spacecraft Simulator at GSFC, it was found that the noise level in the experiment was not below the required specifications. Inverter switching spikes, ringing on the data handling lines due to current surges, RF filters with common (floating) tie points, and internal grounding problems caused the noise in the lines.

By placing LC filters in the power and information output lines, removing the RF filters and rearranging the internal grounds the noise was reduced to acceptable levels.

5.3.3.2 Acoustical Sensors

The PZT sensors used in this experiment could be a source of noise if not carefully isolated acoustically from the structural part of the spacecraft. The check on spurious counts, however, is provided by the blocked tube.

Nevertheless, criticism (10) has been leveled at the reliability of this method (mic sensors) of cosmic dust detection. The main criticism has been that the transducers produce spurious counts due to temperature gradients. Thermal cycling of the equipment should assure freedom from structural noises.

The results of a thermal study were reported by Bohn et al (11) at the Tenth Cospar Meeting in London 1967. These studies were made using transducers from experiments on Explorer I, Pioneer I, Vanguard III, Explorer VIII, Mariner II, Mariner IV, OGOs I, II, and III, Surveyor Lander, and Lunar Explorer XXXV.

The sensors were subjected to temperature ranges of from -20°C to $+46^{\circ}\text{C}$ with both positive and negative thermal gradients of from $0.01^{\circ}\text{C}/\text{m}$ to $2.2^{\circ}\text{C}/\text{m}$. A total of 339 complete thermal cycles were made with a total testing time of over 32,000 minutes. Furthermore the temperature gradients and temperature extremes exceeded

5.3.3.2 Cont.

those normally experienced by satellites. The few pulses that could not be associated with identifiable interference were at a temperature below zero. Only two were recorded in the normal operating temperature range of satellites. We do not know what the source of these two pulses was. Nazarova (17) reported similar results at the London COSPAR meetings.

The greatest danger of spurious results is due to electromagnetic disturbances. With this in mind tube #3 was blocked so that no particles could enter. The electronics was identical to the other tubes. When the Sagalyn Thermal Charged Particle Experiment was operating all tubes, including the blocked one, responded clearly showing interference. It was not necessary to have the blocked tube to give this information because repeated response of the other tubes, whenever this experiment was operating, was sufficient evidence to locate the disturbance. The real value of the blocked tube lay in the fact that at no other time did it respond.

5.3.3 Plasma Sensors

This can be a source of error due to interference and in fact the front film did respond when the Sagalyn experiment was operating. The blocked tube again showed that the interference was present. The impact plasma sensor is not as susceptible to disturbances.

6. EXPERIMENT DATA

The experimenter received the data from GSFC in the form of computer tapes. The data was received in real time and from storage on a tape within the spacecraft which was dumped at a high bit rate upon ground command. The real time data was sent from the spacecraft at one of three different bit rates. The experimenters extracted the information on the tapes and the data was analyzed.

6.1 Quality of Data

After studying and comparing the data from real time and tape storage, a discrepancy was found in the two types of data. There were times for which real-time data and playback data from the onboard tape recorders were both available. The redundancy of this operation provided a check on the two systems of obtaining data. Upon comparison of the two types of data, two important aspects of the playback data emerged: (1) while real-time events are sometime present in playback data, no playback events are found in the real-time data, and (2) front film events on the control tube occur only in the playback data. From these studies, only the real time data was considered reliable.

6.2

Interference Problems

There two types of interference. The first type is one which occurred due to a known command from the ground. The commands were logged, therefore it was easy to check the coincidence of experiment data, and one particular ground command. This interference gave an experiment TOF event showing a time of 0.5 or 1 microsecond. This meant a velocity in the tube in excess of 100 km sec^{-1} , which was not possible except for galactic dust particles -- these are extremely unlikely. The other type of interference was one which occurred in the front film data. For periods of time up to even two hours, all of the front tubes registers would fill up -- including the -X tube. After studying months of the data, a pattern was noticed. When experiment 12 was not on, the problem did not exist, and at certain high altitudes and times, the interference did not occur when experiment 12 was on. Therefore, the final times of high quality data were determined for activity times when the front films were extremely quiet and the blocked tube giving no events. The noise time were very pronounced and once the problem located, it was not difficult to establish the times of good data.

6.3

Reduced Data of Impact Events

No data was finally used from the information stored in the on board tape recorders. High quality data time were established for the front film data. The TOF data required a triple coincidence in a single tube plus the added coincidence of the extra count front film. The reliability of any TOF event found is extremely high. The number of events from the front films are listed below followed by the TOF events.

OGO III Tubes	Fron Film Data Events
+Y	6
+X	6
-X(blocked)	0
-Z	4

TOF Data

Tube	Event	Day-Year
-Z	16 km s^{-1}	172 - '66
-Z	6 km s^{-1}	196 - '66
+X	12 km s^{-1}	47 - '67

The above data are from the tapes received through the period of support of the contract. The period ended 30 June 1968. Further work has continued under a Grant to Temple University. The period covered by good data types extended into the spring and summer of 1967 spacecraft operations.

7. DISCUSSION OF DATA

The data from the OGO III dust particle experiment represents the first measurement in cislunar space since Pioneer I. Most of the data gathering time was in the higher altitudes primarily between 50,000 and 110,000 km. The spacecraft went into a slow spin a few days after launch, and it was not possible to obtain orbital elements of the TOF events. However, flux information is obtained.

7.1 Summary of OGO III Flux Measurement

The flux derived from the front film events is

$$\Phi = 2 \times 10^{-3} \text{ events m}^{-2} \text{ s}^{-1}.$$

The time for good data periods was 1505 hrs and the exposed area was 15 cm². Since the front films are essentially flat plates, the above flux is considered to be over π sr. For the above flux and the difference in solid angles of the front film and the TOF tube, a prediction of 4 ± 2 events would be predicted. Thus, the flux determined from the two measurements is in excellent agreement.

7.2 Comparison of OGO III Flux Measurement With Other Direct Measurements

Data from OGO III can be compared in a meaningful way with data from previous experiments in interplanetary, cislunar, and selenocentric space. The cumulative fluxes derived from Pioneer I, Mariner IV, Lunar Orbiter, OGO III and Lunar Explorer 35 are given in Table 1. The mass sensitivities for Mariner IV and Pioneer I have been revised since the original publications because of the results of hypervelocity calibration studies reported by Böhn, et al (9).

For the empirical equation $\Phi = km^{-a}$, where Φ is the flux ($\text{p m}^{-2} \text{ s}^{-1} \pi^{-1} \text{ sr}^{-1}$), m is the mass (g), and k and a are constants, the log equation

$$\log \Phi = \log k - a \log m$$

is linear with slope $-a$. The data for the experiments listed above were plotted, and a linear curve fitted to them using linear regression curve fitting techniques. The slope of the curve is such that $a = 0.86$. In Figure 28, it is readily seen that the OGO III data point is in excellent agreement with the measurements in cislunar and non-shower periods in selenocentric space.

7.2 con't

At the present time, the physics of microparticle hyper-velocity impact is only partially understood. The mass threshold sensitivities of the various sensors will be modified as more laboratory data on the nature of the impact phenomenon becomes available. Thus, the cumulative flux-mass distribution models will also reflect these changes. However, there is a high degree of consistency in the data from the various experiments depicted in Figure 28. The new OGO III data is in strong agreement with that from the other experiments in interplanetary, cislunar and selenocentric space.

LIST OF PUBLICATIONS

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- Alexander, W. M., C. W. Arthur, J. Lloyd Bohn, J. H. Johnson, and B. J. Farmer, "Lunar Explorer 35 and OGO III: 1970 Dust Particle Data and Analysis of Shower Related Picogram Lunar Ejecta Orbits in Earth-Moon System", paper to be presented at Fourteenth COSPAR Meeting, Seattle, Washington, June 1971, to be published in Space Research XII, (North-Holland, Amsterdam, 1972).
- Arthur, C. W., W. M. Alexander, J. Lloyd Bohn, J. H. Johnson, and B. J. Farmer, "Results of a 1970 Geminid Dust Particle Rocket Experiment and Analysis of OGO III Dust Particle Velocity Measurements", paper to be presented at Fourteenth COSPAR Meeting, Seattle, Washington, June 1971, to be published in Space Research XII, (North-Holland, Amsterdam, 1972).

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TABLE 1.
Cumulative Flux Data (8, 18)

SPACECRAFT	MASS SENSITIVITY (grams)	CUMULATIVE FLUX (particles/m ² sec πsr)
Explorer I	$>8.3 \times 10^{-11}$	4.25×10^{-3}
Vanguard III	$>3.3 \times 10^{-10}$	5.0×10^{-4}
Pioneer I	1.1×10^{-11}	3.0×10^{-4}
Explorer VIII	1.0×10^{-9} - 1.0×10^{-8} $>1.0 \times 10^{-8}$	1.55×10^{-4} 2.5×10^{-6}
Mariner IV (1AU)	5.0×10^{-12}	7.3×10^{-5}
OGO III	2.0×10^{-13}	2.0×10^{-3}
Lunar Explorer 35	1.0×10^{-9}	2.0×10^{-6}
Lunar Explorer 35 (mic.)	5.0×10^{-12}	2.5×10^{-4}
Lunar Explorer 35 (cap.-miccoin.)	1.0×10^{-10}	7.4×10^{-6}

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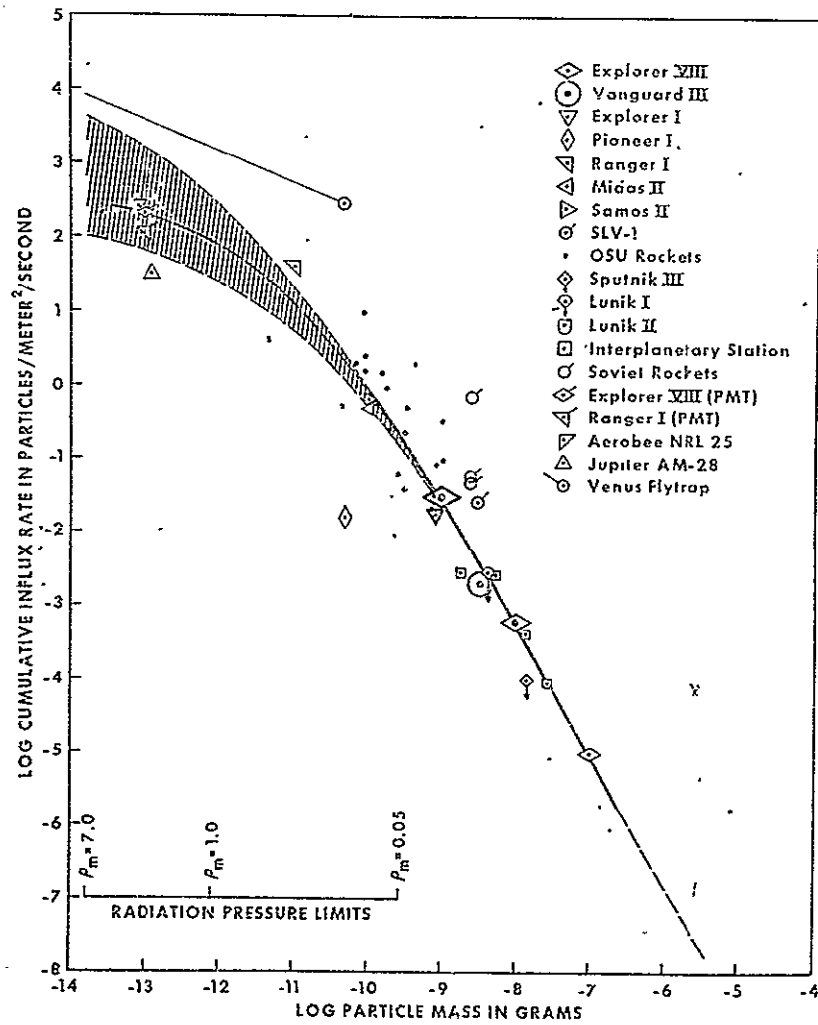


FIGURE 1

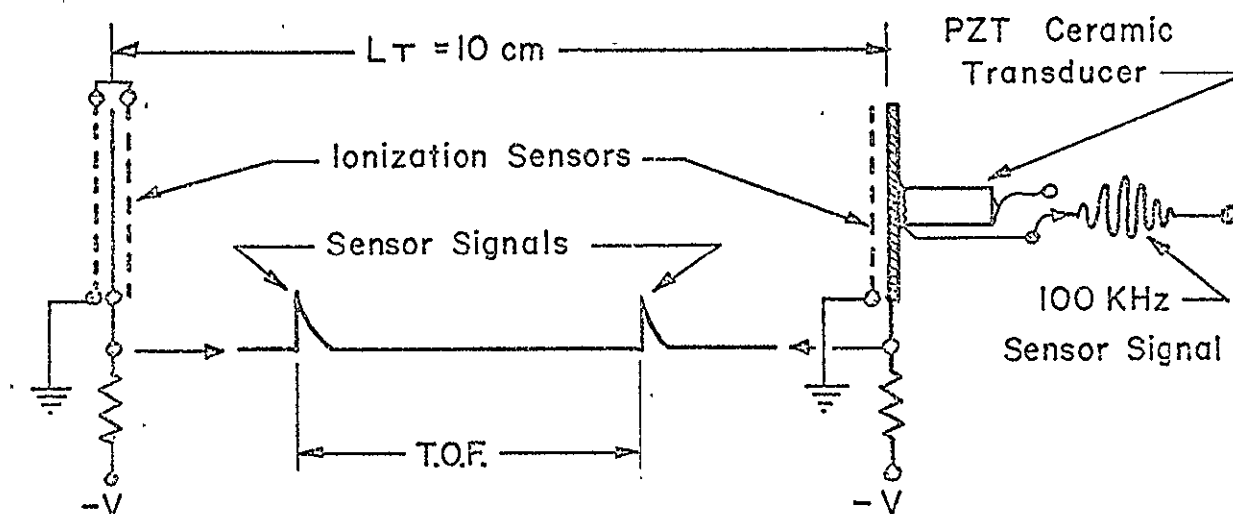
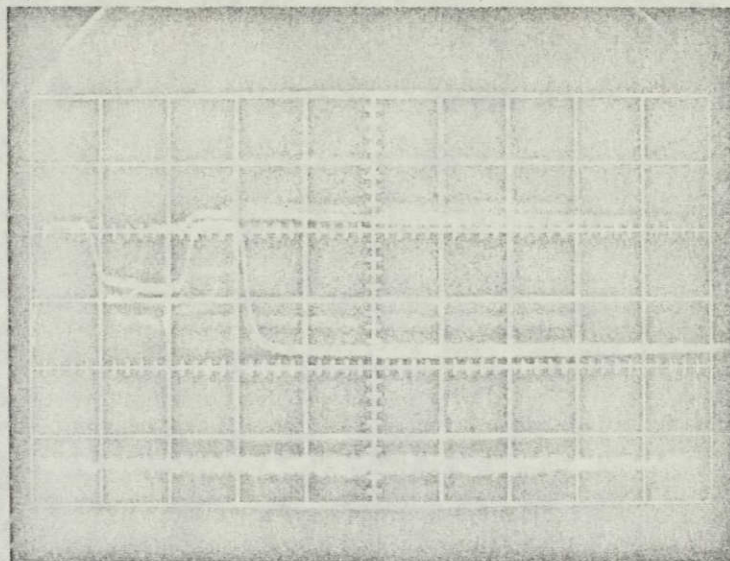


Figure 2



↑
Plasma

FIG. 3

NOT REPRODUCIBLE

Detection of Plasma from Micro-particle Hypervelocity
Impacts on Thin Films

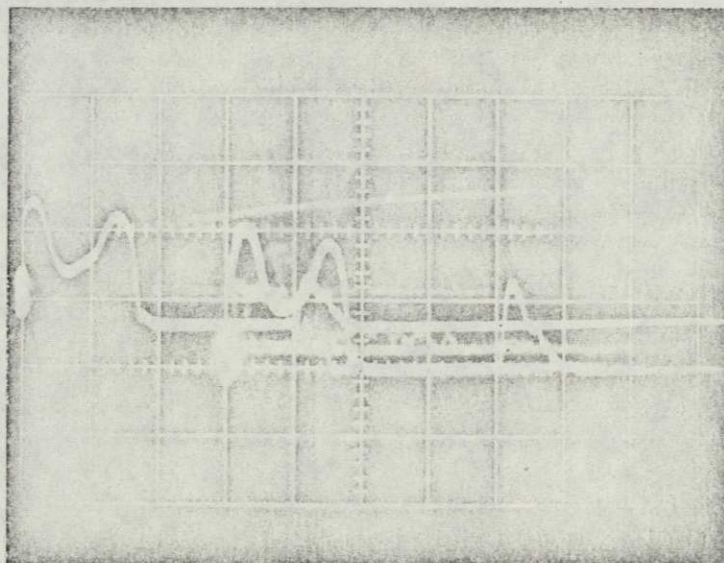
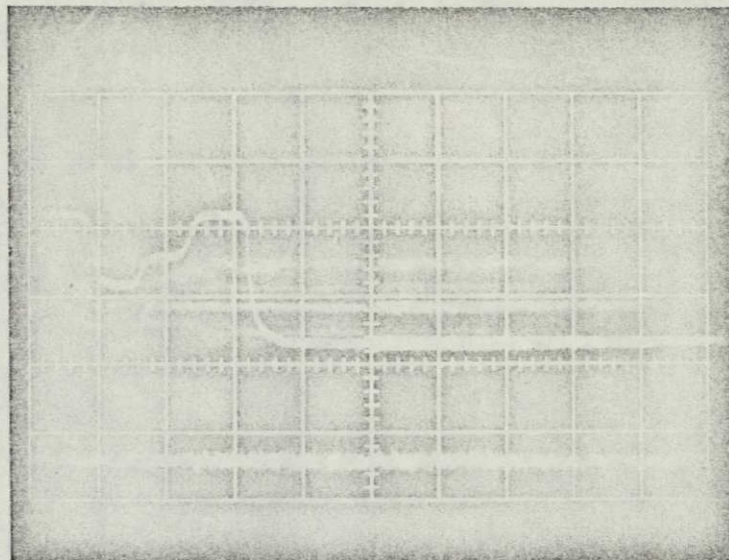


FIG. 4

Detection of Plasma from Micro-particle Hypervelocity
Impacts on Plates



↑ TOF ↑

FIG. 5

Time of Flight Measurement of Hypervelocity Particle
in OGO III Tube

NOT REPRODUCIBLE

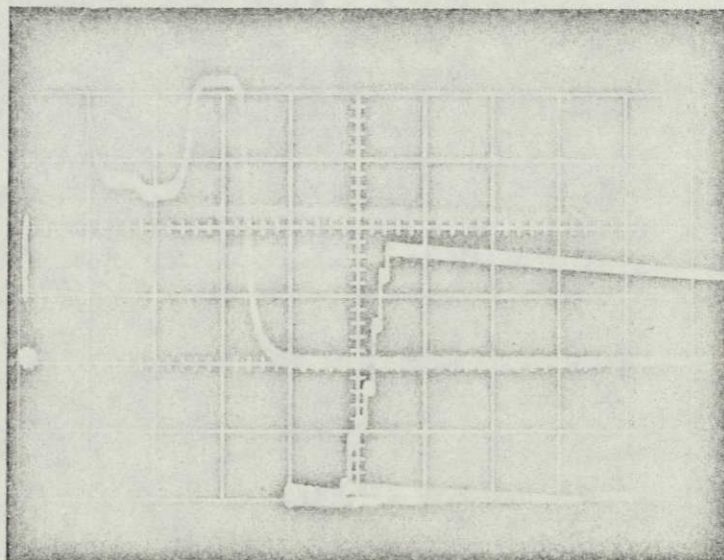
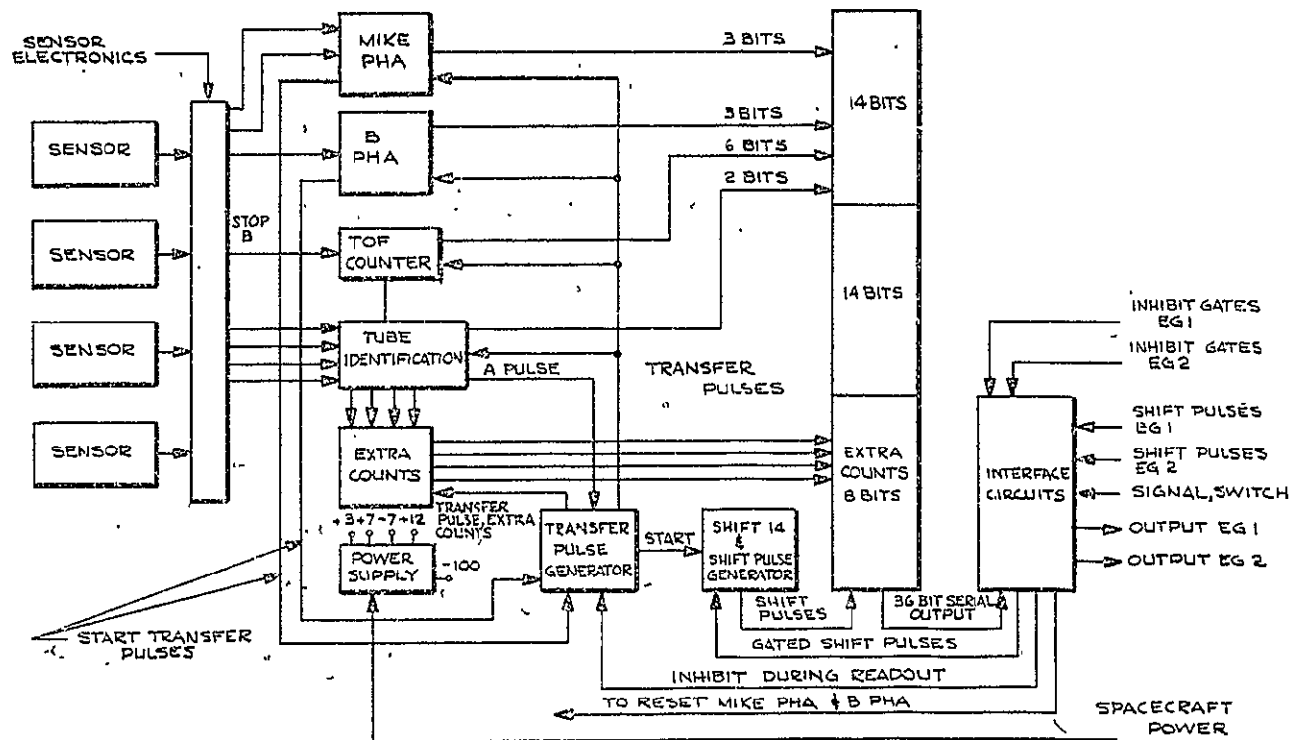


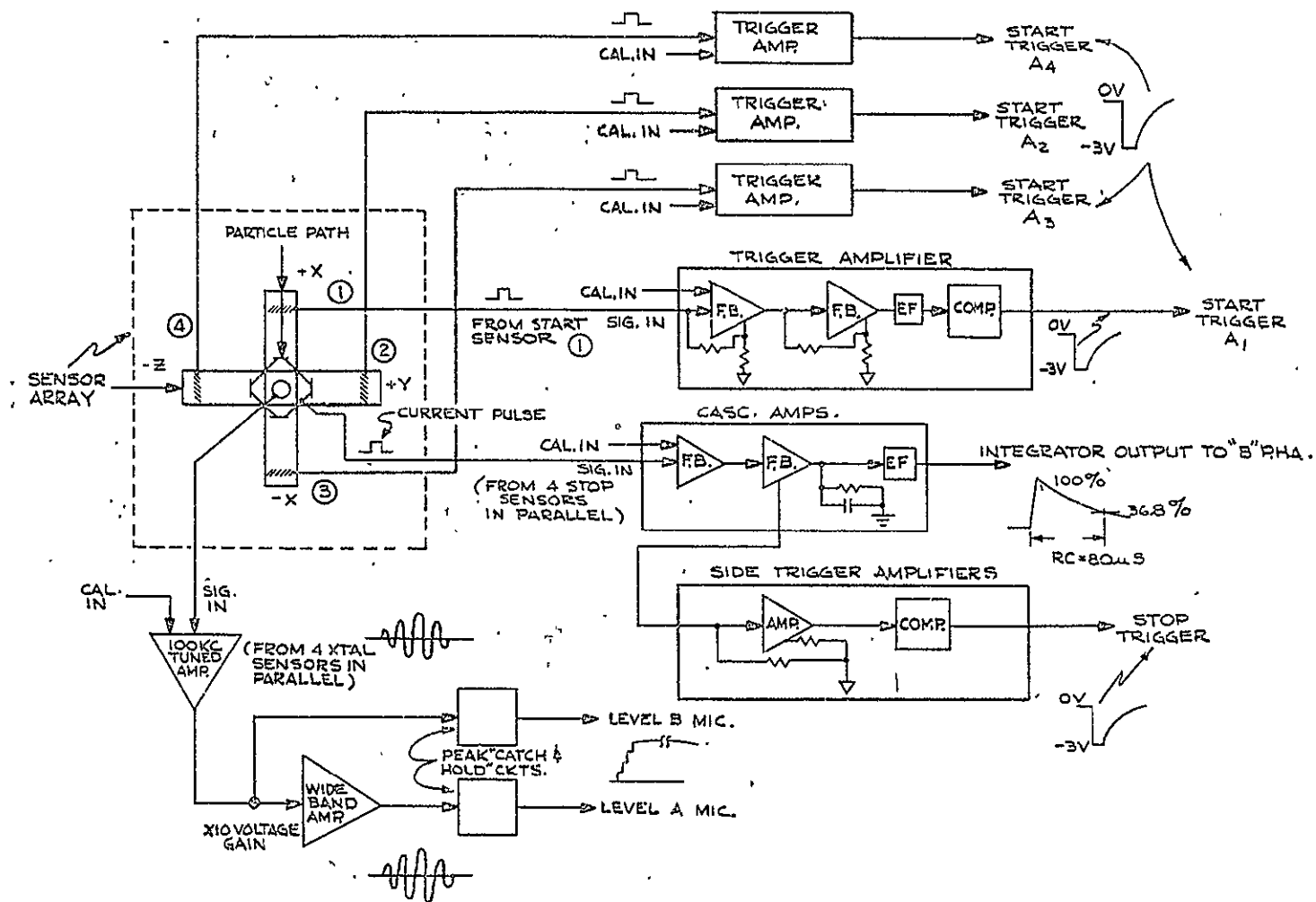
FIG. 6

Impact Impulse of Micro-particle Hypervelocity Impact

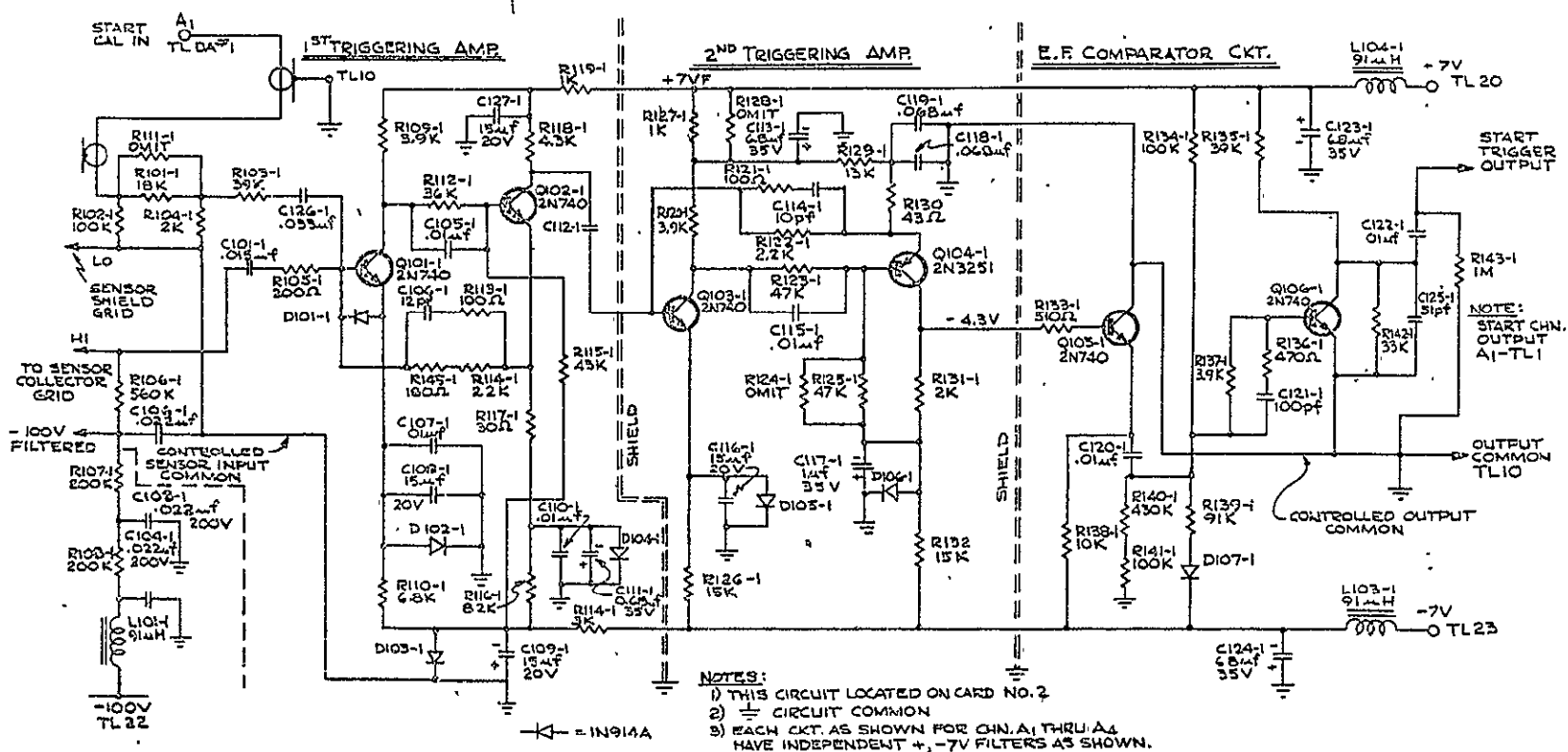


ELECTRONIC INSTRUMENTATION BLOCK DIAGRAM

FIGURE 7

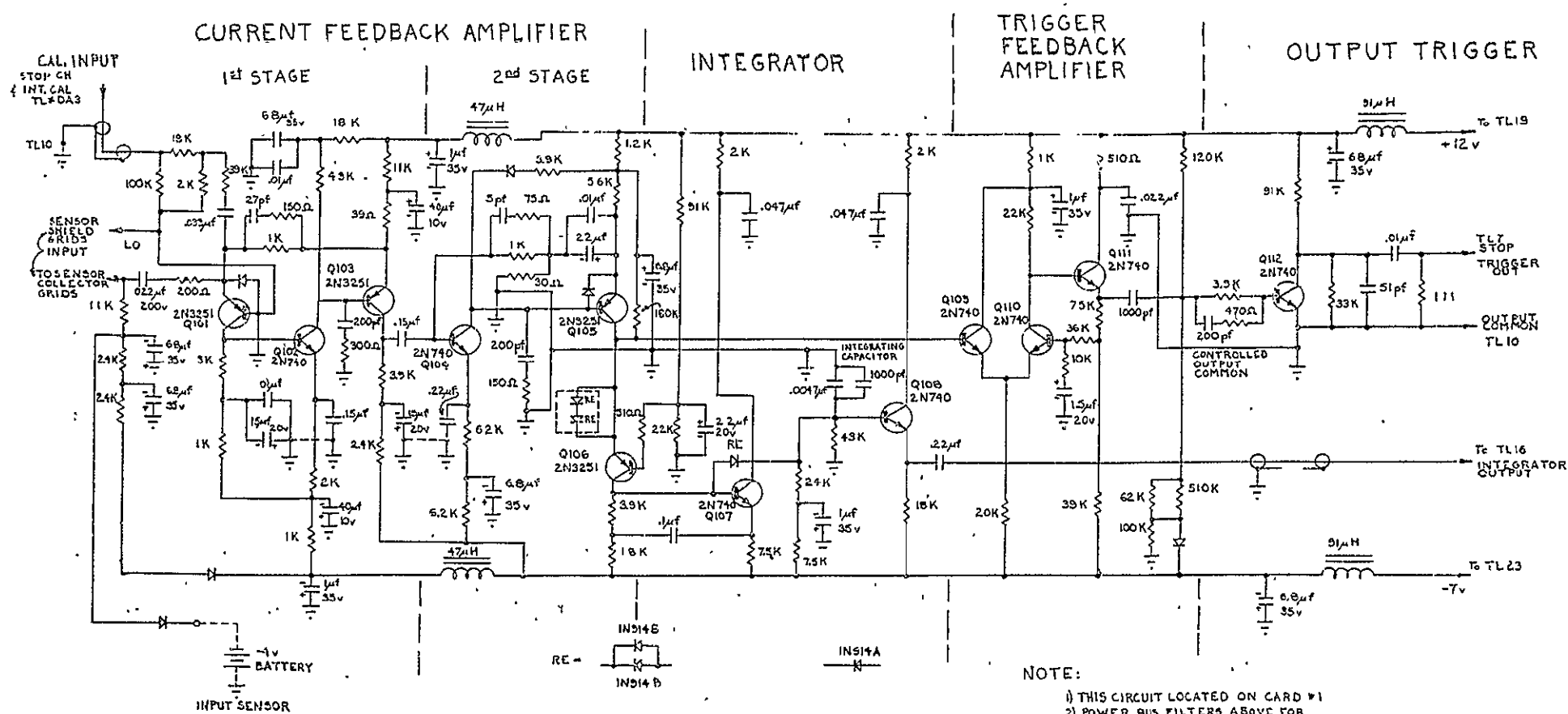


SENSOR ELECTRONICS BLOCK DIAGRAM
FIGURE 8



TOF START TRIGGER SYSTEM

FIGURE 10

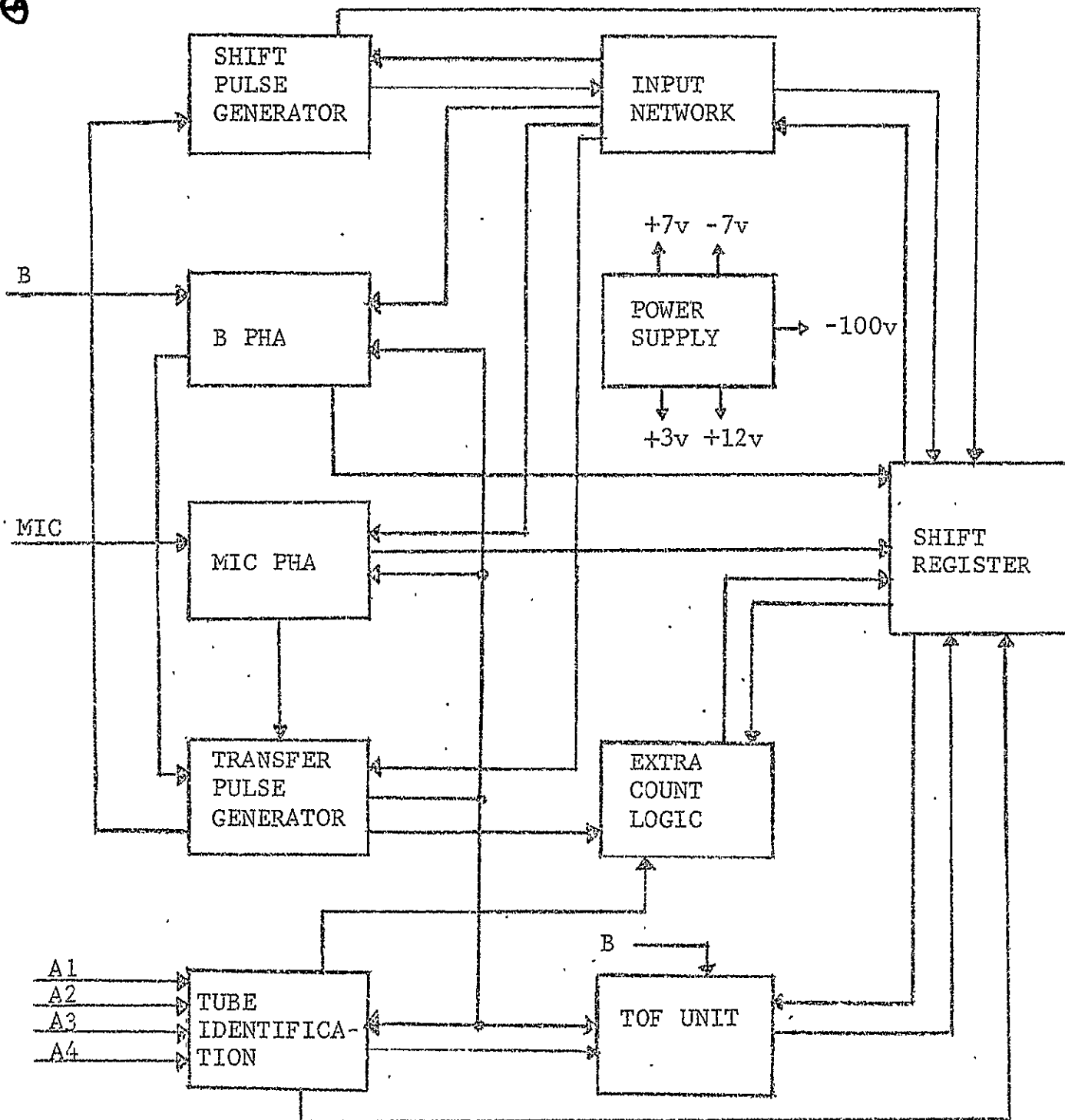


NOTE:

- 1) THIS CIRCUIT LOCATED ON CARD #1
- 2) POWER BUS FILTERS ABOVE FOR CARD #1 ONLY (CIRCUIT SHOWN ABOVE)

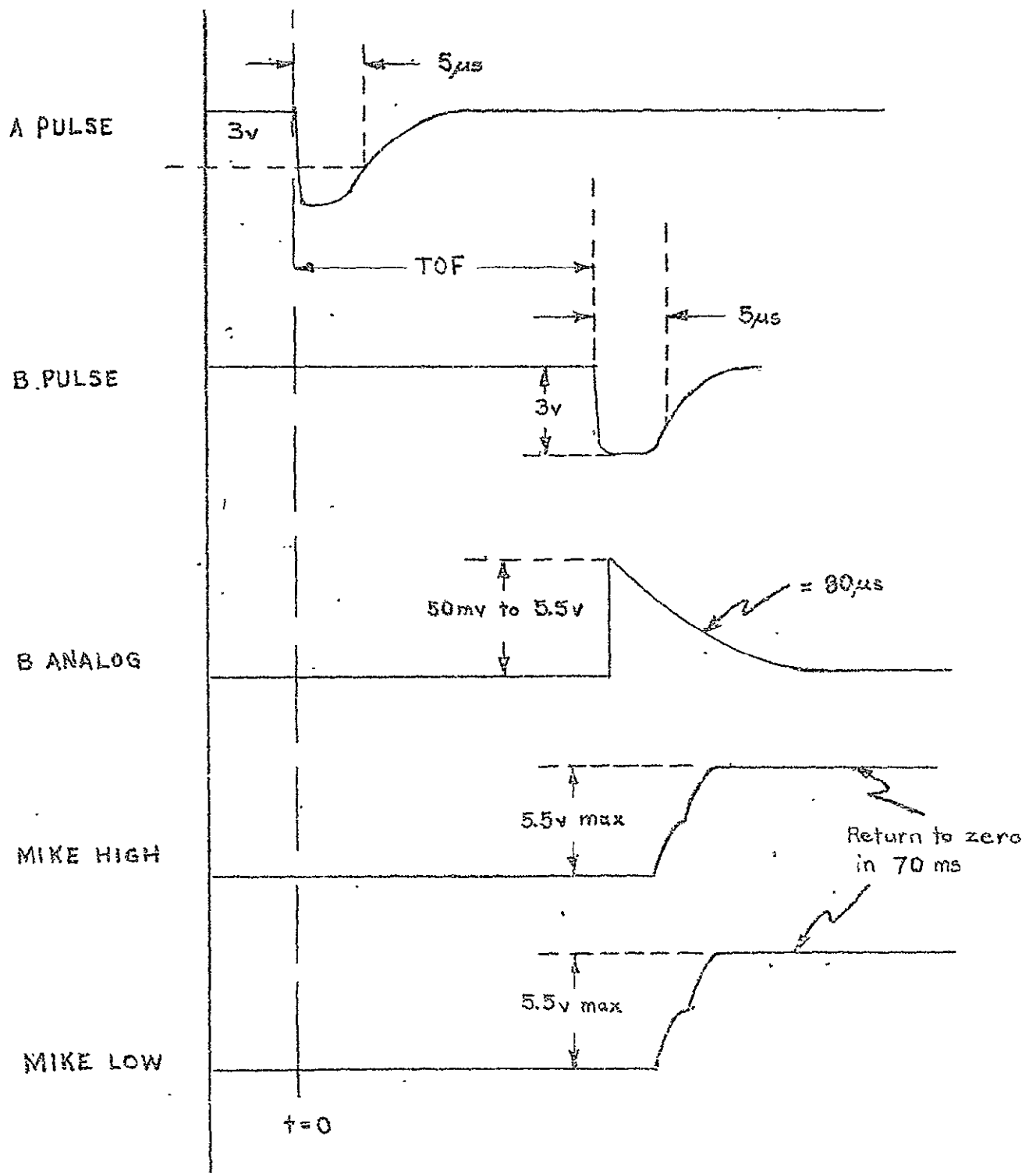
TOF STOP TRIGGER AND INTEGRATOR SYSTEM

FIGURE 11

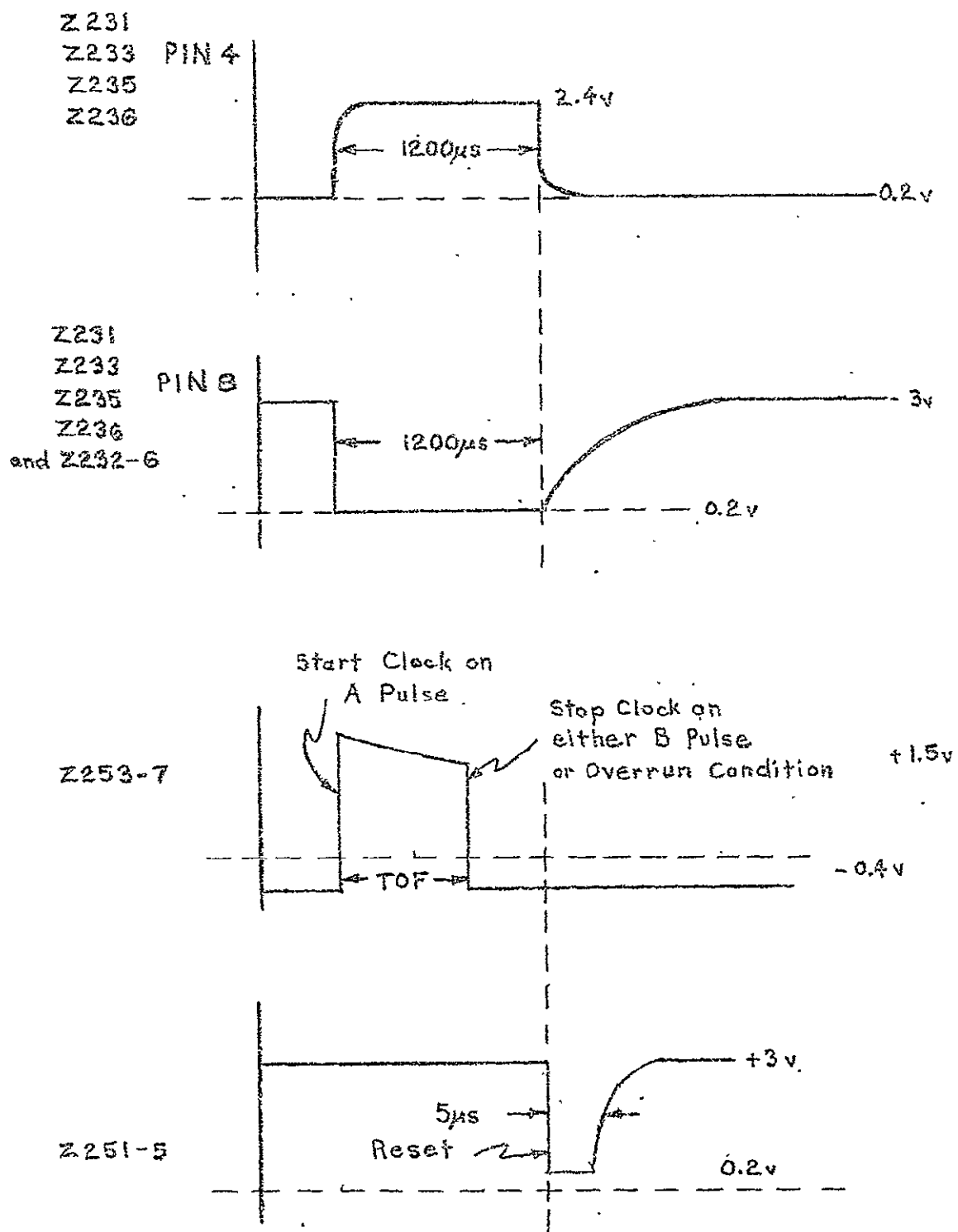


OGO III Dust Particle
Experiment Logic,
Power Supply and
Interface System

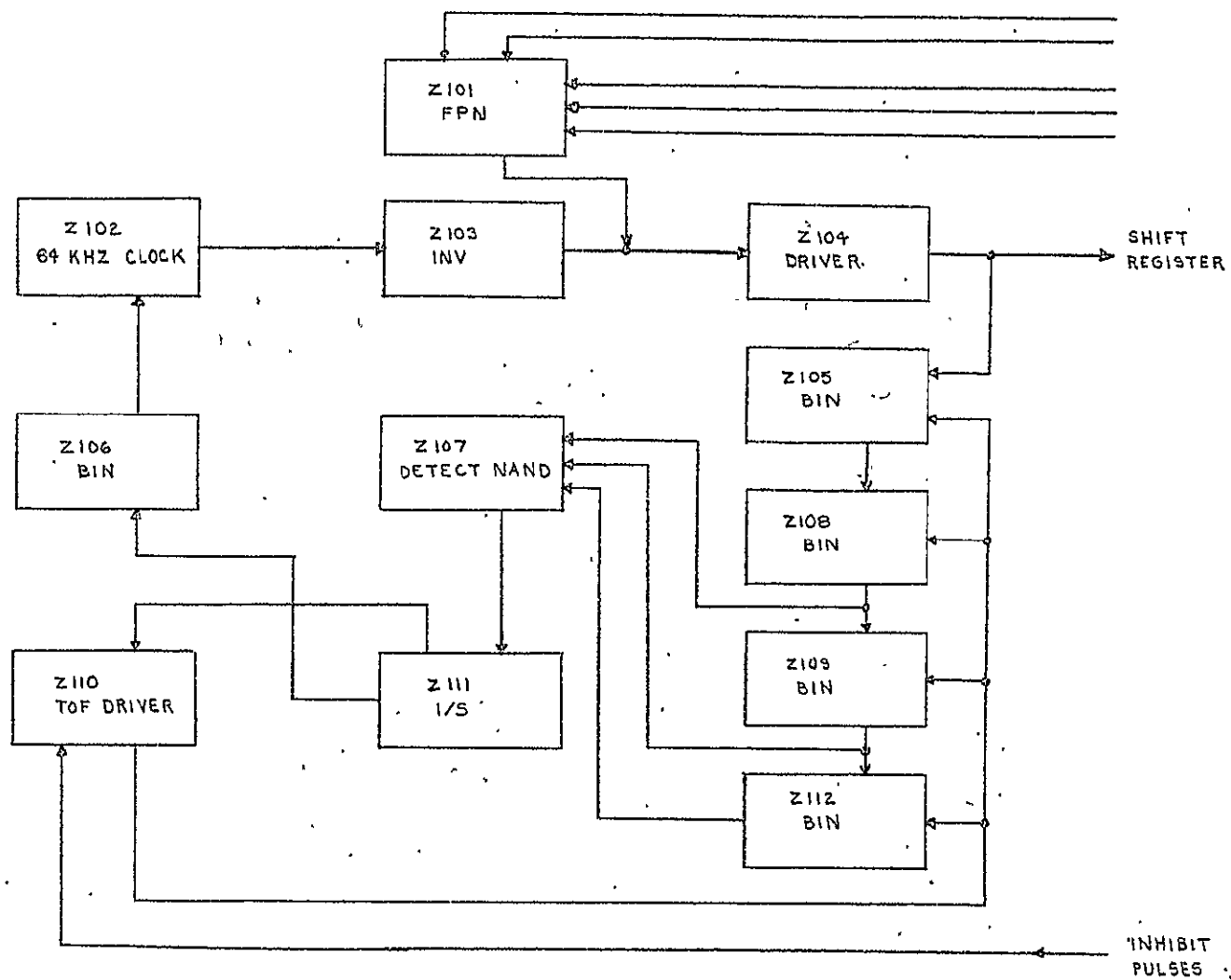
FIGURE 12A



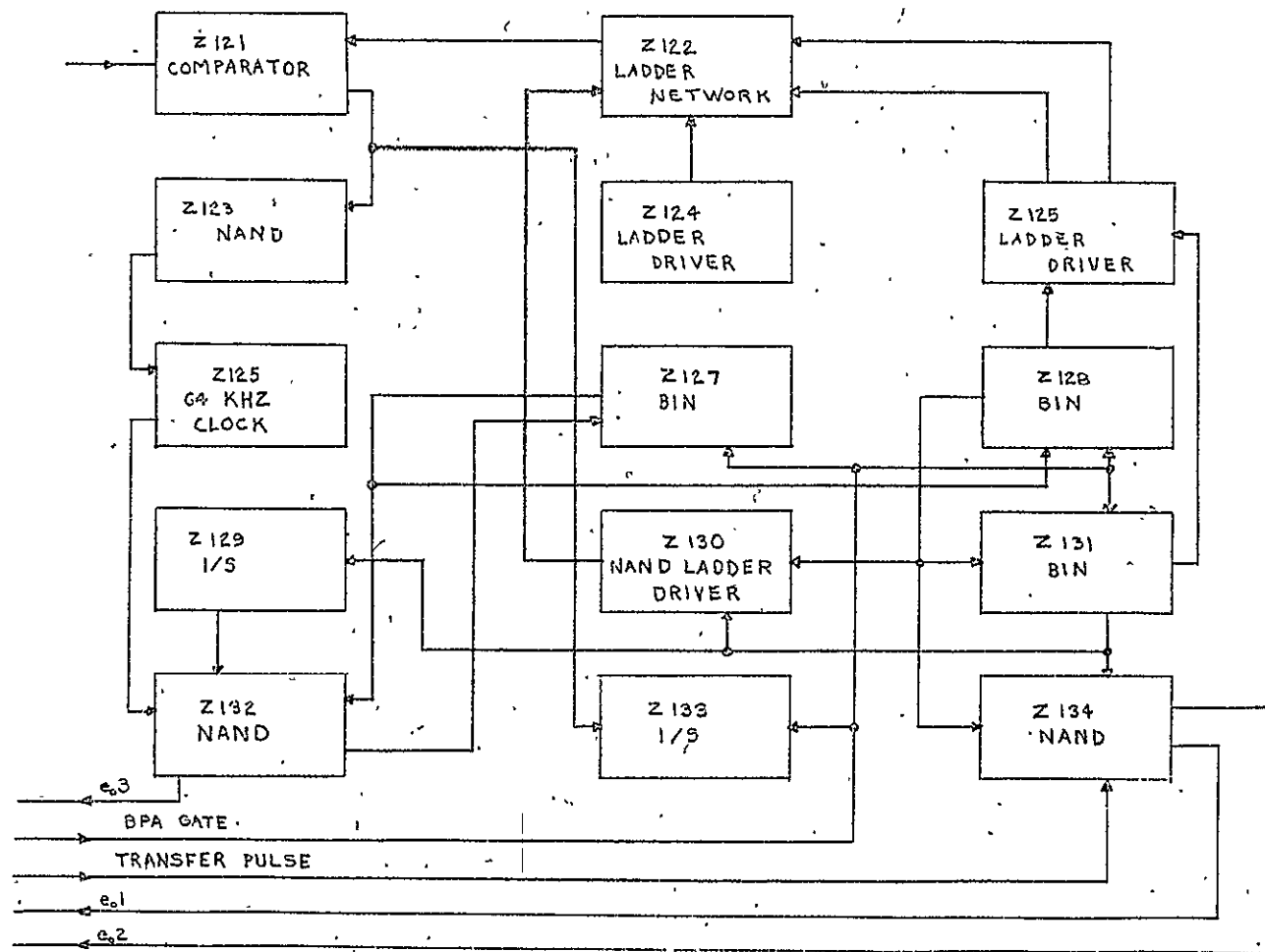
SENSOR SIGNALS
FIGURE 12 B



MODULE WAVEFORMS
FIGURE 12 C

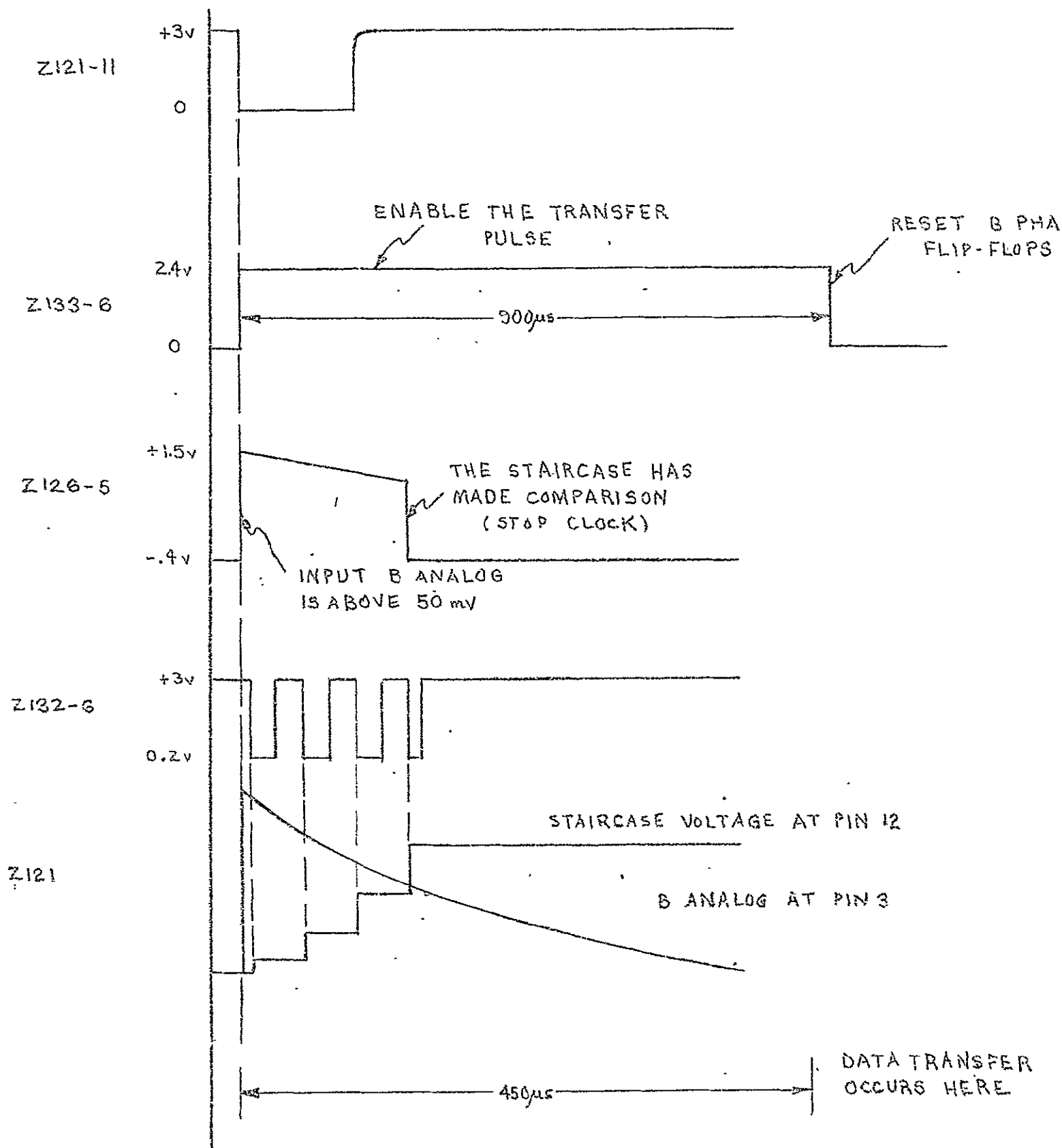


SHIFT PULSE GENERATOR
FIGURE 13



PLASMA PULSE HEIGHT ANALYZER

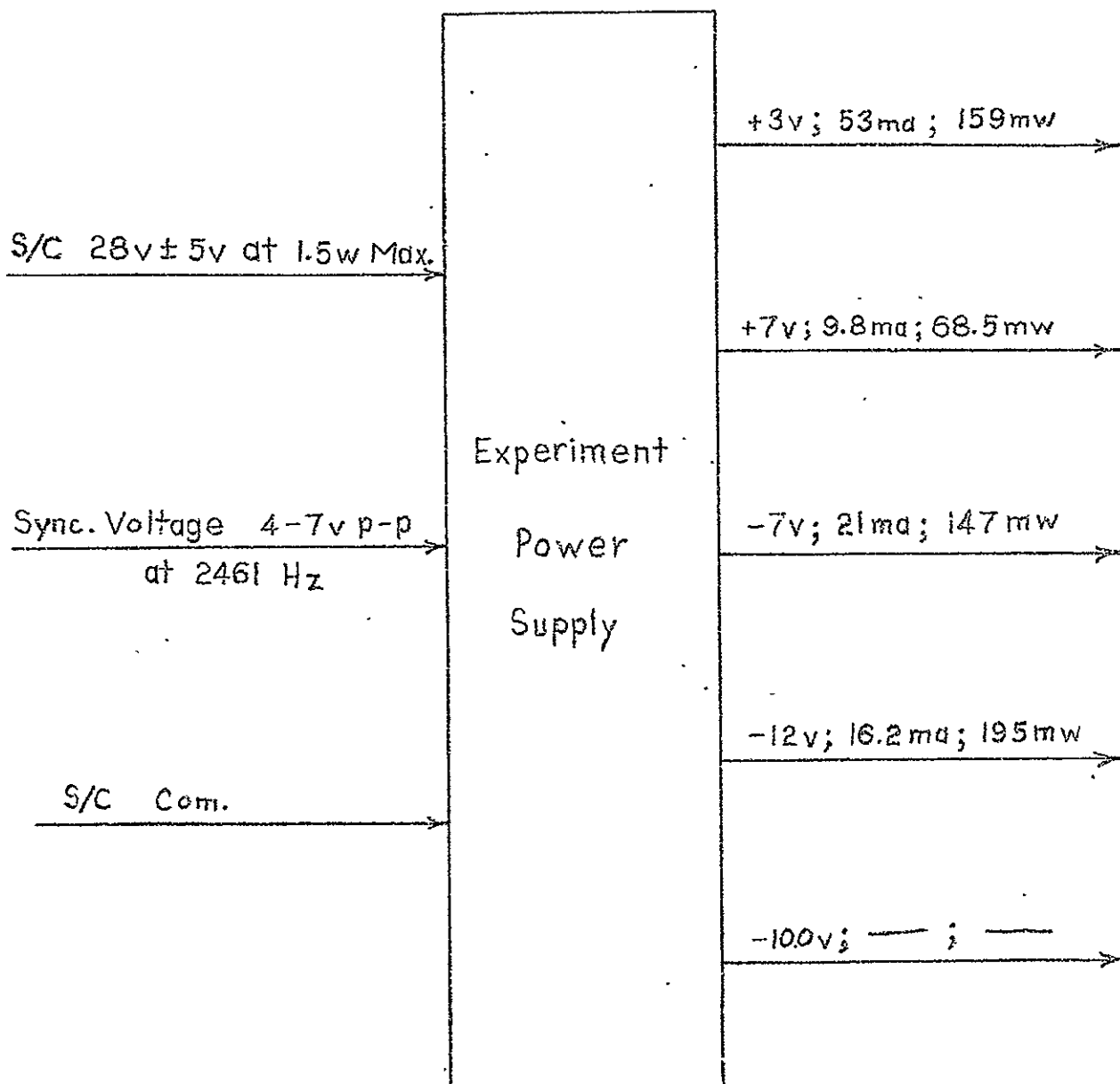
FIGURE 14



B PULSE HEIGHT ANALYZER WAVEFORM
FIGURE 14 B

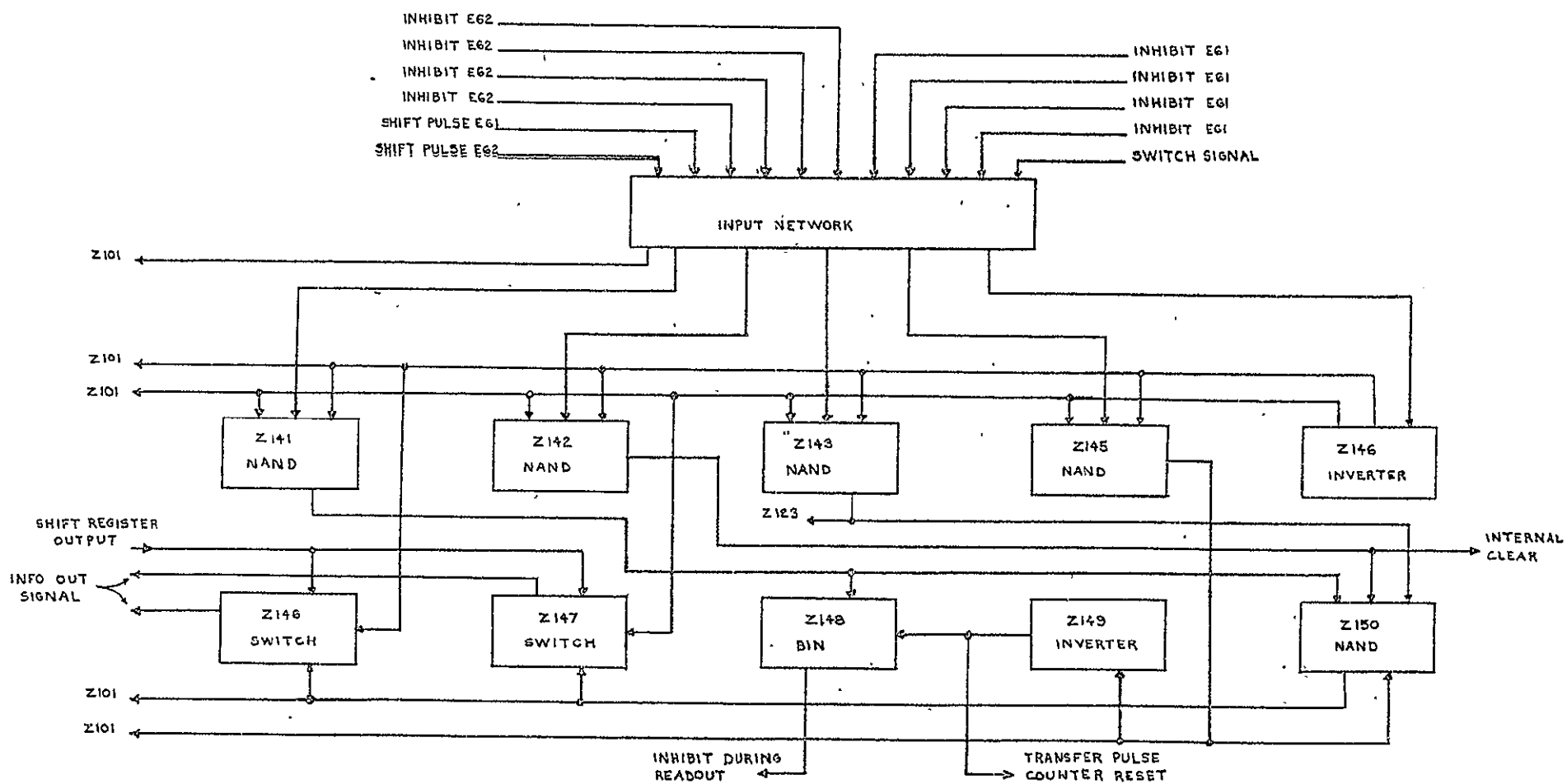
Spacecraft

Experiment



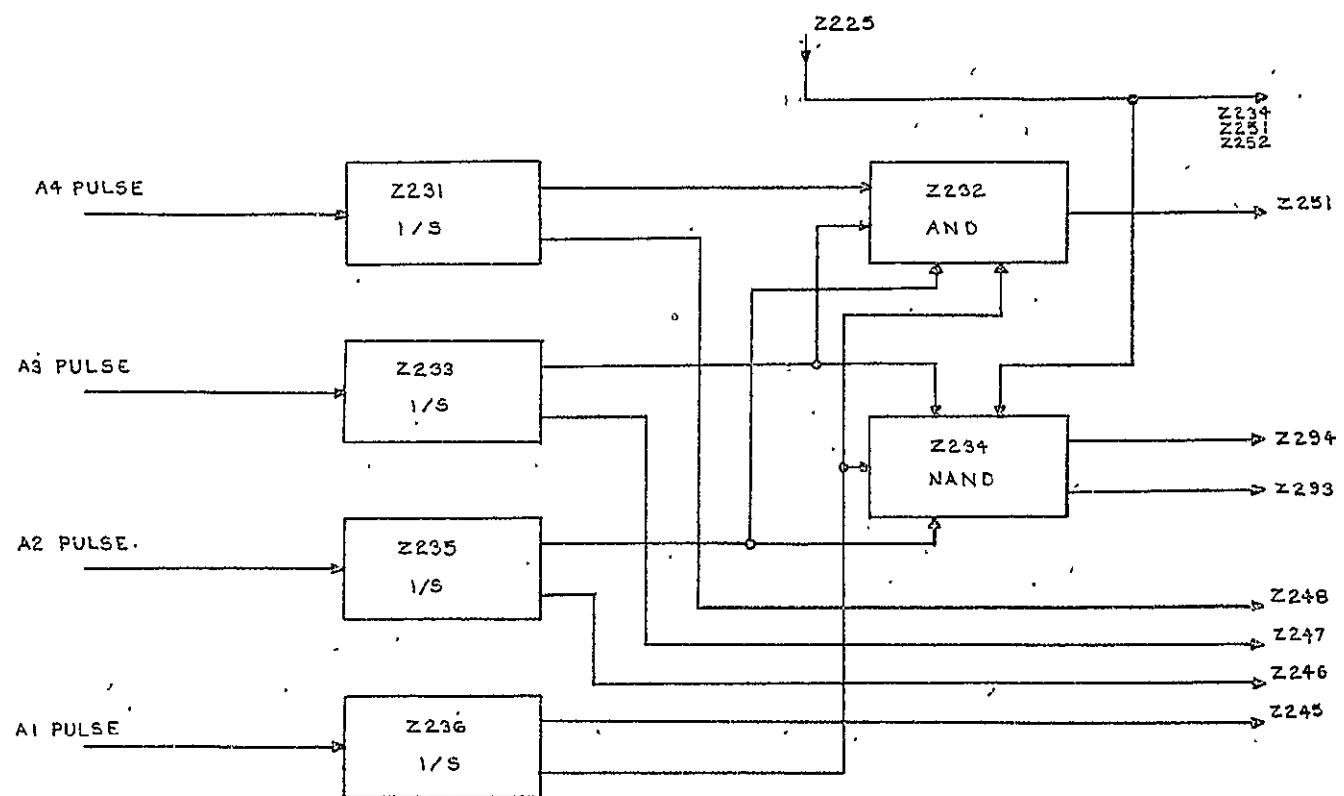
OGO III Experiment Power Supply System

FIGURE 15



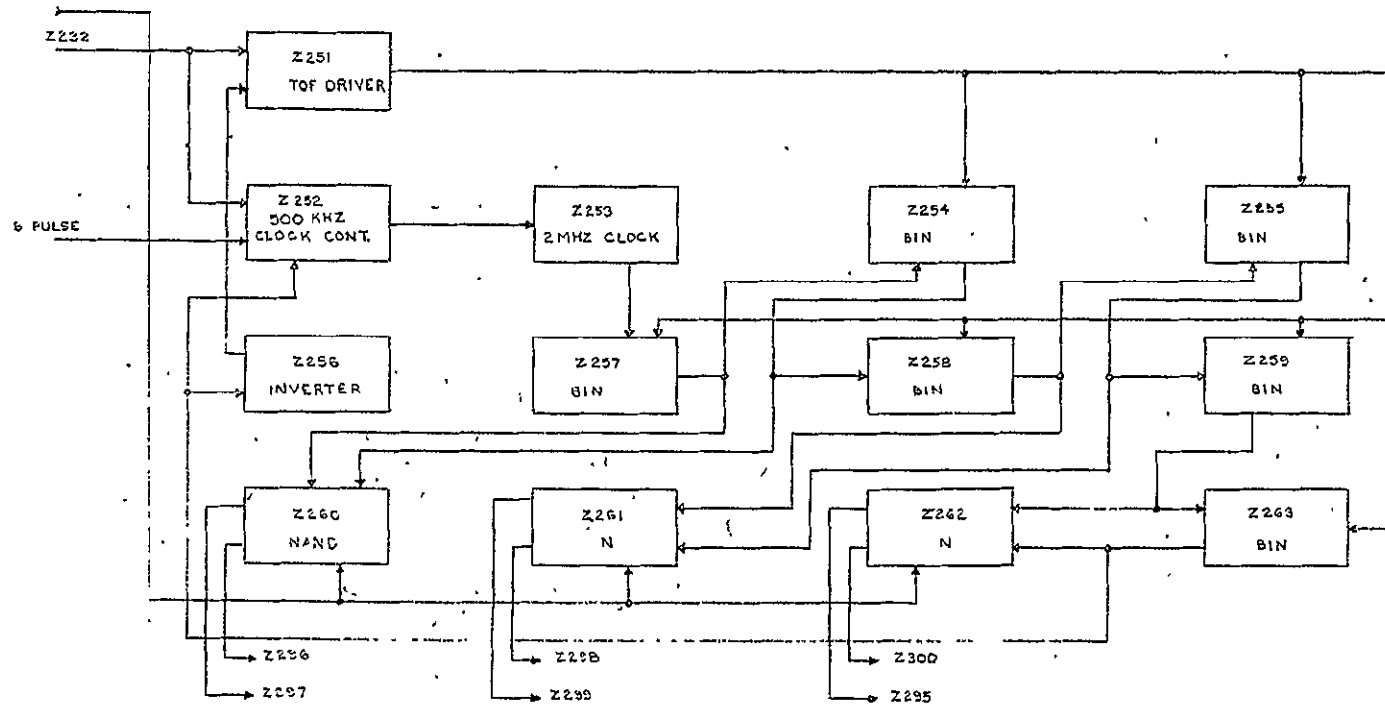
EXPERIMENT INTERFACE SYSTEM

FIGURE 16



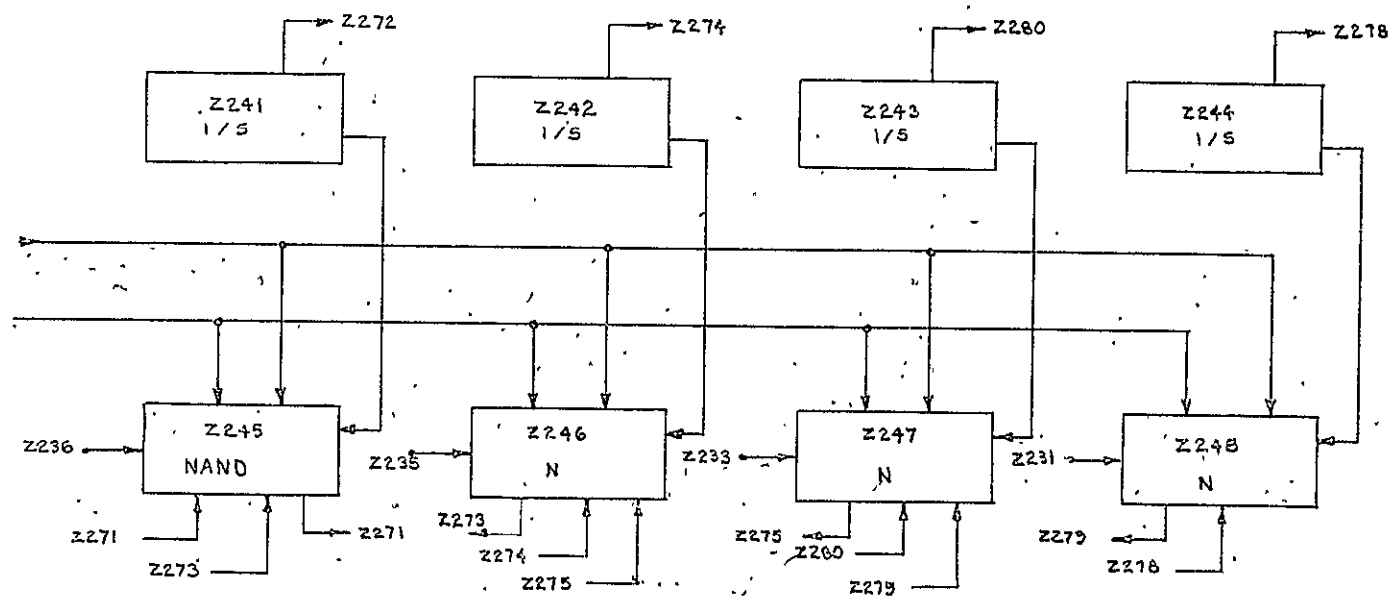
TUBE IDENTIFICATION CHART

FIGURE 17

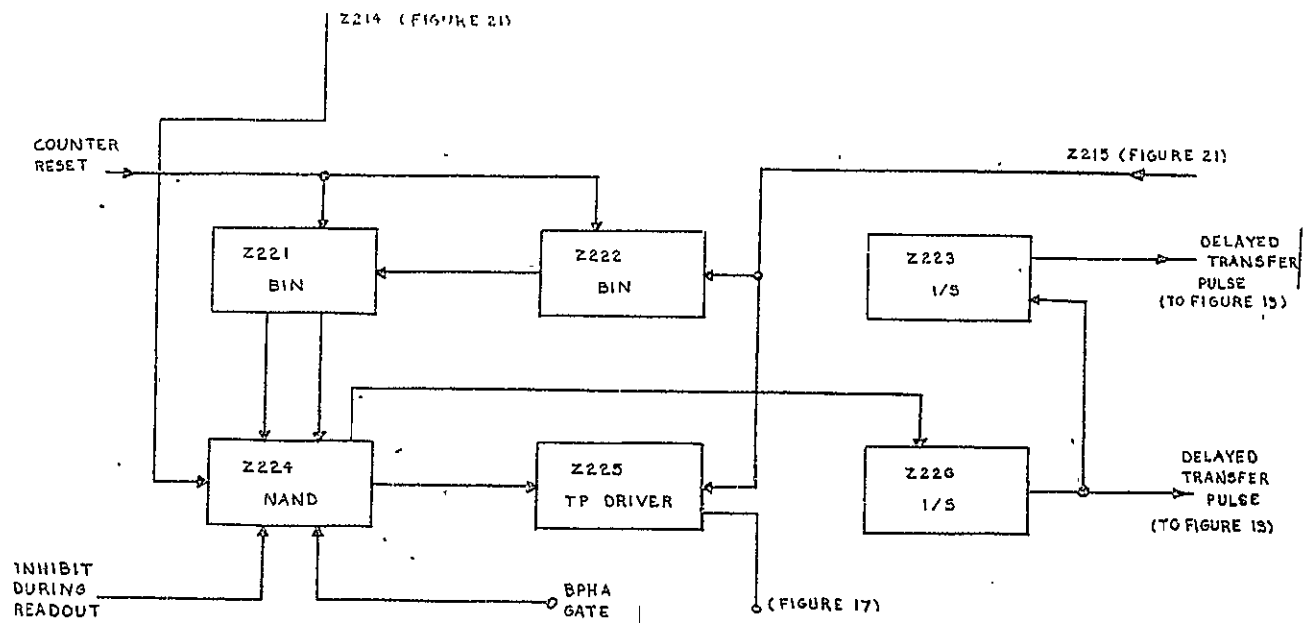


TIME OF FLIGHT UNIT
FIGURE 18



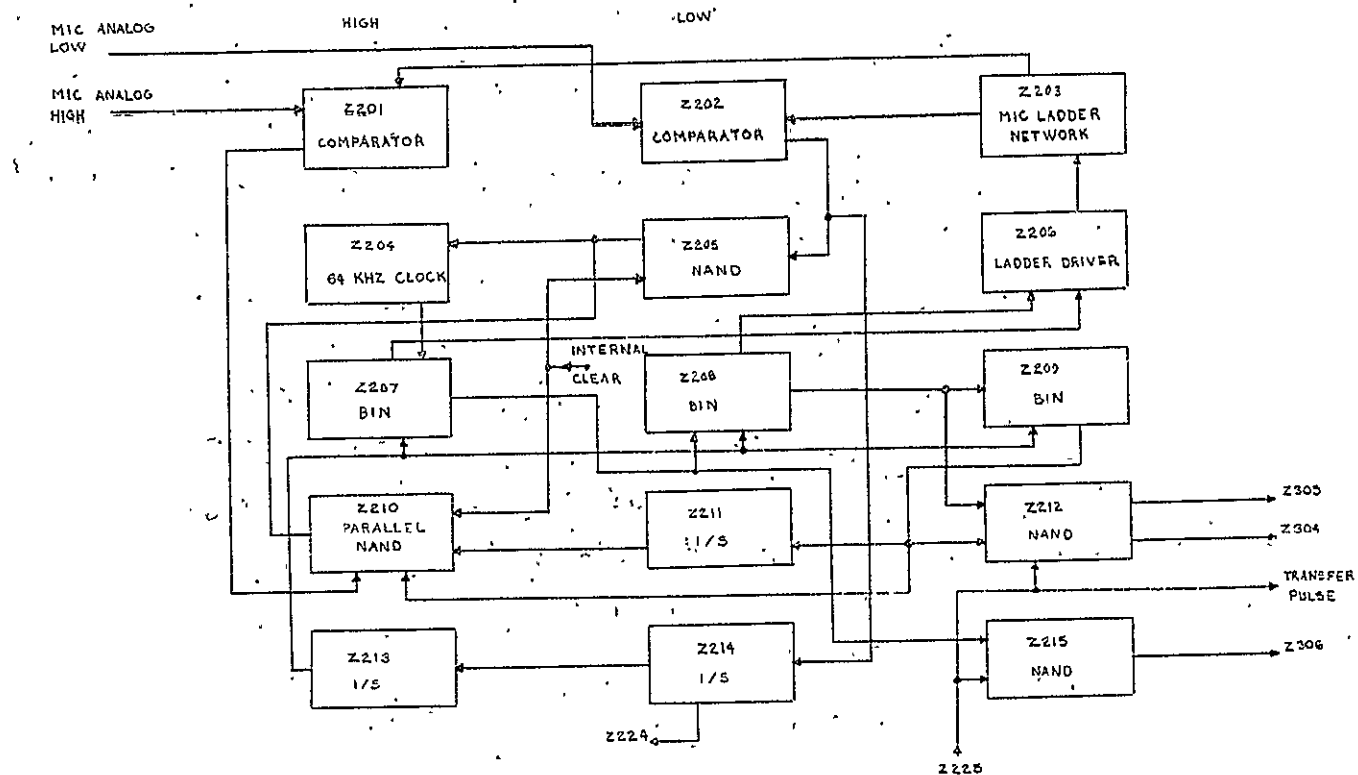


EXTRA COUNT LOGIC CIRCUIT
FIGURE 19 B

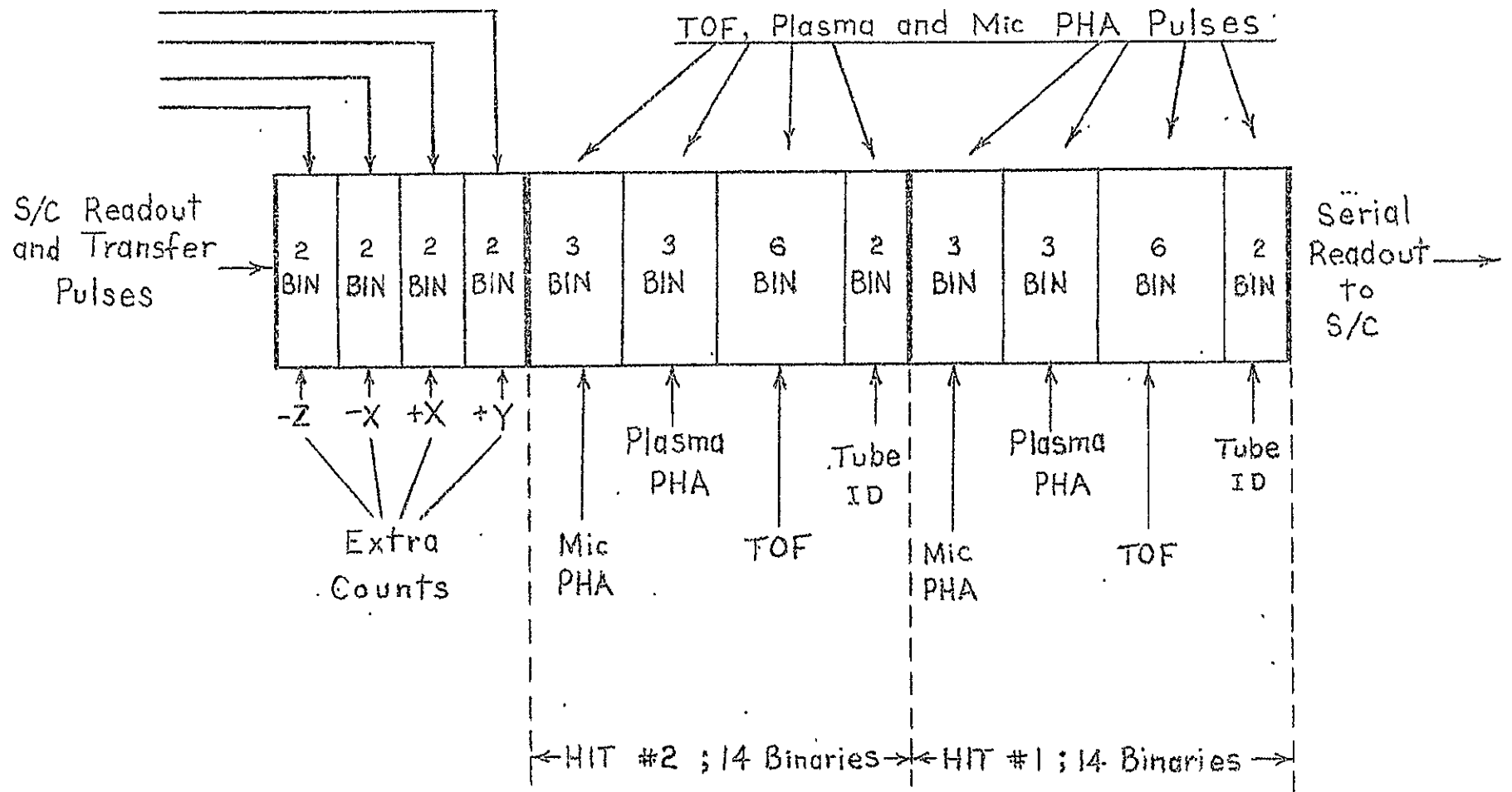


TRANSFER PULSE GENERATOR

FIGURE 20

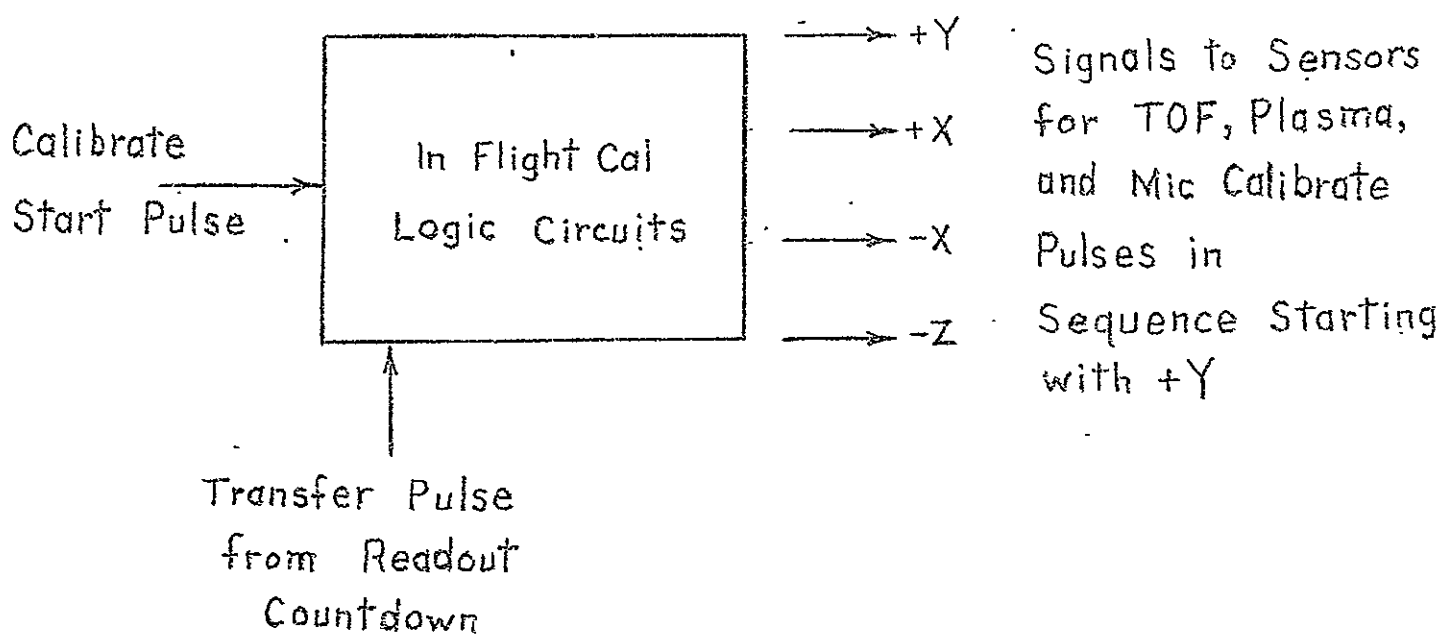


MIC PULSE HEIGHT ANALYSIS CIRCUIT
FIGURE 21



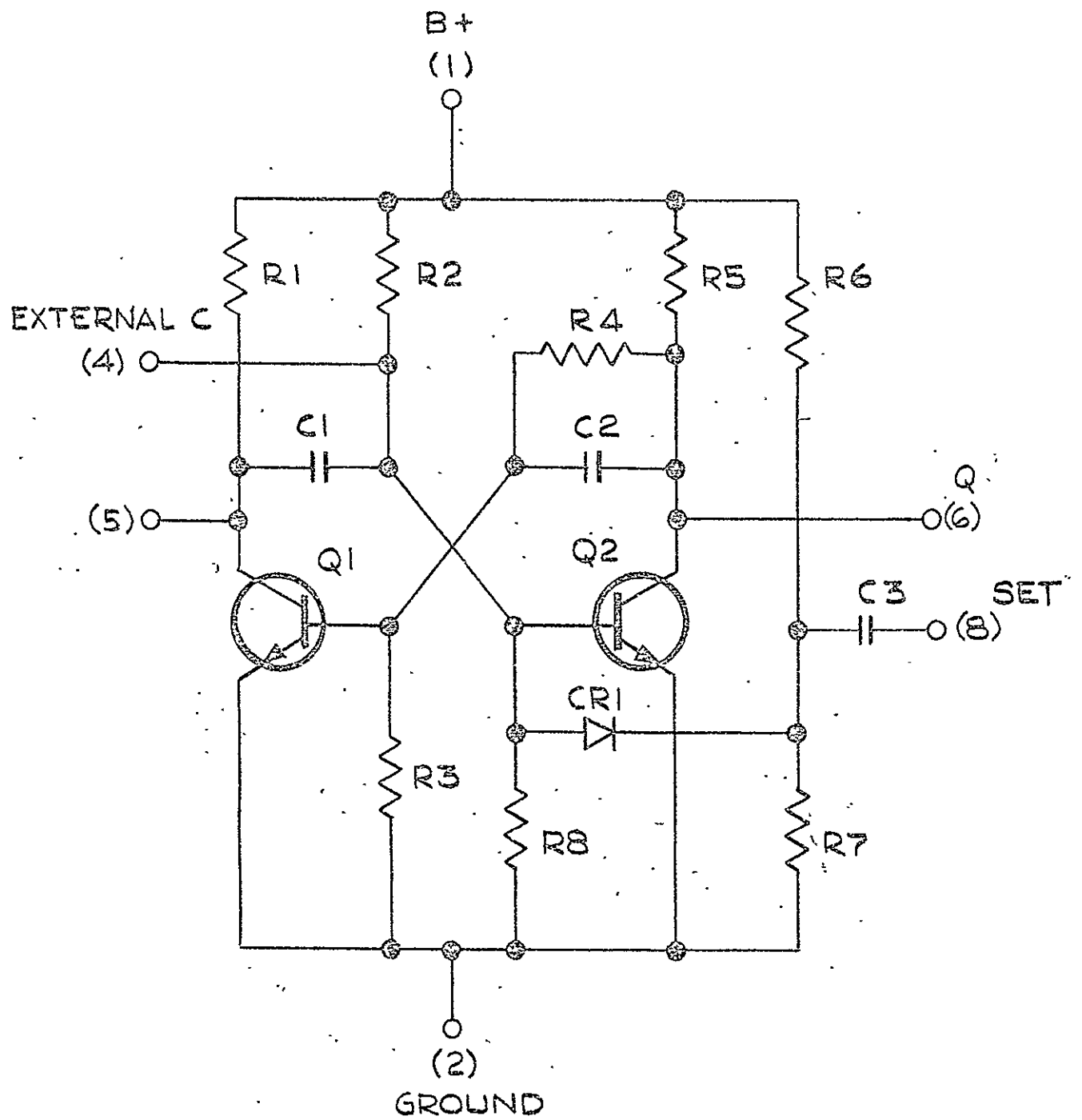
OGO III Dust Particle Experiment 36 Bit Shift Register

FIGURE 22



OGO III Dust Particle Experiment
In-flight Calibration System

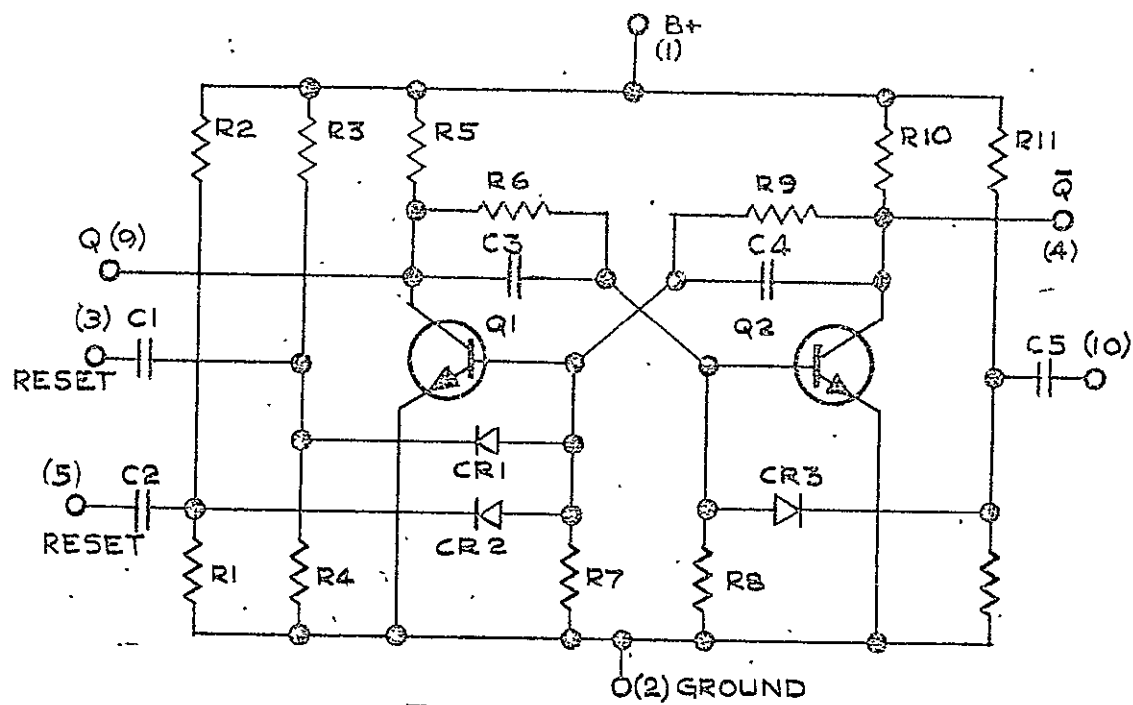
FIGURE 23



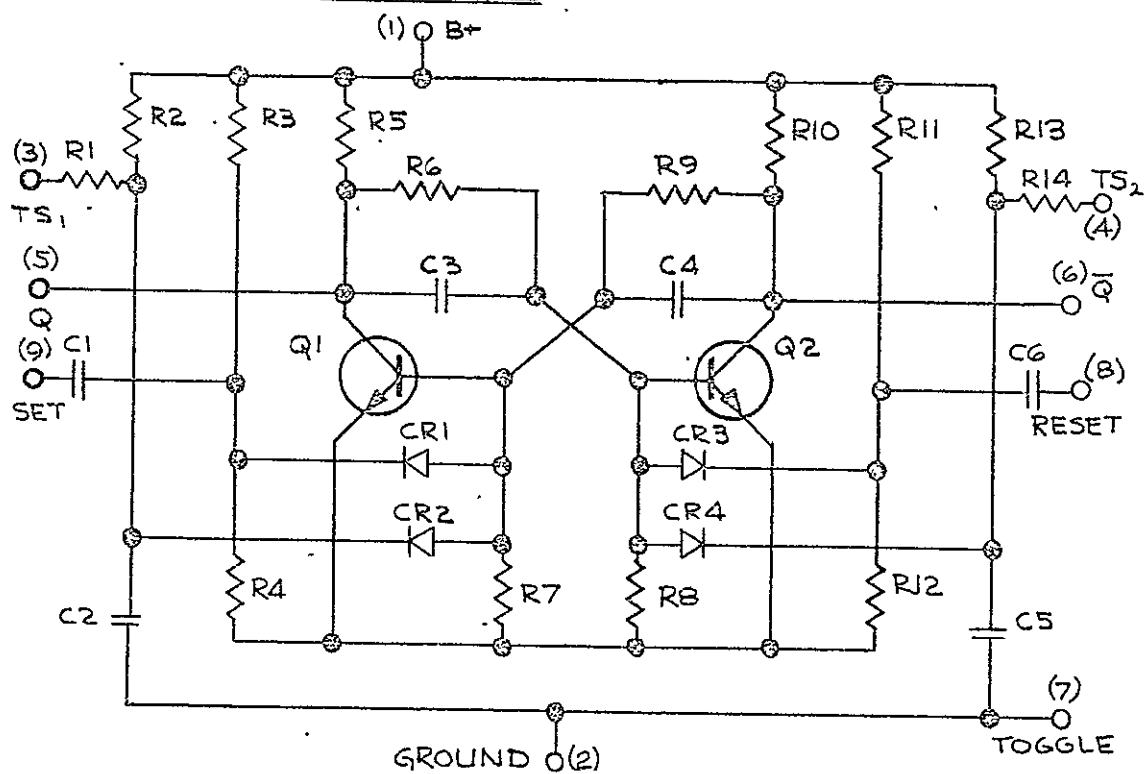
ONE SHOT

MONOSTABLE MULTIVIBRATOR

FIGURE 24 A



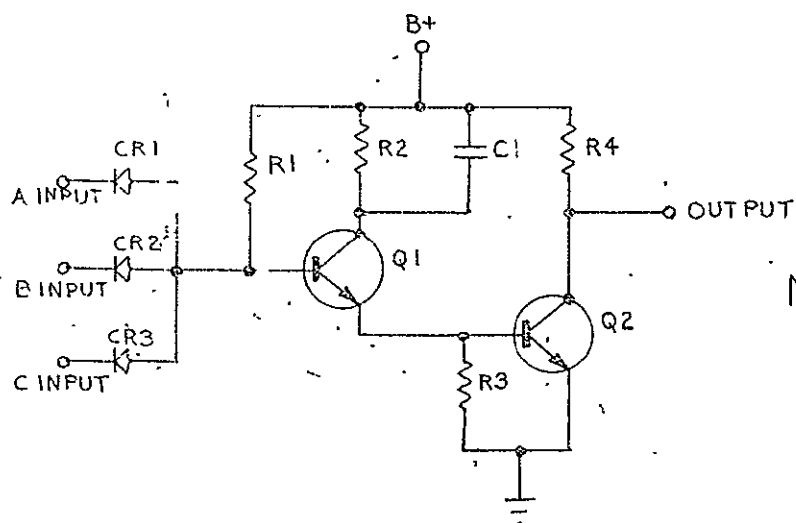
FLIP FLOP



FLIP FLOP (CONTROL CLOCK)

BISTABLE MULTIVIBRATOR

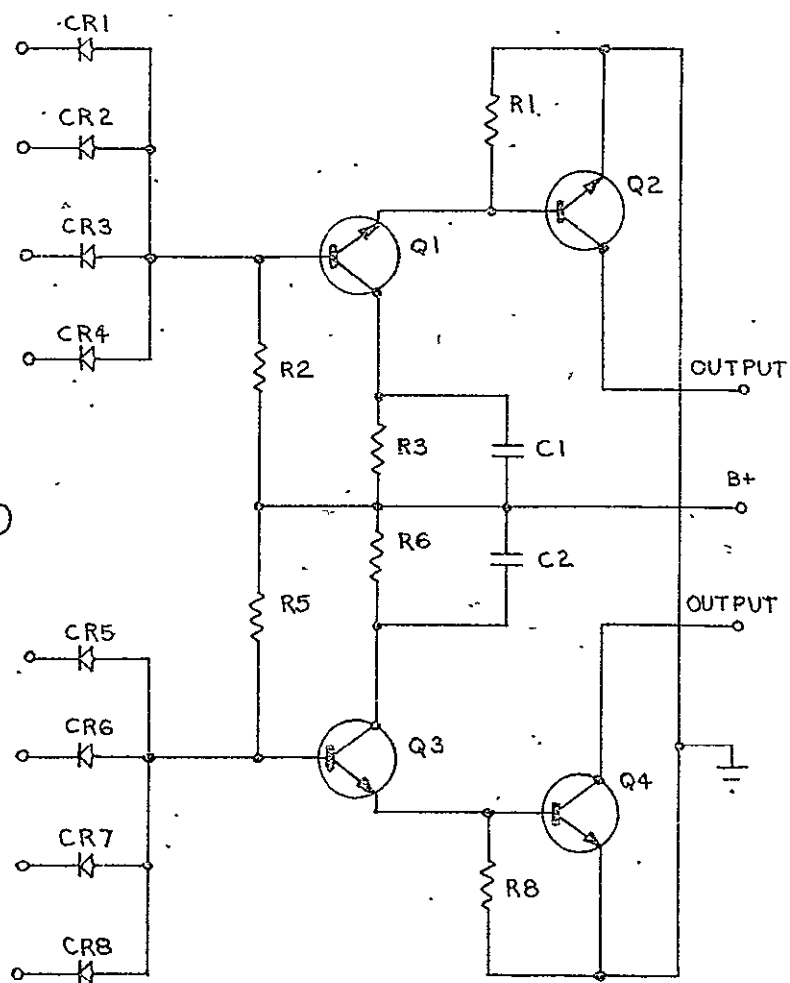
FIGURE 24 B

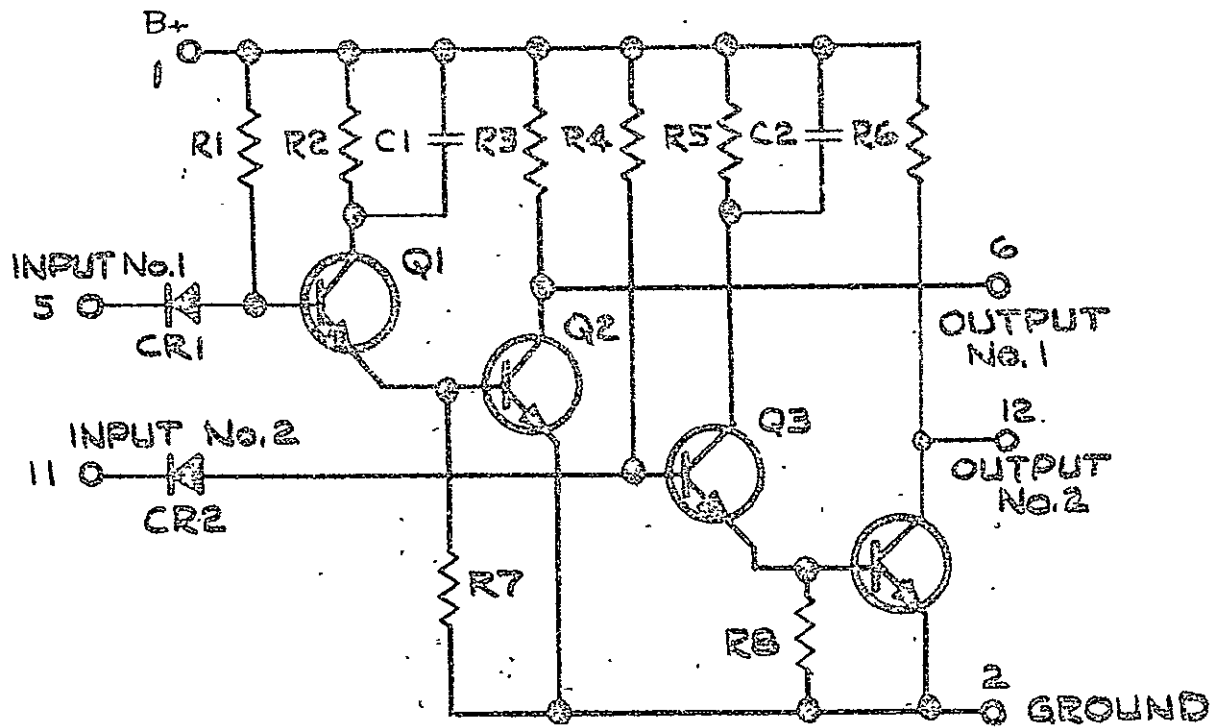


NAND LOGIC GATE

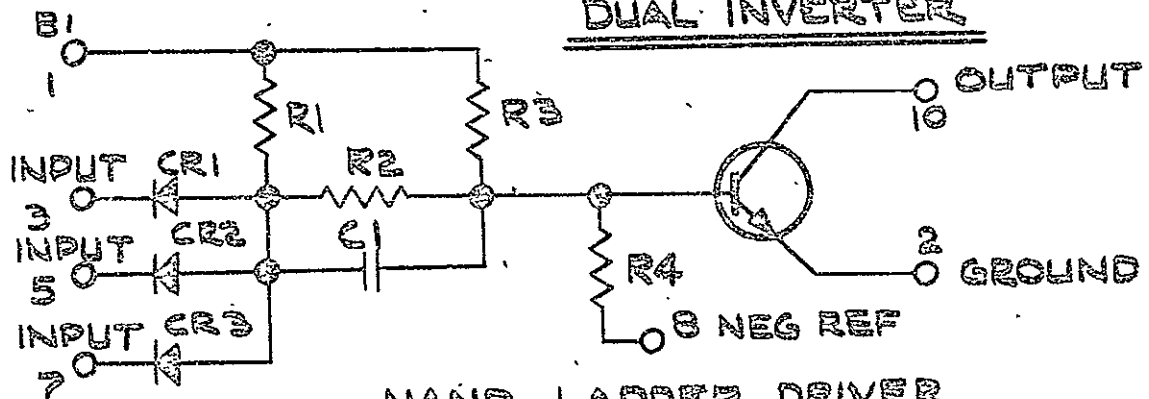
DUAL PARALLEL NAND

FIGURE 24 C

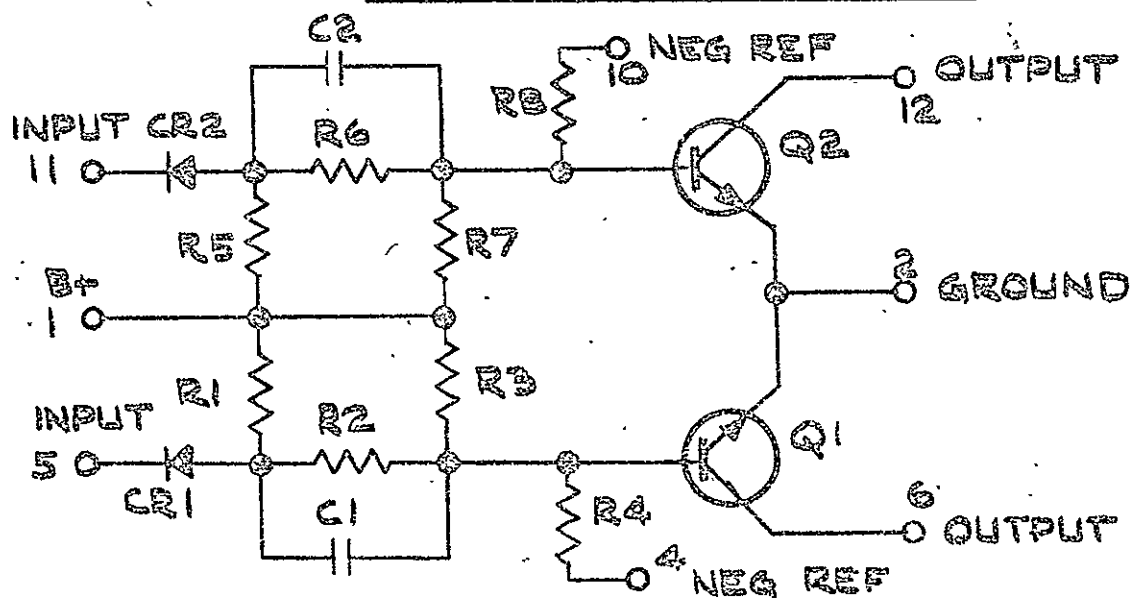




DUAL INVERTER

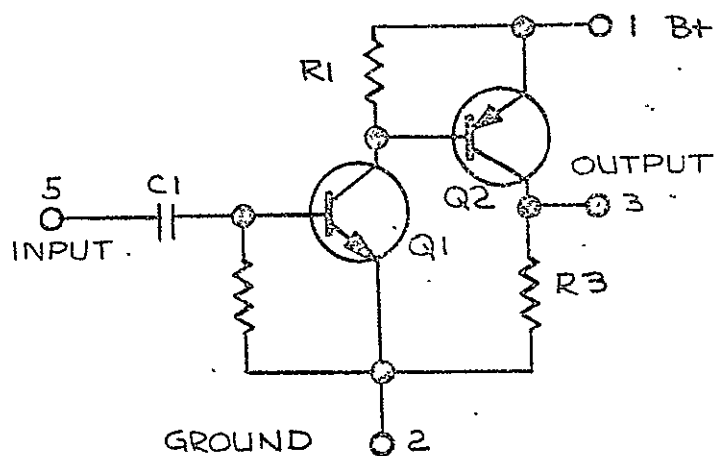


NAND LADDER DRIVER

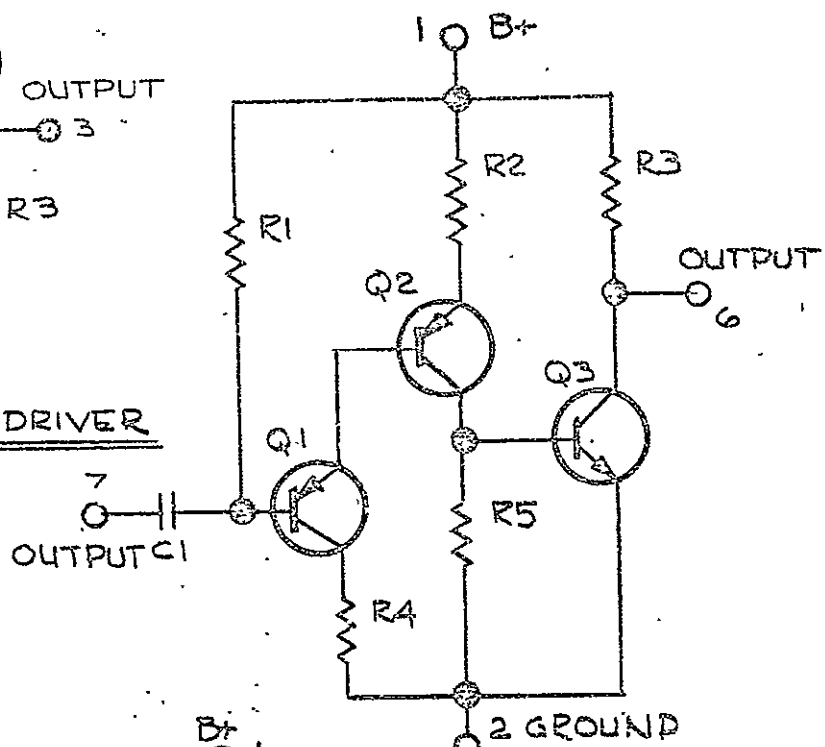


DUAL INVERTER LADDER DRIVER

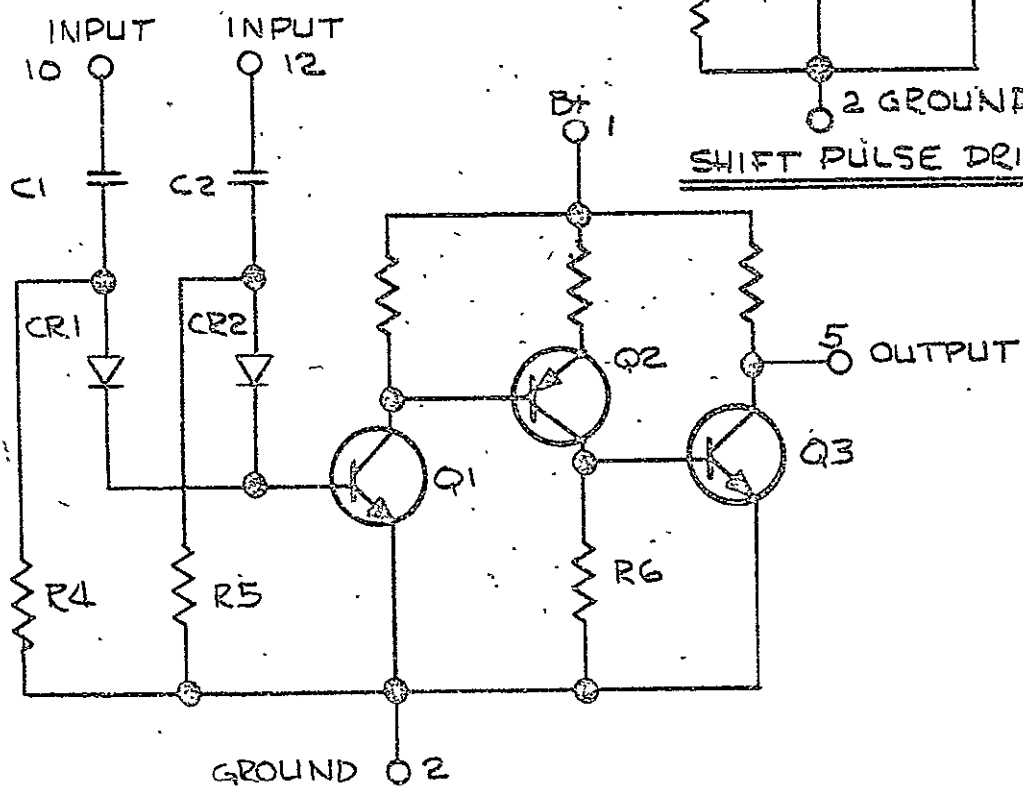
FIGURE 24 D



TRANSFER PULSE DRIVER

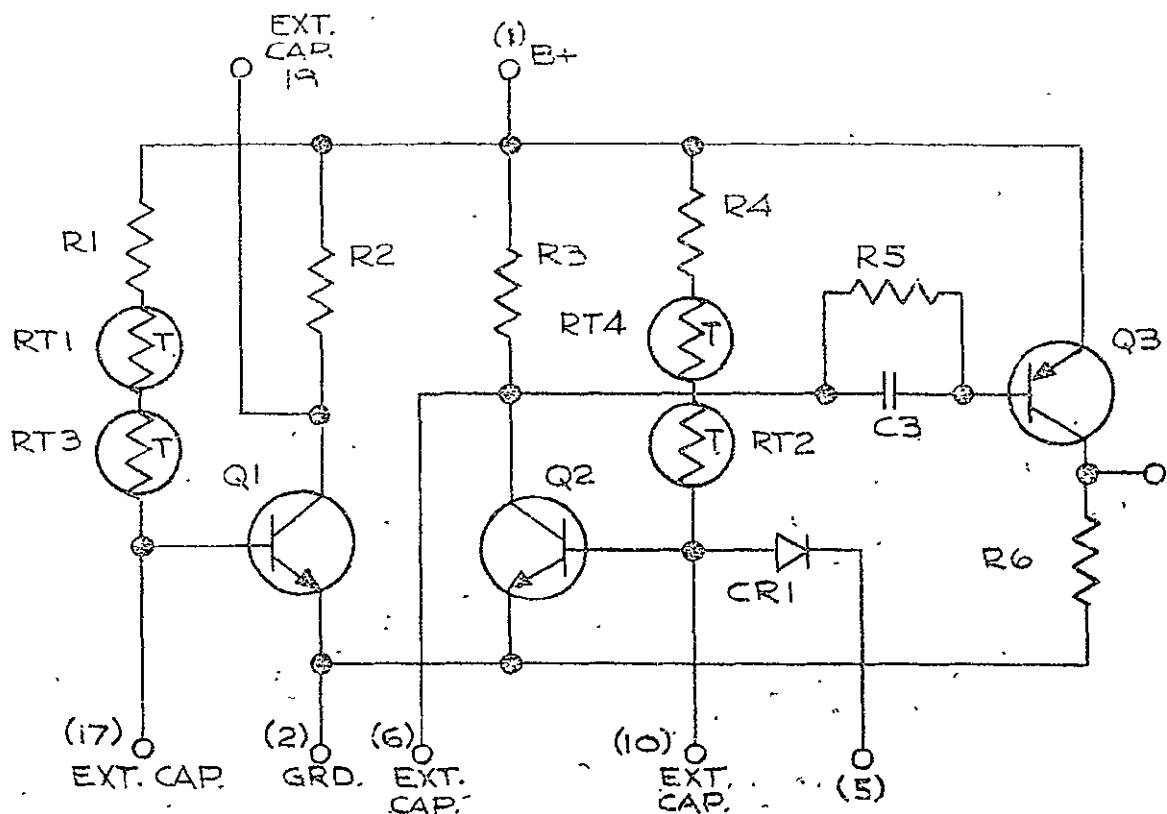


SHIFT PULSE DRIVER

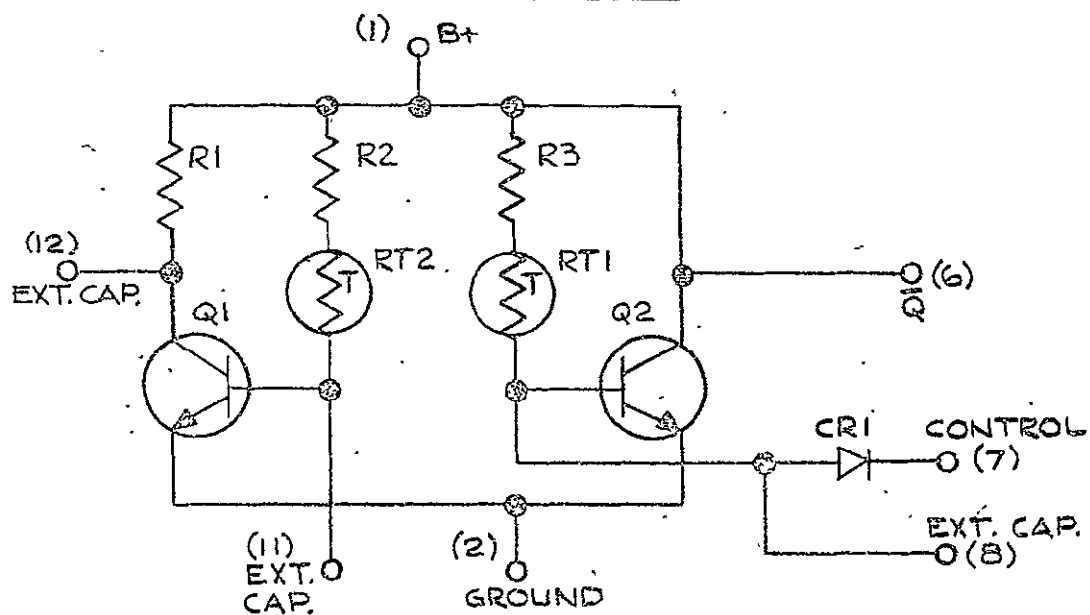


T.O.F. DRIVER

FIGURE 24 E

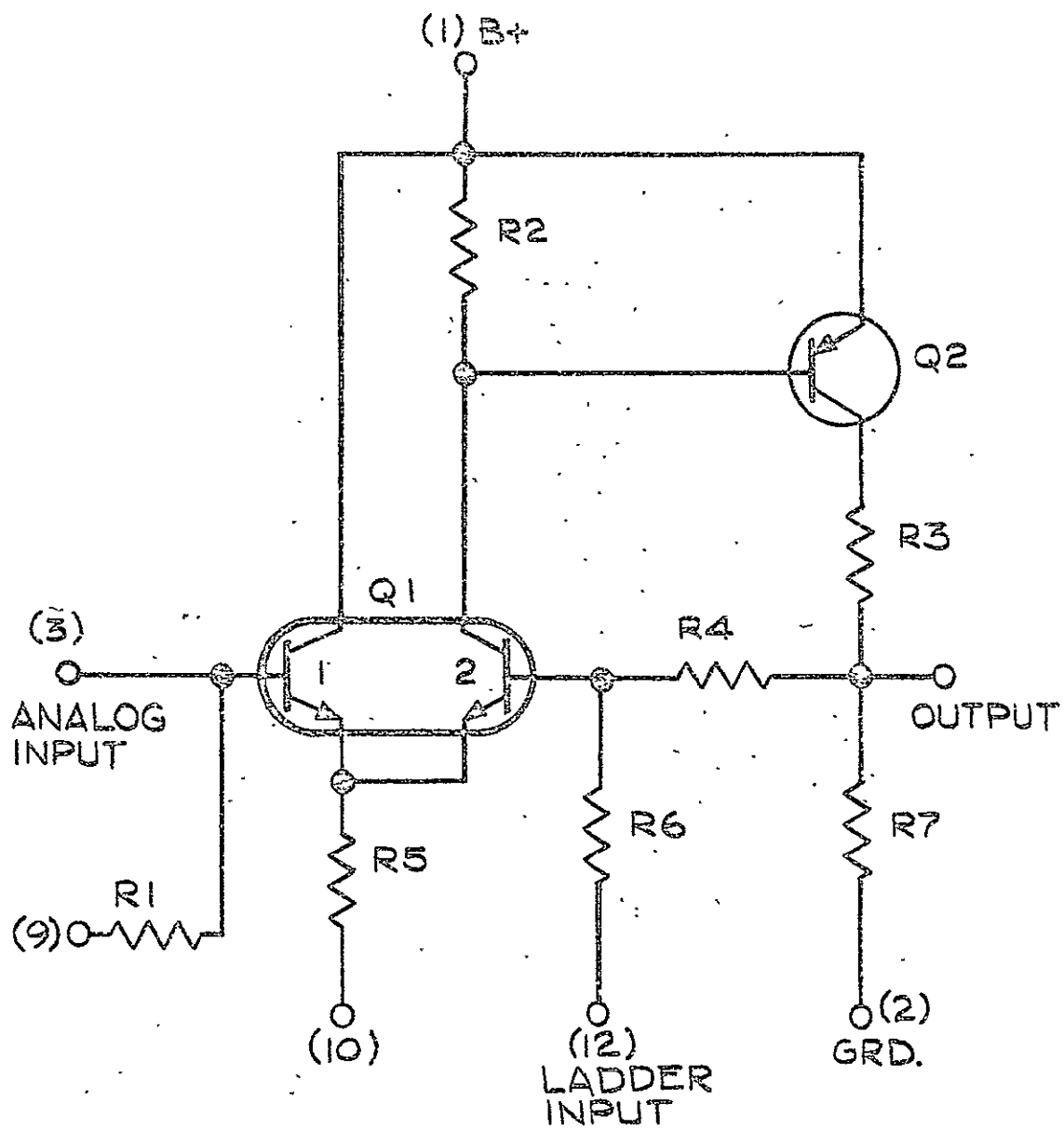


64 KC CLOCK

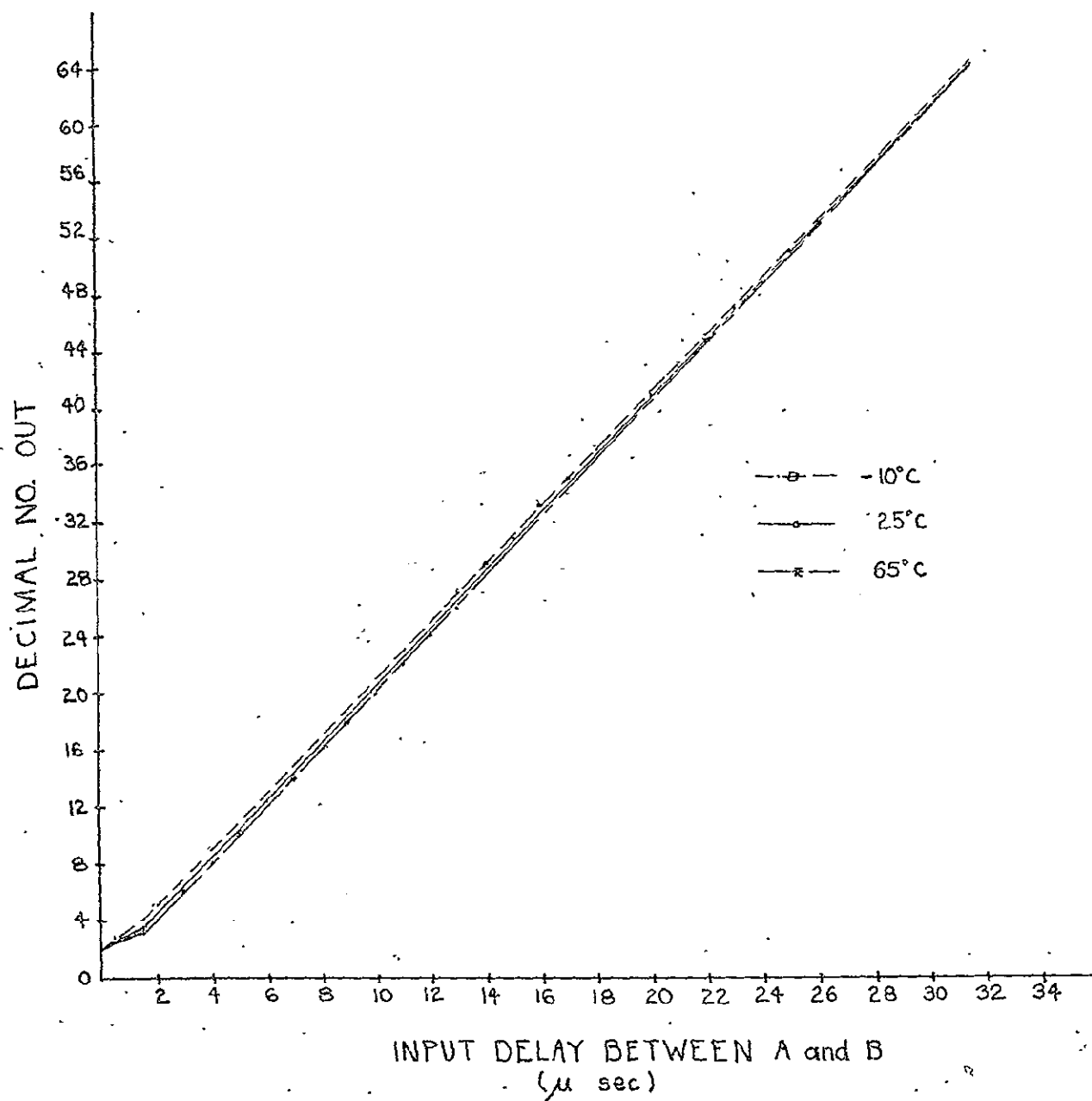


2 MC CLOCK

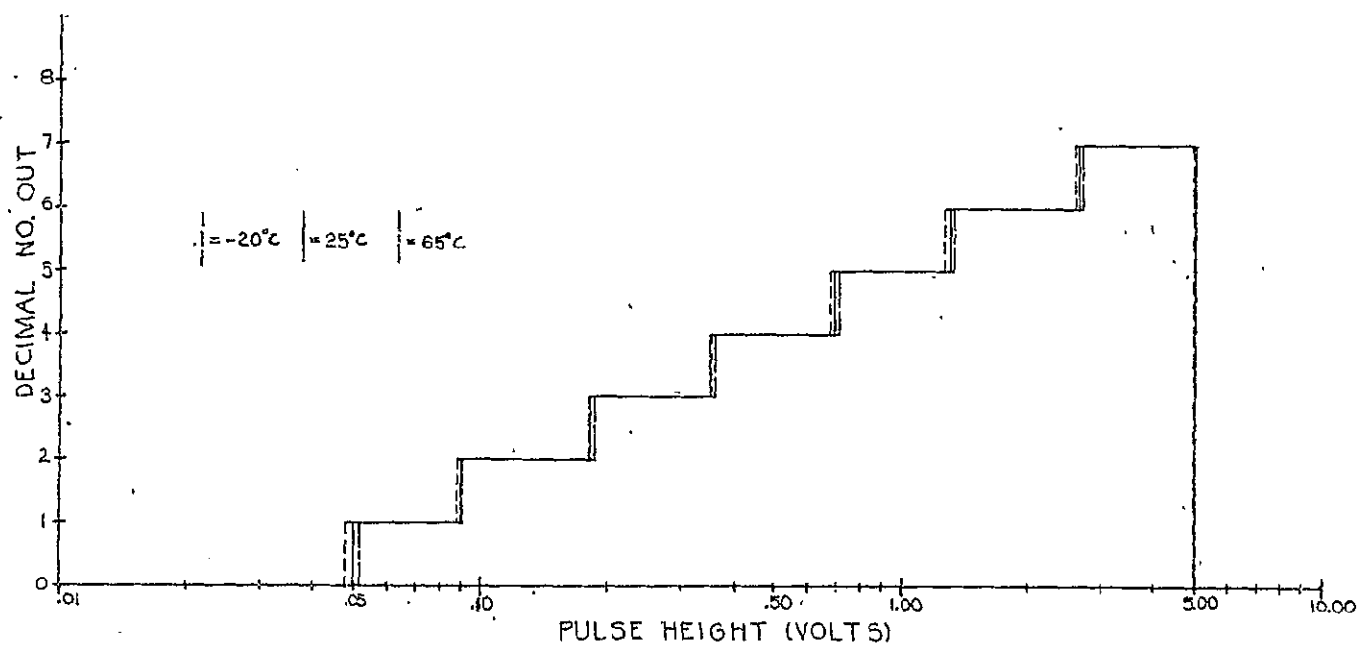
FIGURE 24 F



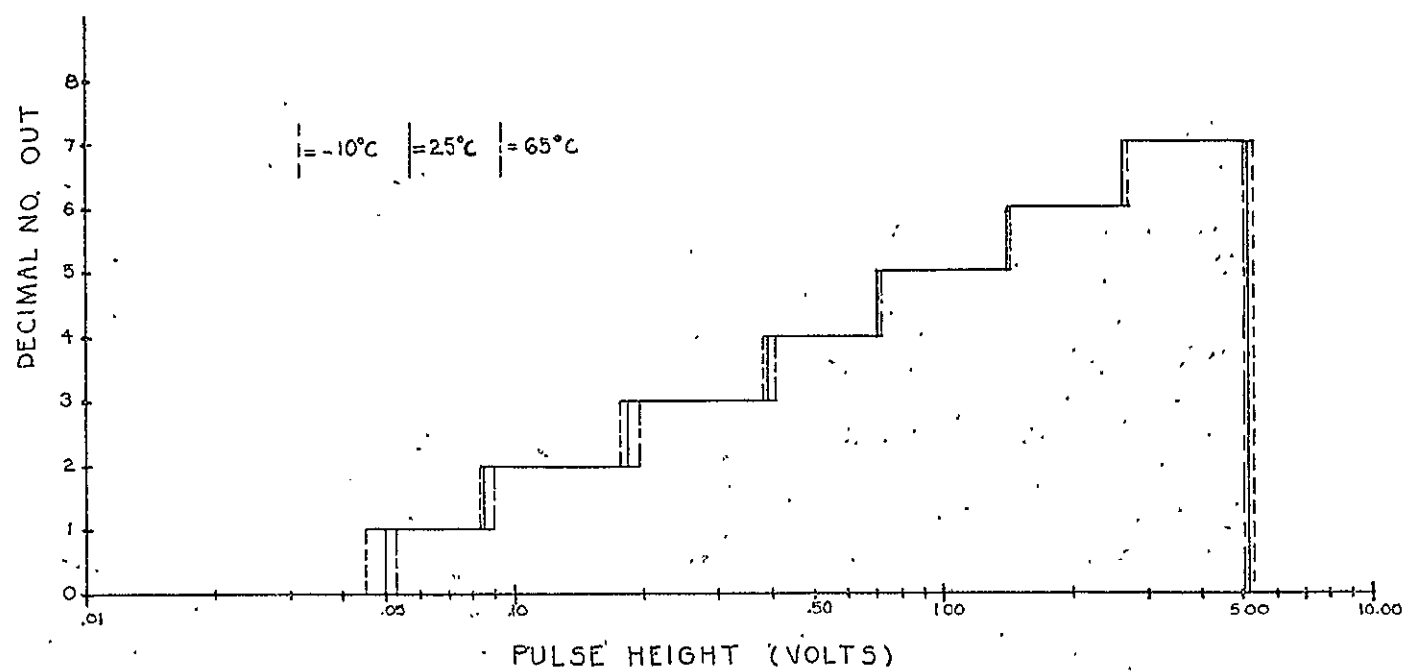
COMPARATOR
FIGURE 24 G



TIME-OF-FLIGHT CALIBRATION
FIGURE 25



MICROPHONE PULSE HEIGHT ANALYZER CALIBRATION
FIGURE 26



B-PULSE HEIGHT ANALYZER CALIBRATION
FIGURE 27

CUMULATIVE DUST PARTICLE FLUX IN INTERPLANETARY, CIS-LUNAR AND SELENOCENTRIC SPACE

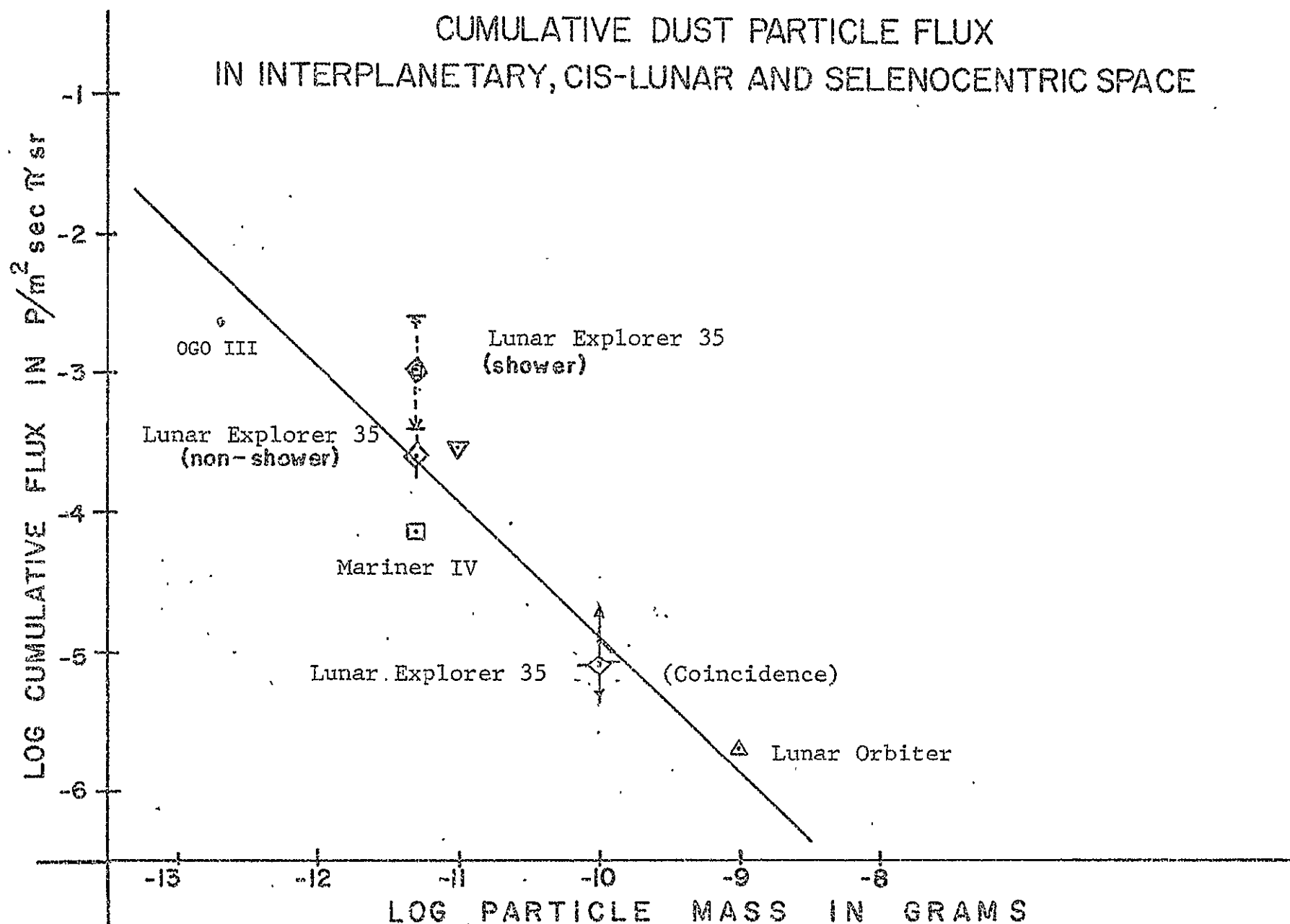


FIGURE 28

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