NASA Case No. MFS-20935-1

NOTICE Publish: Fig. 1

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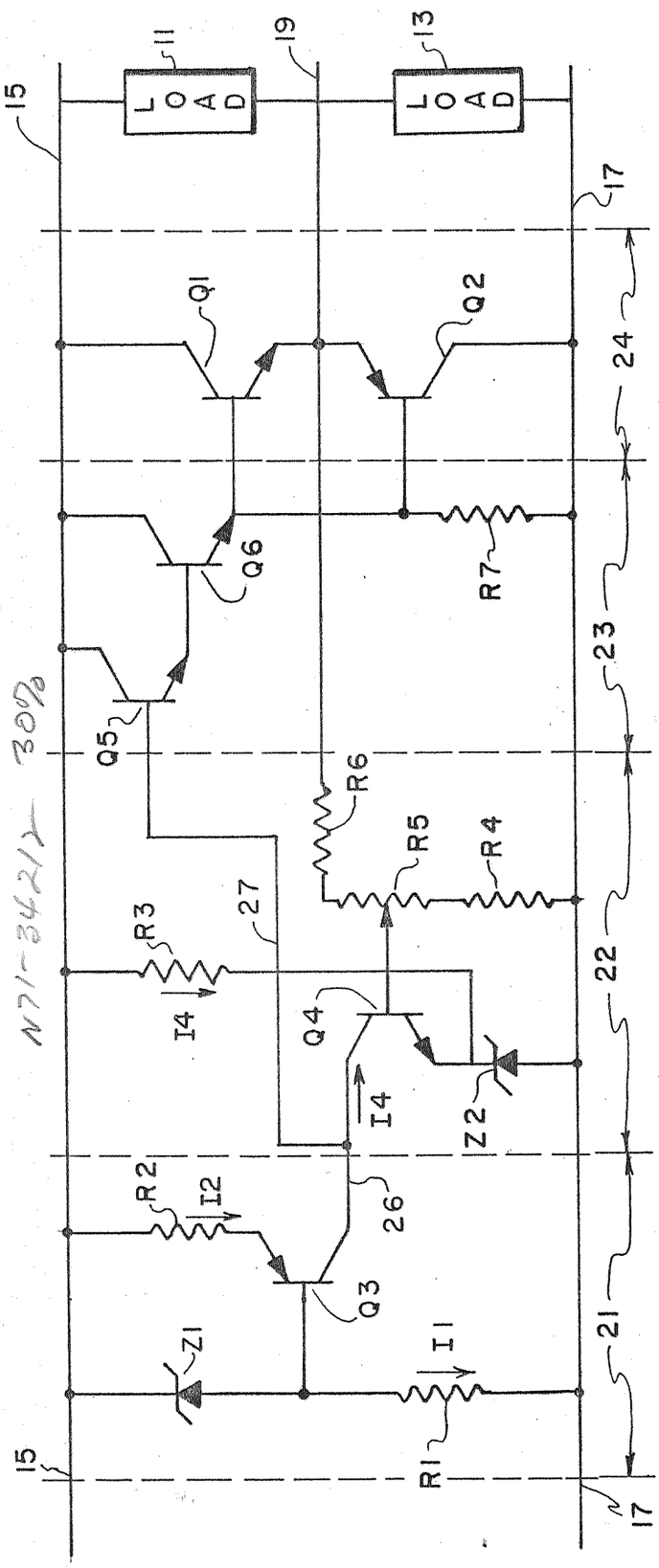

N71-34212 30pp

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MSFC - Form 3055 (February 1968)

CASE # MFS-20935
CURRENT REGULATING VOLTAGE DIVIDER
SH 1 OF 1

NASA Case No. MFS-20935
Marshall Space Flight Center

TECHNICAL ABSTRACT

OF

Current Regulating Voltage Divider

The invention relates to voltage regulation systems and more specifically to a voltage control system which regulates by shunting the load current.

As shown by the single figure of the drawing, the current regulator 24 provides a voltage control between a center line 19 and a more positive input line 15 and a lesser positive voltage input line 17. The system has a conventional voltage sampling stage 22 for the center line 19 as well as conventional preregulator 21 and driver 23 stages. The loads between the center line 19 and the two input lines 15, 17 are each shunted by a transistor Q1 or Q2 whose base voltage is determined by the driver stage 23, and which voltage is normally at a level to turn the transistors off. The transistors Q1, Q2 are of the opposite conducting type and when the loads vary so as to change the center line voltage 19, the proper transistor comes on to supply or pass the necessary current to maintain the line voltage level.

The novelty of the invention lies in the arrangement of transistors Q1 and Q2 with respect to the load whereby a novel system of dividing voltage levels has been accomplished by regulating current flow, which aside from small leakage and regulation losses, has a power loss determined by the imbalance in current requirements for the loads. Herebefore, circuits to divide current required that the power loss in the circuit be a significant part of the total power usage.

Inventor: Howard B. Hester

Employer: Marshall Space Flight Center

Application Filed: April 21, 1971

Serial No. 136007

APPLICATION FOR LETTERS PATENT

TO ALL WHOM IT MAY CONCERN:

BE IT KNOWN THAT Howard B. Hester, citizen of the United States of America, resident of Huntsville, Madison County, Alabama, has invented certain new and useful improvements in CURRENT REGULATING VOLTAGE DIVIDER of which the following is a specification:

SUMMARY OF THE INVENTION

The present invention provides a voltage control between a center line and a more positive voltage input line and a lesser positive voltage input line. The control provides a conventional voltage sampling means for the center line, as well as conventional preregulator, comparison, and driver stages. The loads between the center line and two input lines are each shunted by a transistor whose base voltage is determined by the driver stage, and which voltage is normally at a level to turn the transistors off. The transistors are of the opposite conducting type and when the loads vary so as to change the center line voltage, the proper transistor comes on to supply or pass the necessary current to maintain the center line voltage level.

Accordingly, it is an object of the present invention to provide a current regulating voltage divider.

Another object is to provide a voltage divider system that has a power loss determined substantially by the imbalance in current requirements of the loads.

Other objects, features, and advantages of the invention will become apparent as the description proceeds.

BRIEF DESCRIPTION OF THE DRAWINGS

The single Figure of the drawings schematically illustrates the present invention.

DESCRIPTION OF THE PREFERRED EMBODIMENT

Referring now to the single Figure wherein it is shown two input lines 15 and 17, one relatively negative and the other relatively positive, having a substantially constant voltage difference. A center line 19 is also provided which has voltage level intermediate of the two input lines. A first electrical

load 11 extends between the center line 19 and the positive input line 15 and a second electrical load 13 extends between the center line 19 and the negative input line 17.

The present invention provides a current regulator 24 having two opposite conducting transistors Q1 and Q2 to shunt the loads 11 and 13 and supply or pass current necessary to maintain the voltage level of the center line 19 substantially constant. The transistors Q1 and Q2 are normally biased off. The transistors are controlled by a preregulator 21, comparison reference and sampling 22, and driver 23 stages.

The preregulator 21 uses a series arrangement of a zener diode Z1 and resistor R1 across the input lines 15, 17 to establish a voltage level between the two which is a level above line 19 by several volts. To keep the power lost in the circuit low, resistor R1 is chosen sufficiently large to reduce the current I1 therethrough as much as possible. But current I1 must be kept large enough that zener diode Z1 is in the zener region. Resistor R2 is placed between the emitter of PNP transistor Q3 and the positive input line 15 to provide a voltage drop that causes transistor Q3 to decrease or increase the current flow I2 so that a substantial constant current flow is maintained. Resistor R2 is chosen as large as possible, but just low enough to pass sufficient current to drive transistor Q5.

The collector of PNP transistor Q3 is joined to the collector of NPN transistor Q4 of the comparison stage 22. The emitter of transistor Q4 is connected between zener diode 22 and resistor R3, which are serially connected between the two input lines 15, 17 to provide a constant emitter voltage. Resistor R3 is chosen large as possible but must be low enough to pass current I3 at a level significant larger than the current I4 passing through transistor Q4, which is approximately the same as current I2 passing through resistor R2.

Resistors R4, R5, and R6 are serially connected between the center line 19 and the negative input line 17 to sample the voltage of line 19. The resistors R4, R5, and R6 are chosen so that their sum is large and voltage level of the center of variable resistor R5 is approximately equal under current flow to the voltage level of zener diode Z2, but the current flow is large enough to control transistor Q4. Variable Resistor R5 is set to provide a base voltage for transistor Q4 very close to the constant emitter voltage so that slight decreases in the voltage level of the center line causes transistor Q4 to effectively increase or decrease its resistance between its emitter and collector. As the current flow to the collector of transistor Q4 from the preregulator 21 is substantially constant, the increasing or decreasing resistance action of transistor Q4 causes a corresponding increase or decrease in the voltage level between the collectors of transistors Q3, Q4 and the input lines.

The voltage from the connecting line 26 between the transistors Q3 and Q4 is applied by line 27 to the base of transistor Q5 of the driver stage 23, which consists of transistors Q5 and Q6 in an emitter follower configuration serially connected with resistor R7 across the input lines 15, 17. The variation in base voltage of transistor Q6 sets the intermediate voltage desired for operating the control NPN transistor Q1 and PNP transistor Q2.

The components of the circuit are selected whereby transistors Q1 and Q2 are off when the loads are operating at a designed level. However, if load 11 should tend to increase (decrease resistance), for example, the intermediate voltage of the center line will tend to raise to a higher positive value, which is detected by the reference sampling stage 22, and the base of the control transistors Q1 and Q2 will be caused to become more negative by the action of driver transistors Q5 and Q6 decreasing the

current flow through resistor R7. This will result in PNP transistor Q2 being biased on to shunt current around load 13 so as to maintain the center line voltage level. Transistor Q1 will remain off in this situation. If load 13 decreased, the base of the control transistors Q1 and Q2 will become more positive causing NPN transistor Q1 to be biased on and PNP transistor Q2 to remain off so current is shunted about load 11 to maintain the center line voltage level.

It is now believed apparent that a novel system of dividing voltage levels has been disclosed which aside from small leakage and regulation losses, has a power loss determined by the imbalance in current requirements of the loads. It is, therefore, to be understood that within the scope of the appended claims, the invention may be practiced other than as specifically described.