

General Disclaimer

One or more of the Following Statements may affect this Document

- This document has been reproduced from the best copy furnished by the organizational source. It is being released in the interest of making available as much information as possible.
- This document may contain data, which exceeds the sheet parameters. It was furnished in this condition by the organizational source and is the best copy available.
- This document may contain tone-on-tone or color graphs, charts and/or pictures, which have been reproduced in black and white.
- This document is paginated as submitted by the original source.
- Portions of this document are not fully legible due to the historical nature of some of the material. However, it is the best reproduction available from the original submission.

RELIABILITY STUDIES IN SEMICONDUCTOR FABRICATION

Final Technical Report
NASA Grant NGR 05-010-041

CR-119800

Solid-State Laboratory
Department of Electrical Engineering
University of California, Santa Barbara



BACKGROUND:

The NASA Grant NGR 05-010-041 was awarded to the University of California, Santa Barbara for a period of approximately one year beginning about 1 April 1969. The Grant title, "Reliability Studies in Semiconductor Fabrication," was to be conducted under the direction of Drs. P. F. Ordnung and J. G. Skalnik, and was for a total of \$14,859.

A request was made by the University of California, Santa Barbara on 25 March 1970 to extend the period of the subject grant. The extension was granted to 30 September 1970 by means of a letter dated 14 April 1970 from Joseph T. Davis, Grants Officer.

Our first grant monitor was Mr. Jeffrey J. Bowe, Code TCP, NASA/ERC, 575 Technology Square, Cambridge, Mass. Our second and current grant monitor is Mr. C. Gentry Miles, Code S&E-R, Research Planning Office, George C. Marshall Space Flight Center, Marshall Space Flight Center, Alabama, 35812.

Our first technical report was dated 21 November 1969. The title was, "A Study of High-Temperature BBr₃ Deposition," and entailed a detailed study of the characterization and calibration of a BBr₃ deposition-furnace system. Briefly, the fifty-page report presented the results of the measurements of oxide thickness and V/I for a series of silicon wafers subjected to a variety of operating conditions. Curves of oxide thickness and V/I were plotted as a function of dope-N₂ flow rate, moist-oxygen flow rate, wet-oxygen

63	63
(THRU)	(CODE)
2	2
(ACCESSION NUMBER)	(CATEGORY)
17	CR 119800
(PAGES)	(NASA CR OR TMX OR AD NUMBER)

flow rate, warm-up time, dope time, purge time and furnace temperature.

Our second technical report was dated 27 April 1970. The second technical report was a short letter report that described briefly our progress on an antimony buried-layer system and an epitaxial-reactor system. This letter report also mentioned a study of furnace-room contamination sources and cleaning procedures.

Our third technical report was dated 6 August 1970, and was a 20-page report entitled, "Furnace-Tube Contamination." Briefly, the report described the construction and testing of a series of silicon p-n diodes in order to first isolate and then prove the elimination of furnace-tube contamination. Contamination is measured essentially by means of the observation of diode reverse-leakage current.

This present document represents the fourth and final technical report on NASA Grant NGR 05-010-041.

DESCRIPTION OF FINAL REPORT:

The fourth and final technical report is a 38-page report entitled, "Profiling Procedures: I. Anodic Oxidation. II. OLS-Profile-Program. Five copies of the report are included with this fourth and final submission.

Prior to the formal ending date, 30 September 1970, of Grant NGR 05-010-041, we were engaged in further work on the BBr_3 deposition process. The first technical report covered the measurement of oxide thickness and V/I as a function of several BBr_3 system parameters. The additional work on the BBr_3 process involved the extension of the measurements to include the determination of junction depth, x_j , as a function of the system parameters.

Our initial efforts to measure x_j by grooving and staining led to seemingly erratic results in which the x_j did not appear to increase smoothly with increase or monotonic change in system parameters. In an attempt to resolve the difficulty, many additional silicon wafers were processed through the BBr_3

deposition system. These additional wafers were subjected to an anodic-oxidation process in an attempt to measure x_j much more accurately than possible by use of the staining-and-grooving process.

The anodic-oxidation procedure is described in detail on pages 4 through 9 of the enclosed fourth and final report. Photographs of the actual apparatus are shown in Fig. 1 of the enclosed report. Briefly, the anodic-oxidation process is one by means of which silicon-oxide is grown on the surface of a silicon wafer through which impurities have been diffused. The oxide growth is produced by the process of using the silicon wafer as one electrical terminal of an electrolytic process.

After a short cycle of oxide growth, the oxide is etched from the wafer surface by use of a standard HF etch. A V/I measurement is made on the exposed surface. In a broad sense, the V/I measurement indicates the total impurities in the wafer in the region from the surface to the position of the junction, x_j . Successive oxidations, etchings, and V/I measurements gradually lead to an accurate determination of the position of the junction.

The series of V/I measurements made between steps of anodic oxidation serve also to measure or delineate the profile of impurities in the region from the original wafer surface to the position of the junction. Since the profile shape, as well as the value of x_j , is desired information, a computer program was established to allow accurate and convenient calculations of the profile shape from the experimental measurements of anodic-oxide thickness and V/I. The computer program was prepared for use on the UC-Santa Barbara, on-line, time-shared system (OLS).

The OLS procedure is described in detail on pages 11 through 38 of the enclosed fourth and final report. Briefly, it may be noted in Display 8 on page 17 of the enclosed report that the display oscilloscope of the OLS system has instructed the operator to enter his experimental voltage (actually V/I)

readings. Display II on page 19 of the enclosed report instructs the operator to enter his experimental oxide-thickness measurements. After a plea for patience on the part of the operator in Display 13, the computed profile is presented in Displays 14 and 16.

Unfortunately, the refinements of the measurement techniques and the development of fast and accurate computer calculation methods have not yet led to understanding the seemingly erratic behavior of X_j with system parameters. Additional work on this problem is in progress under a new source of funding. Mr. Hormoz Motamedi, who has performed most of the actual processing and calculations and who wrote the report entitled, "Profiling Procedures," will continue to investigate this and related problems.

It is probably appropriate to state that a recent article in the February 1971 issue of the Journal of the Electrochemical Society refers to the erratic change in X_j with system parameters of a boron system. The article is entitled, "Glass Source B Diffusion in Si and SiO_2 " by D. M. Brown and P. R. Kennicott. Brown and Kennicott write that "----junction depths are observed first to increase and then suddenly to decrease with increasing----." Similar erratic behavior has been reported in "Effect of Extremely Thin Nitrogenous Surface Films on Phosphorus-Impurity Profiles in Silicon," by J. Makris, A. Ferris-Prabhu, and M. L. Joshi, in IBM Journal of Research and Development, March (1971) p. 132.

Summary

The NASA Grant NGR 05-010-041 officially covered the time period from 1 April 1969 to 30 September 1970. Four technical reports have been presented, as follows:

1. 21 November 1969 A Study of High-Temperature BBr_3 Deposition.
2. 27 April 1970 A brief letter progress report.
3. 6 August 1970 Furnace-Tube Contamination.
4. April 1971 Profiling Procedures: I. Anodic Oxidation.
II. OLS- Profile Program.

P. F. Ordnung
P. F. Ordnung,

J. G. Skalnik
J. G. Skalnik

APPENDIX

Attached is a copy of a paper to be presented in the Region VI conference in Sacramento in June 1971. The paper is entitled, "Capacitance of P-N Junctions." Related to the general question of studies of profiles of impurity distribution in semiconductors is that of its measurement; such as by capacitance. Many capacitance formulas exist, but the question is: to what do they relate - or, parenthetically, what does the concept of capacitance for a p-n junction mean? Our awareness of this problem grew out of numerical computer studies that were being conducted by Mr. David Heald, Ph.D. candidate and Acting Assistant Professor of Electrical Engineering here in the department.

This led to a thermodynamic derivation of the concept of capacitance. It has been known for a long time that some of the formulas for capacitance do not relate too well to physical experiments performed on junctions. Now that we have a formula that rests on a basic physical derivation, the next step is to check it with a variety of experiments. These will involve generating profiles, carefully measuring them, theoretically computing their capacitance, and then measuring this capacitance. Thus, we hope to provide reliable correlation between theory and measurement.

We hope to find support for this effort. It is clearly related to the reliability studies called for in the present contract.

David L. Heald, Philip F. Ordnung, John G. Skalnik
University of California, Santa Barbara

NQR-05-010-041

ABSTRACT

An area of considerable interest and significance is that of the theory and calculation of incremental capacitance of p-n junctions. The literature includes several different viewpoints concerning the details of the concept of capacitance of p-n junctions. In addition, the incremental capacitance of a p-n junction with an arbitrary doping profile is difficult to calculate accurately.

In this paper, the nature of the capacitance of a p-n junction is explored. After a review of several formulations available in the literature, a thermodynamic derivation of the capacitance is presented and discussed. A numerical comparison is given for the capacitance calculated by use of various formulations. The numerical solutions are presented for an asymmetrical step junction.

Concept of the Capacitance of a P-N Junction.

In this paper the term junction capacitance and the symbol C_t refer to the total incremental capacitance of p-n junctions. In certain formulations, the capacitance C_t is considered to be composed of the two components of space-charge or depletion capacitance, C_s , and diffusion capacitance, C_d . For large reverse bias, C_t is dominated by C_s . For large forward bias, C_t is dominated by C_d . The difficulty of definition and evaluation C_d and C_s is discussed in the following paragraphs.

The classical first-order expression for the space-charge capacitance of a unit-area step junction is based on the complete depletion approximation and is given by the relation

$$C_s = \sqrt{\frac{qK_s \epsilon_0 N_a N_d}{2(N_a + N_d)\psi_T}} \quad (1)$$

where ψ_T is the sum of the built-in potential and the applied voltage V , N_a is the acceptor density on the p-side, N_d is the donor density on the n-side, q is the electronic charge, and $K_s \epsilon_0$ is the dielectric constant. For linearly graded junctions, a cube-root dependence of C_s on voltage is often quoted; however, as Chang¹ has noted, a more careful analysis for the linearly graded junction also yields a square-root relation between C_s and ψ_T .

In an early step-junction analysis, Chang² calculated capacitance by determining the change in maximum electric field,

E_m , with change in applied voltage. The calculated capacitance agreed with the classical relation (1) for nearly symmetrical junctions, but deviated significantly for strongly asymmetrical junctions.

A typical distribution of net charge density and associated electric field for a p⁺-n step junction is shown in Fig. 1. The plots shown were obtained by numerical computer solutions of the appropriate differential equations for the junction. Characteristically, as clearly shown in Fig. 1, the distribution of net charge density in a p⁺-n step junction exhibits spikes. The spike in the p-side approaches a surface charge characteristic of a metal plate. The spike on the n-side is equivalent to the formation of the inversion layer in a surface device. By inspection of Fig. 1, it may be noted that the depletion region does not extend to the position, x_j , of the metallurgical junction, and that the position of the maximum electric field departs negligibly from x_j .

Gummel and Sharfetter³ observed that Chang's method of calculating the space-charge capacitance of p⁺-n junctions omitted contributions resulting from changes in hole density in the n-layer with changes in applied voltage, V . The nature of the change in hole and electron densities with change in voltage applied to a p⁺-n step junction is shown in Fig. 2. In Fig. 2a, hole and electron distributions are shown for two values of applied forward bias separated by ΔV . In Fig. 2b, the resulting changes in hole and electron distributions are shown. The shaded area in Fig. 2b represents equal changes in the hole and electron densities, and will be negligible in comparison with the remaining area for reverse or small forward bias. The net change in charge with applied voltage is illustrated in Fig. 2c. The position x_e is defined to be the position at which the change in net charge density with V is equal to zero. It may also be noted that x_e is essentially the position at which hole density is equal in magnitude to the electron density.

The change in net charge with applied voltage is further illustrated in Fig. 3. The solid curve in Fig. 3a illustrates the net charge distribution for zero bias. The "plus" and "minus" marks illustrate the change in hole and electron densities for a change in applied voltage. A sketch of the change in hole and electron densities is shown in Fig. 3b. The plot in Fig. 2

is drawn for a large forward bias. The sketch in Fig. 3 is drawn for small change around zero bias.

For a symmetrical junction, x_e will coincide with x_j . By integrating Poisson's equation, one may show that the maximum electric field is at x_j and that change in x_j with voltage accurately reflects the change in charge stored on either side of the junction; that is, the change in E_m with voltage is an accurate measure of the change of charge with voltage on an equivalent "plate" of a capacitor.

For an asymmetrical junction, x_j and x_e will not coincide. The position of x_e is voltage dependent. A capacitance calculation based only on changes with voltage of the electric field at either x_j or the position of maximum electric field accounts for less than the true change in stored charge. An accurate calculation requires the determination at the position x_e of the change in electric field with change in applied voltage. The calculation is complicated by the fact that the position of x_e is voltage dependent.

In a later derivation,¹ Chang modified his original² analysis and developed the following expression for incremental capacitance, C_t , of a p-n junction:

$$C_t = q \int_0^L \frac{dp}{dV} dx = q \int_0^L \frac{dn}{dV} dx \quad (2)$$

In (2), the junction is assumed to be totally enclosed within a semiconductor section of length L .

DeMari⁴ and Arandjelovic⁵ used (2) as the basis of their numerical work. Computational accuracy for either dp/dV or dn/dV is difficult to achieve because of the large dynamic range of numbers encountered in the numerical solution. For example, the subtraction of two successive solutions for the hole density in the neutral p-region should yield zero, as shown in Fig. 2b. However, roundoff error may easily overshadow the important changes in density that occur at the edges of the depletion region.

The first integral in (2) represents an evaluation of the area under the entire curve labelled Δp in Fig. 2b. The shaded area in Fig. 2b will be significant for large forward bias and represents those holes neutralized by electrons. Although these holes do not contribute to net charge density, they will result in a transient component of current when the bias is changed. In order to include the shaded area explicitly in the analytical formula for capacitance, (2) may be rewritten as follows:

$$C_t = q \int_0^L \frac{dp}{dV} dx = q \int_0^{x_e} \frac{d(p-n+N)}{dV} dx$$

$$+ q \int_{x_e}^L \frac{dp}{dV} dx + q \int_0^{x_e} \frac{dn}{dV} dx \quad (3)$$

Since the doping concentration, N , is independent of V , the N -term can be added to (3). The last two terms in (3) are associated with the shaded area in Fig. 2b and are reminiscent of the minority-carrier diffusion capacitance of classical theory. In the first term of (3), $(p-n+N)$ is the net charge density ρ and may be related to electric field by means of Poisson's equation. Thus

$$q \int_0^{x_e} \frac{d(p-n+N)}{dV} dx = q \int_0^{x_e} \frac{dp}{dV} dx = K_s \epsilon_0 \frac{dE(x_e)}{dV} \quad (4)$$

By the substitution of (4) into (3), the capacitance in (2) may be expressed in the following alternate form:

$$C_t = K_s \epsilon_0 \frac{dE(x_e)}{dV} + q \left(\int_0^{x_e} \frac{dn}{dV} dx + \int_{x_e}^L \frac{dp}{dV} dx \right) \quad (5)$$

Since dn/dV and dp/dV in (5) are evaluated in regions of relatively small dynamic range for the variables, (5) may be superior to (2) for the purpose of accurate numerical calculations; however, a major virtue of (5) may be that associated with the grouping of factors. The first term may be identified as the space-charge capacitance, C_s . The second term may be identified as the diffusion capacitance, C_d .

The foregoing discussion has involved a steady-state analysis. According to Gummel and Scharfetter³, the experimentally measured small-signal, low frequency capacitance matches reasonably well the space-charge capacitance given in (5) for reverse bias, small-forward bias, and low frequency. When appreciable forward current flows, diffusion capacitance must be included.

By use of the conventional depletion approximation for a long-base diode, the minority-carrier diffusion capacitance may be calculated by integrating dn/dV over the neutral p-region and dp/dV over the neutral n-region. An alternate, small-signal, low-frequency analysis yields a diffusion capacitance that is half that calculated by the integration procedure. Decreasing the storage of minority carriers in the neutral regions is accomplished by a current flow in the external circuit. Some of the carriers may be removed by external current flow, but some will recombine with majority carriers and the disappearance will not be detected as current in the external circuit. Accordingly, the capacitance calculated on the basis of a small-signal theory is smaller than that calculated by the integration procedure. For higher frequencies, ($\omega\tau \gg 1.0$), recombination will not be able to follow the

If the depletion approximation were used to calculate diffusion capacitance, the shaded area of Fig. 2 in the depletion region would be omitted from the calculation. Since (5) does not involve use of the depletion approximation, the diffusion capacitance calculated by use of (5) will differ somewhat from that calculated by use of the depletion approximation.

A substantially different incremental capacitance calculation was made by Kennedy, Coley, and Kleinfelder.⁶ Their calculation is based upon the following equation.

$$C_t = \frac{1}{V} \frac{d}{dV} \left[\frac{K_s \epsilon_0}{2} \int_0^L E^2 dx \right] \quad (6)$$

For a given value of V, the term within the brackets represents the total energy stored in electrostatic field in the semiconductor. Thus Kennedy, et al. have related the incremental capacitance to the rate of change with voltage of the total electrostatically stored energy in the semiconductor.

Philosophical Comments on Capacitance.

It is clear that several methods exist for the calculation of capacitance. It is not clear how these methods compare. A philosophically sound method should relate capacitance to some fundamental circuit property. For example, one concept of incremental capacitance would be the ratio of the change in charge supplied to a junction in response to the change in voltage applied across it. From another viewpoint, one might compute incremental capacitance by computing the total change in stored energy that results from a change in applied terminal voltage. Stored-energy calculation might be based upon the following equation.

$$\Delta W = \frac{1}{2} C_t (V + \Delta V)^2 - \frac{1}{2} C_t V^2 \quad (7)$$

is the increase in stored energy when the terminal voltage is increased from V to V + ΔV. If V ≠ 0 and ΔV is small enough so that C_t remains reasonably constant over ΔV, Eq. (7) may be solved as follows:

$$C_t = \frac{1}{V} \frac{\Delta W}{\Delta V} \quad (8)$$

It might appear from (8) that the calculation of incremental capacitance from energy concepts is that which Kennedy, et al. have used. In fact, (6) and (8) differ because the total stored energy is not the same as the energy stored in the electrostatic field. The most obvious difference exists in a junction under thermodynamic

A Thermodynamic Derivation of Incremental Capacitance.

Thermodynamically⁷ the energy ΔW (in electron volts) added to a system by a process of adding Δn particles to a point in the system where each particle has a potential of μ electron volts is given as follows:

$$\Delta W = \mu \Delta n \quad (9)$$

Implicit in the process is the transport of a particle from a place at which the potential energy is zero; i.e., a point well removed from the system, to the point in question. In a system with several different kinds of particles, each will have its own potential. Then the energy added by augmenting the number of each kind may be computed by an extension of the process defined in (9).

In a semiconductor the particles consist of electrons and holes (the absence of electrons). If electrons are moved from an outside point to a point within the semiconductor where a potential of μⁿ electron volts exists, then μⁿ electron volts of energy are added per added electron. A hole is produced at a point by removing an electron from that point. Thus the addition of holes to a point where the potential is μ^p corresponds to a loss of energy from the system in the amount μ^p electron volts per hole. If both electrons and holes in respective quantities Δn and Δp are added where the respective potentials are μⁿ and μ^p, the net energy added to the system is expressed as follows:

$$\Delta W = \mu^n \Delta n - \mu^p \Delta p \quad (10)$$

If electron and hole densities are added throughout a device; i.e., Δn and Δp are both functions of x as are both μⁿ and μ^p, the energy added over the length, L, of the device is expressed as follows:

$$\Delta W = \int_0^L (\mu^n \Delta n - \mu^p \Delta p) dx \quad (11)$$

Moreover if the changes in the electron and hole populations occur in response to a change in terminal voltage ΔV that is applied between the ends of the device, the rate of change of energy added with respect to applied voltage may be expressed as in the following equation in which the limit as the increments go to zero has been taken

$$\frac{dW}{dV} = \int_0^L \left[\mu^n \frac{dn}{dV} - \mu^p \frac{dp}{dV} \right] dx \quad (12)$$

over a set of energy levels. The distribution will be such that the energy added may be computed as the product of a single number μ^n with Δn .⁸ Likewise a set of holes added at a point x will be distributed over a set of energy levels such that the energy loss is the product of a single number μ^p with Δp . Then the quantities μ^n and μ^p are known as the electrochemical potentials (or quasi-Fermi levels or imrefs) respectively of electrons and holes.

An electrochemical potential consists of two independent parts--namely, an electrical potential energy per particle that results from the existence of electrical fields and a chemical potential energy that results from the chemical fields of the particle. Thus the electrochemical potentials μ^n and μ^p may be expressed as follows:

$$\begin{aligned} \mu^n &= -q\psi(x) & + & & q\phi^n(x) \\ &\text{electrostatic} & & & \text{chemical energy} \\ &\text{energy of an} & & & \text{of an electron} \\ &\text{electron at } x. & & & \text{at } x. \end{aligned} \quad (13)$$

$$\begin{aligned} \mu^p &= -q\psi(x) & + & & q\phi^p(x) \\ &\text{electrostatic} & & & \text{chemical energy} \\ &\text{energy of an} & & & \text{of an electron} \\ &\text{electron at } x & & & \text{at } x \text{ where a} \\ &\text{where a hole} & & & \text{hole is located.} \\ &\text{is located.} & & & \end{aligned}$$

In these equations q is the magnitude of the electronic charge, $\psi(x)$ is the electric potential at x , and ϕ^n and ϕ^p are the chemical potentials.

The electric potential $\psi(x)$ is related in a conventional manner to electrostatic field theory. The chemical potentials are related to the statistics of the electron and hole distributions within the semiconductors. Under the assumption that the semiconductor is nondegeneratively doped so that Maxwell-Boltzman statistics apply, the values of the chemical potentials ϕ^n and ϕ^p are given as follows:

$$\begin{aligned} \phi^n(x) &= \frac{kT}{q} \ln \left(\frac{n}{n_i} \right) \\ \phi^p(x) &= - \frac{kT}{q} \ln \left(\frac{p}{n_i} \right) \end{aligned} \quad (14)$$

where k is Boltzman's constant, T is temperature, and n_i is the intrinsic carrier concentration.

At this point, the rate of change with respect to V of energy added to a semiconductor may be shown to consist of two components: the rate of change with respect to V of energy added to the electric field and to the chemical field. A substi-

$$\begin{aligned} \frac{dV}{dx} &= \int_0^L q\psi(x) \left(\frac{dn}{dV} - \frac{dp}{dV} \right) dx \\ &+ \int_0^L q \left(\phi^n \frac{dn}{dV} - \phi^p \frac{dp}{dV} \right) dx \end{aligned} \quad (15)$$

The significance of the first term in (15) can be recognized as follows:

The rate of change with V of energy added to the electric field

$$= \int_0^L q\psi(x) \left(\frac{dn}{dV} - \frac{dp}{dV} \right) dx \quad (16a)$$

The significance of the second term in (15) can be recognized by analogy to (16a) as follows:

The rate of change with V of energy added to the chemical field

$$= \int_0^L q \left(\phi^n \frac{dn}{dV} - \phi^p \frac{dp}{dV} \right) dx \quad (16b)$$

The incremental capacitance of a semiconductor junction, as obtained from thermodynamic considerations, may therefore be expressed by the substitution of Eqs. (16) into (8). Thus

$$\begin{aligned} C_t &= \frac{1}{V} \left[\begin{array}{l} \text{The rate of change with} \\ \text{V of energy added to the} \\ \text{electric field} \end{array} \right] \\ &+ \frac{1}{V} \left[\begin{array}{l} \text{The rate of change with} \\ \text{V of energy added to the} \\ \text{chemical field} \end{array} \right] \end{aligned} \quad (17)$$

Correspondence of (6) With the First Term in (17).

The first term in (17) corresponds to (6). To show this, and incidentally to strengthen the identifications in (16), the first term in (15) will be transformed. Assuming that the electric field at the boundaries of the device is unaffected by terminal voltage and replacing $(dp/dn) - (dn/dV)$ with dp/dV , one may perform an integration by parts*.

* In order to perform the integration, let $u = \psi$ so $du = \frac{d\psi}{dx} dx = -E dx$ and let $dv = q \frac{d}{dV} (p dx)$ so that $v = q \frac{d}{dV} \int_0^x p d\tau$. But $\int_0^x p d\tau = K_s \epsilon_0 E(x)$. Thus the integration by parts yields

By means of (18), the first term in (17) has been shown to be identical with (6). Thus (6) should be accurate in those regions of applied voltage for which the first term in (17) dominates C_t .

Thermodynamic Considerations of the Relative Sizes of Terms in (17).

A p-n junction in equilibrium internally and with its environment will be in a state of lowest energy. While it will contain both electrically and chemically stored energy, net energy cannot be taken from the junction without violating the laws of thermodynamics. If a bias, forward or reverse, is applied to a junction in equilibrium, the effect is to cause an increase in stored energy. The biasing source supplies this energy which is stored in the electrical and chemical fields.

These two components of stored energy may be calculated by rewriting (15) as

$$\frac{dW}{dV} = \frac{d}{dV} \left[\frac{K_s \epsilon_0}{2} \int_0^L E^2 dx \right] + kT \int_0^L \left[\ln\left(\frac{p}{n_i}\right) \frac{dp}{dV} + \ln\left(\frac{n}{n_i}\right) \frac{dn}{dV} \right] dx \quad (19)$$

in which (14) and (18) have been used. By means of identity

$$\frac{d}{dx} (y \ln y - y) = \ln y \frac{dy}{dx}$$

the second term in (19) may be transformed to yield

$$\frac{dW}{dV} = \frac{d}{dV} \left[\frac{K_s \epsilon_0}{2} \int_0^L E^2 dx \right] + kT \frac{d}{dV} \left[\int_0^L \left[p \ln\left(\frac{p}{n_i}\right) - p + n \ln\left(\frac{n}{n_i}\right) - n \right] dx \right] \quad (20)$$

The first term in the brackets has previously been established as the total electrostatically stored energy for a given voltage V . By analogy, the second term within the brackets is recognized as the total chemically stored energy for a given V .

$$\int_0^L q \psi \frac{dp}{dV} dx = \psi q \frac{dE}{dV} \Big|_0^L + K_s \epsilon_0 q \int_0^L E \frac{dE}{dV} dx$$

The first term on the right is zero as stated in the text. By recognizing that

$$\int_0^L E \frac{dE}{dV} dx = \frac{1}{2} \frac{d}{dV} \int_0^L E^2 dx, \text{ one may transform the second term to yield the right side of (18).}$$

zero when $V = 0$, the integration constant is taken as the negative of the sum of the electrically and chemically stored energies at $V = 0$. The integration of (20) yields a result that may be expressed as follows:

$$W = \left[\begin{array}{l} \text{Total electrostatically} \\ \text{stored energy} \end{array} \right] - \left[\begin{array}{l} \text{Electrostatically stored} \\ \text{energy at } V = 0 \end{array} \right] + \left[\begin{array}{l} \text{Total chemically stored} \\ \text{energy at } V \end{array} \right] - \left[\begin{array}{l} \text{Chemically stored energy} \\ \text{at } V = 0 \end{array} \right] \quad (21)$$

If the electric field distribution for equilibrium conditions is denoted as E_0 , the electrostatically stored energy at $V = 0$ may be expressed as follows:

$$\text{Electrostatically stored energy at } V = 0 = \frac{K_s \epsilon_0}{2} \int_0^L E_0^2 dx \quad (22)$$

With the aid of (22), the available energy (21) may be expressed in the following form:

$$W = \frac{K_s \epsilon_0}{2} \int_0^L (E^2 - E_0^2) dx + \left[\begin{array}{l} \text{Chemically stored energy relative to} \\ \text{that at } V=0 \end{array} \right] \quad (23)$$

The first term in (23) is identified as the electrically stored energy relative to that at $V = 0$; hence the identification shown for the second term obtains.

The significant observation at this point is at $V=0$, $W=0$ and that for $V \neq 0$, $W > 0$. For a forward biased junction $E < E_0$. The first term on the right in (23) is then negative. As the forward bias is increased, W increases. It follows that the chemically stored term in (23) must increase in value not only by an amount to represent the value of W but also to compensate the amount by which the first term is negative. This is clearly evident in Fig. 4 where the typical behavior of the chemically and electrically stored energies, as well as the total and available stored energies, are shown as a function of V . Since incremental capacitance is expressed by (17) in terms of the rate of change of energy with V , it is clear from inspection of the curves in Fig. 4 that the chemically stored energy will dominate capacitance for high forward bias and that the electrically stored energy will dominate for high reverse bias.

of computing capacitance, the ambipolar equations were solved on a computer. The procedure involved the following one-dimensional equations:

$$\frac{d^2\psi}{dx^2} = -\frac{q}{K_s \epsilon_0} \rho \quad \text{Poisson's Eq.}$$

$$J_n = q\mu_n n E + qD_n \frac{dn}{dx} \quad \text{Electron Current Eq.}$$

$$J_p = q\mu_p p E - qD_p \frac{dp}{dx} \quad \text{Hole Current Eq.}$$

$$J + \frac{1}{q} \frac{dJ_n}{dx} = 0 \quad \text{Electron Steady-State Continuity Eq.}$$

$$J - \frac{1}{q} \frac{dJ_p}{dx} = 0 \quad \text{Hole Steady-State Continuity Eq.}$$

$$J = \frac{1}{\tau} \frac{pn - n_i^2}{p + n + 2n_i} \quad \text{Shockley-Read-Hall Recombination Model}$$

Current density is denoted by J and the mobility and diffusivity by μ and D respectively. These quantities are subscripted p or n indicating reference to holes or electrons. The material lifetime is given by τ .

Given a set of boundary conditions, the above differential equations were solved for the carrier densities, electric field, and charge density throughout the device (see Figs. 1 - 3). The energy and capacitance computations are then performed. Since the focus is on comparison of capacitance obtained by various methods, the details of the computations are omitted.

Capacitance Comparisons and Conclusions

The capacitance of a p^+-n step junction has been calculated as a function of V by the following methods:

- Classical first-order theory (1)
- Chang's first method (change in maximum electric field with voltage)
- Junction incremental capacitance (5)
- Kennedy's method (6)
- Rate of change of total thermodynamic energy (17)

The results are shown in Fig. 5.

The capacitance as obtained by the various methods will be compared to that which is thermodynamically obtained. In doing so, one must observe that the thermodynamic values, as plotted in Fig. 5, are inaccurate in the neighborhood of $V = 0$. The reason is that as $V \rightarrow 0$, $(1/V) dw/dV$ becomes indeterminate and an appropriate al-

ternative method must be used; the thermodynamic calculations are believed to be accurate.

At large values of reverse bias, Kennedy's method (d) yields the same values as the thermodynamic method (e). The other methods yield smaller values under reverse bias. At $V = 0$, Kennedy's method diverges, fundamentally. For forward bias, the junction incremental capacitance (c) yields the same results as the thermodynamic method.

REFERENCES

- Y.F. Chang, "The Capacitance of $p-n$ Junctions," Solid-State Electronics, Vol. 10, pp. 281-287, 1967.
- Y.F. Chang, "Capacitance of $p-n$ Junctions: Space-Charge Capacitance," J. of Applied Physics, Vol. 37, pp. 2337-2342, 1966.
- H.K. Gummel and D.L. Scharfetter, "Depletion-Layer Capacitance of p^+-n Step Junctions," J. of Applied Physics, Vol. 38, pp. 2148-2153, 1967.
- A. DeMari, Ph.D. Thesis, California Institute of Technology, 1967.
- V. Arandjelovic, "Accurate Numerical Steady-State Solutions for a Diffused One-Dimensional Junction Diode," Solid-State Electronics, Vol. 13, pp. 865-871, 1970.
- D.P. Kennedy, P.C. Murley, W. Kleinfelder, "On the Measurement of Impurity Atom Distributions in Silicon by the Differential Capacitance Technique," IBM J. of Research and Development, Vol. 12, pp. 399-409, 1968.
- A.C. Smith, J.F. Janek, R.B. Adler, Electronic Conduction in Solids, McGraw-Hill, 1967, Sec. 3.4.
- E. Spenke, Electronic Semiconductors, McGraw-Hill, 1958, Chapt. 8.
- D.L. Heald, Ph.D. Thesis, University of California, Santa Barbara, 1971.

Figure 1. p^+-n step junction with corresponding charge density, p , and electric field, E .

Figure 2. a) Hole and electron densities for junction of Fig. 1 for forward bias.* — $V=0.5$ v. --- $V=0.45$ v.
b) Change in hole density, Δp , and in electron density, Δn . c) Net change in charge density, Δp .

*The metallurgical junction is denoted by x_j ; the point at which the change in charge density, Δp , changes sign is denoted by x_e .

Figure 3. a) Charge density for junction in Fig. 1 for $V = 0$. The "plus" and "minus" marks indicate the location and sign of added charge if the bias is increased in the forward direction by ΔV . b) Net change in charge density. A capacitance calculation by (5) for this case is relatively insensitive to the exact location of x_e , in contrast to the high forward bias case of Fig. 2.

Figure 4. Stored energy for the junction of Fig. 1. The units of the energy scale are applicable in an absolute sense only to the available stored energy. The slope of the electrically stored energy tends to zero for large forward bias while that of the chemically stored energy tends to zero for large reverse bias.

Figure 5. Capacitance of the junction of Fig. 1. a) Classical first-order theory (2). b) Change in maximum electric field with voltage. c) Junction incremental capacitance (5). d) Rate of change of electrically stored energy (6). e) Rate of change of total thermodynamically stored energy (17). For the region near $V=0$, between vertical dotted lines, the numerical calculation of capacitance by (e) as performed in this work is inaccurate.

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.

P^+	N
$N_d = 5 \times 10^{16}$	$N_d = 5 \times 10^{14}$

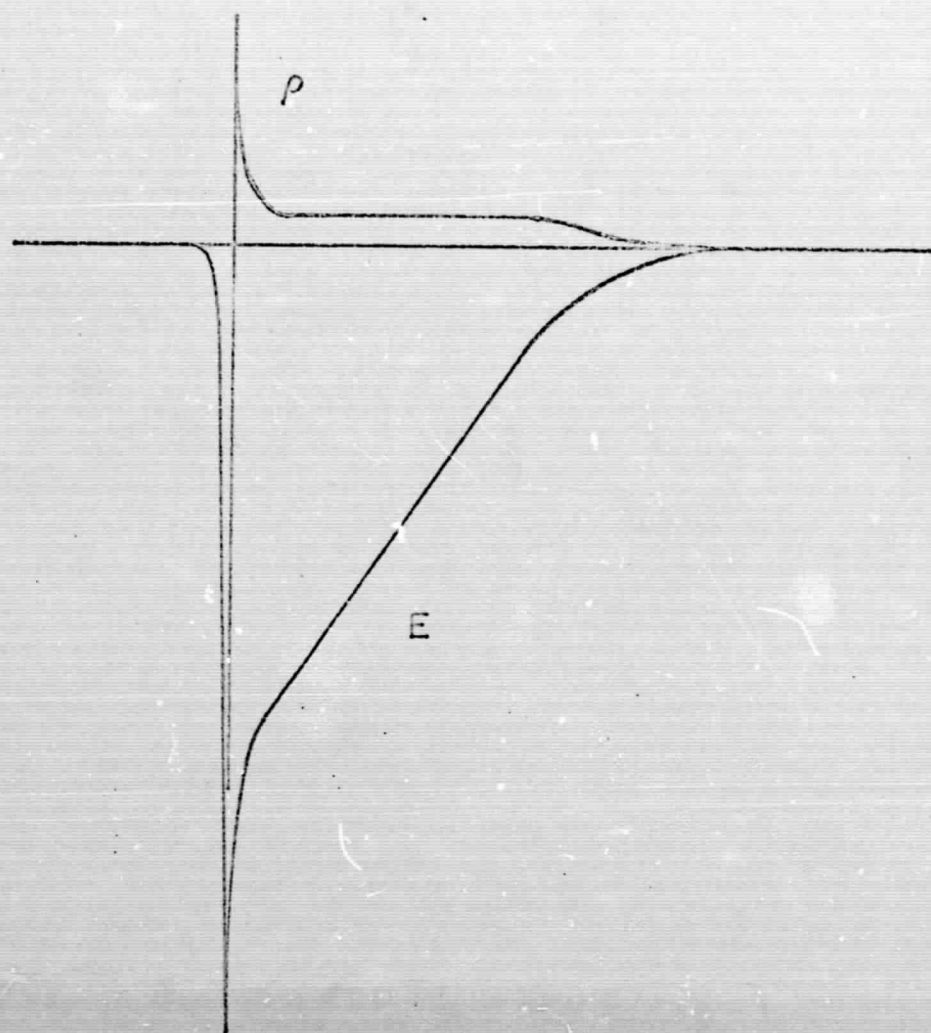


Fig. 1

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.

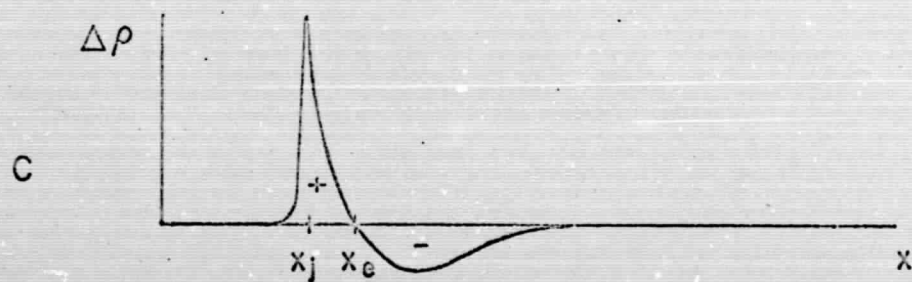
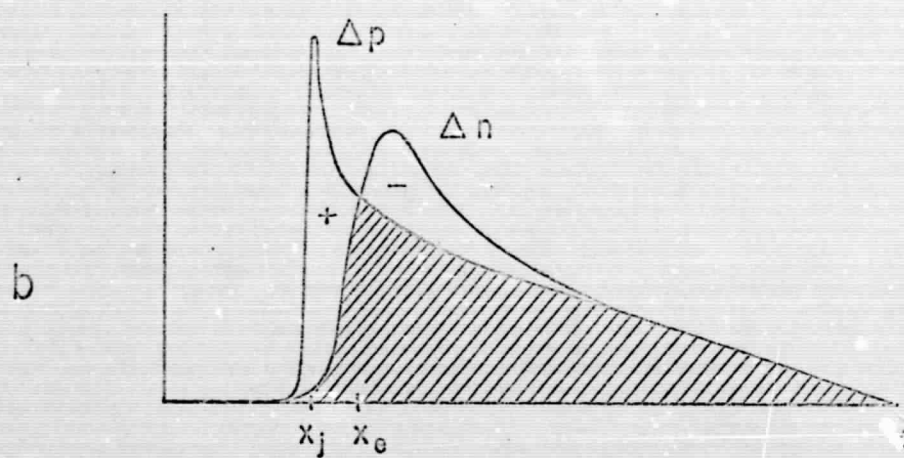
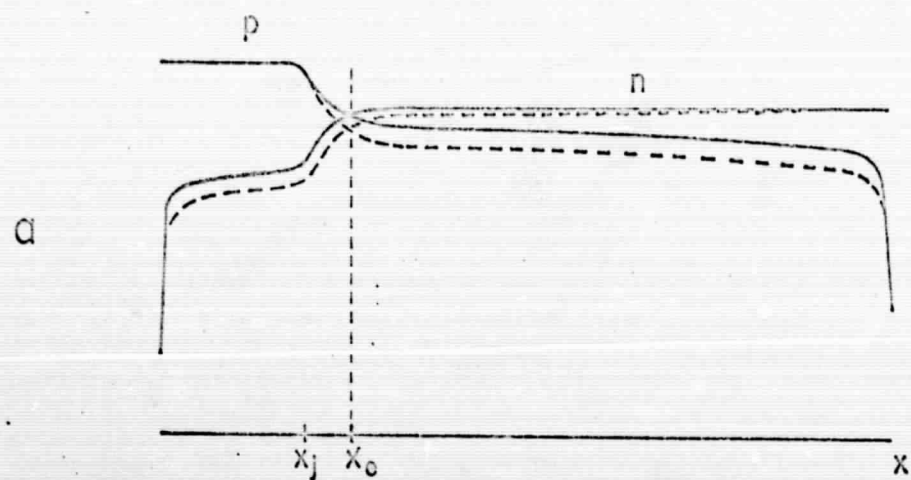
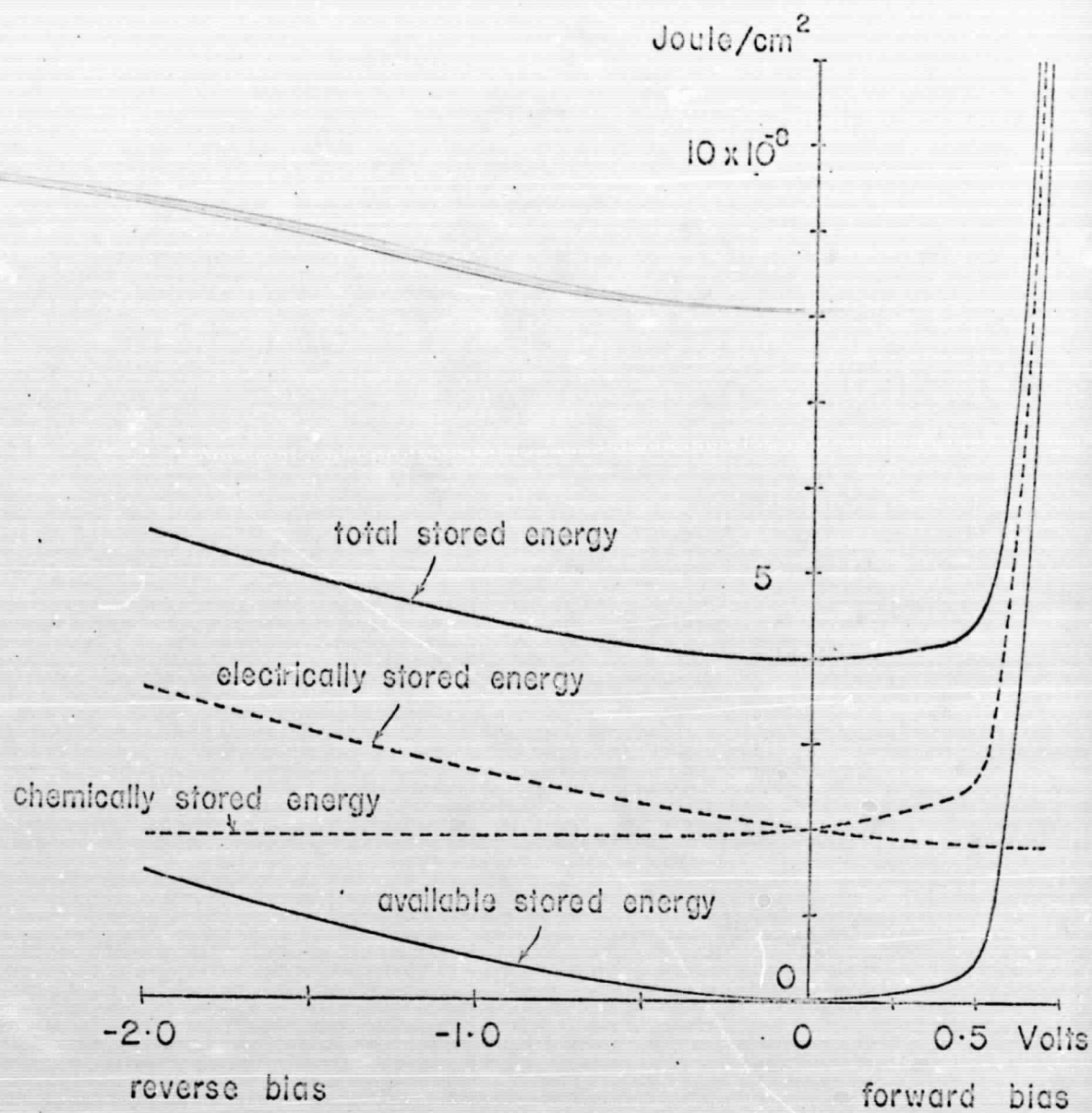


Fig. 2

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.



PRECEDING PAGE BLANK NOT FILMED

Fig. 4

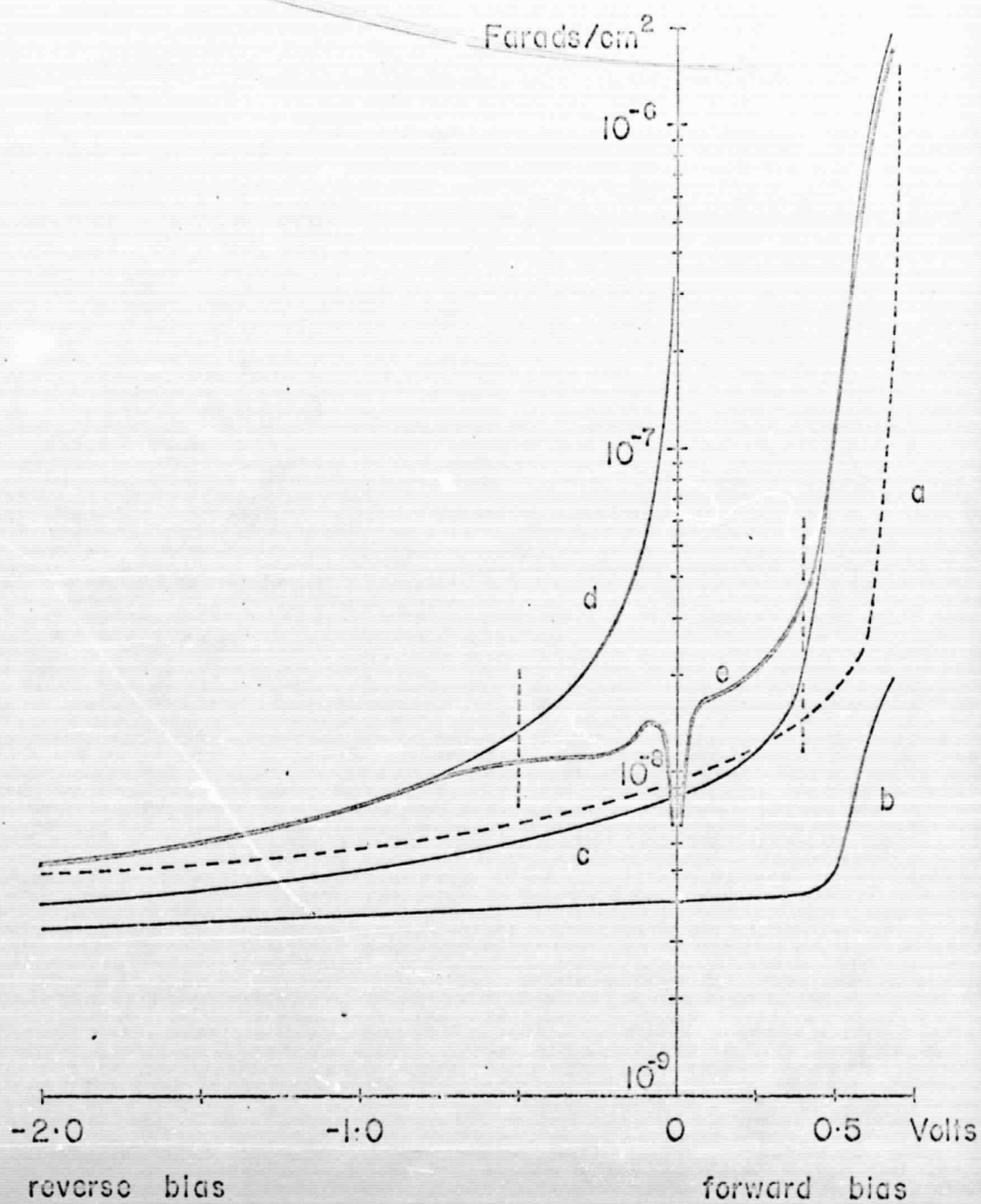


Fig. 5

REPRODUCIBILITY OF THE ORIGINAL PAGE IS POOR.