

# NASA TECH BRIEF

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### Gate Protective Device for SOS Array

**The problem:**

One of the problems in CMOS (complementary-symmetry metal-oxide semiconductor) technology is that SOS (silicon oxide on sapphire) arrays are subject to breakdown voltages caused by electrostatic discharge from a person or a piece of equipment in contact with the external leads of the circuit. Because breakdown voltage  $BV_{ox}$  across thin (1000 angstroms) gate oxides is about 70 volts, it can be easily exceeded by such discharges.

**The solution:**

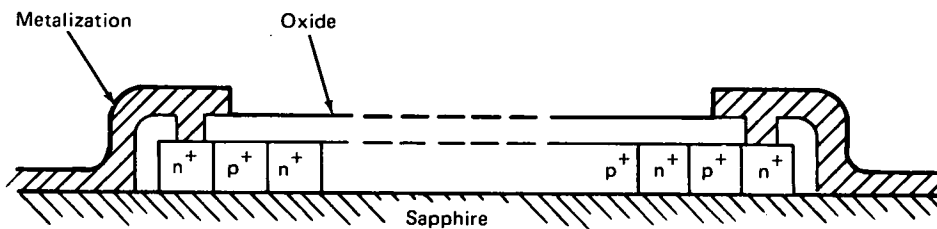
A gate protective device was made which consists of alternate heavily doped  $n^+$  and  $p^+$  diffusions to eliminate the problem.

**How it's done:**

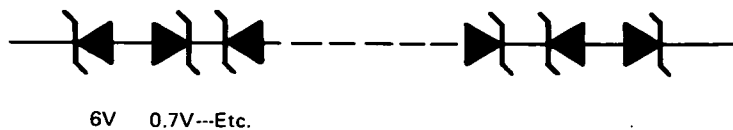
As a function of the human body resistance, the limiting of transient voltage across the gate oxide requires that the dynamic impedance  $R_{dyn}$  of the protective device be

$$R_{dyn} \leq \frac{BV_{ox}}{V_{body}} R_{body}$$

where  $BV_{ox}$  is the breakdown voltage (70 volts) and  $R_{body}$  and  $V_{body}$  are selected at 1000 ohms and 1000 volts of the human body which are the practical worst-case levels. In addition, this protective device must handle a current of approximately 1 ampere.



Cross Section



Schematic Representation

(continued overleaf)

A device satisfying these requirements consists of alternate heavily doped  $n^+$  and  $p^+$  diffusions which are easily produced during the normal double epitaxial processing. Schematically, this device represents a series of reverse-biased zener diodes and alternate forward diodes, as shown in the figure. For a junction doped heavily on both sides ( $10^{19}/\text{cm}^3$ ), the zener breakdown voltage is approximately 6 volts. Thus, for a string of  $2n$  junctions, there are  $n$  6-volt zener diodes and  $n$  forward diode drops of approximately 0.7 volt each in series. The total voltage drop can be easily fixed with the appropriate number of junctions.

Several devices of this geometry were made which consisted of nine alternately diffused strips (eight junctions). Results showed that each device had a 27-volt breakdown in either direction. This breakdown was reproducible across the entire wafer with a tolerance of better than  $\pm 2$  volts.

**Note:**

Requests for further information may be directed to:  
Technology Utilization Officer  
NASA Headquarters  
Code KT  
Washington, D. C. 20546  
Reference: B72-10755

**Patent status:**

Title to this invention has been waived under the provisions of the National Aeronautics and Space Act [42 U.S.C. 2457 (f)], to the RCA Corp., Princeton, N. J. 08540.

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