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METALLIZATION FAILURES

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16. Abstract Metallization-related failure mechanisms are a major cause of integrated circuit failures under accelerated stress and field operation conditions. Industry's approach has been, (1) a better understanding of the aluminum system, now the most widely used material, and (2) evaluation of alternative metal systems.

The newer and more complex multilevel metallization systems require low temperature deposition techniques and critical, etching-through methods due to smaller geometry and closer spacing.

Aluminum metallization offers many advantages, but also has limitations. Alternative materials are being considered for large scale integrated arrays. This survey defines the merits and restrictions of metallization systems in current usage and those under development. Although no specific recommendations are made references can be drawn from the data presented. The advanced state of beam lead technology is apparent.

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SUMMARY

Metallization-related failure mechanisms have been shown to be a major cause of integrated circuit failures under accelerated stress conditions, as well as in actual use under field operation. The integrated circuit industry is aware of the problem and is attempting to solve it in one of two ways: (1) better understanding of the aluminum system, which is the most widely used metallization material for silicon integrated circuits both as a single level and multilevel metallization, or (2) evaluating alternative metal systems.

As integrated circuit structures become more complex, additional processing steps are required to obtain multilevel metallization. Low temperature deposition of dielectrics is essential, and etching through to interconnect the levels of metallization is critical. In addition, smaller geometry and closer spacings are required.

Aluminum metallization offers many advantages, but also has limitations particularly at elevated temperatures and high current densities. As an alternative, multilayer systems of the general form, silicon device-metal-inorganic insulator-metal, are being considered to produce large scale integrated arrays. This survey defines the merits and restrictions of metallization systems in current usage and systems under development. To offer any specific recommendations would be presumptuous without detailed knowledge of the device structure, applications, environmental conditions and manufacturers capability. In cases where aluminum metallization can be used the preference is obvious; since it is a single metal system, well-investigated and lends itself to production techniques. If field conditions and specific applications rule out aluminum, then titanium-platinum-gold or titanium-palladium-gold would be advisable. In either case beam lead technology appears to be well enough advanced technically to warrant specification.

INTRODUCTION

Metallization-related failure mechanisms have been shown to be a major cause of integrated circuit failures under accelerated stress conditions as well as in actual use under field conditions (ref. 1). This survey will concentrate on inherent limitations in material combinations, and methods of detecting these, to provide guide lines for characterization and selection of metallization systems for silicon integrated circuits.

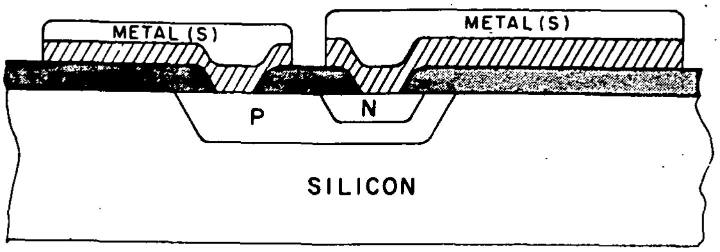
This section presents detailed technical information on processing steps for the fabrication of large-scale integrated circuits, subsequent to diffusion, and the effects of such steps on metallization reliability. The critical steps in integrated circuit fabrication are discussed, and properties of the metallization reliability are examined, particularly in terms of their impact on long term reliability. Desired properties of the metal films are considered relative to the rather extensive body of available information on metallization related failure mechanisms in integrated circuits, both of conventional complexity and LSI arrays.

Metallization characterization tests are determined by: (1) properties of metal thin films, (2) metallization requirements, (3) integrated circuit processing, and (4) long term stress.

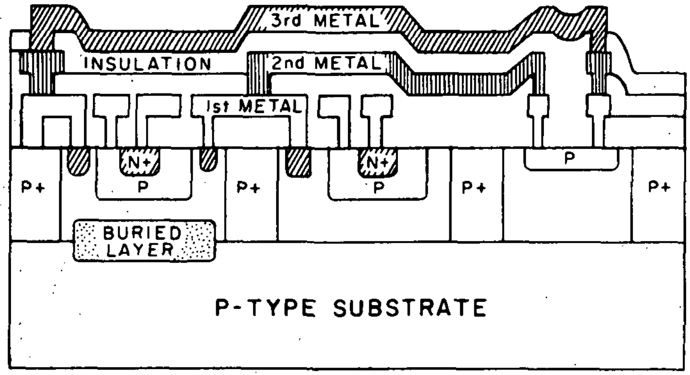
Both single and multilayer metallization systems will be discussed as such, and as to their applicability to multilevel integrated circuit fabrication. Figure 1 shows a schematic of single metal, multilayer, and multilevel metallization.

A definition of terms used in figure 1 is as follows:

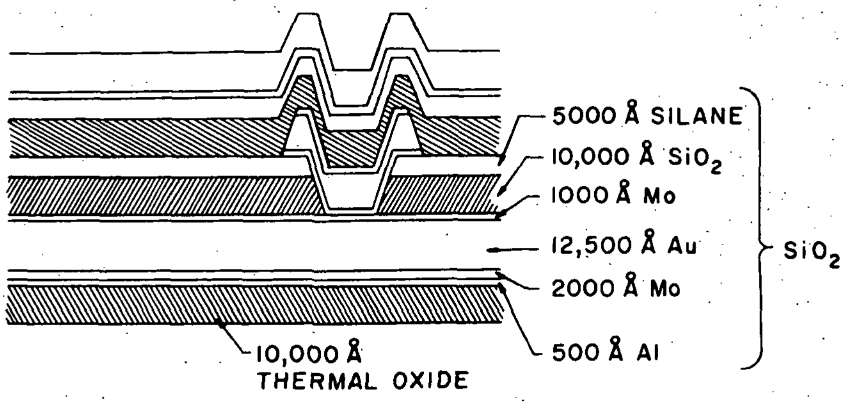
1. Silicon device-- a semiconductor made of silicon, and including metal contact, may be a bipolar transistor, a field effect transistor, a metal-silicon diode or an integrated circuit.
2. Metallization system-- the interconnecting metal pattern on a silicon device; the metal may be a single material (e.g. Al) or a composite sandwich structure, (e.g. Ti-Pt-Au). See figure 1 top.
3. Multilayer or multilevel metallization system-- two or more metal layers separated by dielectric layers and connected in such a manner as to optimize silicon device performance. Commonly used in large scale integration (LSI- see figure 1 middle and bottom)



METALLIZATION SYSTEM
ON SILICON DEVICE



MULTILAYER METALLIZATION SYSTEM



Mo-Au-Mo-SiO_2 MULTILEVEL SYSTEM

Figure 1.- Schematic of Single Metal, Multilayer, and Multilevel Metallization

METALLIZATION FAILURES

Before discussing specific metallization requirements and comparing various metal systems presently in use, we should be cognizant of the potential causes of metallization failures. It has been found that in some cases trends in integrated circuit design and processing technology may in fact increase the relative susceptibility of monolithic circuits to failure due to metallization-related mechanisms.

Metallization related failures observed to date are occasionally due to shorting, for example, reaction of metal with the substrate, under-etching or metal-metal shorts between layers in multilevel metallized arrays. However, the largest number of metallization related failures are due to *opens*. Table 1 enumerates the various causes of *opens* or localized reduced cross-sectional area in metallization. Quite often more than one cause or mechanism contributes to a given failure. For example, shadowing at steps can cause the localized cross-sectional area to be reduced, which in effect can produce excessively high current density and *opens* by electromigration. Figure 2 is a Scanning Electron Microscope micrograph of the shadowing effect.

TABLE 1.- REASONS FOR OPENS OR LOCALIZED REDUCED CROSS-SECTIONAL AREA IN MULTILEVEL METALLIZATION

1. Electromigration	13. Photolithographic defects
2. Localized melting of metal due to excessive joule heating	14. Over etching of contact areas enhanced by electrolytic action
3. Metallization scratches	15. Inadequately opened contact windows
4. Notches in the metal edge at steps	16. Residual oxide at metal-metal contact interface
5. Microcracks at steps	17. Inadequate contact alloying
6. Filamentation of metallization at steps	18. Overalloying (excess Al-Si interface penetration in the case of aluminum metallization)
7. Tunnels under metallization at steps	19. Al-Si eutectic formation (applying to aluminum metallization)
8. Shadowing at steps	20. Kirkendall effect
9. Fatigue effects	21. Corrosion effects
10. Stress cracking	
11. Loss of adhesion	
12. Over etching of metallization due to poor photoresist adhesion at a step	

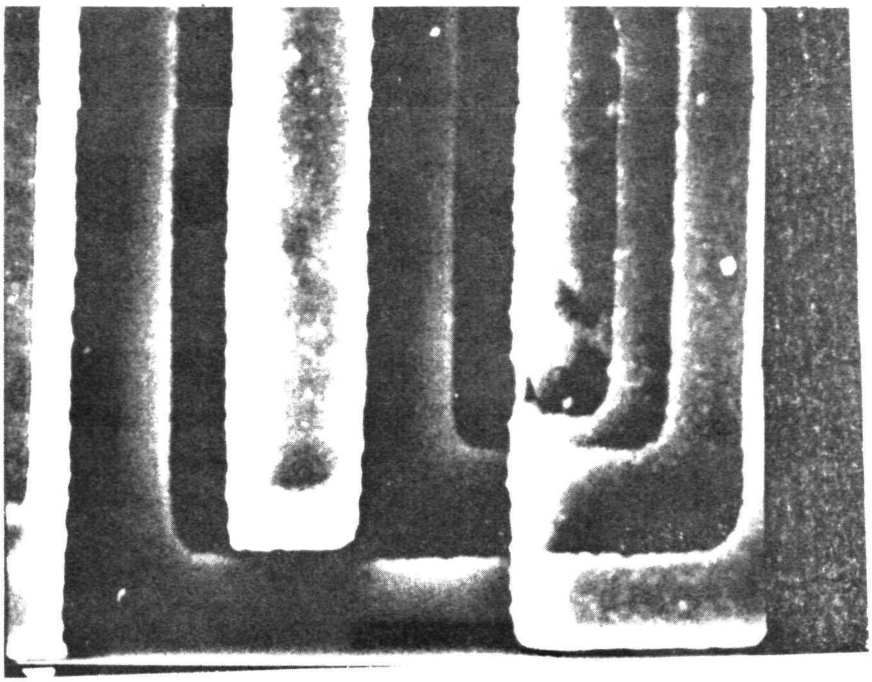


Figure 2.- Scanning Electron Microscope Micrograph of Shadowing Effect

Another significant classification of events that leads to metallization failure are those events which uniformly affect the thickness of metallization at all places on a chip or a wafer or a wafer lot. For example, poor process control may result in thin metallization because of an inadequate charge during metal evaporation or because of gross shadowing due to fixtures and supporting hardware in the evaporation chamber. Also, inadequate thickness can be the result of improper specification. It is judged that this category of failure mechanism is unnecessarily high. When present, it contributes significantly to failure by aggravating other mechanisms listed in Table 1. Once this category of failure mechanisms is identified, remedial action is normally simple.

In considering long-term reliability of metallizations, temperature and temperature gradient, ambient, current density and other factors must be taken into account in assessing the relative reliability hazards of various systems. Unfortunately much of the available data is obtained under high stress conditions and there are major difficulties in extrapolating the results of such conditions to factors occurring at lower stress levels. Sometimes the temperature dependence of failure rate at high stress levels is determined entirely by a mechanism with a high activation energy, whereas a totally different mechanism with a lower activation energy is the dominant factor at lower stress levels.

In considering maximum current densities for cross-sectional areas, important factors which should be taken into account are film thickness, line width, current crowding at corners, and various factors which influence the cross-sectional area of metal films in localized regions, including scratches, notches, microcracks and tunnels at steps produced during metal etch-back.

Other reliability factors unique to each metallization system include ability to form ohmic contacts to silicon, susceptibility to peeling and corrosion, temperature cycling effects, and bondability.

Many failures are a result of specific process conditions, rather than the inherent limitations of the materials involved. For example, in the case of Mo-Au layered structures, excellent high temperature reliability (300°C) and relatively low susceptibility to electromigration have been observed on some samples. Other samples have had problems with peeling, Au-Si interaction, undercutting and other effects.

Metal-dielectric interaction can be an important factor in the reliability of integrated circuits. The most commonly used dielectric is thermally grown SiO_2, but it must be realized that the extent of the interaction is determined by the exact nature of the oxide, prior processes it has been subjected to, and the presence of a borosilicate or phosphosilicate surface layer arising from the diffusion processes. Also, various deposited dielectrics including silicon nitride, aluminum oxide, and phosphosilicate glass are appearing in large-scale arrays.

In multilevel structures, procedures have been developed for insuring that the angle at the edge of a photolithographically defined cut in the oxide is not excessively steep. One technique described in the literature (ref. 2) uses a combination of r-f sputtered SiO_2 and chemically-vapor-plated SiO_2. The faster etching SiO_2 on top results in a less steep angle into the contact cut than would be obtained with a homogeneous SiO_2 film. Another procedure uses a single deposited dielectric layer in which the composition of the film is changed as deposition of the film progresses. The net result is a film in which the initially deposited layers have a lower etch rate than subsequently deposited portions of the layers. An example of a system which can be applied for this type of structure is vapor-plated phosphosilicate (the etch rate of phosphosilicate containing 3 to 4 percent by weight phosphorus in buffered hydrofluoric (HF) is approximately twice that of chemically-vapor-plated SiO_2 containing no phosphorus). Generally the metallization on such devices is aluminum. Among available developmental multilevel arrays, aluminum has most frequently been used for both first and second-level metallization. The molybdenum-gold system, modified to moly-gold-moly in each layer, has been used for multilevel metallized applications.

Some of the most significant failure mechanisms are discussed in the following sections.

Electromigration

Electromigration (ref. 3) becomes an important failure mode commonly found in high power devices and integrated circuits where aluminum conductors carry current densities in excess of 10^5 amperes/cm^2 at temperatures above 100°C. The mode of failure is an open circuit caused by the movement of aluminum ions in the direction of the electron flow. This failure mode is enhanced when a thermal gradient, a current gradient or a compositional gradient exists in the conductor.

The crystallite size in aluminum conductor films is regarded as important (ref. 4). Experimental failure data obtained for small crystalline aluminum films (1.2 micron lateral size)is shown in Table 2 . Mean-time-to-failure as a function of current density and film temperature is plotted and presented in figure 3. Corresponding experiments on what is considered to be large crystalline, well-ordered aluminum film conductors were run. The large crystallites (8 microns lateral geometry) were obtained by monitoring the substrate temperature at 400°C during deposition. The data from this experiment is presented in Table 3 and plotted in figure 4. The increase in activation energy from 0.48 to 0.84 eV for this failure mode for large crystallite well-ordered films over the activation energy of fine-grained aluminum films is attributed to the reduction of grain boundaries.

A further increase in activation energy for mass transport should be obtained by the elimination of surface diffusion by an overcoat of silica glass (7000 Å). Experimental data for the failed films and the predicted lifetime are presented in Tables 4 and 5 and plotted in figure 5. The activation energy of 1.2 eV for these thick, wide, well-ordered and glass films approaches the predicted maximum activation energy of 1.4 eV which is the activation energy for self-diffusion of aluminum in bulk aluminum.

Aluminum film lifetime is also a function of the stripe cross-sectional area, since for a given rate of transport or void growth, the greater the film cross-sectional area, the longer it should take to cause a void to grow across the conductor resulting in an open circuit. Experimental data for variable line-width aluminum conductors is shown in Table 6. Putting MTF data together for large-grained aluminum films of variable line width results in a plot shown in figure 6. From this it appears that mean-time-to-failure varies in a linear manner with line width of aluminum conductor stripes.

To evaluate the effect of conductor width under stress tests, well-ordered films of 0.15 mil line width and thickness varying from 200-12,000 Å were tested and the data is shown in Table 7.

TABLE 2.- TEST DATA FOR SMALL CRYSTALLITE ALUMINUM FILMS

Film No.	Thickness (Å)	$J \times 10^{-6}$ (A/cm^2)	T (^oC)	$\frac{10^3}{T^oK}$	MTF (Hours)	$\frac{10^{14}}{MTF\ J^2}$
AD	7400	0.5	177	2.22	480	0.83
BD	7060	1.21	186	2.18	47	1.45
CD	7000	1.5	195	2.135	19.5	2.28
DD	6800	2.82	238	1.96	3.5	3.70
AB	7400	0.5	192	2.15	250	1.60
BB	7060	1.22	200	2.11	38	1.80
CB	7000	1.5	212	2.06	8	5.55
DB	6800	2.88	260	1.87	1.5	8.03
BA	7060	0.987	109	2.62	850	0.121
CA	7000	1.46	121	2.54	268	0.175
DA	6800	2.05	134	2.48	183	0.130

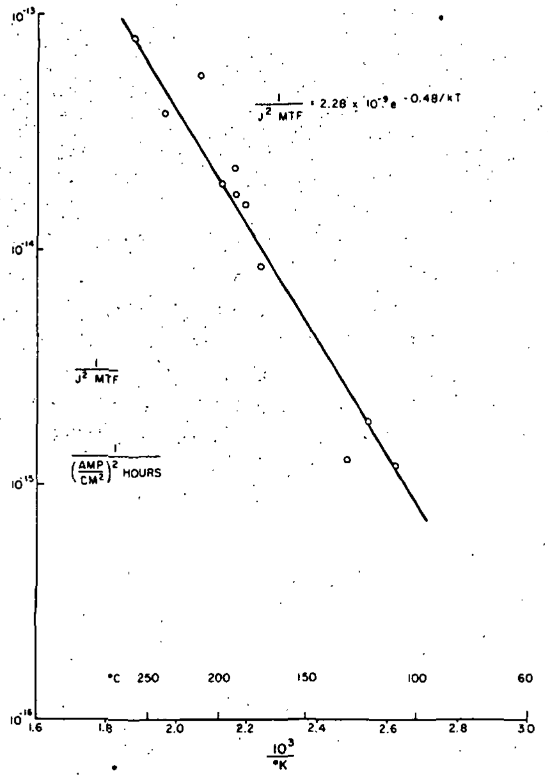


Figure 3.- Mean-Time-To-Failure as a Function of Current Density and Film Temperature: Aluminum Films Evaporated from Tungsten onto Cold Substrate

TABLE 3.- TEST DATA FOR LARGE CRYSTAL ALUMINUM FILMS

Film No.	Thickness (Å)	Width (mils)	$J \times 10^{-6}$ (A/cm^2)	MTF (Hours)	$\frac{10^{15}}{J^2\ MTF}$	T (°C)	$\frac{10^3}{T^oK}$
AB	6036	0.582	0.6	510	5.45	193	2.145
BD	6036	0.644	1.27	270	2.30	183	2.18
CD	6036	0.644	1.106	254	3.22	185	2.18
DD	6036	0.638	1.95	20.3	12.9	220	2.03
BB	6036	0.644	1.15	180	4.21	205	2.09
CD	6036	0.644	1.37	63	8.45	206	2.085
DB	6036	0.638	1.97	12	21.6	230	1.99
AD	6036	0.582	0.548	1125	2.96	177	2.22
DA	6036	0.638	2.02	53	4.63	184	2.19
CA	6036	0.644	1.31	840	0.695	155	2.34

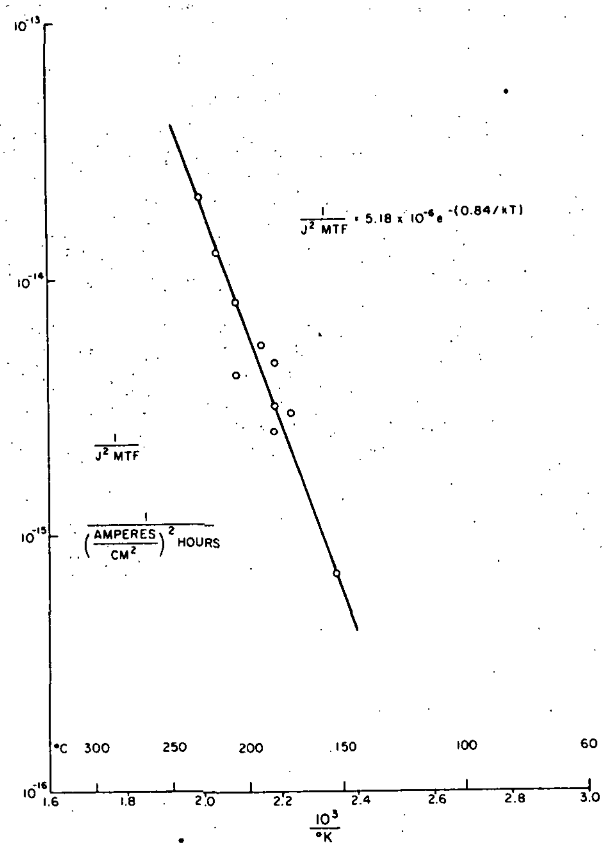


Figure 4.- Mean-Time-To-Failure as a Function of Current Density and Film Temperature: Aluminum Films Evaporated from Tungsten Filaments Condensed onto Hot (400°C) Substrates

TABLE 4.- GLASSED LARGE CRYSTAL ALUMINUM PERFORMANCE

Film Thickness (Å)	Film Width (mils)	J x 10^{-6} A/cm^2	MTF Hours	$\frac{10^{15}}{J^2 \text{ MTF}}$	Film Temp.	$\frac{10^3}{K}$
12,200	1.46	0.908	1700	0.713	212	2.06
12,200	1.46	0.860	1060	1.28	221	2.02
12,200	1.43	0.870	395	3.33	246	1.93

TABLE 5.- GLASSED LARGE CRYSTAL ALUMINUM PREDICTED PERFORMANCE

Film Thickness (Å)	Film Width (mils)	Jx10^{-6} (A/cm^{2}p)	Estimated MTF Hours	$\frac{10^{15}}{J^2\text{MTF}}$	Film Temp. ^{o}C	$\frac{10^3}{^oK}$	Sample Size	No. of Failures	Hours on Test
12,200	1.46	0.777	5,400	0.306	203	2.10	15	7	3900
12,200	1.46	0.702	12,000	0.170	189	1.16	13	2	2590
12,200	1.46	0.460	16,000	0.295	200	2.11	13	1	2333

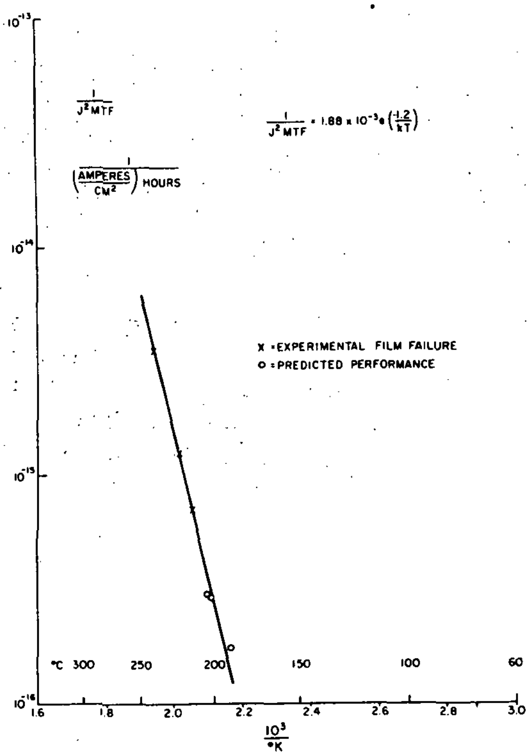


Figure 5.- Mean-Time-To-Failure as a Function of Current Density and Film Temperature: 1.46 Mil Wide by 12,200 A Thick, Well Ordered Aluminum Coated with 6000 A Thick Glass Film

TABLE 6.- TEST DATA FOR LARGE CRYSTAL ALUMINUM FILM CONDUCTORS OF VARIABLE LINE WIDTHS

Film Thickness (Å)	Film Width	Film Cross-sectional Area ($cm^2 \times 10^8$)	$Jx10^{-6}$ (A/cm^2)	T (^{o}C)	$\frac{10^3}{T(^{o}K)}$	Experimental MTF (hours)	Calculated MTF (hours)
7540	0.45	8.62	1.85	176	2.275	230	211
7540	0.94	18.0	1.42	170	2.26	650	660
7540	1.40	26.8	1.48	190	2.16	320	341
7540	1.87	35.9	1.51	230	1.98	76	76
7265	0.46	8.42	1.48	205	2.09	96	76
7265	0.93	17.1	1.42	219	2.035	47	69
7265	1.42	26.2	1.39	231	1.985	49	68
7125	0.54	9.75	1.51	196	2.135	130	93
7125	1.00	18.1	1.57	210	2.07	127	84
7125	1.47	26.6	0.93	198	2.12	670	575
7125	1.98	36.8	1.00	210	2.07	450	420

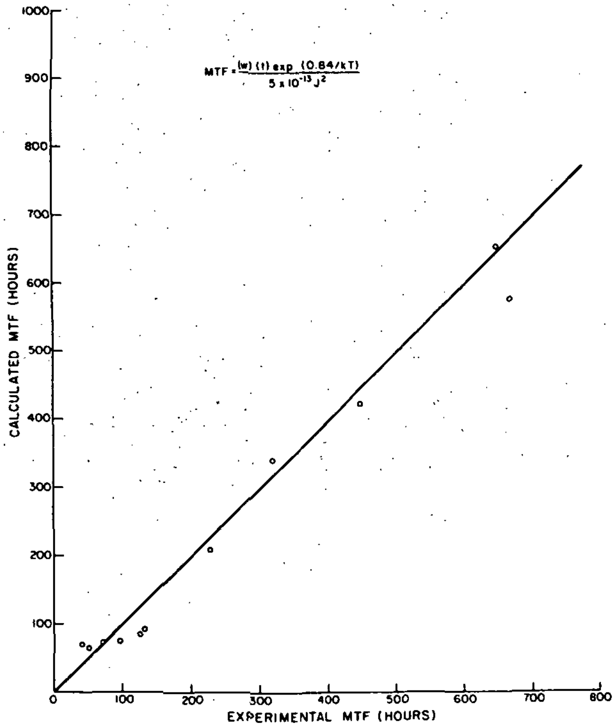


Figure 6.- Experimentally Determined vs Calculated Mean-Time-to-Failure for Large-Grained Aluminum Films of Variable Line Width

TABLE 7.- TEST DATA FOR LARGE CRYSTAL ALUMINUM FILM CONDUCTORS OF VARIABLE THICKNESS

Film Thickness (Å)	Film Width	Film Cross-sectional area ($cm^2 \times 10^8$)	$J \times 10^{-6}$ (A/cm^2)	T (^oC)	$\frac{10^3}{T(^oK)}$	Experimental MTF	Calculated MTF	Volume Resistivity ohm-cm $\times 10^6$
2017	.63	3.22	2.010	204	2.100	24	21	6.02
2068	.66	3.46	1.780	204	2.10	35	16	7.05
2440	.57	3.53	2.07	200	2.115	36	14	4.82
3320	.52	4.38	1.560	192	2.15	33	45	3.53
3840	.58	5.66	2.175	206	2.09	11	17	3.42
8838	.51	11.42	1.477	202	2.10	80	80	3.05
9455	.43	10.32	1.457	200	2.115	62	86	3.06
10500	.39	10.40	1.460	200	2.115	100	87	3.04
12540	.42	13.38	1.655	222	2.02	38	35	3.11

As in previously mentioned experiments, the MTF data was plotted against mathematically calculated MTF and shown in figure 7. One can conclude from the last two figures (figures 6 and 7), that film lifetime is definitely a function of film cross-sectional area for both temperature and stress conditions.

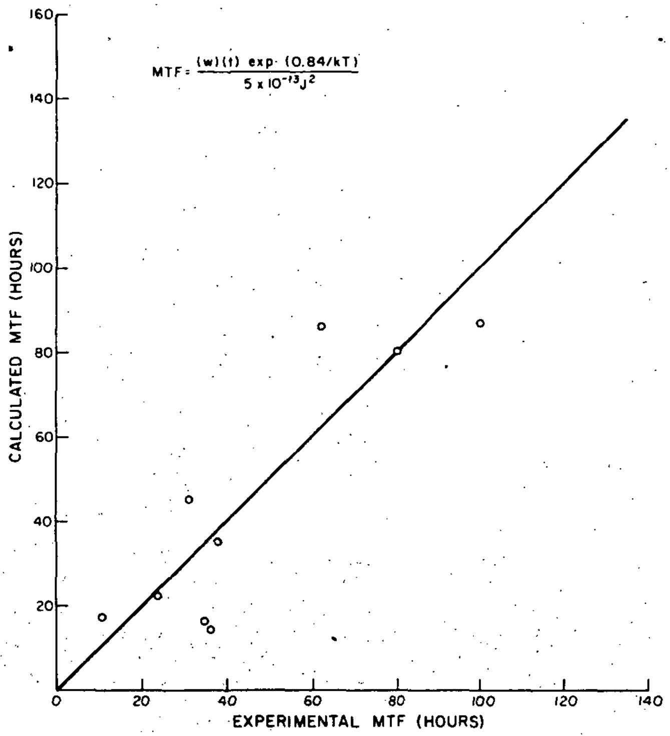


Figure 7.- Experimentally Determined vs Calculated Mean-Time-To-Failure for Large Grained Aluminum Film Conductors of Variable Thickness

In figure 8, experimentally determined film volume resistivities were plotted as a function of film thickness. It can be seen that for film thicknesses under 5000 Å the volume resistivity increases rapidly. A MTF comparison of small crystallites, large crystallite and glass, large crystallite aluminum films as a function of current density, temperature and cross-sectional area is represented in figure 9. The points were derived mathematically and show by the intersection at 255°C that lattice diffusion effects are predominant. Under 275°C orders of magnitude improvements in lifetime are realized by using well-ordered, large-grain, glassed films.

A design guide is given in figures 10, 11, and 12 where the product of the aluminum line thickness and width are 10^{-7} cm^2 which is a typical line width of 0.5 mil and 7900 Å thickness. Since lifetime is directly proportional to film cross-sectional area, the life of films possessing other dimensions can be determined from the plots.

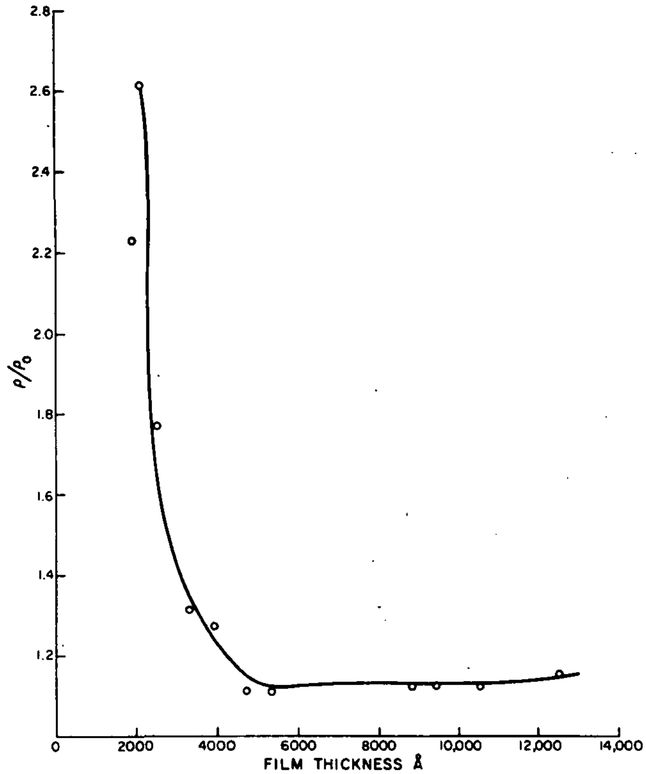


Figure 8.- Aluminum Film Resistivity Normalized to Bulk Resistivity as a Function of Film Thickness

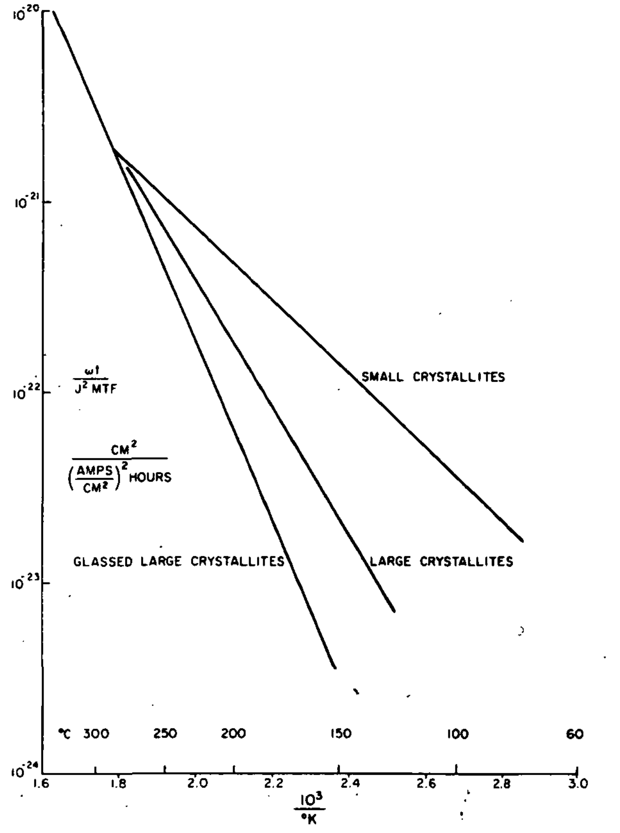


Figure 9.- Mean-Time-To-Failure for Aluminum Film Conductors as a Function of Current Density, Temperature and Cross-sectional Dimensions

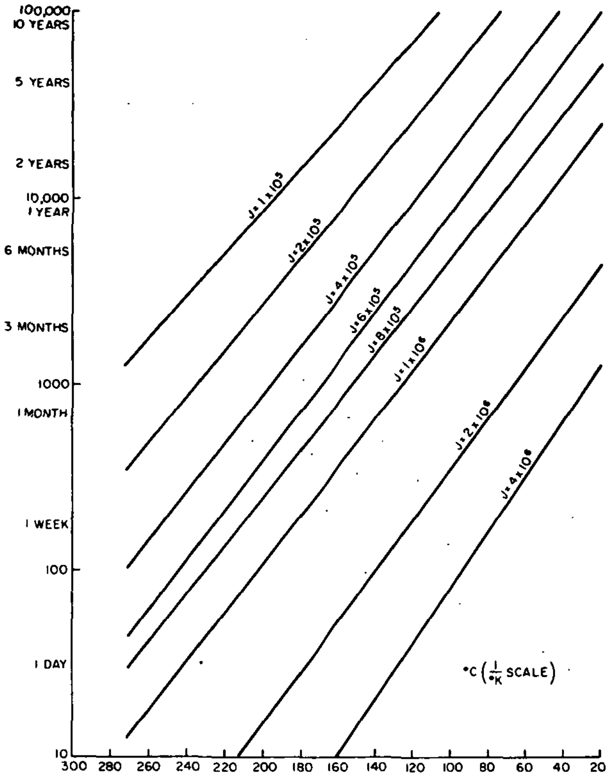


Figure 10.- Small Crystallite Aluminum Film Lifetime of Conductors with 10^{-7} cm^2 Cross-sectional Area

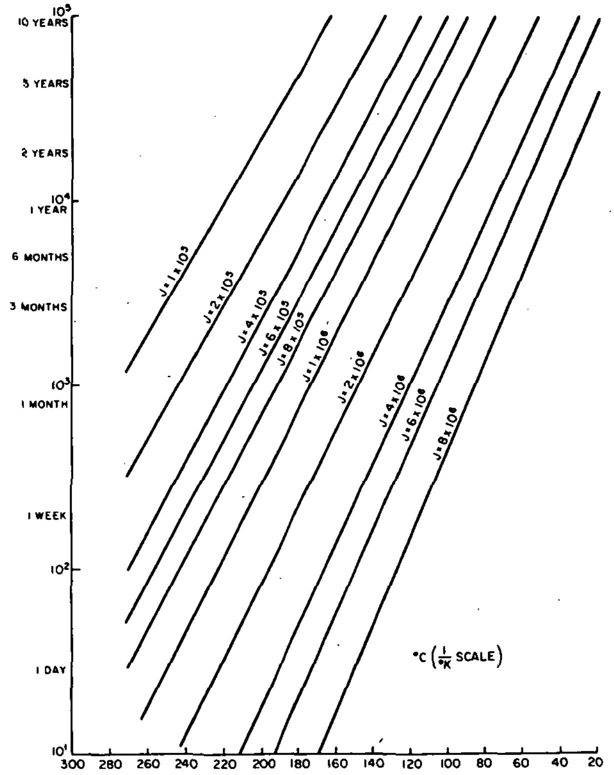


Figure 11.- Large Crystallite Aluminum Film Lifetime of Conductors with 10^{-7} cm^2 Cross-sectional Area

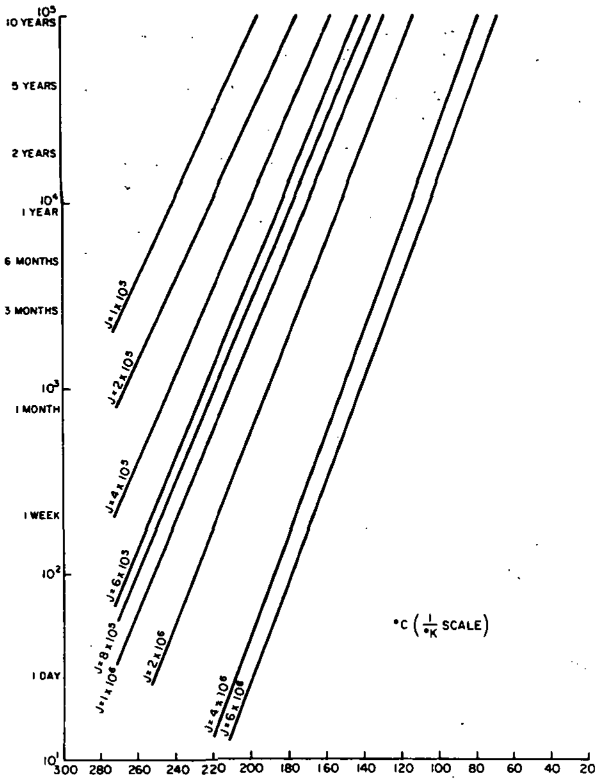


Figure 12.- Glassed Large Crystallite Aluminum Film Lifetime for Conductors with a Cross-section of 10^{-7} cm^2

Etch Pits

A failure mode common in aluminum silicon contacts is the growth of etch pits into the silicon at the positive terminals (ref. 5) under high current density and temperature stress. The pit formation may not be obvious prior to removal of the aluminum. The formation is believed to be due to the dissolution of silicon into aluminum to saturation and the transport of the dissolved silicon by momentum exchange, enabling further dissolution of aluminum. At 235°C about 0.003 weight percent of silicon can exist in solid solution with aluminum. Because silicon will preferentially enter aluminum at crystalline dislocations, rather than uniformly over the interface, the process results in the formation of etch pits. The process can continue until the junction beneath the aluminum-silicon contact is electrically shorted.

Aluminum-Silicon Reaction

Another failure mode is the reaction between aluminum and silicon dioxide. The reaction is initially important in device fabrication to effect good ohmic contact; but this reaction may play in the degradation of the reliability of devices under stress and at elevated temperatures. Figure 13 presents a plot of the depth of penetration of aluminum into the glass as a function of time. From the slopes of these experimental lines the rates of penetration of aluminum into glass was determined in angstroms/ minute and are listed in Table 8. An Arrhenius plot of this data is given in figure 14. Figure 15 presents an extrapolation of the data to lower temperatures. It is obvious that this mode of failure is only significant when operating temperatures exceed 200°C.

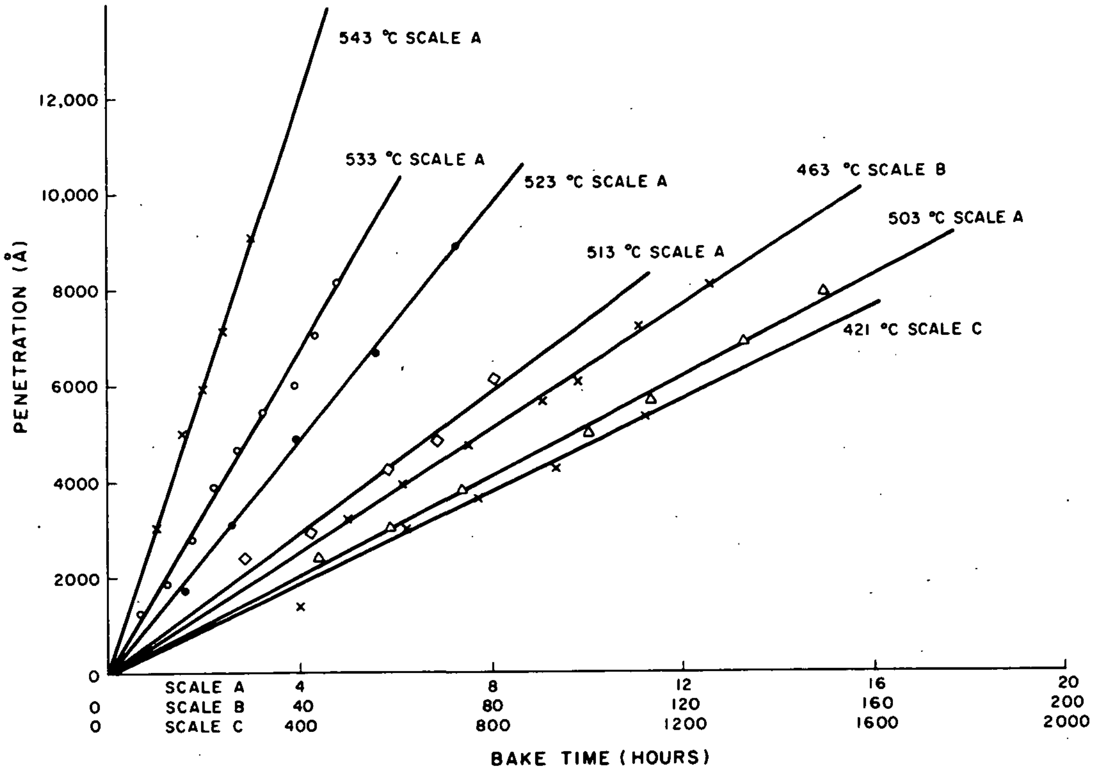


Figure 13.- Penetration of Aluminum into Thermally Grown SiO_2 as a Function of Time and Temperature

TABLE 8.- RATE OF ALUMINUM PENETRATION INTO SiO_2

Temperature (°C)	$\frac{1}{°K}$	Rate (Å/min)
543	1.225	49.0
533	1.241	27.8
523	1.256	19.7
513	1.272	11.8
503	1.289	8.33
463	1.359	1.02
421	1.441	0.076

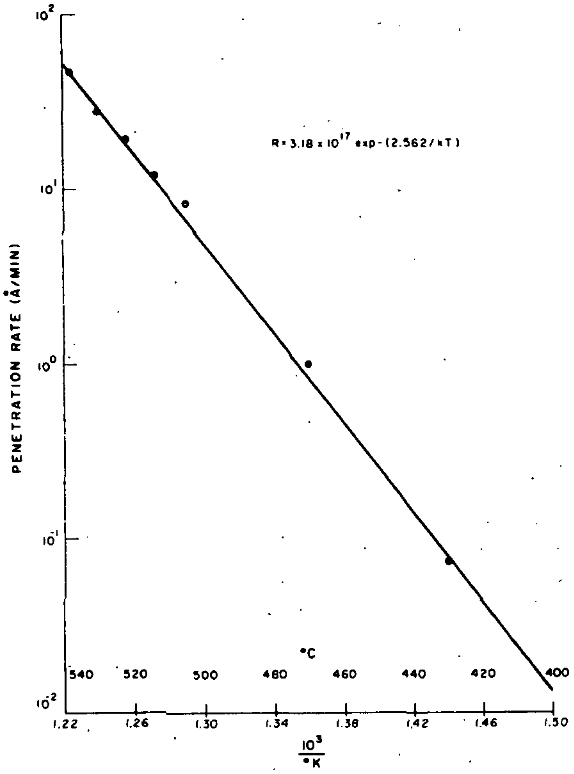


Figure 14.- Penetration Rate of Aluminum Reaction into Thermally Grown SiO_2 as a Function of Temperature

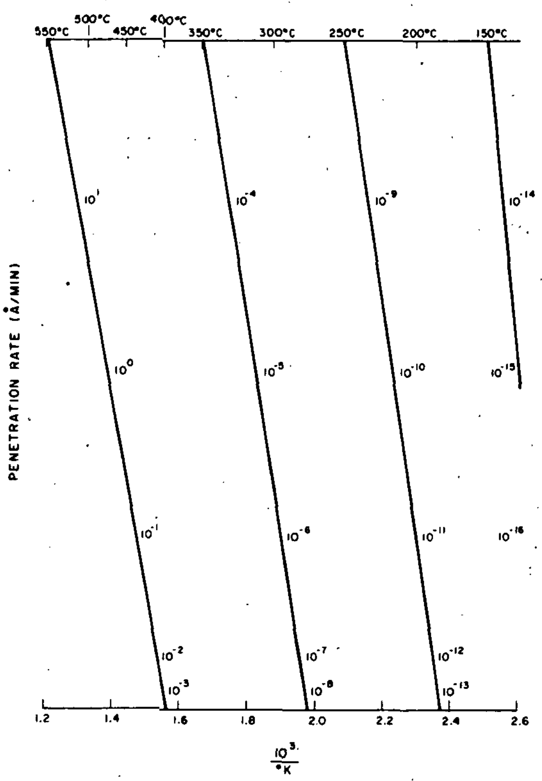


Figure 15.- Penetration of Aluminum into SiO_2 Extrapolated to Lower Temperature

Still another problem is the dissolution of silicon into aluminum. Due to the solid solubility of silicon into aluminum, the latter can act as an etchant for silicon at relatively low temperatures. The etching of silicon by aluminum is not uniform and preferentially attacks crystalline defects to form etch pits. These etch pits can transverse through shallow p-n junctions causing failure by electrical short. According to the metallurgical phase diagram by Hansen (ref. 6) the area of most interest is the range between 300^{o} to 577^{o}C. For a limited supply of aluminum the solubility is shown to fall off from the maximum at 577^{o}C to near zero at below 300^{o}C. Under operational conditions the current density plays a large role in determining actual temperature at any cross-sectional area of the aluminum conductors.

Electromigration has also been observed in a number of other metals, including gold, copper, platinum, tungsten, silver and tin. The current density at which electromigration occurs in gold metallization films is somewhat higher than that of aluminum films (ref. 7). The selection of a metallization system for integrated circuits may involve a number of tradeoffs between cost, performance and reliability. For example, it is possible to insure that the aluminum metallization will not be susceptible to electromigration effects by using design rules which keep the current density in any stripes below 10^5A/cm^2. If this design rule necessitates the use of wider metal stripes, the wider emitter-base and collector-base junctions, (as for example in interdigitated transistor structures) the resulting structure may be lower in performance than would be possible if a higher current density could be used. This is particularly true if the possibility of reductions in cross-sectional areas which might arise as a result of scratches is taken into account. The current and temperature required to produce appreciable metal transport is related to the relative ease of self-diffusion in a metal.

Metal-Metal Interaction

Compound formation and solid solution reactions resulting from intermetallic diffusion are believed to be the mechanisms for some of the failures observed at the ohmic contact interfaces which include metal-semiconductor contacts, expanded metallizations, and bonds to the metallization in semiconductor devices (refs. 8 and 9). Formation of intermetallic compounds can lead to reliability limitations because compounds may have lower electrical or thermal conductivity, different thermal expansion coefficients or brittleness relative to the constituent elements. The net result of intermetallic compound formation is a significant increase in contact resistance and, ultimately open contacts (ref. 9).

Even in systems which do not form compounds, diffusion of one metal into another can result in contact resistance increasing by orders of magnitude. This failure mode is more serious than generally realized and this type of deterioration is usually not recognized during the early stages of device design and manufacture. Diffusion can occur through any of several processes, including vacancy, interstitial dislocation, and grain boundary mechanisms. The predominant diffusion mechanism depends on the type, temperature, structure and geometry of the metallurgical system.

Diffusions have been observed to occur in Ag-Pb, Au-Cr, Au-Ti, Cr-Ni, Cu (NiCr), Cu (Pb-Sn), Ti-Al-Si and Ti-(PtSi). Compounds have been observed to form in Al-Ni, Al-Ta, Au-Ti, Au-(NiCr), Au-(Sb-Sn), and Ti-Al-Si (ref. 8).

Metal-Oxide Interaction

Metals are known to interact with oxides as a result of solid-state reactions at elevated temperatures, and this type of interaction has been shown to occur with aluminum on SiO_2 and on phosphosilicate glasses. Adverse effects can result from this interaction on any type of circuit, but circuits with thin oxide regions are particularly susceptible. For example, the oxide over gate regions of MOS transistors is typically 0.1 to 0.15 microns thick. Accordingly, an important attribute of a metallization system for MOS integrated circuits is the ability to adhere well to oxide but not to react extensively with the thin SiO_2 layer under the gate metal region. There is also a similar requirement for capacitors in bipolar circuits, where such capacitors frequently have 0.1 micron thick oxide, prepared either by anodization or by thermal oxidation. Electrical shorts in MOS structures have been attributed to a solid-state reaction between the electrode metal and SiO_2. The details of oxide preparation can also be a major factor in determining the incidence of such electrical shorts at temperatures of 500°C.

Dielectrics other than SiO_2 are also used at times in integrated circuits. In particular, silicon nitride has been used in a number of types of integrated circuits, and aluminum oxide has been used in MOS circuits. Aluminum adheres well to both of these dielectrics, and has less tendency to react with silicon nitride at elevated temperatures than with SiO_2.

Thermal Stresses

Any metallization system used for integrated circuits must form continuous conducting lines which go up and down steps resulting from topography in the integrated circuits. In bipolar circuits, steps arise at contact cuts to the emitter regions, collector regions, and base regions, as well as between different levels of oxide thickness. In MOS circuits, steps arise at contact cuts and also from field oxide down to gate oxide thicknesses. Such steps frequently are on the order of 1.5 microns high. In multilevel metallized arrays the steps occur at "vias." It is important that processes be used which insure good coverage of the edges of such steps so as not to result in a constriction in the cross-sectional area of the conductor. It must further be realized that stresses existing in a metal as deposited, or stresses resulting from temperature cycling or materials having a different thermal coefficient of expansion, result in subjecting the metal at the step to a particularly severe stress. If that stress exceeds the elastic limits of the thin-film metallization, plastic deformation may result. Each temperature cycle may result in additional plastic deformation and, ultimately, opening of the metal at the step. This type of problem is not effectively screened by a single temperature cycle or even by several cycles, but requires a substantial number of cycles. Aluminum, gold, silver and copper all have thermal coefficients of expansion substantially higher than that of silicon.

Peeling in Layered Systems

Peeling effects, for example, resulting from poor adhesion of gold to molybdenum in devices with Mo-Au metallization, have been a reliability problem. Other binary layer and more complex systems would also be susceptible to possible failure mechanisms as a result of peeling. A single-metal system has no such problems (ref. 10).

Diffusion Effects in Barrier Layer Systems

It is possible to show, by calculation from published diffusion coefficients, and also by experiments under laboratory conditions, that a given metallurgical system consisting of two metal layers which would react, but which are separated by a given type and thickness of barrier layer, will have extremely long life at 300°C or at 400°C. This provides information about the inherent metallurgical stability of the system under accelerated stress conditions. It is, however, very difficult to consistently obtain pin-hole free metallization layers in production, particularly over integrated circuit wafers with considerable topography. Thus systems for which the feasibility of high reliability can be demonstrated are not necessarily reliable in production (ref. 10).

Electrolytic Migration

Electropositive metals, especially silver, but also a number of other metals, including gold, platinum and tin, are susceptible to migration effects as a result of an electric field between adjacent metallization regions.

Scratches in Metallization Stripes

Aluminum and gold, being soft, are quite susceptible to the possibility of scratch formation during device fabrication. Scratches typically would form during the steps of scribing, breaking, and handling the chips to mount them on headers. Harder metals such as molybdenum and chromium are considerably less susceptible to scratches during handling. On the other hand, their lower ductility can result in problems if relatively thick layers are used and are processed through temperature cycles. The problem of scratches in the aluminum metallization can to a very large extent be solved by the process of depositing a dielectric layer over the aluminum prior to scribing. The additional steps required to accomplish this include vapor plating the oxide, typically at 400°C, and using photolithographic techniques to open up areas of the contact pads prior to bonding. The deposited dielectric in this case causes significant improvements in yield through the process and also considerably less susceptibility to reliability problems as a result of scratches and smears of the metallization. Glassing also has the merit of protecting the patterns of closely spaced, adjacent current carrying stripes from corrosion effects, either electrolytic or chemical, and imparting additional freedom from the possibility of shorts due to particles which might bridge between conducting metal stripes. With glassed circuits the only exposed metal is in the area of bonding pads. The spacing between such areas is considerably greater than that between lines in the circuits. Since SiO_2 adheres to aluminum, a wide range of thicknesses of glass can be used.

Deposited dielectrics generally have poor adhesion to gold. Thus wafers in which the top layer in the metallization system is gold are difficult to protect with deposited dielectric unless thick glass layers are used or an additional layer such as chromium or molybdenum is put on top of the gold.

METALLIZATION SYSTEMS

The metallization systems in use today for fabrication of integrated circuits in production can be divided into those used with single-level metallized circuits and those used for multilevel systems containing two or more levels of metallization. The most common metal used in single-level metallization systems is aluminum, and the most common metals used in the layered composite systems are molybdenum-gold and titanium-platinum-gold. All three systems are used in the fabrication of commercially available bipolar integrated circuits. The titanium-platinum-gold system is used in beam-lead fabrication. The systems Al-Si (homogenous) and Ti-Al (layered) are also in use. For MOS integrated circuits, a number of metallization systems are currently in use.

Aluminum is the most widely used system for MOS, with the aluminum obtained by electron-beam evaporation rather than by evaporation from a tungsten coil. The chromium-gold system has been used in MOS. Some MOS devices include silicon gates. Thus, boron-doped polycrystalline silicon is, in effect, a metallization material. Other portions of the metallization of these Si-gate arrays are aluminum metal (refs. 11, 12).

Requirements

The basic requirements of any silicon integrated circuit metallization system are:

1. High conductivity (greater than 10 microhm-cm)
2. Good adhesion to both silicon, dielectrics and glass
3. Low ohmic contact resistance to both n-type and p-type silicon
4. System free from degrading intermetallic compound formation or deleterious silicon reactions during processing or operating life conditions
5. Amenability to practical production methods of deposition and deliniation
6. Resistance to current-induced metal electromigration
7. Freedom from surface instabilities induced by the metal(s) and method of deposition
8. Compatibility with multilevel processing.

The successful production of large-scale integration requires a materials and processing capability for forming metal conductor paths interconnecting the various components. In this respect the following factors must be taken into account:

1. Electrical constraints
2. Chemical needs
3. Metallurgical requirements
4. Mechanical requirements to provide reliable operation
5. The interfaces which must be satisfied by a metallization system.

To consider the electrical requirements, the metallization material must be an excellent conductor, since extremely fine lines are required for multilevel, high density integrated circuits. The thickness of the metal film cannot exceed one-third of the line width. Therefore, for a 2 micron wide conductor line, a 6000 Å thick metal is used, which results in an idealized conductor cross-sectional area of 1-2 x 10^{-8} cm^2. The conducting metal must make ohmic contact to both n-type and p-type silicon. In the case of shallow junctions the emitter and base junctions will be within 1 micron (or less) of the surface. This requires that the metal used for contact to the silicon will not penetrate more than 100 Å.

Table 9 shows the theoretical bulk value resistivity for the better electrical conductors and the ohms per square for a film of this geometry. The total resistance of such a conductor running 10 mils in length is also given. It should be remembered that metals, in general, when deposited as films, exhibit volume resistivities greater than the theoretical bulk resistivities making the table somewhat optimistic.

TABLE 9.- RESISTIVE PROPERTIES OF VARIOUS METALS

Metal	Theoretical Volume Resistivity in Micro-ohm-cm	Ohms/Square for 6000 Å Thick Film	Resistance of a 10 mil Long Conductor, 2 Microns Wide X 6000 Å Thick (ohms)
Ag	1.61	2.7×10^{-2}	3.4
Al	2.74	4.6×10^{-2}	5.8
Au	2.44	4.1	5.2
Cu	1.70	2.8	3.5
Be	3.25	5.42	6.9
Mg	4.3	7.2	9.1
Mo	5.3	8.8	11.2
Rh	4.7	7.8	9.9
Ni	7.8	13.0	16.5
W	5.3	8.8	11.2

Chemically, the metallization must resist deterioration in oxygen at 500°C to survive the post metallization processing steps. Therefore, a metal which produces a thin continuous protective oxide inhibiting further reaction is desirable. Such metals generally are those in which the oxide is less dense than the parent metal. The oxide must also possess a low vapor pressure and must not deteriorate under humid conditions.

The first layer of metallization must act as a reducing agent for silicon dioxide to reproducibly make ohmic contact through the thin oxide layer that readily forms on silicon. When considering the use of multilevel metallization, it is desirable that the metal does not react sufficiently with the dielectric to form conductive electrical paths between the metal layers at the crossover points. It is therefore necessary that the metal be only slightly a reducing agent and that the temperature at which the reduction takes place be reached rapidly and only once to form the ohmic contact. For the contact metal to work effectively, the metal oxide process must readily diffuse into, or react with, the metal rather than remain as an electrical insulator at the interface.

From a metallurgical standpoint, one mode of failure that has been noted is a mass transfer of the metal conductor when carrying a high current density at elevated temperatures. For carrying 1.5×10^6 amp/cm^2 at 175°C, failure is about 23 hours. An exchange of momentum between the electrons and activated metal ions causes the metal ions to be transported in the direction of the electron flow. The result is a depletion of metal at the cathode end where a gradient in current density or temperature exists. The effect is cumulative, further increasing the current density resulting in an open circuit.

As the geometry of the integrated circuit decreases, current densities exceeding 10^6 amp/cm^2 may exist. Since the self-diffusion coefficient for evaporated films decreases when the films become more ordered, the deposition techniques which result in well-ordered films whose resistivity approaches that of bulk metal, will also be more stable at high current densities. Refractory metals have low self-diffusion coefficients, which make them attractive for high current density application.

It is also important that metal conductors do not form intermetallics with silicon or with the overlay metal when subjected to normal processing temperatures (ref. 9). Generally, intermetallics are brittle and highly resistive and, therefore degrade the circuit performance and reliability of the device. To minimize these reactions, metals possessing low diffusion coefficients must be used. An equally important consideration is packaging. Both metal components must be sufficiently soft to flow during bonding. Flow by deformation is required to open fresh and, therefore, clean metal surfaces in intimate contact with each other to promote atomic interdiffusion and crystal growth resulting in a weld.

It is desirable for the conductor used in multilayer metallization schemes to utilize a metal which has a coefficient of thermal expansion near to that of silicon. In the application of glass as a protective layer over the conductor, the bulk expansion differential may be sufficient to cause cracking of the dielectric, thus resulting in electrical shorts. The reduction of glass cracking in multilevel metallization requires that the metal conductor be a reasonable match to the coefficient of expansion of the silicon and the dielectric.

Fabrication Processes

It is very important in the selection of a metallization system to consider the processing steps required in the fabrication of an integrated circuit. These steps are:

1. Deposition of metallization (silicon containing p-n junctions and dielectrics is heated to 200-500^{o}C prior to vacuum deposition and deposition times range from 10-20 minutes for each metal)
2. Heat treatments (5-15 minutes at 300-500^{o}C to insure good ohmic contacts)
3. Glass deposition (200-500^{o}C for 10-20 minutes)
4. Application of solder or eutective bonding material on back of silicon wafer (5 minutes at 200-500^{o}C)
5. Bonding chip to header or package (5 minutes at 400-500^{o}C)
6. Lead bonding (room temperature to 350^{o}C)
7. Sealing package (5-30 minutes at 200-500^{o}C)
8. Operational life stress tests at elevated temperatures (300^{o}C for 1000 or more hours.)

Single Metal Systems

Aluminum is the predominant metallization system used in the fabrication of silicon integrated circuits for the following reasons: (ref. 10)

1. Aluminum can be used in a single-metal system which provides considerable simplicity compared to multimetal systems
2. Aluminum is a low-cost source material
3. Aluminum films have a high electrical conductivity, close to that of the bulk material
4. Aluminum evaporation by a resistance heated tungsten coil is simple
5. Aluminum adheres well to oxides
6. Aluminum layers delineate well by photolithographic techniques
7. Aluminum is easily etched without dissolving SiO_2 or silicon
8. Aluminum reacts with residual SiO_2 in contact areas
9. Aluminum forms low-resistance contacts to n^+ silicon and p-type silicon
10. The solid solubility of silicon in aluminum is such that Al-Si alloys can be used to adjust the amount of penetration at alloying and reduce the amount of penetration as compared to that of pure aluminum
11. There are no compounds in the Al-Si system; thus brittle compounds are not possible, and void formation (Kirkendall effect) has not been a problem at Al-Si interfaces

12. Silicon in solid solution in aluminum does not substantially lower its electrical conductivity
13. Silicon recrystallizes from solid solution in aluminum and contains a substantial amount of aluminum as a p-type dopant, and is thus conductive
14. Aluminum is readily bondable with gold or aluminum wire
15. Aluminum is ductile and thus withstands temperature cycling
16. Aluminum has high resistance to atmospheric oxidation
17. Aluminum single-metal system, in contrast to a system containing several dissimilar metals, cannot result in galvanic action effects
18. The lowest possible melting point in the Al-Si system is the Al-Si eutectic ($577^{o}C$)
19. Aluminum is a satisfactory metallization material for radiation hardened integrated circuits.

For MOS applications the work function of the metal (ref. 13) and the ability to deposit a metal which is free of alkali ion contamination makes aluminum attractive.

It is important that the metallization system be compatible with thin-film resistors and/or capacitors which may be used in integrated circuits. Gold, for example, has been shown to cause devitrification of the amorphous tantalum oxide which is present on stabilized tantalum resistors, and lead to resistor failure (refs. 14 and 15). Aluminum has no such compatibility problems with tantalum.

Aluminum in silicon is a shallow donor (ref. 16) with high solubility. By contrast, many of the other metals used in metallization systems, such as gold, (ref. 16) Molybdenum, (ref. 17) and platinum (ref. 17) have deep lying levels, in some cases with high capture cross sections for minority carriers. Gold and other heavy metals are interstitial diffusants which can precipitate at dislocations in silicon, and may be specifically gettered by the $Si-SiO_2$ interface.

Unfortunately, in certain applications, aluminum does possess undesirable characteristics. Some of the more important limitations of aluminum are listed below:

1. Aluminum is not readily chemically vapor plated in a form which is of high conductivity
2. Aluminum is not readily electroplated
3. Electromigration can form voids in aluminum at current densities lower than those of other metals
4. Electromigration may form spikes which cause shorts through the deposited dielectric in multilevel arrays
5. Aluminum galvanically corrodes with dissimilar metals

6. Aluminum recrystallizes at fairly low temperatures causing hillocks of metal which could break through a dielectric or be difficult to cover
7. Reaction of aluminum and SiO_2 can be significant at temperatures of about $500^{o}C$
8. Aluminum forms compounds with gold which tend to be brittle and result in decreased electrical conductivity
9. Gold wire bonded to aluminum results in reliability problems due to the Kirkendall effect
10. Aluminum is soft and easily scratched
11. Silicon dissolved during contact alloying may precipitate at grain boundaries in aluminum and cause reliability problems
12. Aluminum is typically under stress as deposited
13. The thermal coefficient of expansion of aluminum is greater than that of silicon which results in considerable stress in aluminum during temperature cycling
14. In multilevel metallization structures, the problem of making good aluminum-aluminum contacts has not been completely solved
15. Aluminum is electronegative and corrodes in electrolytes
16. Aluminum is not directly solderable by conventional soldering techniques
17. Aluminum has a higher work function than some metals, and thus results in higher threshold voltages in MOS devices
18. Aluminum dissolves to a small extent in solutions used to etch contacts in deposited dielectrics in multilevel-metallized structures.

High Current Density Tests

High current density tests on aluminum metallization as conducted at $100^{o}C$, $150^{o}C$, and $175^{o}C$ and current levels ($1-2 \times 10^{6} A/cm^{2}$ yielded results shown in Table 10.)

Table 11 presents Mean-Time-To-Failure for aluminum metallization as a function of resistivity and current density.

Examination of the failures showed a single dominating failure mode, i.e. a random opening of the interconnection, occurring in a porous rough-textured metal. During the processing, the aluminum is subjected to $450^{o}C$ for perhaps 30 minutes, and changes from a smooth, nonporous film, beginning to develop a characteristic roughness. This roughness and porosity can be increased by subsequent thermal treatments. The intentional addition of moisture to the dry air furnace has no significant effect. The same rough texture is reported to appear in high current density tests in dry nitrogen sealed To-5 cans. The proposed failure mechanism is that a thermal reaction causes a porosity and reduced cross-sectional area, with a localized increased current density.

TABLE 10.- ALUMINUM HIGH CURRENT TEST DATA

Sample	Resistivity (micro-ohm-cm)	$Jx10^6$	$T(^oC)$	Fraction Failed	Total Test (Hrs.)	50% MTF
2-2	2.6	1.0	178	10/10	14,104	1,300
2-1	4.0	0.93	181	10/10	4,800	440
2-5	4.5	0.93	182	10/10	11,578	1,050
2-7	5.9	1.06	189	10/10	1,046	95
2-3	6.0	1.0	187	10/10	7,745	720
2-6	6.7	0.98	188	10/10	7,745	720
1-2-2	2.6	1.0	109	5/5	2	0.3
2-2-2	2.6	1.0	158	4/10	21,330	4,400
1-1-2	6.0	1.0	119	8/8	7-3/4	0.9
2-1-2	6.0	1.02	172	7/7	5,955	760
3-1	6.1	1.0	193	10/10	7,618	710 Sputtered
3-2	2.6	2.0	189	9/9	680	69
3-1	4.0	2.05	199	10/10	276	25
3-5	4.5	1.96	207	8/8	330	36
3-1	5.9	2.0	225	10/10	60	5.5
3-2	6.7	2.0	238	9/9	78	7.8
1-2-1	2.6	1.99	111	10/10	20-3/4	1.9 MFTI*
2-2-1	2.6	1.99	163	10/10	18-3/4	1.6 MFTI
1-1-1	6.0	1.98	135	10/10	15-3/4	1.4 MFTI
2-1-1	6.0	1.98	185	10/10	19-3/4	1.8 MFTI
3-3	6.0	2.20	225	10/10	140	12.5
1-7-2	3.0	2.16	142	10/10	222	21
2-6-2	3.0	2.20	195	7/7	94	12
1-8-2	3.0	2.19	156	5/5	523	90 Glassed
2-7-2	3.0	2.19	203	7/7	410	53 Glassed
1-7-1	3.0	4.2	182	10/10	13-3/4	1.23
2-6-1	3.0	4.12	234	6/6	6-1/2	0.5
1-8-1	3.0	4.0	193	8/8	14	1.6 Glass
2-7-1	3.0	4.0	243	8/8	8	0.9 Glass

*MFTI = Many Failures on Test Interruption

TABLE 11.- MEAN TIME TO FAILURE FOR ALUMINUM METALLIZATION AS A FUNCTION OF RESISTIVITY AND CURRENT DENSITY

$J = 10^6$ A/cm^2	0.5	1.0	1.2	1.5	2.0	2.8
= 2.6 - cm*	---	1500 hours		--	69	--
= 4.0 < cm	---	470	--	--	25	--
= 6.0 - cm	---	130	--	--	13	--
All available data	480	560	17	20	30	4

*Resistivity varied by deposition rate

This causes localized hot spots and accelerated reaction at these sites. Failure occurs when the voids form continuous breaks across the strip. This is illustrated in figure 16. The 1/2 mil strip was heated 48 hours at 450°C in wet air.

Additional experiments demonstrated the thermal nature of the reaction. Devices with 1/2 mil lines were tested at 2×10^6 A/cm^2 and an oven temperature of 175°C. These units had normal processing, i.e. gold backing, bonding, and To-5 packaging. The mean time to failure was 25 hours. A second group was prebaked at 450°C for 2 hours prior to the high current tests. These units had a mean time to failure of 24 hours. A third group was prebaked 8 hours at 450°C before the high current tests. The mean time to failure was reduced to 15 hours. The aluminum metallization included vacuum evaporated metal using tungsten filaments, tantalum filaments, and electron beam heating. Both normal (10^{-6} torr) vacuum and high (10^{-8} torr) vacuum samples were included. The films were approximately 6000 Å thick, and were generally deposited from 1-10 minutes. All the aluminum tested showed the thermal changes described.

Current induced metal migration is the problem resulting from induced high current density stress. The failure depends on the structure of the film, but lifetime is generally related to the current density by some form of the equation:

$$L = AJ^{-2} \exp. \Phi/KT$$

where L = lifetime in hours

K = Boltzmans constant

T = film temperature

J = current density

A = constant depending on film geometry

Φ = activation energy

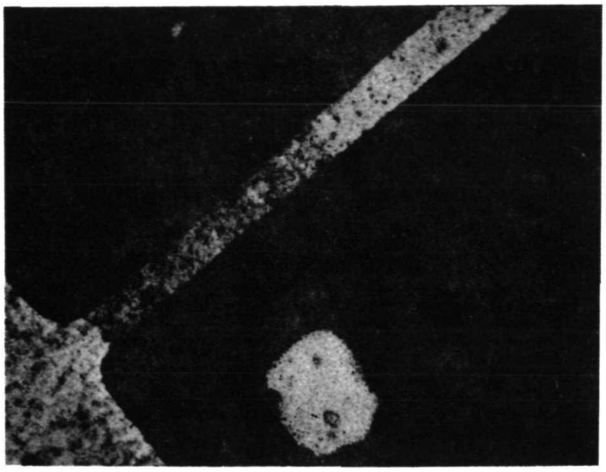
A typical testing procedure could consist of stress levels greater than 10^{-6} A/cm^2. For example, in a 6000 Å film, 75 mA through a 1/2 mil wide conductor is equivalent to 10^6 A/cm^2. For this test, lines 1/2 mil and 1 mil x 54 mil were patterned on oxidized silicon wafers, and the dice mounted on normal To-5 headers. The patterns were connected to the device pins by normal wire bonding techniques, using aluminum or gold wire. The devices were then sealed in dry nitrogen. The testing occurred in temperature controlled ovens, with each device connected to an external load resistor. Measurements of the voltage drop across the external load indicated the current level and the resistance of the sample. By adjusting the value of the external resistance, various current levels could be obtained from a single power supply. Two failure points were used:

1. Opening of the conductor
2. Doubling of the conductor resistance.

Since the samples failed randomly over a period of time, the data was analyzed as follows: the failure time of each sample was obtained daily by periodic checking of each sample. The failure pattern was then plotted on distribution paper. A typical plot is shown in figure 17. Since many samples have shown few failures even after 10,000 hours of test, the mean-time-to-failure in each case is determined from the 50 percent confidence level using the total test hours and the number of failures observed. The mean-time-to-failure from this assumed distribution (Poisson) as compared to the results from distribution plots of the failure times is shown in the correlation plot of figure 18.

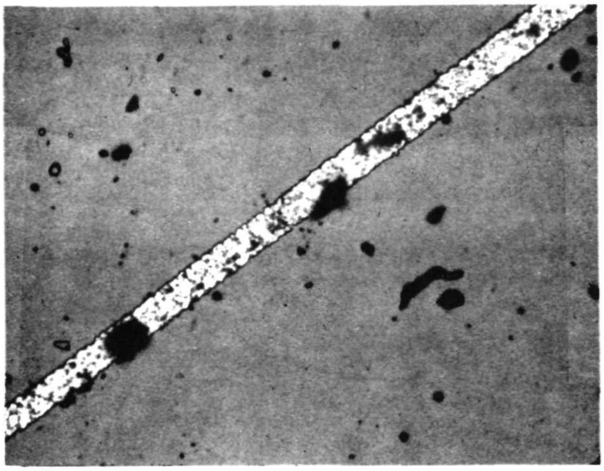
As aluminum is the most widely used metallization system for silicon integrated circuits, comparisons will be drawn throughout the remainder of this survey between the merits and limitations of aluminum and alternate metal systems.

Molybdenum and tungsten appear to be potential single layer contact systems for silicon devices and can be deposited as thin films by either sputtering or electron-gun evaporation.



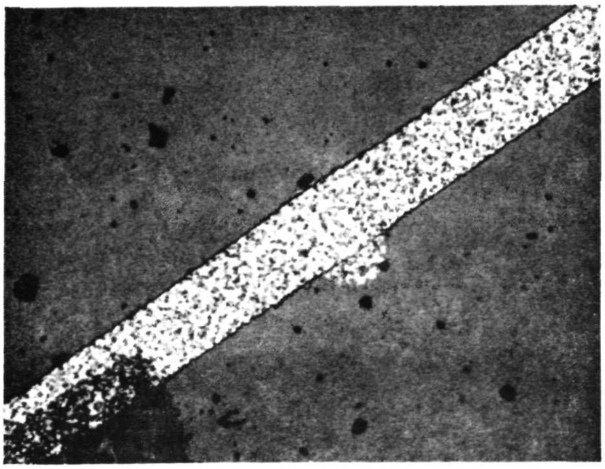
800X

0.5-Mil Line After 48 hrs
450°C



800X

0.5-Mil Line 10^6 A/cm^2
1150 hrs Film Temperature
~180°C



800X

1-Mil Line - No Current

Figure 16.- Photomicrographs of Aluminum Lines

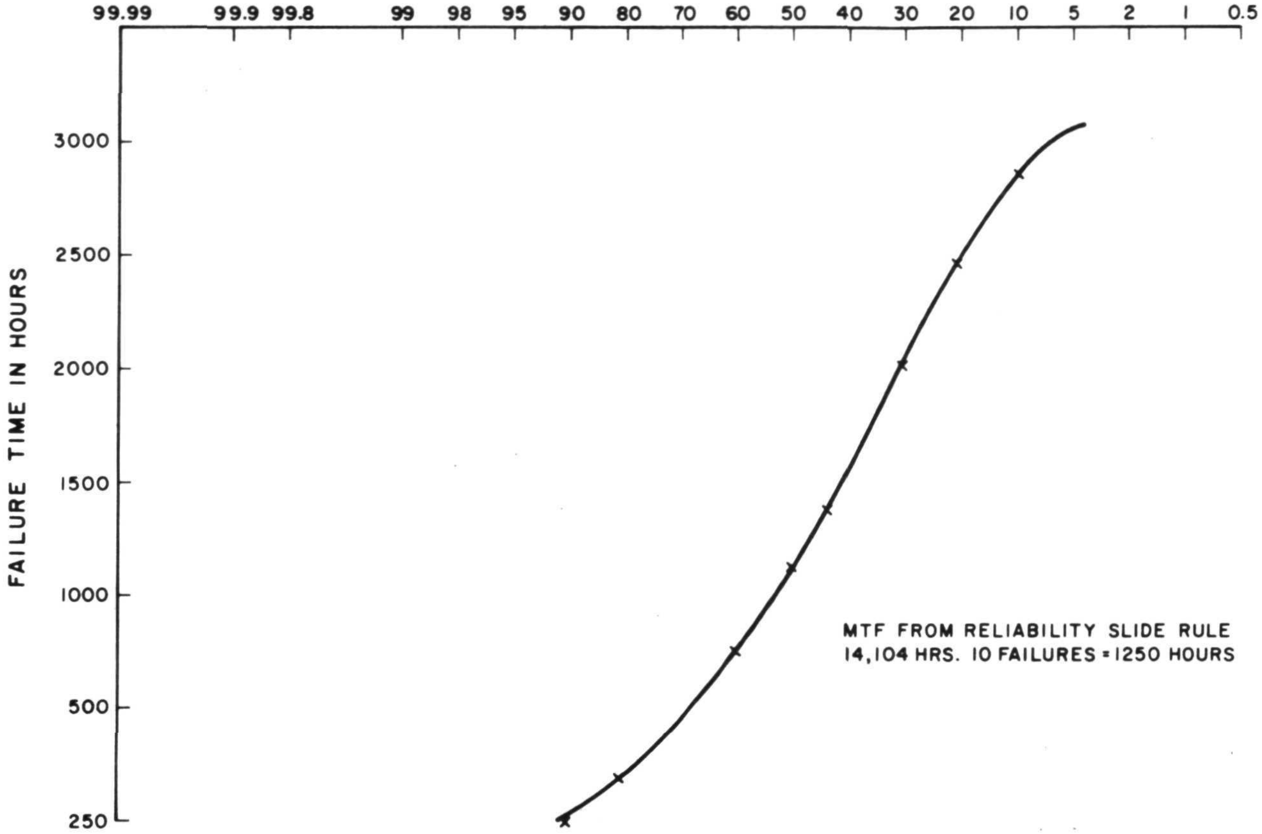


Figure 17.- Probability Plot of Failure Times for Aluminum Sample 2-2 on Test at 10^6 A/cm and 178°C. Resistivity 2.6 micro-ohm-cm

A summary of the film properties is presented in Table 12. The values of resistivity for these films as shown are several times higher than the bulk value. Therefore, for equal conductivity, a Mo or W single layer would have to be several times thicker than aluminum. The resistivity depends upon the deposition conditions, and values lower than those in Table 12 have been referred to in the literature. For example, Gland (ref. 18) found that molybdenum deposited by electron-gun techniques decreased in resistivity with increasing substrate temperature until near bulk resistivities were obtained at 600°C. Bias and getter sputtering (refs. 18 and 19) have also been used to obtain Mo films with resistivities near bulk. However, these techniques do not lend themselves to mass production of silicon integrated circuits.

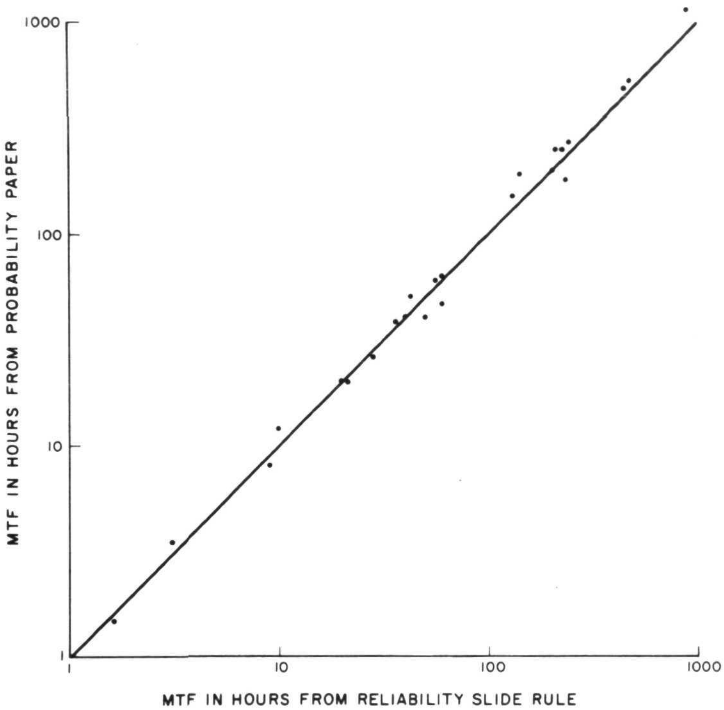


Figure 18.- Correlation Plot Comparing Mean-Time-To-Failure from Distribution Plots and from Reliability Slide Rule

TABLE 12.- DEPOSITION DATA AND PROPERTIES OF W AND Mo

	RF Sputtered		Electron-Gun
	Mo	W	Mo
Deposition Rate	250 Å/min	100 Å/min	10-20 Å/sec
Substrate Temperature	200°C	200°C	200°C
Deposition Pressure	5 microns	5 microns	10^{-6} to 10^{-5} torr
Film Resistivity	15 micro-ohm-cm	25 micro-ohm-cm	30-40 micro-ohm-cm
Adherence	Fair	Fair	Marginal
Ohmic Contact (Si)	Fair, but difficult to reproduce		

Poor adherence to SiO_2 eliminates the high conductivity metals, e.g. Au, Ag and Cu, as single layer systems. It therefore appears that no single layer system will replace aluminum.

Consequently, a two-metal system in which the bottom metal provides adherence, good contact, and metal interaction barrier properties followed by a high conductivity layer which will also accept wire bonds, will be the alternative.

Composite Layered Metallization Systems

The composite layered metallization system consists of a metal which adheres well to SiO_2-Si, on top of which is deposited a high conductivity metal layer. As there are few, the discussion will be limited to several refractory metals combined with Au or Ag as sandwich structures. Although the problems and limitations discussed will refer to these specific systems, some of the general statements could most certainly be extended to other combinations.

Reactions with Silicon and Between Metal Layers.- Some of the expected problem areas may be deduced from the composite films themselves and a knowledge of silicon semiconductor processing. For one thing, the Au-Si eutectic of 377°C means that the layered structure must prevent Au from reaching the silicon during processing steps at temperatures above 377°C.

In cases of metal-Au reactions, there is a resistance increase caused by intermetallic diffusion or compound formation. These visible Au-Si alloying and resistance changes at 450°C air bakes are used as indicators in evaluating the metal systems. To cite an example of such evaluations; oxidized silicon wafers coated with thin metal films are photomasked and the metals etched into 54 mil long conductors, both 0.5 mil and 1.0 mil wide. The test patterns are probed for resistance and baked at 450°C air and 625°C N_2 for times up to 24 hours. Results of such tests are summarized in Table 13. The resistances of several of these are seen to increase considerably over the initial values. These increases may be explained by the diffusion of one of the metals into the other, or by intermetallic compound formation. The resistivities of several metal alloys containing other metals as impurities were tabulated in the International Critical Tables (ref. 6), and show that the resistivity of the binary alloys may be several times larger than the bulk values of either of the components. In a few systems, the resistivity decreased slightly and is attributed to annealing in the higher conductivity materials, e.g.; Ti-Ag and Mo-Au.

CR-Au, Ti-Au and V-Au.- The evaluation of these systems is similar in that all three show large resistance increases after a few minutes at temperatures of 350-450°C. The increases are particularly significant if the Ti, Cr, and V thicknesses are made large to prevent Au-Si alloying.

TABLE 13.- RESISTANCE OF VARIOUS METAL(S) AFTER AIR BAKES, 1- x 54-MIL CONDUCTORS, ALLOY TESTS ARE ON 20-MIL^2 CONTACTS

Metals and Thickness	Resistance, 1-mil x 54-mil conductor, after							
	450°C				650°C			
First Layer ↓ Total Film ↓	Int.R	2 Hrs.	4 Hrs.	Au-Si Alloy	Int.R	2 Hrs.	4 Hrs.	Au-Si Alloy
Al 7000Å	2.7	2.6	2.7					
Cr-Au 2000, 6500Å	5.8	17.4	19.0	100% at 1 Hr.				
Ti-Au 2000, 6500Å	5.4	12	18	100% at 1 Hr.				
V-Au 800-9900 Å 1600-6600 Å	1.7 Ω 3.5	3.6 Ω 7.1	3.6 Ω 5.9	300/400 after 1 Hr.	1.7 Ω 3.6	6.6 Ω 8.3	5.6 Ω 9.5	100% after 30 min.
(Ti-Pt)-Au 3000, 9000Å	2.9	4.0	4.3	0/120 at 4 Hrs.				
Mo-Au 2100, 10000Å 2700, 7200Å	3.2 3.1	2.5 2.8	2.5 2.8	1/400 at 4 Hrs.	2.7 3.2	2.3 2.7	2.3 2.8	12/400 at 4 Hrs.
W-Au 1400-6600 -7200	2.6 3.4	2.6 2.8	2.5 2.7	2/400 at 4 Hrs.	2.5 3.3	2.5 2.7	2.4 2.74	6/400 at 4 Hrs.
Ti-Mo-Au 500, 1500Å 5500Å	5.6	5.7	5.7		5.3	4.8	5.0	
W-Au-Ti -300Å (Ti)	4.9	3.4	3.2		4.7	2.7	2.6	

TABLE 13.- RESISTANCE OF VARIOUS METAL(S) AFTER AIR BAKES, 1- x 54-MIL CONDUCTORS, ALLOY TESTS ARE ON 20-MIL^2 CONTACTS (CON.)

Metals and Thickness	Resistance, 1-mil x 54-mil conductor, after							
	450°C				650°C			
First Layer ↓ Total Film ↓	Int.R	2 Hrs.	4 Hrs.	Au-Si Alloy	Int.R	2 Hrs.	4 Hrs.	Au-Si Alloy
Ni-Au -6500 Å 2700-9500 Å	2.8 2.8	3.3 7.0	2.9 7.0	5/400 after 1 Hr.	3.0 2.6	open 10Ω	open	300/400 at 30 min.
Co-Au 8800 Å 9500 Å	2.4 2.5	2.6 2.7	2.5 2.9	50/400 after 1 Hr.	2.4 2.5	2.4 2.5	2.4 2.5	
Zr-Au 1000-6900 2300-7200	2.3 3.1	2.5 3.0	2.4 2.9	100% after 1 Hr.	2.4 3.2	5.1 5.4	5.03 4.3	
Ta-Au 1600,7200	3.0	3.6	4.2	22/400 at 4 Hrs.	3.1	6.1	5.4	6/400 at 30 min.
Nb-Au 1600-7600 Å 1600-5000 Å	2.5 5.4	3.0 8.9	3.2 9.1	3/500 at 4 Hrs.	2.6 5.3	4.3 19	4.4 18	100/500 at 1 Hr.
Hf-Au 1200-6300 -10000	2.8 2.4	3.6 2.6	3.5 2.6	25/400 at 4 Hrs.	3.0 2.4	9.8 40	9.5 22	

The as-deposited resistivity of the Cr-Au composite films ranged from 6-15 micro-ohm-cm due probably to the relative amount of Cr and Au in the composite film. Increases in resistance after 450°C air bake are shown in figure 19. It is interesting to note that the resistances of films with Cr thicker than 1000 Å increases 200-600 percent within an hour at 450°C and then tapers off. The films with heaviest interface blending (second metal deposition started before the first metal is completely deposited), tend to increase more. Recent studies of Cr-Au (ref. 1) have noted resistance increases as large as 170 percent after 50 hours at 350°C in nitrogen ambients. The results found on sputtered Cr-Au are similar, and the magnitude of the resistance increase is too large to be a simple oxidation of Cr from under the Au. The more plausible explanation lies in the solid state diffusion of Au into the Cr (or Cr into the Au), which results in the formation of a higher resistance intermetallic compound.

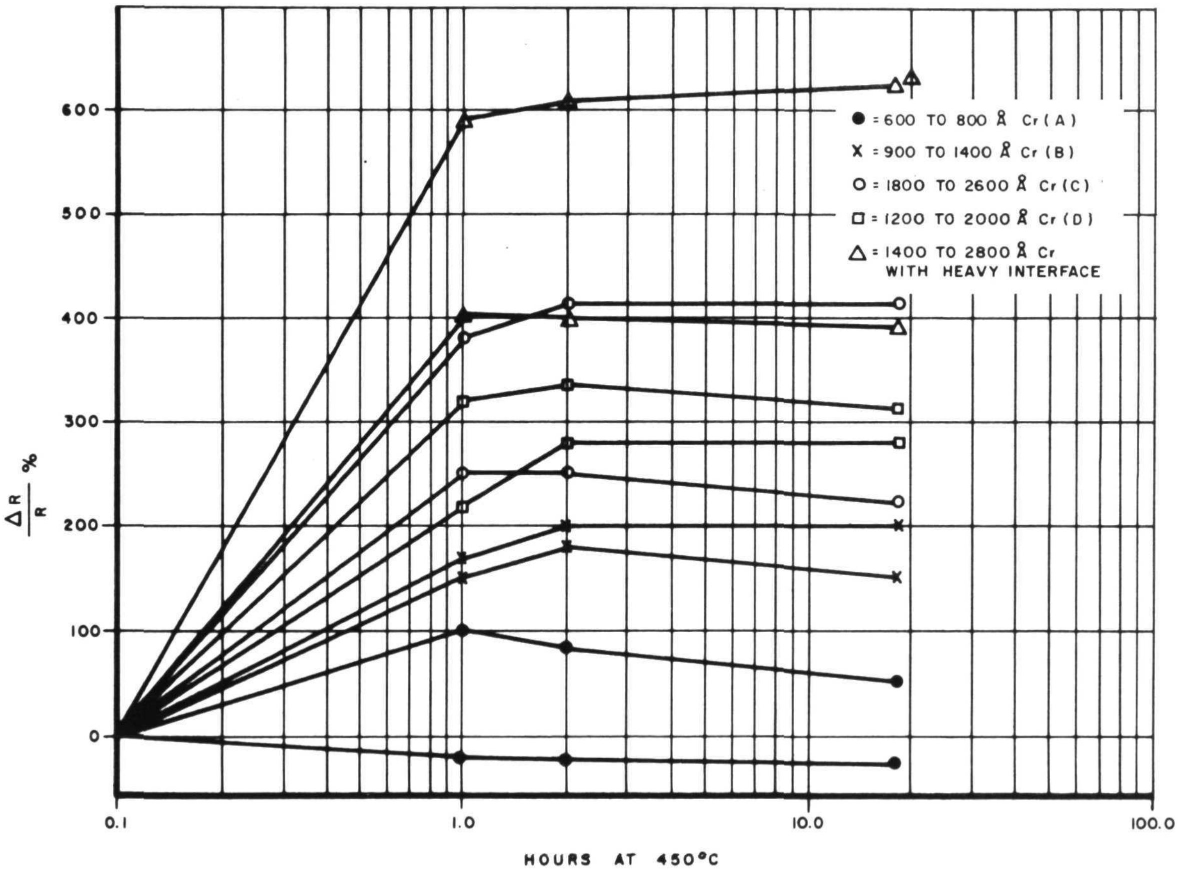


Figure 19.- Resistance Change in Cr-Au Films, Au Thickness 5000 Å

It is very important that gold does not come into contact with silicon at the contact areas. To test for this effect, tests were conducted where various thicknesses of chromium were deposited onto oxide-free silicon wafers while the gold thickness was kept constant. Visual indications of the Au-Si reaction were made and the expected behavior was that the time required for the alloying to occur would increase with Cr thickness. This was not observed on all the oxide-free wafers alloyed within 1/2 hour at 450°C, even though the thickest Cr film was 1500-1900 Å thick.

Similar to the Cr-Au system, it was found that increasing the thickness of titanium increases the resistivity of the titanium-gold metallization, and greatly accelerates the thermally induced resistance rise. The resistivity of 500 Å of titanium and 7000 Å of gold at 450°C increases only 50 percent after 2 hours. By comparison, the resistivity of 2000 Å of titanium and 2000 Å of Au increases by a factor of 15 in 15 minutes at 450°C, and continues to rise for several hours. With 500 Å of titanium the gold reacts with the titanium and silicon in less than 5 minutes at 450°C.

From these results it is apparent that in the Cr-Au, Ti-Au, and V-Au metallizations, the alloying of the gold with silicon through the interface metal is the limiting factor in their use. Increasing this intermediate metal thickness to 1000 Å delays the alloying somewhat, but produces a composite film with a high resistivity. The use of 500 Å of bottom metal gives a film with acceptable resistance properties on SiO_2, but would be unsatisfactory if used in contact with exposed silicon.

Ti-Pt-Au.- The Ti-Au system as discussed previously, can exhibit undesirable intermetallic compound formation. With a barrier metal between the Ti and Au this combination can be useful. Such a system has been developed (ref. 20) in which platinum is used as a barrier to prevent Au-Ti or Au-Si reactions and is used in the beam lead technology. The properties of the metal system will be devoted to beam lead technology.

As an evaluation technique, films of Ti-Pt and Pt-Au were deposited and the thermal behavior studied. The Pt-Au films were formed by sputtering Pt onto a heated SiO_2-Si wafer (250°C) to a nominal thickness of 2000 Å, and then Au was filament-evaporated onto the Pt to a thickness of from 1000 Å to 10,000 Å. The Au and Pt were then rf sputter-etched using photoresist as a mask. The Ti in the Ti-Pt films was deposited by sputtering to a thickness of 2000 Å, the Pt was then sputtered to a nominal thickness of 2000 Å. After sputter-etching the Pt into strips

1 mil wide and 54 mils long, the remaining Ti was removed by chemical etching in a dilute H_2SO_4 solution. The wafers containing the etched patterns were then scribed into three pieces. Measurements were taken, samples were baked at 450°C in air, and remeasured at one hour intervals for 24 hours. The resistance of Pt-Au composite films increased with time at 450°C. The changes shown in Table 14 are scattered, but there is a trend indicating that films containing both small and large amounts of Pt have less of an increase than an intermediate composition film.

TABLE 14.- ΔR OF Pt-Au FILMS WITH 450°C AIR BAKES

Platinum, Percent of Film	Initial ρ Micro-ohm-cm	+ΔR After 2 Hours Percent	ΔR After 4 Hours Percent	T_{Au} (Å)	T_{Pt} (Å)
23	3.7	75	90	11,000	3,300
25	3.6	120	150	6,700	2,300
25	3.6	110	135	6,700	2,300
27	4.6	150	160	4,350	1,650
31	4.5	120	150	5,600	2,500
32	4.6	150	150	4,100	2,000
35	4.6	125	143	6,000	3,300
50	7.6	115	120	1,650	1,650
70	9	125	130	1,100	2,500

The Pt-Au films, after 24 hours at 450°C, were heated to 1000°C for 30 minutes in forming gas to permit them to proceed to a more complete reaction and the final resistance was measured at room temperature. Table 15 compares the experimental resistivity data on Pt-Au after the 1000°C bake with various literature values (refs. 21 and 22) and shows fair agreement. These results indicate that the layered Pt-Au film resistivity can increase by a factor of 10 if complete alloying occurs. The results also show that the resistance change of Pt-Au composite films will be smallest for Pt concentrations less than 35 atomic percent. Hence, the Pt thickness in Pt-Ti-Au should be as thin as possible consistent with retaining the barrier between the Au and the underlying silicon.

The Ti-Pt system likewise undergoes a resistance increase upon thermal treatment at 450°C. As presently used in Ti-Pt-Au systems, the Ti is about 2000 Å and the Pt is 2000 Å. The resistivity of the sputtered Ti is 200 micro-ohm-cm and the sputtered Pt is about 25 micro-ohm-cm. The resistance of a composite Ti-Pt film increases from an initial value of 45 micro-ohm-cm to 75 micro-ohm-cm after two hours at 450°C. This indicates that the Pt can react with both the Ti and the Au to form complex binary and even ternary alloys.

TABLE 15.- RESISTIVITY OF Pt-Au AFTER 30 MINUTES AT 1000°C

Pt-Vol. Percent	Resistivity (micro-ohm-cm)		
	This Work	Reference 8	Johansson 9
10		10	10
23	28	18	23
25	30	19	28
30	35	20	32
35	38	28	38
40		32	37
50	34		35
70	32		32

Table 16 contains some experimental thermal aging data of the Ti-Pt-Au composite films with various Pt-Au thicknesses. Fortunately for users of this system, the delta R of the films with Ti under the Pt is less than the Pt-Au films in Table 16. Evidently, the reaction between the Ti and Pt has reduced the amount of Pt available for reacting with the Au. Note that for Au/(Pt-Ti) thickness ratios of 8500/4500 Å the resistance increase can be held to less than 50 percent after two hours at 450°C. This figure could perhaps be decreased even more by reducing the Pt thickness to a minimum value consistent with preventing the Au from reaching the Ti or Si.

TABLE 16.- ΔR of Ti-Pt AND Ti-Pt-Au AT 450°C

Au (Å)	Ti+Pt (Å)	Int. ρ Micro-ohm-cm	Percent ΔR After 2 Hours at 450+	ΔR After 4 Hours+
0	4400 Å	45	70	
8500	4500	4.8	36 percent	36 percent
*7000	3600	5.0	45 percent	57 percent
6000 Å	3000	4.8	40 percent	48 percent
4000	3300	4.8	100 percent	120 percent
**8400	2600	3.8 micro-ohm-cm	50 percent	58 percent

* Au was electroplated, all other Au were evaporated.
**Film has ~10,000 Å of glass overcoat, + time is indicated ±20 minutes.

The previous discussion indicated that for a minimum change in resistance the volume ratio of Au-Pt should be large or the Pt should be as thin as possible, consistent with preventing the Au from reaching the Ti. This minimum Pt thickness was sought in a series of Au-Si alloying tests in which the Pt thickness ranged from 450-2100 Å. The contacts, consisting of Ti (1500 Å)-Pt-Au (7000 Å) on 20 mil^2 and 100 mil^2 areas of silicon, were baked at 450°C for times ranging from 15 minutes to 4 hours. The test results are summarized as follows:

1. After 4 hours with 450 Å Pt, 10 out of 120 large areas and 5 out of 120 small areas alloyed
2. With 2100 Å Pt, 1 out of 120 large areas and none out of 120 small areas alloyed after 4 hours
3. No well defined minimum Pt thickness existed which would prevent Au-Si alloying
4. Larger areas alloyed first for a given Pt thickness.

The area dependence indicated that pinholes in the Pt were more important than solid-solid diffusion. Assuming that pinholes are the major problem,then the Pt should be as thick as possible to reduce the probability of pinholes, and the Au made correspondingly thicker to reduce thermally induced resistance changes.

Summarizing, the Ti-Pt-Au system can increase in resistance in 450°C bake cycles. This resistance increase is caused by interdiffusion of the Au and Pt. Still,the system can be extremely useful at temperatures of 450°C by making the volume ratio of Au/Pt greater than approximately 3/1. 1500 Å to 2000 Å of Pt is effective in preventing Au-Si or Au-Ti reactions at 450°C.

<u>Cr-Ag-Au and Ti-Ag-Au</u>.- In these systems the Ag and Au behave similarly to the Pt-Au in that the Au and Ag form a continuous series of solid solutions and the resistivity increases drastically during heat treatment. This is in agreement with published values for Ag-Au alloys. For example, Mott and Jones (ref. 21) show the resistivity of a 50 atomic percent alloy to be 24 micro-ohm-cm compared to 1.61 for pure silver and 2.44 for pure gold.

In general, experimental data on Cr-Ag-Au as compared to Ti-Pt-Au, show that the Cr-Ag-Au resistivity after several minutes of 450°C bakes is higher, and that Ag-Au interdiffusion can occur as low as 350°C in a relatively short time. The initial values of resistance in the Cr-Ag-Au system are higher than expected from known individual film resistivities indicating a reaction has already taken place during deposition and subsequent processing. Table 17 shows typical resistance changes obtained on Cr-Ag-Au and Ti-Ag-Au. In both systems the Ag is effective in preventing the Au-Si eutectic formation.

TABLE 17.- Cr-Ag-Au AND Ti-Ag-Au RESISTANCE CHANGES

	Initial Micro-ohm-cm	After 1 Hour at 350°C	After 1 Hour at 450°C
Cr-Ag-Au 1000, 6000 Å (1)	4.2	8	16
Covered with a passivating glass		6	11
Ti-Ag-Au 2000, 8000 Å (1)	4.0	7	17
(1) Au-Ag thickness			

The Cr-Ag-Au system is not as thermally stable as Ti-Pt-Au. However, with these limitations in mind, an excellent low temperature system in Cr-Ag-Au has been developed (ref. 22) for metallization of transistors.

Omitting the Au from the Cr-Ag-Au and Ti-Ag-Au increases the thermal resistance stability as shown by the data in Table 18. Note that after 2 hours at 450°C in air, neither the Ti-Ag nor Cr-Ag had exhibited a large increase in resistance.

Air bakes cause some discoloration of the Ag surface which may be due to oxidation. However, the small resistance change in Ti-Ag indicates that the effect of the Ag oxidation is slight. The discolored surface may present problems in wire bonding directly to the Ag film but in multilayer LSI work, the top metallization could be overlayed with a thin Au film to facilitate this operation.

The smaller change in Ti-Ag than in Cr-Ag shown in Table 18 is real and has been repeated several times. The small changes in both Ti-Ag and Cr-Ag resistance up to two hours at 450°C indicates that both may be combined as Ti-Ag-Cr or Cr-Ag-Ti and used in multilayer LSI work. The top film of Cr or Ti would be used to increase the adherence of the glass that is used to separate the conductor levels.

TABLE 18. Ti-Ag AND Cr-Ag RESISTANCE CHANGES (1 mil x 54 mil)

	Initial R (ohm)	2 Hours at 450°C air	4 Hours at 450°C air
Cr-Ag 2800, 6800 Å	2.1	3.9	25
Ti-Ag 1500, 3500 Å	3.4	2.9	2.9

Mo-Au and W-Au.- As additional composite metal systems, Mo-Au and W-Au systems have been considered. In the Mo-Au system as with the other refractory metal-gold systems the thickness of the molybdenum film is considered critical. In one set of experiments to investigate the thermal stability of the Mo-Au system, the molybdenum thickness was varied from 500 Å to 8200 Å. No resistance increases were found after four hours at 450°C, provided the ratio of Au/Mo was greater than about 3/1 and no interface mixing of the Mo and Au was used during deposition. In films which had blended interfaces during deposition and thin Au (1500 Å Au/2000 Å Mo), the resistance increased 20-50 percent after four hours at 450°C. Using relatively good vacuum of 10^{-6} to 10^{-5} torr and sequential deposition of the Mo and Au in the same pump down, the Au to Mo adherence is excellent and no interfacial blending is necessary to promote adherence. It has been reported in the literature (ref. 23) that the thermal behavior of sputtered and electron-gun Mo covered with filament-evaporated or low pressure triode sputtered Au are similar in that no increases in resistance are observed. However, it was noted that the low pressure triode sputtered Au had 2-3 times the resistivity of the evaporated Au (ref. 23). The high Au resistivity is attributed to scattering at grain boundaries. The gold films contain extremely small crystallites due to a large number of nucleation sites which are enhanced by the sputtering mode of deposition. Using 2100 Å of Mo prevents Au-Si alloying at 450°C.

The Mo-Au and W-Au systems behave similarly in thermal stability tests even after 4 hours at 625°C. Any resistance change was less than 5 percent and it usually decreased, indicating an annealing effect. Tungsten is as effective as molybdenum as a barrier metal.

Unfortunately, the adherence of both Mo and W to SiO_2 is marginal, so an additional adherent layer is sometimes used. Titanium has worked as an excellent "glue" for these materials. Even with the titanium, the thermal stability of Ti (500 Å)-Mo or W (2000 Å) and Au films is satisfactory. Data on typical films are summarized in Table 19.

Ni-Au or Co-Au.- The behavior of these films is not similar to any of the others discussed. A slight reaction between the metals occurs; but tests show that after one hour at 450°C the surface of the Au becomes discolored and the film is hard and rough. This could make wire bonding difficult. In the case of Ni-Au the nickel did not prevent Au-Si alloying.

TABLE 19.- RESISTANCE CHANGE

Metals and Thickness	Resistance of 1 mil x 54 mils Strip After							
	450°C Air Bake				625°C Air Bake			
	Initial Resistance	Resistance After 2 Hours	Resistance After 4 Hours	Au-Si Alloy (2)	Initial Resistance	Resistance After 2 Hours	Resistance After 4 Hours	Au-Si Alloy
W - Au								
1400-6600 Å	2.6	2.6	2.5	2/400 at	2.5	2.5	2.4	6/400 at
(1) 2500-7200 Å	3.4	2.8	2.7	4 hours	3.3	2.7	2.74	4 hours
Mo - Au								
2100-10K Å	3.2	2.5	2.5	1/400 at	2.7	2.3	2.3	12/400
2700-7200 Å	3.1	2.8	2.8	4 hours	3.2	2.7	2.8	4 hours
To - Mo - Au								
(3) 500, 1500 Å								
5000 Å	5.6	5.7	5.7		5.3	4.8	5.0	

(1) The second thickness value is the total thickness

(2) Metal-Si contact area 4 x 5 mils

(3) 0.5 x 54 mils strip

Resistance Change and Au-Si Alloying

Some fairly comprehensive data are summarized in Table 20. Combining results from tests along with adherence properties and fabrication difficulties indicates that no one system will meet all requirements listed in the previous section.

TABLE 20.- SUMMARY, RESISTANCE CHANGE AND Au-Si ALLOYING

Metals Examined	+ ΔR at 450°C 2 Hours	Au-Si (1 hour at 450°C) Alloying
Al	0	
Ti-Pt	0	
Ti-Rh	0	
Ti-Pt-Au	<50 percent	No
Ti-Ag-Au	>100 percent	No
Ti-Mo-Au	0	No
Ti-Ag	5-10 percent	
Cr-Ag-Au	>100 percent	No
W-Au	0	No
Zr-Au	<50 percent	Yes
Nb-Au	<100 percent	No
Ni-Au	<100 percent	Some
Co-Au	<50 percent	Some
V-Au	>100 percent	Yes
Ta-Au	<50 percent	Some
Cr-Au	>100 percent	Yes
Ti-Au	>100 percent	Yes
Mo-Au	0	No
Hf-Au	<50 percent	Some

In general, the systems which most nearly meet these requirements may be separated into two groups:

1. Those destined for low temperature applications, e.g. beam leads or plastic encapsulation
2. Metallization for systems requiring relatively high temperature long processing schedules, LSI multilayer systems.

The combinations that could be useful as a substitute for aluminum in these two groups are:

(a) For beam leads and plastics; Ti-Pt-Au, Ti-W-Au, Ti-Pt, Ti-Rh and perhaps Ti-Ni-Au and Ti-Co-Au
(b) For multilayer LSI; Ti-Mo-Au, Ti-Pt-Au, Ti-Ag and Cr-Ag.

Systems which may also be satisfactory to use for beam leads and plastics include Ta-Au, Hf-Au and Nb-Au but so far an etchant has not been developed that will etch these materials without also attacking the silicon or SiO_2.

In the search for an alternate metallization system to replace aluminum, it readily becomes apparent that no alternative single layer material conveniently satisfies all the necessary requirements. Briefly these are:

1. Good adhesion to silicon and silicon dioxide
2. Satisfactory ohmic contact to silicon
3. Good conductivity-resistivity less than 10 micro-ohm-cm
4. Economical to use, i.e. easily deposited in thin films and configured by etching.

In the previous sections, alternate materials were discussed; they consisted of a refractory metal layer followed by a noble metal which acts as the main conductor. One of the most satisfactory substitutes consisted of a titanium layer followed by a platinum barrier film between the titanium and an upper gold film which acts as the primary conductor. Obviously, such a composite film is more complex than aluminum to deposit and quite difficult to etch, but the versatility of the new sputtering techniques in both deposition and etching of metal layers has significantly offset this drawback.

Furthermore, the excellent characteristics of refractory-noble metal systems with respect to shallow penetration into silicon, excellent resistance to deterioration in adverse environments and the greatly increased current carrying lifetime, as compared to aluminum, makes their usage most attractive on high frequency, high power devices and integrated circuits.

CONTACT RESISTANCE

The amount of contact resistance and linearity of resistance introduced by a metallization process is an important problem in the successful fabrication of integrated circuits. This section summarizes the results of contact measurements using metal layers of Al, Cr, Mo, Ni and Ti; with and without a platinum silicide layer on both N and P type silicon. The PtSi process used here is similar to the process described in reference 20.

Experiments were conducted on N and P type silicon samples with approximately 5000 Å thermal oxide, photomasked and 4 x 5 mil contact areas spaced approximately 4 mils apart etched through the glass down to the silicon. The various metals were deposited by a filament evaporation, electron beam evaporation, or low pressure dc sputtering.

The measurement technique included probing four adjacent metallized pads, two with the DVM leads and two with the constant current leads. The contact resistance as measured included the effects of spreading resistance (ref. 24). To check for non-linearity, measurements were made at 10 and 100 mA. and visually monitored on a transistor curve tracer. These results are shown in Table 21 and represent the average from several runs. Generally, values were reproducible to better than ± 25 percent.

The data of Table 21 shows that various metals have low ohmic contact resistance on low resistivity n and p type silicon. As the silicon resistivity increases, the contact resistance increases, as does the nonlinearity. All of the metals exhibited rectifying contacts on n type silicon above about 0.01 ohm-cm. Although the contact resistance increases, the Al p-type silicon contacts are ohmic at least up to 1 ohm-cm particularly after a mild bake, ($450^{\circ}C$ - 10 minutes). It is of interest to note that this same heat treatment increases the contact resistance of aluminum on n type silicon (0.1 ohm-cm).

The use of Pt-Si is known to lower the contact resistance regardless of the metal used, especially on mid-resistivity n type silicon, where an order of magnitude reduction is obtained. The resistance values for the various metals on PtSi-Si is almost independent of the metal used, suggesting that the potential barrier is in the PtSi-Si region. An independent measurement of the resistivity of PtSi shows that it is approximately 100 micro-ohm-cm (bulk Pt = 10 micro-ohm-cm). For the areas of the contacts used, this yields a figure of 10^{-5} ohms and therefore would not be detected in these measurements.

In addition to lowering the contact resistance, the PtSi yields ohmic contacts to higher silicon resistivity. For example,

TABLE 21.- METAL SILICON CONTACT RESISTANCE, IN OHMS, AREA = 10^{-4} CM^2

Si Resistivity (ohm-cm) and Type	Metal and Metal + PtSi									
	Al	PtSi	Mo	PtSi	Ni	PtSi	Cr	PtSi	Ti	PtSi
0.001 N	0.09	0.02	0.08	0.02	0.02	0.02	0.03	0.03	0.01	0.01
0.01 N	6 (R)	0.1	5 (R)	0.4	2	0.03	3 (R)	0.2	4	0.2
0.1 N						40 (R)				50 (R)
0.002 P	0.03	0.02	0.06	0.03	0.02	0.02	0.04	0.04	0.01	0.01
0.04 P	1	0.7	3 (R)	1	4 (R)	2	8 (R)	1		0.9
0.08 P					45 (R)	4				3
0.5 P	20	10	80 (R)	10	100 (R)	20	200 (R)	15		15

(R) Indicates Rectifying Contact identified by the relation $R_{10\ mA} = R_{100\ mA}$ (See figure 1).

the Al-N-Si contacts rectify at 0.01 ohm-cm. This figure is increased to approximately 0.05 ohm-cm for Al-PtSi-N-Si.

In the early use of platinum contacts it became obvious that the silicon must be as free as possible of oxide and contaminants if the platinum is to form the silicide. The platinum silicide process used includes:

1. the deposition of platinum after a pre-ohmic etch, with either an electron gun or sputtering.
2. Sintering at 600-700°C to form the silicide.
3. Chemically removing the excess platinum from the SiO_2 masked surface.

Since platinum will not reduce the silicon oxide it is imperative that silicon in contact areas be oxide free. If this is not the case then the PtSi will not form.

TEMPERATURE STABILITY

Air bakes at 450°C for 15 minutes generally lower the contact resistance (but rarely more than 50 percent) if the surface is clean and proper shielding of the substrate is used during the initial evaporation or pre-sputter. An exception to this was aluminum on n-type silicon, where the resistance increased 25-50 percent during the bakes. In general, the changes were less on PtSi units. Evidence of the stability of metal PtSi contacts is shown in Table 22. These data compare the contact resistance obtained on AlSi and Al-PtSi-Si contacts with heat-treatment, and indicate the stability of the PtSi at elevated temperatures. Other tests conducted, with MoAu on PtSi-Si contacts, also showed extremely stable behavior on long term storage at 250°C.

TABLE 22.- TEMPERATURE STABILITY, CONTACT RESISTANCE IN OHMS

Si Resistivity and Type	Initial Resistance (ohm)		After 15 min. 450°C Cir		After 15 min. 600°C Forming Gas	
	Al	+PtSi	Al	+PtSi	Al	+PtSi
0.001 N	0.08	0.02	0.08	0.02	4 to 10 (R)	0.02
0.01 N	4 to 9 (R)	0.1	50to 20 (R)	0.1	15 to 60 (R)	0.09
0.002 P	0.03	0.03	0.02	0.02	0.1	0.02
0.5 P	50 to 70 (R)	30	25	30	25	

(R) Indicates Rectifying Contact

CURRENT DENSITY

In this section various metal systems in use will be discussed as to current density capabilities and high temperature operation reliability. In each case the results will be compared to relative data on aluminum metallization.

Chromium-Gold

Some chromium-gold test results are given in Table 23. Related groups are averaged to increase the sample sizes. The mechanism of the chromium-gold failures was discussed previously in reference to the thermally induced resistance rise. The observed doubling of the conductor resistance in 500 hours at about 220°C is in agreement with the self-diffusion energy for gold, or about 1.8eV. Although the resistance rise occurred in all samples, including those not carrying current, many of the samples continued to conduct for many hours, although with increased power dissipation. Eventually, burnout occurs. Glassing of the chromium-gold system did not improve the life at the lower current levels, but merely accelerated the resistance rise mechanism by the elevated temperature processing.

Chromium-Silver-Gold

As indicated in the thermal testing section, the addition of silver to the chromium-gold metallization improves the thermal stability. Samples under discussion were prepared with 22 percent silver by volume of the gold. The films were patterned and glassed. The resistivity rose to 15 micro-ohm-cm for the encapsulated units. Current density tests at $2x10^6$ A/cm^2 and 222°C gave a mean-time-to-failure of 600 hours. A sample at $1x10^6 A/cm^2$ and 195°C gave an estimated mean-time-to-failure of 6700 hours. These failures are both of the catastrophic open and the resistance increase type. Since these samples have high resistivities, and were glassed, a direct comparison with the chromium-gold binary system is difficult. However, it appears that there is a significant improvement in the lifetime over the chromium-gold system, although the mechanism of failure is similar.

Titanium-Gold

The titanium-gold metallization results have been promising at current levels greater than $2x10^6 A/cm^2$. A study of the titanium-gold metallization system and its thermal stability was presented previously. This revealed a potential failure mechanism for the titanium-gold system as a resistance increase, followed by a burnout in a localized area. This failure mode appears similar to that seen in about 500 hours with the chromium-gold system and about 7000 hours with the molybdenum-gold system.

TABLE 23.- CHROMIUM-GOLD HIGH CURRENT TEST DATA

Sample	Resistivity (micro-ohm-cm)	$J \times 10^6$	$T(^oC)$	Fraction Failed	Total Test (Hrs.)	50% MTF
2-9	4.3	1.0	180	2/10	71,240	2,400
2-4	8.1	0.99	186	2/10	77,885	2,900
2-3-2	10.9	1.02	219	7/7	3,407	430
1-3-2	10.9	1.56	153	6.6	6-1/2	1
3-6	4.3	2.0	186	10/10	42,080	3,850
3-8	7.2	1.94	220	10/10	7,702	700
2-10	8.1	1.9	228	10/10	7,509	700
2-3-1	10.9	1.9	243	9/9	17-3/4	1.8
1-3-1	10.9	2.9	186	9/9	13-3/4	1.7 MFTI
3-9	7.2	3.2	285	5/5	12	2.1

The titanium-gold data is given in Table 24. There appears to be a strong dependence on initial resistivity, and therefore on the titanium thickness. Films with approximately 6.5 micro-ohm-cm resistivity are characterized by about 1000Å of titanium and good high current performance. Lifetimes of 19,000 hours at $1x10^5$ A/cm^2 and 7,500 hours at $2x10^6$ A/cm^2 are indicated. At higher current densities, the lifetimes are greatly reduced. The distribution of the failure times are shown in figure 20. From these results, the titanium-gold system on SiO_2 continues to show promise as a low temperature system, if the titanium thickness is less than 1000Å. However, these thin titanium layers are inadequate to prevent alloying of the gold with exposed silicon, if elevated temperatures (>370°C) are involved. This limitation of the titanium-gold system was discussed earlier.

TABLE 24.- TITANIUM-GOLD HIGH CURRENT TEST DATA

Sample	Resistivity (micro-ohm-cm)	J x 10^6	T(°C)	Fraction Failed	Total Test (Hrs.)	50% MTF
1-5	6.5	0.98	179	4/10	91,300	20,000
1-4-2	8.5	1.56	153	4/7	20,240	5,300
2-4-2	8.5	1.58	176	9/9	7,650	760
1-10	6.5	1.88	193	8/10	68,680	7,800
1-4-1	8.5	2.9	186	10/10	19	1.7
2-4-1	8.5	2.91	243	10/10	21-1/2	2.0

Titanium-Platinum-Gold

The initial thermal and high current density tests of the titanium-platinum-gold films have indicated a need to study the thickness effects in this system more completely. A sample of etched titanium-platinum (3500Å) was coated with evaporated gold to a total thickness of 8000Å. The titanium thickness was estimated to be 2000Å. Initially, the resistivity was 4.4 micro-ohm-cm. However, after gold backing and mounting, and encapsulation, the resistance had risen such that the resistivity was 4.8 micro-ohm-cm. In order to gather information, titanium-platinum-gold samples were placed on test at current densities even higher than normal. Also samples were sputter-etched from a film of 3500Å titanium-platinum, with a gold layer of 2,220Å. The initial resistivity was 6 micro-ohm-cm, but after processing and encapsulation, the resistivity had risen to 8.9 micro-ohm-cm. The ambient temperature for these high current tests was 125°C. The results are shown in Table 25. The $1.8x10^6$ A/cm^2 and higher current density samples showed primarily a resistance rise prior to failure.

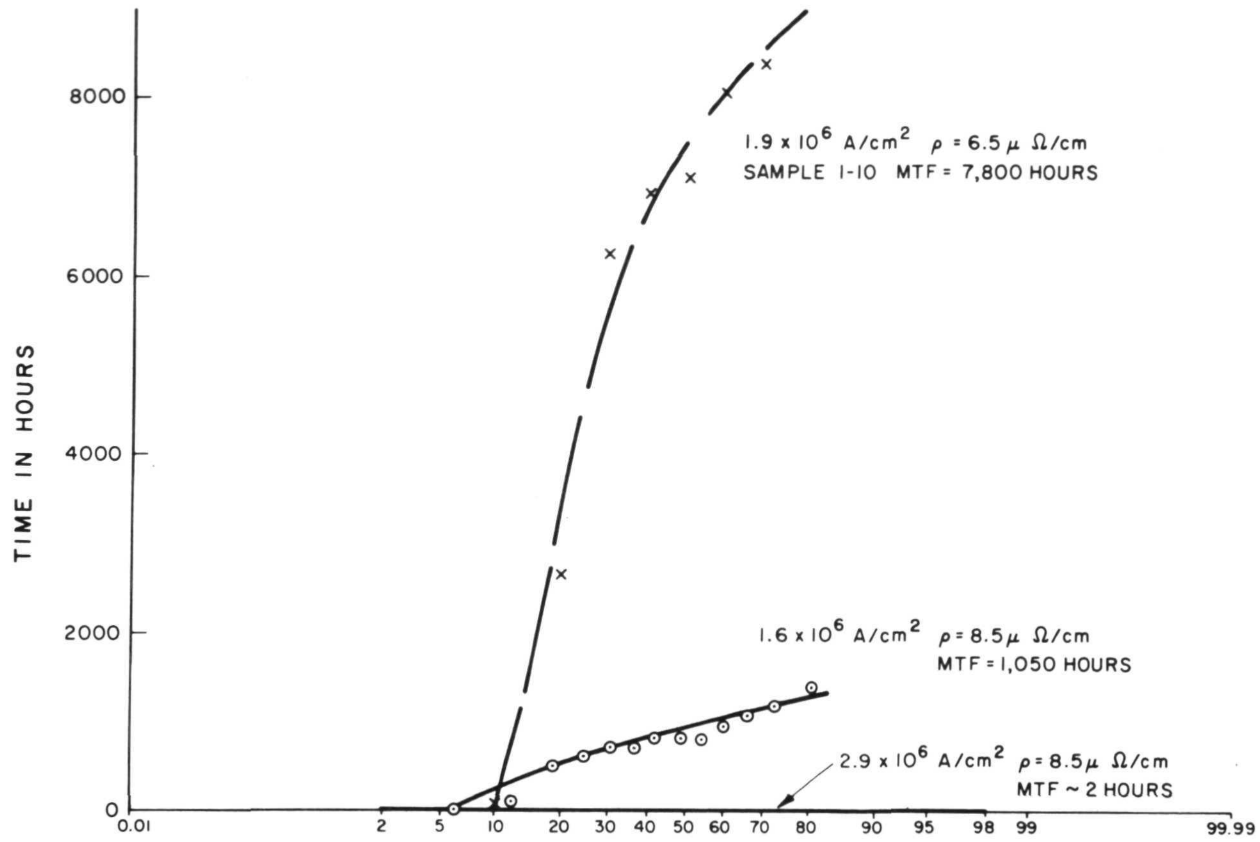


Figure 20.- Distribution Plot of Titanium-Gold Failures at 175°C Ti-Pt-Au Total Thickness (9000Å) Normalized Resistance as a Function of Time on Test at 3.5 x 10^6 cm^2 and 225°C

TABLE 25.- TITANIUM-PLATINUM-GOLD HIGH CURRENT DATA

Sample	Resis-tivity (micro-ohm-cm)	J x 10^6 A/cm^2	T(°C)	Fraction Failed	Total Test Hours	50% MTF Hours
4-3	8.9	0.9	170	3/8	17,606	4,600
4-4	8.9	1.8	190	6/10	16,314	2,400
4-5	8.9	2.4	271	6/7	3,710	550
4-2	4.8	3.5	225	10/10	494	45
4-1	4.8	6.3	625	10/10	-	1/2

The high current results are in agreement with the thermal studies. Figure 21 shows the resistance increase as a function of time for a typical sample at 3.5 x 10^6 A/cm^2 and 225°C. This

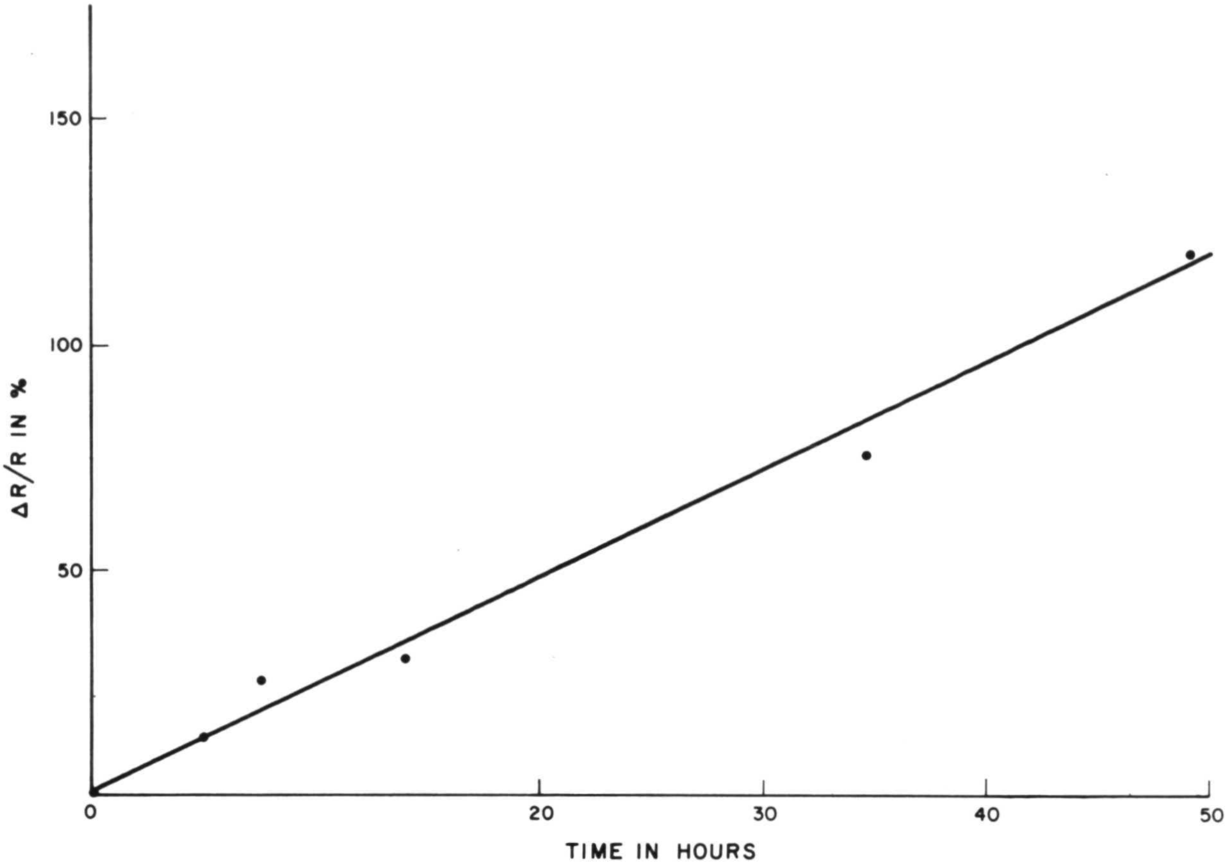


Figure 21.- Ti-Pt-Au Total Thickness (9000Å) Normalized Resistance as a Function of Time on Test at $3.5 \times 10^6 A/cm^2$ and 225°C

film consisted of about 3500Å of titanium-platinum and 4500Å of gold. The adjacent 1-mil conductor (no current) showed no significant change in resistance. In a $6.3 \times 10^6 A/cm^2$ test, where the film temperature was 500°C, the adjacent conductor (no current) showed a 4.5 percent increase in resistance, although the test was less than 1/2 hour in duration. Examination of the ohmic failure at 3.5×10^6 A/cm^2 showed a very roughened surface. The edge around the gold pattern is the titanium-platinum layer, which was left slightly wider than the evaporated gold. This sample showed an ohmic increase as would be predicted by the 450°C thermal tests.

Although these tests were not as complete as those of the other metallizations, they indicate a resistance mode of failure may be induced in Ti-Pt-Au at elevated temperatures and/or high current densities.

TABLE 26.- MOLYBDENUM-GOLD HIGH CURRENT TEST DATA

Sample	Resistivity (Micro-ohm-cm)	J x 10^6	T(^oC)	Fraction Failed	Total Test (Hrs.)	50% MTF
1-1	3.3	1.02	178	9/9	64,830	6,400
1-2	4.1	0.96	180	9/10	69,770	7,200
1-3	4.3	1.0	180	10/10	57,646	5,300
1-4	5.1	0.98	181	10/10	71,675	6,700
1-5-2	4.3	1.57	128	3/10	16,501	4,350
1-6	3.3	2.02	187	7/10	74,545	9,400
1-7	4.1	1.88	192	7/10	72,270	9,200
1-8	4.3	1.92	196	9/10	52,653	5,250
1-9	5.1	1.88	196	6/10	63,197	9,500
3-7	5.1	2.0	191	10/10	41,534	3,850
1-6-2	4.3	2.06	144	4/10	5,124	1,080
2-9-2	6.8	1.96	247	9/9	2,519	250 Glassed
1-5-1	4.3	3.03	150	10/10	19-3/4	1.8 MFTI
2-9-1	4.3	3.5	300	10/10	12-1/2	1.2 Glass
2-3	5.1	3.75	241	10/10	4,795	445
1-6-1	4.3	3.92	184	6/6	6-1/2	0.95
3-4	9.4	1.75	243	10/10	3,330	310 Sputter
3-5	7.2	2.06	202	6/10	63,839	9,600 Sputter
3-3	10.4	2.0	309	2/2	26	9,600 Sputter
2-1	7.2	3.65	297	10/10	789	71
1-10-2	6.8	1.89	184	10/10	4,463	415 Glassed
2-5-2	4.3	1.58	176	0/9	22,500	7,320
-8-2	4.3	1.98	220	4/4	3,820	810

Molybdenum-Gold

Considerable data on the molybdenum-gold system is shown in Table 26. This metallization appears to be the most promising to date. The results show that good reliability is obtained at 175°C ambient temperature and current levels up to 2 x 10^6 A/cm^2. At higher current levels, the lifetime is higher than for the other metallizations. The glassing does not appear to significantly increase the lifetime on the high current tests. The failure mechanism appears in the long life samples as a resistance increase. Opens have occurred within the first 200 or so hours of operation of samples at low temperatures (185°C), and low current densities. At higher temperatures (>185°C), the characteristic failure mode is characterized by a doubling of resistance in about 7,000 hours. Analysis of the five long life groups gives a sample of 50, with 2 opens occurring at 28 and 200 hours. The rest of the failures have been ohmic (resistance doubling). The distribution of these failures is shown in figure 22. A typical resistance failure is shown in figure 23.

Each sample consisted of a chip mounted in a TO-5 can with both a 1/2 and a 1 mil wide conducting strip wired to the pins. The first tests were on the 1/2 mil lines. Following the failure of the 1/2 mil conductor, the resistance of the 1 mil conductor was verified. Following the verification of the 1 mil lines, the samples are often returned to the test sockets, using the 1 mil conductor. The applied voltage and external load resistors were the same as used for the 1/2 mil test, so the current through each test conductor was about the same as before, but the current density is about half the first test value. The load resistors were generally at least ten times the resistance of the test conductor, to minimize the current density variation due to sample resistance changes. Each test was started after a 24-hour preheat before applying current to the samples. The current was increased slowly over a several minute period to the desired value.

One sample of evaporated molybdenum-gold in the tests at 150°C oven temperature showed an early increase in resistance. This molybdenum-gold conductor, 1 mil wide x 54 mil long initially showed a higher than normal resistance (7.35 ohms vs 5.91 ohms). This sample showed an increasing resistance during the early portion of the test, and doubled its resistance in about 28 hours. The other eight samples of this group did not show this change. However, the average temperature for the group was 247°C, while this particular device operated initially at 260°C, due to its higher resistance. As the resistance increases, the current falls slightly, and the temperature rises. The resistance and the calculated temperatures of this sample during the first 60 hours of

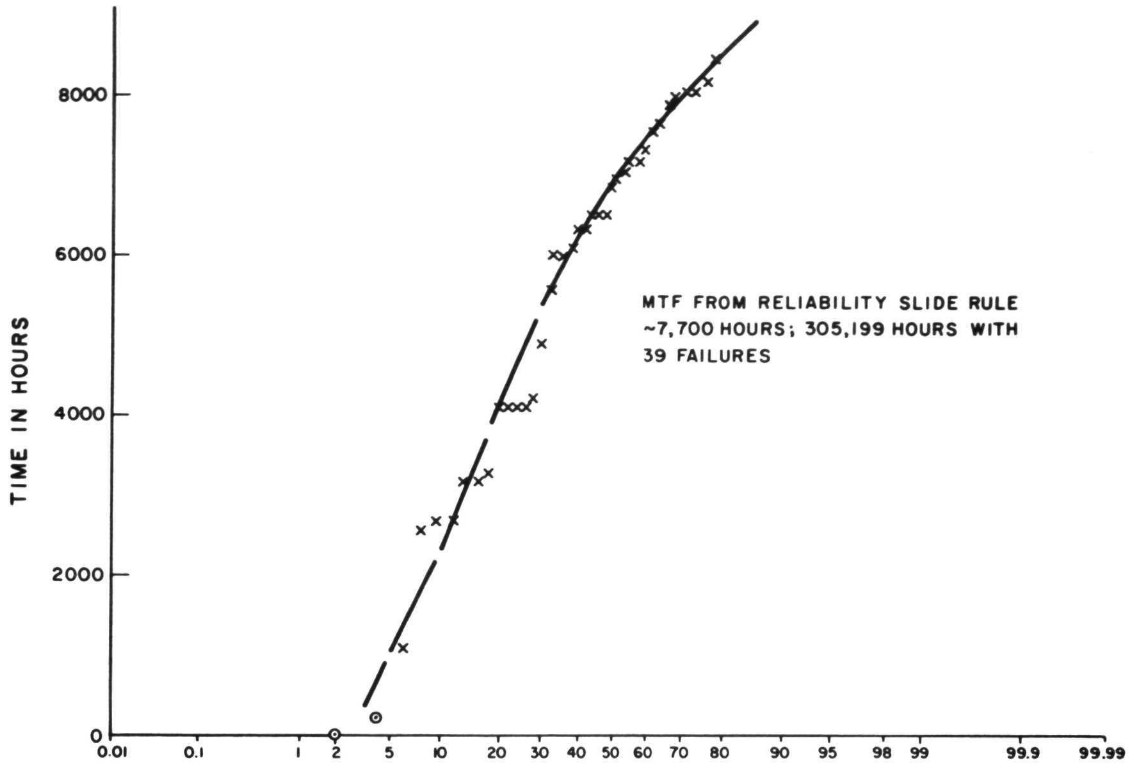


Figure 22.- Distribution Plot of Molybdenum-Gold Failures at 175°C and 2 x 10^6 A/cm^2

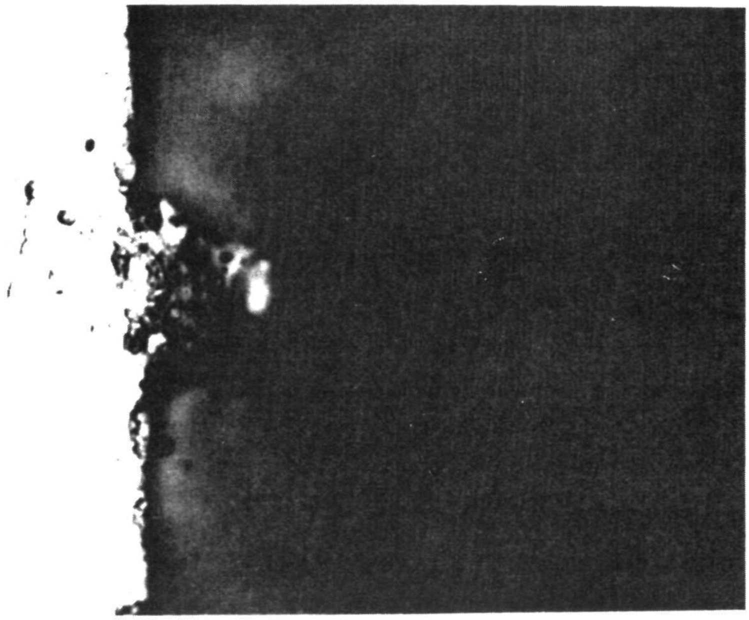


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Figure 23.- Molybdenum-Gold Failure at 2 x 10^6 A/cm^2
No. 1-86 Initial Resistance = 21.2 Ohms, Resistance at 4200 Hours = 96 Ohms

test are shown in figure 24. When this device was opened for inspection, it was discovered that the die was bonded poorly to the header, which would reduce the thermal transfer to the header, raising the sample temperature considerably above the estimated values based on a good thermal transfer. The 1/2 mil strip showed a normal gold burnout failure occurring under the silicate glass (figure 25). The 1 mil strip showed a large area of missing or spotty gold under the cracked glass. Some of the

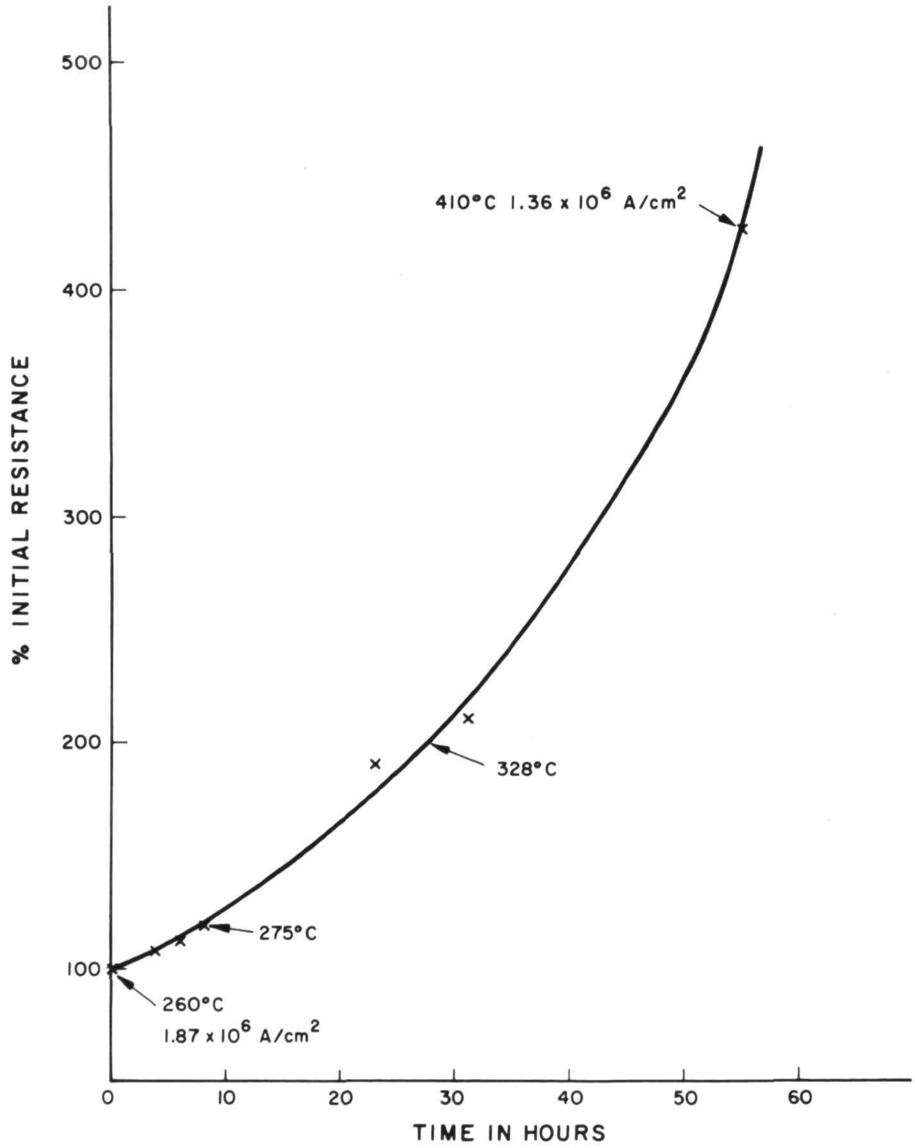


Figure 24.- DC Resistance of Moly-Gold 1-mil Strip (#2-81) as a Function of Time at 1.96×10^6 A/cm^2 - Estimated Film Temperature 247^{O}C (average)

gold appeared as raised areas above the intact molybdenum film. This failure is therefore attributed to a higher than normal operating temperature caused by the high initial resistance and a poor die bond to the header. This elevated temperature caused a premature failure of the 1 mil conductor with a doubling of resistance in 28 hours (figure 26).

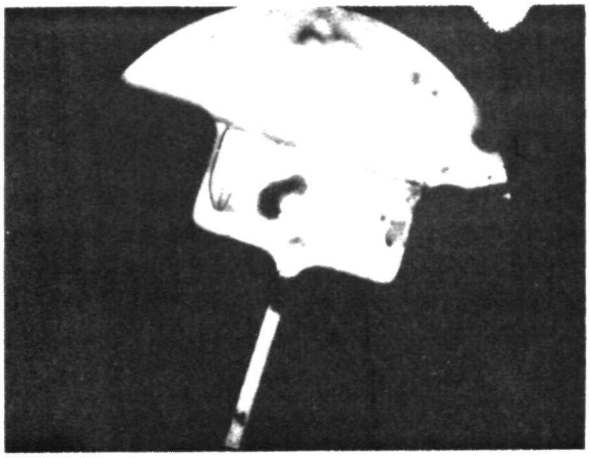


Figure 25.- 1/2-Mil Conductor Failure Sample 2-81 Failed <5 Minutes at $3.5 \times 10^6 A/cm^2$

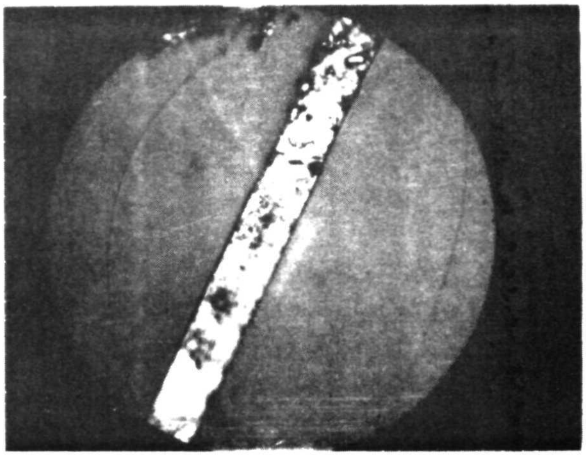


Figure 26.- 1-Mil Conductor Failure Sample 2-81 Initial Resistance 7.35 Ohms, failed 28 hours at 1.9×10^6 A/cm^2

Two failure modes have been indicated. The failures which occur early in life or at elevated current levels are a catastrophic burnout failure, with no resistance rise prior to failure. The samples not carrying current and at 175°C have not shown any measurable resistance increase in over 10,000 hours of test. However, samples at 2×10^6 A/cm^2 and 175°C ambient have shown a failure mode characterized by a doubling of resistance in about 7,000 hours.

The increased resistance leads to higher dissipation and ultimate failure from localized high temperature areas. The sample at 1×10^6 A/cm^2 showed only a slightly longer life than the 2×10^6 A/cm^2 group. The distributions of the failure times are shown in figure 27. The 10^6 A/cm^2 group had a large number of failures at about 7,200 hours, with a few earlier failures. Examination of the 7,250 hour failures showed an extensive and very uniform loss of the conductors. The appearance and distribution of the failures was suggestive of a wear-out mechanism, occurring uniformly at about 7,200 hours. A typical failure is shown in figure 28.

This mechanism is the formation of an intermetallic material with a high resistivity, leading to catastrophic failure over a

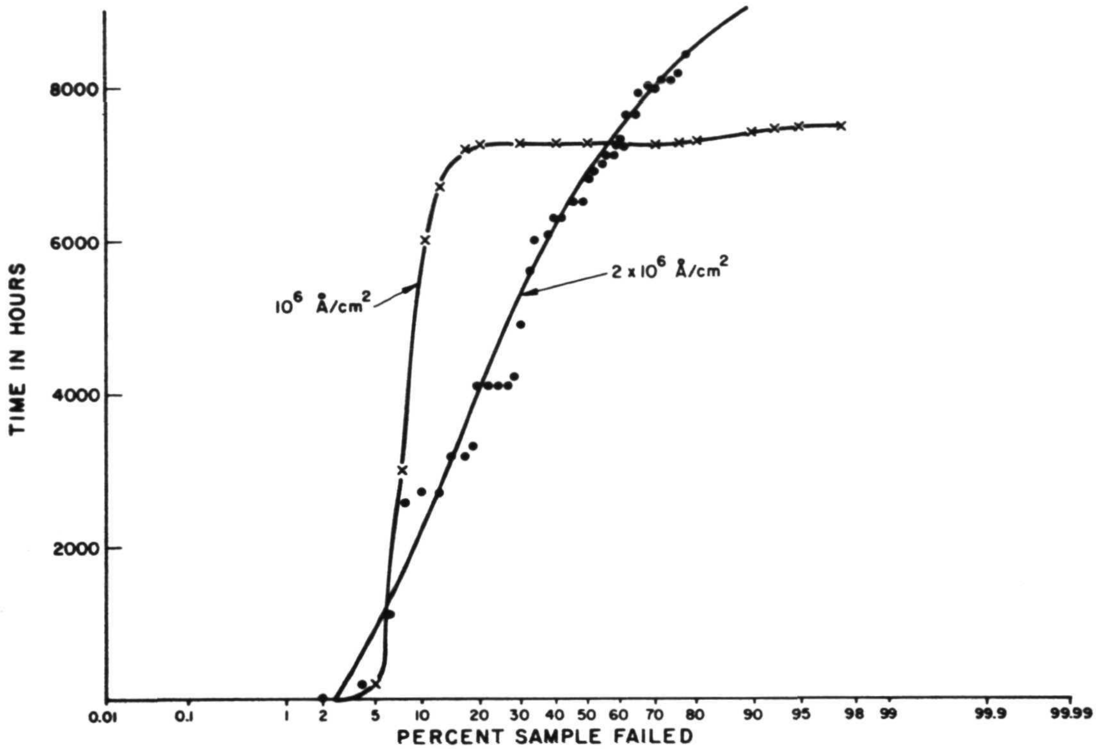
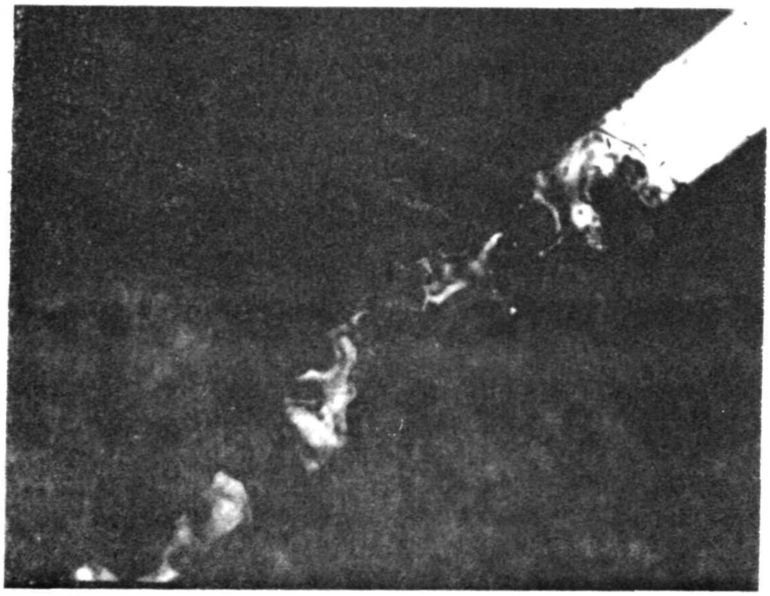


Figure 27.- Distribution Plot of Molybdenum-Gold Failures at 175^{o}C and 1 or 2 x 10^6 Å/cm^2



(1040X)

Figure 28.- Sample 1-15. Molybdenum-Gold Failure ~7000 hours 175^{o}C 1 x 10^6 A/cm^2

short period of time. The estimated temperature coefficient for this reaction is about 1.8 eV, in agreement with the gold self-diffusion value. The lack of any detectable resistance rise in conductors adjacent to the test conductor indicated that little or no reaction occurs at 175°C in the absence of the current flow. At high current levels, this reaction mechanism leads to failure at somewhat shorter times, although these tests have indicated that at 2×10^6 A/cm^2, the molybdenum-gold system has the longest life of the systems tested.

Summary of Current Density Tests

The lifetimes of Al films at $J = 10^6$, $s \times 10^6$ A/cm^2 and 175°C are 780 and 20 hours, respectively. These values are similar to the results reported by Blech, et al (ref. 25), and to the results obtained by Black (ref. 3) on small-to-medium crystallite size aluminum films.

The aluminum failures occur as a catastrophic opening of the conductor, appearing as either a crack or melted region. No resistance increases were detected prior to failure. Table 27 summarized the results from all tests.

Assuming that the temperature coefficient (or activation energy) of the electron current migration reaction is associated with the self-diffusion energy, the use of gold systems were expected to provide considerable improvement. The activation energy for gold would be about 1.8 eV, which should give a factor of 100 improvement in lifetime over aluminum in the temperature range of the experiments. In practice, a significant improvement is found.

In a previous section the chromium gold-system has been found to have a failure mode involving the formation of a high resistance intermetallic compound. The chromium-gold metallizations underwent a resistance rise during the processing and continued during current tests. The samples doubled in resistance in about 500 hours at 2×10^6 A/cm^2 and 175°C ambient. Although the resistance rise occurred in all samples, including those not carrying current though not necessarily as great; many of the samples continued to conduct for many hours, but with increased power dissipation. Eventually burnout occurred.

The titanium-gold system has properties similar to those of the chromium-gold system. There is a resistance increase in the thermal treatment, and this has also been observed in the high current studies. However, it appears at a much later time, and the mean-time-to-failure at 2×10^6 A/cm^2 and 193°C is approximately 7,500 hours. A sample at 10^6 A/cm^2 and 179°C had an indicated mean-time-to-failure of 19,000 hours. However, the lifetime is sensitive to the resistivity of the sample, and the

TABLE 27.- CURRENT DENSITY TEST RESULTS

	Current Density J 10^6 A/cm^2	Resis-tivity (micro-ohm-cm)	Average Temperature	50% MTF (hours)
Al	1.0	4.7	167°C	780
	2.0	4.4	185°C	19
Cr-Au	1.0	7.8	195°C	13,500
	2.0	7.6	219°C	1,500
Ti-Pt-Au	0.98	6.5	179°C	20,000
	1.88	6.5	193°C	7,800
Mo-Au	1.0	4.2	177°C	6,700
	2.0	4.4	194°C	5,250
Ti-Pt-Au	0.9	8.9	180°C	4,600
	1.8	8.9	190°C	2,500

higher resistivity samples have a reduced lifetime. At 2×10^6 3×10^6 A/cm^2 and 210°C the life was only 1.9 hours.

The Ti-Pt-Au samples were from a lot which had only 2,000 Å gold deposited over 1,500 Å Pt. From the thermal tests discussed in a previous section, this combination of thickness in Au-Pt is expected to exhibit a thermally induced resistance increase. Even though the current density samples were not of optimized thickness, the lifetime was longer than 2,500 hours at 1.8×10^6 A/cm^2.

The extended lifetime of the Au based systems is further exemplified by the data on the MoAu samples. Even at 2×10^6 A/cm^2, the lifetime of the MoAu samples exceeded 6,000 hours.

The current density studies reported here on the Au based systems were not designed to be as intensive as those reported on aluminum (ref. 3). Consequently, the results do not necessarily indicate that Au migration is a predominant failure mode in the metal Au systems tested. The intended result of qualitative comparison in lifetime was accomplished, and shows that the Au based systems are capable of lifetimes of 10 to 100 times longer than aluminum at a very high current density.

MULTILAYER METALLIZATIONS

In the study of metal-dielectric-metal-multilayer films, not only is the behavior of the metal film itself important, but also the adherance of the deposited glass layers and the possible effect of the glass deposition cycle on the metal films themselves. Of considerable significance is the resulting etching characteristic of the glass when opening "via" holes down to the underlying conductor patterns.

A preliminary evaluation of multilayer processing with various metallizations was conducted in a series of tests to determine the compatibility of each metallization with specific glass processing steps.

The control for the thermal tests of multilayer systems consisted of six aluminum metallizations that were combined with six glass combinations. The glasses were as follows:

(1) 6000 Å sputtered quartz
(2) 500 Å sputtered quartz plus 6000-8000 Å pyrolytically deposited SiO_2
(3) 500 Å sputtered quartz plus 6000-8000 Å low temperature hydrolyzed $SiCl_4$ glass
(4) 6000-8000 Å low temperature hydrolyzed $SiCl_4$ glass
(5) 6000-8000 Å pyrolitically deposited SiO_2
(6) 500 Å low temperature hydrolyzed $SiCl_4$ glass plus 6000-8000 Å pyrolitically deposited SiO_2

Most of the aluminum metallizations showed some deterioration at least after 18 hours at 450°C. The aluminum metallizations that showed little change unprotected were compatible with all glasses and combinations. These were the ultra-high vacuum metal deposition with a high substrate temperature, and an aluminum-silicon metallization. The normal tungsten filament evaporated aluminum and the low temperature substrate deposition from a BN boat were generally poor, although the glasses showed some protective action. There appeared to be little advantage to combining the sputtered quartz and the low temperature glass. However, the thin sputtered quartz had a beneficial effect when the high temperature glass was applied. The sputtered quartz single layer also had a beneficial effect. The SiO_2 with its high (425°C) deposition temperature was unsatisfactory on these "poor metallizations". The combination of thin low temperature glass followed by the SiO_2 had little advantage over the single SiO_2 layer. Two aluminum metallizations which would othersie show thermal deterioration, showed promise when used with glass over-coatings. These were a tantalum filament evaporated aluminum and the sputtered aluminum. Both of these were compatible with most glass combinations. The sputtered film showed a high resistivity and earlier tests showed cases of severe "nuggeting".

Therefore, the tantalum filament evaporated aluminum was chosen as a reference metallization. This material showed deterioration when unprotected, but was greatly improved by the use of any of the glass combinations. (See figures 29 and 30).

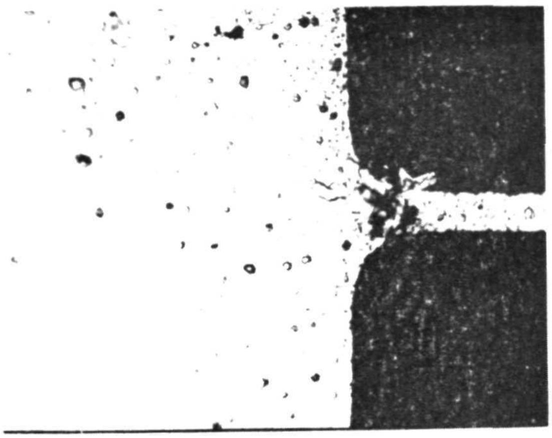


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Figure 29.- Aluminum (Tantalum Filament Evaporation) after 18 Hours at 450°C in Air

(1000X)

Figure 30.- Aluminum (Tantalum Filament Evaporation) and SiO_2 after 18 Hours at 450°C in Air

The higher temperature SiO_2 operation caused some mild deterioration of the metallization, which was reduced when an initial thin layer of sputtered quartz or low temperature glass was applied prior to the SiO_2 operation. All the glasses adhered to the aluminum metallizations and no cracking, or loss of glass was noted.

Molybdenum-gold and molybdenum-gold-molybdenum films were prepared using 2000 Å of molybdenum, 4000 Å of gold, and, in some cases, 200 Å of molybdenum as a top layer. The compatibility of the metallization with various glassing processes was checked by depositing a layer of glass over the patterned metallization before the thermal tests. The evaporated molybdenum-gold and molybdenum-gold-molybdenum films, sputtered molybdenum-gold, the referenced metal aluminum and a titanium-gold film were rated for compatibility with the various glasses in Table 28. There were cases of cracked glass and poor adherence, as indicated in the table.

The unprotected films varied in performance. The aluminum showed mild deterioration starting in 1/2 hour at 450°C. The deterioration of the molybdenum-gold films was varied.

TABLE 28.- COMPATIBILITY RATING OF THE VARIOUS METALLIZATIONS AND GLASSING COMBINATIONS

Glass / Metal	None	Sputtered Quartz	Sputtered Quartz + Low Temp Glass	Sputtered Quartz + SiO_2	Low Temp. Glass	SiO_2
Aluminum Evaporated	2-1	3-4	3-4	3-4	2-4	3-4
Evaporated Ti-Au	1-1	2-3*	**	**	2-3*	2-3
Evaporated Mo-Au	3-4	3-4*	**	**	3-3*	3-4
Evaporated Mo-Au-Mo	1-1	**	**	**	2-3	3-4
Sputtered Mo-Au	1-1* 3-4	3-4*	3-4*	1-2*	1-3*	3-4

* Cracked glass and poor adherence
** Sample not available
\+ Thin gold top layer plus thick interface zone

Level-Time Rating

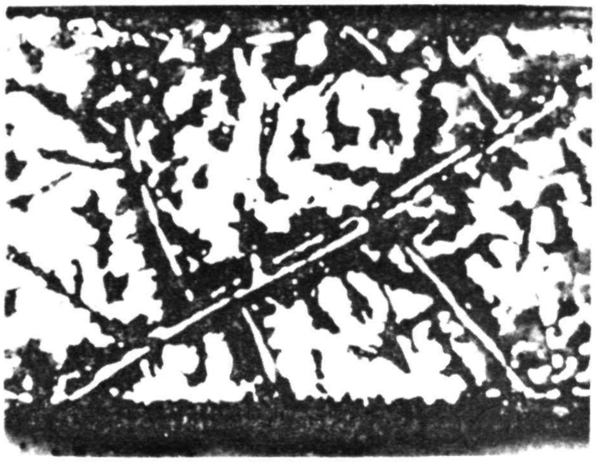
Level 1 = Severe Degradation
2 = Mild Degradation
3 = Little or no Degradation

Time 0 = During Processing
1 = in 1/2 hour at 450°C
2 = in 1 1/2 hours at 450°C
3 = in 18 hours at 450°C
4 = Little or no degradation in 18 hours

Molybdenum-gold-molybdenum films showed a detrimental effect after only 1/2 hour at 450°C. A similar result was observed with molybdenum-gold films in which the top layer was extremely thin (1000 Å) and, also, if a thick interface was used between the molybdenum and gold. It had been shown that at least 2000 Å of molybdenum are necessary to prevent the alloying of the gold to exposed silicon. It had also been noted that there is a dependence of the gold thickness. The use of 1000 Å of gold is necessary for satisfactory wire bonding, and these tests suggest that 6000 Å of gold are needed to prevent deterioration of the metallization on the long high temperature bakes. This could be explained by the assumption that oxygen is diffusing through the gold layer, reacting with the molybdenum film and promoting the deterioration observed. The use of the heavier gold film presents no difficulties.

Molybdenum films showed good stability after 18 hours baking at 450°C in air. These films were not protected by a glass overcoat and were deposited by sputtering onto a thermally oxidized substrate. Dark edges are observed along the molybdenum-gold films due to oxidation of the molybdenum out from beneath the top gold layer, a frequently observed mode of deterioration unless a glass passivation overcoat is used. If the top gold is thin and a heavy interface is used, the deterioration becomes quite severe even though a glass passivation is used. (See figure 31.)

Cracking of the glass layer was seen with the gold top layers and sputtered quartz, sputtered quartz plus low temperature glass, sputtered quartz plus SiO_2 and the low temperature glass. The only glass adhering to the gold (either evaporated or sputtered) was the SiO_2 (even in this case adherence to larger areas of gold was marginal). The films with the SiO_2 showed little or no deterioration in 18 hours at 450°C. The deterioration noted in the cracked samples originated around the exposed metal area further suggesting that the diffusion of oxygen through the gold or glass is a probable mechanism.



(1520X)

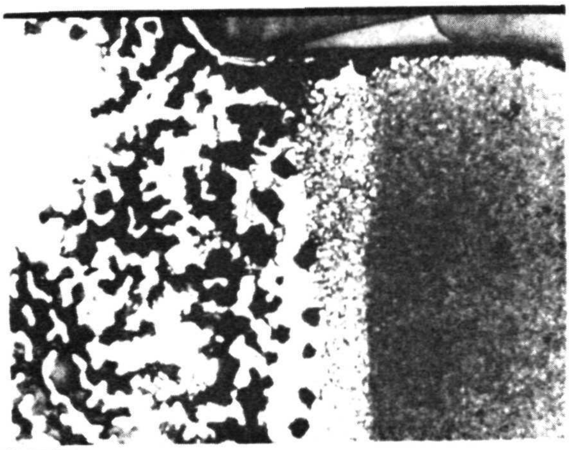
Figure 31.- Sputtered molybdenum-Gold Film and Low Temperature Glass After 18 Hours at 450°C in Air (Thin Gold Layer)

The above action is not surprising. Gold when deposited upon glass substrates does not adhere well, and glass deposited upon gold should behave similarly. The adhesion in this case will be enhanced by the surface roughness or texture of the gold film. The SiO_2 adhesion, however, is improved because this passivation is deposited by vapor or gas plating. In this method, corrosive constituents are reacted at an elevated temperature at the surface of the substrate. No doubt a certain amount of reaction between the gold and one or more materials in the vapors does occur before the actual glass layers start to form, resulting in an improved metal-to-glass bond.

The molybdenum-gold-molybdenum film showed interesting properties. If the film is heated at 450°C with the top molybdenum layer exposed to air, the sample deteriorates as expected. This deterioration carries through to the intermediate gold layer. If the top molybdenum film is removed before the baking, the results

Note: The term SiO_2 refers to gas vapor deposited material.

are similar to those with the two-layer metallization. The glass adherence of both the low temperature glass and the SiO_2 to the three-layer metallization was excellent, which justifies the additional molybdenum layer. There was no visible deterioration under the low temperature glass at 1 1/2 hours, but after 18 hours at 450°C there appeared a mild deterioration similar to that occurring in the exposed areas. The sample passivated with SiO_2 showed no deterioration under the glass (see figure 32) during the 18 hour test. The severe deterioration in the exposed pad occurred between 6 and 18 hours at 450°C in air. This sample had a molybdenum thickness of about 2000 Å and a gold layer of about 3000 Å. Samples with 6000 Å of gold did not show this deterioration even after 18 hours.



Etched Pad Area to Left, Glassed Area to Right

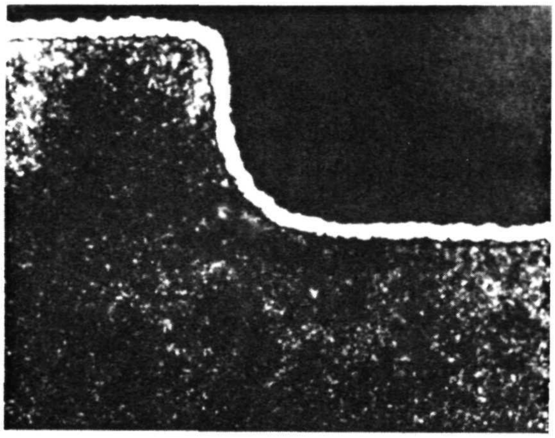
(1520X)

Figure 32.- Evaporated Molybdenum-Gold-Molybdenum Film and SiO_2 after 18 Hours at 450°C in Air

The bulk resistivity of the samples was individually checked during the test, when the chip was of adequate size for convenient probing. The aluminum film had a resistivity of 3.0 micro-ohm-cm throughout the test. The evaporated molybdenum-gold films had resistivities of 7.7 and 8.0 micro-ohm-cm. Again, little change was seen during the thermal tests. The molybdenum-gold-molybdenum film had an initial resistivity of 9.3 micro-ohm-cm to be compared with the 8.9 micro-ohm-cm for the two-layer metallization. Again, little change was seen during the baking. The sputtered molybdenum gold showed an apparent resistivity of 21.7 micro-ohm-cm (because of a thin gold layer) with no change in resistivity during the baking.

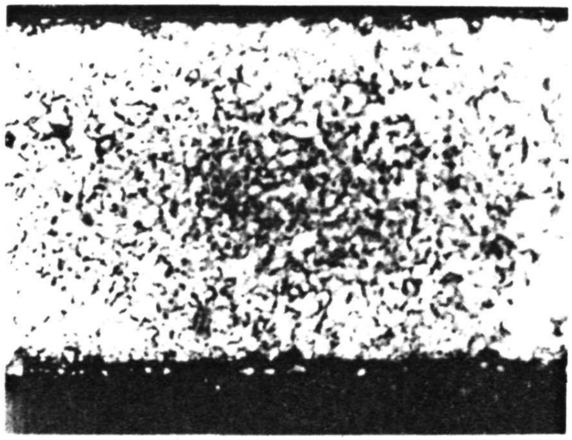
Titanium-gold films of 1000 Å of electron beam evaporated titanium and evaporated gold to a total thickness of 4000-5000 Å were included in the glass compatibility study. The unprotected film deteriorated rapidly and completely in the air bake at 450°C. The edges of the film showed little or no deterioration. The edge was apparently an intact gold film which was undercut during the titanium etch (see figure 33).

Both the sputtered quartz and the low temperature glass showed cracking on this metallization, with severe deterioration of the exposed metal, and mild deterioration of the protected areas. The SiO_2 film did not crack and the protected metal showed little or no deterioration in three hours and mild deterioration in 18 hours (see figure 34).



(1520X)

Figure 33.- Titanium-Gold Film after 18 Hours at 450°C in Air



(1520X)

Figure 34.- Titanium-Gold Film and SiO_2 after 18 Hours at 450°C in Air

The titanium-gold film had an initial resistivity of 3.4 micro-ohm-cm with no significant increase on baking. This is surprising, in view of the obvious visible deterioration of the film in many cases. However, the average measured resistance of the 1/2 mil x 54 mil line before glassing was 18.8 micro-ohm-cm and, after glassing and baking, 1 1/2 hours at 450°C, the value was 19.2 micro-ohm-cm.

MULTILAYER TEST VEHICLES

A section of the miltilayer test vehicle used in this work is shown in figure 35. Cross section photomicrographs taken with normal right-angle cross-sectioning shows little detail in

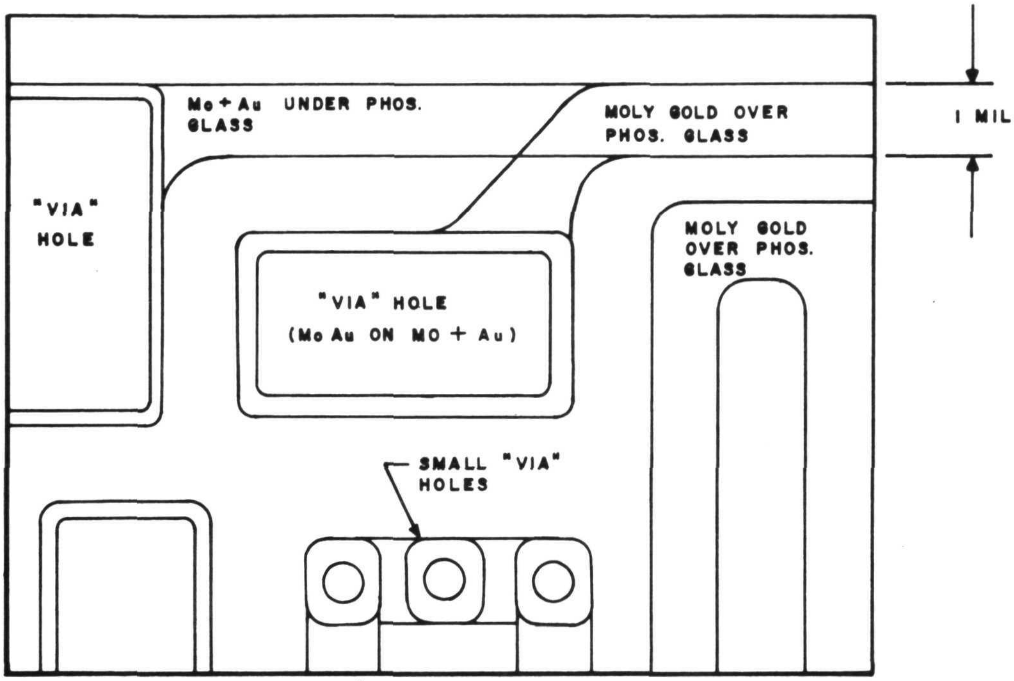
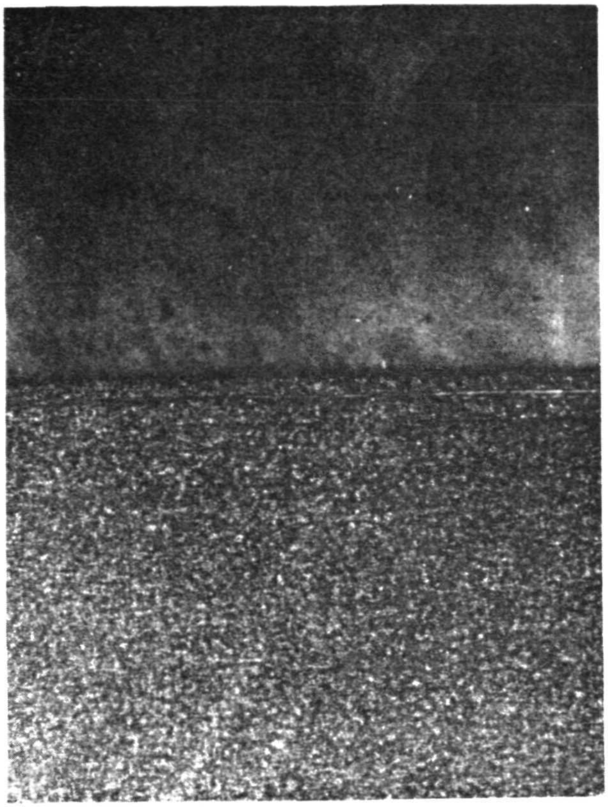


Figure 35.- Multilayer Structure

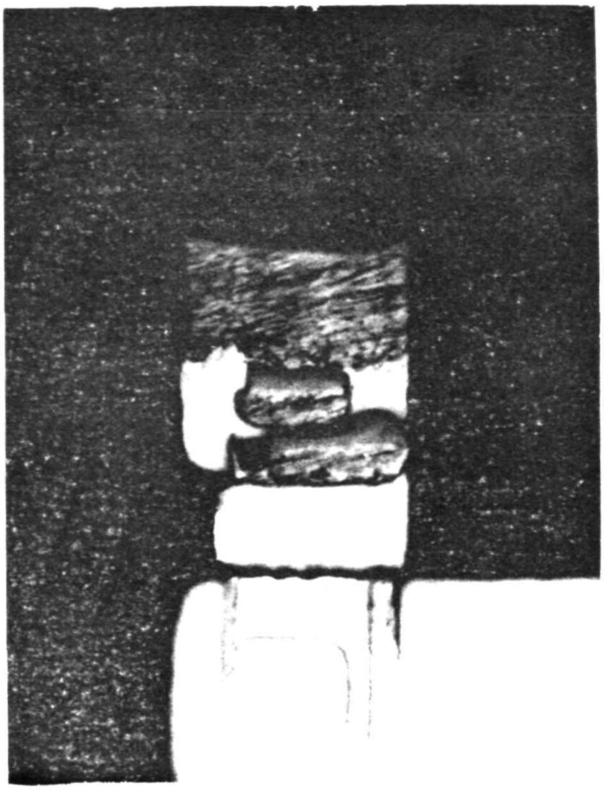
the multilayer structure. An example is shown in figure 36. By cross-sectioning at approximately 5^{o}, a ten-fold expansion of the metallization is obtained. An example of this technique is shown in figure 37. This is an angle cross-section taken at 1200X of the multilayer vehicle, cutting through a small "via" hole. In this example, the bottom molybdenum was 1000 Å, with 1500 Å of vacuum-deposited gold. An additional 2500 Å of gold was vacuum-deposited onto this layer before patterning. A layer of 6000 Å of silicate glass was deposited over the patterned bottom layer, and the "via" holes etched in the glass layer. A second metallization of molybdenum-gold is deposited, followed by a top silicate glass layer. This is shown schematically in figure 38. The thin molybdenum layer on the top of the bottom gold layer is sometimes omitted. It serves as an indicator for judging the etching of the "via" holes and improves the glass adherence when used. Another angle cross section is shown in figure 39.

This multilayer vehicle using molybdenum-gold-molybdenum-glass-molybdenum-gold-glass layers was subjected to the 450°C air



1500X

Figure 36.- Normal Cross Section of Multilayer Molybdenum-Gold-Glass-Molybdenum-Gold-Glass



1200X

Figure 37.- 5° Angle Cross Section of Multilayer Molybdenum-Gold-Glass Molybdenum-Gold

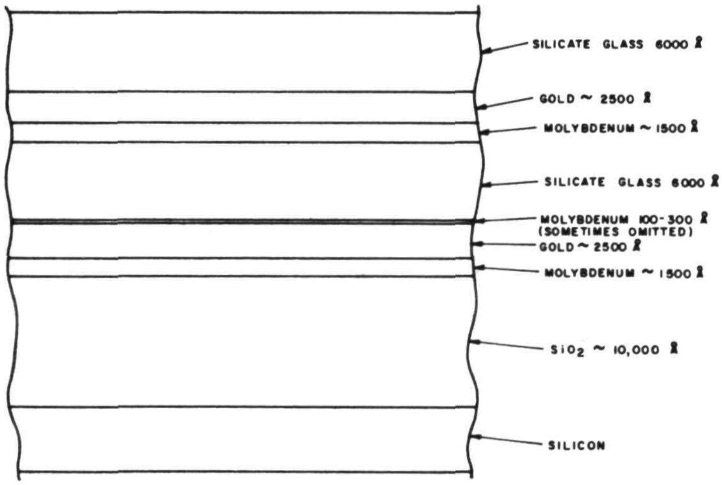


Figure 38.- Schematic Representation of of Molybdenum-Gold Multilayer Test Vehicle

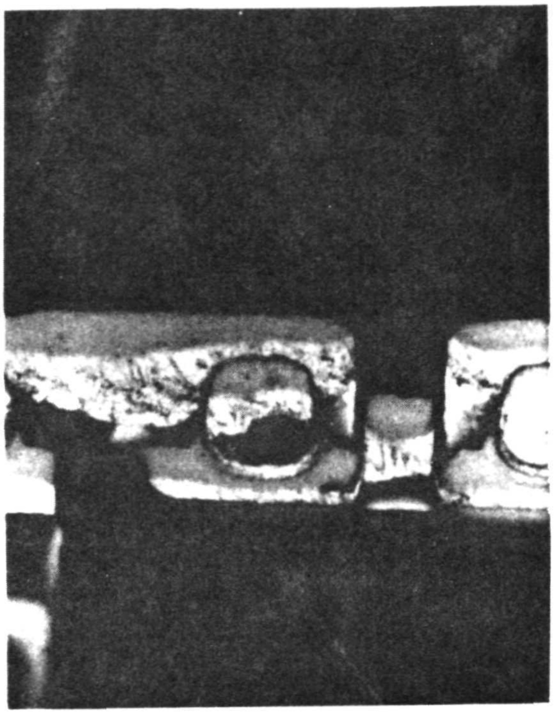
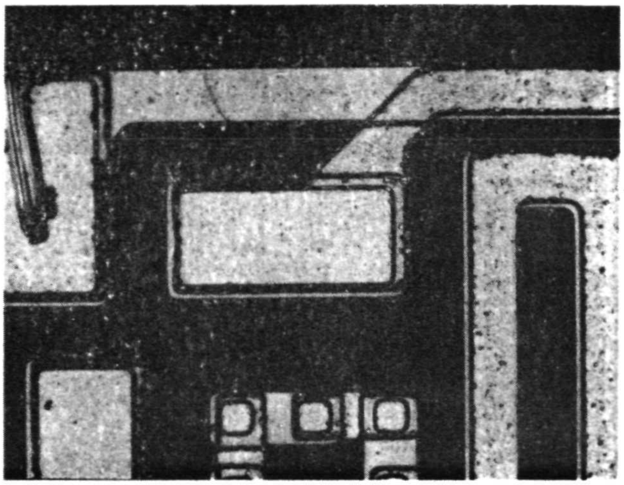


Figure 39.- 5° Angle Cross Section of Multilayer Molybdenum-Gold-Molybdenum-Glass-Molybdenum-Gold-Glass

bake for 12 hours with no physical deterioration seen in any layers or areas. No significant resistance changes were seen in the conductor strips, and the contact through the "via" holes between the alternate conductors was found to have negligible resistance. The series resistance through the 200 "via" holes was 8 ohms, which was nearly the value of a solid conductor of the same length. The voltage breakdown between the isolated metal layers was greater than 400 volts.

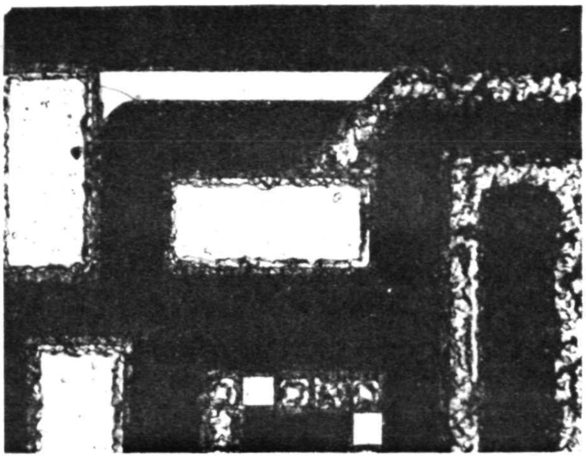
Two additional photographs (figures 40 and 41) show the stability of a molybdenum-gold-SiO_2-glass-molybdenum-gold multilayer structure after 450°C air baking. The various components in this structure were shown in the diagram of figure 35. The photographs show that little or no deterioration has taken place at one hour at 450°C; however, after 18 hours, the top layer of molybdenum-gold that has the SiO_2 as a substrate has undergone severe deterioration. The large "via" holes are degraded completely, undoubtedly because the SiO_2 edge closely surrounds the molybdenum-gold in the "via" hole. It is important to note that the bottom layer of the molybdenum-gold deposited upon thermal oxide and covered with SiO_2 has not deteriorated during baking.

In other parameters these multilayer structures are satisfactory, as they show very low contact resistances between the layers and few if any shorts between the layers.



(375X)

Figure 40.- Molybdenum-Gold-SiO_2-Glass-Molybdenum-Gold Multilayers after 1 Hour at 450°C in Air

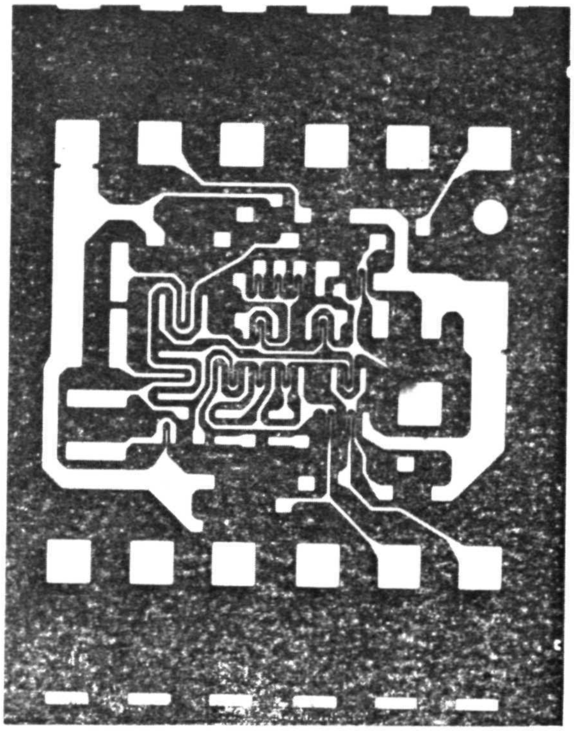


(375X)

Figure 41.- Molybdenum-Gold Multilayer SiO_2 Structure After 18 Hours at 450°C in Air

FINE LINE PATTERNING

Of no small consideration are the difficulties encountered in patterning single layer or multilevel metallization on silicon integrated circuits. The conductors considered so far involved the etching techniques suitable for patterning lines 9.5 mil (12.5 microns) or larger. A typical metal pattern chosen has lines 1,2,4 and 5 microns wide and with spaces of 3 microns or greater and is shown in figure 42. The die dimension is about 20 mils.



125X

Figure 42.- Interconnect Metal Mask

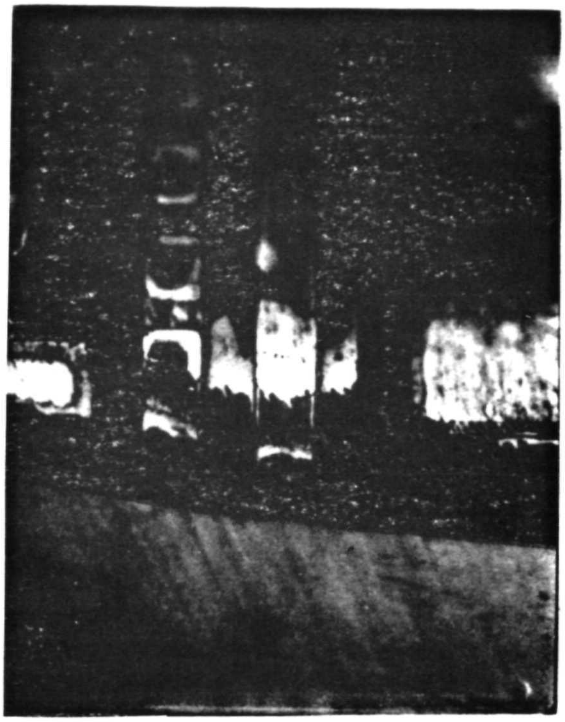
The first attempt to etch this pattern in conventional aluminum metallization (6000 Å of evaporated metal) showed that with the normal KMER* photoresist techniques the center portion of the pattern could not be defined. The pattern was not resolved in the developed photoresist, and therefore, was not reproduced in the etched metal. Exposure and development variations were not successful. However, when a change in the resist was made, decreasing the film thickness by dilution of the resist, and other modifications, the pattern was faithfully reproduced in the development resist pattern. Using this modified resist, it was possible to pattern the aluminum interconnect metal. The fine-line pattern has been reproduced consistently in aluminum, and chromium-aluminum films up to 6000 Å thick, in chromium-gold, titanium-gold, molybdenum-gold-molybdenum, and chromium-copper films of 6000 Å total thickness and in chromium films <1000 Å thick. Although it is difficult to evaluate the ease of etching each metallization on the basis of a limited number of samples, the chromium-gold system appeared the most difficult to pattern successfully, with titanium-gold next in difficulty. The aluminum-chromium, and molybdenum-gold films were patterned with little difficulty. However, in the molybdenum-gold films, those that were sputtered generally gave more problems than those that were evaporated. Even in the most difficult cases, the 3 micron lines were always retained. Many of the 1 micron lines were etched successfully, but were lost in subsequent cleaning and removal of the resist. The problem is minimized by substitution of a gentle TCE rinse for the normal TCE spray cleaning.

The normal photoresist retains the exposed portions, and the unexposed area is removed in the development. In some processes, it is convenient to use the Shipley AZ 1350 Resist, in which the exposed portion is removed by the development step. Using Shipley AZ 1350 Resist the fine-line pattern has been consistently reproduced.

With the increased complexity and fine-line geometry of the test patterns being used, the difficulties of consistently patterning a complex metallization became more apparent. Specifically, the use of the present multilayer test pattern has disclosed photoresist problems. The difficulty, generally, is seen with the use of a vigorous etching solution, usually heated, and appears in the form of lifting photoresist toward the end of the etching process. While no definite conclusions have been possible, several tendencies have been noted. First, the final bake time and temperature are critical for these complex patterns. Inadequate postbake, after development, commonly causes poor adherence. There has also been a tendency for more adherence problems with the molybdenum top coated metallizations, especially where the molybdenum is thicker than a few hundred angstroms. This problem is probably due to the undercutting of the resist during the etching of the thicker bottom molybdenum layer. However, the use of controlled etching conditions has, to a large degree, eliminated any serious problems. A common cause of difficulty is the use of molybdenum etch at too low a temperature, resulting in an excessive etching time. The etching step for the bottom 2000 Å of molybdenum should not be much greater than 15 seconds, and never longer than 30 seconds. After etching, a rapid and complete rinsing in deionized water is necessary. With an adequate postbake (30 minutes at 180°C for the resist used in this experiment), there has been little adherence problems. However, it has occasionally proved difficult to completely remove the resist from the water. The use of an acetone rinse, 15 seconds in hot J-100 (photoresist remover), followed by a second acetone rinse, and another 15 seconds in hot J-100 has proven satisfactory in even the most difficult cases. The wafer is then cleaned by an acetone rinse, and TCE sprayed.

Before any further processing, the wafer is rinsed at least 30 minutes in deionized water. Before metallization steps, a 5 second dip in very dilute (40-1) buffered HF etch, followed by a deionized water rinse is performed. This produced wafers which wet evenly when removed from the final water rinse. Any tendency of uneven wetting necessitates additional cleaning before metallization.

Using these procedures, successful multilayer metallizations have been completed. A cross section of one is shown in figure 43. This is taken at 300X after an angle cross section has been polished.



~300X

Figure 43.- 5° Angle Cross Section of Multilayer Molybdenum-Gold-Molybdenum-Glass-Molybdenum-Gold-Glass

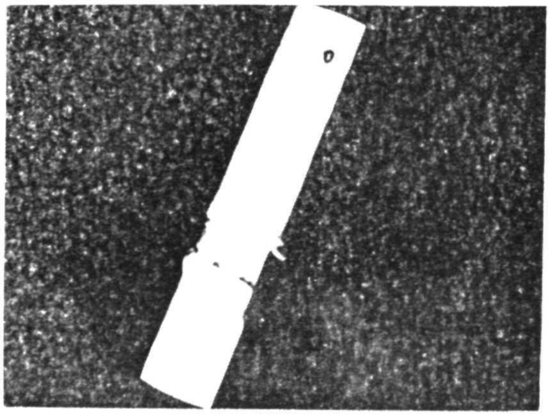
It will be noted that the top gold is the same width as the molybdenum stripe, showing no significant undercutting of the top metallization. The bottom metallization is best shown in figure 44 at 1200X. This shows the bottom molybdenum and the gold layer quite clearly; again there is no evidence of undercutting. The top molybdenum appears as the brown film, smaller in width than the gold. This brown film forms during the glassing operation (425°C-oxidizing atmosphere). Before glassing, microscopic examination showed no exposed gold at the edges of the 1.5 mil strip.

To show that undercutting can indeed occur, figure 45 shows a 400X photomicrograph of a 2 mil line patterned in a molybdenum-gold metallization. Scratching the top gold layer clearly shows the undercut molybdenum layer. When this is observed, it is generally not uniform across the wafer, but appears to be most pronounced in the outer portions of the wafer.

The difficulties encountered are not limited to the molybdenum-gold system, but are characteristic of the processing of all the single and multilayer films. An attempt to etch a 2 mil line in a 3 microns thick aluminum film is shown in figure 46. This resulted when the normal aluminum etching process was used on this "thick" film. It demonstrates the problems of etching a film which is only 1/16 as thick as the width of the patterned line. The etching of these thick films may be avoided in the gold systems by etching only a thin layer, then plating additional gold on the patterned wafer.

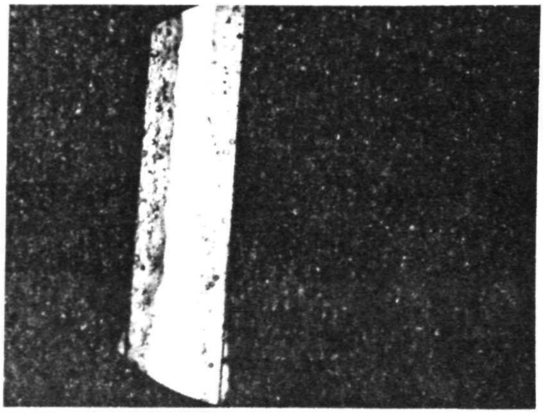
1200X

Figure 44.- 5° Angle Cross Section of Multilayer Molybdenum-Gold-Molybdenum-Glass Molybdenum-Gold-Glass



400X

Figure 45.- Photomicrograph of Scratched Molybdenum-Gold Metallization - Line 2 mils Wide



400X

Figure 46.- Photomicrograph of Poorly Etched 3-micron Aluminum Film - Line 2 mils Wide

SPUTTER ETCHED SEMICONDUCTOR CONTACTS

One of the more recent but well-known techniques of depositing thin films in which high energy (500 eV) ions bombard a target of material is known as sputter deposition. By means of momentum transfer from the bombarding ions, material (atoms) is removed from the source and deposited on the substrate to form a thin film. Sputter etching uses the same technique of ion bombardment but by proper selection of masking materials, the films are selectively removed to delineate thin film contact. This technique has been used in etching Cr-SiO cermet resistor films (ref. 26). Small emitter openings have been etched in SiO_2 (ref. 26) and Pt in the beam lead metallization (ref. 20). The purpose of the work reported here is to see just how practical this method of etching is and to determine if it might be adaptable to production type processes.

Semiconductor contacts are usually delineated by a photoresist mask and chemically etched. This technique works well for a wide variety of materials and definition can be achieved of about 0.1 mil lines and spacing. In some particular applications such as thicker (1 micron) aluminum or an extremely difficult-to-etch combination of metals, e.g., Ti-Pt-Au, chemical etching has several disadvantages. In the Ti-Pt-Au system, the etchant used to attack the Pt readily etches and undercuts the gold.

Typical equipment used in sputter etching consists of an r-f sputtering unit depicted in figure 47. The sputtering fixtures are mounted in a diode configuration with a horizontal source facing upwards. For deposition, wafers are held face down on the substrate holder but in sputter etching the wafers are simply placed on the source and they in turn become part of the source from which material will be removed by ion bombardment. The plate under the wafers should be a material which sputters slowly.

Masking for the sputter etching technique has been provided by photoresist. Photoresist sputters at approximately the same rate as gold under ordinary conditions. This means that about 10,000 Å or more of resist is needed to mask the sputter etching of 7,000 Å of gold and 1,500 Å of platinum.

If the photoresist is thin enough so that most of it (but not all) is removed in sputtering the Au and Pt, the remaining resist is extremely difficult to remove. In most cases this resist residue may be removed by extended boiling in resist stripper.

It has been reported (refs. 26 and 27) that the removal rates of photoresists in sputter etching depend on the wafer

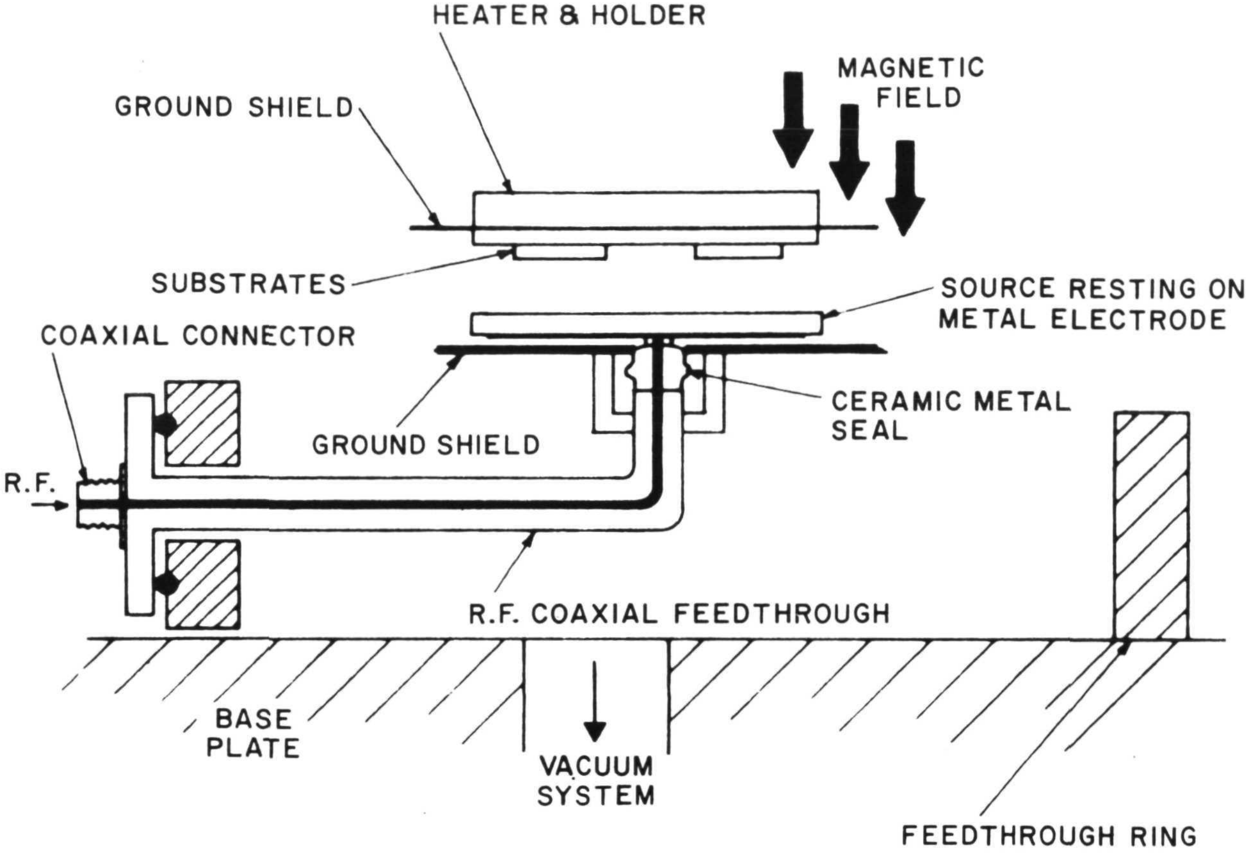
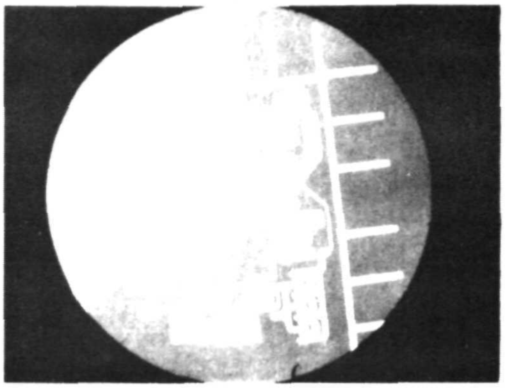


Figure 47.- Diagram of Diode RF Sputtering System

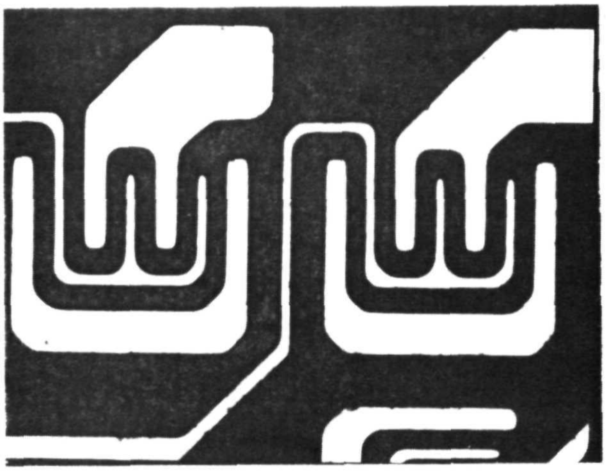
temperature and the reactive gases in the vacuum system. The removal rate increases with wafer temperature and can be decreased by a factor of two simply by water cooling the source target.

A second masking process has been used in beam lead work (ref. 20). In this use only the Pt is sputter etched and the thicker gold plated beams serve as the etch mask. After deposition of the Ti-Pt, the gold is plated to 2 microns or greater on the beams. The thick gold then serves as a mask and only approximately 3000 Å of the gold is removed in sputter etching the 2000 Å Pt film.

Figure 48 contains photomicrographs of a portion of the first layer metallization in a multilayer test pattern. This pattern was photo masked with 9000 Å of KMER (poise 0.15) and the Au and Pt were RF sputter etched. The Au thickness is approximately 8000 Å and the Pt is 1500 Å. Figure 48 (b) is a blown-up view of a portion of the pattern in figure 48 (a). The



(a)



(b)

Figure 48.- Photomicrographs of Sputter-Etched Ti-Pt-Au; Smallest Line 0.2 mil, Au 8000 Å, Pt 2000 Å, Ti 2000 Å

smallest line here is approximately 0.2 mil. There is excellent edge definition. This is not just a carefully selected portion of the wafer as every pattern over the whole wafer duplicates the photoresist mask. Nonuniform film thickness or etch characteristics do not degrade the definition that can be obtained by sputter etching. Figure 49 shows a cross section of the Ti-Pt-Au metallization. The magnification here is 1500X. The thickness of the Au is 8000 Å on top of 1500 Å of Pt. It can be noted that almost vertical edges of the line exist indicating that little or no undercutting occurs in the RF sputter etching.

Materials other than Pt and Au have also been sputter etched. At reasonable RF power levels, about 2.5 hours were required to remove 1.2 microns of aluminum. The technique is not very attractive for sputter etching of the aluminum because of the slow etch rate but as shown by the photos, excellent edge definition can be obtained even on this thickness of aluminum.

To demonstrate the versatility of sputter etching, four wafers were sputter etched simultaneously with different metallizations:

(1) Ti-Pt (2000 Å) - Au (8000 Å)
(2) Ti-Pt (2000 Å) - Au (5000 Å)
(3) Mo (2000 Å) - Au (5000 Å)
(4) Cr (2000 Å) - Au (5000 Å)

All four were sputter etched in one run. The gold cleared on some while the others were still not down to the second metal.

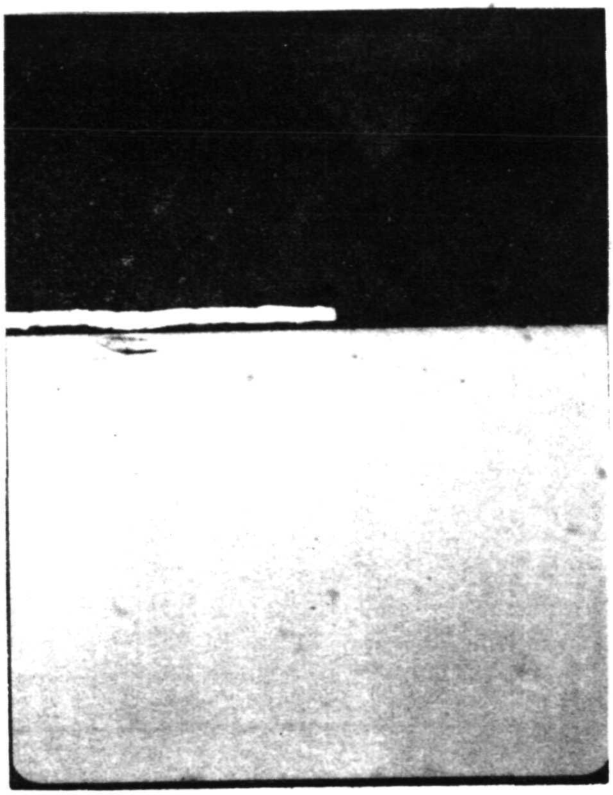


Figure 49.- Cross Section of Sputter-Etched Ti-Pt-Au

The Cr and Mo metals were being bombarded for a full five minutes after the gold cleared while waiting for the thicker Au and Pt metals to complete etching. There was no indication of undercutting on any of the wafers and a continuous film of Cr, Mo or Ti remained on all wafers. Therefore the process is easily controlled and is only limited by the resolution of the masking material and the relative sputtering rates of the materials.

Sputter etching of the Pt for beam lead work which is the Ti-Pt-Au system, has also been demonstrated. The Pt is sputter etched using either photoresist as a mask or the gold plating. In using the gold mask, the Pt is not etched until after the gold plating of the beams is completed. The thick gold (2 microns to 0.5 mil) then serves as a mask for sputter etching the Pt. The sputtering rate for the gold is only slightly faster than the Pt and approximately 3000 Å of plated gold is removed while sputter etching the Pt. The technique actually reduces the number of resist steps in the beam lead fabrication process by at least one from the required steps had chemical etching been used.

These results indicate the feasibility of the sputter etch technique in delineating semiconductor contacts. The practicality and adaptability of this technique for a production process obviously depends on the metal system to be etched. Clearly, its use in etching aluminum is limited. Even though excellent definition is obtained in aluminum, the extremely slow etch rate makes this technique impractical. However, for a system such as Ti-Pt-Au the sputter etching technique is practical and amendable to a production process.

BEAM LEAD TECHNOLOGY

The inception of beam leads dates back to 1964 when M.P. Lepselter of Bell Laboratories introduced the technology at the Electron Device Meeting in Washington, D.C. (ref. 20). Essentially, the original process was developed to batch-fabricate integrated circuits with electroformed electrodes cantilevered beyond the edges of the wafer. This type of structure simplifies the assembly and interconnections of individual units and integrated circuits, provides its own protective seal, and leads to a new class of integrated circuits (ref. 28), where isolation is accomplished by etched trenches under the metal bridging connections.

One-half-mil thick leads cantilevered beyond the edge of a silicon chip can be used for structural support of the chip as well as for electrical contact. The beam leads may be bonded to a metal-filmed substrate with matching patterns, eliminating the need for eutectic brazing to the substrate. This technique imposes no penalty upon the device.

These structures have been centrifuged without failure to an acceleration level of 135,000 g's. A typical geometric configuration would be a 7-mil square silicon chip, the beam leads 1 mil wide with 0.2 mil clearance between the electrode fingers, which are thinner than the beam leads. These fingers can have the close spacing required for high frequency operation.

Contact holes are etched through the oxide covering the silicon, platinum silicide ohmic contacts are formed in the holes and titanium and platinum layers are sputtered onto the silicon dioxide. Gold beams are electroformed using platinum as a base. The excess platinum outside the pattern is removed by glow discharge etching; the titanium is subsequently etched away. The slice is then turned over and an etch-masking pattern is developed in registry with the metallized patterns on the other side. The unmasked areas are etched away leaving individual devices with beam leads cantilevered beyond the edges of the slice with no additional processing. The previous etching operation may be used to cut isolation trenches in the integrated circuits, replacing isolation diffusion or solid-dielectric isolation.

Beam leads are used as alignment guides with multiple leads extending beyond the chip, locating one lead automatically registers the remaining leads. The surfaces to be joined to each other are both annealed gold and gold-gold bonds which make a very reliable meta-lurgical system. In addition, the handling during testing makes it possible that the silicon never be touched.

An early application of beam leads was 2 DCTL gates with 3 and 4 inputs of high frequency transistors, and nine beam-leaded boron-diffused silicon resistors. Several circuits wired as 3-stage ring oscillators with a fan-in of 3-4, and fan out of 1, yielded measured propagation delay of 4.2 ns.

A specific application of beam leads to monolithic integrated circuits was investigated by Waggerer (ref. 29). As a consequence of etching away the unwanted silicon from under the beam leads, isolated pads of silicon may be attained, interconnected by beam leads. The only capacitive coupling in these small metal-over-oxide overlays is typically 0.05 pf.

The processing was developed to survive 350°C oxidizing ambients (air or steam) continuously for 1000 hours without degradation. The metallurgical system is Pt_5Si_2-Ti-Pt-Au. Platinum silicide is used as the ohmic contact material for it is the most stable of the silicon compounds, has extreme corrosion resistance and is a solid phase at 980°C (ref. 30). It has an optical reflectivity different from either silicon or platinum and forms ohmic contact to heavily doped silicon.

In this particular reference the platinum is sputtered and heated to 700°C in an inert atmosphere. The platinum reacts with silicon to form Pt_5Si_2 which is a solid phase and will not ball up or creep beyond the edges of the contact holes as a eutectic would do. Platinum over the oxide is removed, leaving silicide inside the contact holes. Then titanium is deposited which has a high oxygen activity, refractory in nature, an ability to absorb almost half its weight in reaction products interstitially and the natural oxide that it does form is completely self-passivating at temperatures of about 400°C.

Table 29 lists some common metals and free energies of formation of their oxides in order of activity (ref. 31). This may be used as a guide for surface-bonding strengths. Titanium is the first active metal after silicon and in addition to having great bonding strength, titanium may be used to penetrate a thin SiO_2 layer (gettering). Gold is used as beam lead material because of its corrosion resistance, ease of bonding, low yield point, high elongation and suitability with high resolution electroforming. However, gold is a very reactive metal and reacts with titanium chemically at relatively low temperatures for form compounds which are undesirable. So platinum is used in a sandwich structure for it has a low diffusion coefficient with gold (D is less than 10^{-10} cm^2/sec. at 900°C) (ref. 32).

Metal films are normally deposited by evaporation but in this case, since there is a need for extreme adherence of titanium to silicon dioxide, the sputtering technique is used. Since sputtered metals have many times the energy of thermally

TABLE 29.- FREE ENERGY OF FORMATION OF METAL OXIDES AT $500^{o}K$ IN ORDER OF ACTIVITY

Metal	-F (K cal/mole)	$-f^{o}$ (K/cal/gram atom oxygen)
NiO	46.1	46.1
MoO_2	114.5	57.2
Cr_2O_2	240.2	80.1
Na_2O	83.0	83.0
Ta_2O_5	434.9	87.0
SiO_2	187.9	95.0
TiO	112.2	112.2
ZrO_2	238.4	119.2
Al_2O_3	362.1	120.7

evaporated metals, and are capable of dislodging impurities; it was decided to use the sputtering technique for both the titanium and platinum.

Electroforming is used to deposit 0.5 mil thick beam leads. The technique has been developed to the point where extremely small geometries are feasible. Using high resolution KPR*, dimensions under 0.2 mils are possible. At this stage the electrodes and beams are defined by gold. The remainder of the slice is coated with continuous layers of titanium and platinum plus patterns for beam leads and electroformed fingers. Titanium is easily etched using the gold pattern; but the platinum pattern must be formed by back sputtering.

This technology was developed mainly to improve the reliability of silicon planar devices by the elimination of "flying leads" (conventional wire bonding). The requisites of a good beam lead metallurgical system are essentially the same as for single and multi-metal systems:

1. Resistivity less than 10 micro-ohm-cm
2. Good adhesion to silicon and dielectrics
3. Low contact resistance to P-type and N-type silicon
4. Does not form degrading intermetallics between metal layers
5. Resists electromigration
6. Resists normal or electrochemical corrosion
7. Readily deposited and defined

*Product of Eastman Kodak

8. Introduces a minimum amount of damage or surface instability while being deposited
9. Compatible with multilevel processing
10. Beams must be ductile and easily bonded

Since the properties of a metal demanded by each function vary markedly, it is difficult to find a simple metallurgical system that will satisfy all the requirements. With the exception of the all-aluminum beam lead metallurgy (refs. 33 and 34) all other metallurgical systems reported are composed of three or more metals; the contact metal, the bond metal, the diffusion barrier metal, and the beam metal. This section will discuss beam lead materials, processing and reliability of beam lead technology now in use or to be used in the immediate future.

The first level metallization must have high conductivity, low contact resistance, must not degrade at high temperatures or current densities and be amenable to production techniques. Of the more commonly used metals: aluminum, chromium, titanium, molybdenum, platinum, palladium, cobalt and nickel; each appear to have advantages and disadvantages. In some cases these characteristics have been discussed in previous sections; but bear repeating.

Aluminum has high conductivity and low contact resistance but will dissolve the silicon substrate at elevated temperatures and/or high current densities. Chromium is an excellent contact metal as well as a good bond metal but forms rectifying contacts on P-type silicon over 0.02 ohm-cm. Nickel also makes rectifying contact on high-resistivity P-type silicon and suffers from degrading intermetallic compounds at high temperatures. Molybdenum is a good contact material and has good temperature stability but does form rectifying contacts on high-resistivity N-and P-type silicon (above 0.01 ohm-cm). Platinum comes the closest to the ideal contact material. It does, however, have one property that limits its use. Due to its very high melting point, it must be evaporated by electron beam or sputtered so that xrays are present during the deposition which can cause damage to MOS devices. Recently, palladium has been suggested (ref. 35) as a replacement for platinum on MOS devices since it can be evaporated from a tungsten filament, thus eliminating any possibility of xray damage. Since palladium has similar characteristics to platinum and can usually be etched*, the consensus of opinion is that palladium will replace platinum in beam lead technology. In the case of either palladium or platinum, a silicide is formed and markedly reduces contact resistance. See Table 30 (same as Table 21 in a previous section).

Metal silicide-Si contacts are prepared as follows. Silicide films of about 1000 Å in thickness are deposited onto oxidized

*Palladium can be etched in concentrated sulphuric acid at 60°C

TABLE 30.- METAL SILICON CONTACT RESISTANCE IN OHMS, AREA = $10^{-4} cm^2$

Si Resistivity Ohm-cm	Metal and Metal + PtSi									
	Al	PtSi	Mo	PtSi	Ni	PtSi	Cr	PtSi	Ti	PtSi
N-Type Si 0.001	0.09	0.02	0.08	0.02	0.02	0.02	0.03	0.03	0.01	0.01
0.01	6 (R)	0.1	5 (R)	0.4	2	0.3	3 (R)	0.2	4	0.2
P-Type Si 0.002	0.03	0.02	0.06	0.03	0.02	0.04	0.04	0.04	0.01	0.01
0.04	1	0.7	3 (R)	1	4 (R)	2	8 (R)	1	---	0.9
0.08	---	---	---	---	45 (R)	4	---	---	---	3
0.5	20	10	80 (R)	10	100 (R)	20	200 (R)	15	---	15

silicon wafers with contact holes by vacuum evaporation. The source silicides are prepared by melting the stoichiometric amounts of their constituent materials with the use of an hf generator in an argon atmosphere. In order to prevent oxidation of the silicide layer, the Pt layer of about 2000 Å in thickness is successively deposited onto the silicide layer. Evaporated platinum and silicide layers are chemically etched to form expanded contacts using photo resist techniques. These specimens are then heat-treated for 10 minutes at a proper temperature between 300°C and 700°C in an argon atmosphere. After heat treatment, a gold outer layer is deposited in order to make easy bonding of the lead wire for the electrical measurements. The I-V characteristics of the silicide-silicon contacts have been observed using a diode curve tracer and the measurements of the contact resistances carried out by the ordinary dc four-probe method. The shear adherence of the silicide layer to the SiO_2 surface is determined by the scribing technique (ref. 36).

The results of x-ray analysis show that as-deposited, silicides are amorphous but when silicide-silicon contacts are heat treated at temperatures above 400°C for 10 minutes the diffraction pattern corresponding to the silicides appears in addition to those of platinum and silicon. In the case of CoSi-Si contacts, the diffraction pattern corresponding to CoSi is observed for heat treatment at 400°C and those corresponding to CoSi and $CoSi_2$ at 500°C. In the case of PtSi-Si contacts, only diffraction patterns corresponding to PtSi is observed for heat treatment above 400°C. From the features of the I-V characteristics it has been found that the silicides such as CoSi, $CoSi_2$ and PtSi provide good ohmic contacts to n-type silicon having the resistivities less than 0.005 ohm-cm and to p-type silicon less than 0.01 ohm-cm.

The results of the measurements of the specific contact resistance, Rc for CoSi-Si and PtSi-Si contacts are given in Table 30 along with those of Al-Si (ref. 37). All the measured values are the average of at least four measurements. The values of Rc are reproducible to ±20 percent. It should be noted that all of the silicides studied yield low resistance ohmic contacts to heavily doped silicon and Rc is strongly dependent on the resistivity of silicon, regardless of the particular silicide contact. The effects of heat treatment on Rc are remarkable when the resistivity of silicon is relatively high.

The shear adherence of silicides to SiO_2 is presented in Table 31 in comparison with those of some familiar metals. Shearing forces are calculated from the indentation hardnfess of SiO_2 and the critical loads at which the silicide films are stripped from SiO_2 leaving a clear channel (ref. 38). The results are rather qualitative because measurements of the

TABLE 31.- THE VARIATION OF THE SPECIFIC CONTACT RESISTANCE WITH RESISTIVITY OF P-Si

Si Resistivity (ohm-cm)	Specific Contact Resistance (ohm-cm^2)		
	CoSi	PtSi	Al
1×10^{-2}	1.0×10^{-4}	1.3×10^{-4}	1.2×10^{-4}
5×10^{-3}	3.8×10^{-5}	5.8×10^{-5}	5.4×10^{-4}
2×10^{-3}	----	----	3.4×10^{-5}
1×10^{-3}	6.2×10^{-6}	1.2×10^{-5}	----

shearing forces larger than 1.70×10^{10} dynes/cm^2 become difficult due to cracking of SiO_2 surface. As seen in Table 32, PtSi exhibits excellent adherence to SiO_2.

TABLE 32.- ADHERENCE OF METAL SILICIDES TO SiO_2

Material	Shearing Force (10^8 dynes/cm^2)	Adherence to SiO_2
FeSi	37	low
$CoSi_2$	120	high
PtSi	170	very high
Au	--	very low
Al	170	very high
Co	54	intermediate
Mo	113	high
Ta	98	high
$CoSi_2$	70	intermediate

The experimental results suggest that the composite layered structures such as PtSi-Pt and CoSi-Pt-Au are suitable for reliable ohmic contacts for silicon planar devices. By applying these structures, a simplified process of beam lead technology has been developed.

In an analysis of beam lead technology the metal film deposited over the dielectric must adhere to silicon, silicon dioxide, silicon nitride, aluminum oxide and the second metal layer. In other words, the first metal film must not react with any material in which it contacts in a manner that would degrade the metallurgical system, electrically or mechanically. Although titanium is being used for most beam lead devices without any serious limitation, there are a number of other metals such as chromium, aluminum, zirconium, and hafnium, which could be considered as bond metals because of their adhesive qualities. Aluminum, in fact, has been used by itself to form a complete beam lead system (ref. 38). This system, however, is limited to low current (10^5 amps/cm^2) and low temperatures (400°C). Since all of these beam metals are very active, they are subject to corrosive undercutting during defining; therefore, they must be deposited in very thin layers.

As gold is most often used as the beam lead material, a diffusion barrier layer metal is used to prevent gold diffusion. Molybdenum is a good diffusion barrier and has the added advantage of being inexpensive and readily defined by chemical etching in the presence of the gold beam, eliminating several costly fabricating steps. Tests have shown molybdenum-gold metallization to be severely corroded in 85°C, 85 percent relative humidity ambients in 48 hours, where platinum-gold metallizations have exceeded 1000 hours in the same atmosphere (ref. 39). Since the beam is the contact medium between chip and substrate, special consideration must be given to its compatibility with the substrate metallurgy as well as the chip metallurgy. In general, a beam metal must have the following characteristics:

1. Good mechanical strength
2. Easily deposited in thick layers (>50,000 Å)
3. Easily defined by controlled deposition or etching
4. High corrosion resistance
5. Low yield point
6. Coefficient of expansion near to that of silicon or high elongation to overcome mismatch
7. High conductivity
8. Easily bonded.

Gold, aluminum, nickel (ref. 40) and copper (ref. 38) are most often suggested as potential beam metals that could be used in conjunction with a variety of bond and barrier metals. Unfortunately, many of these metal systems deteriorate rapidly in corrosive environments which are accelerated if the metals are under electrical bias. Table 33 shows the effect of electrical bias on some of these metal systems while submerged in a boiling 1 percent solution of ammonium hydroxide in deionized water. The vehicles used for testing the metals listed were silicon dice upon which has been patterned parallel "dogbone" conductors to which suitable bonded connections were made. A potential of 10 volts was applied to pairs of the strips while chips were submerged in the electrolyte.

Although the all-aluminum beam lead system has too many restrictions for general use, it does offer a simple, inexpensive metallurgy for low current applications. A typical all-aluminum system (ref. 34) consists of a conventional integrated circuit on which a layer of silane glass is deposited and windows are

TABLE 33.- ELECTROCHEMICAL CORROSION TEST RESULTS (REF. 41)

Metal	Type of Failure	Time	Remarks
Al	All contacts open	<5 min	(-) Terminal faster
Ti-Pt-Au	Resistance increase	>3 hr	Au deplates (+) terminal
Ti-Pt	Slight resistance change	>24 hr	Au wire bond opened
Ti-Rh	Slight resistance change	>24 hr	Au wire bond opened
Cr-Ag-Au	Open (Cr)	<5 min	Cr from under Ag-Au, even with glass or Si_3N_4 overcoat
Ti-Ag	Large resistance change	<5 min	Ag corrodes but not removed
Hf-Au	Resistance increase	>3 hr	Au deplates (+)
Ti-Ag-Au	Resistance increase	>3 hr	Au deplates (+)
Ti-Mo-Au	Open (Mo)	<5 min	Mo from between Ti and Au
Ti-Au	Resistance increase	>3 hr	Au deplates (+)
Mo-Au	Open (Mo)	<5 min	Mo from under Au, even with glass overcoat
Cr-Au	Open (Cr)	<5 min	Cr from under Au
W-Au	Resistance increase	2-3 hr	W removed = some rate as Au
Zr-Au	Resistance increase	>3 hr	Au deplates (+)
Nb-Au	Resistance increase	>3 hr	Au deplates (+)
Ta-Au	Resistance increase	>3 hr	Au deplates (+)
Ni-Au	Resistance increase	>3 hr	Au deplates (+)
Co-Au	Resistance increase	>3 hr	Au deplates (+)
V-Au	Open (V)	<5 min	V removed (+) from under Au

opened over the bonding pads. (See figure 50.) This is followed by a multiple source deposition of aluminum until a 5-10 micron layer is deposited. The aluminum is then defined and the slice thinned and etched through. While these devices did pass the standard storage and operating life tests at low current densities, failure by electromigration does occur at current densities above 10^5 amps/cm^2. Another reference (ref. 38) describes a process which includes the application of silicon nitride as passivation on top of the thermally grown silicon oxide. The aluminum contacts and interconnections are fabricated using standard techniques. They are mechanically and electrically protected by a cover of SiO_2. A combined layer of sputtered and vapor deposited SiO_2 proved to yield the best protection. The sputtered quartz shows excellent adherence to the aluminum interconnections, however, since the sputtering rates were low (150 Å/min), the desirable total thickness of the quartz layer was achieved by an additional fast pyrolythic deposition using the silane-oxygen system (400 Å/min). With the combination of

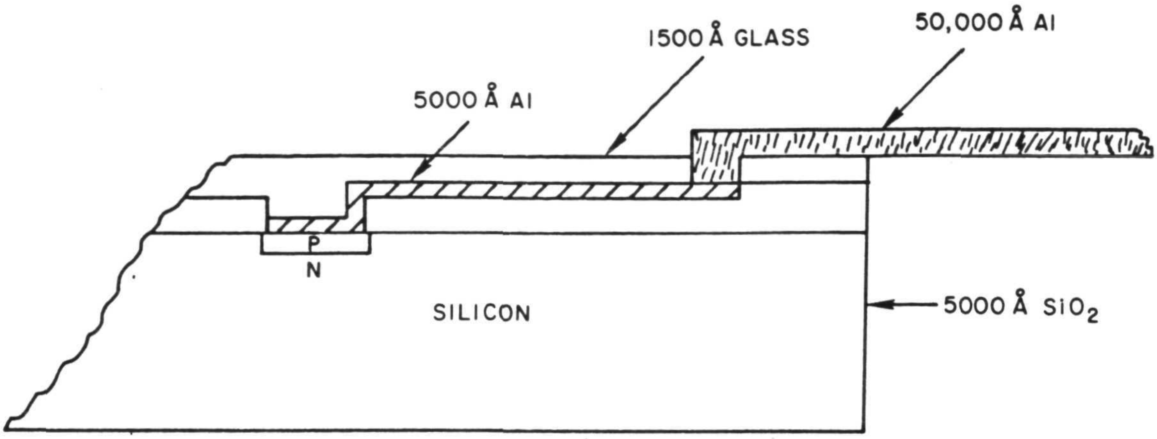


Figure 50.- Aluminum Beam Lead System with Separately Deposited Beams

2000 Å sputtered and 6000 A pyrolythic quartz, the pinhole density dropped to a minimum. Ninety seven percent of the circuits were free of pinholes. For the connection to the beam leads, feed-through windows are cut in the deposited oxide and layers of titanium (1000 Å), platinum (3000 Å) and gold (2000Å) are sequentially sputtered onto the entire wafer. The beams are then electroplated to the proper height. The sputtered gold and platinum is removed from the unwanted areas by sputter etching and the titanium is chemically etched. See figures 51 and 52. Despite the fact that pure metal layers were deposited, all devices with aluminum interconnections and Ti-Pt-Au beams showed high contact resistance (up to 1000 ohms). The electrical behavior of these contacts strongly indicated the existence of an aluminum oxide between the aluminum interconnections and the titanium. Therefore, it was necessary to introduce a sputter etching step prior to the deposition of the titanium. With this method and the sequential deposition of pure Ti-Pt-Au, excellent contacts were obtained.

A copper system (ref. 38) was also developed with the purpose to increase the radiation resistance of integrated beam lead devices. Again silicon nitride is used as passivation on top of the thermally grown oxide. Platinum silicide provides the semiconductor-metal contact (ref. 41). Titanium (1000 Å) platinum (3000 Å) and copper (2000 Å) is then sputtered sequentially and the interconnections and beams electroformed to the desirable height. Sputter etching is again used to remove the sputtered copper and platinum from unwanted areas. The titanium bottom layer is etched away chemically. Along with the work referenced above, two multilayer interconnection systems for integrated circuits have been developed. In both systems, platinum silicide provides the necessary semiconductor-metal contacts. The first layer interconnections consist of titanium,

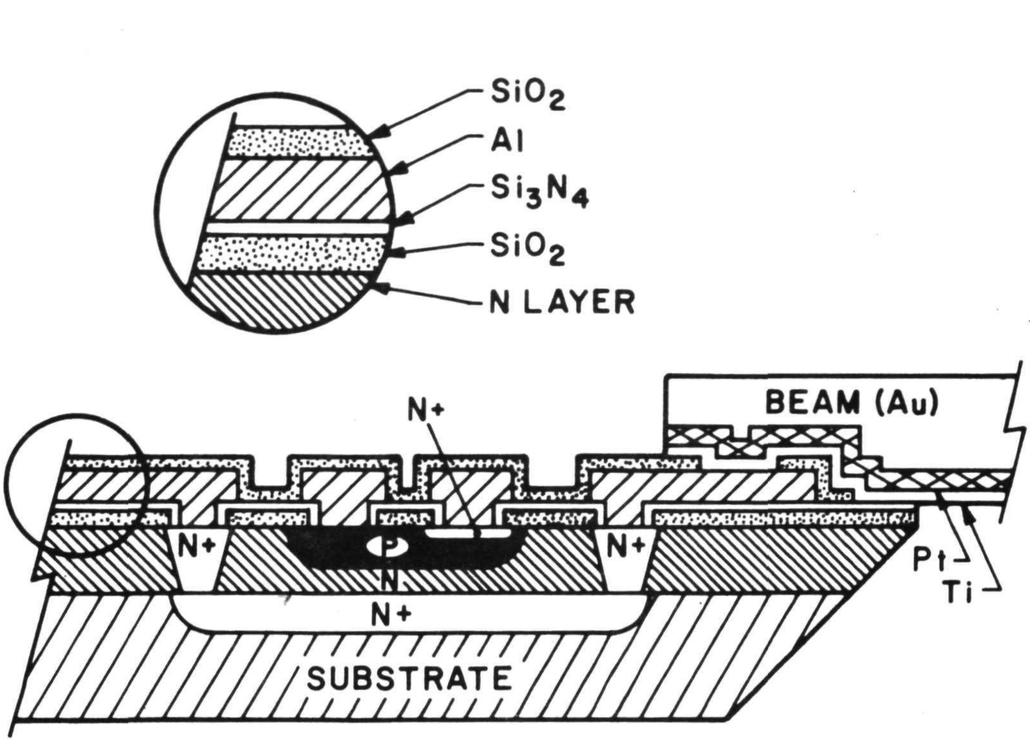


Figure 51.- Cross Section of Beam Lead Device with Glassivated Aluminum Interconnections

platinum, and gold. A dielectric layer of sputtered quartz is applied on top of the first metal level. After the feed-through holes are etched where contact to the lower level is desired, titanium and gold is sputtered; and the top layer is electroformed using the gold layer as a base. The removing of the undesired gold and titanium layer inbetween the interconnection pattern by sputter and chemical etching completes the fabrication of this double layer system. Electrical testing of these crossovers showed a break-through strength of approximately 80 volts. In a second multilayer interconnection system, the two metal layers are separated by a combination of SiO_2 and an air gap (ref. 43). After the first layer of interconnection is formed, a layer of SiO_2 is sputtered on top of it. Feed-through holes are etched in the oxide to provide the contact areas between the two metal levels. Copper is sputtered then over the whole area and built up to the desired thickness of the air gap by electroplating. Feed-through holes are etched through the copper using sputter etching. Electroforming of the gold top layer, using the copper as a base and removing this copper after plating by chemical etching, completes this structure of two layers of interconnections isolated by a quartz-air gap dielectric. (See figure 52.)

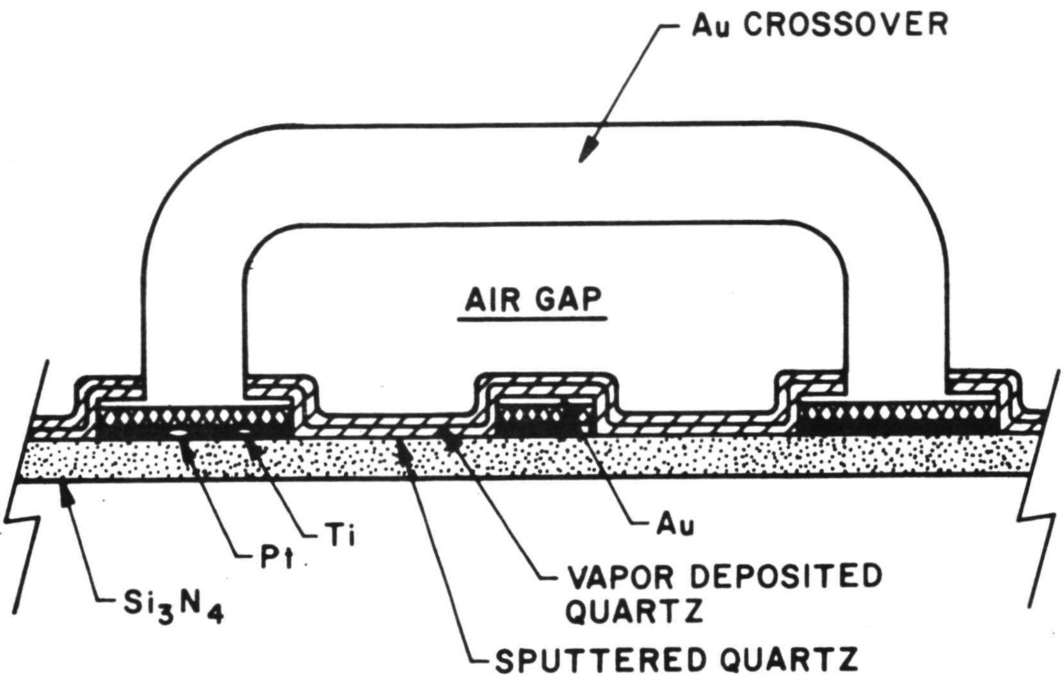


Figure 52.- Cross Section of Dielectric and Air Gap Isolated Crossover

Platinum and palladium have not been evaluated as beam metals but they have potential in this application for high-reliability devices which are subjected to very severe corrosive environments. The cost would be higher and the bonding would be more difficult but the thermal expansion mismatch would be less and the corrosion resistance would be far superior to any other metal system.

For most applications gold beams are almost the unanimous choice due to ease of bonding and fabrication. In addition, gold has a relatively high corrosion resistance. While gold on titanium and platinum is the technique most widely used, there are recent reports on gold beams on aluminum (ref. 34) and molybdenum-aluminum (ref. 44).

This survey was intended to cover only metallization; but one might say that a metallization system is only as good as the dielectric under or on top of it. Currently three dielectrics are used; silicon dioxide, silicon nitride and aluminum oxide.

They can be used separately or combined. Silicon dioxide is usually deposited by the thermal oxidation of silicon. Although oxide processing has improved in the past few years, it has inherent disadvantages in its lack of resistance to ion migration (1000 Å of SiO_2 is penetrated by sodium in 20 minutes at 300°C) of alkali metals and permeability by moisture and certain dopant materials (gallium and aluminum). Due to its porous structure, impurities migrate quite readily through silicon dioxide (ref. 44). The field migration of impurities is accelerated by elevated temperatures. The movement of this ionic charge toward the silicon-silicon dioxide interface and the subsequent buildup and termination of an ionic induced field within the semiconductor material results in degradation of both bipolar and MOS devices. In bipolar device structures and integrated circuits, this ionic oxide contamination causes degradation of junction characteristics due to accumulation, depletion and inversion. Accumulation generally results in lowered breakdown voltage. Inversion causes an increase in leakage current. Treating the silicon dioxide surface with P_2O_5 prior to metallization has improved the stability of silicon dioxide. The phosphorus is deposited from a vapor on the silicon dioxide in a diffusion furnace at temperatures from 900-1100°C for short periods of time. The phosphosilicate glass forms on the device surface as a result of this process. The theory is that the phospho-silicate glass acts as a gettering agent for ionic impurities; and also neutralizes sodium ion contamination near the silicon-silicon dioxide interface (ref. 45).

Silicon nitride has two main advantages:

1. It is found to be a barrier to field-enhanced (10^5V/cm) sodium diffusion at 400°C
2. The dense silicon nitride film has made it possible to consider eliminating hermetic packaging. With the demise of junction sealed hermetic chips, the reliability of plastic packaging would be improved.

In addition to silicon nitride's extreme resistance to ionic contaminants, its properties include a high degree of chemical inertness, high temperature strength, extreme hardness, and thermal shock resistance. Silicon nitride will crack but not until the thickness of the deposit exceeds 2000 Å.

Table 34 presents a comparison of properties of silicon dioxide and silicon nitride. As can be noted, the physical, chemical and electrical properties of silicon nitride films are process dependent. If silicon nitride should be used as a replacement for silicon dioxide it would provide a better diffusion mask and passive dielectric. However, there is instability of the $Si\text{-}Si_3N_4$ interface due to tunneling and trapping at the interface. Silicon nitride deposited over a thermal oxide will not contaminate the oxide layer composite it covers and will act as a barrier to impurities if it is free of pinholes. The quality of the oxide is extremely critical in MOS structures as the conventional oxide remains and the silicon nitride is deposited over this oxide. In the contact windows the silicon dioxide is regrown prior to silicon nitride deposition producing a more uniform stress-free film and minimizing pitting of the highly phosphorus doped silicon during the nitride etch.

TABLE 34.- SUMMARY OF PHYSICAL PROPERTIES (ref. 46)

	SiO_2 Amorph.	Si_3N_4 Cryst.	Si_3N_4 Amorph.	$Si\text{-}O_xN_y$ Amorph.
Melting Point (^oC)	~1600	~1900	--	--
Density g cm^{-3}	2.2	3.4	3.1	--
Index of Refraction	1.46	2.1	2.05	1.60-1.88
Dielectric Constant	3.8-3.9	9.4	7.5	4.77-6.12
Dielectric Strength V cm^{-1}	~5 x 10^6	--	~1 x 10^7	~5 x 10^6
Infrared Absorption Band μm	9.3	10.6	11.5-12.0	9.3-12.0
Energy Gap (e.v.)	8	3.9-4.0	~5.0	--
Thermal Expansion Coeff./^oC	5.6x10^{-7}	3.0-3.5 x10^{-6}	--	--
Thermal Conductivity cal cm^{-1} sec^{-1} $^oC^{-1}$	0.0032	0.067	--	--
dc Resistivity ohm-cm				
at 25^oC	10^{14}-10^{16}	10^{15}	~10^{14}	
at 250^oC	--	--	--	
at 300^oC	--	--	--	
at 350^oC	--	~10^{13}	~2 x 10^{13}	
Etch Rate in Å/min in 10:1 NH_4:HF	1000	<0.1	5-10	33-400

(Thermal Expansion Coefficient of Silicon: 3.2 x 10^{-6}/^oC.)

The most widely used technique of depositing silicon nitride is pyrolytic decomposition followed by synthesis at elevated temperature. The gases, in most cases silane and ammonia, in a carefully controlled ratio, are reacted using a carrier gas (H_2-N_2, etc.) at temperatures from 750-900°C. Another reaction is the pyrolysis of silicon tetrachloride and ammonia over the same temperature range. The more critical deposition parameters and their effects on film properties are shown in Table 35.

TABLE 35.- SiO_2-SiN_4 DIELECTRIC COMBINATIONS

	SiO_2	SiN_4
MOS Logic	500 Å	≥1000 Å
Bipolar	5000 Å	≥1000 Å
Nonvolatile Memories	<50 Å	≥1000 Å

Two other deposition techniques used for silicon nitride are rf and dc sputtering, or glow discharge. Rf reactive sputtering has been found to be superior to dc sputtering because it does not have problems of dissociations, and nonstochemetric deposition (ref. 46). Sputtering must be accomplished without oxygen contamination since it will react more readily than nitrogen to give a silicon oxynitride type film. In glow discharge the rf technique is usually used. The merit of this technique is the low temperature to which the substrate is exposed. The high temperature which is generated within the gaseous discharge initiates the decomposition reaction of the reactant gas mixture. The energy for the reaction is usually supplied to a low pressure gas stream and is either inductively or capacitively coupled by an rf coil surrounding a quartz reaction tube. Substrate temperatures around 300°C produce high density film.

Since nitride passivated devices also have an oxide-silicon interface, annealing is done subsequent to opening windows through the nitride (refs. 48 and 49). This allows the forming gas or H_2 to permeate the Si-SiO_2 interface to reduce the number of states. Since most passivating silicon nitride films are deposited at a thickness of 1000-1500 Å, new techniques of etching have been developed:

1. Use of silicon dioxide in place of photoresist for masking
2. Anodic conversion of silicon nitride to silicon dioxide followed by conventional oxide etching
3. Sputter etching using photoresist as a mask.

Oxide masking with pyrolitically deposited SiO_2 is the most common method used for selective etching of Si_2N_4. This is accomplished in most cases in the same furnace as the nitride deposition. The etchant used is a mixture of phosphoric acid and water which etches silicon nitride much faster than silicon dioxide. Typical etch rates with this solution would be 150 Å/min for silicon nitride and 20 Å/min for silicon dioxide. Silicon nitride etched contact windows are well defined and do not have the slope of an oxide window. This causes difficulty with stress and shadowing of deposited metal contacts. Generally, the silicon nitride is deposited over a thin silicon dioxide film in the contact windows. The etching of the oxide is accomplished using the silicon nitride as a mask. This procedure in many cases causes "shelving" (see figure 53) of the silicon nitride at the oxide interface due to lateral etching of the oxide. This can cause shadowing of the metal deposit, stress and cracking under thermal cycling. The so-called "shelving" causes the oxide step under the nitride to have a lateral etched shelf, possibly causing:

1. Discontinuity in metal film contact
2. Stress in deposited metal film
3. Variation in thickness of deposited metal films
4. Alloying at elevated temperature (400°C) due to cracking or shadowing in barrier metal (Pt, Pd).

The scanning electron microscope is a valuable tool for determining the extent of this problem, and for determining process control improvements needed to minimize the effect in etching this composite film.

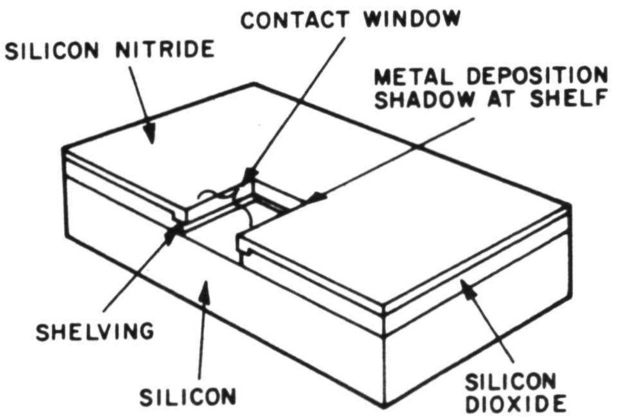


Figure 53.- Shelving in Oxide-Nitride Dielectrics

The barrier capability of silicon nitride can be monitored using the same MOS capacitor C-V measurement used on silicon dioxide. In this case, films of silicon nitride-silicon dioxide composite can be intentionally contaminated. It has been found that the etch rate of silicon nitride in buffered HF (25°C) is a very good measure of film density and quality. Etch rates greater than 25 Å/min are an indication of films which will fail to mask the diffusion of sodium ions and water vapor. A graph of etch versus density, computed from oxygen content for Si_3N_4 films is presented in figure 54.

Exposure of oxidized silicon surfaces to ionizing radiation brings about permanent changes in the motion of a positive space charge in the insulation, and an increase in density of fast

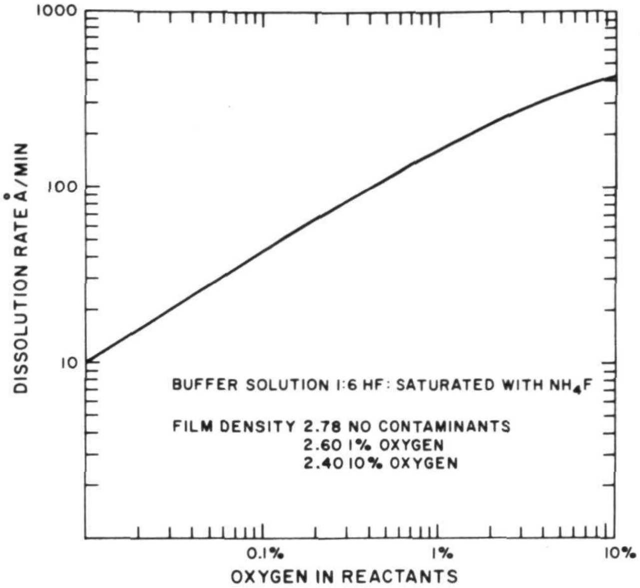


Figure 54.- Etch Rates of Silicon Nitride vs Oxygen Content

interface states (ref. 50). Less sensitivity to ionizing gate threshold voltages have been obtained with doses of $1x10^{14}$ e/cm^2 (1.5 mev electrons) for nitride oxide gate dielectrics as compared to $1x10^{11}$ e/cm^2 for oxide gate dielectrics (ref. 51).

The intrinsic capability of silicon nitride as a barrier has been well documented in the literature (refs. 52, 48 and 53). These studies indicate negligible penetration of solium into silicon nitride by either thermal diffusion up to temperatures of 600°C or field-enhanced diffusion to 300°C. Many laboratories have monitored silicon nitride-silicon dioxide composites using the MOS C-V measurement technique and have found it to be an extremely effective tool for measuring integrity of the dielectrics (ref. 54).

One additional film dielectric that shows promise as both a protective passivating layer and a source of improvement in MIS transistor characteristics is aluminum oxide. This film is used in a composite structure with SiO_2 similar to silicon nitride-silicon dioxide. The most widely used deposition technique is the synthesis of $AlCl_3$ using both hydrogen and carbon dioxide to hydrolyze $AlCl_3$ to Al_2O_3 (ref. 55). The composite film is processed very much like silicon nitride in that a good quality, clean oxide with low interface density is the initial gate dielectric and the barrier Al_2O_3 is deposited over it. Temperature of deposition is normally 900°C. Al_2O_3 has also been deposited by r-f sputtering both on silicon and over SiO_2. Good control of processing and deposition conditions is necessary to produce good quality films (ref. 56). The Al_2O_3 composite is particularly attractive since it causes a positive shift in threshold voltage due to some polarization at the Al_2O_3-SiO_2 interface which is not clearly understood at this time (ref. 57). This voltage shift allows for very low threshold device structures. These alumina layers give good protection against external contamination and, like silicon nitride, the use of Al_2O_3-SiO_2 composite in practical MOST's is dependent on quality SiO_2 beneath the alumina.

METALIZATION

Metallization on an oxide-free surface is very important. A thin oxide or organics will prevent the formation of a uniform contact area. The following procedure has been used which has consistently yielded excellent results. Removal of organics takes place in an oxygen glow discharge (asher) for 30 minutes followed by a two minute etch (600 HO, 15 HF, $7HNO_3$) immediately preceding evaporation. Sputter etching for precleaning (refs. 58 and 59), is used; but generally not preferred since it heats the silicon wafer and can reoxidize the surface if a sufficient amount of oxygen is present. Various metals have been investigated and evaluated as ohmic contacts to silicon; however, only platinum has seen extensive use in beam lead technology. Electron beam evaporation and dc and r-f sputtering of platinum are being used but the best results are obtained with r-f sputtering. The sputtering system consists of a sputtering electrode for each metal and one backsputtering electrode with four water-cooled platens for slice holding. After an initial pumpdown to 10^{-6} torr, the chamber is backfilled with ultrahigh purity argon to slightly higher pressure (25 to 100 microns) while pumping against a restriction (e.g. partially opened high vacuum valve). This facilitates plasma initiation after which the electrode is presputtered for five minutes with the shutter in place. 500-800 Å of platinum is then deposited in six minutes using conditions outlined in Table 36.

TABLE 36.- SPUTTERING CONDITIONS

Source to substrate distance	1-1/4 inches
Chamber pressure	25 microns
Atmosphere	Ultra high purity argon
RF power	100 watts
Platen diameter	7 inches

Formation of platinum silicide takes place at temperatures from 550-700°C. It can be formed inside the vacuum chamber or preferably in a tube-type furnace. Heating in the vacuum system requires jigging which, when heated, adds considerably to the pumping time and makes frequent maintenance necessary. In order to prevent the silicon surface from oxidizing through the thin platinum layer, the wafers are loaded immediately after deposition onto a cool boat in a vertical position parallel to the gas flow. After a five-minute flush, the boat is positioned in the tube outside the furnace end before heating for 20 minutes at 640°C. The boat is cooled at the tube end for 10 minutes. Before heating, the platinum surface is uniformly colored and afterwards is gray in the contact windows. If a change in color is not observed, then silicide is not formed. The excess platinum over the oxide is removed using room temperature aqua-regia which does not attack the silicide. Wafers may be successfully reprocessed through the cycle providing that no shallow junction devices are present.

Titanium-molybdenum-gold is evaporated by means of an electron-beam dual gun, diffusion-pumped system capable of co-evaporating molybdenum and gold at a pressure of $< 3 \times 10^{-7}$ torr. Metal bell jars are preferable so that the surface can be heated or cooled by means of water flowing through coils. Bell jar walls should be heated when the jar is opened to prevent condensation and, during initial pumpdown, to provide outgasing. To increase titanium gettering efficiency and decrease outgasing during evaporation, the walls are chilled. An efficient deposition rate is 200 Å/min. Molybdenum (ultra-high purity) is deposited immediately following the titanium to insure a non-oxidized interface. Because of high resistance and poor adhesion, the molybdenum-gold interface has proven to be weak unless the gold is codeposited for the last 50 Å or followed by a one hour bake at 300°C after etching excess metal from between gold beams. Molybdenum is deposited at a rate of 200 Å/min for 10 minutes followed by a 1400 Å layer of gold deposited at a rate of 200 Å/min. Typical resistivities are: Ti = 74 micro-ohm-cm, Mo = 40-60 micro-ohm-cm and Au = 4 micro-ohm-cm. The adherence of titanium is greatly affected by the precleaning. If aqua-regia is the last step before evaporation, peeling can be seen during the evaporation. The same condition occurs if water is allowed to evaporate from the silicon surface.

An alternative system uses aluminum interconnects and gold beams (refs. 59 and 60). Following a filament evaporation of 12,000 Å of aluminum, the aluminum is etched in phosphoric-nitric acid using photoresist for deliniation. 4000 Å of silane is deposited, windows opened to the aluminum, followed by depositions of 800 Å of Ti, 2000 Å of Mo and 1400 Å of gold using electron beam evaporations. The titanium has excellent adhesion to the aluminum while the molybdenum serves as the barrier metal preventing the formation of gold aluminum intermetallics. Advantages of this system are:

1. Aluminum contacts have been investigated extensively
2. Capability to apply the beam lead technology to integrated circuits having standard metallization.

A third system consists of the Ti-Pt-Au metallurgy (ref. 20). Of the systems used this one is least affected by surface conditions. Excellent adhesion at all interfaces is commonplace. Initially, the three metal layers were sputtered, but gold sputtering was unsatisfactory. Presputtering is essential to remove residual oxides of titanium. Care must be taken to eliminate all traces of oxygen or water vapor. Titanium is sputtered at a rate of 100 Å/min to a total thickness of 900 Å. Platinum is deposited at a rate of 200 Å/min to a thickness of 2000 Å preceded by another five-minute presputtering step. Either of two processing procedures are used: the platinum properly masked with photoresist covering the metallization pattern, is etched in $HCL/HNO_3/H_2O$ at 80°C. Thus, the titanium becomes the conductive metal for gold plating. The second procedure requires gold plating directly on the platinum using titanium and platinum as the conductive metals for gold plating.

Gold beams are electroformed in two steps using separate photoresist techniques (ref. 61). A positive type resist is used for the interconnecting metal since fine line geometries are needed. In the second plate, where fine geometries are not needed, a negative resist is preferred becuase of better durability for the longer plating times required. Acid type gold baths (refs. 61 and 62) having a gold content of 0.7-1.5 troy ounces per gallon, a density of 14° to 16° baume, and operating at a temperature of 45°C are used. In addition to adhesion, thickness and ductility are of prime concern. Thicknesses are checked optically during plating. A microhardness test after plating is used as a measure of ductility. Interconnecting metal is plated to 0.1 mil and the beam buildup requires a total thickness of 0.5 mil. The gold plating is baked in a nitrogen atmosphere at 350°C to improve beam adherence. The titanium is etched from between the beams, the gold beams themselves acting as the etch mask. Over etching can be a problem which results in a weakening of the beam adhesion. An alternative sputter-etch technique involves the removal of platinum using gold beams as the mask. Uniform removal from areas having a width of <0.2 mil are practical without undercutting the larger areas, which is sometimes a drawback for chemical etching. Either of two procedures can be followed for effective platinum removal. One is the use of argon as the ionizing gas; the bombardment continues into the titanium layer requiring a thicker titanium layer. In the second procedure, oxygen in argon is the ionizing gas. In this case the titanium forms an oxide which protects the titanium film from attack. This thin oxide is subsequently removed by sputter-etching. In the case of titanium-molybdenum-gold, each metal is removed selectively using chemical etches.

CONCLUSION

In an industry such as integrated circuits, where technology progresses so rapidly, there are probably no two manufacturers who use exactly the same processing to fabricate similar type circuits; which makes the interpretation of reliability data from manufacturer to manufacturer difficult to correlate. In cases where the development of a process has been difficult, and therefore slow, the engineers may have designed around this deficiency. This sort of procedure may or may not directly affect reliability. Regardless of processing procedures, the specific integrated circuit structure and design can be important factors in determining whether a given metallurgical reaction results in significant degradation of the device characteristics. Many failures observed and discussed previously are due to manufacturing defects rather than inherent limitations of the metallurgical systems. It is therefore very important to consider the capability of the manufacturer, both from the technical approach and from processing reliability.

As discussed, aluminum is the most widely used metallization system at this time for the fabrication of silicon integrated circuits. Although aluminum has certain limitations, (if these limitations are not prohibitive) aluminum is the best choice for both single and multilevel metallization. Beam lead technology although originally developed for the titanium-platinum-gold metallurgical system has been successfully adapted to the all aluminum system.

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