Final Report

A DIGITAL MATCHED FILTER TECHNIQUE FOR THE TRACKING AND DATA ACQUISITION SYSTEM

By

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16. Abstract

The report presents design information and test results for a breadboard implementation of a digital matched filter for PN sequences. The device is intended to expedite acquisition in PN spread-spectrum communication systems.

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1. INTRODUCTION

This document is the final report under Contract NAS5-20201. The contract requires the development, test and delivery of a breadboard Digital Matched Filter for Pseudo-Noise Sequences. This device has the capability of greatly reducing the initial synchronization time normally encountered with pseudo-noise coded spread-spectrum communication systems.

The primary objective of this program is to demonstrate a working model of a unique implementation of a Digital Matched Filter for Pseudo-Noise Sequences thereby resolving any remaining theoretical uncertainties concerning this implementation. A secondary objective is to provide preliminary guidelines for the application of a Digital Matched Filter in the Tracking Data Relay Satellite (TDRS) communication and tracking links or similar application.

This report reviews the basic principles underlying the digital matched filter design. A detailed description of the breadboard implementation is given. The results of laboratory tests and comparison with theoretical performance is presented. The report concludes with a discussion of digital matched filter application in communication and tracking links such as TDRS.

2. MOTIVATION FOR MATCHED FILTER DETECTION OF PN SEQUENCES

The reduction of initial acquisition time in PN communications and ranging systems is the motivation for matched filter reception as opposed to correlation by multiplication and integration. To illustrate the comparison consider, in Figure 1, an elementary multiply-integrate detector. The PN generator produces a code with transition interval (chip duration) Δ. Integration is over a duration of M chips sufficient to provide adequate SNR at the integrator output. The initial acquisition process consists of bringing the local and received PN sequences into synchronism to within Δ. This is accomplished by stepping the code generator by increments Δ after each $M\Delta$ integration until the integrator output crosses a threshold level. The code generator must dwell at each step position for at least one integration interval $M\Delta$. The acquisition time depends on the initial time uncertainty, T_{unc}, in synchronization between local and received time base. This uncertainty involves unknown propagation delay and lack of synchronism between the clocks at the transmitting and receiving terminals. At worst the receiver must search through the entire range of T_{unc} in steps of Δ dwelling $M\Delta$ seconds at each step. This process requires a time $M\Delta(T_{unc}/\Delta) = M\,T_{unc}$. We define T_{unc} to exclude the position of correct correlation so that

$$\text{Max. Acquisition Time for Multiplier-Integrator} = (T_{unc} + \Delta)\,M \qquad (1)$$

If there is no time uncertainty, $T_{unc} = 0$, but it still takes $M\Delta$ seconds for the integrator output to build up to the desired level from the instant the signal is applied to the receiver.

It may turn out, in some instances, that the code period P(in chips) is less than the time uncertainty. In that case synchronization of the code sequences will not resolve the total time uncertainty, but there will remain

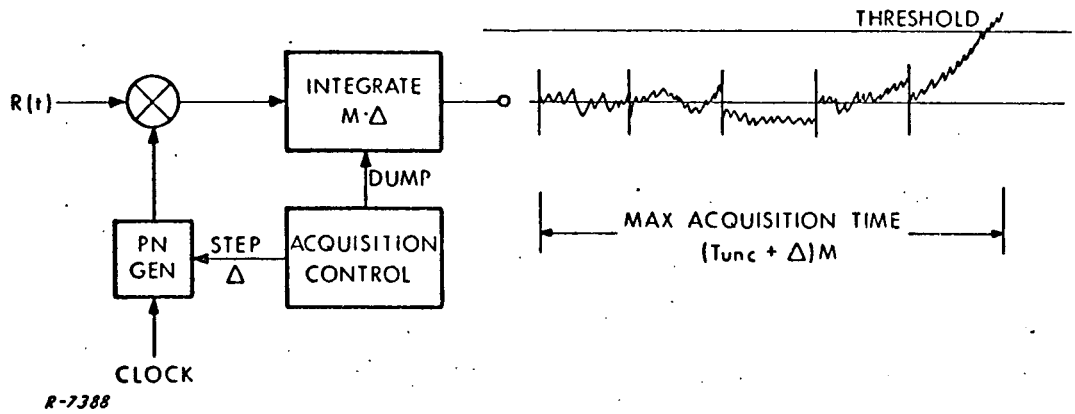
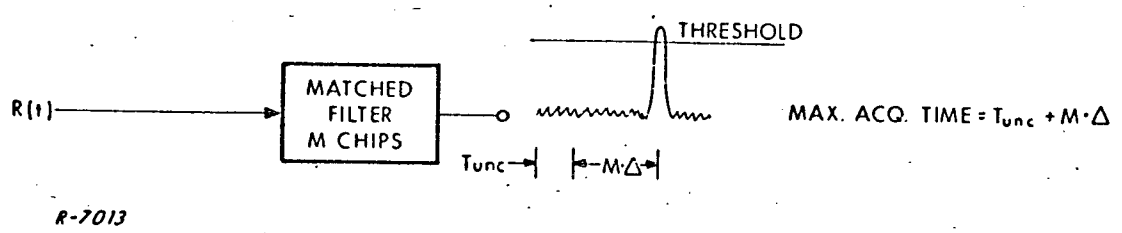


Figure 1 Multiplier-Integrator Acquisition

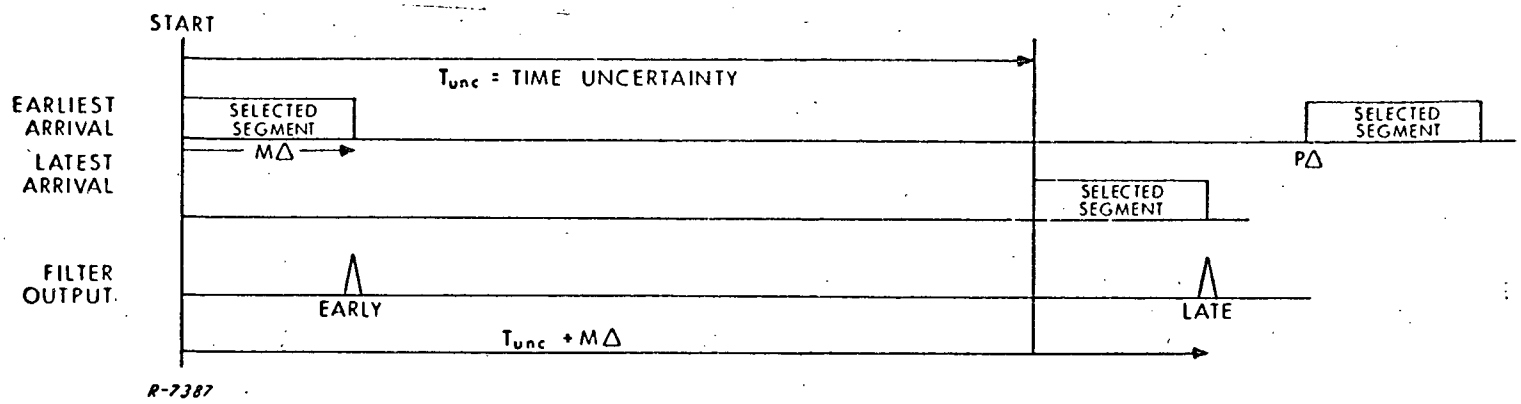
a time ambiguity equal to an unknown number of complete code periods. Nevertheless, after code acquisition it is possible to demodulate data and to measure fine but ambiguous range. For purposes of code acquisition the time search need cover only one period $P\Delta$ and the maximum acquisition time is $P\Delta M$. If the integration interval equals the code period the maximum acquisition time for the multiplier integrator becomes ΔP^2.

With the matched filter (Figure 2) the acquisition procedure consists of setting the filter impulse response with an M-chip segment of the expected PN sequence. The segment is selected to coincide with that portion of the sequence which would arrive at the instant when the signal is applied to the receiver assuming the earliest possible arrival as defined by the initial uncertainty. The filter will respond with an output pulse corresponding to the autocorrelation of the code segment whenever the matched segment arrives. The threshold crossing of the output pulse establishes receiver synchronization.

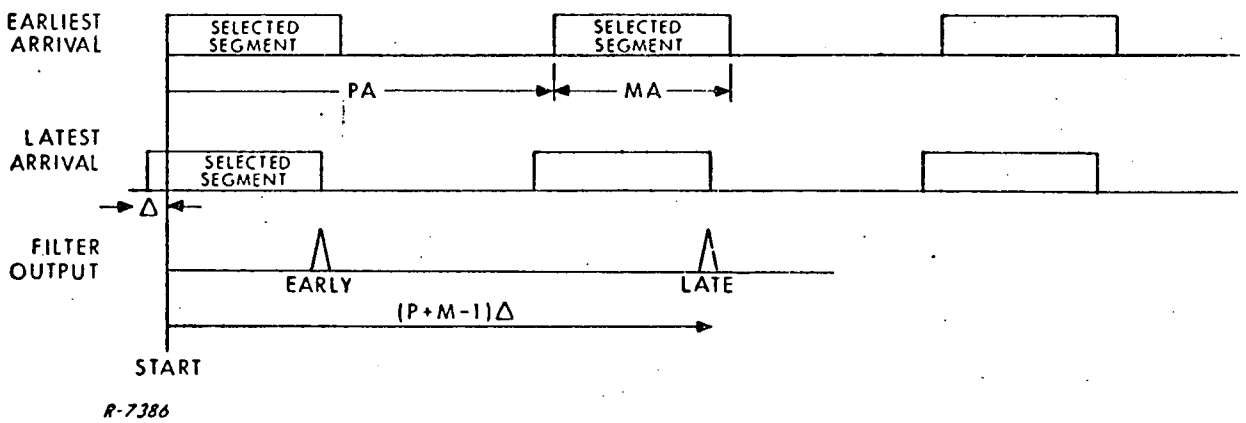
These relationships are pictured in Figure 2b, where the upper line indicates the earliest possible arrival with the selected segment identified. The next line shows the latest possible arrival with the selected segment appearing T_{unc} after its occurrence in the first line.



(a) Matched Filter Output Correlation Pulse



(b) Acquisition when $P\Delta > T_{unc}$



(c) Acquisition when $P\Delta < T_{unc}$

Figure 2 Matched Filter Acquisition

The earliest possible output correlation pulse and the latest output pulse are shown on the next line. It follows from inspection of Figure 2b that

$$\text{Max. Acquisition Time for Matched Filter} = T_{unc} + M\Delta \qquad (2)$$

Once again, even when $T_{unc} = 0$ it takes $M\Delta$ seconds to get a response.

When the code period $P\Delta$ is less than the time uncertainty, the analysis is complicated by the possibility of partial correlation. Since the selected segment recurs at the code period, the receiver may begin the acquisition process in the middle of this segment. We shall bypass this problem by demanding 100% correlation. This will tend to overestimate acquisition time because threshold crossings due to partial correlation are ignored. The worst case situation is shown in Figure 2c where the latest possible arriving sequence misses 100% correlation at the starting instant by one chip duration Δ. It can be seen that the maximum acquisition time is $(P+M-1)\Delta$ which becomes $(2P-1)\Delta$ when the integration interval equals the code period.

Comparison of Eqs. (1) and (2) or its special cases shows an improvement in acquisition time by a factor of approximately the number of chips M in the integration time.

3. HEURISTIC DEVELOPMENT OF DIGITAL MATCHED FILTER

3.1 Analog Version

Having established the motivation for matched filter acquisition in PN systems, we turn now to a discussion leading to the specific digital implementation developed by Teledyne ADCOM. As a starting point consider the straightforward analog implementation shown in Figure 3. The input IF signal is down-converted to dc with a pair of quadrature local oscillators. The matched filter is realized by a pair of tapped delay lines with appropriate PN code weighting at each tap. The sum I and sum Q outputs are the components of the complex envelope of the matched filter response.

The waveforms sketched on the right would appear at the respective outputs when the code sequence is phase-reversal modulated by data and the LO is tracking the input carrier phase. For acquisition, the sum-of-squares output can be compared to a threshold. For data demodulation, the I sum output is sampled at the pulse peak. A phase error can be derived by sampling the Q sum at the same instant. The two samples may then be applied to a Costas loop (not shown) to phase lock the LO.

3.2 I-Q Digital Version

The remainder of this section considers digital methods for obtaining equivalent I sum and Q sum outputs. For purposes of comparison we show, in Figure 4, a straightforward digital implementation consisting of quadrature mixing and A/D conversion followed by a tapped shift register bank with as many one-bit shift registers as there are bits per sample. The tap weighting indicated by the exclusive-or gates is applied to every

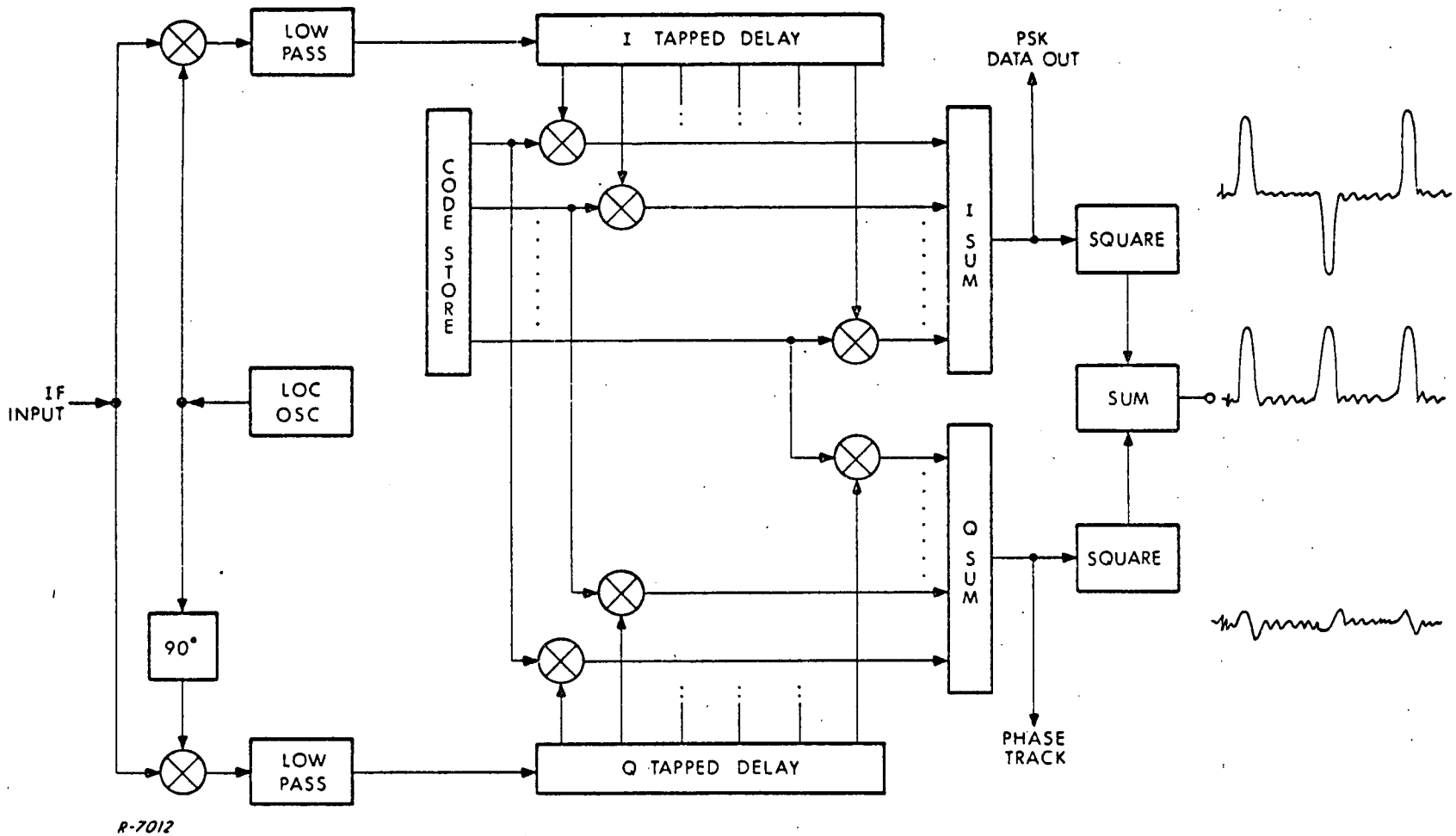


Figure 3 Lowpass Tapped Delay Line Matched Filter

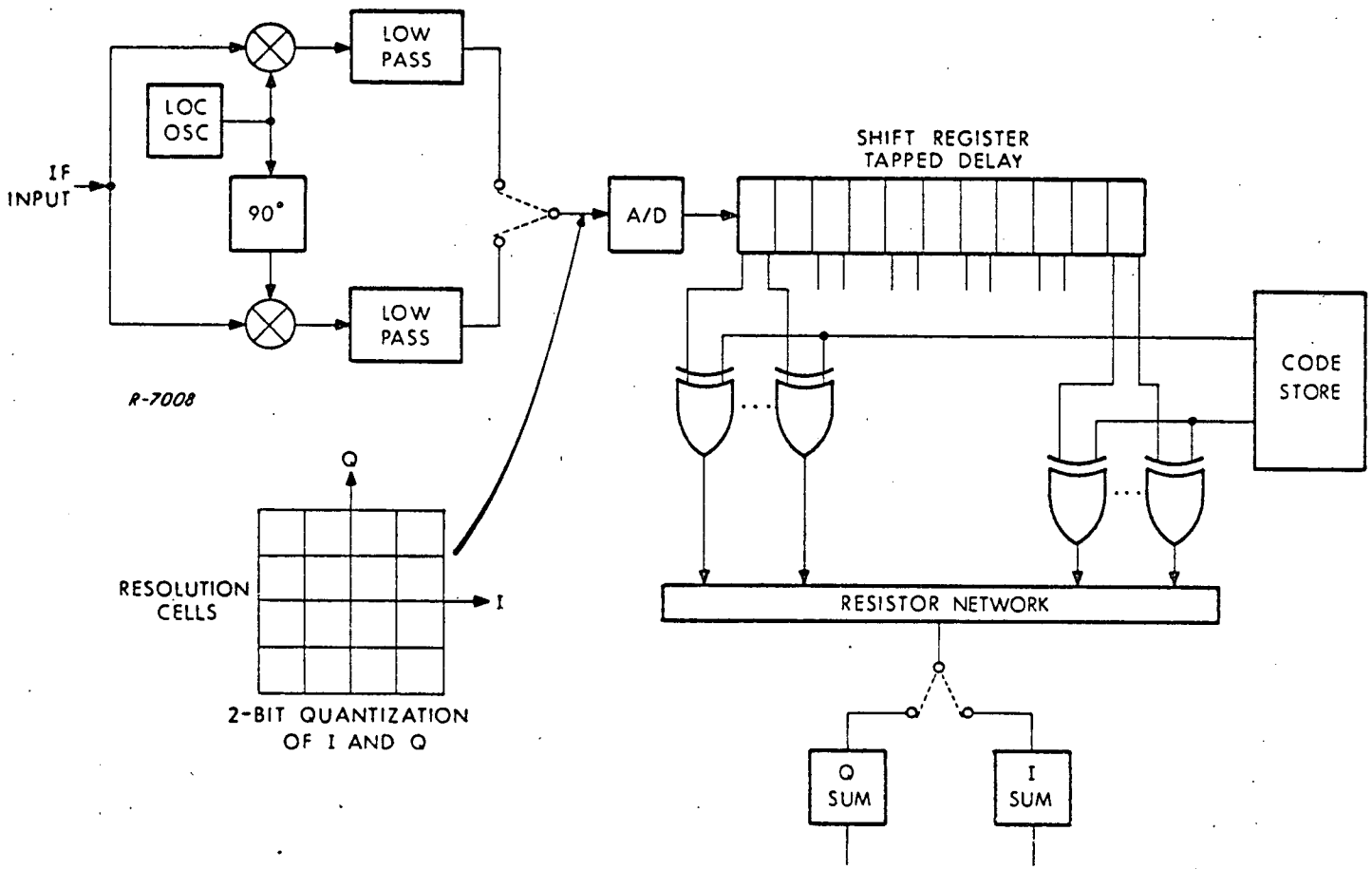


Figure 4 In-Phase/Quadrature Digital Matched Filter

other tap since both I and Q appear successively at the tapped shift-register stages. The resistor network provides D/A conversion for each tap product and also sums over the code length.

The diagram in the lower left indicates the effect of quantization on the signal resolution in the I-Q plane. For 2 bit (4 level) quantization, the signal is resolvable into one of the 16 cells. It can be seen that the resolution in phase into less than four quadrants is achieved only at the higher amplitudes and then only if the signal level falls properly within the dynamic range of the A/D converter.

3.3 Multiphase 1-Bit Version

The digital matched filter developed by Teledyne ADCOM differs from the preceding in that the resolution cell structure has the form of the circle in Figure 5, although the block diagram shown is still not the final configuration. Instead of inphase and quadrature sampling we have LO phase references at 0°, 120° and 240°, but only retain 1 bit (i.e., sign) of amplitude information. The resulting resolution cell structure is divided into angular sectors with each sector being defined by the three bits from the three phase samples, respectively. The bits are loaded successively into a shift register. Every third stage is tapped and weighted by the stored code through a single exclusive-or gate. The summed output is commutated into three storage elements corresponding to the three phase references. The final step is a trigonometric transformation which brings the output back into the conventional I-Q form. The details of the trigonometric transformation are given in Appendix A. The system shown in Figure 5 would behave very nearly like an ideal matched filter preceded by a limiter.

Although the illustrations pertain to the simplest case of three phases, the principles apply to any odd number of phases. Even numbers

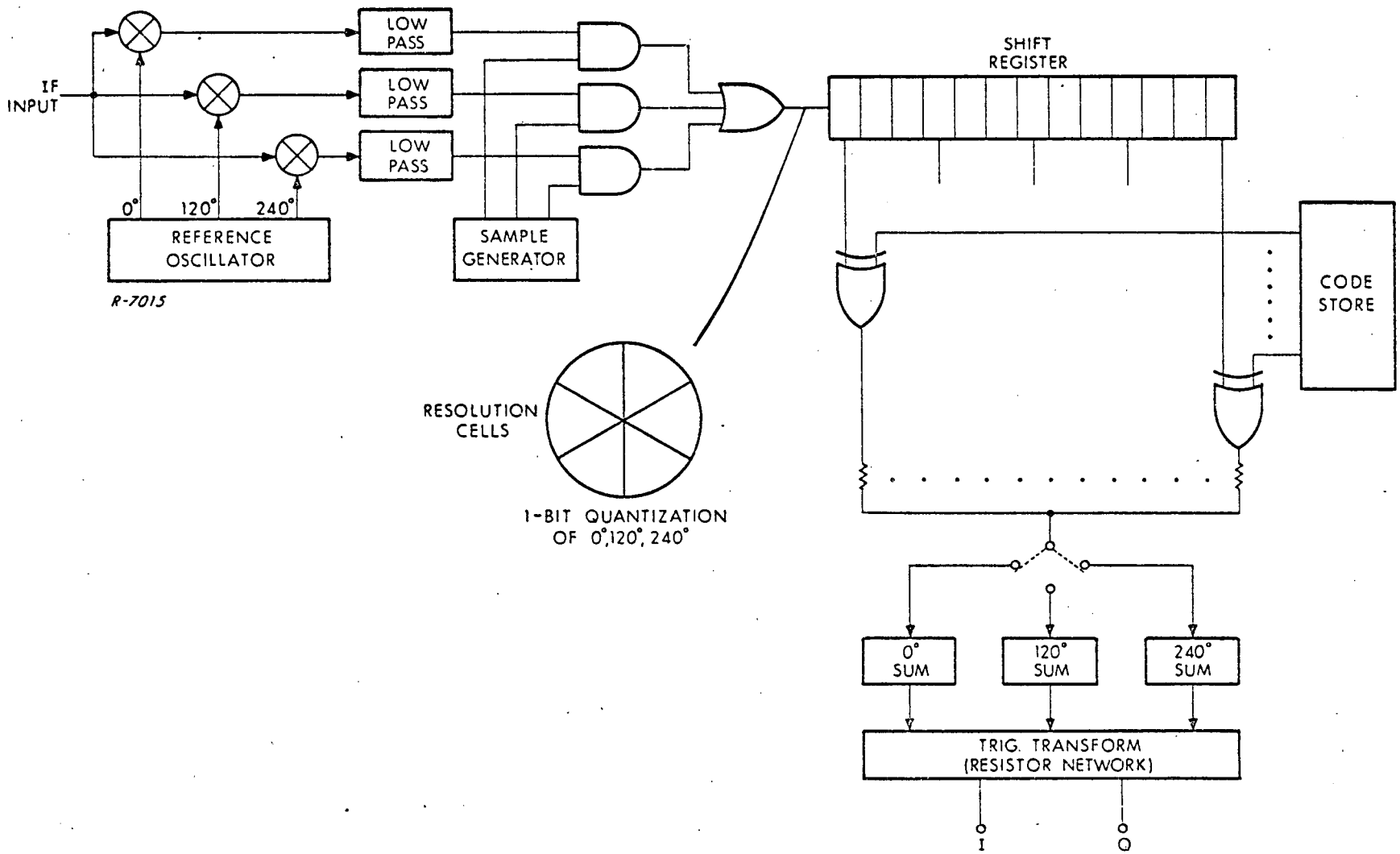


Figure 5 Multiphase One-Bit Sample Digital Matched Filter

of phases are not suitable since 180° phase shifts lead to non-independent samples. The implemented digital matched filter breadboard has the capability of three (0°, 120°, 240°) or five phases (0°, 72°, 144°, 216°, 288°).

3.4 Sampling Time Considerations

In the digitization process care must be taken as to where the sampling instants fall with respect to chip transitions. The sampler is generally preceded by a lowpass or equivalent bandpass filter approximately matched to the chip rate bandwidth. This ensures maximum SNR at the sampling instant provided the sample is properly located in time. The situation is illustrated in Figure 6 for a chip transition having passed through a simple RC lowpass filter. The filter output analog waveform would have the indicated exponential rise and fall. The optimum sampling instant is, of course, just prior to the next transition. However, during acquisition, chip rate synchronism is not yet achieved and the samples could just as well fall in the early part of a chip where the SNR is poor. To guard against the latter possibility, one must resort to multiple samples per chip. In the case of I-Q samples two pairs of samples can be taken during each chip interval. The resultant digital data can then be processed to minimize the loss due to non-synchronism (Figure 6, second line).

With multiple-phase samples a further option is available. Ignoring for the moment the 1-bit quantization, we observe that the multi-phase representation, e.g. 0°, 120°, 240°, is redundant since only two independent components (not necessarily orthogonal) are sufficient to define a phasor. Thus, while ideally the three samples should occur at the point of maximum SNR, they can be distributed through the bit interval, as shown on the bottom of Figure 6, with little degradation. Since each sample is the result of a phase-shift by the same amount from its neighbors, any triplet can be regarded as spanning a hypothetical chip interval. This feature has important implications in the ultimate implementation.

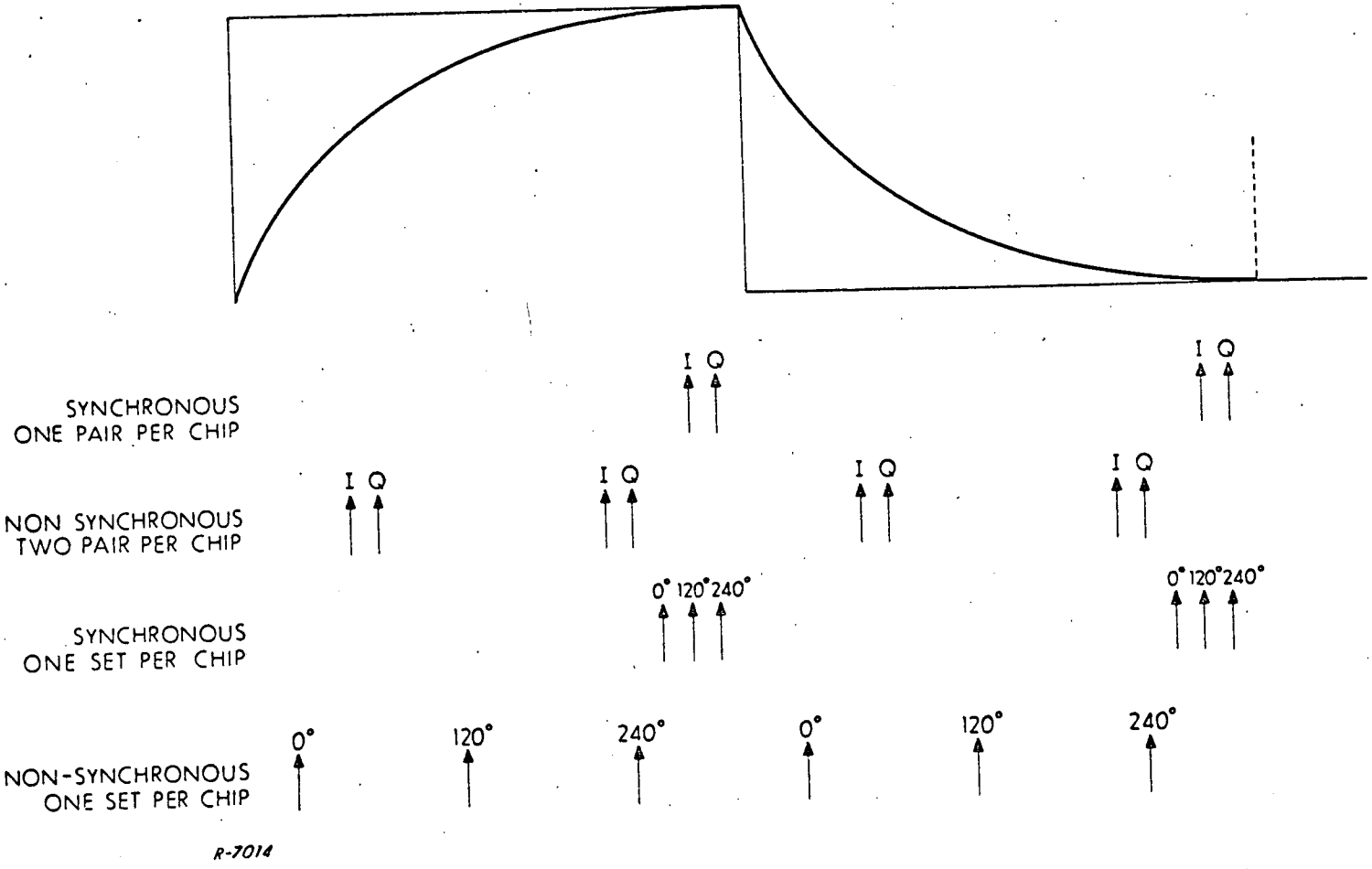


Figure 6 Relationship of Samples to Filtered PSK Sequence

The above reasoning of three distributed phase samples during a chip interval applies, of course, also to five multiphase samples.

3.5 Direct IF Sampling

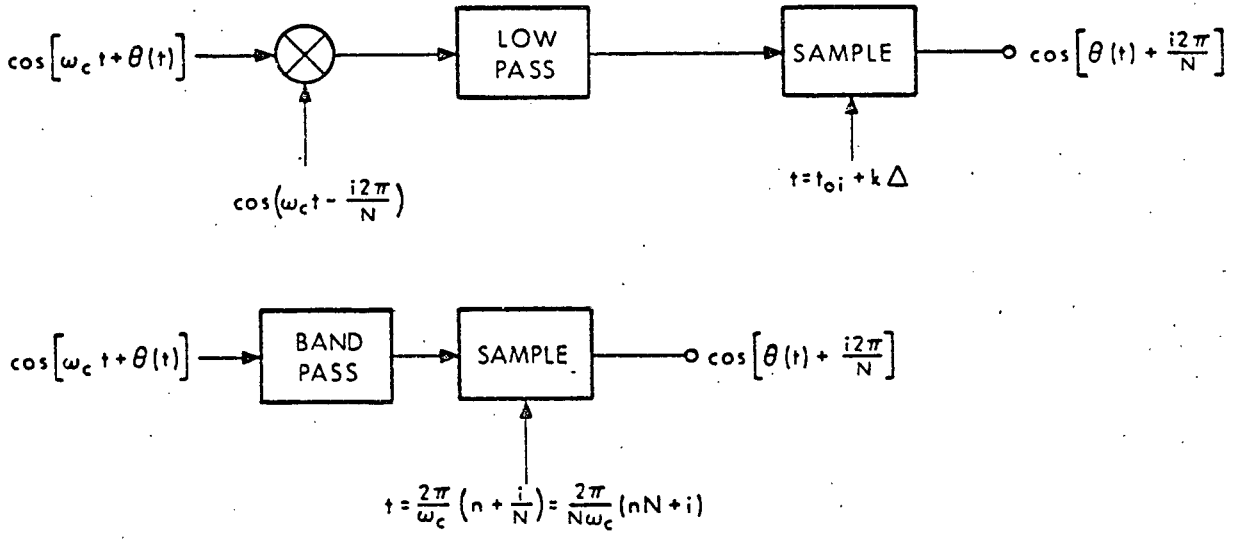
The final concept to be explained before describing the actual implementation is a direct IF sampler and digitizer that replaces the multiple mixes and lowpass filter configuration in Figure 5. The principles of direct IF sampling are indicated in Figure 7. The upper diagram shows the conventional down-conversion with an appropriate phase reference LO. The PN modulation is represented by $\theta(t)$, N is the number of phases being sampled and Δ is the chip interval. After lowpass filtering samples are taken at intervals Δ to yield the desired i'th phase sample.

In the lower diagram a bandpass filter is used for noise rejection and samples of the IF signal are taken at precisely defined instants. The sampling time is an integer multiple n of the nominal IF period plus a fraction $\frac{i}{N}$ of the period according to which sample is required. Sampling the IF directly in this manner produces the same result as down-conversion and sampling.

We observe that the sampling instant

$$t = \frac{2\pi}{N\omega_c} (n\,N + i)$$

is an integer multiple of the period corresponding to N times the nominal IF frequency ω_c. The sampling strobes can therefore be generated by dividing down a clock running at $N\omega_c$. By choosing the divide ratio appropriately it is possible to obtain the N phases at successive sampling instants distributed through the chip interval. A divide ratio of Np + 1 has the desired property where (Np + 1) is the number of IF cycles per chip. This can be



N = NUMBER OF PHASES = NUMBER OF SAMPLES PER CHIP

Δ = CHIP DURATION

$(nN+i) = s[Np+1]$ $\quad Np+1=f_c\Delta$ = NUMBER OF IF CYCLES PER CHIP

R-7007

Figure 7 Direct IF Sampling Relations

demonstrated as follows: The successive sampling instants starting at t = 0 are

$$
\begin{array}{lcll}
 & 0^\circ & 0 & \\
\frac{1}{N} \cdot 360^\circ & : \frac{2\pi}{N\omega_c}(Np+1) & = \frac{2\pi}{\omega_c}\left(p+\frac{1}{N}\right) & \approx \frac{1}{N}\Delta \\
\frac{2}{N} \cdot 360^\circ & : \frac{2\pi}{N\omega_c} 2(Np+1) & = \frac{2\pi}{\omega_c}\left(2p+\frac{2}{N}\right) & \approx \frac{2}{N}\Delta \\
\vdots & \vdots & \vdots & \\
\frac{N-1}{N} \cdot 360^\circ & : \frac{2\pi}{N\omega_c}(N-1)(Np+1) & = \frac{2\pi}{\omega_c}\left((N-1)p+\frac{N-1}{N}\right) & \approx \frac{N-1}{N}\Delta \\
\frac{N}{N} \cdot 360^\circ \rightarrow 0^\circ & : \frac{2\pi}{N\omega_c} N(Np+1) & = \frac{2\pi}{\omega_c}(Np+1) & = \Delta
\end{array}
$$

We are now in a position to proceed to a description of the bread-board implementation.

4. DIGITAL MATCHED FILTER IMPLEMENTATION

4.1 General Description

A simplified block diagram of the digital matched filter for three-phase sampling is shown in Figure 8. The IF input goes through a bandpass filter and limiter to become data for a shift-register. A 3×IF oscillator is divided down to yield the shift-register clock. As explained in the previous section the clock samples the data at the appropriate instant for the successive multiphase samples.

The shift-register is tapped at every third stage for multiplication in an exclusive-or by the stored code. The results are added in a resistive summer. Two previous sums are stored in Sample-and-Hold circuits. A second resistive network combines the current and two previous sums to recover the I-Q components. A new output is produced every clock cycle, i.e., three times per chip. Every third such output corresponds to correctly framed chip transistions and is therefore a valid point on the correlation function. The intervening outputs correspond to overlap conditions. The sketch in the lower right of Figure 8 shows a hypothetical output waveform as a function of time in the vicinity of the correlation peak.

The entire processing sequence is illustrated in Figure 9 for a short code of five chips. The upper two lines are the IF and 3×IF references, respectively. There are seven IF cycles per chip hence the divide ratio is seven which has the required form ($7 = 3 \times 3 + 1$). The $\frac{3}{7}$ IF clock is seen to coincide successively with the 0°, 120° and 240° phases of the IF. The input PSK is shown on a carrier shifted 90° with respect to the local reference. Sampling the PSK signal produces the indicated sequence of +, - and ?. The ? denotes an ambiguous situation where the sampling strobe falls at a zero crossing of the input PSK signal. The samples are multiplied

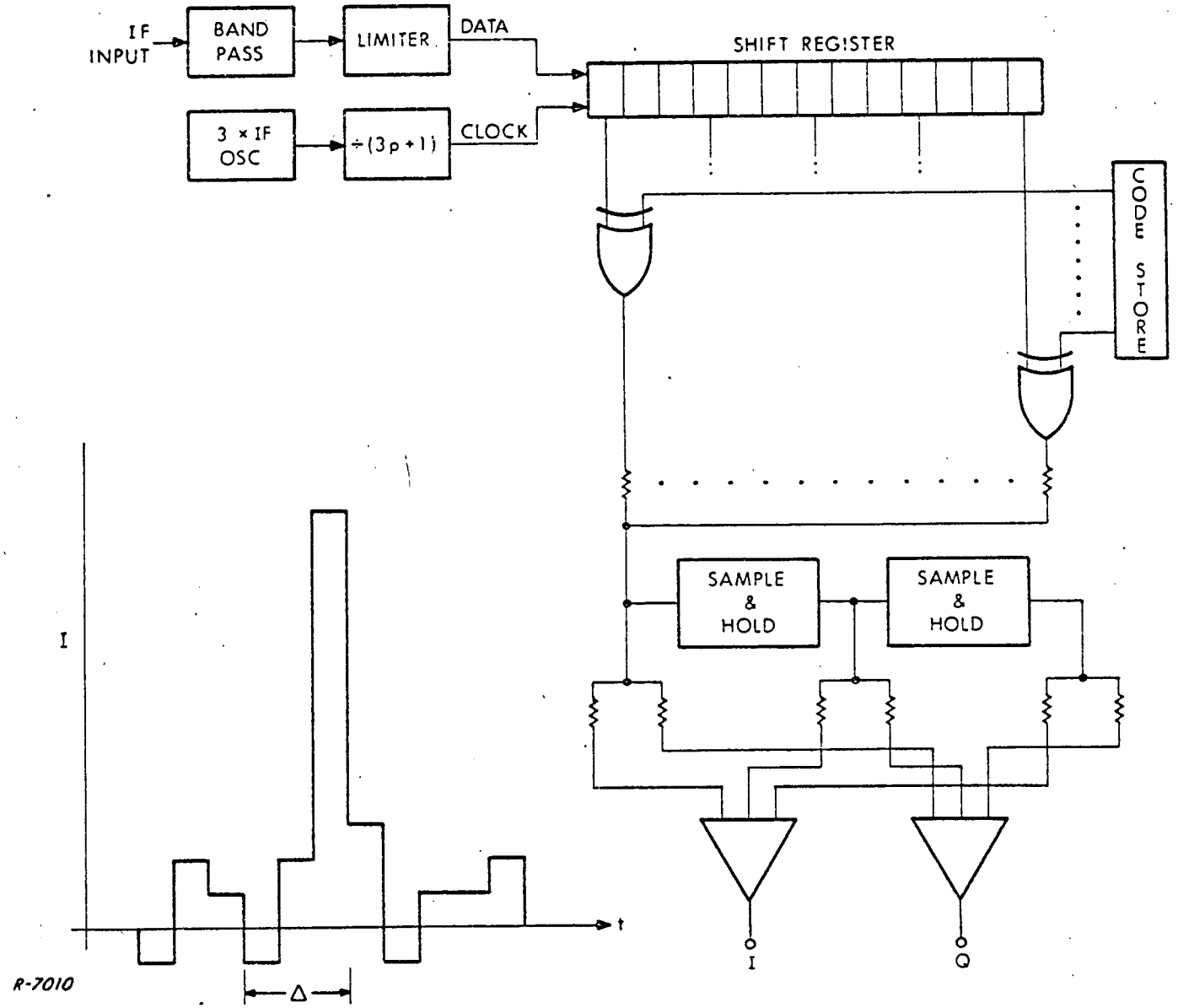


Figure 8 Direct IF Sampling Multiphase Digital Matched Filter

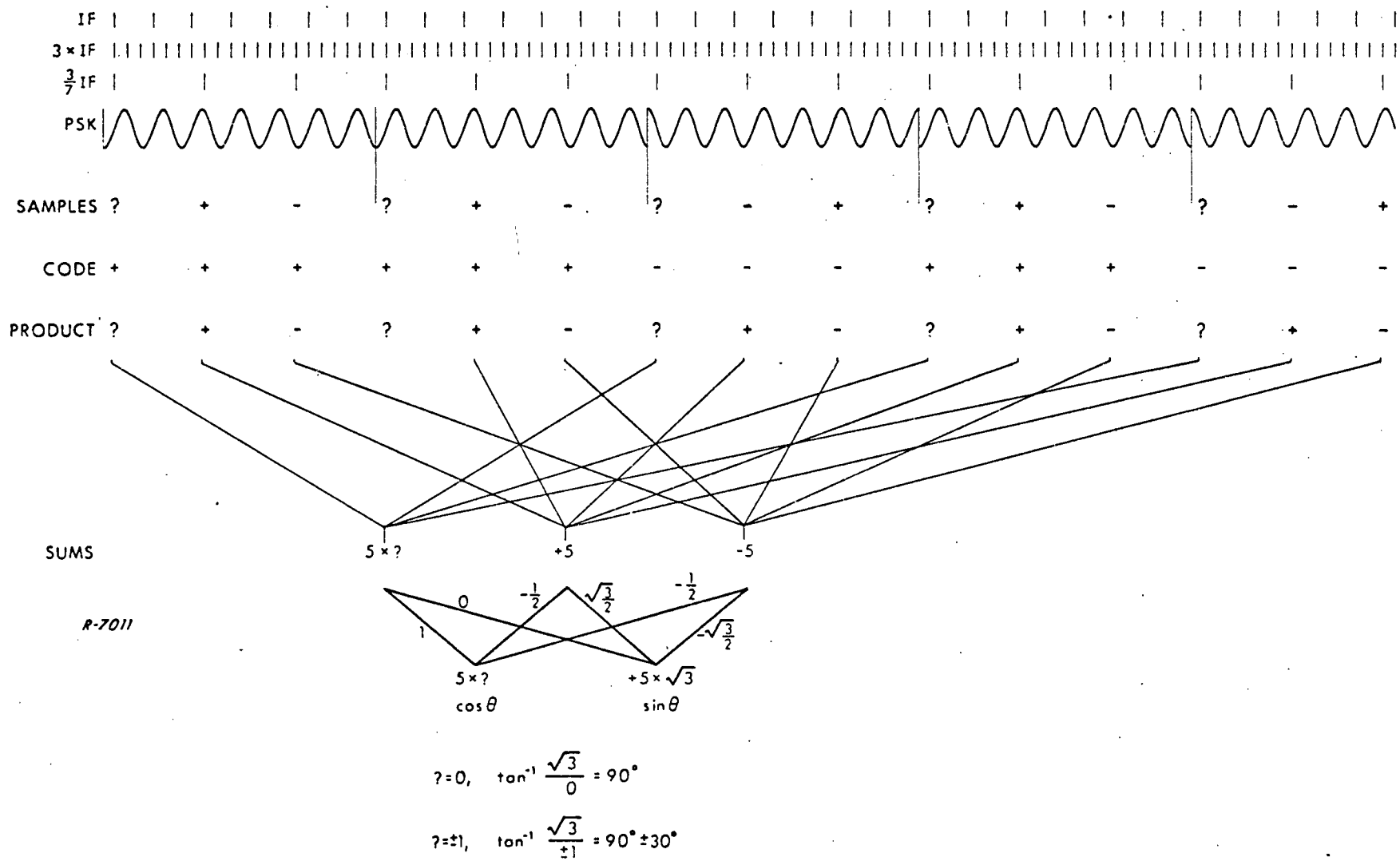


Figure 9 Direct IF Sampling Waveforms

by a code of the form +, +, -, +, -. The sample-and-hold is implicitly indicated by applying the same code element to three successive phase samples. The products are summed for each of the three phases, respectively, and the sums are combined in a trigonometric transformation consisting of sines and cosines of 0°, 120° and 240°. The final I-Q outputs are

$$\cos\theta = 5 \times ?$$

$$\sin\theta = 5 \times \sqrt{3}$$

where θ is phase angle between the received PSK and the local reference. By assigning specific values to ?, phase estimate may be derived. When ? = 0, i.e., equal number of +'s and -'s in the ambiguous cases, $\theta = 90°$ which agrees with the actual phase. When the ambiguous cases are all + or all -, the indicated phase is 90°+30° or 90°-30°, respectively. This result is consistent with the expected resolution in phase for three phase sampling (see Figure 5).

4.2 Summary of Digital Matched Filter Features

The significant advantages of the Teledyne ADCOM digital matched filter can be understood with reference to Figure 8.

1. The direct IF sampling eliminates the need for mixers and lowpass filters.
2. The IF limiter - a consequence of 1-bit A/D conversion - makes the operation virtually insensitive to input signal level.
3. Only 3 or 5 bits per chip need to be processed as compared to at least 8 for competing approaches. The 8 bits are comprised of (2 I-Q channels) (2 samples/chip) (2 bits/sample).
4. The sequential processing allows one set of exclusive-or gates to serve all multiple phase samples.
5. The complete computation cycle at 3 or 5 times the chip rate permits time resolution for acquisition to 1/3 or 1/5 the chip duration.

4.3 Detailed System Implementation

In this section we describe the implementation details of the digital matched filter including the auxiliary circuits required to test the device. A block diagram of the breadboard is shown in Figure 10. Various switching options and access points have been built into the system to permit flexible operation under conditions other than those specified.

4.3.1 IF Section

The balanced mixer at the upper left produces a PSK modulated signal. One input is a pseudo-noise code at 100 kHz chip rate and the other is the 1.6 MHz IF carrier. The mixer output is coupled back into the system through external ports to permit insertion of an attenuator for SNR adjustment. The PSK signal may be combined with external noise or interference through a resistive summing junction. Then follows a 4th order Butterworth IF bandpass filter selected from one of two plug-in modules. The noise bandwidths are 200 kHz or 300 kHz. These filter bandwidths were chosen on the basis of transient response to a phase reversal input. A narrower filter, e.g., 150 kHz would lead to an excessively long transient. This would produce inter-symbol interference and would cause errors in samples distributed through the chip interval.

The bandpass filter is followed by a limiter (Schmitt trigger) that produces a logic compatible two-state output. (The Schmitt trigger may require occasional zero setting in accordance with the procedure of Appendix B.)

4.3.2 Matched Filter Section

The limited IF is strobed into the data shift register at instants defined by the clock. The clock generation (300 kHz or 500 kHz) is discussed in Section 4.3.3. The shift register is tapped at specific stages and the outputs are applied to exclusive-or gates. A switching

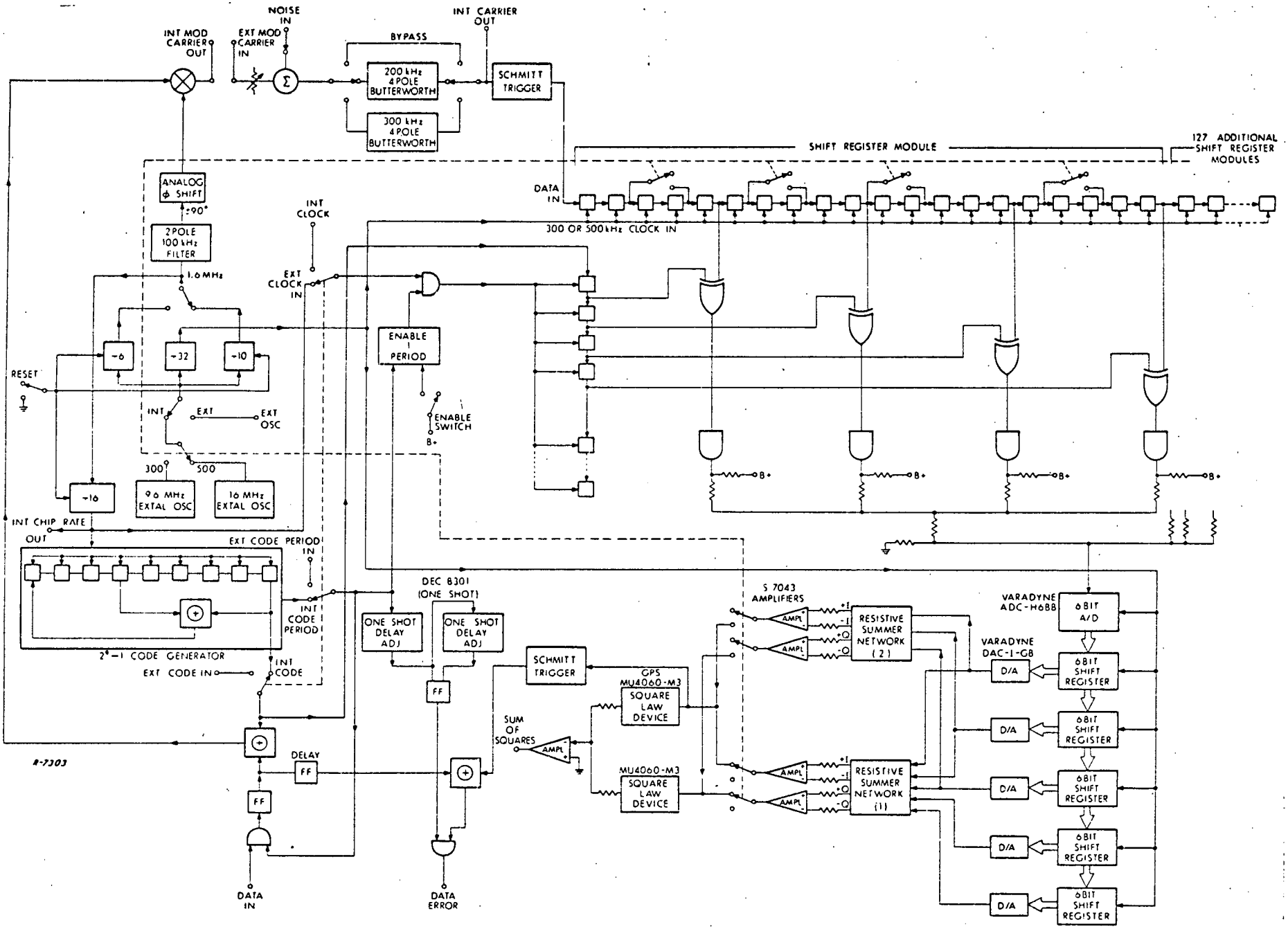


Figure 10 Digital Matched Filter Block Diagram

option allows intermediate stages of the shift register to be bypassed so that the tap spacing is either 3 or 5 stages.

The other inputs to the exclusive-or gates come from a code storage register which is previously loaded with the desired code sequence. The gate outputs are summed through drivers in a resistor network.

The sample-and-hold function on the sums (see Figure 8) is performed digitally by means of an A/D converter and five holding registers. At each clock cycle the contents of each register are transferred to the succeeding one. The outputs of the registers go to D/A converters and then to a resistor network for trigonometric transformation into I-Q form. Two such networks and associated op amps are provided for 3 phase and 5 phase operation. The selected I component contains the data modulation which was applied as phase-reversal or complementation of the entire code period. The sign of the I component is extracted by a Schmitt trigger circuit for subsequent comparison with the input data. (The Schmitt trigger may require occasional zero setting in accordance with Appendix B.) The data sampling, comparison and error count processes are described in Section 4.3.3.

The envelope of the matched filter output is derived by summing the squares of the I and Q components.

4.3.3 Clock, Code and Data Generation

Timing for the system is derived from one of two oscillators, 9.6 MHz or 16 MHz. Provision has also been made for the insertion of an external oscillator. The IF at 1.6 MHz is generated by dividing the oscillator frequencies by 6 and 10, respectively. The selected oscillator is also divided by 32 to produce the sampling clock frequencies of 300 kHz or 500 kHz. This procedure is equivalent to division of a 3×IF or 5×IF by 16

where 16 = 3×5+1 has the correct form for both 3- and 5-phase sampling. The reason for the additional factor of 2 is to create symmetrical square-waves out of the divider.

A 1.6 MHz phase shifter on the LO input to the mixer provides an adjustment for phasing the input signal so that the I component at the output of the matched filter is a maximum. Thls then corresponds to the coherent operation under which tests were conducted.

A further division of the 1.6 MHz IF reference by 16 yields the chip-rate frequency of 100 kHz. It has been found that for consistent operation all the dividers in the timing generation must be reset to the same initial conditions when the system is turned on after a mode change. A reset button on the front panel accomplishes this function.

A 9-stage code generator driven by the 100 kHz chip-rate clock produces a 511 chip maximal-length PN sequence. The generator also puts out a code period pulse at the code repetition rate, i.e., every 511 chips. Provisions have been made for external insertion of code sequences and code period pulses. The 100 kHz chip-rate clock is made available at an output terminal for the purpose of driving an external code generator.

The code period pulse serves several functions. It enables a gate in the lower left so that a flip-flop may be set by the input data. The data value is modulo-2 added (⊕) to the code sequence for one complete code period, thereby complementing or not complementing the code in accordance with the data. The data delayed by one period is compared in a modulo-2 adder with the output from the I component of the matched filter. Whenever the two data values disagree an error count is registered. However, the output of the matched filter is meaningful only at the instant of peak correlation. This event recurs at the code period and the code period pulse is used to derive a strobe that samples the data error at the right time. The strobe is developed by two successive one-shot delays

whose outputs set and reset a flip-flop. The delay through the first one-shot is adjusted to compensate for delays through the processor. The second one-shot defines the strobe width.

The final function of the code period pulse is to enable the loading of the code storage register. When the front panel enable button is pressed the code sequence from the generator is clocked into the storage register for one code period. An external or internal clock may be used to load the code register. Its contents then remain fixed until the code is to be changed. The register must be reloaded whenever the system is turned on.

5. SYSTEM OPERATION

A photo of the front panel of the digital matched filter is shown in Figure 11. The switches and terminals have the following functions:

OSC INT or EXT	Switch to select internal or external reference oscillator.
EXT OSC IN	Connector for external oscillator.
CODE INT or EXT	Switch to select internal or external code generator.
EXT CODE IN	Connector for external code.
EXT CODE PER IN	Input connector for code period pulse from external code generator. Output for code period pulse to synchronize oscilloscope when system is in CODE INT mode.
LOAD CODE	Pushbutton to load code into storage register.
EXT CLOCK IN	Connector for external clock to be used only to load external code into storage register.
RESET	Pushbutton to initialize dividers in timing section.
SELECT 300 or 500	Selects 300 kHz or 500 kHz clock corresponding to 3-phase or 5-phase sampling.
DATA IN	Connector for data input.
NOISE IN	Connector for additive noise or interference at IF.
EXT MOD CARRIER IN	Connector for signal input at IF.
INT MOD CARRIER OUT	Connector for output from IF signal generator. This terminal is connected to EXT MOD CARRIER IN by means of a jumper cable through an external attenuator.

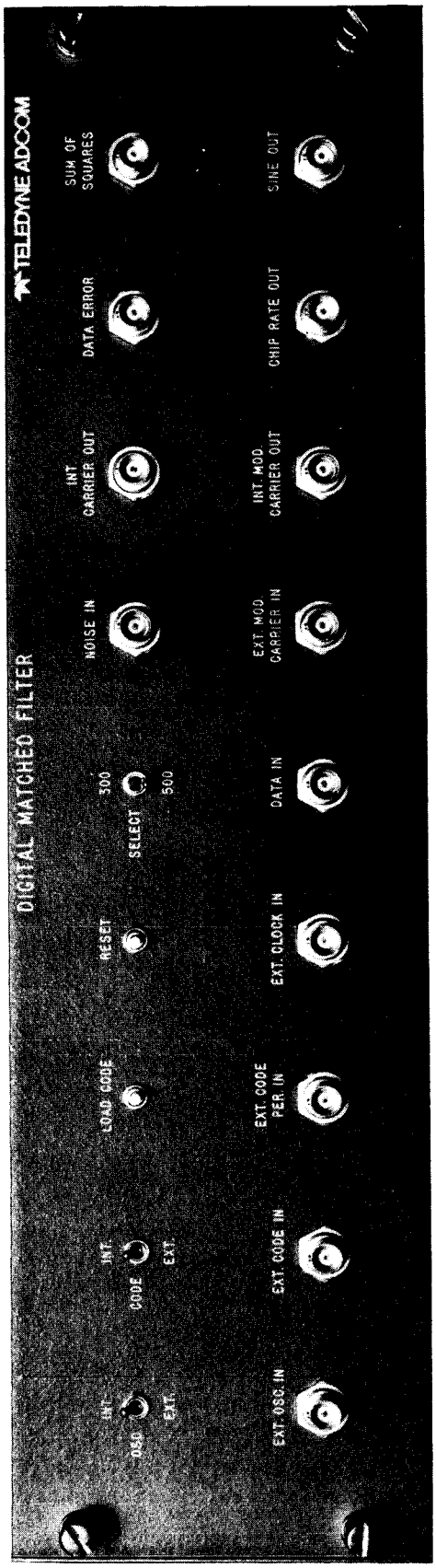


Figure 11 Digital Matched Filter Front Panel

INT CARRIER OUT	Connector tied to bandpass filter output for purposes of SNR measurement.
DATA ERROR	Output for data error to be connected to error counter.
CHIP RATE OUT	Connector for chip-rate clock output to drive external code generator.
SUM OF SQUARES	Connector for matched filter output envelope.
SINE OUTPUT	Connector for matched filter output in-phase (I) component.

The setup for experimentation is shown in Figure 12. A random data source, e.g., a noise source or a squarewave generator whose frequency is non-synchronous with the code repetition rate, is connected to the DATA IN port. The INT MOD CARRIER OUT is passed through a calibrated attenuator and connected to the EXT MOD CARRIER IN. A source of noise or interference is connected to the NOISE port. Signal-to-noise ratio measurements are made at the output of the filter of known noise-bandwidth which is accessible at the INT CARRIER OUT terminal. The combined signal and noise at the output of the filter should be at least -30 dBm.

The DATA ERROR output is applied to a counter which can be started and stopped by manual control or by a timer with a capability up to two minues.

To begin an experiment, insert the appropriate card for the desired IF filter bandwidth. Select clock rate 300 kHz (3 phase) or 500 kHz (5 phase). Load code register by pressing LOAD CODE button. Depress

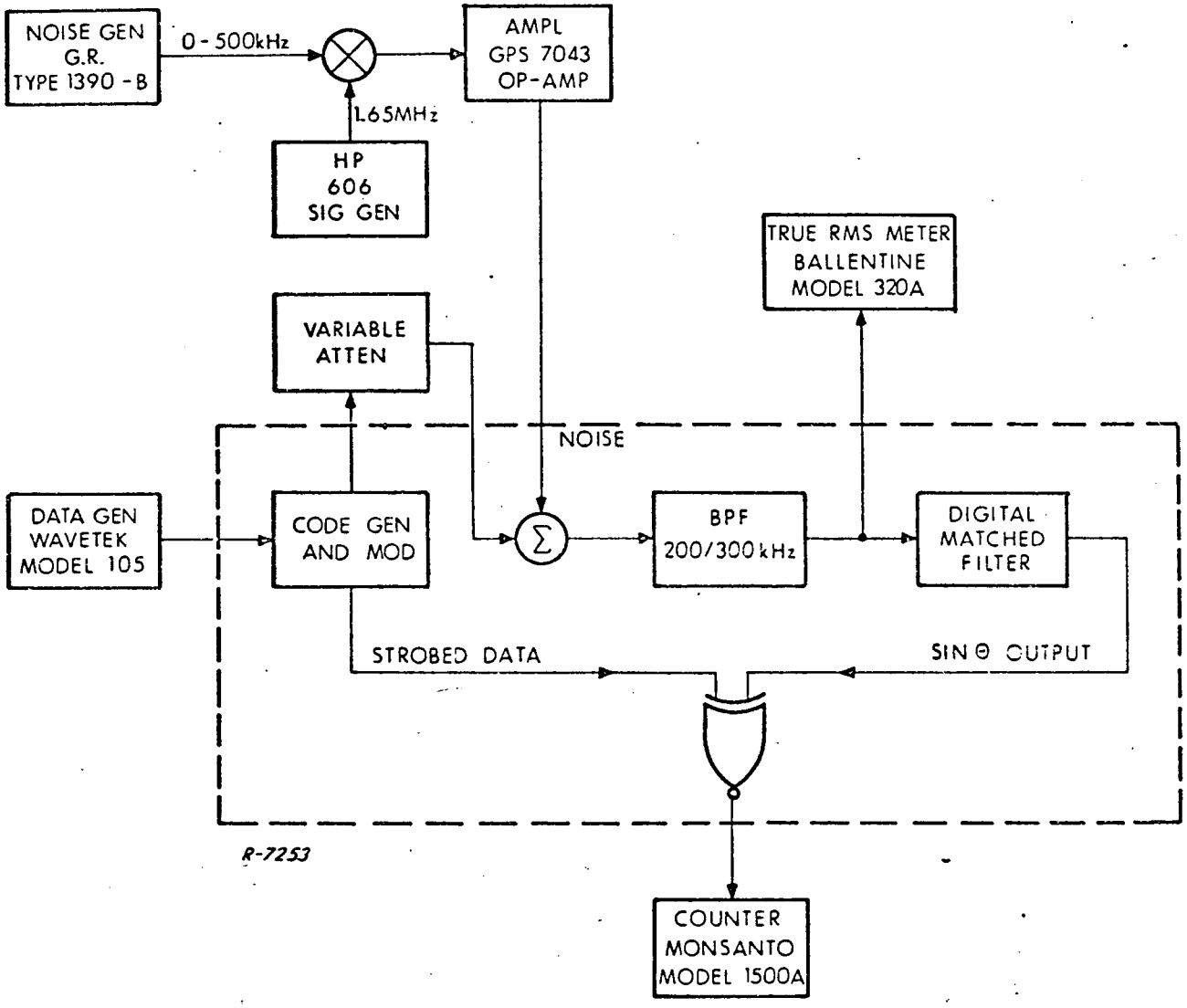


Figure 12 Experimental Test Setup

RESET button. To verify correct operation connect SINE output and SUM SQUARES output to dual trace oscilloscope synchronized to the code period from the EXT CODE PER IN terminal. Patch in signal but omit noise and data. The scope should show a positive or negative peak on the SINE trace that coincides with the peak on the SUM OF SQUARES. To optimize performance adjust phase control (knurled knob inside chassis) to maximize SINE output at the appropriate point.

Now connect data source and set up desired signal and noise conditions in the bandpass filter. Record error count for appropriate length of time to ensure statistically significant results.

6. TEST RESULTS AND COMPARISON WITH THEORY

6.1 Noise Interference

Two kinds of tests were conducted with the digital matched filter: noise and CW interference. Gaussian noise of uniform spectral density in the band of interest was added to the input signal. The theoretical performance under these conditions is governed by the well known error probability for coherent PSK shown in Figure 13. The abscissa is expressed as the ratio of energy E to noise-power density N_o. In terms of system parameters

$$\frac{E}{N_o} = \left(\frac{S}{N}\right)_{in} B_n M\Delta$$

where $(S/N)_{in}$ is the SNR in the IF filter of noise-bandwidth B_n and $M \cdot \Delta$ is total signal duration. For the case at hand M=511, $\Delta = 10^{-5}$ sec and B_n = 200 kHz or 300 kHz. The dB value that must be added to $(S/N)_{in}$ to yield E/N_o is 30 dB and 32 dB for B_n = 200 kHz and 300 kHz, respectively.

Since the data rate is $10^5/511$ bits/sec, the conversion from errors per minute to errors per bit is

$$Pe = \frac{511}{105} \times \frac{1}{60} \left(\frac{Err}{min}\right) = 0.85 \times 10^{-4} \left(\frac{Err}{min}\right)$$

The raw data taken during the acceptance test procedures is given in Appendix C. The data are plotted in Figures 13-18.

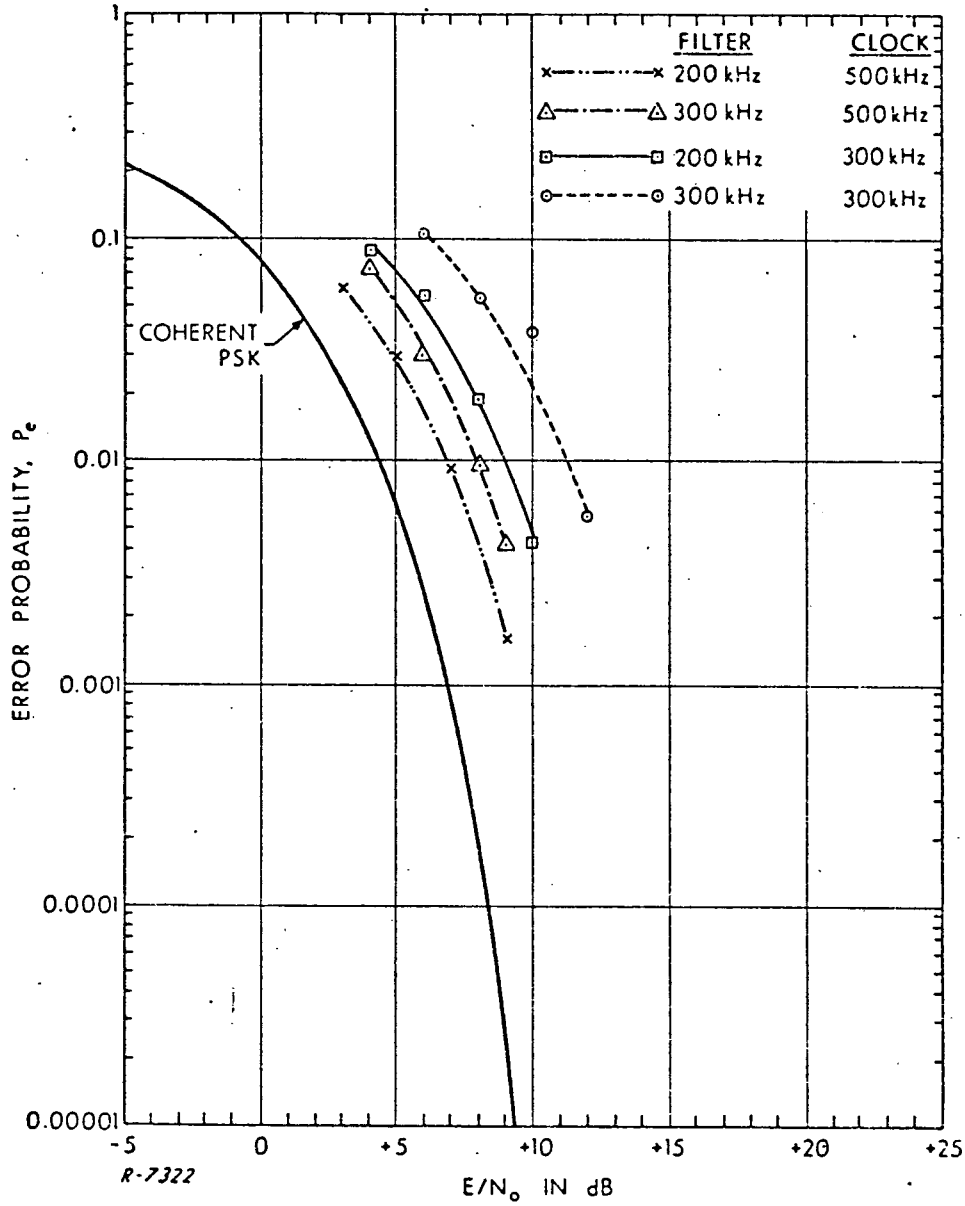


Figure 13 Error Rates for Noise Interference with External Code

Two code options were available. The Internal Code is the 511 chip maximal length sequence produced by the PN generator. The External Code is an all "1"s code corresponding to no spectrum spreading. Under noise interference the theoretical optimum performance of Internal and External codes is the same since the parameter E/N_o is the same for both. However, there is a difference in actual performance due to the effect of the pre-selector bandpass filter on the Internal Code signal. At every chip transition the filter introduces transients (inter-symbol interference) which tend to cause perturbations in the phase samples distributed through each chip. In the absence of code transitions (i.e., External Code) the transients occur at the data rate ($\sim$200 Hz) or less and may be ignored.

The best performance against noise was achieved for 500 kHz clock (5 phase samples) and 200 kHz pre-selector filter. At an error rate of 10^{-2}, the test results were within less than 3 dB of theory for external (no) code (Figure 13) and within 3.5 dB for the maximal length interval code (Figure 14). When the bandpass filter was widened to 300 kHz with the same 500 kHz clock, the performance degraded by about 1 dB in both cases. These results indicate that the degradation due to filter transients, i.e. inter-symbol interference, is slightly more than 0.5 dB. Within the accuracy of the measurements, the loss attributable to filter transients is the same for the two filters.

With a clock rate of 300 kHz (3 phase samples) and the 200 kHz filter, the tests showed about 4.5 dB departure from theory for External Code and 6 dB for Internal Code. The effects of chip transition transients amount to 1.5 dB. A narrower filter would be expected to show in even greater loss. Using the wider 300 kHz filter the deviation from optimum was nearly 6.5 dB for both Internal and External Code. The differences in inter-symbol interference effects between the two codes do not show up apparently because the additive noise is the dominant factor when the wider filter output is sampled at the lower rate of 300 kHz (3 samples per chip).

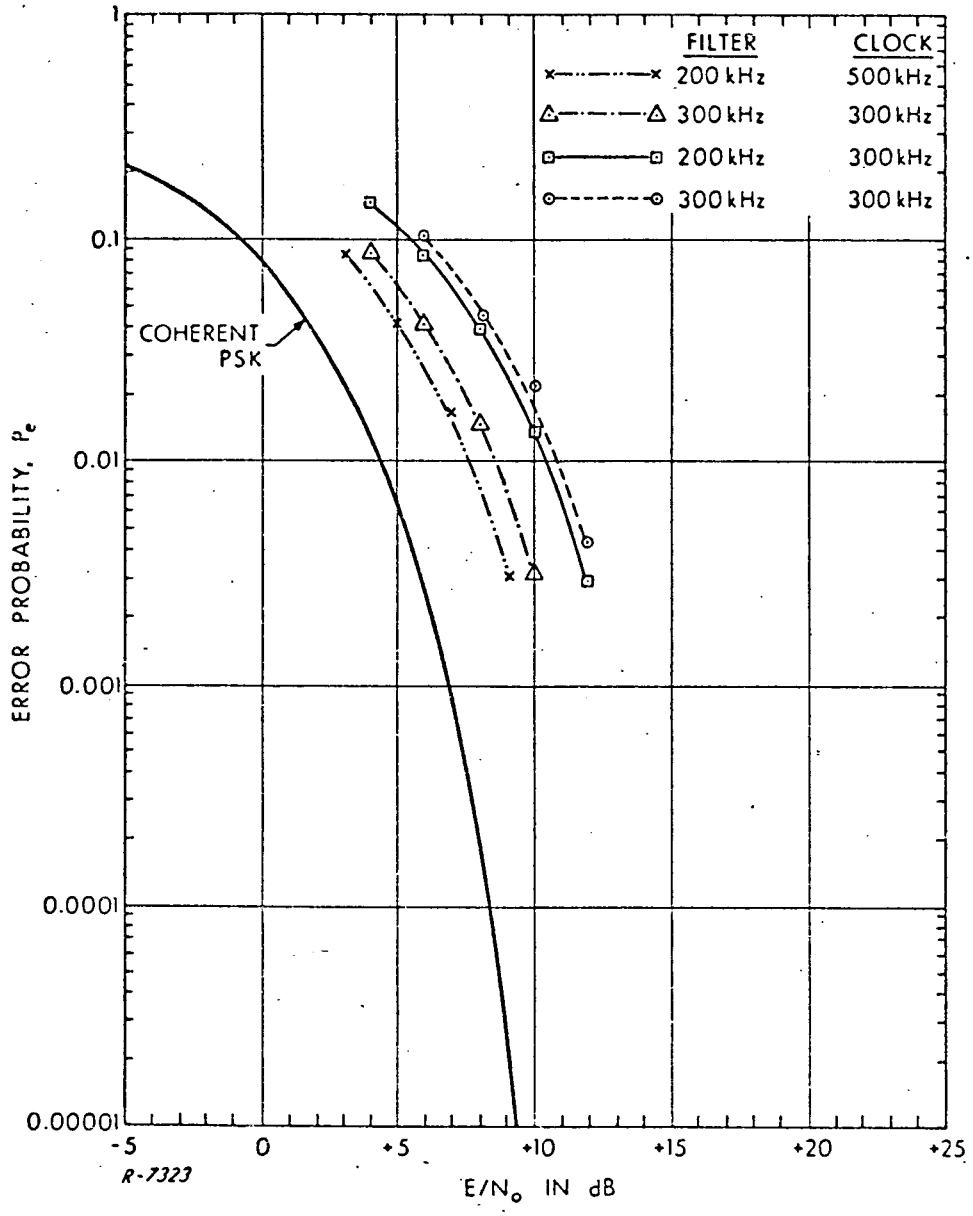


Figure 14 Error Rates for Noise Interference with Internal Code

6.2 CW Interference

The theoretical performance of an optimum matched filter with CW interference rests on a less solid foundation than with noise. Without spectrum spreading the error rate for coherent PSK with CW interference at band center is

$$Pe = \frac{1}{\pi} \cos^{-1} \sqrt{\frac{S}{I}}$$

where S/I is the signal-to-interference ratio.

When the data is carried on a PN sequence, the performance depends on the details of the cross-correlation properties of the code with the specific interference frequency. It can be argued, however, that when CW interference is passed through a matched filter or correlator, it is converted to noise if the number of chips in the code is large so that the central limit theorem applies. The error rate is then dependent only on the equivalent signal-to-noise ratio at the filter or correlator output. This procedure is justified in the present case of 511 chips. The SNR at the output of the filter, corresponding to E/N_o in the case of noise, is $M \frac{S}{I}$ where M is the processing gain or number of chips in the code. For comparison with theory in the CW case the coherent PSK error rate is plotted vs. $M \frac{S}{I}$ as shown in Figures 15-18.

The CW test results were taken at various frequencies within the IF band. The error rate varied considerably due to the above-mentioned specific code cross-correlation effects. The dependence of the results on filter bandwidth and number of phase samples are somewhat different than with noise. The wider filter bandwidth does not affect the level of CW interference but does improve the signal due to less inter-symbol interference. The difference between clock rates (number of phase samples) is hardly significant in the light of the error rate variations.

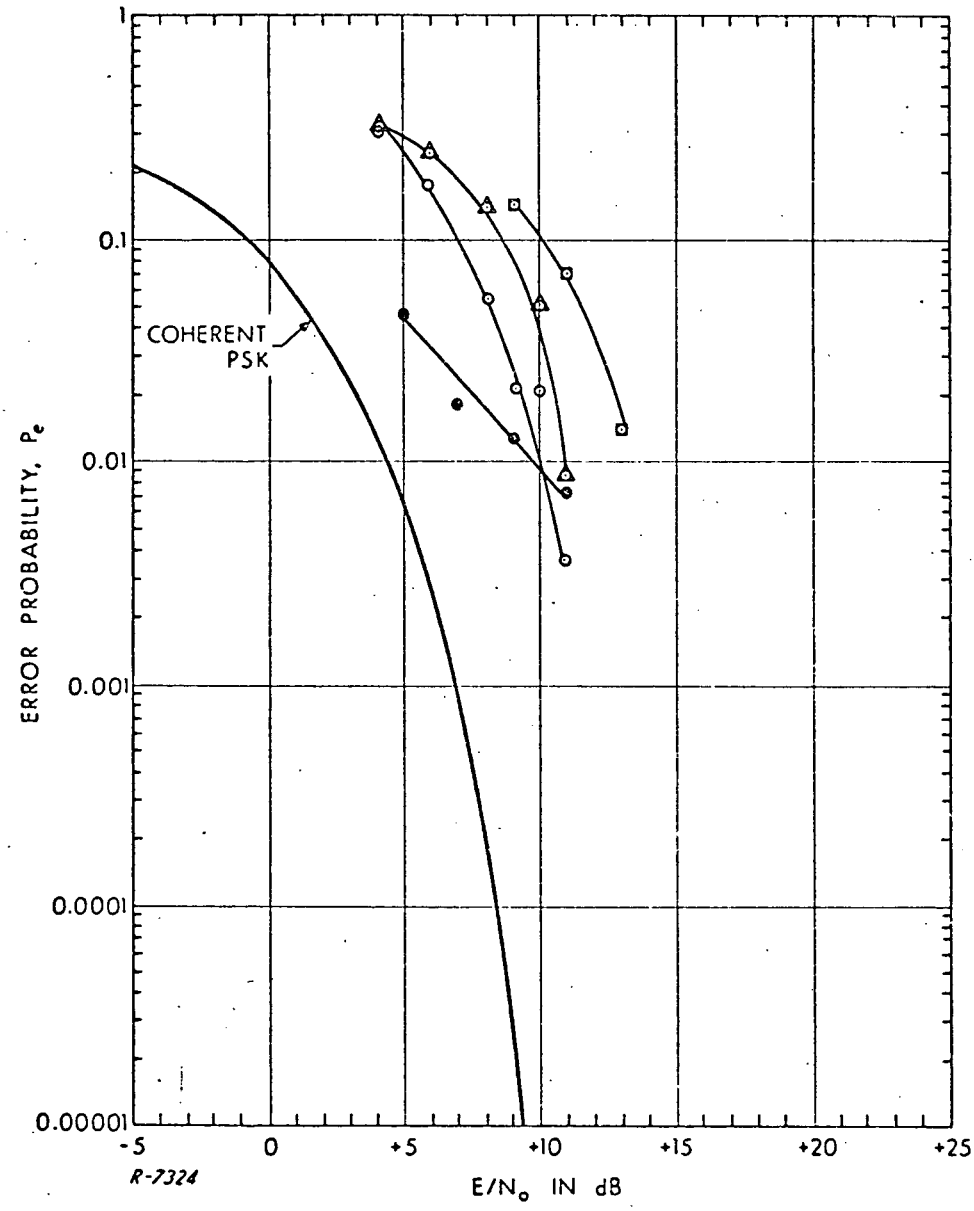


Figure 15 Error Rates for CW Interference at Various Inband Frequencies, Internal Code, 200 kHz Pre-Selector Filter, 500 kHz Clock

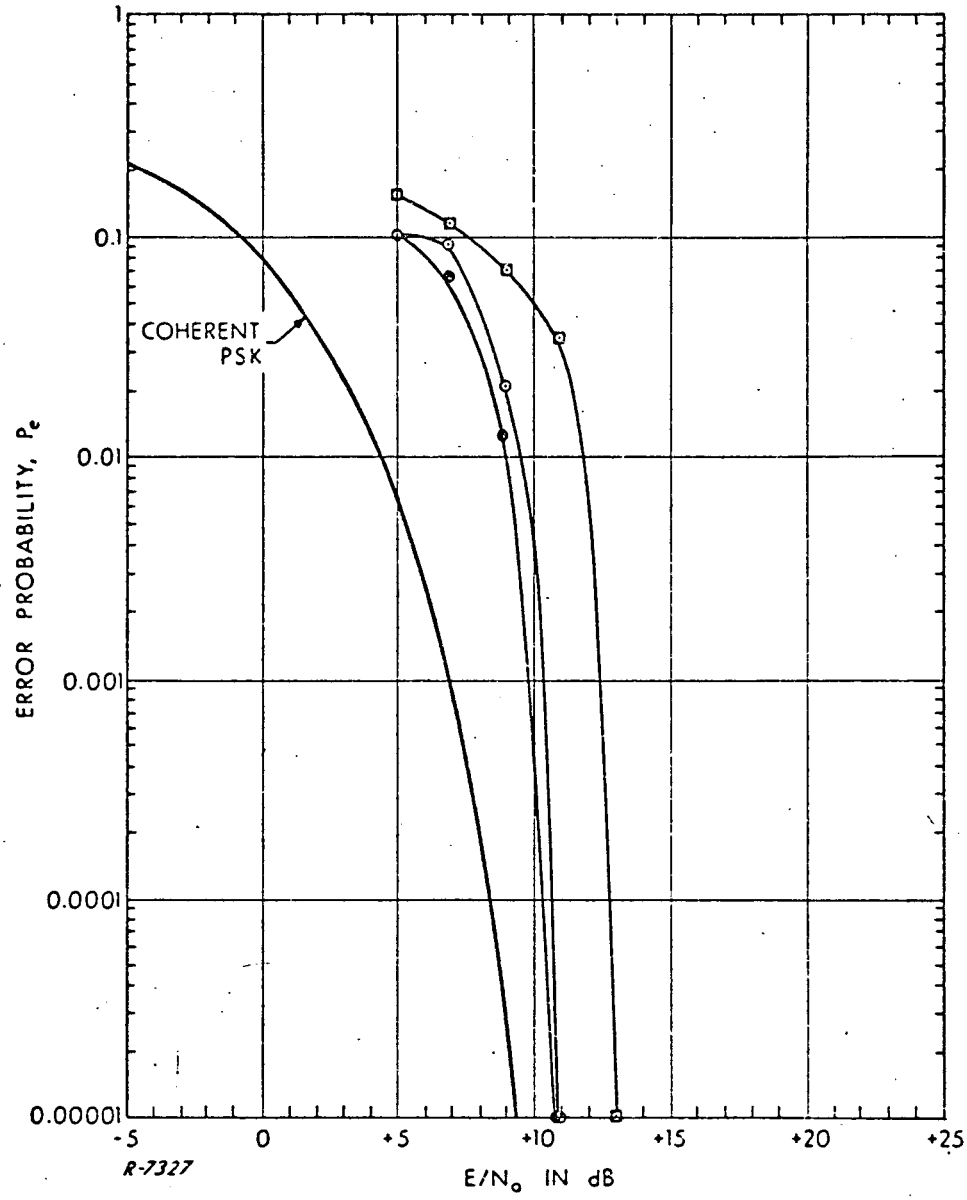


Figure 16 Error Rates for CW Interference at Various Inband Frequencies, Internal Code, 300 kHz Pre-Selector Filter, 500 kHz Clock

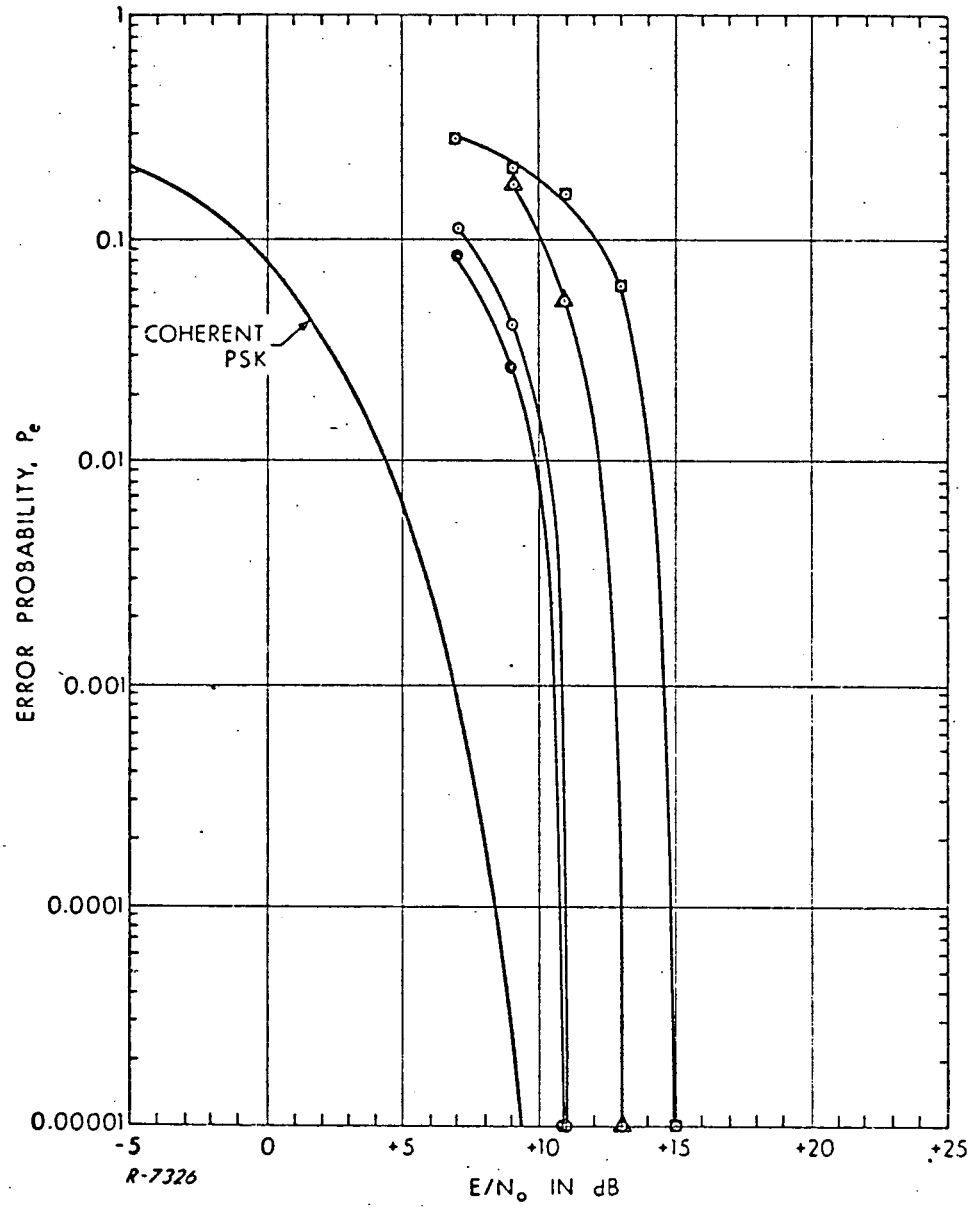


Figure 17 Error Rates for CW Interference at Various Inband Frequencies, Internal Code, 200 kHz Pre-Selector Filter, 300 kHz Clock

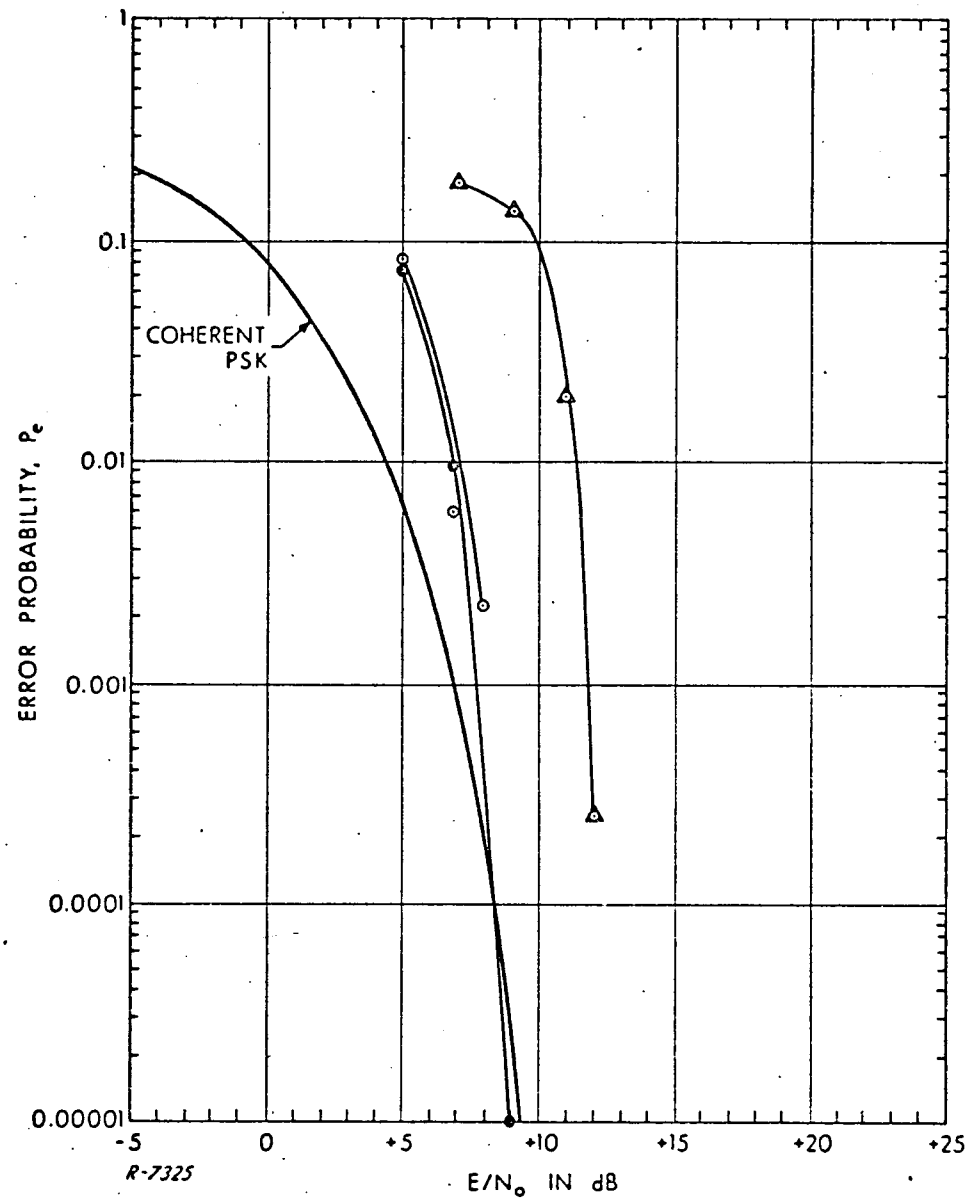


Figure 18 Error Rates for CW Interference at Various Inband Frequencies, Internal Code, 300 kHz Pre-Selector Filter, 300 kHz Clock

6.3 Conclusions

The specifications of the contract called for noise performance within 5 dB of theory at an error rate of 10^{-2} and CW error rate within 9 dB of theory. The combination of 5 samples per chip (500 kHz clock) and 200 kHz bandpass filter meets these specifications and is recommended for future application.

7. APPLICATION CONSIDERATIONS

In a PN communication or ranging system the digital matched filter finds application in one of two forms, either as an acquisition aid alone or as the total communication function. In the first instance, the purpose of the matched filter is to determine time of arrival of the selected PN sequence. Observation of the Sum-of-Squares output will indicate the time of maximum correlation. The Sum-of-Squares may be monitored while a local oscillator sweep is in progress. The filter will respond with the characteristic auto-correlation pulse when the frequency is correct to within roughly the inverse integration time. Thereby both time and frequency initial acquisition can be accomplished. When the correlation pulse exceeds a preset threshold, a hand-over will take place to a conventional multiplier-integrator correlation process combined with a phase locked loop for final frequency and time acquisition.

In the second mode of operation the matched filter performs both initial and final acquisition as well as data demodulation. After the initial frequency sweep acquisition is complete, the sine and cosine sampled outputs of the digital matched filter are applied to a Costas type PLL which controls the phase reference oscillator. Delay tracking is accomplished by a form of early-late gate operating on the correlation output pulse. Data is extracted from the in-phase matched filter output similar to the way it is done on the breadboard described above. This mode of operation requires some additional development effort since the operation of a PLL and delay tracking loop on the output of a digital matched filter has not previously been demonstrated.

Assuming the loop acquisition times are equal for both cases, the total acquisition will be the same whether the filter is used to aid acquisition or to perform all the functions. In accordance with Section 2, when the time uncertainty is governed by the code period, the maximum initial search time is $2M\Delta$ for each frequency cell in the frequency uncertainty range F_u. Since there are approximately $F_u M \Delta$ frequency cells, the maximum initial acquisition time excluding loop acquisition is $2F_u(M\Delta)^2$.

An additional factor that must be considered is range ambiguity resolution. The preceding discussion has focussed on range acquisition to within a fraction of the chip duration, but the resultant range measurement would be ambiguous by multiples of the code period. It is suggested therefore to change the code structure periodically at intervals sufficient to resolve the ambiguity. This can be accommodated in the digital matched filter by effectively changing the stored code at the appropriate times. The acquisition process would then require a final step for ambiguity resolution. After the tracking loops have acquired on the code that appears more frequently (Code A), the filter is shifted to Code B to await the arrival of the corresponding code segment. Its arrival, as indicated by the Sum-of-Squares output provides the final synchronization.

The implementation of a digital matched filter for a system such as TDRS depends primarily on the specified chip rate and on the availability of special large scale integrated circuits (LSI). Logic speeds permit operation of most of the matched filter for chip rates up to 2 MHz. However, beyond 200 or 300 kHz chip rate the digital Sample and Hold devices at the output of the summing point would begin to fail. These circuits consist of A/D converters and D/A converters with intervening holding registers. To overcome the speed limitation of these devices, it will become necessary to introduce some additional parallel in place of sequential processing. The details of this parallel processing have not been worked out pending a clear definition of actual chip-rate requirements.

Spacecraft application of the digital matched filter will require the use of large scale integrated circuits. Each package would contain a large number of filter stages including delay register, code storage, exclusive-or gates and summing resistors. It is especially important to perform summing in the LSI circuit, for otherwise the package becomes pin limited rather than internal logic limited. A number of developments are underway for LSI devices of this kind. None of them has the precise form of the Teledyne ADCOM digital matched filter. However, the design can be adapted to these devices should they become readily available.

Appendix A

A DIGITAL MATCHED FILTER FOR PSEUDO-NOISE SEQUENCES

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Summary

A digital implementation of a matched filter for pseudo-noise (PN) signals is described. The implementation employs a multiple phase, 1-bit, direct IF sampling scheme and a shift-register tapped delay line. Computer simulations indicate moderate departure from optimum performance.

1. Introduction

This paper describes the design and simulated performance of a novel digital matched filter implementation for pseudo-noise (PN) signals. PN sequences play an important role in many varieties of systems including anti-jam communications, multiple access, time delay measurement and tracking systems. In each of these applications the receiver can employ either correlation (multiplier-integrator) or matched filter detection.

A major obstacle to the use of correlation detectors is the problem of initial synchronization, i.e., the mechanism for getting the received and local sequences in step. Synchronization is achieved by a series of trial correlations whose number is on the order of the time uncertainty divided by the chip duration. The initial acquisition time may become excessive since the local sequence must dwell at a given phase until a decision can be made at the output of the correlator. If the correlation is less than what would be expected from synchronized sequences, the generator is stepped on to a new phase differing by at most one chip interval. In this way the entire time uncertainty or code period must be searched through chip-by-chip until a sufficiently high correlation is observed.

A significantly shorter acquisition time is obtainable from a matched filter instead of a correlator. The filter is matched to a segment of the PN sequence known a priori not to have arrived yet at the receiver. When the segment arrives, the filter responds with an output pulse, the pulse shape being the autocorrelation function of the PN segment in question. The arrival of the pulse immediately synchronizes the receiver. The acquisition time is assured to be less than the time uncertainty, since the matched filter is set to a segment whose earliest possible time of arrival (TOA) coincides with the time of filter setup and whose latest possible TOA occurs later by precisely the time uncertainty. While the idea of matched filters and even digital matched filters for PN sequences is not new, the novelty of the work reported here is that it promises a feasible implementation suitable for large time-bandwidth products.

The digital matched filter design is based on the well-known concept of the tapped delay line. The received signal is applied to the input of the delay line and the tap outputs are summed after being weighted in accordance with the corresponding samples of the anticipated waveform. An overall block diagram of the digital matched filter is shown in Fig. 1.

2. Sampling Subsystem

The sampling subsystem, which converts the analog input to a digital data stream, has several unique features. Before describing these it is appropriate to review the conventional approach to digitizing PN spread-spectrum signals. Figure 2 shows one possible method. Dual mixers driven by in-phase and quadrature components of a local oscillator convert the modulated IF to two lowpass signals which are filtered and sampled at the chip rate by an A/D converter. In order for the samples to benefit from the total energy in each chip the filtering must be nearly matched to the chip duration yielding an output waveform of gradual transitions between chip states. Since the noise power is constant, the SNR consequently varies during the chip reaching a maximum just before the next transition. Under synchronous conditions sampling can take place at the optimum instant. However, during acquisition the samples can fall anywhere and measures must be taken to avoid recurrent sampling in a region of poor SNR. This can be accomplished by adding redundant samples between the original ones so that at least one set of samples encounters good SNR. As more sample instants are added one can also widen the lowpass filter since several successive samples

can be combined to produce a filtering effect which utilizes the total bit energy.

The number of quantization levels at the A/D converters determine the amplitude and phase resolution of the sampling system. For example, if the quadrature and in-phase components are each sampled to four levels (2 bits), there are 16 resolution cells in amplitude and phase (as shown in Fig. 3a) corresponding to the 2^4 possible binary words.

A more effective way of assigning resolution cells is shown in Fig. 3b where 14 phase cells are distributed uniformiy around the unit circle. This type of resolution can be obtained by means of multiple, say N, phase detectors each quantized to one bit accuracy. Each phase detector has as reference one of N phases of the local oscillator and the A/D converter simply retains the sign of the output.

We now observe that the multiplicity of sample instants required for SNR considerations can simultaneously perform the function of multiple phase samples. Thus different carrier phases can be sampled at different instants thereby providing both the necessary time stagger as well as finer phase resolution. Furthermore, N time-staggered phase samples permit N-fold time sharing of many circuit functions.

The final step in arriving at the proposed sampling subsystem is to do away with the multiplicity of phase detectors (i.e., mixers and filters). This can be accomplished by direct sampling of the received IF signal through a narrow (nanosecond) sampling gate. The sampling strobe is applied N times per chip in synchronism with each of N phases of an IF reference clock. The sample strobes corresponding to the different reference phases are staggered through the bit duration. Thereby, the signal is digitized through a single sampling gate and the binary representation appears in serial form. Thus, if three samples are taken, they occur at carrier phases of 0°, 120° and 240°, respectively. The digital output at each sampling instant is either a "0" or a "1," corresponding to two-level quantization. The functions of the lowpass filter following the mixers in Fig. 2 must now be performed at bandpass by the IF filter preceding the sampler. This simply means that the IF bandwidth is approximately matched to the chip duration.

3. Tap Weighting and Phase Combiner

In this section we derive the structure of the tap weighting and phase transformation. The latter performs the function of transforming the multiple phase samples derived by the IF sampler into the conventional co-phase and quadrature matched filter outputs. In deriving the necessary processing functions the quantization at the input is ignored.

The successive samples taken at IF phase increments $2\pi/N$ staggered during each chip are propagated through the shift-register delay-line. Every N'th stage of the register is tapped so that the phase samples associated with a given chip appear sequentially at the tap output. At successive instants $0 \le i < N$ the n'th output tap represents

$$\cos\left(\frac{i2\pi}{N} + \phi_n + \theta\right)$$

where ϕ_n is the PN phase of the chip at the n'th tap and θ is an arbitrary phase shift between the received carrier and local reference.

Consider now two sets of tap weightings of the form $\cos \phi_n$ and $\sin \phi_n$. The PN modulation can be either bi-phase or quadra-phase. In view of the arbitrary phase shift θ we may choose the phase modulation to fall at any convenient set of two or four equally spaced angles. With bi-phase modulation one can select $\phi_n = 0, 180^\circ$ thereby eliminating $\sin \phi_n$ and reducing $\cos \phi_n$ to ± 1. For quadra-phase modulation we choose $\pm 45^\circ$ and $\pm 135^\circ$ so that $\cos \phi_n$ and $\sin \phi_n$ become binary quantities (± 0.707). The tap weighting is then simply a two-state logic operation. Note that this would not be true for the four angles 0, 90°, 180° and 270° which lead to three states for $\cos \phi_n$ and $\sin \phi_n$.

We assume now that the tap weightings are matched to the chips appearing at the respective tap outputs. The pairs of products

$$\cos \phi_n \cos\left(\frac{i2\pi}{N} + \phi_n + \theta\right)$$

$$\sin \phi_n \cos\left(\frac{i2\pi}{N} + \phi_n + \theta\right)$$

are separately summed on n in the cosine and sine summer, respectively. The two sums can be represented as the complex number:

$$C_i + jS_i = \sum_{n=1}^{M} e^{j\phi_n} \cos\left(\frac{i2\pi}{N} + \phi_n + \theta\right)$$

$$= \frac{1}{2} \sum_{n=1}^{M} \left[e^{-j\left(\frac{i2\pi}{N} + \theta\right)} + e^{+j\left(\frac{i2\pi}{N} + 2\phi_n + \theta\right)} \right]$$

$$i = 0, 1, \ldots, N-1$$

The phase transformation consists of multiplying the preceding equation by $e^{j(i2\pi)/N}$ respectively for each i and summing on i. The result is

$$\sum_{i=0}^{N-1} e^{j(i2\pi)/N} \left(C_i + jS_i\right) = \frac{1}{2} MN\, e^{-j\theta}$$

Placing the phase transformation into real terms we find the matrix operation shown in Table 1.

The configuration shown in Fig. 1 implements the preceding operations. The tap weightings are loaded in advance of the arrival of the desired signal from the digital PN sequence generator. The weights are applied to each phase sample as it appears at the tap and summed with the corresponding phase samples from all the other chips. Since the quantized phase samples and the weightings are both binary quantities, the summer can be regarded as a D/A converter, one whose resistive ladder has equal size elements. N successive sum outputs are stored in Sample and Hold devices prior to the phase transformation. The N phase samples associated with one chip are combined by the N x 2 matrix into the co-phase and quadrature components one would normally obtain from the lowpass equivalent implementation of a matched filter for a bandpass signal.

4. Filter Output and Performance Criteria

The sum of squares of the two outputs from the phase transformation yields the squared envelope of the matched filter output and the arctan operation produces an estimate of the unknown phase shift θ.

The matched filter, being a passive device, performs the same computations on the input signal for all phase sample and chip positions. Since the receiver does not know the chip phase, an output is generated for each clock cycle corresponding to one shift of the delay-line register, i.e., an advance by one phase sample. When the contents of the sample-and-holds at the input to the transformation matrix correspond to N samples between the actual chip transistion points, the envelope output is a point on the correlation between the PN sequence programmed into the matched filter and the received waveform. The outputs at instants when the S+H contents correspond to samples from two adjacent chips provide a more or less smooth transition between points on the correlation function.

Synchronization or time-of-arrival measurement using the digital matched filter proceeds in a straightforward manner. The envelope output is compared to a threshold appropriately set between the peak of the autocorrelation and the maximum sidelobes.

For comparative evaluation it is convenient to employ the SNR defined as

$$\left(\frac{S}{N}\right)_o = \frac{(\text{Peak Signal})^2}{\text{Noise Power}}$$

For an ideal linear matched filter one has the well-known result

$$\left(\frac{S}{N}\right)_o = M \frac{2E_c}{N_o}$$

where E_c is the energy per chip, N_o is the single-sided input noise power density and M is the number of chips in the sequence to which the filter is matched.

The simulation described later is based on an input SNR as observed in the IF filter bandwidth. Denoting by B_n the noise-bandwidth of this filter and by F_{ss} the spread-spectrum chip rate, the SNR at the IF filter output is

$$\left(\frac{S}{N}\right)_{in} = \frac{F_c F_{ss}}{N_o B_n}$$

Consequently the ideal SNR relation becomes

$$\left(\frac{S}{N}\right)_o = 2M \frac{B_n}{F_{ss}} \left(\frac{S}{N}\right)_{in}$$

A comparable SNR measure from the envelope output of the non-linear digital matched filter cannot be obtained by separately inserting signal and noise. Instead we shall assume that the output, when the PN sequence is propagating through the filter prior to synchronization, can be represented as an envelope of gaussian noise. The envelope is Rayleigh distributed with mean square equal to twice the noise power.

Contributions to the pre-sync power come from both the autocorrelation sidelobes and the additive noise or interference.

The peak signal shall be taken as the mean value of the output envelope after synchronization, i.e., the correlation peak. The resultant SNR is defined as

$$\left(\frac{S}{N}\right)_o = \frac{(\text{Post-sync Mean})^2}{(\text{Pre-sync Mean Square})/2}$$

Due to the system nonlinearities introduced by 1-bit quantization and envelope extraction this SNR will be different from that of the ideal matched filter.

5. Computer Simulation

The primary features of the digital matched filter, viz. the multiple phase sampling and the two-level quantization are not amenable to analytical treatment. Consequently, a computer simulation was developed to evaluate the filter performance under various conditions. The simulation followed in general terms the signal flow in Fig. 1.

The inputs to the sampler were generated individually and consist of the following items:

1) Quadra-phase modulated signal
2) Signal distortion due to a single-pole bandpass filter
3) Gaussian additive noise as observed at the bandpass filter output

The performance criterion is the output signal-to-noise ratio $(S/N)_o$ defined in Sec. 4.

The data for M = 300, $B_n/F_{ss} = 2$ are shown in Fig. 4. A curve has been fitted to the experimental points for N = 3, i.e., three samples per chip. There is some scatter in the points attributable to statistical variation due to small sample size in the simulation experiment. Nevertheless the performance trend is clearly evident. The $(S/N)_o$ is close to optimum at low and moderate output SNR and departs from the optimum at higher SNR. This behavior has not been studied theoretically; it is believed to be due to the method of measuring $(S/N)_o$ and the fact that the 1-bit quantizer (limiter) tends to maintain a constant pre-sync output noise level independent of input noise level.

Different values of B_n and N were also investigated. Table 2 shows deviations from ideal for several combinations. The starred entries were taken at the same SNR $[(S/N)_{in} = -15\,dB]$. Although it cannot be definitely concluded from this limited data, one would expect that the performance is optimized at a lower B_n for N = 3 than for N = 5.

Table 2

Deviation from Optimum

$\frac{B_n}{F_{ss}}$	N = 3	N = 5
1.5	-0.3 dB	
2.0	-2.7 dB*	
3.0	-3.4 dB*	-2.5 dB*
4.0		-2.4 dB

The data from all noise simulation runs with nearly optimum parameter sets (N and B_n) are combined in Fig. 5 where the ordinate is given in the normalized form $(S/N)_o/2MB_n$ so that all points can be compared to the same standard.

Finally, we note that there is no clear-cut advantage for N = 5 over N = 3, although this conclusion may change with additional data. Hence, from strictly a practical point of view N = 3 would be preferable.

Acknowledgment

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The author acknowledges with thanks the work of Mr. Edward P. Greene in preparing the simulation program and the helpful suggestions of Mr. Ralph Zaorski on the sampling implementation.

$$\begin{bmatrix} \frac{MN}{2}\cos\theta \\ -\frac{MN}{2}\sin\theta \end{bmatrix} = \begin{bmatrix} 1 & 0 & \cos\frac{2\pi}{N} & -\sin\frac{2\pi}{N} & \cdots & \cos\frac{(N-1)\,2\pi}{N} & -\sin\frac{(N-1)\,2\pi}{N} \\ 0 & 1 & \sin\frac{2\pi}{N} & \cos\frac{2\pi}{N} & \cdots & \sin\frac{(N-1)\,2\pi}{N} & \cos\frac{(N-1)\,2\pi}{N} \end{bmatrix} \times$$

$$\begin{bmatrix} \sum_n \cos[\phi(t_n)+\theta]\cos\phi(t_n) \\ \sum_n \cos[\phi(t_n)+\theta]\sin\phi(t_n) \\ \sum_n \cos(\frac{2\pi}{N}+\phi(t_n)+\theta)\cos\phi(t_n) \\ \sum_n \cos(\frac{2\pi}{N}+\phi(t_n)+\theta)\sin\phi(t_n) \\ \vdots \qquad\qquad \vdots \\ \sum_n \cos[\frac{(N-1)\,2\pi}{N}+\phi(t_n)+\theta]\cos\phi(t_n) \\ \sum_n \cos[\frac{(N-1)\,2\pi}{N}+\phi(t_n)+\theta]\sin\phi(t_n) \end{bmatrix}$$

Table 1
Phase Combiner Matrix Transformation

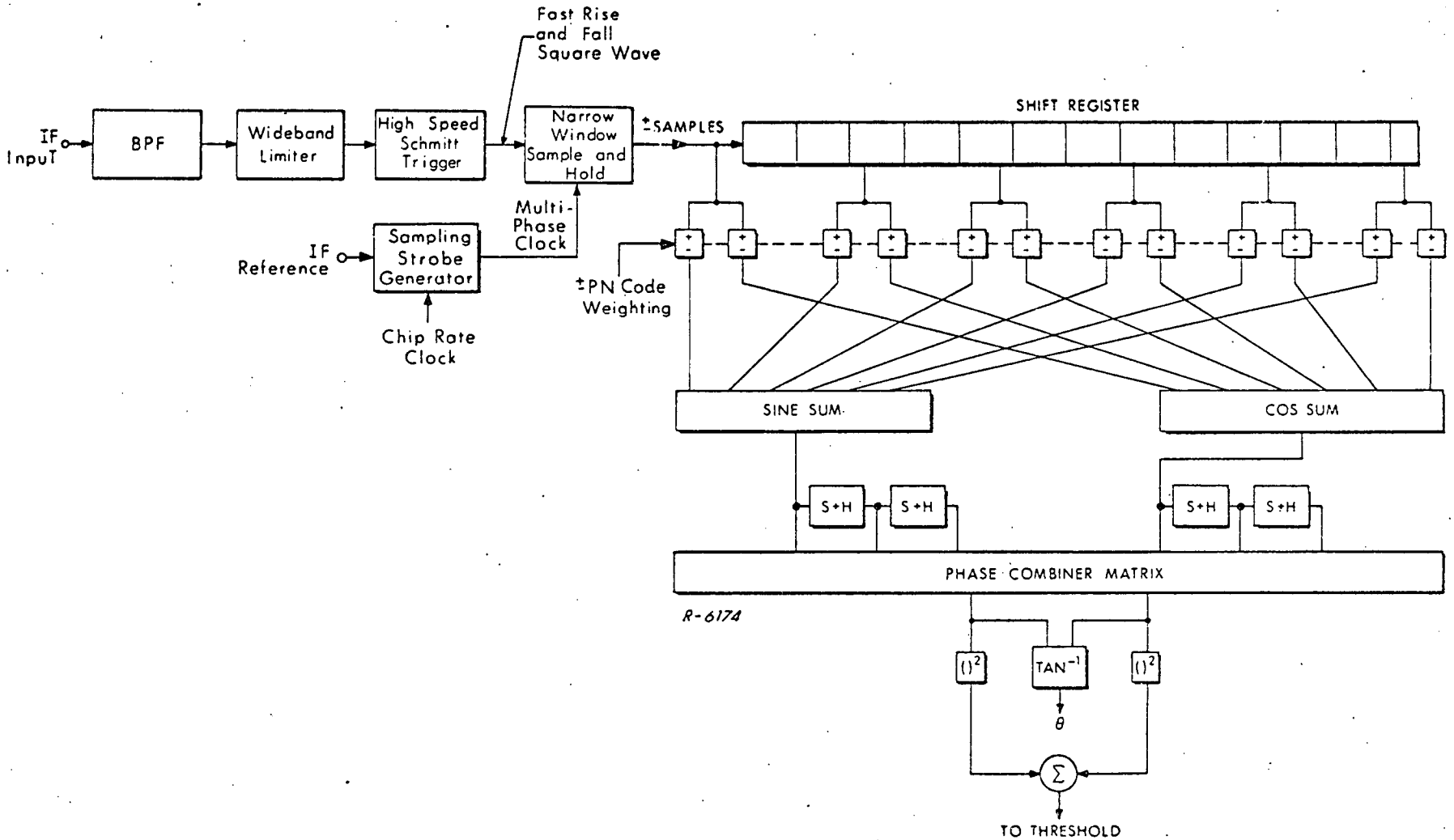


Fig. 1 Digital Matched Filter for PN Sequences

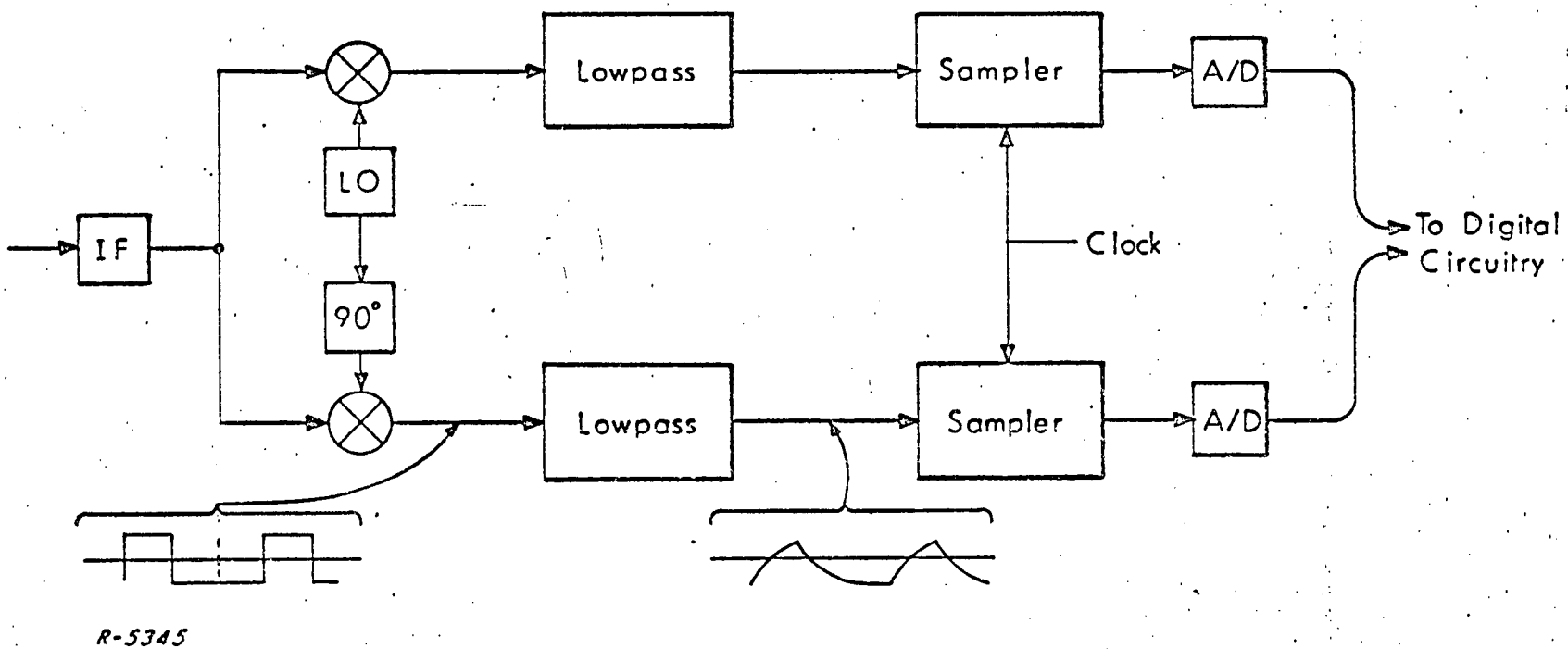


Fig. 2 Conventional Sampling Subsystem

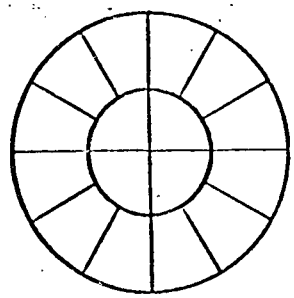
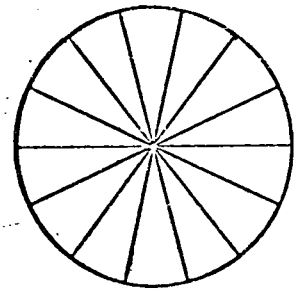


Fig. 3a Resolution Cells for 2-Bit Quantization of In-Phase and Quadrature Phase Detector Outputs



R-5344

Fig. 3b Resolution Cells for 1-Bit Quantization of Multiple Phase Detector Outputs

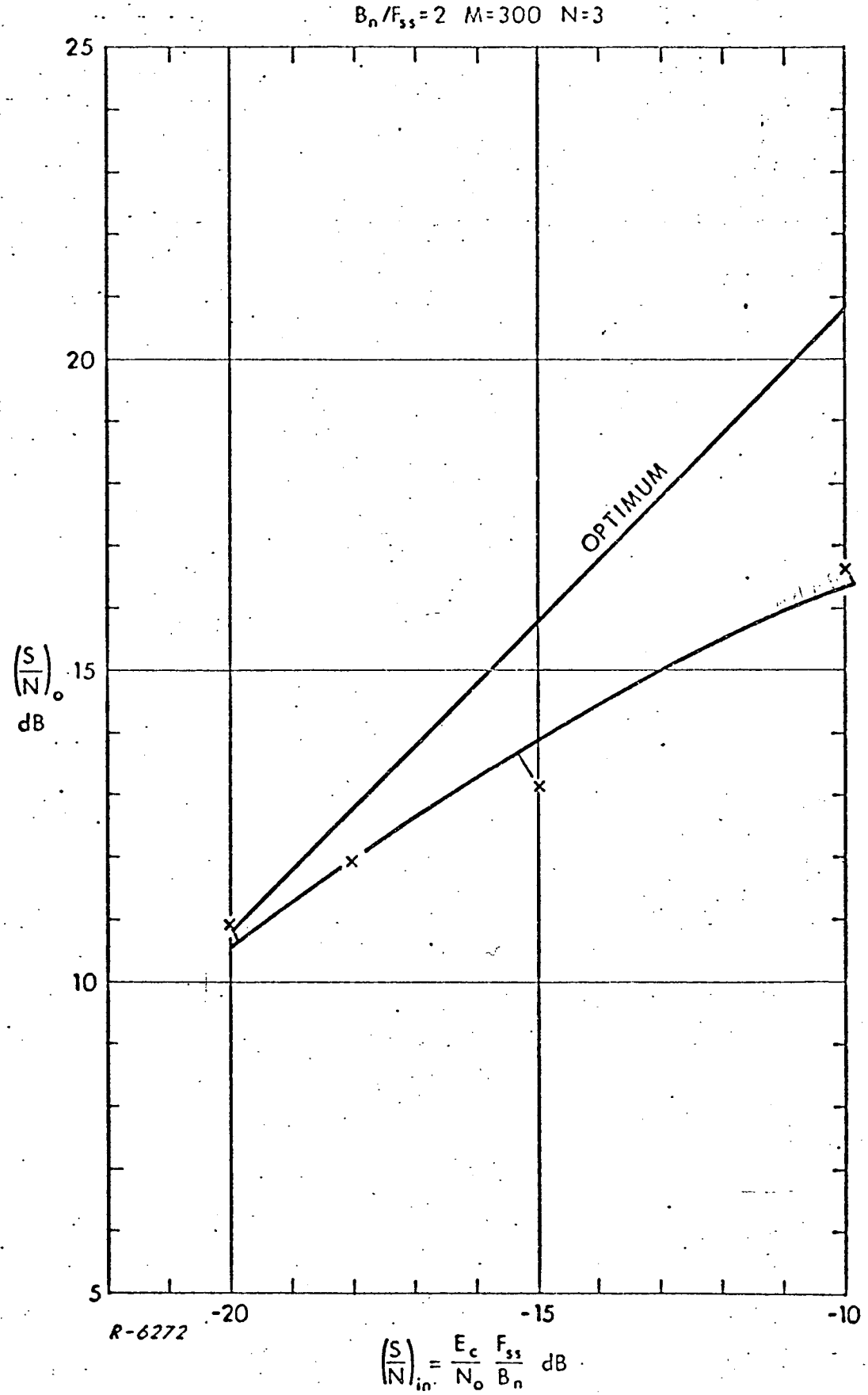


Fig. 4 Optimum SNR and Simulation Results for Gaussian Noise and M = 300

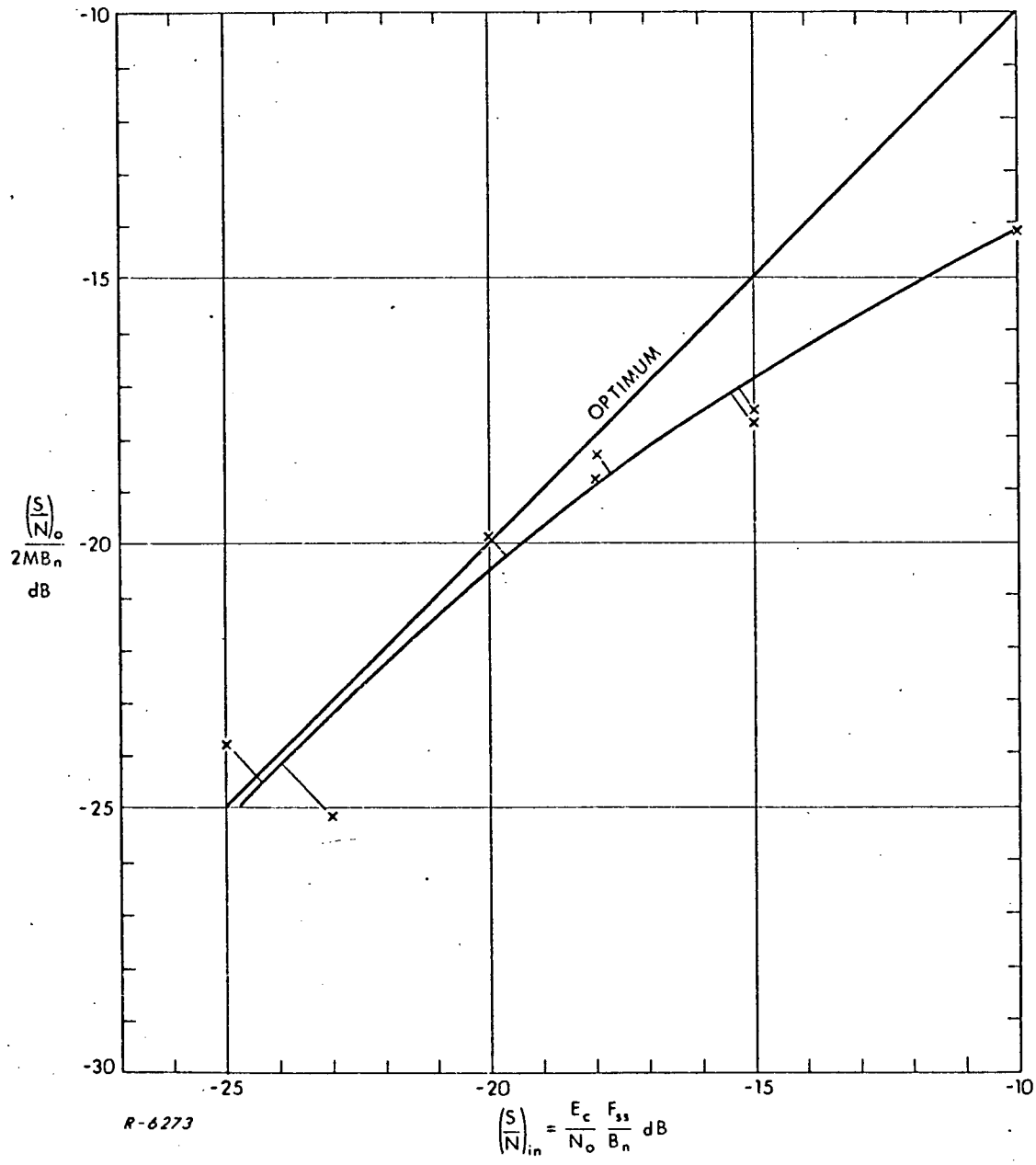


Fig. 5 Normalized SNR for Gaussian Noise

Appendix B

DIGITAL MATCHED FILTER ALIGNMENT PROCEDURE

The circuits that require alignment in the Digital Matched Filter System consist of two Schmitt trigger circuits. One circuit follows the preselector filter and is used to shape the 1.6 MHz modulated sinewave carrier into a squarewave suitable to the digital circuits it feeds. The other Schmitt trigger circuit follows sin θ output and is used to shape the sine θ output waveform prior to the error detector processor. Both these circuits are subject to some drifts and their alignment renders a more optimized system performance.

The card containing the Schmitt trigger following the preselector filter is located at row B column 23. The output of this circuit at pin L2 (B23L2, available at the connector at the front of the system behind the guard panel) should be observed on a scope. With no input to the circuit, (the patch cable between EXT MOD CARRIER IN connector and INT MOD CARRIER OUT connector on the system front panel must be removed) the potentiometer R_2 on this card must be adjusted for a balanced output. This means that the circuit should trigger on the slight amount of system noise present and thus the total number of "ON" and "OFF" states at the output as observed on the scope should be about equal. This accomplishes the alignment of the first Schmitt trigger.

The Schmitt trigger for shaping sin θ output waveform is located on the Squarer card at row C & D, column 2. The output of this circuit at pin D2U2 should be observed on a scope, and with no input to the system (the patch cable between EXT MOD CARRIER IN and INT MOD CARRIER OUT connectors must be disconnected) the potentiometer R_{11} on the Squarer card should be adjusted for approximately equal number of "ON" and "OFF" states at the Schmitt trigger output. It is to be noted that the

Schmitt trigger should be carried out only after the alignment of the first Schmitt trigger, card B22, has been accomplished according to the given procedure.

No other adjustments are necessary for the alignment of the Digital Matched Filter System.

Appendix C

DIGITAL MATCHED FILTER ACCEPTANCE TEST DATA

DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
	NOISE INTERFERENCE INTERNAL CODE 200 KC PRESELECTOR FILTER 500 KC CLOCK		
-27 db	3 db	1052	.0885
-25 db	5 db	476	.0404
-23 db	7 db	204	.0173
-21 db	9 db	36	.00305
	NOISE INTERFERENCE EXTERNAL CODE 200 KH_z PRESELECTOR FILTER 500 KH_z CLOCK		
-27	+3	708	0.06
-25	+5	336	0.029
-23	+7	106	0.009
-21	+9	19	0.0016

8/26/71
KA

2

DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
	NOISE INTERFERENCE		
	INTERNAL CODE		
	300 KH_z PRESELECTOR FILTER		
	500 KH_z CLOCK		
-28	+4	1010	0.086
-26	+6	500	0.0425
-24	+8	165	0.014
-22	+10	38	0.0032
EXTERNAL CODE			
-28	+4	852	0.072
-26	+6	336	0.029
-24	+8	110	0.0093
-23	+9	48	0.0041

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DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

NOISE INTERFERENCE
200 KH_z PRESELECTOR FILTER
300 KH_z CLOCK

$\frac{I}{S}$ (db)	$\frac{E}{N}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
INTERNAL			
-26	+4	1683	.14
-24	+6	1022	.086
-22	+8	489	.041
-20	+10	160	.013
-18	+12	34	.003
EXTERNAL			
-26	+4	1040	0.088
-24	+6	640	0.054
-22	+8	224	0.019
-20	+10	49	0.00416

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HB

DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
	NOISE INTERFERENCE 300 KH_z PRESELECTOR FILTER 300 KH_z CLOCK		
INTERNAL			
-26	+6	1200	0.102
-24	+8	520	0.044
-22	+10	244	0.021
-20	+12	51	0.0043
EXTERNAL			
-26	+6	1200	0.102
-24	+8	632	0.054
-22	+10	436	0.037
-20	+12	65	0.0055

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W.D

DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

C W INTERFERENCE
INTERNAL CODE
200 KH_z PRESELECTOR FILTER
500 KH_z CLOCK

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
-23	+4	3470	0.3
-21	+6	2750	0.23
-19	+8	1600	0.136
-17	+10	600	0.051
-16	+11	100	0.0085
-23	+4	3800	0.32
-21	+6	2120	0.18
-19	+8	648	0.055
-18	+9	250	0.021
-17	+10	250	0.021
-16	+11	44	0.0037
-22	+5	554	0.047
-20	+7	212	0.018
-18	+9	150	0.013
-16	+11	86	0.0073
-18	+9	1600	0.136
-16	+11	816	0.07
-15	+13	172	0.0145

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M.C

DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
	C.W. INTERFERENCE 300 KH_Z PRESELECTOR FILTER 500 KH_Z CLOCK		
INTERNAL			
-22	+5	1816	0.155
-20	+7	1280	0.110
-18	+9	824	0.070
-16	+11	360	0.0305
-14	+13	0	0
EXTERNAL			
-40	-13	348	0.030
-38	-11	134	0.0114
-37	-10	54	0.0046
-36	-9	39	0.0033
EXTERNAL			
-38	-11	600	0.051
-36	-9	648	0.055
-34	-7	110	0.0093
-32	-5	9	0.00076
INTERNAL			
-22	+5	1270	0.108
-20	+7	1052	0.090
-18	+9	248	0.021
-16	+11	0	0
INTERNAL			
-22	+5	1200	0.102
-20	+7	780	0.066
-18	+9	141	0.0120
-16	+11	0	0
EXTERNAL			
-38	-11	470	0.040
-36	-9	67	0.0057

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DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
		C W INTERFERENCE 200 KH_z PRESELECTOR FILTER 300 KH_z CLOCK	
INTERNAL			
-20	7	~~2372~~ 3372 R.S	.286
-18	9	2444 M.D	.207
-16	11	1744	.148
-14	13	708	.06
-12	15	0	0
EXTERNAL			
-24	3	6000	0.51
-23	4	1700	0.145
-22	5	3	.00025
EXTERNAL			
-22	5	1364	0.116
-21	6	1050	.0809
-20	7	32	.0027
INTERNAL			
-20	7	1300	0.11
-18	9	466	0.04
-16	11	0	0
INTERNAL			
-20	7	940	0.08
-18	9	300	0.0255
-16		0	0
EXTERNAL			
-26	1	20000	1.7
-25	2	1200	.102
-24	3	0	0
EXTERNAL			
-20	7	2800	.24
-19	8	173	.0147
-18	9	0	0
EXTERNAL			
-28	-1	10000	0.85
-27	0	1820	0.155
-26	1	306	0.026
-25	2	0	0
INTERNAL			
-18	9	2000	0.17
-16	11	700	0.051
-14	13	0	0

8/24/71 M.D

DIGITAL MATCHED FILTER
ACCEPTANCE TEST DATA

C W INTERFERENCE
300 KH_z PRESELECTOR FILTER
300 KH_z CLOCK

$\frac{I}{S}$ (db)	$\frac{E}{N_o}$ (db)	ERRORS PER MINUTE	ERROR PROBABILITY P_e
INTERNAL			
-22	5	864	.073
-20	7	116	.0098
-18	9	0	0
EXTERNAL			
-26	1	1846	0.156
-24	3	350	0.03
-22	5	0	0
EXTERNAL			
-26	1	1608	0.136
-24	3	115	0.0097
-23	4	674	0.057
-22	5	912	0.077
-20	7	19	0.0016
INTERNAL			
-20	7	2088	0.178
-18	9	1576	0.133
-16	11	234	0.020
-15	10	3	0.00025
INTERNAL			
-22	5	950	0.081
-20	7	81	0.0069
-19	8	26	0.0022
EXTERNAL			
-26	1	1960	0.166
-24	3	632	0.054
-22	5	258	0.022
-20	7	1	0.000085

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HA