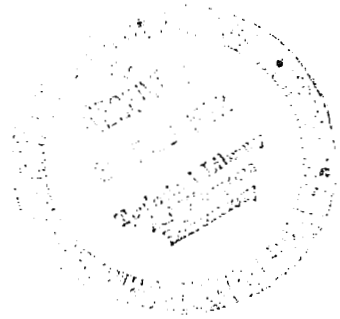
NASA TECHNICAL NOTE

NASA TN D-6590

ANALYTICAL DESIGN OF A PARASITIC-LOADING DIGITAL SPEED CONTROLLER FOR A 400-HERTZ TURBINE-DRIVEN ALTERNATOR

by Bill D. Ingle and John P. Ryan

Lewis Research Center
Cleveland, Ohio 44135



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION • WASHINGTON, D. C. • JANUARY 1972

1. Report No. NASA TN D-6590	2. Government Accession No.	3. Recipient's Catalog No.
4. Title and Subtitle ANALYTICAL DESIGN OF A PARASITIC-LOADING DIGITAL SPEED CONTROLLER FOR A 400-HERTZ TURBINE-DRIVEN ALTERNATOR		5. Report Date January 1972 6. Performing Organization Code
7. Author(s) Bill D. Ingle and John P. Ryan		8. Performing Organization Report No. E-6430
9. Performing Organization Name and Address Lewis Research Center National Aeronautics and Space Administration Cleveland, Ohio 44135		10. Work Unit No. 120-27 11. Contract or Grant No.
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Washington, D. C. 20546		13. Type of Report and Period Covered Technical Note 14. Sponsoring Agency Code

15. Supplementary Notes

16. Abstract

A design for a solid-state parasitic speed controller using digital logic was analyzed. Parasitic speed controllers are used in space power electrical generating systems to control the speed of turbine-driven alternators within specified limits. The analysis included the performance characteristics of the speed controller and the generation of timing functions. The speed controller using digital logic applies step loads to the alternator. The step loads conduct for a full half wave starting at either zero or 180 electrical degrees. The digital-speed-controller hardware has not been fabricated or tested.

17. Key Words (Suggested by Author(s))
Electronic controller
Speed control
Electrical power systems

18. Distribution Statement
Unclassified - unlimited

19. Security Classif. (of this report)	20. Security Classif. (of this page)	21. No. of Pages	22. Price*
Unclassified	Unclassified	48	$3.00

* For sale by the National Technical Information Service, Springfield, Virginia 22151

ANALYTICAL DESIGN OF A PARASITIC-LOADING DIGITAL SPEED CONTROLLER FOR A 400-HERTZ TURBINE-DRIVEN ALTERNATOR

by Bill D. Ingle and John P. Ryan*

Lewis Research Center

SUMMARY

In dynamic space power systems, a speed controller maintains the speed of the turbine-driven alternator within specified limits by maintaining a balance between the alternator input power and the alternator load. Previous speed control systems have utilized analog control logic and phase-controlled power-output stages. A digital speed controller for a 400-hertz power system was analyzed as part of a continuing effort to apply the state-of-the-art control techniques as they become available. This investigation was limited to a mathematical analysis of the performance characteristics of the digital speed controller. The digital-speed-controller hardware has not been fabricated. The analysis of the power generating system, including the digital speed controller, is recommended for a later study. The digital-speed-controller design as discussed in this report utilizes digital logic in applying step loads to the alternator. The step loads conduct for a full half wave starting at either zero or 180 degrees. The power-output stages apply power in discrete balanced, three-phase increments. The design effort required to adapt this speed-controller concept for operation at a higher line frequency and at a lower power level per speed-controller load step is also discussed.

The change in line frequency resulting from a 100-percent change in useful system load is 0.02 percent of rated. The time required for the speed controller to respond to a change in input frequency is nominally 50 milliseconds.

The digital speed controller will, however, produce a power fluctuation on the alternator output. This fluctuation appears in the power generating system as a voltage modulation and as a frequency modulation. This characteristic is typical of speed controllers utilizing power-output stages in which turnon is initiated at either zero of 180 degrees. The level of modulation can be readily controlled by proper selection of the power rating of the individual parasitic-load steps.

*Associate Professor of Electrical Engineering Technology, Purdue University, Indianapolis Regional Campus, Indianapolis, Indiana.

INTRODUCTION

The Lewis Research Center is currently investigating several concepts for the generation of electric power for space applications (refs. 1 to 4). These space power systems include a parasitic-loading speed controller for the purpose of maintaining the speed of a turboalternator within specified limits. A digital speed controller was analyzed for use in these 400-hertz turboalternator power systems, and the results of this analysis are presented in this report.

In these power systems, turbine power is nominally a constant, the speed of the turboalternator (and system frequency) being controlled by maintaining a balance between the power input to the alternator and power in the alternator load. The power in the alternator load is composed of the system useful load (that power which is available to the user of the power system) and that load on the alternator required to maintain the system functions such as power conditioning, voltage control, and speed control. The control and power-conditioning functions effectively appear as parasitic loads on the power generating system.

Previous power generation systems have included an analog type of speed control in which phase-controlled power-output stages have been used (refs. 5 and 6). The analysis of the digital speed controller was initiated as part of a continuing effort to investigate the state-of-the-art control techniques as they become available.

The digital speed controller compares the half period of the alternator frequency with a fixed time reference, after a fixed delay. The controller then applies a balanced three-phase parasitic load to the alternator as a function of the magnitude of this time difference. The parasitic load is applied in discrete steps. The step loads conduct for a full half wave starting at either zero or 180 degrees of the line voltage wave, referred to in this report as zero-degree firing.

The digital-speed-controller hardware has not been fabricated; therefore, all performance information presented in this report is based on computation. There are design characteristics in this type of digital speed controller which may ultimately be cause for concern. These characteristics are the degree of adaptability for operation in higher frequency ($f_{line} > 400$ Hz) power systems and at a lower power level per speed-controller load step. The step application of parasitic load could generate both voltage and frequency modulation on the power system output bus. These effects are discussed in more detail in the section PROPOSED SPEED-CONTROLLER CIRCUIT.

The analysis of the digital speed control is preceded by a general discussion of the control concept as applied in this design and is followed by a detailed review of the individual speed-controller subcircuits. The effects of various circuit design parameters on the performance of the speed controller are discussed, and then the effects of various system design parameters on the performance of the speed controller are discussed.

SPEED-CONTROL SYSTEM

The control of speed (line frequency) in the dynamic energy conversion systems being investigated at Lewis typically consists of an electronic speed controller applying parasitic load to a turbine-driven alternator. Parasitic-loading speed controllers maintain a balance of output power on the alternator such that the parasitic load applied by the speed controller plus the power dissipated in the useful (system) load equals the power developed by the turbine (less system losses). Figure 1 is a block diagram of a typical power generation system.

The parasitic load in the digital speed controller is applied as blocks of three-phase power, as illustrated in figure 2. The digital system will produce a change in the magnitude of the line voltage in proportion to the amount of parasitic power being switched

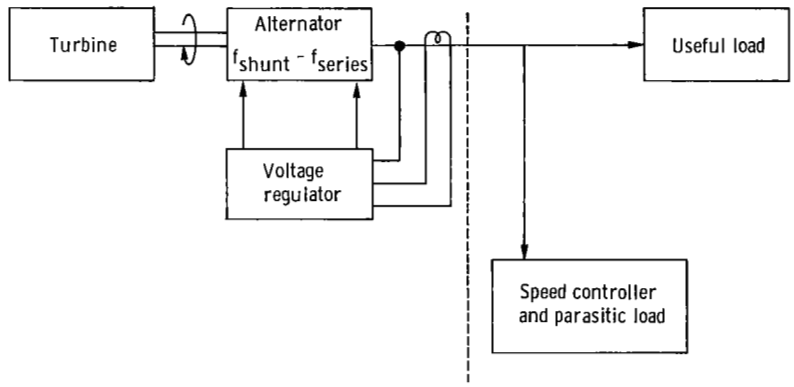


Figure 1. - Block diagram of parasitically loaded dynamic power generation system. Sum of useful and parasitic power is constant.

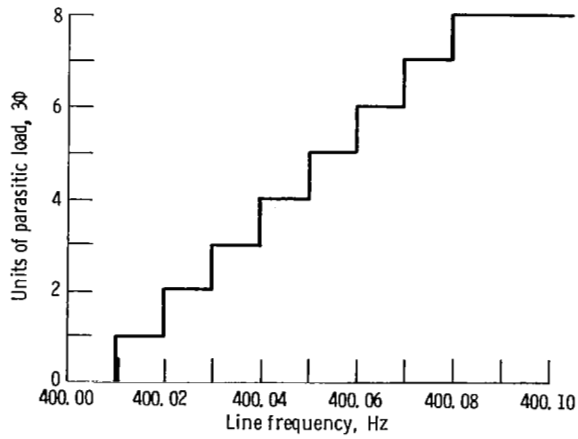


Figure 2. - Parasitic-loading characteristic of digital speed controller.

per load step in relation to the alternator rating. This assumes the voltage regulator will not respond fast enough to correct for these voltage variations. The line voltage variation will be a minimum for useful loads that require an output line frequency which corresponds to one of the fixed parasitic-load-step turnon frequencies, as shown in figure 2. The maximum voltage variation will occur for useful loads which require an output line frequency between these parasitic-load-step turnon frequencies. This voltage variation will effectively appear in the system as line voltage modulation.

The loading characteristic of the digital speed controller will also include a frequency-dependent component. This frequency component will effectively appear in the system as frequency modulation.

The design of the speed controller emphasized the use of medium-speed, digital, integrated circuit (IC) modules where possible. In general, the faster the rated operating speed of an IC module, the lower the operating signal level and, also, the signal-to-noise ratio. A low signal-to-noise ratio increases the possibility of circuit malfunction. The specific design goals for the digital speed controller are itemized in table I. These goals generally represent the state of the art for exiting analog speed

TABLE I. - DESIGN GOALS FOR DIGITAL SPEED CONTROLLER

Nominal frequency, Hz	400
Frequency range, Hz	+0.08 to -0.00
Frequency recovery time (100 percent load change), msec	≤75
Minimum number of three-phase PLR's	8
Parasitic power rating, kW	50
Line voltage (three-phase)	120/208
Voltage modulation without voltage regulator compensation, percent	≤1

controllers. The exceptions are the frequency range and the parasitic power rating. The power rating has been increased to reflect the trend of future space power generating systems, while the decrease in frequency range is an attempt to illustrate the inherent state-of-the-art capabilities of digital systems. It is recognized that the system gain, as reflected in this value of frequency range, could present a stability problem. However, preliminary computations indicate that the speed-controller design being presented here would be stable.

In using digital-type logic, the alternator line frequency signal is modified by the various subcircuits as the signal progresses sequentially from the comparator to the power-output stage and parasitic-load resistors. The various subcircuits of the digital speed controller are activated and subsequently reset by a timing signal in order to obtain this sequential transfer of information.

An abbreviated block diagram of the digital speed controller is shown in figure 3. This figure will permit the circuit philosophy to be discussed prior to the detailed discussion of the controller. The digital speed controller functionally consists of a frequency reference, a deviation error detector, a period counter, a low-frequency detector, a magnitude error detector, a decoder, and multiple three-phase power-output stages.

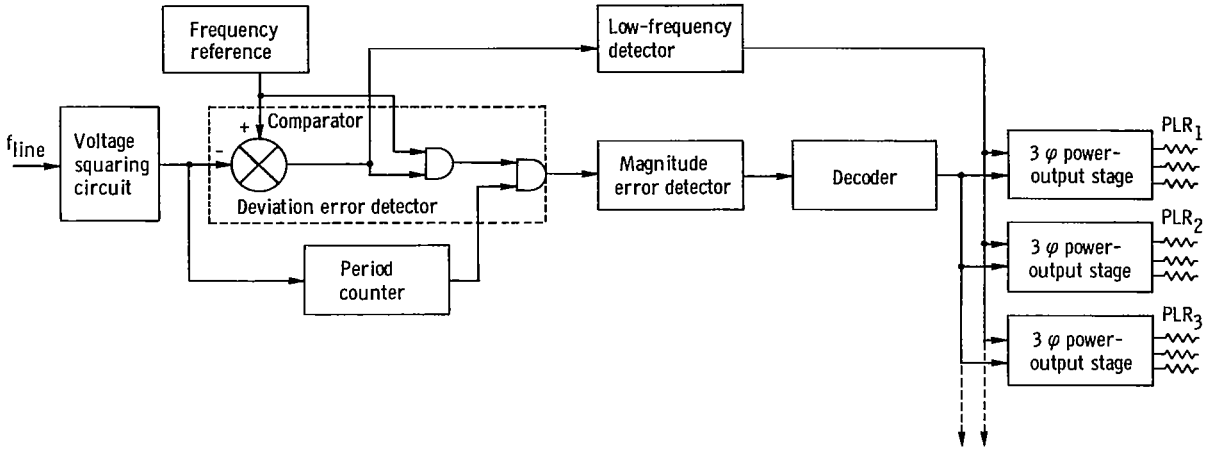


Figure 3. - Abbreviated block diagram for digital speed controller.

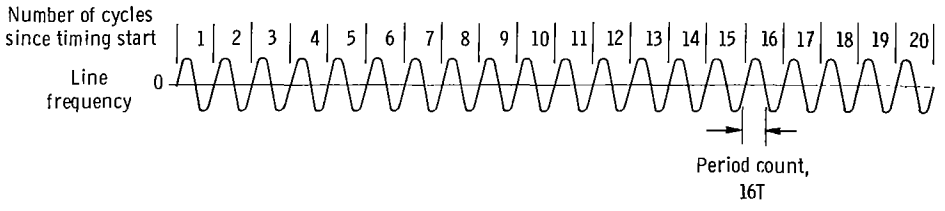
The input line frequency to the speed controller is converted into a square wave to obtain an input signal which is compatible with the digital logic concept.

The line frequency signal is compared with a constant-frequency reference. A series of rectangular pulses is obtained which is the difference between these two inputs. This difference signal is used to gate a high-frequency square-wave generator. These high-frequency pulses are sampled following a fixed delay after initiation of the pulse series. The number of high-frequency pulses gated during the period following the delay is proportional to the frequency error between the alternator and the constant-frequency reference. The high-frequency pulses determine which power-output stages and consequently which parasitic-load elements are connected to the alternator power bus. Eight parasitic power levels can be obtained in this design by the use of five power-output stages. This is accomplished as a result of having combined the advantages of binary control with a special decoder. The parasitic-load elements on the power-output stages will, as a result, have unequal power ratings. The special decoder will, however, permit the individual load elements to be used for approximately the same number of parasitic-load levels.

As stated at the beginning of this section, a series of rectangular pulses is generated as a result of comparing the alternator signal with the frequency reference. This resultant signal exists for alternator frequencies below the reference frequency as well as

for alternator frequencies above it. As such, the loading characteristic of figure 2 would be folded about the ordinate axis. The speed controller must therefore be inhibited for alternator frequencies below the reference.

The timing signal is generated from the alternator line frequency. The timing signals in this report are referred to as a period count of nT, for example 16T, which indicates the period of the positive portion of the nth cycle of the alternator output wave. This is illustrated in sketch (a).



(a)

In addition, a timing function is generated which subdivides a particular period of alternator line frequency into 1-microsecond increments. For example, the period count of 17TR1 is generated 1 microsecond after the initiation of the 17th cycle of the alternator output wave. The duration of the period count 17TR1 is 1 microsecond. The period count of 16T and 17TR1 in the example was selected for convenience only. In this digital-speed-controller concept, several period counts are generated during the time required for one complete cycle of speed-controller operation.

One cycle of speed-controller operation (referred to as a sampling cycle) is defined as the number of cycles of alternator line frequency which occur between the application of a given value of parasitic load and the subsequent reapplication of a given value of parasitic load.

A very general description of a typical parasitic-load change would involve the following sequence of events:

(1) Assume one parasitic-load element is connected to the line and the alternator line frequency has increased because of a reduction in useful load.

(2) The error (difference) signal would increase at the comparator output (see fig. 3).

(3) The positive portion of the 16th error signal would be filled with high-frequency (1-MHz) pulses.

(4) The number of high-frequency pulses as stored in the error detector circuit would increase.

(5) The new error count would be applied, through the decoder, to the power-output stages. The output stages would in turn apply the number of parasitic-load steps as required.

(6) The next cycle of operation would be initiated to determine the next error pulse count, and the sequence would be repeated.

A detailed discussion of the sequence of events is presented in appendix A.

CONCEPTUAL SPEED-CONTROLLER CIRCUIT

A block diagram of a digital speed controller is illustrated in figure 4. The description of this speed controller has been abbreviated to simplify the presentation, and as such represents only a concept. Shown in figure 4 are the major circuit functions which make up the conceptual speed controller.

A speed-controller design such as would be proposed for use in a space power generating system is discussed in the section PROPOSED SPEED-CONTROLLER CIRCUIT.

The frequency reference consists of a 5-megahertz free-running crystal-controlled oscillator in which the output is counted down to obtain a 1-megahertz output signal (referred to as the subcarrier) and a 400.00-hertz reference signal. The number of 1-megahertz pulses at the input to the magnitude error detector determines the amount of parasitic load to be applied to the alternator. The 400.00-hertz reference is compared with the alternator line frequency to generate a series of rectangular wave pulses. The 16th positive pulse gates the output of the 1-megahertz signal. The two divide counters are synchronized with the alternator line frequency. The synchronization takes place at the leading edge of the alternator line frequency signal. The counters are synchronized to reduce the frequency drift in the speed controller. This subject is discussed in detail in the section PROPOSED SPEED-CONTROLLER CIRCUIT.

The deviation error detector basically consists of a comparator, a subcarrier gate circuit, and a sampling period gate circuit. The detector utilized differential amplifiers and logic-type NAND circuits. The deviation error detector forms the pulse error count signal which is described by the Boolean expression (16T) (ϵ^{+}) (f_{sc}), where (f_{sc}) is the 1-megahertz frequency of the subcarrier. The pulse error count signal determines the parasitic-load level applied to the alternator output. The detector also separates the difference error signal $\epsilon^{\pm}$ into the positive and negative (inverted) components, ϵ^{+} and $\overline{\epsilon^{-}}$, respectively.

The f_{line} period counter generates the various timing functions for the speed controller. Specifically, the period counter (1) resets the various logic functions necessary to maintain a continuous flow of error information into the power-output stages, (2) determines the gating time for the pulse error count signal, and (3) reinitiates successive sampling cycles to provide continuous sensing of the alternator line frequency. The

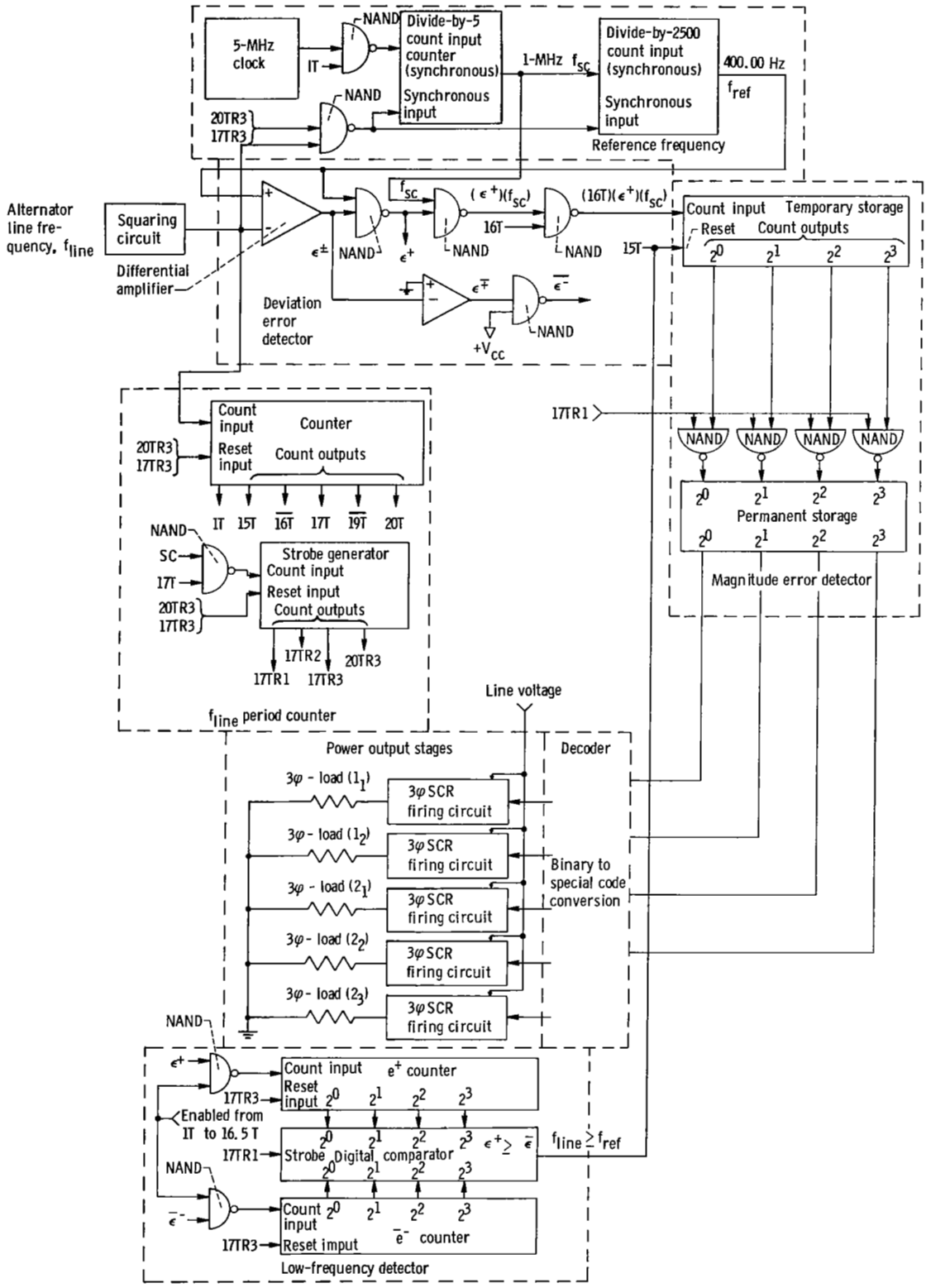


Figure 4. - Block diagram for digital speed controller (conceptual).

error signal is counted during the 16th cycle of the alternator line frequency. This 16-cycle delay in sampling the period count generates a 1-megahertz error pulse for each unit of parasitic load. For example, 8 error pulses in the deviation error detector will apply 8 units of parasitic load.

The magnitude error detector includes temporary and permanent storage registers. The temporary storage subcircuit provides a binary logic output as a function of the series of error pulses which are generated by the deviation error detector. The temporary storage subcircuit functionally determines the new loading data for the speed controller while the permanent storage subcircuit retains the previous error loading data.

The new loading data are transferred from the temporary storage to the permanent storage on command from the f_{line} period counter. The data transfer occurs in the period (17TR2) following the determination of the new speed error.

The output of the permanent storage subcircuit is in the form of binary logic. The parasitic-load element usage factor is quite low for a power-output stage if based on the binary concept. Usage factor is the ratio of the number of discrete parasitic-load levels in which a particular load element is used to the total number of discrete parasitic-load levels in the system. This usage factor becomes more critical in systems requiring an overload capability, as is the case in turbine-driven alternator power systems. (Previous power systems have included a 1.8 per unit overload capability.) An additional problem of binary loading systems is the wide range of power ratings for the parasitic-load elements in an operating power system. For example, using a binary load range of 15, the power rating for the parasitic-loading elements would vary over an 8 to 1 range. Assuming the elements to be designed on the basis of a constant power dissipation per unit of surface, the packaging of such a parasitic-load assembly would be simplified by reducing the power range of the elements.

As a result of these considerations, a special decoder was designed which limits the power range of the elements to 2 to 1 and provides a load usage for all elements between 50 and 62 percent of the loading conditions.

Each power-output stage in the speed controller consists of three single-phase full-wave silicon-controlled-rectifier(SCR) power stages and includes the SCR firing logic (gate control). The SCR gate power is controlled by a solid-state firing circuit utilizing a pulse transformer and a solid-state one-shot multivibrator. The one-shot multivibrator limits the average gate power dissipation while delivering high-peak gate power. This SCR control technique improves the power-output stage reliability.

The low-frequency detector inhibits the speed controller by counting the number of ϵ^+ pulses and the number of $\overline{\epsilon^-}$ pulses in the comparator output signal through the positive portion of the 16th period of alternator frequency. For alternator frequencies equal to or higher than the reference, the number of ϵ^+ pulses and the number of $\overline{\epsilon^-}$

pulses will be the same. For alternator frequencies below the reference, the number of ϵ^- pulses will outnumber the number of ϵ^+ pulses. The digital comparator in the low-frequency detector provides an output signal only for inputs of line frequency greater than the reference frequency.

The digital comparator in the low-frequency detector provides an output signal only for inputs of line frequency equal to or greater than the reference frequency.

The sequence of operation for the various subcircuits within the speed controller can best be explained by referring to a timing chart as illustrated in figure 5. The complete timing function is provided by the f_{line} period counter and the strobe generator. The period counter counts through 17 cycles of the alternator line output frequency. After 17 cycles the system is reset to zero, and the logic starts a new sampling cycle. The strobe generator subdivides the positive portion of specific alternator periods into 1250 increments as needed to generate the R1, R2, and R3 components of the 17TR1, 17TR2, and 17TR3 reset pulses. This function permits the sequential operation of various reset functions within one period of the alternator output. At the start of a sampling cycle (the leading edge of 1T), the period counter, the low-frequency detector, and the reference frequency subcircuits are turned (gated) on. These three subcircuits will provide information as to the magnitude of the frequency error and the polarity, that is, whether the alternator frequency is above the reference or below it. At this

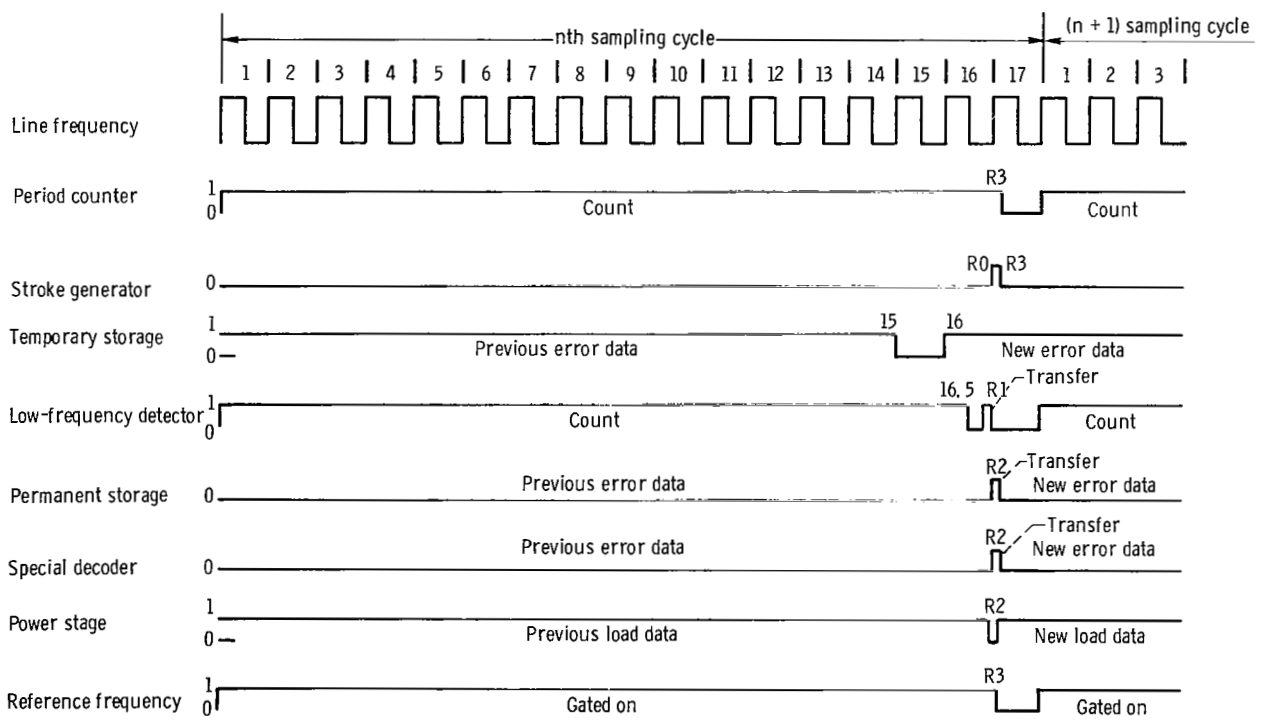


Figure 5. - Timing chart for digital speed controller.

time (the leading edge of 1T), it is noteworthy that the temporary and permanent storage subcircuits as well as the decoder and power-output stages contain the logic information generated during the previous sampling cycle.

At the beginning of the 15th period count (15T), the temporary storage subcircuit is reset to zero in preparation for the new frequency error data to be entered at the beginning of the next period count (16T). In addition to the new error data being entered into the temporary storage, the low-frequency detector is gated off, and the information contained therein is stored until also transferred to the temporary storage subcircuit. The strobe generator which provides gating pulses every 1 microsecond is gated on during the positive part of the 17th period (17T). The first reset pulse (17TR1, 1 μsec after the start of the 17th period of the line frequency) transfers the low-frequency data, while the second reset pulse (17TR2) transfers the frequency error data to permanent storage. The data transferred to the permanent storage subcircuit are transmitted to the decoder immediately. A delay of approximately 35 nanoseconds is actually incurred in this transfer, which is the propagation delay of the subcircuit. A discussion of the effect of these component delays is presented in the section Propagation Delays Associated With the Deviation Error Signal. The loading information which was transferred into the temporary storage subcircuit at the leading edge of 16T is transferred to the SCR power-output stages at 19TR2 only during the first sampling cycle. This function was introduced to prevent a false application of parasitic load during an initial turnon transient. After the first sampling cycle, the load error is transferred to the SCR's at 17TR2. Timing sequences not shown in figure 5 are the delays for the various power supplies which are required for the clock reference, the logic circuits, and the SCR firing circuits. This includes the delay provided for initial reset of the speed-controller logic. Initial reset removes all binary logic data which may have been retained by the speed controller following the previous test run.

A detailed discussion of the signal flow within the speed controller is presented in appendix A for the speed transient generated by the application of useful load.

Subcircuit Analysis

A detailed discussion of each speed-controller subcircuit is presented in this section. The complete circuit schematic including the timing diagram is shown in appendix A.

Reference frequency subcircuit. - The reference frequency subcircuit consists of a 5-megahertz free-running crystal-controlled, temperature-controlled astable multivibrator (clock), a synchronous divide-by-5 counter, and a synchronous divide-by-2500 counter. The free-running astable multivibrator frequency source (5 MHz) was chosen

to permit a long-term (≥5 yr) speed-controller system frequency stability of 1 part in 10^6. Stability as used here encompasses all the parameters (fabrication, thermal, aging, etc.) which cause the oscillator frequency f_{osc} to deviate from the design value. To obtain this long-term stability, the following features must be incorporated into the design of the oscillator:

(1) Crystal control

(2) Temperature control

(3) Astable operation

(4) 72-Hour initial settling time

The multivibrator frequency stability is specified as 1 part in 10^{10}, which remains reasonably constant following initial startup. The frequency error at startup is expected to be less than 1 part in 10^5 and will reach design level at approximately 72 hours.

The synchronous divide-by-5 counter provides a subcarrier frequency f_{sc} of 1 megahertz which is gated on periodically. The selection of 1 megahertz as the subcarrier frequency permits the use of medium-speed digital logic modules having a cutoff frequency of 2 megahertz. The synchronous divide-by-2500 counter provides a synchronous reference frequency of 400.00 which is compared with the alternator line frequency. The multivibrator frequency is gated into the divide-by-5 counter at the beginning of the first period of the alternator output wave (1T) and is gated off at 17TR3. Both counters (divide by 5 and 2500) are synchronous counters (ref. 7). By using synchronous counting, the propagation delay of the circuit can be reduced to the delay of one flip-flop (typically 35 nsec). This means that the nominal delay between the 5-megahertz leading edge and the 1-megahertz leading edge and the delay between the 1-megahertz leading edge and the 400-hertz leading edge are each 35 nanoseconds (max 80 nsec).

The frequency stability of the multivibrator frequency source (1 part in 10^{10}) will also apply to the accuracy of the subcarrier (1 MHz) and the reference frequency (400 Hz) except for the constant propagation delay of 35 nanoseconds. This timing accuracy is important because the speed controller relies on the time relation between the subcarrier frequency and the 16th positive portion of the alternator line frequency f_{line} to generate a frequency error between the line frequency and the reference frequency. The logic circuits used for the divide-by-5 counter are transistor-transistor-logic (TTL) circuits because of the 5-megahertz input frequency. The TTL circuits have a typical cutoff frequency of 35 megahertz. The logic circuits which make up the divide-by-2500 counter are diode-transistor-logic (DTL) circuits which have a typical cutoff frequency of 2 megahertz.

Deviation error detector. - The deviation error detector consists of two differential amplifiers and several logic NAND circuits. The functions of the deviation error detec-

tor are shown in figure 6. The detector provides the following functions:

(1) Generates the error signal $\epsilon^{\pm}$ proportional to the period of $f_{line} - f_{ref}$ for a specific period count

(2) Generates an inverted error signal $\epsilon^{\mp}$ in correspondence with the error signal $\epsilon^{\pm}$

(3) Generates the component parts ϵ^{+} and $\overline{\epsilon^{-}}$ of the error signal by eliminating the negative portion of $\epsilon^{\pm}$ and $\epsilon^{\mp}$

(4) Forms the pulse error count signal in conjunction with the f_{line} period counter and the 1-megahertz subcarrier, which is described by the following Boolean expression:

$$\text{Pulse error count} = (16T)(\epsilon^{+})(f_{sc})$$

where f_{sc} is the frequency of the subcarrier. The deviation error detector separates the bipolar difference signal $\epsilon^{\pm}$ into its component parts ϵ^{+} and $\overline{\epsilon^{-}}$ and fills the 16th

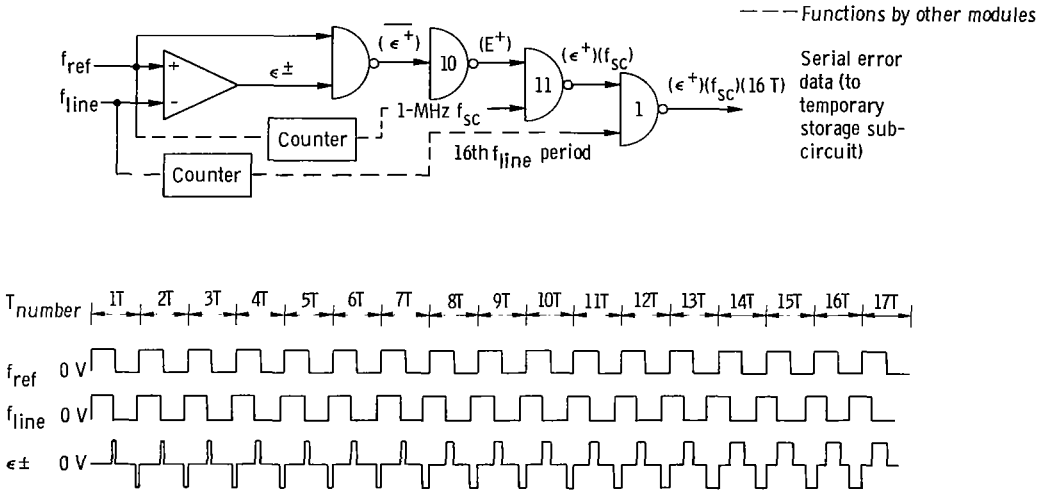


Figure 6. - Block diagram for deviation error detector.

ϵ^{+} signal with 1-megahertz pulses. For a specific period count, the time duration of the ϵ^{+} signal is porportional to the difference in period between the reference frequency (400.00 Hz) and the alternator line frequency f_{line}. By gating on the subcarrier (SC) only during this difference time, a number of pulses are generated. This number is proportional to the frequency error and is termed the error pulse count. The circuit module, NAND gate 11 (fig. 6), digitizes the frequency error. Table II lists the error

TABLE II. - DEVIATION ERROR DETECTOR OPERATION

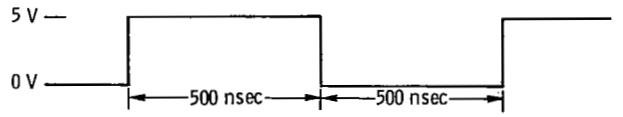
Frequency, Hz		Frequency deviation, Hz	Pulse count	PLR load (units)	Time duration of 16th ϵ^+ signal, nsec
f_{ref}	f_{line}				
400.00	400.10	0.10	8	8	9685
400.00	400.09	.09	8	8	8716
400.00	400.08	.08	8	8	7748
400.00	400.07	.07	7	7	6780
400.00	400.06	.06	6	6	5811
400.00	400.05	.05	5	5	4843
400.00	400.04	.04	4	4	3874
400.00	400.03	.03	3	3	2906
400.00	400.02	.02	2	2	1937
400.00	400.01	.01	1	1	968
400.00	400.00	.00	0	[a]0	0
400.00	399.99	-.01	1	[a]0	968
400.00	399.98	-.02	2	[a]0	1937
400.00	399.97	-.03	3	[a]0	2906
400.00	399.96	-.04	4	[a]0	3874
400.00	399.95	-.05	5	[a]0	4843

[a]Pulse count is inhibited and permanent storage is reset to zero for any $f_{line} < f_{ref}$.

count assignments with the corresponding 16th ϵ^+ time duration. The following calculations illustrate the previous discussion. The time duration of the first ϵ^+ signal (positive part) for an error pulse count of 1 is

Frequency, f, Hz	Time duration of first ϵ^+ signal, nsec
400.00 (f_{ref})	1 250 000.000
400.01 (assumed f_{line})	1 249 968.750
	Difference 31.25

The time required for an error pulse count of 1 is 1000 nanoseconds. This includes the positive part and dwell time or zero part, as indicated in sketch (b).



(b)

Since the duration of an error pulse increases 31.25 nanoseconds each half cycle, the number of complete cycles required is

$$\frac{1000 \text{ nsec}}{31.25 \text{ nsec}} = 32 \text{ half cycles}$$

$$= 16 \text{ complete cycles of alternator line frequency}$$

Actually, the period count of 16T utilizes line frequency half cycles through the 31st. The effect on system performance of the computed number of half cycles and the actual number being different is insignificant when considered with the delay at the start of an error pulse $\epsilon^{\pm}$. This error is of the order of 100 nanoseconds and is discussed further in the section FREQUENCY ERROR ANALYSIS.

Low-frequency detector. - The low-frequency detector stores the number of ϵ^{+} pulses and the number of $\overline{\epsilon^{-}}$ pulses which occur during the time interval starting with the leading edge of the first period (1T) and continuing through the positive portion of the 16th period, 16.5T, which is defined as the leading edge of the zero portion of the 16th period of the alternator line frequency. These pulse numbers are then compared in a digital comparator. If the ϵ^{+} number is equal to the $\overline{\epsilon^{-}}$ number, the signal $f_{line} \geq f_{ref}$ exists which will permit the error data in the temporary storage subcircuit to be transferred into the decoder. If the ϵ^{+} number is less than the $\overline{\epsilon^{-}}$ number, the transfer of error data from the temporary storage subcircuit will be inhibited. The lack of error data transfer will cause the speed controller to remove all units of load from the alternator line. The low-frequency detector is required because the error pulse count signal occurs for line frequencies below as well as above the reference frequency (400.00 Hz), as can be seen from table II. For example, the same pulse error count is obtained for a frequency deviation of both 0.02 and -0.02 hertz. Figure 7 shows the positive pulse count ϵ^{+} and the inverted negative pulse count $\overline{\epsilon^{-}}$ for these two conditions, $f_{line} \geq f_{ref}$ and $f_{line} < f_{ref}$. The waveform for $\overline{\epsilon^{-}}$ is shown as a series of positive pulses. The sequence of operation for the low-frequency detector is itemized for these two conditions:

For $f_{line} \geq f_{ref}$,

(1) The number of ϵ^{+} pulses equals the number of $\overline{\epsilon^{-}}$ pulses during the 16th period count.

(2) Item (1) causes $A \geq B$ output to be true at 17TR1.

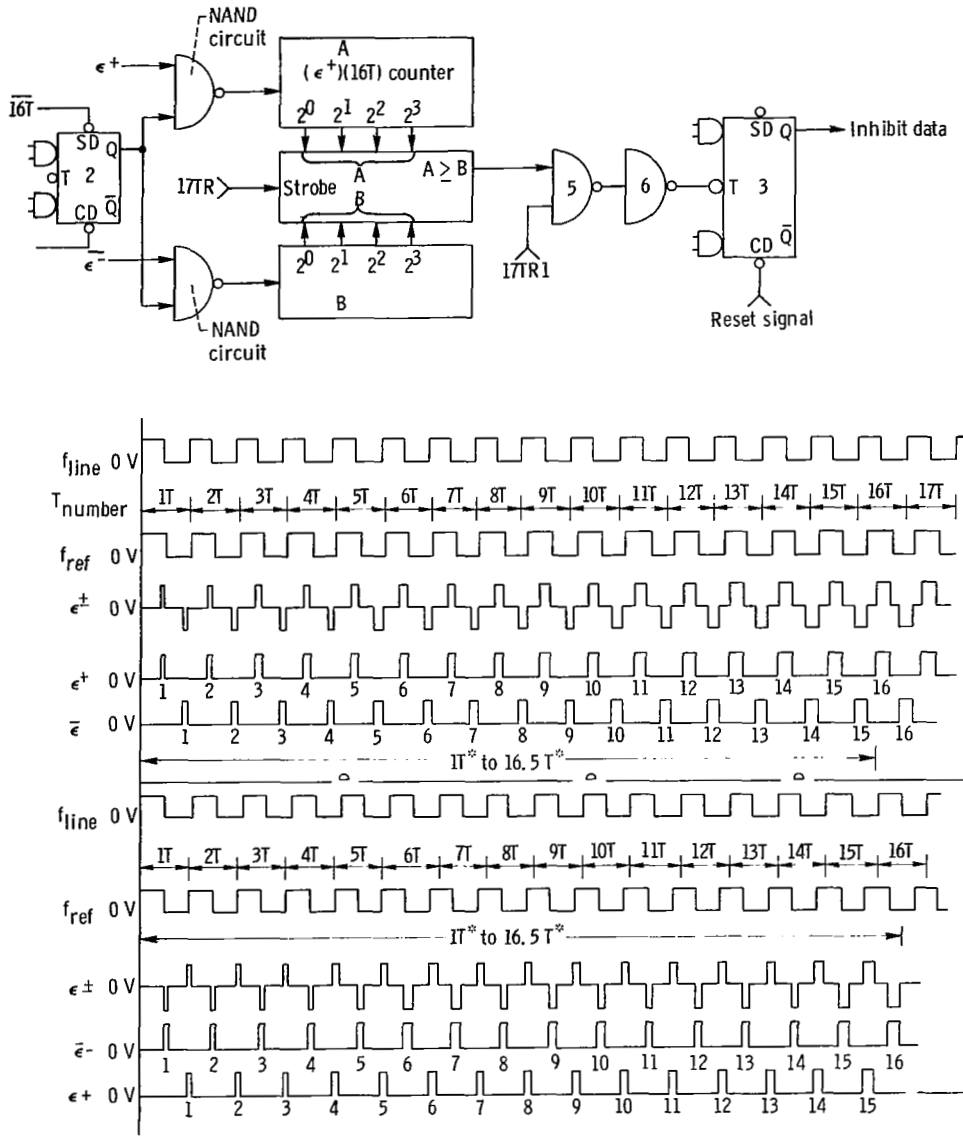


Figure 7. - Low-frequency detector operation. (Asterisk denotes leading edge.)

(3) The signal $A \geq B$ does not trigger multivibrator FF3 (fig. 7).

(4) FF3Q remains at a false level (0 V).

(5) Consequently, the temporary storage is not reset. The error pulse count which was loaded in at the previous $(16T)(\epsilon^+)$ is transferred into the permanent storage at 17TR2.

For $f_{line} < f_{ref}$,

(1) The number of ϵ^+ pulses is less than the number of $\overline{\epsilon^-}$ pulses during the 16th period count.

(2) Item (1) causes $A \geq B$ output to be false at 17TR1.

(3) The signal $A \geq B$ triggers FF3 (fig. 7).

(4) FF3Q changes from the false level (0 V) to a true level (+ V).

(5) Consequently, the temporary storage is reset to zero, and the error pulse count which was loaded at the beginning of the previous 16T is removed.

(6) The zero error pulse count is transferred at 17TR2, and all parasitic loads are removed from the alternator.

FF2 allows the ϵ^+ and $\overline{\epsilon^-}$ pulses to be counted from 1T (leading edge) until the occurrence of the leading edge of 16T.

Magnitude error detector. - The magnitude error detector includes temporary and permanent storage registers. The temporary storage subcircuit accumulates the pulse error count and converts this pulse error count from serial input to parallel binary output.

The permanent storage subcircuit is required to store the pulse error count from 17TR2 until the next 17TR2. Essentially, while the temporary storage is changing from one value of error count to another value of error count, the permanent storage is providing a constant error count to the power-output stages. Table III lists the equivalen-

TABLE III. - INPUT-OUTPUT EQUIVALENCIES FOR TEMPORARY STORAGE COMPONENT

Serial input, $(16T)(\epsilon^+)(8)(f_{sc})$, pulse error count	Parallel output			
	2^3	2^2	2^1	2^0
	Equivalent value			
1	0	0	0	1
2	0	0	1	0
3	0	0	1	1
4	0	1	0	0
5	0	1	0	1
6	0	1	1	0
7	0	1	1	1
8	1	0	0	0
9	1	0	0	0
10	1	0	0	0
...	1	0	0	0

cies between the incoming error pulse count and the output binary count. An error pulse count greater than or equal to 8 causes the speed controller to saturate at 8 units of load. As shown in figure 8, when the output of the temporary storage reaches a count of 8 (NAND gate 2), then FF1 inhibits NAND gate 1 and the temporary storage output remains at a count of 8. FF1 is reset at the leading edge of 1T, and the sequence repeats

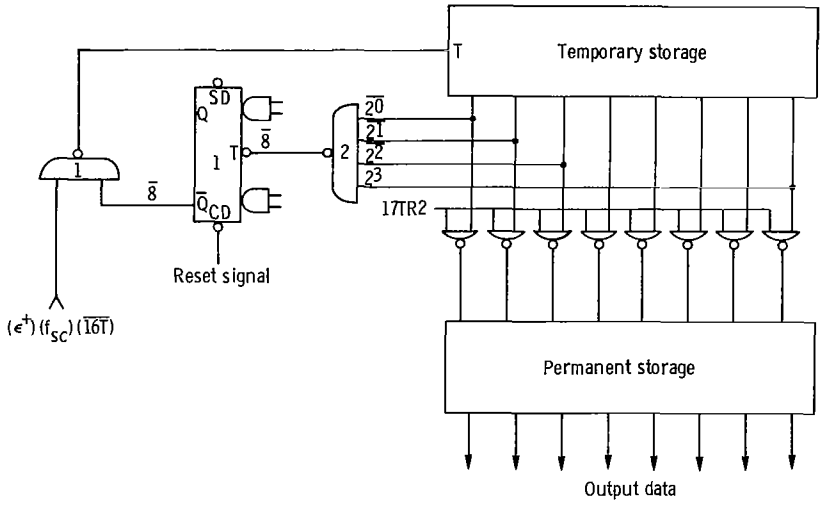


Figure 8. - Block diagram for magnitude error detector.

itself during the next sampling cycle. From figure 5, the error count is stored in the temporary storage register from the leading edges of 16T to 15T. The error count is erased, temporary storage is reset to 0000 from the leading edge of 15T to the leading edge of 16T. The pulse error count is transferred at 17TR2 and stored in the permanent storage. This 15T reset serves an additional function. Table II illustrates the ambiguity of the magnitude pulse error count, namely, the inability of the magnitude error detector to determine frequency polarity. If the alternator line frequency is less than the reference frequency (400.00 Hz), the signal $f_{line} \geq f_{ref}$ from the low-frequency detector is zero volts, which inhibits NAND gate 1, as discussed previously. At the next 15T (leading edge), the temporary storage is reset to 0000, and this error pulse count (0000) is then transferred into the permanent storage.

Decoder. - The special decoder (ref. 8) is required to increase the utilization of the parasitic-load resistors and to minimize the load error in the event of a malfunction of one of the SCR circuits. The transformation of the binary error count signal into the special code is illustrated in table IV. For example, the Boolean transmission equation for 1 unit of parasitic load (first element) would be as follows:

$$L_1 = 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3} + 2^0\,2^1\,2^2\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,2^3 \qquad (1)$$

TABLE IV. - DECODER BINARY TO SPECIAL CODE

CONVERSION FOR VARIOUS PULSE ERROR COUNTS

Pulse error count (base 10)	Binary input				Unit load (a)				
	2^3	2^2	2^1	2^0	L_1	L_2	L_3	L_4	L_5
	Special code input				Special code output				
0	0	0	0	0	0	0	0	0	0
1	0	0	0	1	1	0	0	0	0
2	0	0	1	0	1	1	0	0	0
3	0	0	1	1	0	1	1	0	0
4	0	1	0	0	1	1	0	1	0
5	0	1	0	1	1	0	0	1	1
6	0	1	1	0	1	1	1	0	1
7	0	1	1	1	0	1	1	1	1
8	1	0	0	0	1	1	1	1	1

[a]Load L_1 is first single unit load (1_1); load L_2 is second single unit load (1_2); load L_3 is first double unit load (2_1); load L_4 is second double unit load (2_2); load L_5 is third double unit load (2_3).

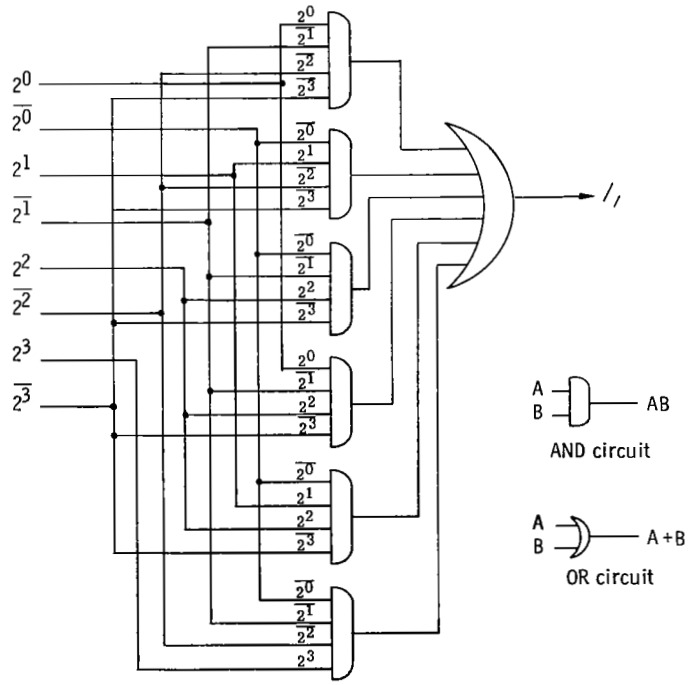


Figure 9. - Binary to special code conversion decoder (first element only).

This Boolean transmission equation can be synthesized by the use of NAND gates and NOR gates as illustrated in figure 9.

The complete derivation of the matrix circuit, in addition to an alternative code conversion, is given in appendix B. The special decoder has some interesting properties. As can be seen from table IV, wherever possible, the transformation uses two single unit loads instead of one double unit of load. The advantage of this arrangement is that, in the event of a malfunction, the load resolution error is minimized. The probabilities that a single unit load and a double unit load are being used are as follows:

$$Pr[L_1] = Pr[L_2] = \frac{6}{9}$$

$$Pr[L_3] = Pr[L_4] = Pr[L_5] = \frac{4}{9}$$

The probabilities that a specific unit of load is used assumes that any frequency deviation in the range 400.00 to 400.08 hertz is equally probable.

In this system, the deviations 0.07 and 0.08 hertz are overload conditions. Therefore, with the deviation limited to 0.00 to 0.06 hertz, the probabilities that a specific unit load is used are as follows:

$$Pr[L_1] = \frac{5}{7}$$

$$Pr[L_2] = \frac{4}{7}$$

$$Pr[L_3] = Pr[L_4] = Pr[L_5] = \frac{2}{7}$$

Power-output stage. - Figure 10 shows the logic drawing for the time-delayed silicon-controlled-rectifier firing circuit. FF4 prevents NOR gate 6 from transferring the pulse error count from the magnitude error detector to the SCR power stage until the first 19T (leading edge) period count.

This 19T (leading edge) delay in the transfer of the loading data to the SCR occurs only during initial turnon of the speed controller. During subsequent sampling cycles, the loading data will be transferred at 17TR2.

NOR gate 8 allows the parasitic-load data to be applied only during the zero voltage crossover (0 to 15 V) of the alternator output line voltage. This SCR firing scheme minimizes the load current switching transients.

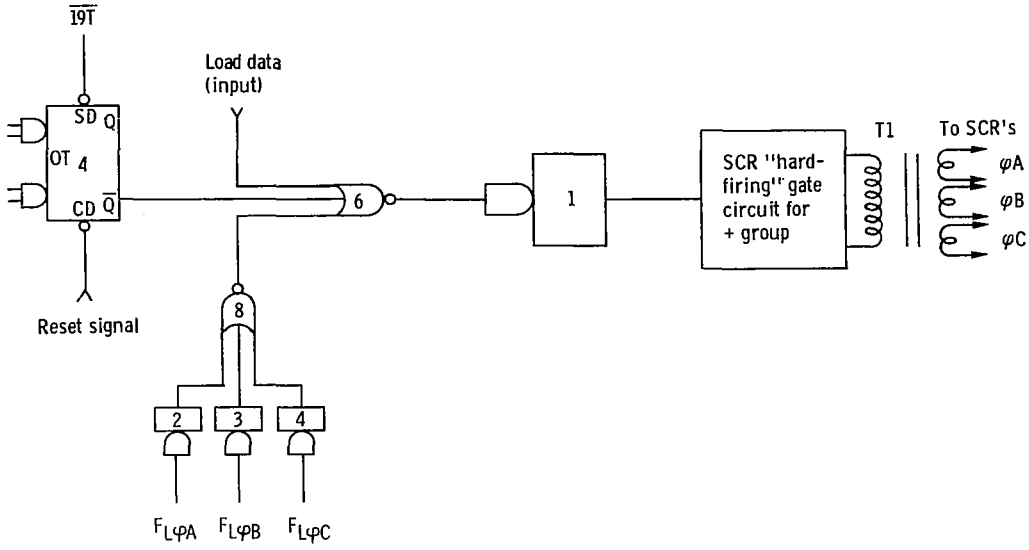


Figure 10. - Block diagram for power output stage (+ group).

NOR gate 6 controls the monostable one-shot multivibrator (1). The one shot, together with a high-level SCR gate signal, is used to provide "hard-firing" of the silicon-controlled rectifiers and to minimize the duration of gate power applied to the silicon-controlled rectifiers. FF4, NOR gates 6 and 8, and one-shot 1 provide the firing logic for the + group of SCR's. A similar arrangement of logic modules controls the - group.

"Hard-firing" is defined as the application of the maximum rated direct-current triggering current and/or voltage to the gate of an SCR, wherein the buildup of the current wave shape is very short (<25 percent) when compared to the device turnon time. A separate 15-volt power supply is used for the SCR gate circuits. The gate signal is coupled to the SCR by use of a pulse transformer. The pulse transformer T1 was incorporated into the firing circuit to balance out the delay caused by the addition of the pulse transformer T2. Transformer T2 is required for decoupling of the ground between the negative group of silicon-controlled rectifiers and their respective firing circuits.

The actual turnon of the SCR may be delayed and is a function of several parameters, such as the instantaneous value of line voltage, the line frequency, the SCR turnon time, the alternator armature inductance, and the number of discrete parasitic-load steps. This delay is expected to be of the order of 1 degree.

The maximum time required to change from one unit of parasitic load to another is nominally 42.5 milliseconds (time to reach 17TR2). The system ramifications of switching from one load to another are discussed further in the section FREQUENCY ERROR ANALYSIS.

Power Consumption

The digital speed controller as illustrated in appendix A consists of NAND and NOR type logic modules, flip-flop multivibrators, one-shot multivibrators, inverters, a crystal oscillator, silicon-controlled rectifiers, and the associated power supplies required for these components. The estimated quantity of each of these components is listed in the following table:

Component	Quantity
NAND/NOR gate	120
FF multivibrator	60
FF one-shot multivibrator	42
Inverting amplifier	6
Crystal oscillator	1
Silicon-controlled rectifier	30
Power supply	3

The power consumption within these components is approximately 175 watts at minimum parasitic load. Approximately 60 percent of this power loss is consumed in the associated power supplies. The power consumption at maximum parasitic load is approximately 475 watts. This additional power loss (300 W) is consumed in the power-output stage, specifically in the silicon-controlled rectifiers and their firing circuits. These losses in the power-output stage do not affect system efficiency; however, they do increase the thermal load on the coolant system. The system efficiency is determined at a maximum useful (vehicle) load condition (minimum parasitic load).

FREQUENCY ERROR ANALYSIS

The topics of concern here are the effect of the various delays generated by the component propagation delays and the synchronizing technique on the speed controller.

Propagation Delays Associated With the Deviation Error Signal

In order to minimize the timing errors of the speed controller, the synchronism or coincidence between the ϵ^+, f_{ref}, 1-megahertz subcarrier and the 16th count of the period counter must be maintained. These signals combine to generate the frequency

error signal supplied to the temporary storage subcircuit of the magnitude error detector.

The circuit as shown in figure 6 illustrates this relation for line frequencies where $f_{line} > f_{ref}$. The ϵ^+ synchronism with the reference frequency f_{ref} is illustrated in the timing drawing of figure 6. Since NAND logic gates have an average propagation delay of 50 nanoseconds (80 nsec max, ref. 7), the 1-megahertz subcarrier will require the insertion of an additional delay using NAND logic modules to maintain the synchronism through NAND gate 11. The 1-megahertz subcarrier is generated at the same time as the f_{ref} signal. The synchronism of the 1-megahertz subcarrier through NAND gate 11 maintains the synchronism of the right terminus of the subcarrier pulses with the right terminus of the difference signal ϵ^+. The importance of this synchronism is discussed in the section Speed-Controller Transfer Frequencies.

Likewise, the synchronism of the 16th period count (right terminus) has to be maintained with the pulse error count signal (output of NAND gate 11). A time shift between these two signals could result in the loss of 1 or more error counts. This would result in an incorrect parasitic-load application for a given useful load condition (line frequency). This time shift would be controlled by the addition of a delay to the period count circuit. The relative delays incurred by the various circuit functions are as indicated in figure 11. The total delay is of the order of 2000 nanoseconds. The amount of added delay would depend upon the particular speed-controller prototype. The IC modules contain several circuit functions; for instance, four logic gates are available on one circuit module. The magnitude of these additional delays would be determined during the speed-controller initial checkout. This would be incorporated as a calibration procedure following fabrication. Appendix A illustrates the location of these circuits as required to balance out the propagation errors.

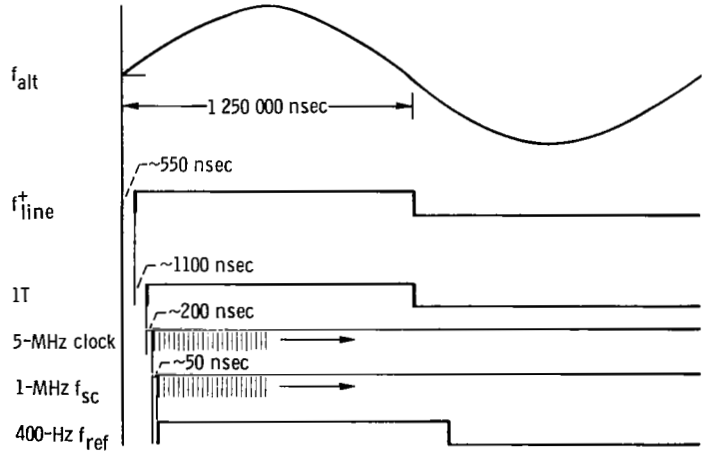


Figure 11. - Relative delays in generation of pulse error count (uncompensated) (not to scale).

Speed-Controller Transfer Frequencies

The object of this section is to determine the range of frequencies in which the speed controller switches from one value of parasitic load to another. From the timing diagram of figure 6, it can be seen that the terminus (right side) of the frequency difference signal ϵ^+ is synchronous with the reference frequency f_{ref}, and the left side is synchronous with the line frequency f_{line}.

This difference signal ϵ^+ is combined with the 1-megahertz subcarrier frequency (f_{sc}) to generate a pulse error count (ϵ^+) (f_{sc}) as indicated in figure 12.

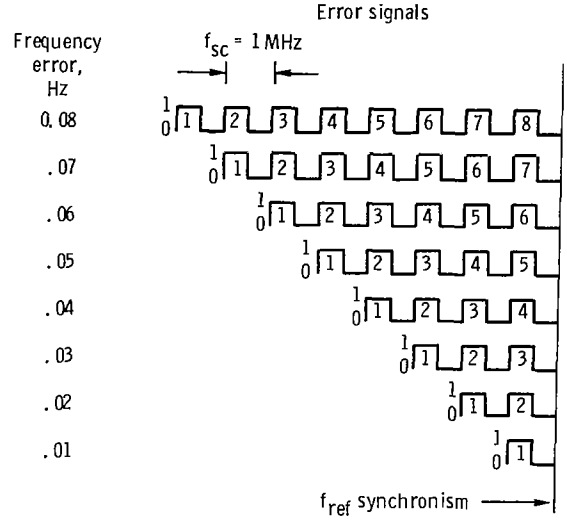


Figure 12. - Deviation error detector output.

Figure 12 not only indicates the relation between the frequency error and the number of logic error pulses but more importantly illustrates the time relation between the 1-megahertz subcarrier and the ϵ^+ (difference) signal. As discussed in the previous section, the right sides (termini) of both the subcarrier and the difference signal are in coincidence by the use of inserted delays.

To determine the line frequency at which the speed controller switches parasitic load, assume the logic circuits do not respond to a pulse width less than 50 nanoseconds. The possible speed-controller switching times for a frequency error of 1 count are shown in figure 13.

The difference signal ϵ^+ as shown in figure 13 is continuously variable. The difference signal is illustrated as the difference between f_{line} synchronism and f_{ref} synchronism. The figure indicates the relation to obtain 1 error pulse (1 MHz). The

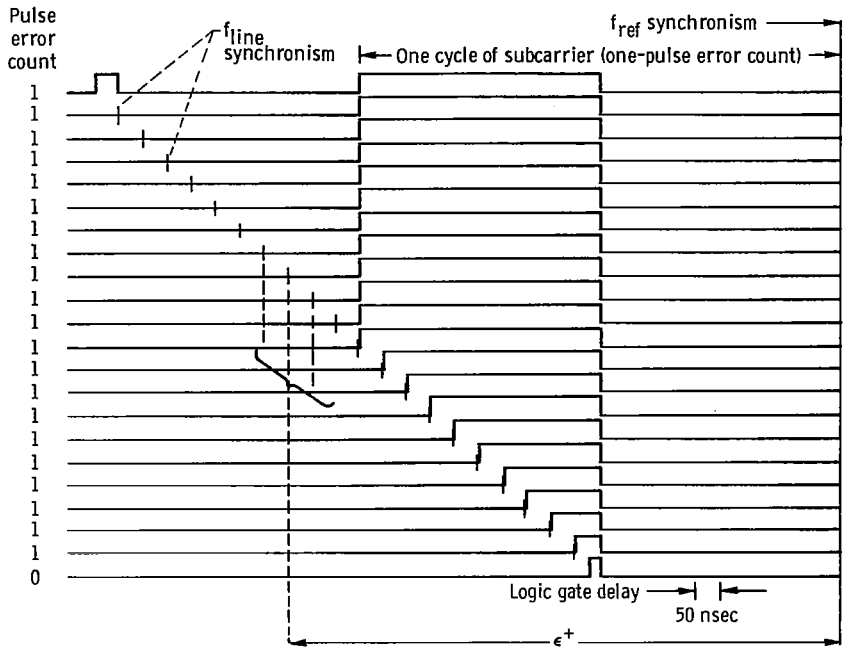


Figure 13. - Range of positive difference error signal ϵ^+ for error count of 1.

time base of the difference signal ϵ^+ therefore can vary from 550 to 1550 nanoseconds and still contain only the 1 error pulse. The bottom wave shape of figure 13 indicates a zero error count since the difference signal ϵ^+ is less than 50 nanoseconds.

Based on this variation of ϵ^+, the lower limit of f_{line} and the upper limit of f_{line} at which the parasitic load will transfer is determined by the following analysis. The time base for a half cycle of f_{line} is

$$\frac{550 \text{ nsec}}{31 \text{ half cycles}} = 17.74 \text{ nsec/half cycle}$$

$$\frac{1550 \text{ nsec}}{31 \text{ half cycles}} = 50.00 \text{ nsec/half cycle}$$

where 31 is the number of half cycles through the 16th period count. The period error between f_{ref} and f_{line} is

$$t_{ref} - t_{line} = (2)\ (17.74 \text{ nsec}) = 35.48 \text{ nsec} \quad (2)$$

$$t_{ref} - t_{line} = (2)\ (50 \text{ nsec}) = 100 \text{ nsec} \quad (3)$$

However

$$t_{ref} = 2\ 500\ 000 \text{ nsec}$$

From equation (2)

$$t_{\text{line lower limit}} = 2\ 499\ 964.52 \text{ nsec}$$

From equation (3)

$$t_{\text{line upper limit}} = 2\ 499\ 900.00 \text{ nsec}$$

Then

$$f_{\text{line lower limit}} = \frac{1}{2\ 499\ 964.52 \text{ nsec}} = 400.0056768 \text{ Hz}$$

$$f_{\text{line upper limit}} = \frac{1}{2\ 499\ 900.00 \text{ nsec}} = 400.0160006 \text{ Hz}$$

Therefore, the speed controller will switch from 1 unit of power to 2 units of power at an alternator frequency ≥400.016 hertz. The speed controller will switch from 1 unit of power to zero units of power at an alternator line frequency ≤400.00567 hertz. Table V lists the transfer frequencies for unit loads from zero to 8. Note that adjacent loads transfer at the same frequency. Figure 14 graphically illustrates this range of

TABLE V. - SPEED-CONTROLLER TRANSFER FREQUENCIES

Parasitic load		Transfer frequency, Hz
Initial	Final	
0	1	400.0057
1	2	400.0160
2	3	400.0263
3	4	400.0366
4	5	400.0470
5	6	400.0573
6	7	400.0676
7	8	400.0780

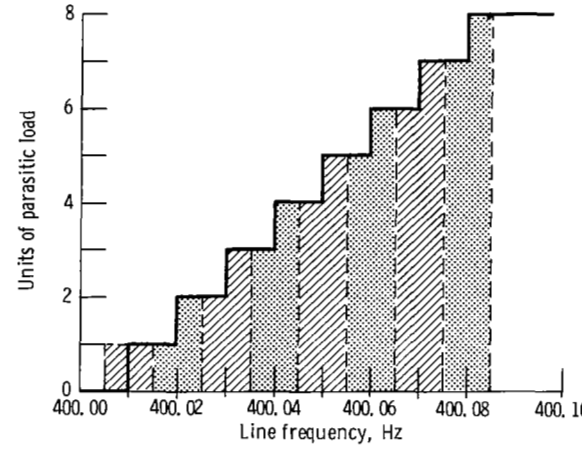


Figure 14. - Transfer frequency of speed controller for increments of line frequency.

transfer frequencies as a function of the control characteristic previously discussed in figure 2. The significant feature of figure 14 is that the transfer of parasitic load takes place without any overlap in frequency. An overlap in load transfer frequency presents load instabilities.

The transfer frequencies for adjacent loads can be separated. This in effect would generate a frequency dead band between the adjacent values of parasitic load. The technique would effectively consist of subdividing the first pulse error count and would thereby determine where in the cycle f_{line} synchronism occurs (see fig. 13). This information would be used to increase or decrease the number in the temporary storage counter by 1 count. This modification would involve gating on a separate output signal from the 5-megahertz frequency reference during the first pulse error count. The number of 5-megahertz pulses which are counted would modify the output signal of the temporary storage counter by 1 count. It would be necessary to change the configuration of the temporary counter from an up-count to an up-count, down-count counter like that used in the permanent storage counter circuit (ref. 8). This modification to provide a control dead band was not included in this design since the need for a control dead band was considered unnecessary at this time.

PROPOSED SPEED-CONTROLLER CIRCUIT

Subcircuit Analysis

The system parameters of a proposed speed controller are discussed in this section. The conceptual speed controller as discussed to this point served to establish the basis for the design approach. The system parameters of these two concepts are itemized in table VI. The proposed speed controller incorporates a digital vernier (fine control)

TABLE VI. - COMPARISON OF SPEED-CONTROLLER CONCEPTS

Speed-controller concept	Logic type	Number of PLR steps	Discrete number of PLR loads	Parasitic power/ Load step	Relative voltage modulation	Relative frequency modulation	Subcarrier frequency, f_{sc}, MHz	Period of continuous range, t_{cr}, μsec (a)	Error pulse count	Sampling delay, cycles
A	5 percent TTL, 95 percent DTL	8	5	$P_{alt}/8$	1.0	1.0	1	0.4999	8	16
B	25 percent TTL, 75 percent DTL	40	8	$P_{alt}/40$	.2	.2	5	.4999	40	16

[a] Period of control range $= \frac{1}{f_{ref}} - \frac{1}{f_{zero\ useful\ load}} = \frac{\Delta f}{(f_{ref})(f_{zero\ useful\ load})}$.

feature for the purpose of reducing the magnitude of the parasitic power fluctuation and thereby the frequency modulation level.

The fine control feature (vernier) is obtained by changing the subcarrier frequency to 5 megahertz and using the increased number of error pulse counts to apply additional units of parasitic load (PLR).

The basic equation relating the speed-controller parameters is

$$\text{Number of parasitic load steps} = (\text{Sampling delay})\left(\frac{1}{f_{ref}} - \frac{1}{f_{\text{zero useful load}}}\right)(f_{sc}) \qquad (4)$$

As can be seen, the three parameters determining the number of parasitic load steps are (1) the sampling delay, (2) the period of the control range, and (3) the frequency of the subcarrier. The sampling delay is defined as the number of cycles of alternator line frequency which occur, after the start of a sampling cycle, before the number of subcarrier pulses are counted (which determines the error pulse count). The period of the control range is defined as $1/f_{ref} - 1/f_{\text{zero useful load}}$. The first two parameters reflect directly in the performance of the speed control system. The third parameter, the subcarrier frequency, does not appear in the system characteristics; therefore, it can be changed without affecting the performance limits of the system.

In reference to equation (4), the sampling delay remains at 16 cycles. This results in the speed controller maintaining the same response time for a change in system frequency. The period of the control range $1/f_{ref} - 1/f_{\text{zero useful load}}$ remains the same at 0.4999 microsecond. (The control range in terms of frequency remains at 0.08 Hz.) The gain of the frequency loop within the power generating system will remain unchanged and as a result should not present any additional control problems. The error pulse count, using the 5-megahertz subcarrier, is five times the previous error pulse count. The maximum error pulse count is 40, as compared with the previous pulse count of 8. As before, the number of parasitic-load steps is equal to the error pulse count. This results in the parasitic load having 40 steps.

The availability of an error pulse count of 40 results in the parasitic-load line frequency relation indicated in table VII. The proposed speed controller incorporates a coarse-fine control function, where the fine control consists of the tenth values (0.2, 0.4, 0.6, 0.8) and the coarse control consists of the values 1.0, 2.0, 3.0, 4.0, and 5.0.

The decoder conversion would take the form illustrated in table VIII. The number of physical parasitic loads required to provide the 40 parasitic-load steps is 8.

The same parasitic-load element use factor consideration applies to the fine control feature as to the coarse control. The fine control consists of two elements rated at a 0.2 value of parasitic load and one element rated at a 0.4 value. The development of the diode matrix circuit for this code converter is not detailed here; however, the procedure

TABLE VII. - PARASITIC-LOAD TRANSFER FREQUENCIES FOR

40 ERROR PULSE COUNT

Pulse error count	Line frequency, Hz	Parasitic load	Pulse error count	Line frequency, Hz	Parasitic load
1	400.002	0.2	21	400.042	4.2
2	400.004	.4	22	400.044	4.4
3	400.006	.6	23	400.046	4.6
4	400.008	.8	24	400.048	4.8
5	400.010	1.0	25	400.050	5.0
6	400.012	1.2	26	400.052	5.2
7	400.014	1.4	27	400.054	5.4
8	400.016	1.6	28	400.056	5.6
9	400.018	1.8	29	400.058	5.8
10	400.020	2.0	30	400.060	6.0
11	400.022	2.2	31	400.062	6.2
12	400.024	2.4	32	400.064	6.4
13	400.026	2.6	33	400.066	6.6
14	400.028	2.8	34	400.068	6.8
15	400.030	3.0	35	400.070	7.0
16	400.032	3.2	36	400.072	7.2
17	400.034	3.4	37	400.074	7.4
18	400.036	3.6	38	400.076	7.6
19	400.038	3.8	39	400.078	7.8
20	400.040	4.0	40	400.080	8.0

TABLE VIII. - DECODER BINARY TO SPECIAL CODE CONVERSION FOR VARIOUS PULSE ERROR COUNTS

Pulse error count (base 10)	Binary input						Parasitic load								Frequency deviation, Hz
	2^0	2^1	2^2	2^3	2^4	2^5	0.2	0.2	0.4	1_1	1_2	2_1	2_2	2_3	
	Special code input						Special code output								
0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0.000
1	1	0	0	0	0	0	1	0	0	0	0	0	0	0	.002
2	0	1	0	0	0	0	1	1	0	0	0	0	0	0	.004
3	1	1	0	0	0	0	0	1	1	0	0	0	0	0	.006
4	0	0	1	0	0	0	1	1	1	0	0	0	0	0	.008
5	1	0	1	0	0	0	0	0	0	1	0	0	0	0	.010
6	0	1	1	0	0	0	1	0	0	1	0	0	0	0	.012
7	1	1	1	0	0	0	1	1	0	1	0	0	0	0	.014
8	0	0	0	1	0	0	0	1	1	1	0	0	0	0	.016
9	1	0	0	1	0	0	1	1	1	1	0	0	0	0	.018
10	0	1	0	1	0	0	0	0	0	1	1	0	0	0	.020
11	1	1	0	1	0	0	1	0	0	1	1	0	0	0	.022
12	0	0	1	1	0	0	1	1	0	1	1	0	0	0	.024
13	1	0	1	1	0	0	0	1	1	1	1	0	0	0	.026
14	0	1	1	1	0	0	1	1	1	1	1	0	0	0	.028
15	1	1	1	1	0	0	0	0	0	0	1	1	0	0	.030
16	0	0	0	0	1	0	1	0	0	0	1	1	0	0	.032
17	1	0	0	0	1	0	1	1	0	0	1	1	0	0	.034
18	0	1	0	0	1	0	0	1	1	0	1	1	0	0	.036
19	1	1	0	0	1	0	1	1	1	0	1	1	0	0	.038
20	0	0	1	0	1	0	0	0	0	1	1	0	1	0	.040
21	1	0	1	0	1	0	1	0	0	1	1	0	1	0	.042
22	0	1	1	0	1	0	1	1	0	1	1	0	1	0	.044
23	1	1	1	0	1	0	0	1	1	1	1	0	1	0	.046
24	0	0	0	1	1	0	1	1	1	1	1	0	1	0	.048
25	1	0	0	1	1	0	0	0	0	1	0	0	1	1	.050
26	0	1	0	1	1	0	1	0	0	1	0	0	1	1	.052
27	1	1	0	1	1	0	1	1	0	1	0	0	1	1	.054
28	0	0	1	1	1	0	0	1	1	1	0	0	1	1	.056
29	1	0	1	1	1	0	1	1	1	1	0	0	1	1	.058
30	0	1	1	1	1	0	0	0	0	1	1	1	0	1	.060
31	1	1	1	1	1	0	1	0	0	1	1	1	0	1	.062
32	0	0	0	0	0	1	1	1	0	1	1	1	0	1	.064
33	1	0	0	0	0	1	0	1	1	1	1	1	0	1	.066
34	0	1	0	0	0	1	1	1	1	1	1	1	0	1	.068
35	1	1	0	0	0	1	0	0	0	0	1	1	1	1	.070
36	0	0	1	0	0	1	1	0	0	0	1	1	1	1	.072
37	1	0	1	0	0	1	1	1	0	0	1	1	1	1	.074
38	0	1	1	0	0	1	0	1	1	0	1	1	1	1	.076
39	1	1	1	0	0	1	1	1	1	0	1	1	1	1	.078
40	0	0	0	1	0	1	0	0	0	1	1	1	1	1	.080

is outlined in appendix B for the conceptual design case.

The modulation of the alternator output voltage wave, as discussed in the section SPEED-CONTROL SYSTEM, is the result of applying loads of varying magnitude to the alternator. The voltage modulation level (table VI) relates the modulation of the conceptual speed controller (concept A) to that of the proposed version (concept B).

As noted, the voltage modulation for speed controllers having 40 parasitic-load steps is approximately 20 percent of the conceptual design having 8 load steps. This level of modulation represents a worst case condition since it assumes the voltage regulator will not respond to load changes occurring at a 200-hertz rate. The level of modulation would be reduced if the regulator did respond to a load rate of this magnitude. The absolute magnitude of voltage modulation, and frequency modulation as well, has not been computed.

The modifications to the basic speed controller as required to obtain 40 levels of parasitic load are the following:

(1) The frequency of the subcarrier would be changed from 1 to 5 megahertz.

(2) The logic circuits in the deviation error detector and the magnitude error detector would require the use of TTL logic modules instead of the DTL modules.

(3) The storage capacity of the temporary storage subcircuit and the permanent storage subcircuit would have to be increased from the present count of 15 (max) to a count of 63 (max). Specifically, six bistable flip-flops would be required in each storage register instead of the present four.

(4) The special decoder would take the form illustrated in table VIII. This would replace the decoder for the basic speed-controller concept.

(5) The number of power-output stages and discrete parasitic-load registors (PLR's) would increase to eight from the present five.

Operation at Higher Frequencies

The digital speed controller is designed for use on a 400-hertz power generating system. The information presented in this section considers the modifications and performance characteristics resulting from operation at a higher line frequency. A line frequency of 1200 hertz was arbitrarily chosen for this analysis. Equation (4) relates the various parameters at the speed controller. The number of discrete PLR's will change from five to eight (40 steps). The sampling delay will be increased by a factor of 3 to 48 (the ratio of line frequency). This selection for the sampling delay maintains the response of the speed controller to a change in frequency at approximately 50 milliseconds. The frequency control range in this example will remain at 0.08 hertz, which results in a period for the control range of 55.5 nanoseconds. This assumption maintains the present relation of 1 error pulse count for each step.

Based on these assumptions, the resultant subcarrier frequency (from eq. (4)) is 15 megahertz.

A 15-megahertz subcarrier requires the use of second-generation TTL logic modules which have a propagation delay of approximately 6 nanoseconds. An analysis of the switching frequency, as dicsussed in the section Speed-Controller Transfer Frequencies, indicates the difference signal ϵ^+ can vary from 39.33 to 105.99 nanoseconds for 1 error pulse. This results in an f_{line} lower limit of 1200.001672 hertz and an f_{line} upper limit of 1200.002086 hertz. Since the speed controller applies load in 0.002-hertz increments, the f_{line} lower limit must be $\geq$1200.00 1 hertz, while the f_{line} upper limit must be $\leq$1200.003 hertz. The magnitudes of the f_{line} lower limit and the f_{line} upper limit as computed above are in agreement with this limitation.

The design of a speed controller for operation at 1200 hertz would require a change in the frequency reference, including the countdown circuit, in the maximum count capacity of the f_{line} period counter, and to TTL logic modules, in the deviation error detector, magnitude error detector, and strobe generator. The hardware is commercially available to provide these functions.

Operation at Lower Power Level per Speed-Controller Load Step

The power level at which a given digital speed controller can perform is governed by the number of discrete parasitic-load steps within the controller. The effect of decreasing the power level results in a decrease in voltage modulation on the alternator output for a given speed-controller design. Previous investigations indicate the voltage change at the useful load bus is directly proportional to the magnitude of the load change relative to the alternator capacity. This assumes that the frequency corresponding to the speed-controller sampling cycle is higher than that frequency which the voltage regulator can follow. For modulation frequencies within the response capability of the voltage regulator, the level of modulation would be less.

As a first-order approximation, the voltage change at the alternator load bus for a change in load can be defined by

$$\Delta V = \frac{E_{line}}{\text{Number of effective PLR steps}} \tag{5}$$

where E is the root-mean-square alternator voltage. Since voltage modulation is defined as

$$\text{Percent voltage modulation} = \frac{E_{max} - E_{min}}{E_{max} + E_{min}} (100)$$

the voltage modulation can be expressed in terms of parasitic-load steps as

$$\text{Percent voltage modulation} = \frac{50}{\text{Number of effective PLR steps}} \tag{6}$$

A speed controller having 40 parasitic load steps would generate a voltage modulation level of approximately 1.25 percent. The frequency of this modulation could vary from nearly zero to 3 percent of line frequency, depending on the specific value of line frequency for a given power system. This relation applies for all digital-speed-controller designs in which the sampling delay varies directly with the system frequency.

SUMMARY OF RESULTS

An investigation of a parasitic-loading digital speed controller for a 400-hertz turbine-driven alternator produced the following results:

1. The range of frequency control for the speed controller is 0.02 percent (0.08 Hz).
2. The recovery time for a step load change is nominally 50 milliseconds.
3. With the addition of the fine-course feature (40-step parasitic load), the voltage modulation would be nominally $1\frac{1}{4}$ percent.
4. The speed controller has the capability of being scaled for operation at different alternator frequencies and power levels.

Lewis Research Center,
National Aeronautics and Space Administration,
Cleveland, Ohio, July 26, 1971,
120-27.

APPENDIX A

PROPOSED DIGITAL SPEED CONTROLLER

The schematic diagram of the conceptual digital speed controller is presented in figure 15. The figure illustrates the required subcircuits except those within the IC packages (which are from a commercial supplier) and the special decoder. The decoder subcircuit is presented separately in appendix B.

The schematic diagram includes all power supplies and the startup logic. The startup logic involves delaying the turnon of the synchronous counters in the frequency reference and the f_{line} period counter until the initial reset pulse has occurred. This sequence resets all the IC storage modules and thereby removes any data the speed controller may have retained from previous use.

A timing diagram for the speed controller is illustrated in figure 16. The relation among the significant signals as generated by the various subcircuits is presented in this figure. Figure 16, when used in conjunction with figure 15, will simplify the task of determining the generation and the flow of a frequency error signal through the speed controller. The signal flow chart, table IX, provides a guide to the sequential operation of the various subcircuits. The signal flow is itemized as a function of the line frequency f_{line} period count. The chart follows the progression of the error signal through the speed controller for an assumed load transient which generates frequency errors during consecutive sampling periods of 0.10, 0.01, -0.01, and 0.01 hertz. The signal flow is initiated at the beginning of a sampling cycle in which the f_{line} period counter has a zero count.

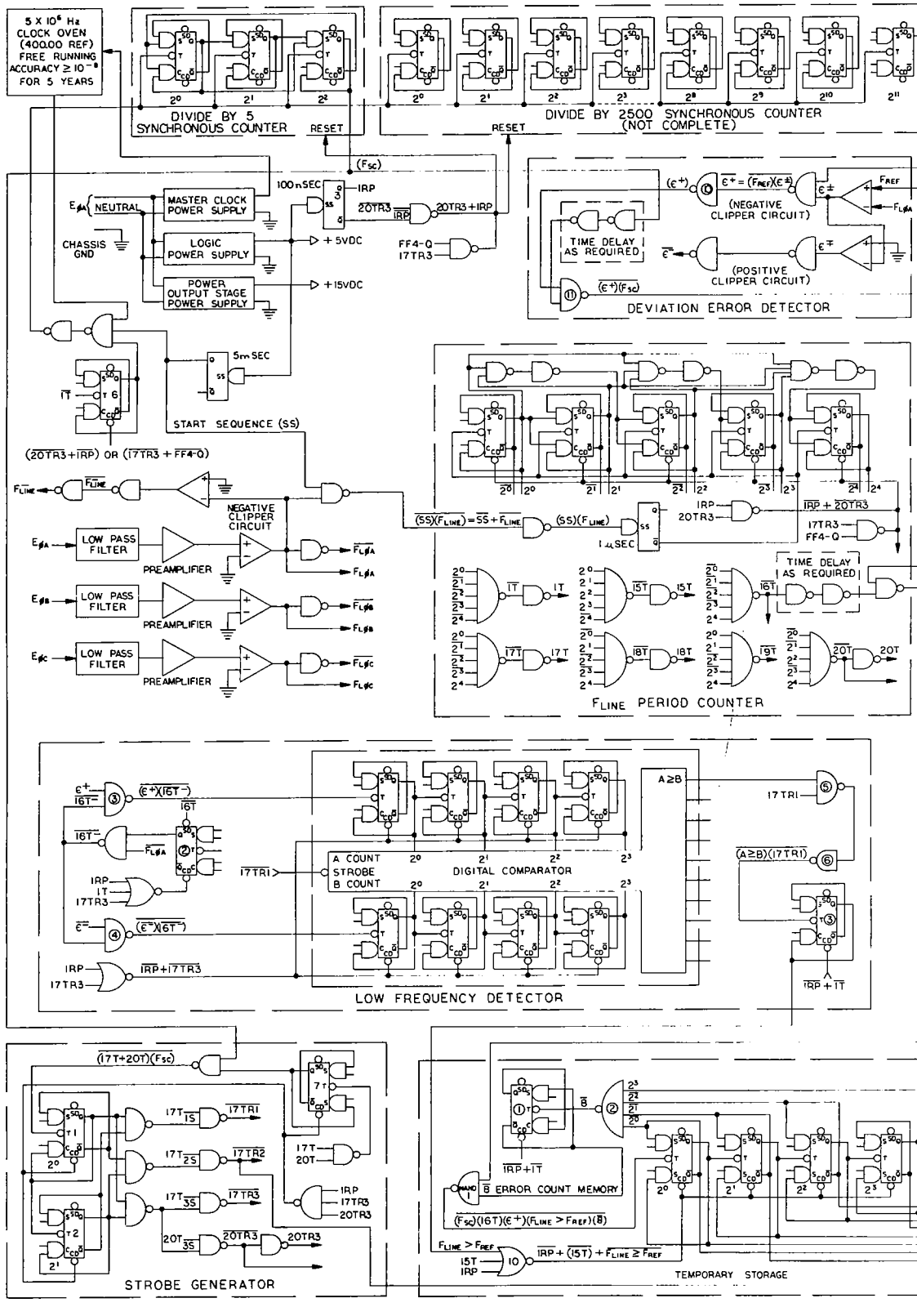
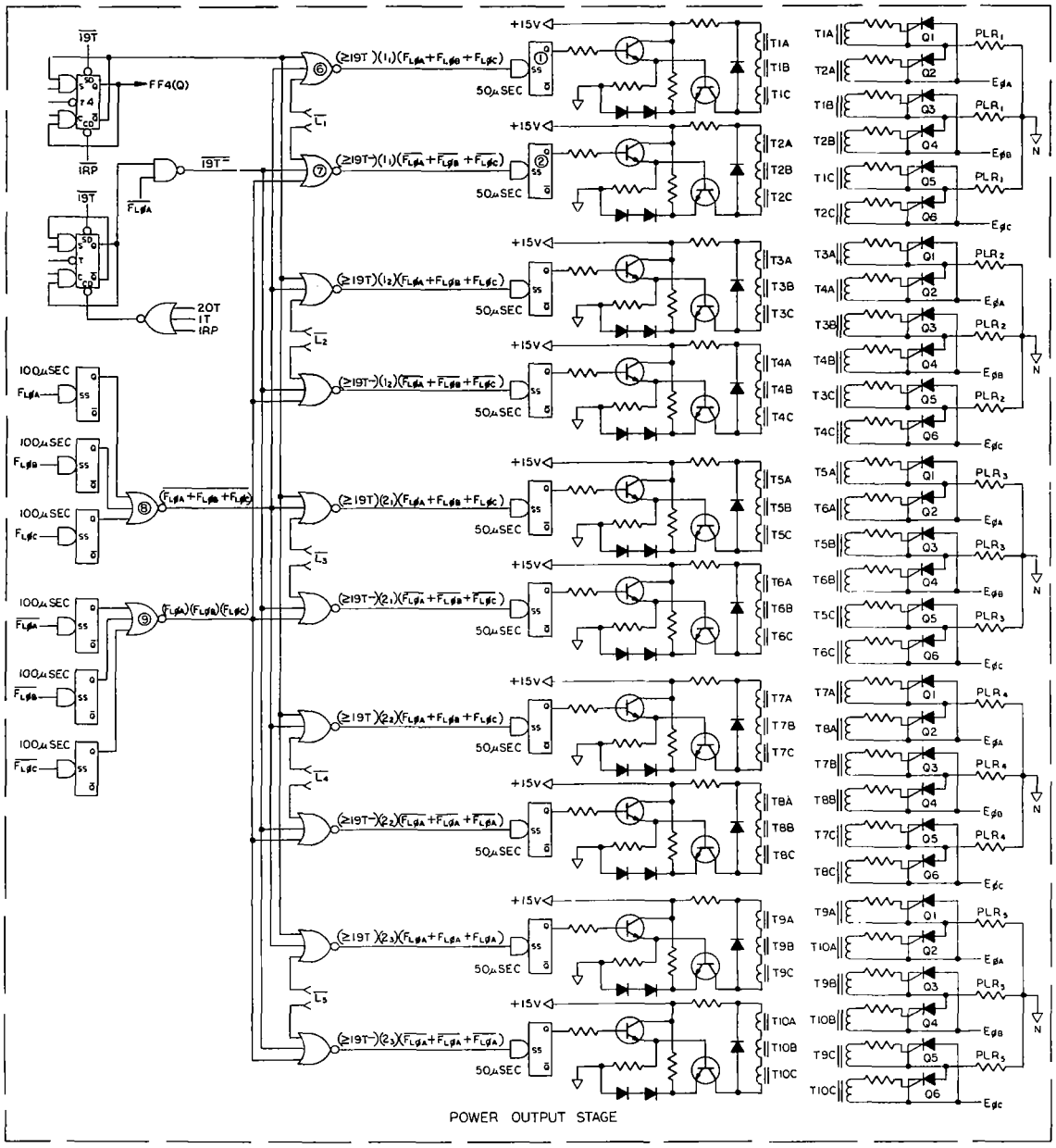
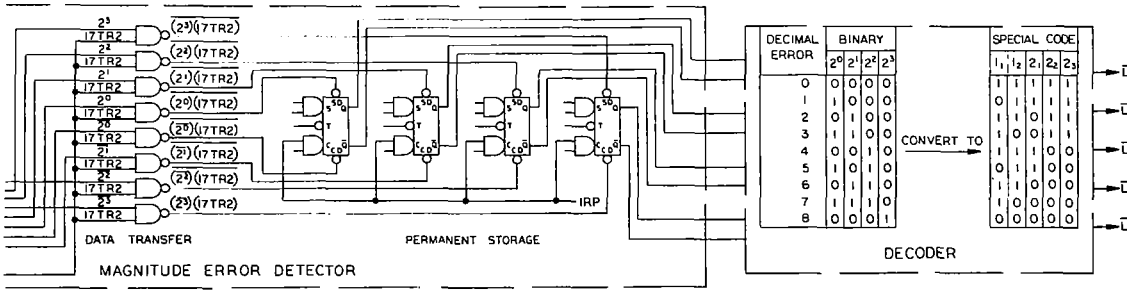


Figure 15. - Schematic diagram





of digital speed controller.

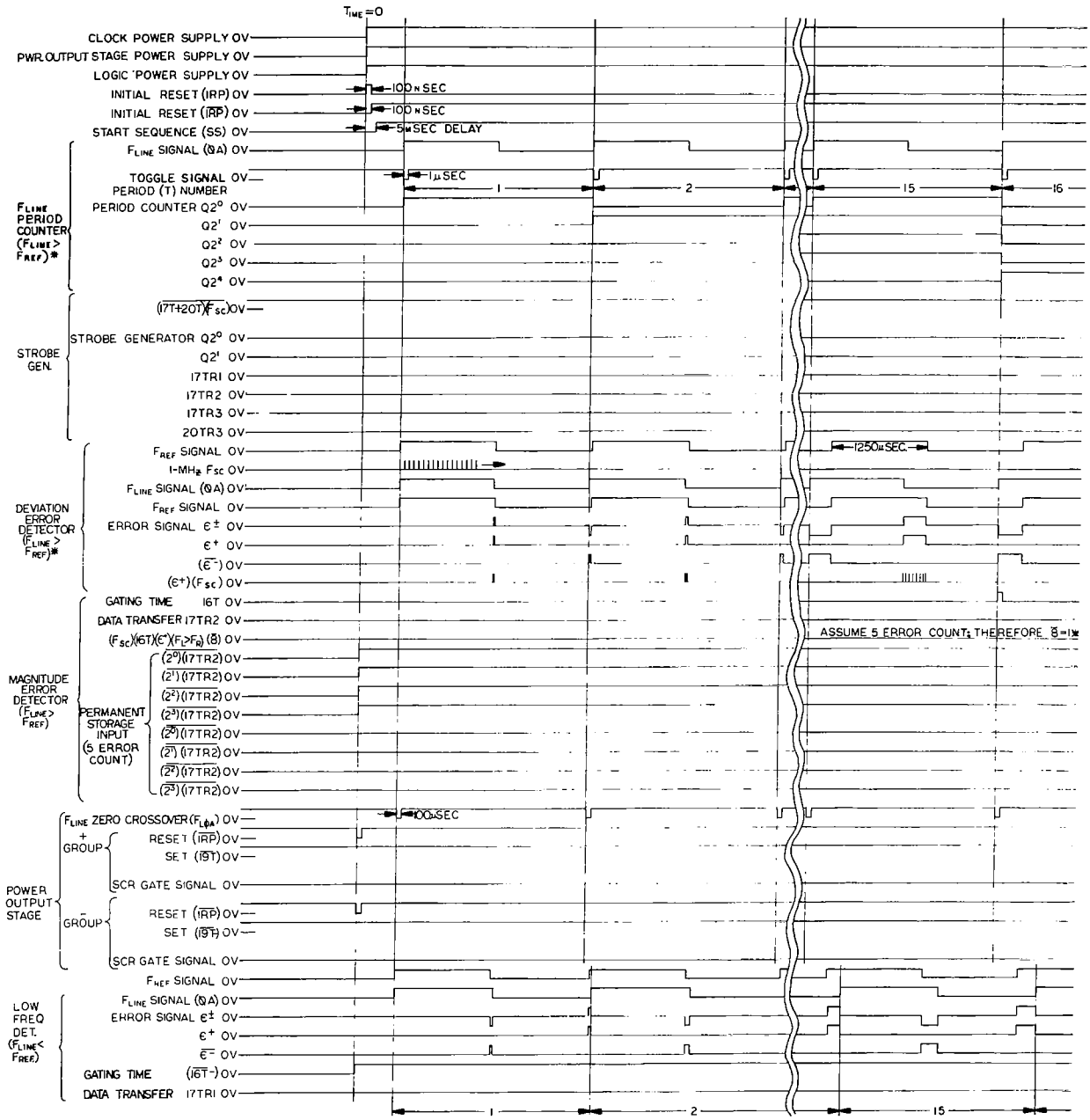
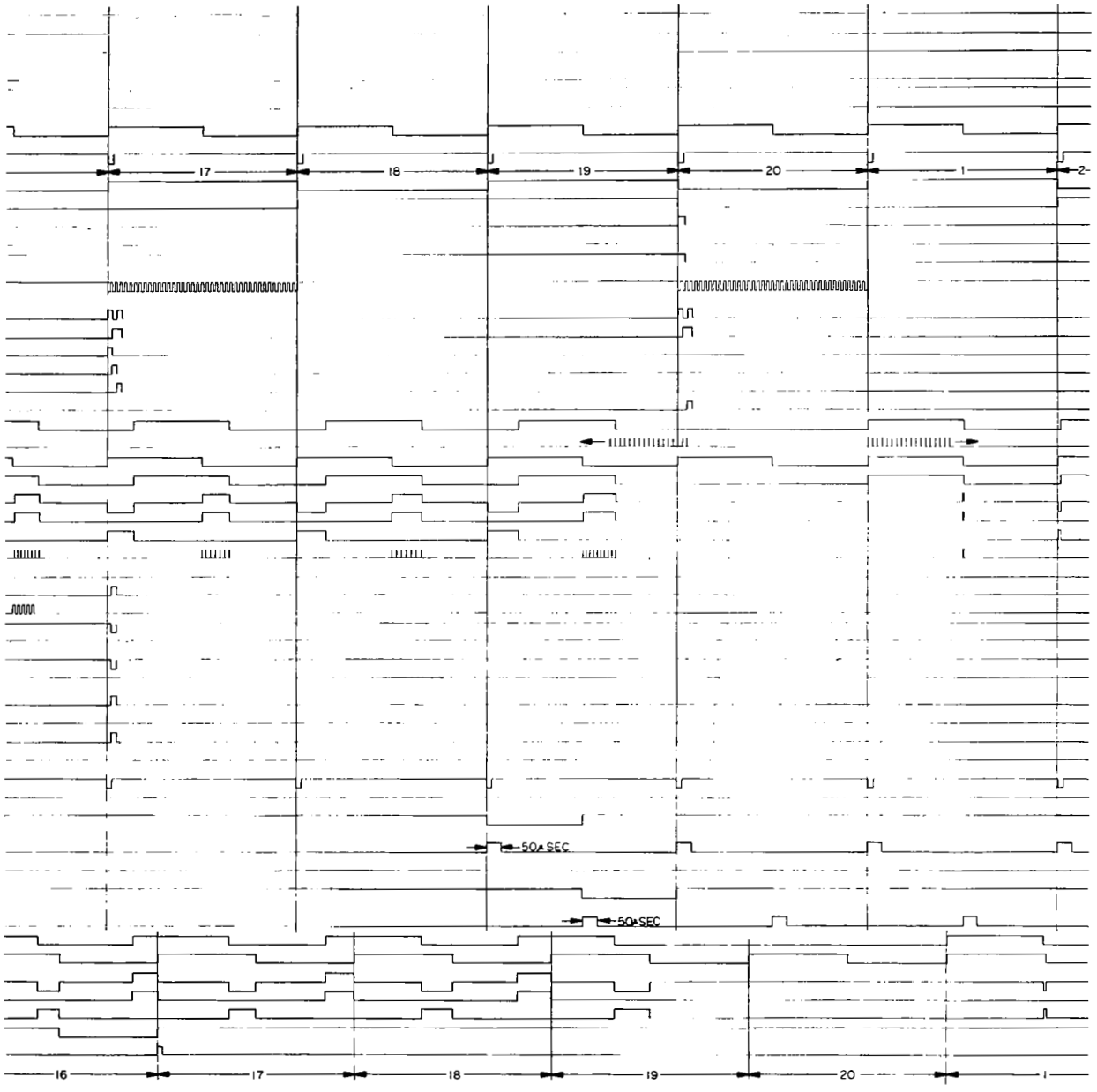


Figure 16. - Timing diagram for digital speed controller. Asterisk denotes assumption of full waveform of f_{line}.



this is not necessarily true, but after 17 T, this assumption is valid. Sampling cycles after startup cycle end at 17 T.

TABLE IX. - SIGNAL FLOW CHART FOR DIGITAL SPEED CONTROLLER

Logic signal, time/f_{line} count[a]	Circuit response
1T	f_{line} period counter active, FF2 is set 0 to 1(Q) FF6 is set from 0 to 1(Q) FF1 is reset to $1(\overline{Q})$ FF3 is reset to 0(Q)
2T to 14T	f_{line} period counter active
15T	Temporary storage is reset to 0000
16T	Pulse error count gated into temporary storage; assume pulse error count of 10, 8 does inhibit NAND-1
$16.5T\left[\overline{16T^-}\right]$	ϵ^+ and $\overline{\epsilon^-}$ gated into low-frequency detector; error count stored in temporary storage is 8; low-frequency detector output signal ($A \geq B$) is zero V
17T	f_{sc} is gated into strobe generator
17TR1	Low-frequency detector strobe is activated; $A > B$ signal is stored in FF3, where $A > B = f_{line} > f_{ref}$ Note: Assume that $A > B$ (i.e., $f_{line} > f_{ref}$) and normal output (Q) of FF3 does not reset temporary storage to 0000
17TR2	Temporary storage error count is transferred into permanent storage; permanent storage data are transferred into special decoder 1_1 load data are gated into Q1 gate circuit at f_{line} $(\varphi A)^a$, into Q3 gate circuit at f_{line} $(\varphi B)^a$, into Q5 gate circuit at f_{line} $(\varphi C)^a$ 1_1 load data are gated into Q2 gate circuit at f_{line} $(\varphi A)^a$, into Q4 gate circuit at f_{line} $(\varphi B)^a$, into Q6 gate circuit at f_{line} $(\varphi C)^a$ 50 μsec pulse is applied to Q1, which is conducting, Q3, which is conducting, and Q5, which begins to conduct
17TR3	Gates off f_{sc} into strobe generator and resets same from 11 to 00 Resets FF6 from 1 to 0; this signal gates off clock (5 MHz) and resets divide-by-5 and divide-by-2500 counters f_{line} period counter is reset to 00000

[a]At leading edge.

TABLE IX. - Continued. SIGNAL FLOW CHART FOR DIGITAL SPEED CONTROLLER

Logic signal, time/f_{line} count[a]	Circuit response
1T	Sets FF6, which gates clock into divide-by-5 and divide-by-2500 counters Sets FF2 from 0 to 1; ϵ^+ and $\overline{\epsilon^-}$ are gated into low-frequency detector Resets FF1 to 1($\overline{Q}$) Resets FF3 to 0(Q) f_{line} period counter active
2T to 14T	f_{line} period counter active
15T	Temporary storage is reset to 0000
16T	Pulse error count gated into temporary storage Assume pulse error count of 1
16.5T[$\overline{16T^-}$]	ϵ^+ and $\overline{\epsilon^-}$ are gated into low-frequency detector
17T	f_{sc} is gated into strobe generator
17TR1	Low-frequency detector strobe is activated; A > B (assumed) signal is stored in FF3, where A > B = $f_{line} > f_{ref}$
17TR2	Temporary storage error count is transferred into permanent storage Permanent storage data are transferred into special decoder; this error is then applied to SCR circuits 50 μsec pulse is applied to SCR gates
17TR3	Gates off f_{sc} into strobe generator and resets same from 11 to 00 Resets FF6 from 1 to 0; this signal gates off clock and resets divide-by-5 and divide-by-2500 counters f_{line} period counter is reset to 00000
1T	Next f_{line} period arrives; f_{line} period counter active Sets FF6, which gates clock into divide-by-5 counter Sets FF2 from 0 to 1; ϵ^+ and $\overline{\epsilon^-}$ are gated into low-frequency detector Resets FF1 to 1($\overline{Q}$) Resets FF3 to 0(Q)

[a]At leading edge.

TABLE IX. - Concluded. SIGNAL FLOW CHART FOR DIGITAL SPEED CONTROLLER

Logic signal, time/f_{line} count[a]	Circuit response
2T to 14T	f_{line} period counter active
15T	Temporary storage is reset to 0000
16T	Pulse error count is gated into temporary storage Assume pulse error count of -1 (i.e., magnitude 1, and $f_{ref} > f_{line}$)
16.5T$\left[\overline{16T^{-}}\right]$	ϵ^{+} and $\overline{\epsilon^{-}}$ are gated into low-frequency detector; B > A due to assumed frequency error; therefore, A $\geq$ B signal is equal to 1
17T	f_{sc} is gated into strobe generator
17TR1	Low-frequency strobe is activated; A $\geq$ B signal is equal to 1; this signal does not set FF3 $f_{line} \geq f_{ref}$ signal resets temporary storage to 0000
17TR2	0000 error count from temporary storage is transferred to permanent storage; permanent storage data are transferred into special decoder; these error data are then applied to SCR circuits; all load is removed (no SCR's are conducting)
17TR3	Gates off f_{sc} into strobe generator and resets generator from 11 to 00 Resets FF6 from 1 to 0; this signal gates off clock and resets divide-by-5 and divide-by-2500 counters f_{line} period counter is reset to 00000
1T	Sets FF6, which gates clock into divide-by-5 and divide-by-2500 counters Sets FF2 from 0 to 1; ϵ^{+} and $\overline{\epsilon^{-}}$ are gated into low-frequency detector Resets FF1 to 1($\overline{Q}$) Resets FF2 to 0(Q) f_{line} period counter active
2T to 14T	f_{line} period counter active
15T	Temporary storage is reset to 0000
16T	Pulse error count is gated into temporary storage; assume pulse error count of 1

[a]At leading edge.

APPENDIX B

DECODER

The advantages of the decoder are discussed in the section CONCEPTUAL SPEED-CONTROLLER CIRCUIT - Subcircuit Analysis. Table IV presents a conversion from binary to the special code. Table IV, however, illustrates the output as a direct function of the input. The schematic diagram, figure 15, indicates an inverted (negated) output is required. This is accomplished by (1) rewriting the code output of table IV as a negation of that presented and (2) recombining these loads to permit the maximum use of single unit load elements. The development of a matrix circuit to provide this function is described in this appendix and reference 9. The information, which is based on table IV, including the revisions just mentioned, is transformed into the following Boolean transmission equations for each parasitic-load element:

$$L_1(\overline{1_1}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3} + \overline{2^0}\,2^1\,2^2\,\overline{2^3} + 2^0\,2^1\,2^2\,\overline{2^3}$$

$$L_2(\overline{1_2}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3} + \overline{2^0}\,2^1\,2^2\,\overline{2^3}$$

$$L_3(\overline{2_1}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3}$$

$$L_4(\overline{2_2}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3}$$

$$L_5(\overline{2_3}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3}$$

The basic concept of the decoder is illustrated in figure 9. The Boolean equations just given, which describe the load element, can be rewritten as follows:

$$L_1(\overline{1_1}) = PE_0 + \ldots + PE_2 + PE_3 + PE_4 + \ldots + PE_6 + PE_7$$

$$L_2(\overline{1_2}) = PE_0 + PE_1 + PE_2 + \ldots + PE_4 + PE_5 + PE_6$$

$$L_3(\overline{2_1}) = PE_0 + PE_1 + \ldots + \ldots + PE_4 + PE_5$$

$$L_4(\overline{2_2}) = PE_0 + PE_1 + PE_2 + PE_3$$

$$L_5(\overline{2_3}) = PE_0 + PE_1 + PE_2 + PE_3$$

where PE is the pulse error count indicated in table IV. For instance, PE_4 is pulse error count 4; PE_4 corresponds with the binary number $2^0\ \overline{2^1}\ 2^2\ \overline{2^3}$ in the previous Boolean equations.

The matrix circuit of figure 17 is derived by utilizing these revised equations. Rewriting the Boolean transmission equations has resulted in a reduction of 50 percent in the number of diodes and resistor elements required. Further simplification of the matrix appears feasible.

The alternative decoder, as also mentioned in the section CONCEPTUAL SPEED-CONTROLLER CIRCUIT - Subcircuit Analysis, basically differs from the decoder described in this section in that all parasitic-load elements are of the same power level. This modification simplifies the fabrication of the PLR assembly since the diameter and

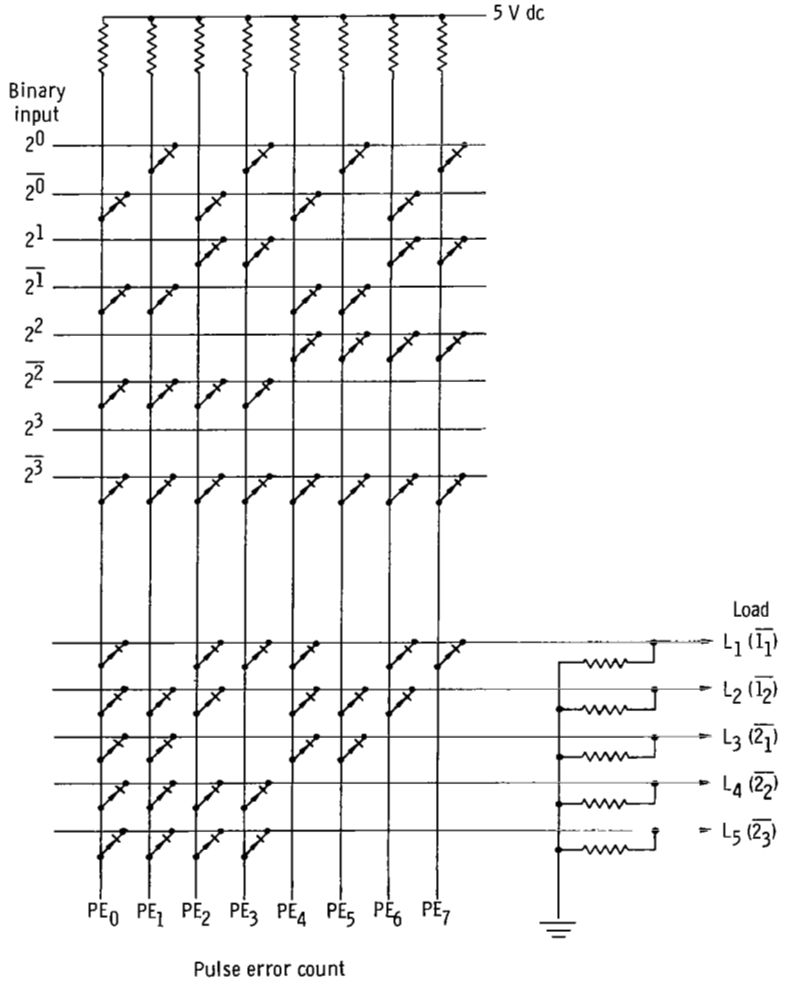


Figure 17. - Schematic of diode matrix board for special code conversion decoder.

length of each element would be the same. However, this modification requires the use of eight parasitic-load elements compared to the five mentioned in the previous discussion.

The conversion from the pulse error count to the special code for this alternative decoder is illustrated in table X. Any failure of a power output stage will affect only one unit of parasitic load instead of possibly two. The use factor for each element is nearly the same; for example, four parasitic-loading conditions require four elements, while the remaining loading conditions each use five elements.

TABLE X. - DECODER ALTERNATIVE BINARY TO SPECIAL CODE CONVERSION

Pulse error count (base 10)	Binary input				Negated special code output (unit loads)							
	2^3	2^2	2^1	2^0	$\overline{1_2}$	$\overline{1_2}$	$\overline{1_3}$	$\overline{1_4}$	$\overline{1_5}$	$\overline{1_6}$	$\overline{1_7}$	$\overline{1_8}$
0	0	0	0	0	1	1	1	1	1	1	1	1
1	0	0	0	1	0	1	1	1	1	1	1	1
2	0	0	1	0	1	0	0	1	1	1	1	1
3	0	0	1	1	1	1	1	0	0	0	1	1
4	0	1	0	0	0	0	1	1	1	1	0	0
5	0	1	0	1	1	1	0	0	0	0	0	1
6	0	1	1	0	0	0	0	0	0	1	1	0
7	0	1	1	1	0	0	0	0	1	0	0	0
8	1	0	0	0	0	0	0	0	0	0	0	0

The Boolean transmission equations for table X are as stated by the following equations:

$$L_1(\overline{1_1}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3}$$

$$L_2(\overline{1_2}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3}$$

$$L_3(\overline{1_3}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3}$$

$$L_4(\overline{1_4}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3}$$

$$L_5(\overline{1_5}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3} + 2^0\,2^1\,2^2\,\overline{2^3}$$

$$L_6(\overline{1_6}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,\overline{2^1}\,2^2\,\overline{2^3} + \overline{2^0}\,2^1\,2^2\,\overline{2^3}$$

$$L_7(\overline{1_7}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,2^2\,\overline{2^3}$$

$$L_8(\overline{1_8}) = \overline{2^0}\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,\overline{2^2}\,\overline{2^3} + \overline{2^0}\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,2^1\,\overline{2^2}\,\overline{2^3} + 2^0\,\overline{2^1}\,2^2\,\overline{2^3}$$

By rewriting these Boolean transmission equations in a manner similar to that done on the five-load-element decoder, the diode matrix circuit for the eight-load-element (alternative) decoder is developed. This matrix circuit is illustrated in figure 18. The matrix circuit of figure 18 has not been incorporated into this digital-speed-controller concept since the advantages for this conversion technique would be determined best by a systems analysis for a specific application. This conclusion is beyond the scope of the investigation of this report.

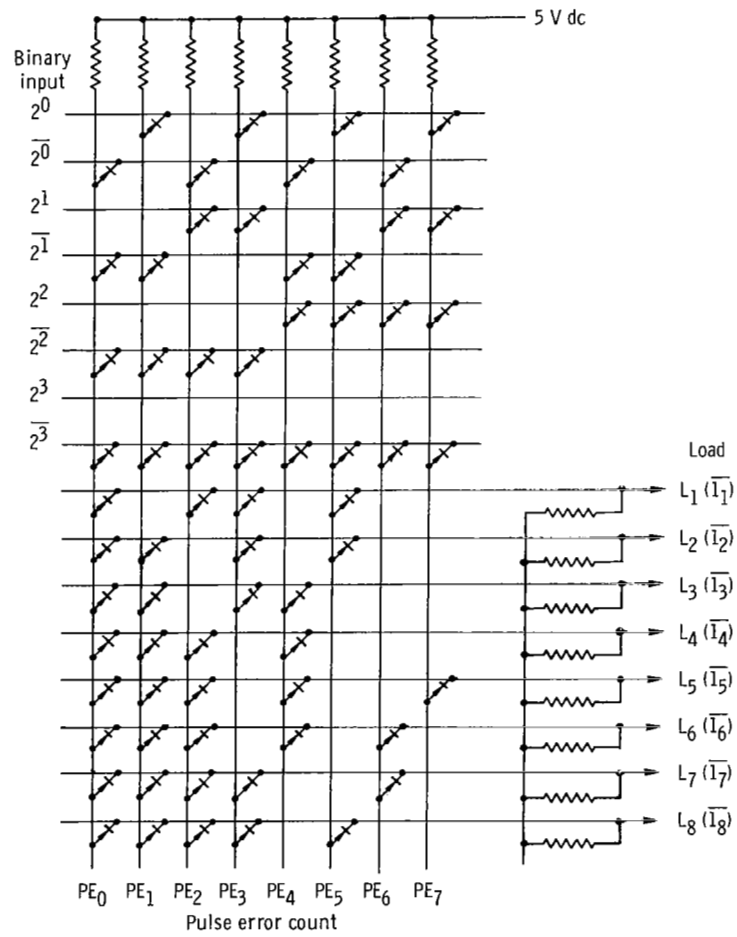


Figure 18. - Schematic of diode matrix board (alternative) for special code conversion decoder.

REFERENCES

1. Guentert, Donald C.; and Johnsen, Roy L.: Study of Brayton Cycle Power Generation System Using SNAP-8 Nuclear Reactor as an Energy Source. NASA TN D-5751, 1970.

2. Thollot, Pierre A.; Bainbridge, Richard C.; and Nestor, James: Description and Performance of the Electrical Subsystem for a 2 to 15 kWe Brayton Power System. Presented at the Fifth Intersociety Energy Conversion Engineering Conference, Las Vegas, Nev., Sept. 21-24, 1970.

3. Valgora, Martin E.; and Perz, Dennis A.: Steady-State Electrical Performance of a 400-Hertz Brayton Cycle Turboalternator and Controls. NASA TN D-5658, 1970.

4. Hodgson, J. N.; and Macosko, R. P.: A SNAP-8 Breadboard System-Operating Experience. Intersociety Energy Conversion Engineering Conference. Vol. 1. IEEE, 1968, pp. 338-351.

5. Word, John L.; Fischer, Raymond L. E.; and Ingle, Bill D.: Static Parasitic Speed Controller for a Brayton-Cycle Turboalternator. NASA TN D-4176, 1967.

6. Ingle, B. D.; and Corcoran, C. S.: Development of a 1200-Hertz Alternator and Controls for Space Power Systems. Intersociety Energy Conversion Engineering Conference. IEEE, 1968, pp. 438-447.

7. Anon.: Digital Application Notes - EECologic 2. Electronic Eng. Co. of California, Mar. 1970, pp. A16-18.

8. Millman, Jacob; and Taub, Herbert: Pulse, Digital, and Switching Waveforms. McGraw-Hill Book Co., Inc., 1965, pp. 671-672.

9. Caldwell, Samuel H.: Switching Circuits and Logical Design. John Wiley & Sons, Inc., 1958, pp. 387-404.

NASA-Langley, 1972 — 3 E-6430