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A DIGITAL-TO-ANALOG CONVERSION CIRCUIT USING THIRD-ORDER POLYNOMIAL INTERPOLATION

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16. Abstract

Zero- and third-order digital-to-analog conversion techniques are described, and the theoretical error performances are compared. The design equations and procedures for constructing a third-order digital-to-analog converter by using analog design elements are presented. Both a zero- and a third-order digital-to-analog converter were built, and the performances are compared with various signal inputs.

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A DIGITAL-TO-ANALOG CONVERSION CIRCUIT USING THIRD-ORDER POLYNOMIAL INTERPOLATION

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SUMMARY

This report describes the basic design for a circuit that is capable of reconstructing digitized analog signals by interpolating between given sample points with a third-order polynomial. From an analytical description of the circuit inputs and outputs, design equations are developed and implemented on an analog computer.

The theoretical error performance of the third-order digital-to-analog converter is developed from the analytical description, and the error performances are compared with experimental results. The same is done for a zero-order (sample and hold) digital-to-analog converter, and these results are compared with results of the third-order digital-to-analog converter.

Both theoretical and experimental comparisons of third-order and zero-order digital-to-analog converters show a markedly superior performance of the third-order digital-to-analog converter. From these results, it is shown that the use of third-order digital-to-analog converters for analog-data reconstruction will allow a significant decrease in the bandwidth required for digital telemetry systems that transmit analog data, with no decrease in the quality of the data.

INTRODUCTION

In most telemetry systems in use today, digital-to-analog conversion is performed by zero-order (sample and hold) interpolation circuits. Such circuits have the attractive feature of relative simplicity. However, because of this attractiveness, the basic disadvantage of these circuits is frequently overlooked. This disadvantage is that higher than necessary sampling rates must be used in the digital encoding of the analog signal. The use of higher sample rates increases the bandwidth necessary to transmit the signal and thereby imposes additional cost and complexity on the remainder of the telemetry system. The design and performance of a digital-to-analog converter (DAC) that uses a third-order polynomial interpolation between sample points are presented in subsequent sections of this report; use of such a DAC permits lower sampling rates without decreasing the accuracy of the reconstructed analog signal. However, if the need to reduce the sampling rate (bandwidth) does not exist, the use of such a DAC will significantly improve the data quality.

The theoretical and practical design and performance of a high-order (third order) interpolation circuit for digital-to-analog conversion of telemetry data are discussed in this report. The study described was initiated in an attempt to relieve the bandwidth problems in the NASA Manned Space Flight Network telemetry system that occur as a result of the high-sampling-rate biomedical data (i.e., electrocardiograms (EKG's)), and, at the same time, to maintain the present accuracy level of the data.

SYMBOLS

A	amplitude
B, C, D, E	constant coefficients of polynomial terms
C_f	feedback capacitance
$\mathscr{E}_{ic}$	initial-condition voltage applied to the circuit
e	voltage
e_{in}	input voltage
e_{out}	output voltage
F, G, H	scale factors
f	frequency, Hz
f_c	cut-off frequency, Hz
f_s	sampling frequency, samples/sec
$\|G(f)\|$	root-mean-square spectrum of g(t)
g(t)	time function
I1, I2, I3	integrators
$K = Z_f/Z_i$	
L	integrator gain, $1/R_iC_f$
m	ratio of the spectrum cut-off rate of the signal to 6 dB/octave

P', Q', R', S', T'	waveform segments of an EKG signal
p	normalized sampling rate, samples/cycle
R	resistance
R_f	feedback resistance
R_i	input resistance
S_1, S_2	switches
s	Laplacian operator
T	period, 1/f, sec
t	time, sec
TP1, TP2	test points
Y	reconstructed signal, V
$\dot{Y}$	first derivative of Y with respect to time
$\ddot{Y}$	second derivative of Y with respect to time
$\dddot{Y}$	third derivative of Y with respect to time
y(t)	analog signal as a function of time, V
y'(t)	analog reconstruction of y(t)
Z_f	feedback impedance
Z_i	input impedance
ϵ	error, percent or pulse code modulation (PCM) counts
ϵ_b	instantaneous error measured near the base-line crossing, percent
ϵ_p	instantaneous error measured at the peaks, percent
ρ	reset time, sec
τ	sampling period, sec
ω	angular frequency, rad/sec

Subscripts:

ic	initial condition

n = 0, 1, 2, 3, . . .

THEORY

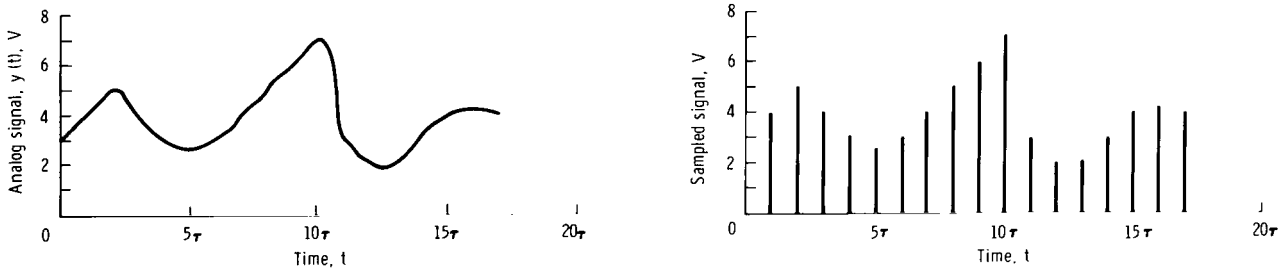
The analog-to-digital encoding used in the Apollo telemetry system is described as follows and is illustrated in figure 1.

1. The analog signal (fig. 1(a)) is sampled for its amplitude value at time intervals spaced τ seconds apart (fig. 1(b)), where τ is the inverse of the sampling rate.

2. The amplitude values are then pulse code modulation (PCM) encoded (fig. 1(c)) before transmission.

In zero-order digital-to-analog conversion, the PCM signal (fig. 1(c)) is accepted and converted to a pulse amplitude modulation (PAM) signal (fig. 1(b)), which is then fed to a holding circuit that provides an output curve similar to the curve shown in figure 2(a). A third-order DAC will also accept PCM signals, convert them to PAM signals, and then compute and output a third-order polynomial, which is a function of time, to fit the transmitted signal samples (fig. 2(b)). The reconstruction errors that result from this and other processes have been found analytically by previous work (ref. 1). Some of the results of that work, along with experimental checks performed in this study, are shown in appendix A.

The purpose of this report is to describe a method of designing a circuit on the analog computer for the third- and zero-order DAC's described in reference 1. The geometries for calculating the errors for the third- and zero-order DAC's are presented in figures 3 and 4. The use of the design method would allow an experimental verification of the error analysis shown in figures 3(c) and 4(c) and also would provide the basic design for a prototype of the third-order DAC.



(a) Analog signal.

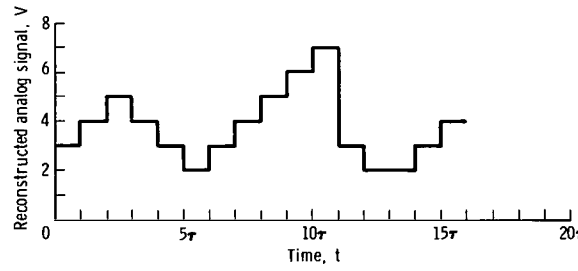
(b) Pulse-amplitude-modulation signal.

Figure 1. - Analog-to-digital encoding.

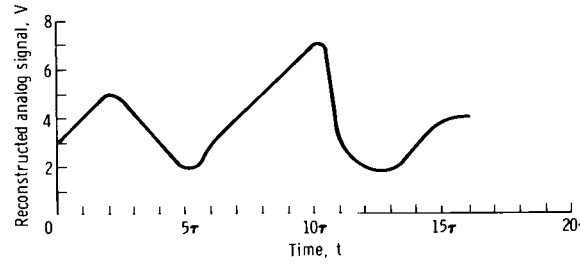
t	PCM signal
0	011
τ	100
2τ	101
3τ	100
4τ	011
5τ	010
6τ	011
7τ	100
8τ	101
9τ	110
10τ	111
11τ	011
12τ	010
13τ	010
14τ	011
15τ	100
16τ	100
17τ	100

(c) Pulse-code-modulation signal (eight quantization levels).

Figure 1. - Concluded.

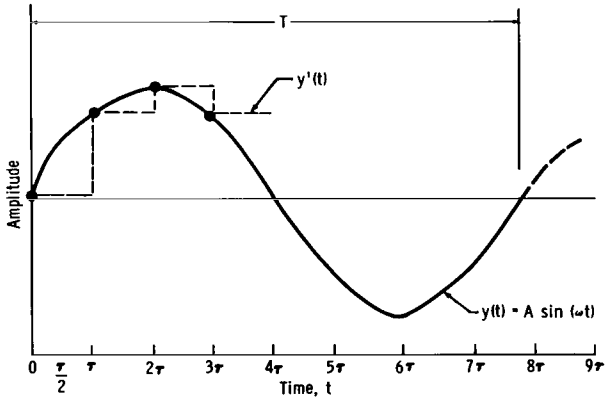


(a) Zero order.

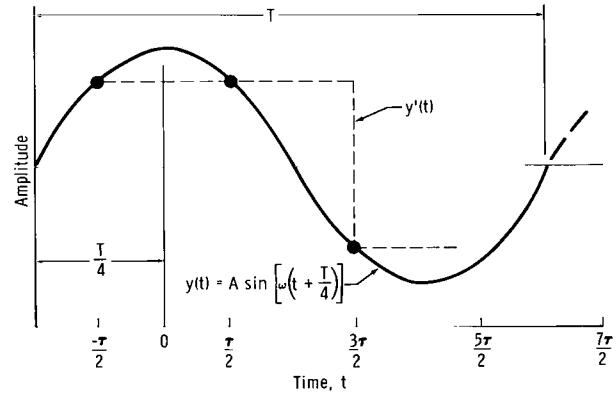


(b) Third order.

Figure 2. - Zero- and third-order DAC outputs.

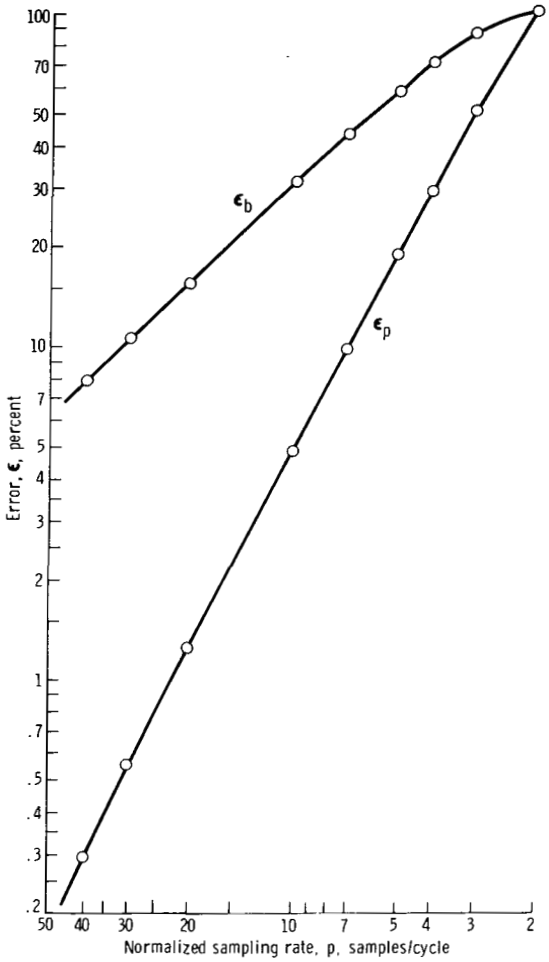


(a) Geometry for calculating ϵ_b.



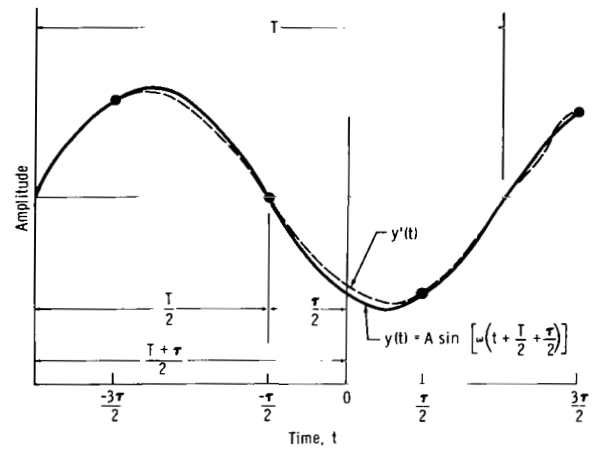
(b) Geometry for calculating ϵ_p.

Figure 3. - Reconstruction errors for a zero-order DAC.

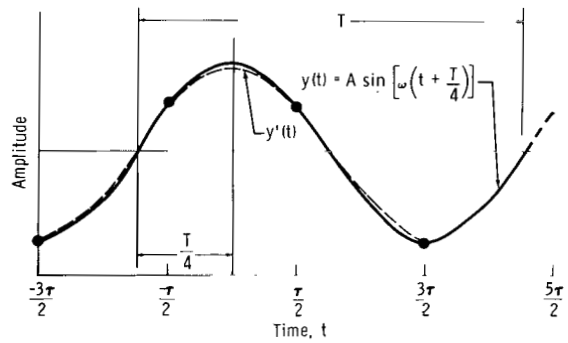


(c) Error as a function of normalized sampling rate.

Figure 3. - Concluded.



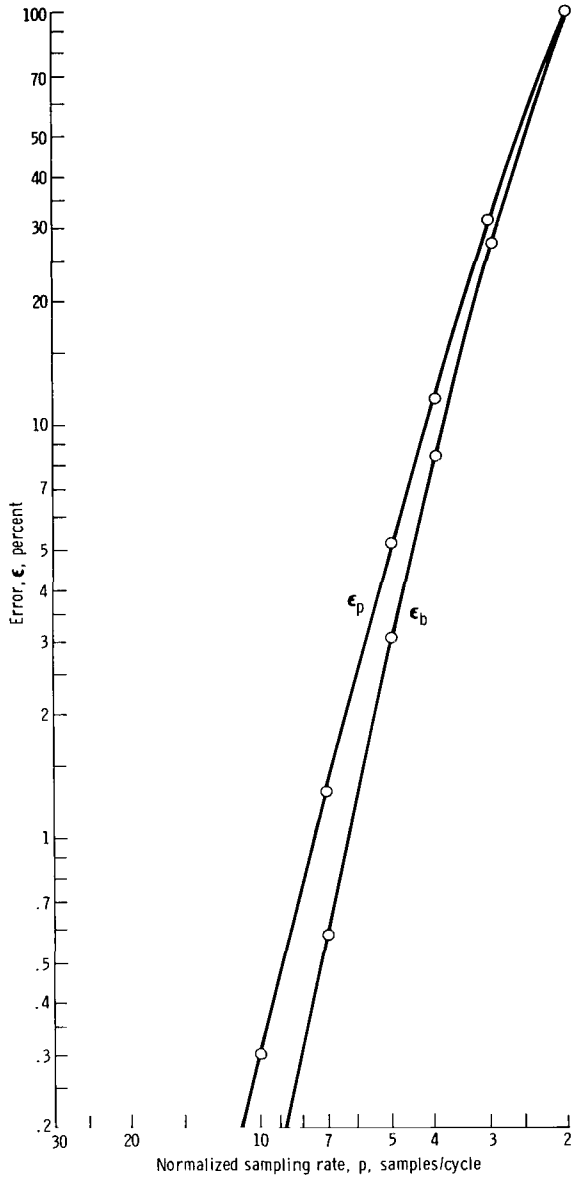
(a) Geometry for calculating ϵ_b.



(b) Geometry for calculating ϵ_p.

Figure 4. - Reconstruction errors for a third-order DAC.

The development of the design equations for a third-order DAC proceeds as follows. The development is facilitated by initially assuming the existence of a PAM version of the analog signal, such as that shown in figure 5. At $t = 0$, the circuit must compute and output a signal that is described by a third-order polynomial that would connect the input PAM signal points Y_{1-n}, Y_{2-n}, Y_{3-n}, and Y_{4-n}. The output actually starts at $t = 0$, $n = 0$ (or Y_2) and continues only until $t = \tau$, $n = 0$ (or Y_3), so that only the central two points of the given four are connected. This completes one cycle of operation. The next cycle begins at $t = 0$, $n = 1$ (or Y_2) and continues until $t = \tau$, $n = 1$ (or Y_3). This cycle could be visualized as sliding the data points leftward past a fixed time scale, so that time, for the circuit, is always between 0 and τ. At the same time, the circuit, in an abstract sense, has both memory and precognition, because the circuit must have knowledge of the samples Y_{1-n} and Y_{4-n}.



(c) Error as a function of normalized sampling rate.

Figure 4. - Concluded.

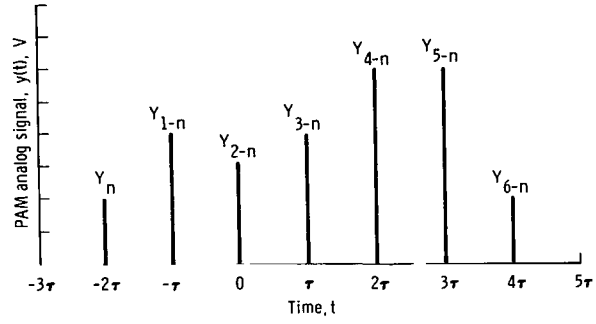


Figure 5. - Third-order PAM version of the analog signal.

This knowledge is necessary because the circuit output between $t = 0$ and $t = \tau$ must be described by

$$y(t) = Bt^3 + Ct^2 + Dt + E \qquad (1)$$

which is a third-order polynomial. Because there are four unknowns (B, C, D, and E) in equation (1), the signal voltages (Y_1, Y_2, Y_3, and Y_4) must be given at four sample times ($-\tau$, 0, τ, and 2τ, respectively) (fig. 5). The coefficients B, C, D, and E may be evaluated from the following equation set.

$$Y(-\tau) = B(-\tau)^3 + C(-\tau)^2 + D(-\tau) + E = Y_1 \qquad (2)$$

$$Y(0) = B(0)^3 + C(0)^2 + D(0) + E = Y_2 \qquad (3)$$

$$Y(\tau) = B(\tau)^3 + C(\tau)^2 + D(\tau) + E = Y_3 \qquad (4)$$

$$Y(2\tau) = B(2\tau)^3 + C(2\tau)^2 + D(2\tau) + E = Y_4 \qquad (5)$$

As a result of solving equations (2) to (5)

$$B = \frac{-Y_1 + 3Y_2 - 3Y_3 + Y_4}{6\tau^3} \tag{6}$$

$$C = \frac{Y_1 - 2Y_2 + Y_3}{2\tau^2} \tag{7}$$

$$D = \frac{-2Y_1 - 3Y_2 + 6Y_3 - Y_4}{6\tau} \tag{8}$$

$$E = Y_2 \tag{9}$$

The initial conditions of the output signal may also be calculated. If

$$Y(t) = Bt^3 + Ct^2 + Dt + E \tag{10}$$

$$\dot{Y}(t) = 3Bt^2 + 2Ct + D \tag{11}$$

$$\ddot{Y}(t) = 6Bt + 2C \tag{12}$$

$$\dddot{Y}(t) = 6B \tag{13}$$

then

$$Y(0) = E \tag{14}$$

$$\dot{Y}(0) = D \tag{15}$$

$$\ddot{Y}(0) = 2C \tag{16}$$

$$\dddot{Y}(0) = 6B \tag{17}$$

Equations (6) to (17) in the preceding section are sufficient for the design of an analog circuit that will perform the desired interpolation. The equations that specify the initial conditions (eqs. (14) to (17)) of the circuit are in terms of B, C, D, and E, which are in terms of Y_1 to Y_4 (eqs. (6) to (9)). The implication is that four samples, in proper time sequence, must be accessed simultaneously for computation of the initial conditions each time a new sample is received by the circuit.

This delay can be readily implemented with a device similar to a shift register (fig. 6). The operation of this arrangement is as follows. If n = 0, then the registers hold, from top to bottom, $Y_{4-n}=Y_4$, $Y_{3-n}=Y_3$, $Y_{2-n}=Y_2$, and $Y_{1-n}=Y_1$. The next data value Y_{5-n} will be read into the top register by a clock pulse which will increment n by 1. Now the top register holds $Y_{5-n}=Y_4$, the next register holds $Y_{4-n}=Y_3$, then $Y_{3-n}=Y_2$, and $Y_{2-n}=Y_1$. The initial-condition circuitry is then ready to compute a new set of initial conditions. The sample-delay circuitry that was discussed in the preceding section may be physically implemented with either analog or digital logic elements. Block diagrams are shown in figures 7 and 8.

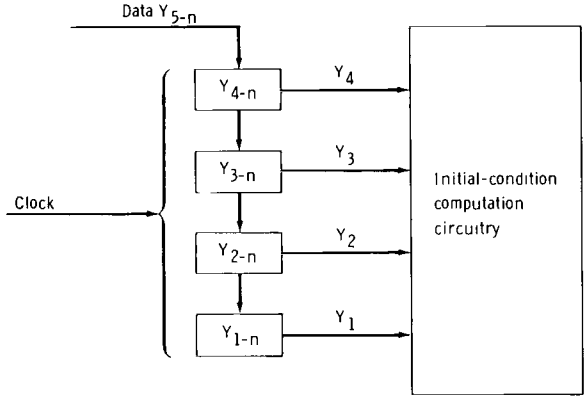


Figure 6. - Sample-delay-circuitry block diagram.

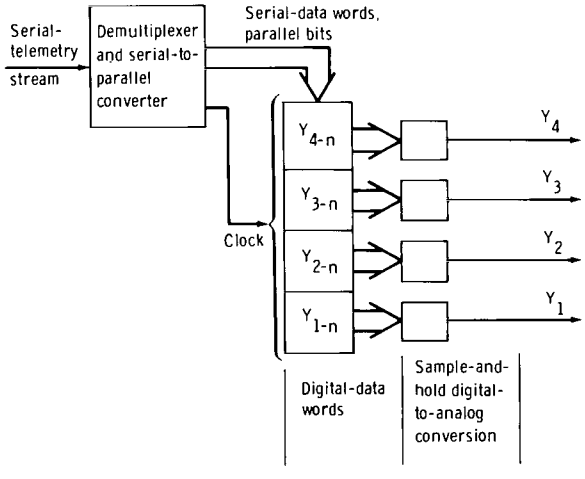


Figure 7.- Flow chart for the use of circuitry with digital logic elements.

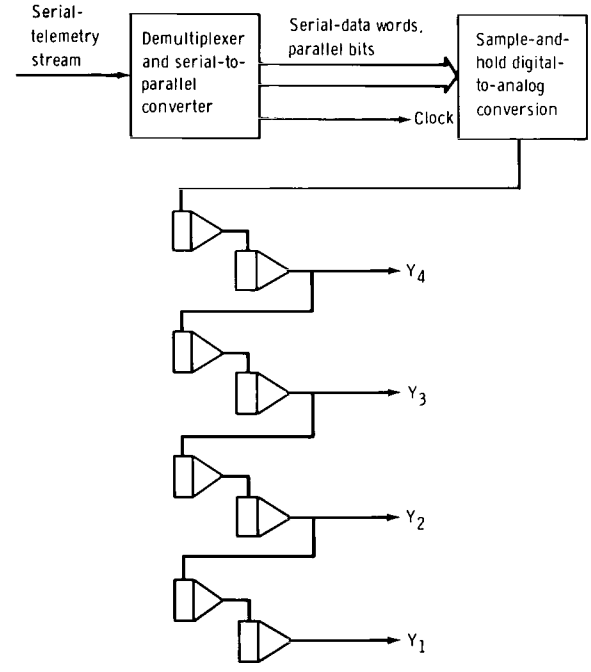


Figure 8.- Flow chart for the use of circuitry with analog logic elements.

The initial-condition circuitry, which is driven by the sample-delay circuitry, is formed of summing amplifiers designed according to equations (6) to (9) and amplitude-scaling constraints. Consideration of full-scale values for Y_1 to Y_4 and of various sampling rates indicates that the initial-condition circuitry will operate well if scaled according to the following equations, which are taken directly from equations (6) to (9). The equations are developed in appendix B.

The initial-condition circuitry should have the following four outputs.

$$-\frac{3B\tau^3}{8} = -\frac{1}{16}\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \tag{18}$$

$$-\frac{C\tau^2}{4} = -\frac{1}{8}\left(Y_1 - 2Y_2 + Y_3\right) \tag{19}$$

$$\frac{D\tau}{4} = \frac{1}{24}\left(-2Y_1 - 3Y_2 + 6Y_3 - Y_4\right) \tag{20}$$

$$-E = -Y_2 \tag{21}$$

The initial-condition-circuitry design is shown in figure 9. (A more extensive discussion of the use of the initial-condition circuitry can be found in appendixes C and D.) Different scaling factors may be chosen, of course, provided appropriate rescaling in the following portions of the circuit is also completed.

The remainder of the interpolation circuit consists of integrators that are driven by the initial-condition circuitry. If equations (17) and (18) are examined simultaneously, it is clear that

$$-\frac{3B\tau^3}{8} = -\frac{\tau^3}{16}\dddot{Y}(0) \tag{22}$$

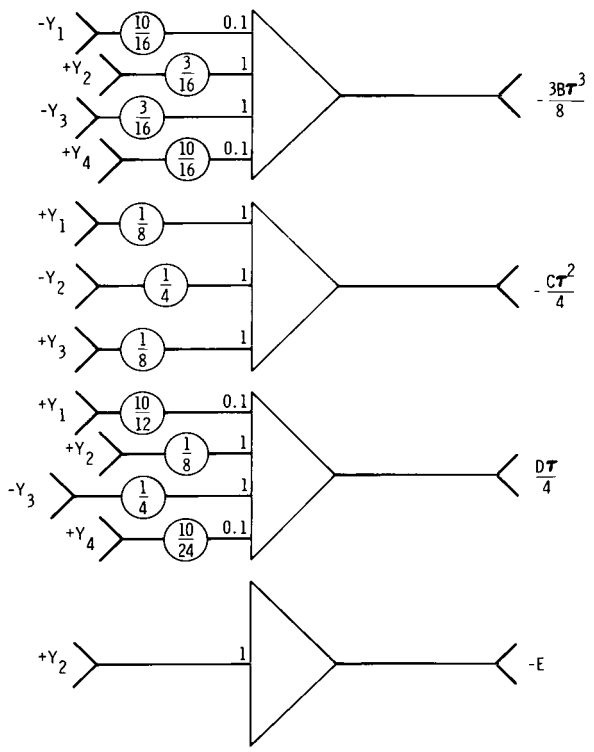


Figure 9. - Initial-condition-circuitry block diagram.

Therefore, if $-3B\tau^3/8$ is input to an integrator with a gain of $-2/\tau$, the output will be $\tau^2\dddot{Y}/8$. This output requires an initial condition of

$$\frac{\tau^2}{8}\ddot{Y}(0) = \frac{2C\tau^2}{8} = \frac{C\tau^2}{4} \tag{23}$$

which is provided by the initial-condition circuitry, as specified by equations (16) and (19).

Equation (19) involves not $+C\tau^2$, but $-C\tau^2$, because integrators invert their initial condition. This procedure is continued through two more integrations, with initial conditions on each integrator initial-condition input appropriate to that integrator output. The final result is shown in figure 10.

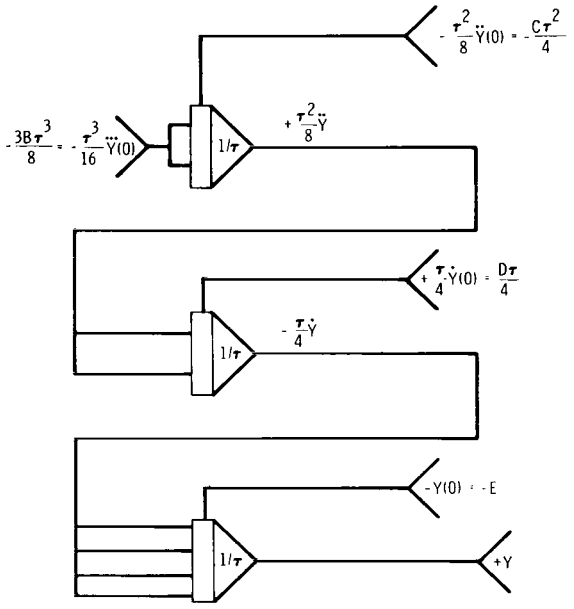


Figure 10. - Integrator-circuitry block diagram.

The circuit discussed in this report requires three timing signals. One signal is a clock (or track) signal that is synchronous with the data. The other two signals (a hold signal and an integrator-reset signal) are derived from the clock signal.

The track and hold signals are necessary only for the track and hold pairs that are used in a shift-register-like arrangement and may be eliminated if the sample-delay circuitry is implemented with digital logic. The track signal occurs at the leading edge of the clock pulse, and the duration of the track signal is 0.01τ. The integrator-reset signal must occur after the clock pulse so that the signals have completed shifting before the resetting of the integrators. The reset signal reinitializes the integrators each time a new sample value enters the circuit. The complete circuit is shown in figure 11 with track and hold amplifiers in the sample-delay circuit. Example analog-data and data-clock sequences are shown in figure 12.

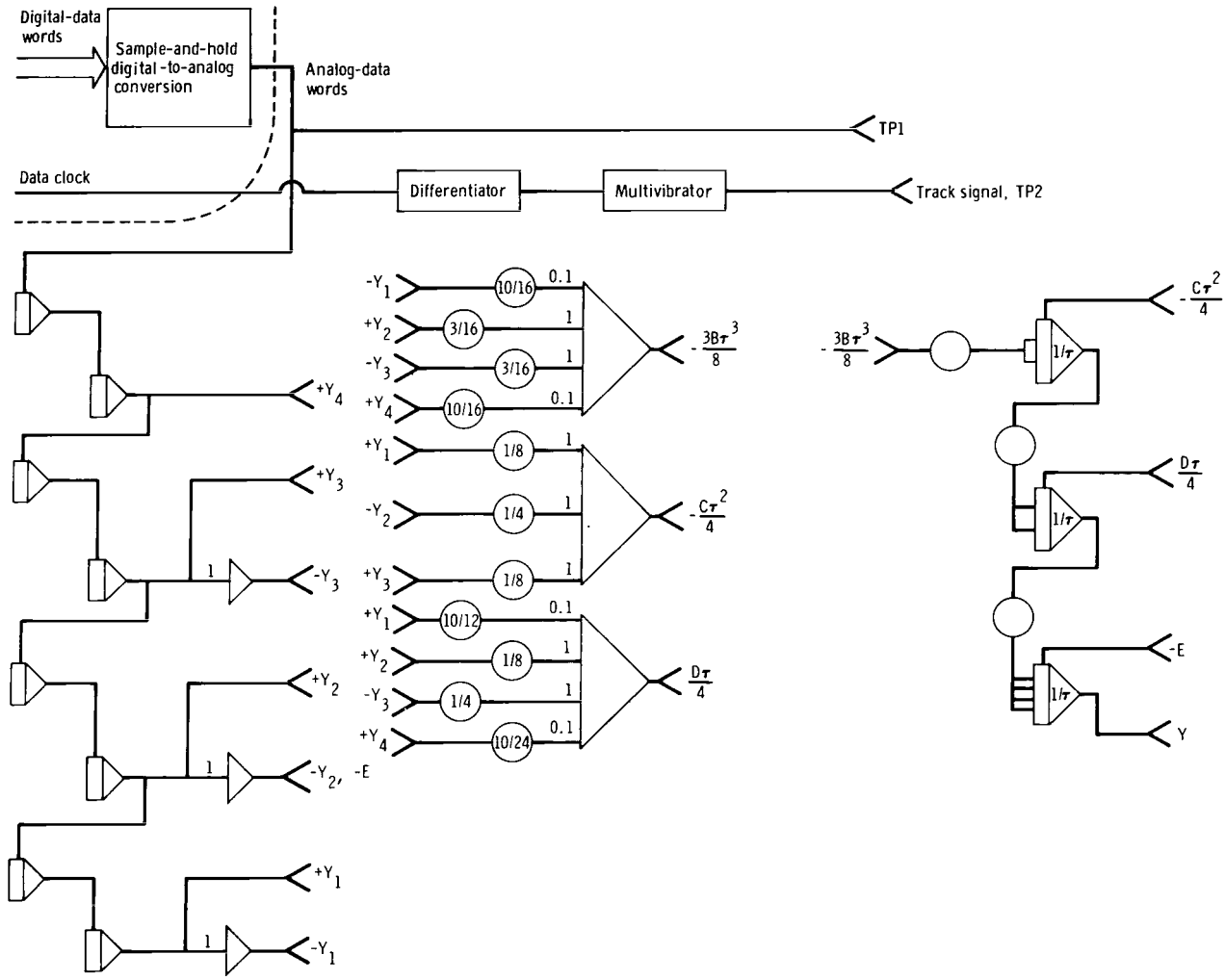
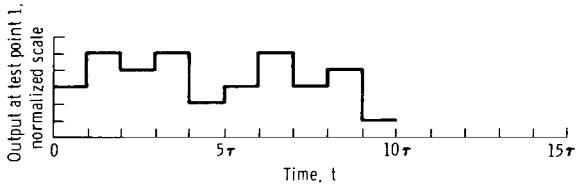
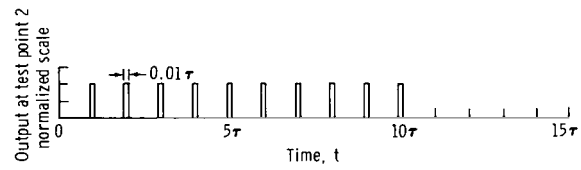


Figure 11. - Third-order DAC block diagram.

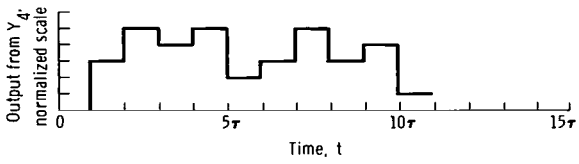


(a) Sample-and-hold reconstruction of an example analog-data word sequence at TP1.

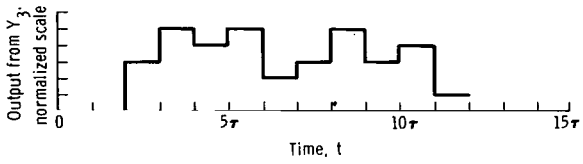


(b) Data-clock (or track) signals at TP2.

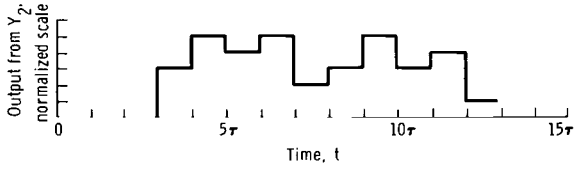
Figure 12. - Example data and clock sequence.



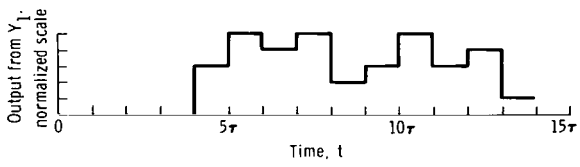
(c) Signal from figure 12(a) phased with the clock signal.



(d) Signal from figure 12(c) delayed one sampling period.



(e) Signal from figure 12(c) delayed two sampling periods.



(f) Signal from figure 12(c) delayed three sampling periods.

Figure 12. - Concluded.

EXPERIMENTAL RESULTS

The digital-to-analog conversions made in this experiment were carried out on an analog computer. A function generator was used to obtain the sinusoidal and square-wave inputs, and a polyrhythm generator was used to obtain the complex EKG analog inputs. The outputs of the system were displayed on an eight-channel strip-chart recorder.

To check the initial-condition-circuitry outputs, a square-wave input was used to simulate a step-function input. The initial-condition circuitry was then checked for zero outputs, because the mathematical derivative of a step function is zero. The functions $\dddot{Y}$, $\ddot{Y}$, and $\dot{Y}$ are shown to be zero in figures 13 and 14. The 0.2-hertz input in figure 15 did not yield derivative values of zero because the sampling rate was only 5 samples/cycle, or 2.5 samples/half-cycle. Four or more samples/half-cycle are required in order for the derivatives to settle to zero, because this would require that $Y_1 = Y_2 = Y_3 = Y_4$, which implies that $B = C = D = 0$. This relationship can be seen by examining equations (6), (7), and (8). If B, C, and D are identically zero, then $\dot{Y}(t) = \ddot{Y}(t) = \dddot{Y}(t) = 0$. (See eqs. (11), (12), and (13).) These zero-derivative outputs were obtained with no adjustments to the theoretical gains of the initial-condition circuitry. The integrator gains were checked with respect to the calibration procedures and were found to agree exactly with the theoretical values.

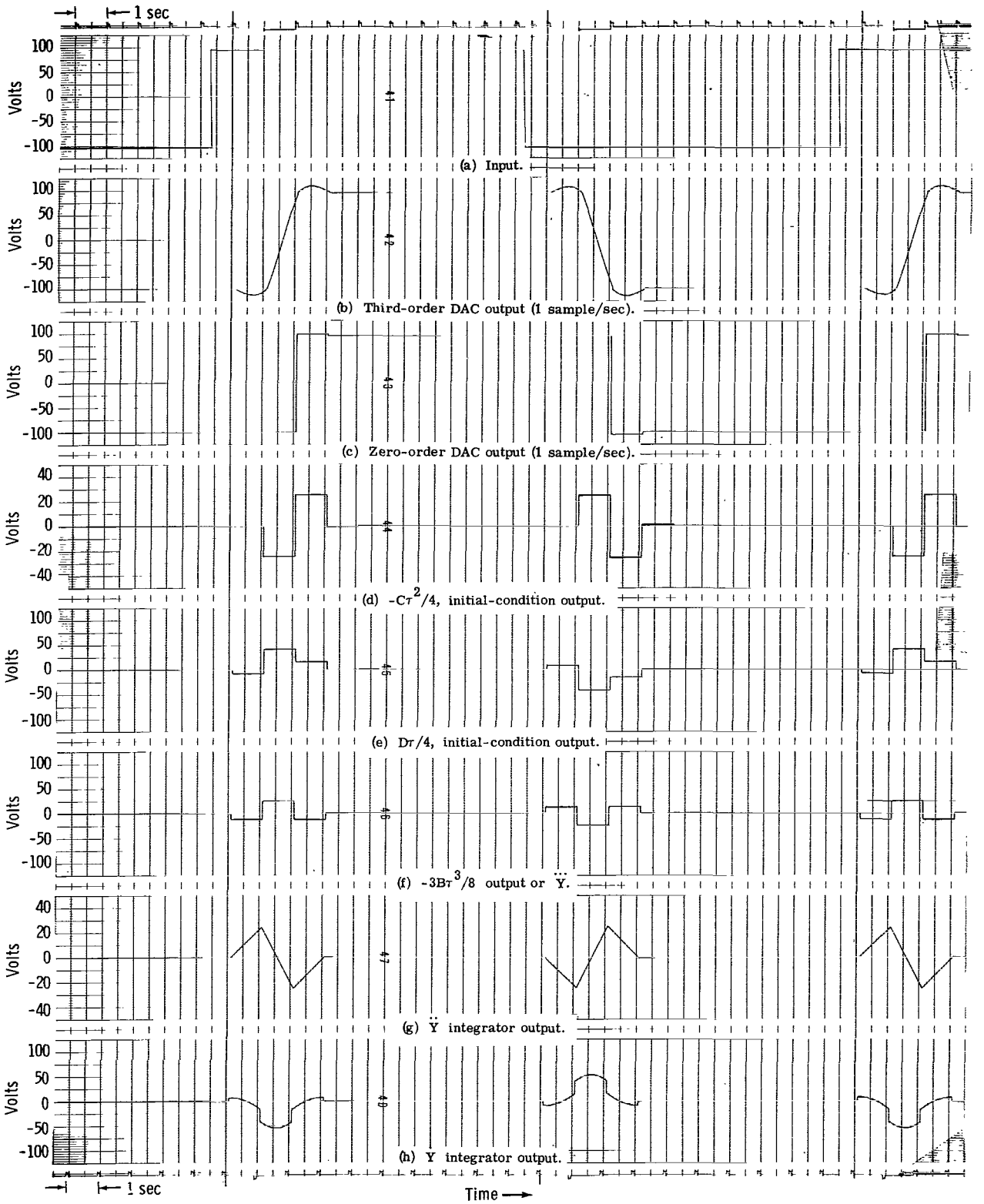


Figure 13. - Results of a 0.05-hertz square-wave input (p = 20 samples/cycle) as a function of time.

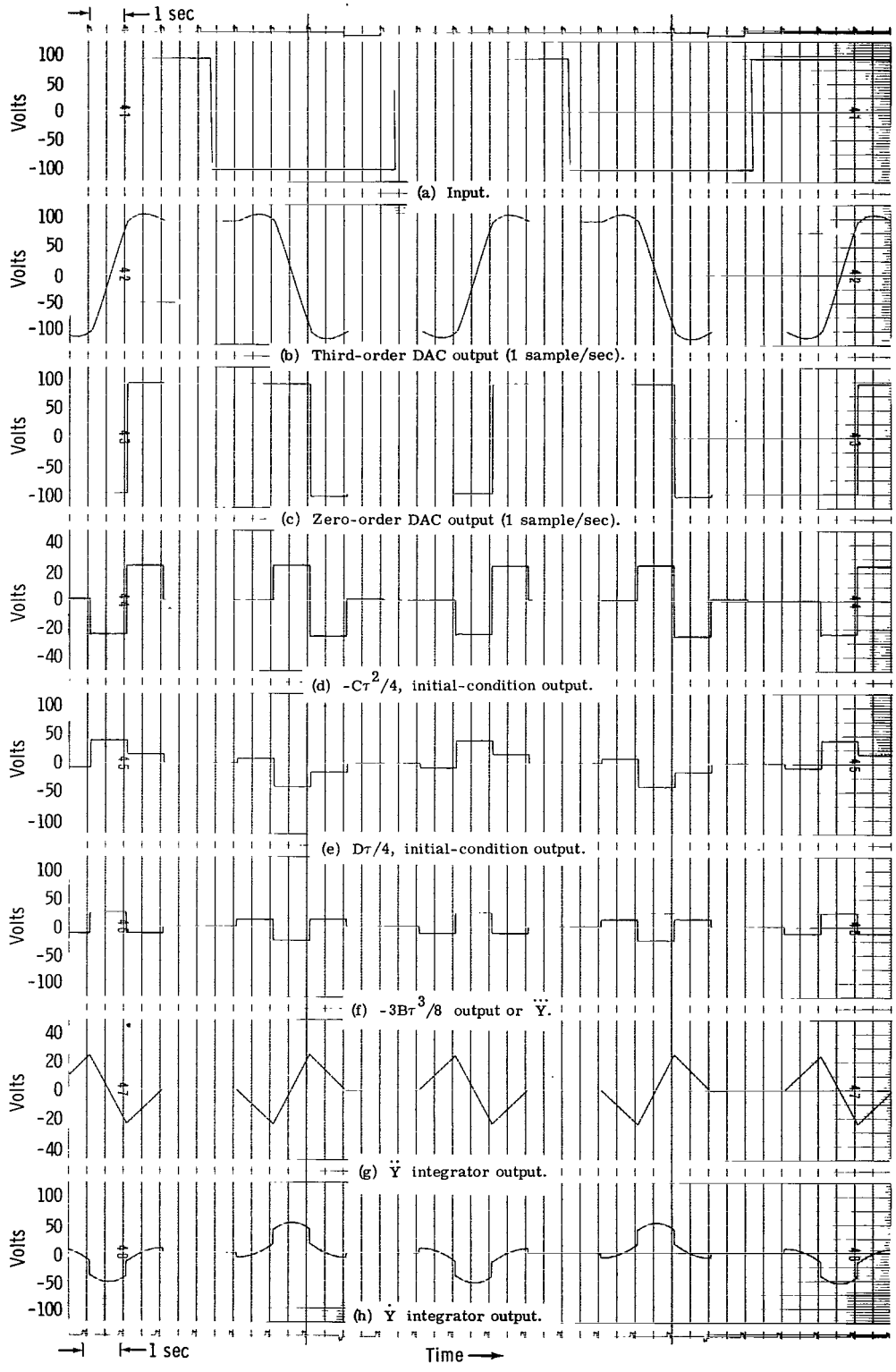


Figure 14. - Results of a 0.1-hertz square-wave input (p = 10 samples/cycle) as a function of time.

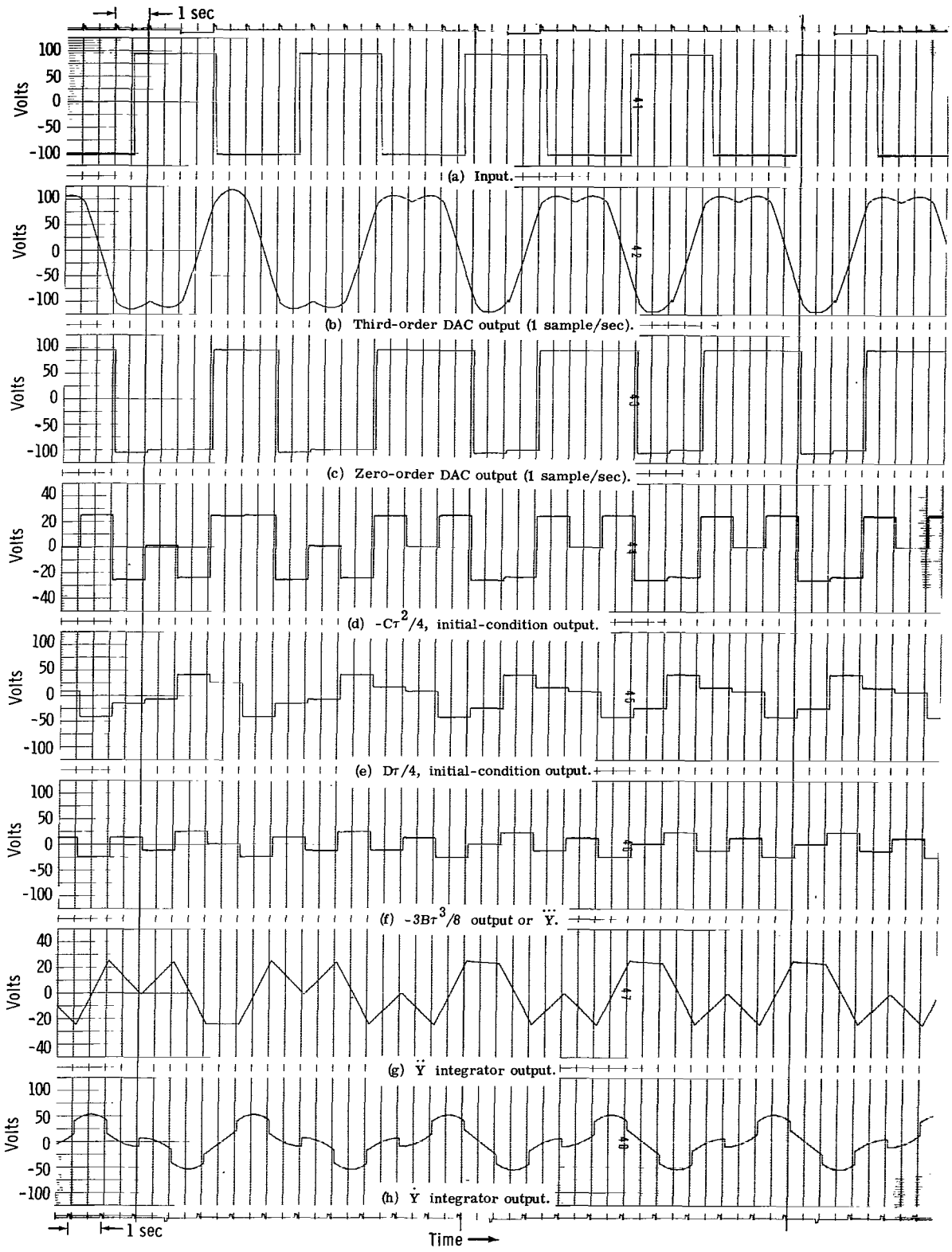


Figure 15. - Results of a 0.2-hertz square-wave input (p = 5 samples/cycle) as a function of time.

To obtain the peak and base-line crossing errors, a comparison of the third-order DAC and the zero-order DAC was obtained by the method shown in figures 3 and 4. The results obtained with sinusoidal inputs of 0.01, 0.02, 0.03, 0.05, 0.07, 0.1, 0.2, 0.3, and 0.4 hertz are shown in figures 16 to 24. The error analysis is shown in figures 3(c) and 4(c). The accuracy of the results is ±2.5 percent. Because these data were obtained from the strip-chart recordings (figs. 16 to 24), the smallest scale obtainable was 5 volts. The experimental errors obtained were less than the theoretical errors in some cases, partly because of the ±2.5-percent accuracy and the inability to reproduce exactly the base-line crossings and peaks of the theoretical analysis. As shown in figures 3(c) and 4(c), the theoretical and experimental errors closely agreed, and the general trends were the same. Because of processing delays within the circuitry, the third-order DAC output lagged the input waveform by two sampling periods (2 seconds in this case) in figures 16 to 24.

Figures 25 to 35 show a comparison of the EKG input from the polyrhythm generator, the third-order DAC output at 100 samples/sec, the zero-order DAC output at 100 samples/sec, and the zero-order DAC output at 200 samples/sec. The zero-order DAC output was artifically delayed two sample periods to permit accurate phase adjustments for error calculations based on comparisons of both zero- and third-order DAC outputs with the original data. Because the input was from the polyrhythm generator, the analog data were stable from cycle to cycle. Therefore, any variation in the DAC outputs was caused by reconstruction errors within the digital-to-analog conversions.

Of the expanded versions of two of the inputs, the third-order DAC output most closely approximates the analog input (figs. 36 and 37). However, a slight error is present in the Q' wave in both figures on the third-order trace. The Q'-to-R' peak transition approximates a step function, and a step function with sharp corners requires an infinite number of terms to fit the curve. The third-order DAC generates only the first four terms of that series. The zero-order DAC is also in error at this point (fig. 37).

It has been shown from both the analytical and the theoretical standpoints that a third-order DAC is more accurate than a zero-order DAC. The third-order DAC output is much smoother because the output is piecewise continuous.

Figures 38 and 39 (cross plots of figs. 3(c) and 4(c)) show that, for normalized sampling frequencies above 5 samples/cycle, it is advantageous to use a third-order DAC instead of a zero-order DAC at twice the rate. This procedure results in a 2:1 advantage. This ratio becomes increasingly larger as p is increased for the zero-order DAC. This advantage is of major importance for two reasons. Use of the third-order DAC allows reduced sampling rates to be used with no degradation in accuracy and allows a substantial reduction in the bandwidth required to transmit the EKG's.

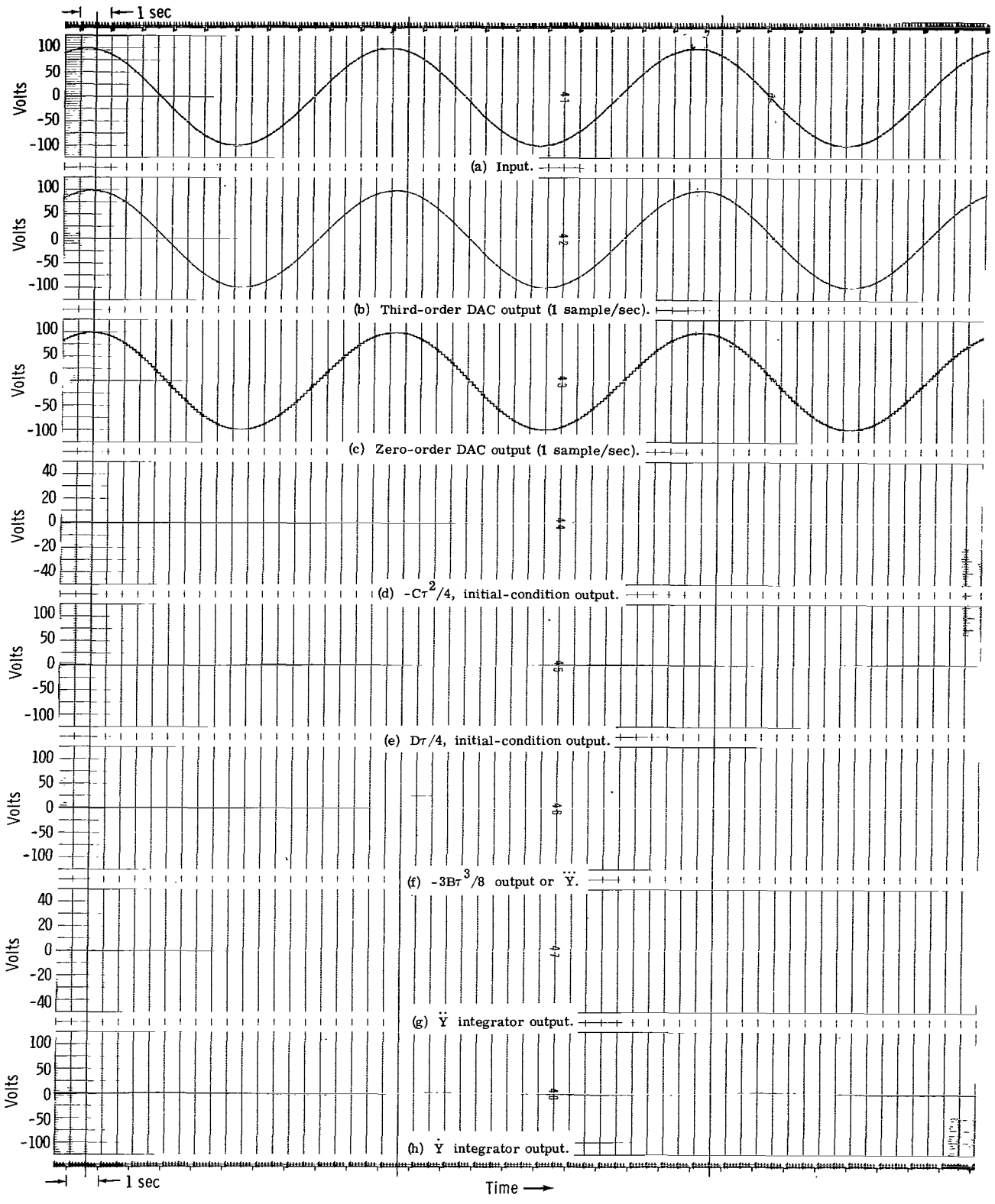


Figure 16. - Results of a 0. 01-hertz sine-wave input (p = 100 samples/cycle) as a function of time.

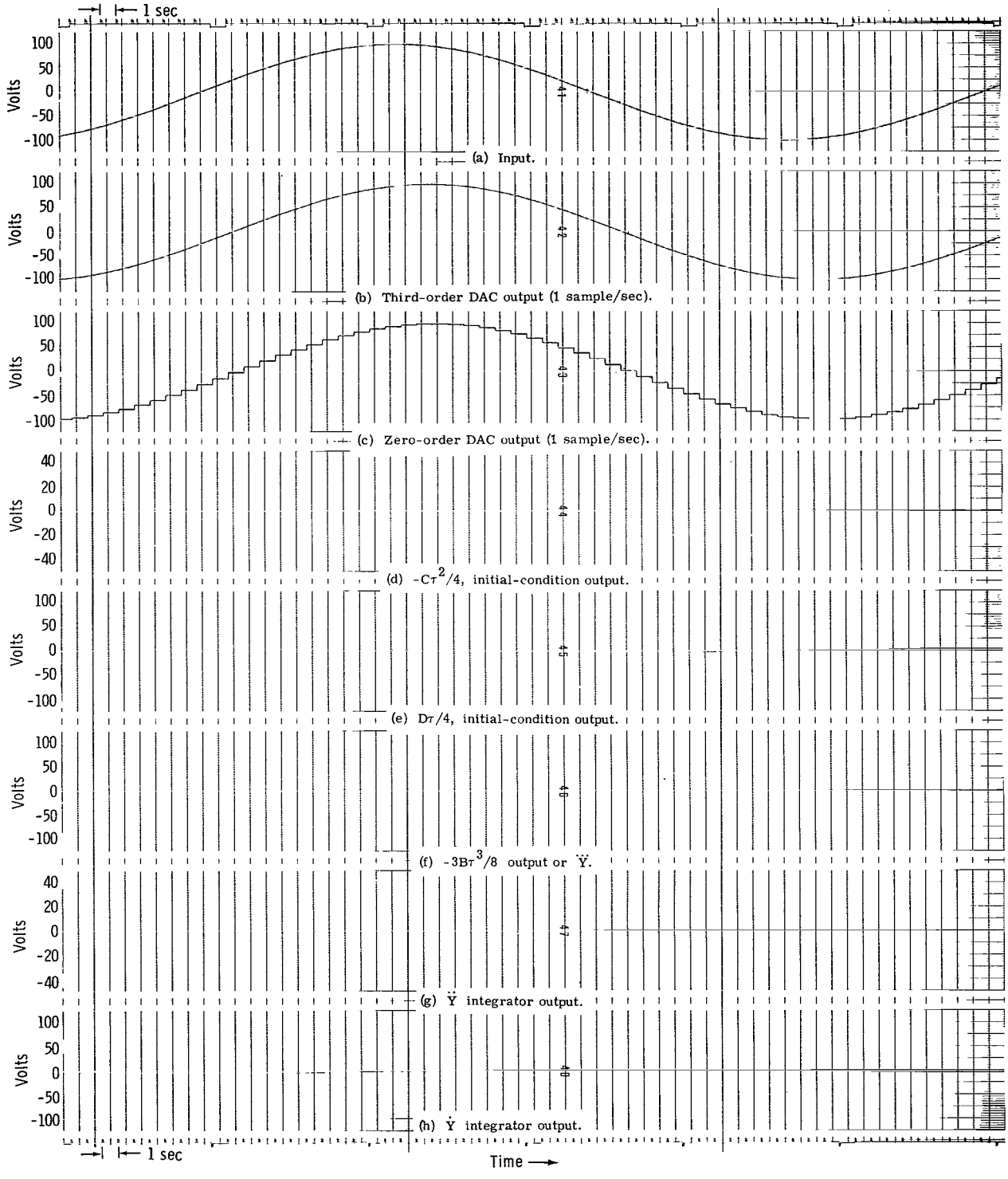


Figure 17. - Results of a 0.02-hertz sine-wave input (p = 50 samples/cycle) as a function of time.

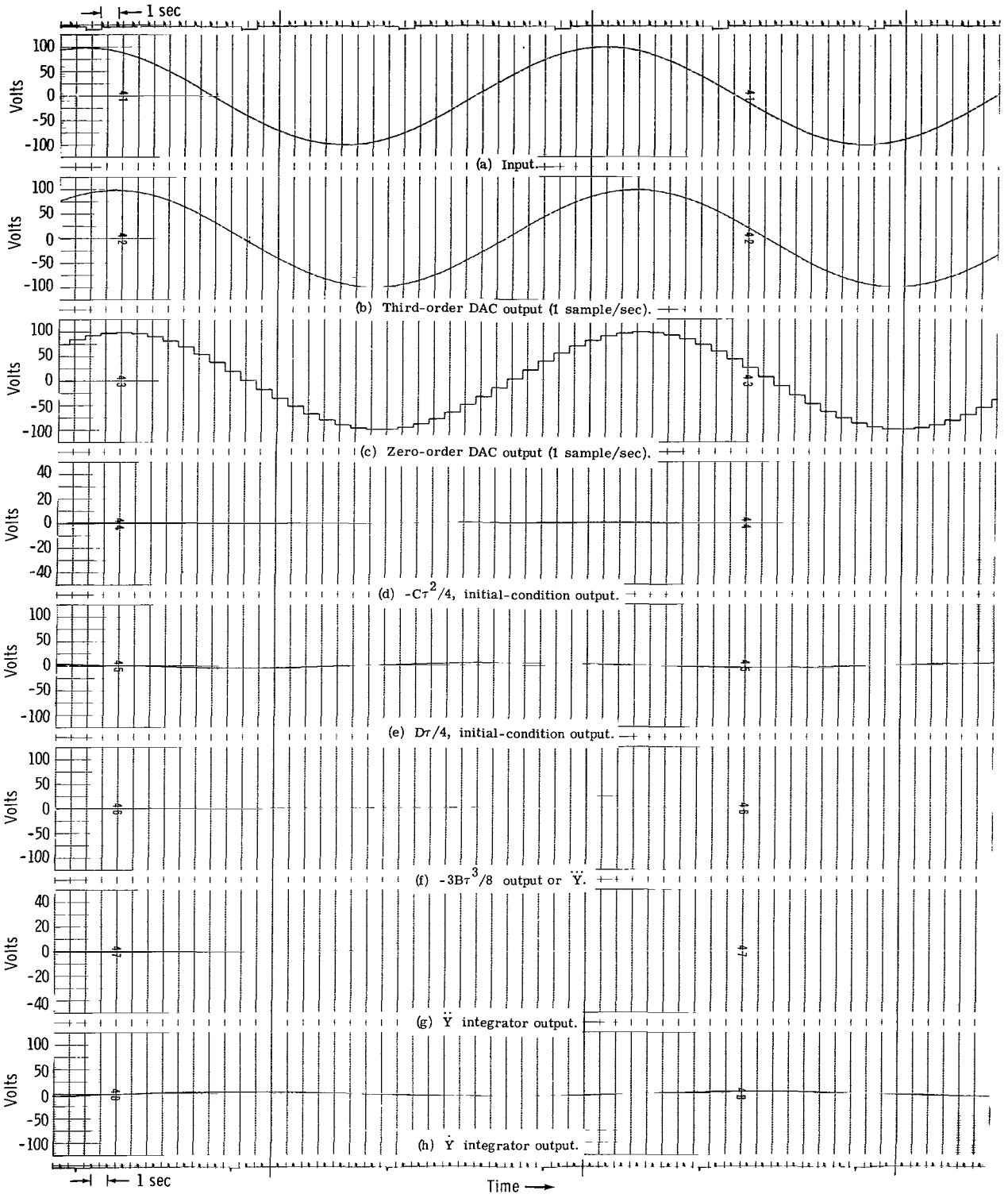


Figure 18. - Results of a 0.03-hertz sine-wave input (p = 33.33 samples/cycle) as a function of time.

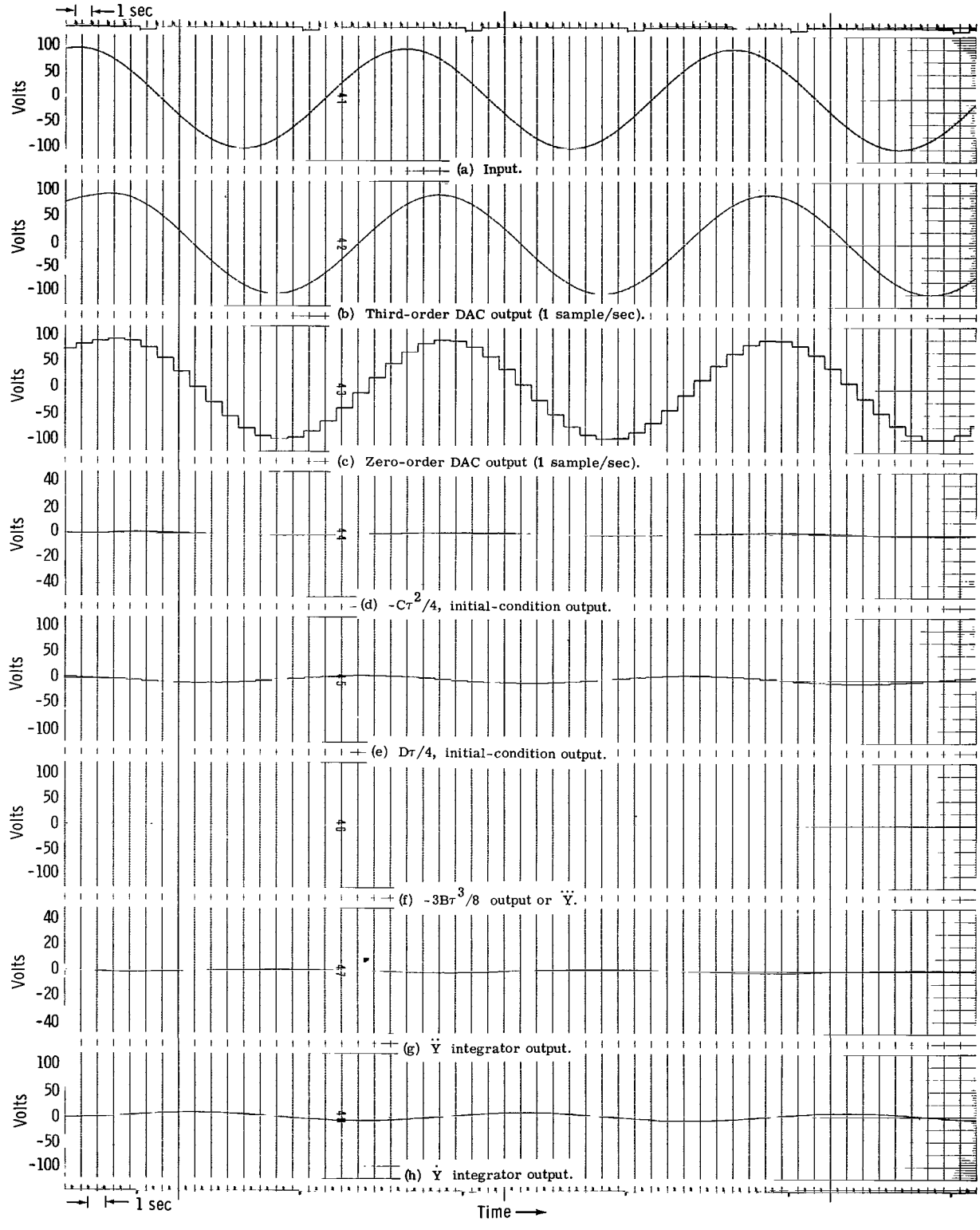


Figure 19. - Results of a 0.05-hertz sine-wave input (p = 20 samples/cycle) as a function of time.

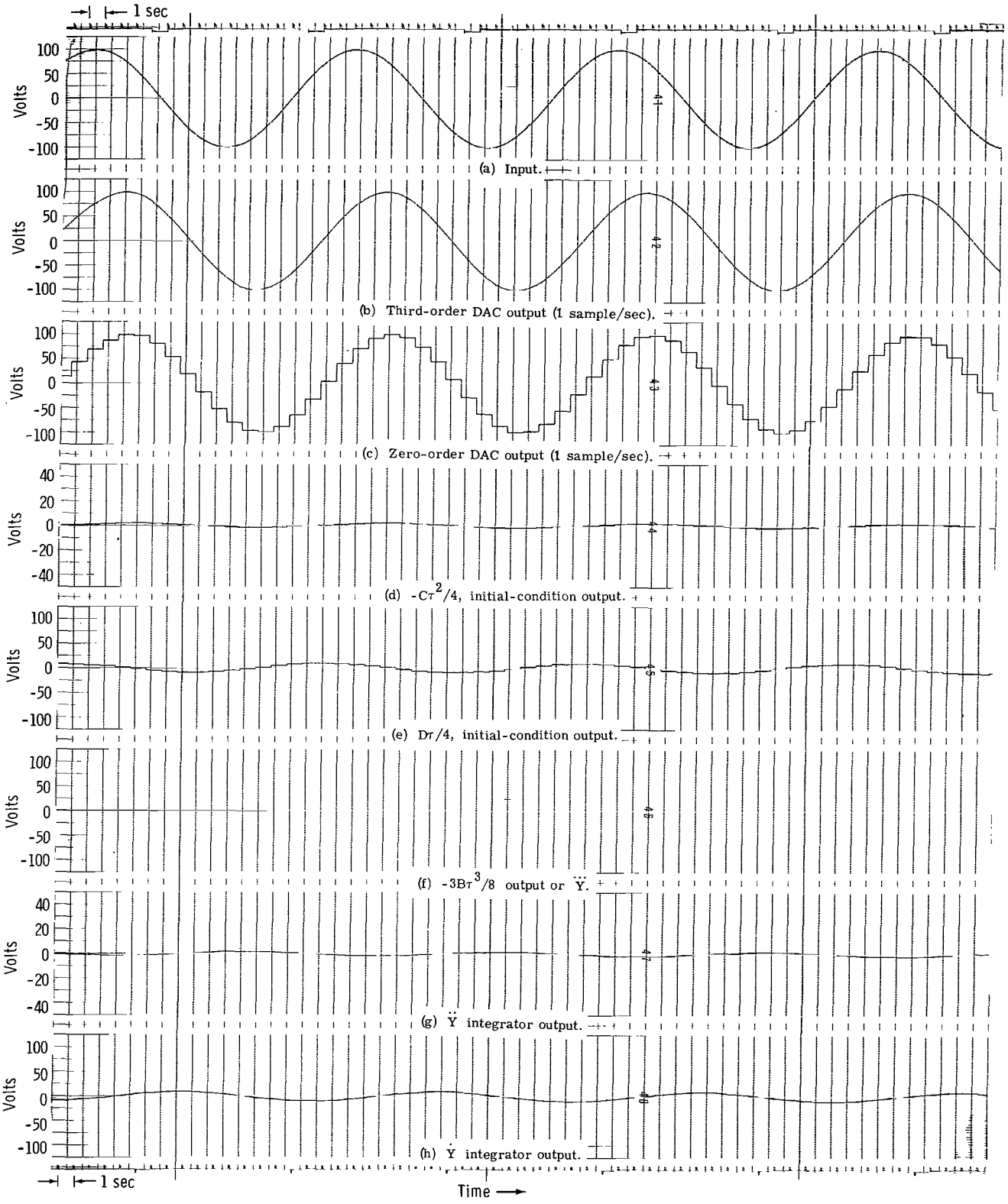


Figure 20. - Results of a 0.07-hertz sine-wave input (p = 14.3 samples/cycle) as a function of time.

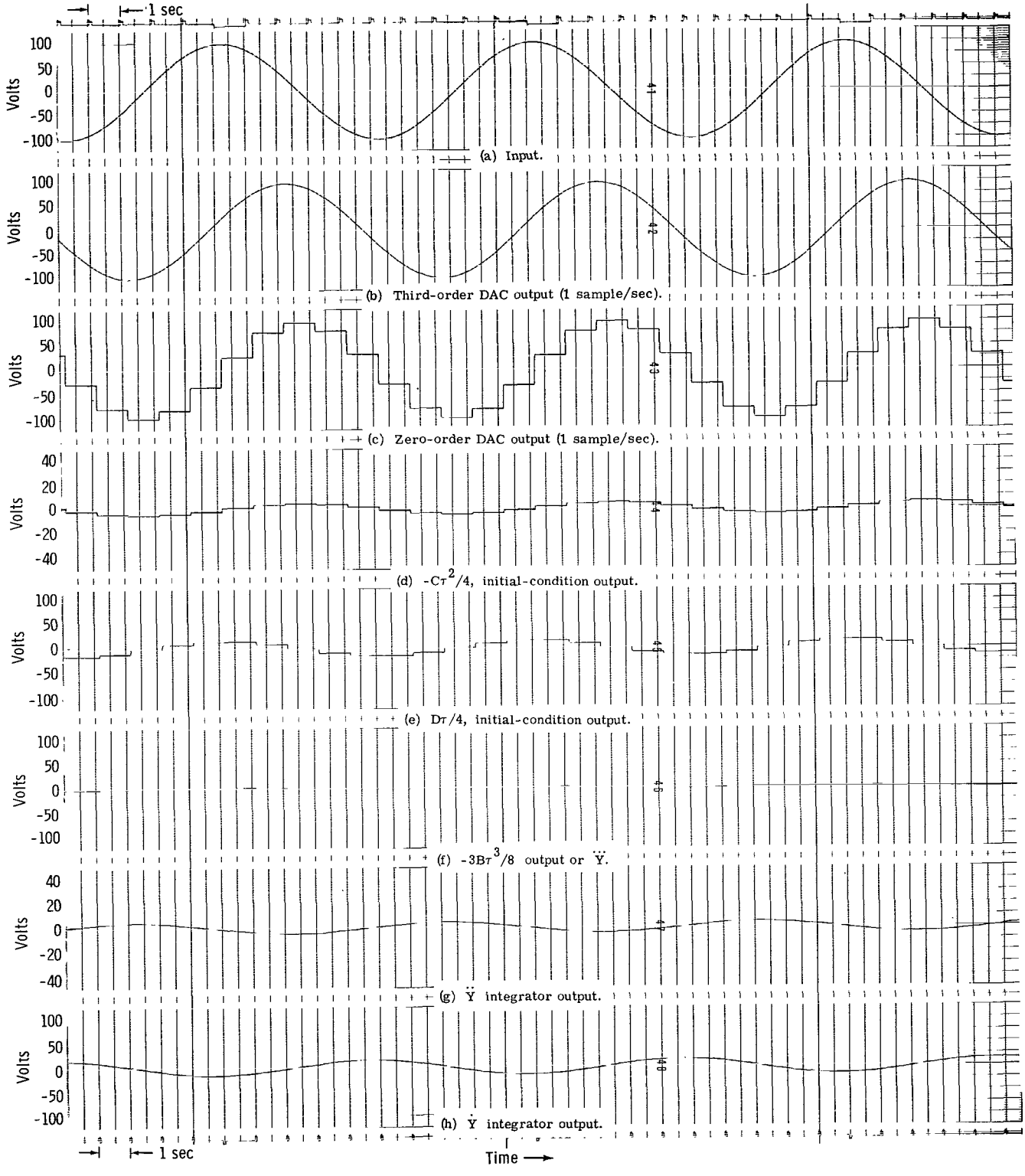


Figure 21.- Results of a 0.1-hertz sine-wave input (p = 10 samples/cycle) as a function of time.

Figure 22. - Results of a 0.2-hertz sine-wave input (p = 5 samples/cycle) as a function of time.

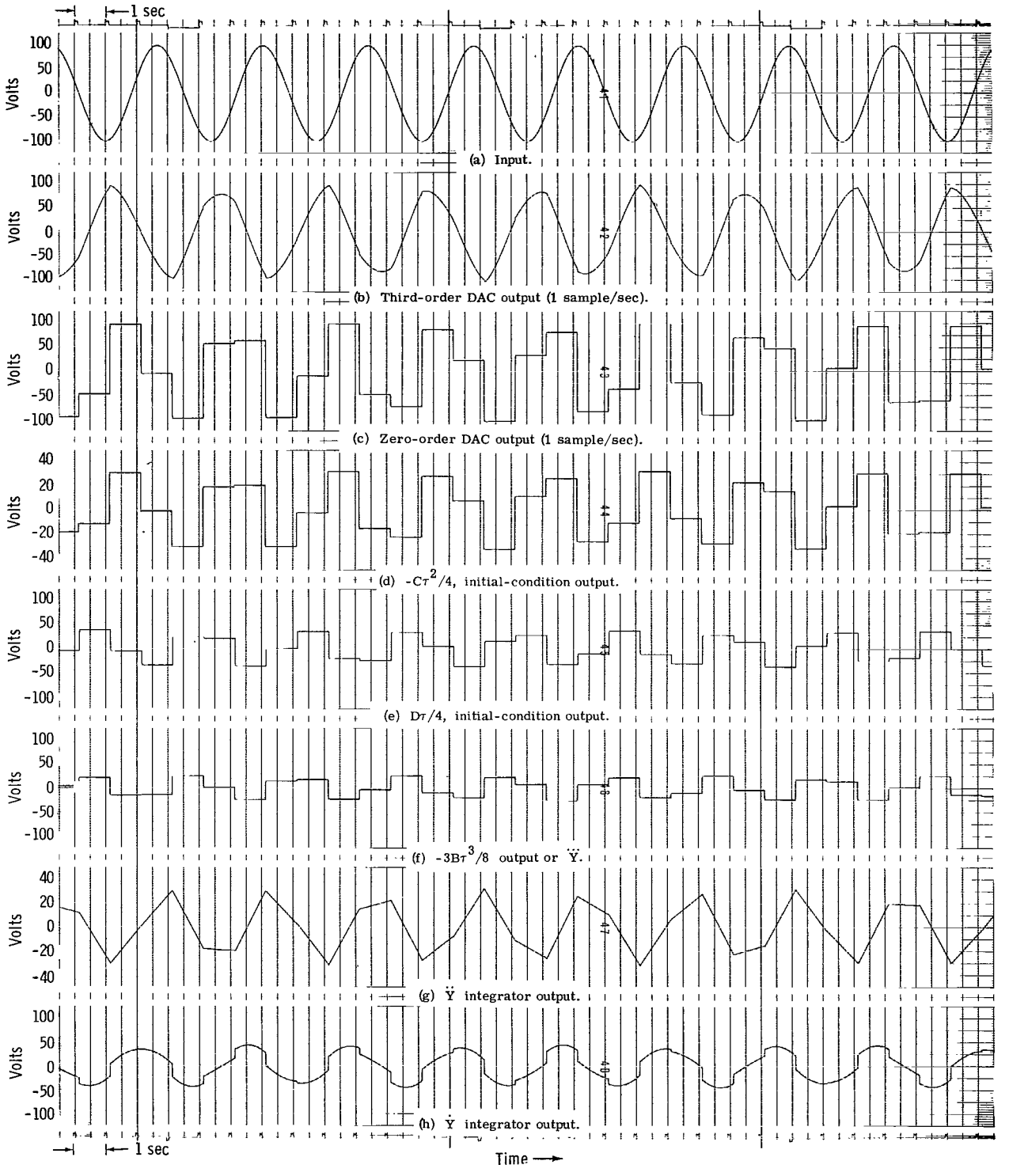


Figure 23.- Results of a 0.3-hertz sine-wave input (p = 3.33 samples/cycle) as a function of time.

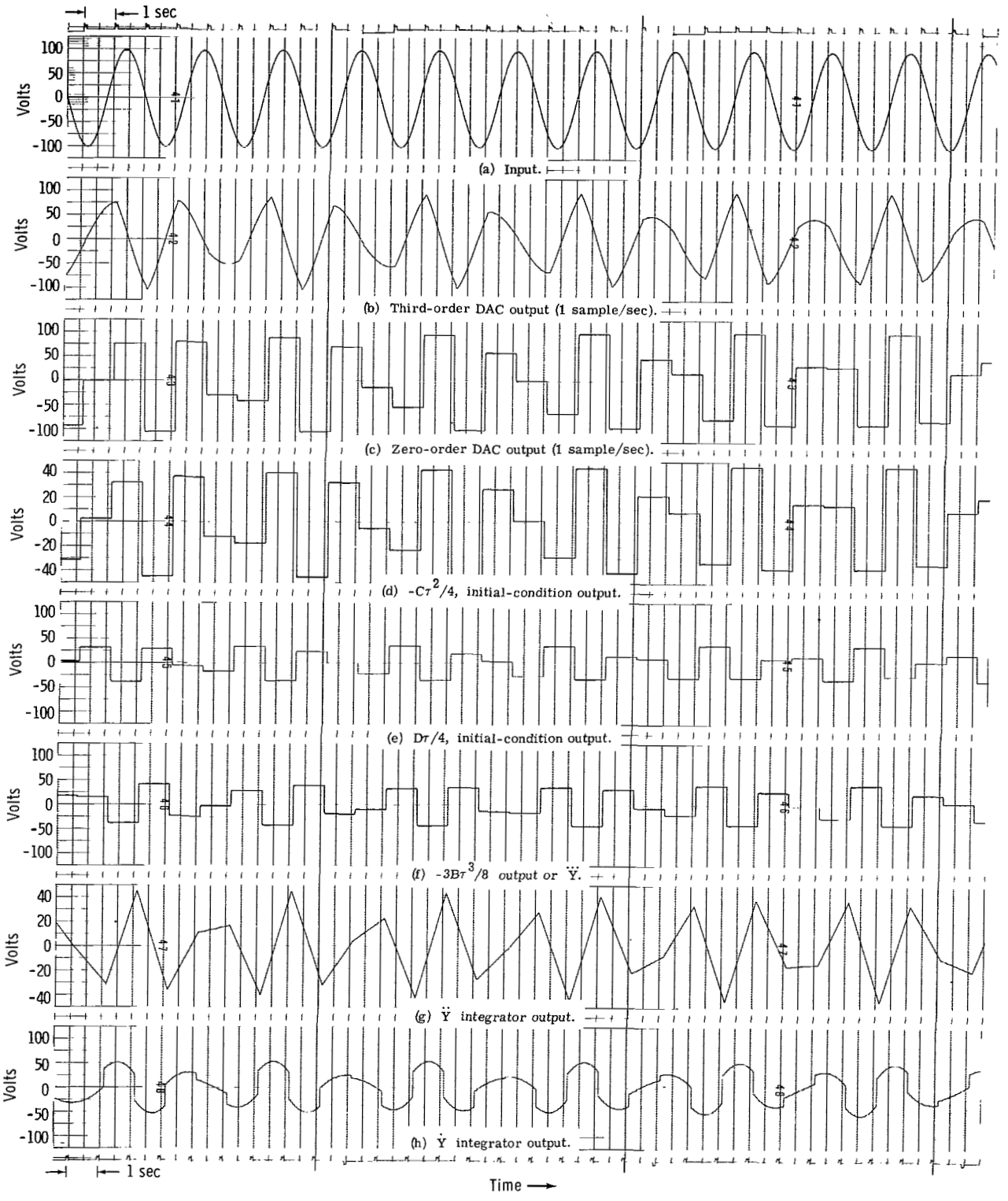


Figure 24. - Results of a 0.4-hertz sine-wave input (p = 2.5 samples/cycle) as a function of time.

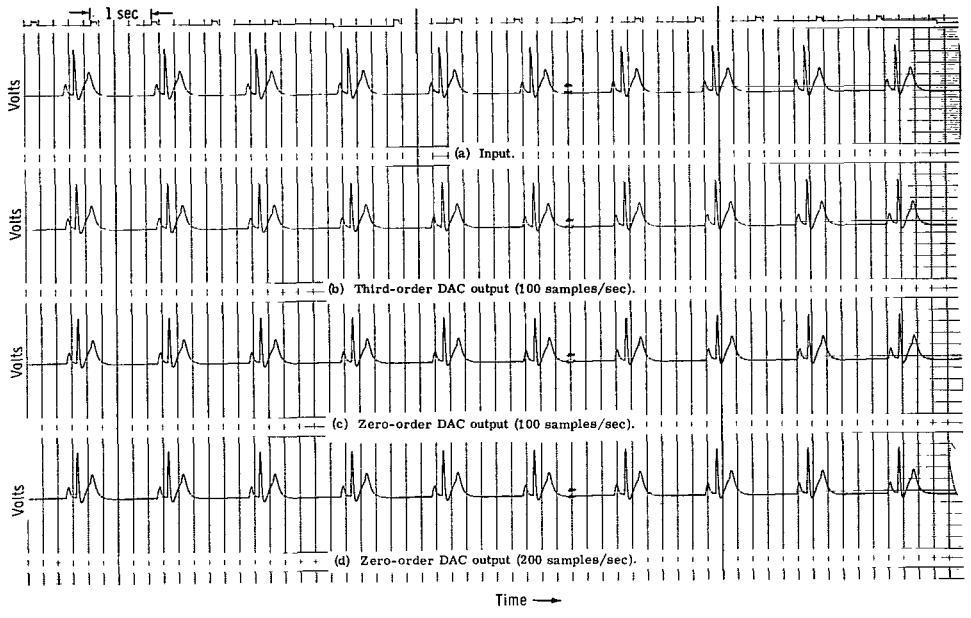


Figure 25. - Sinus bradycardia.

Figure 26. - Normal sinus.

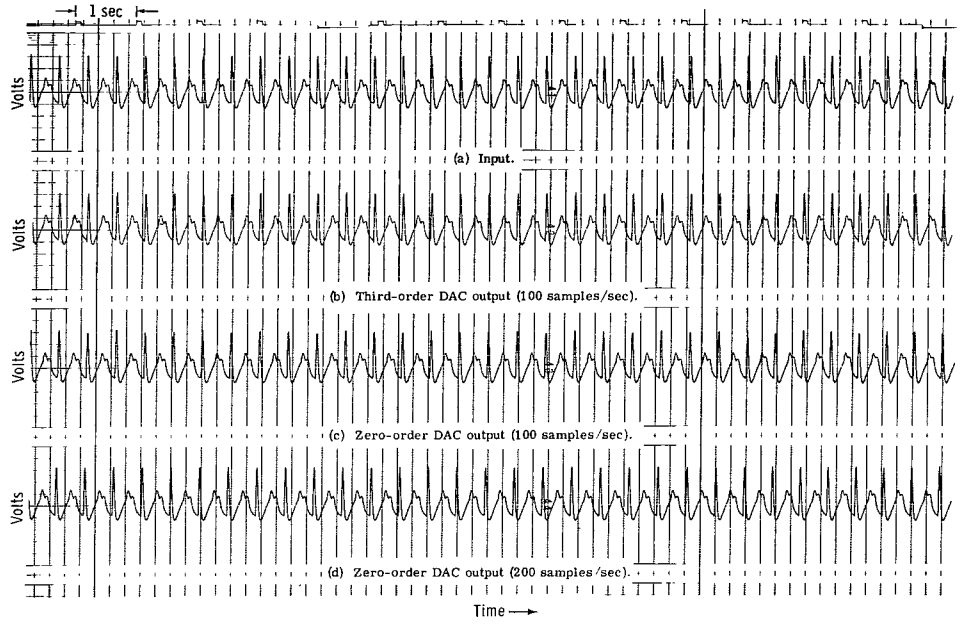


Figure 27. - Sinus tachycardia.

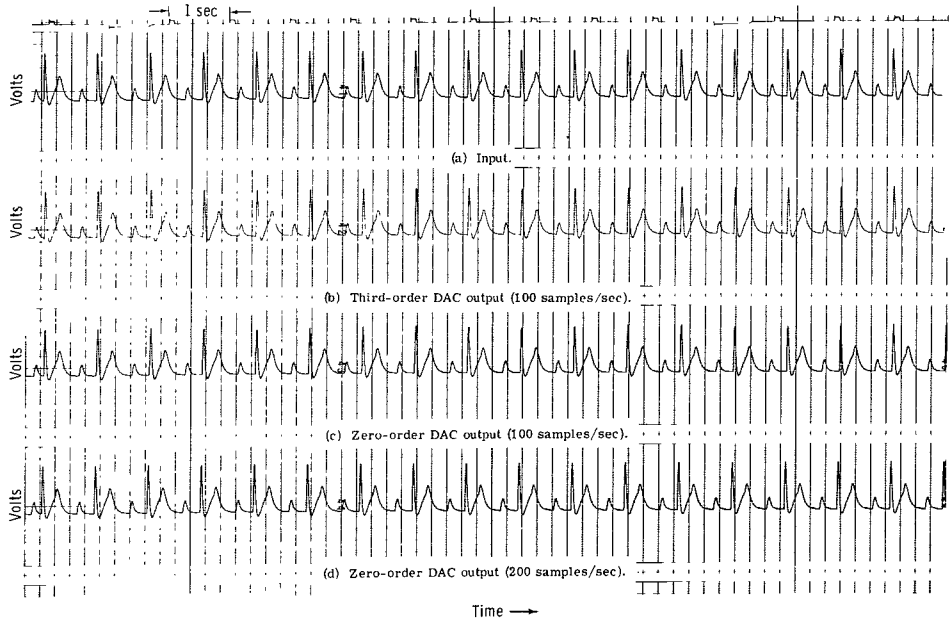


Figure 28. - First-degree block.

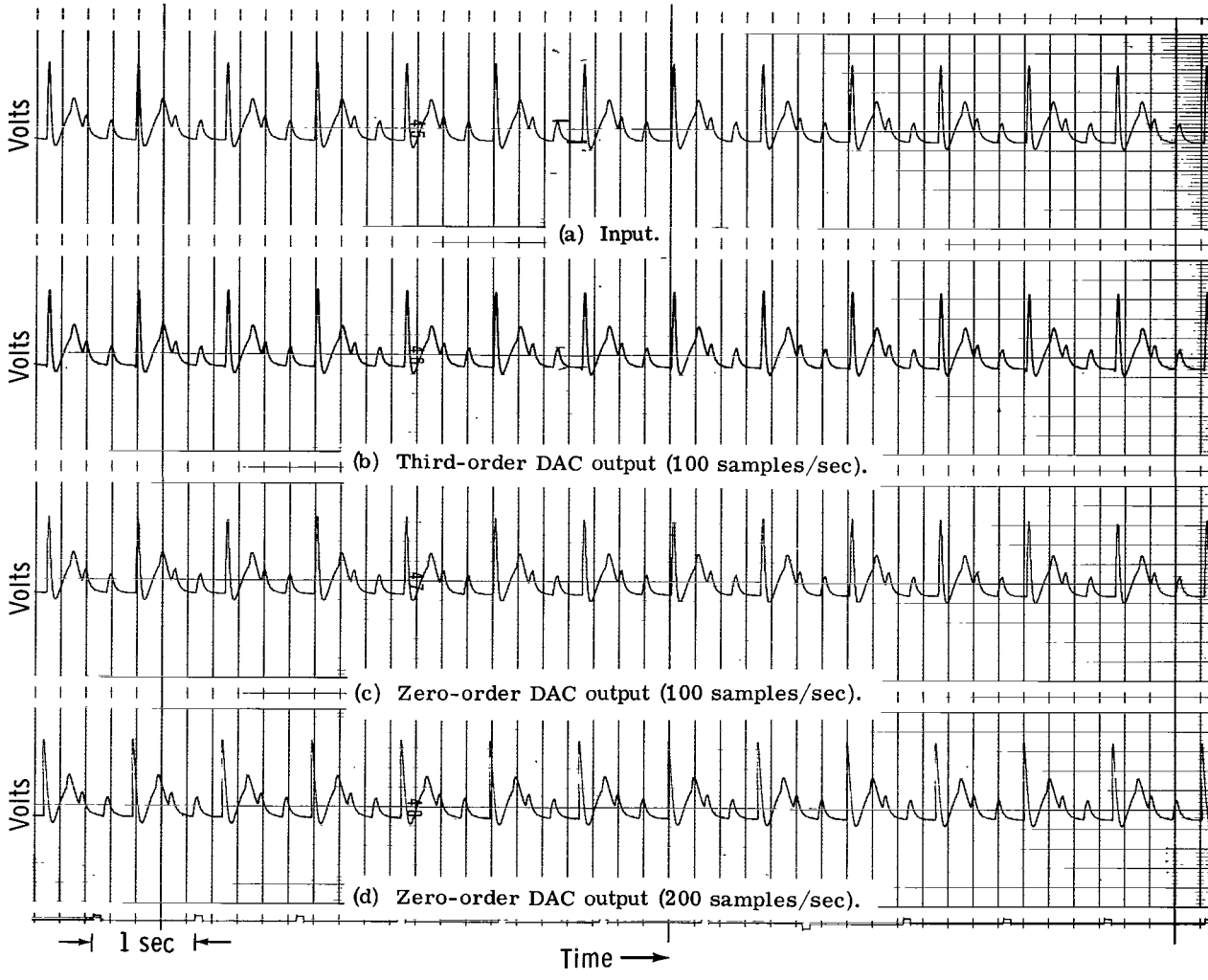


Figure 29. - Second-degree block.

Figure 30. - Third-degree block.

Figure 31. - Atrial flutter.

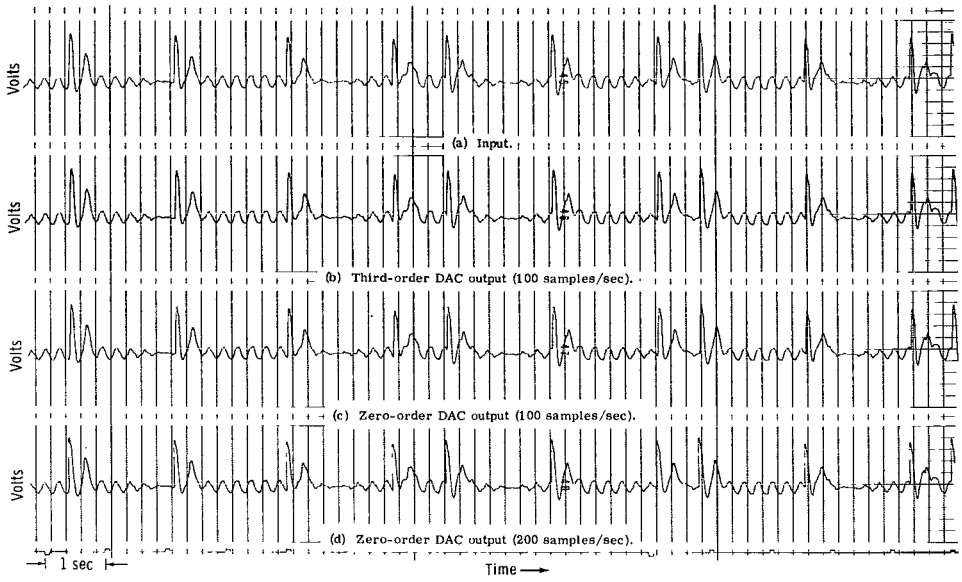


Figure 32. - Atrial fibrillation.

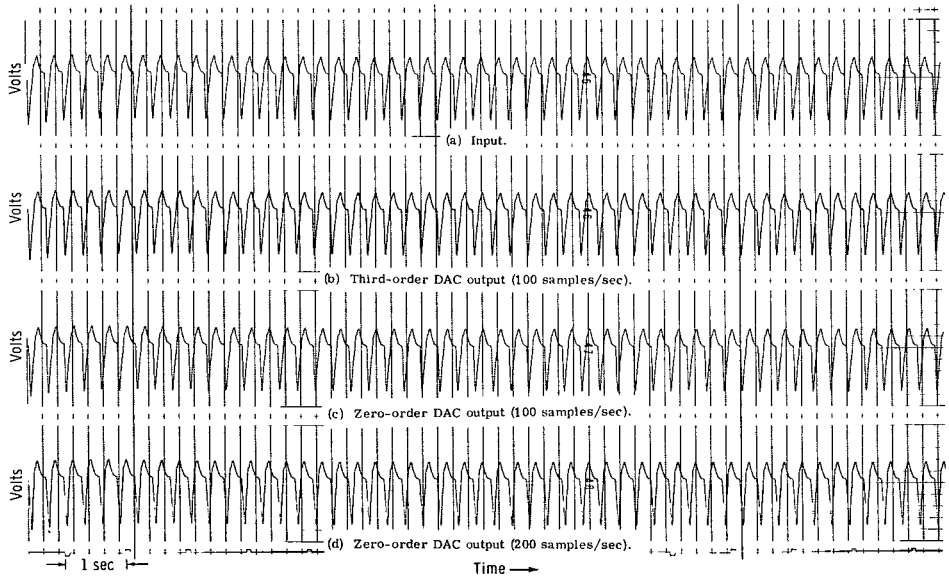


Figure 33. - Ventricular tachycardia.

Figure 34. - Ventricular fibrillation.

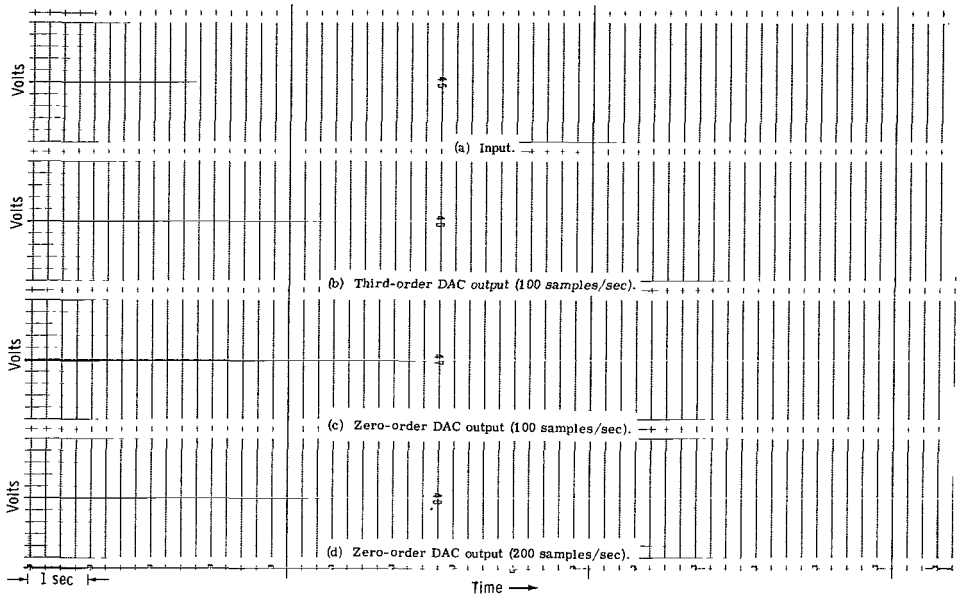


Figure 35. - Asystole.

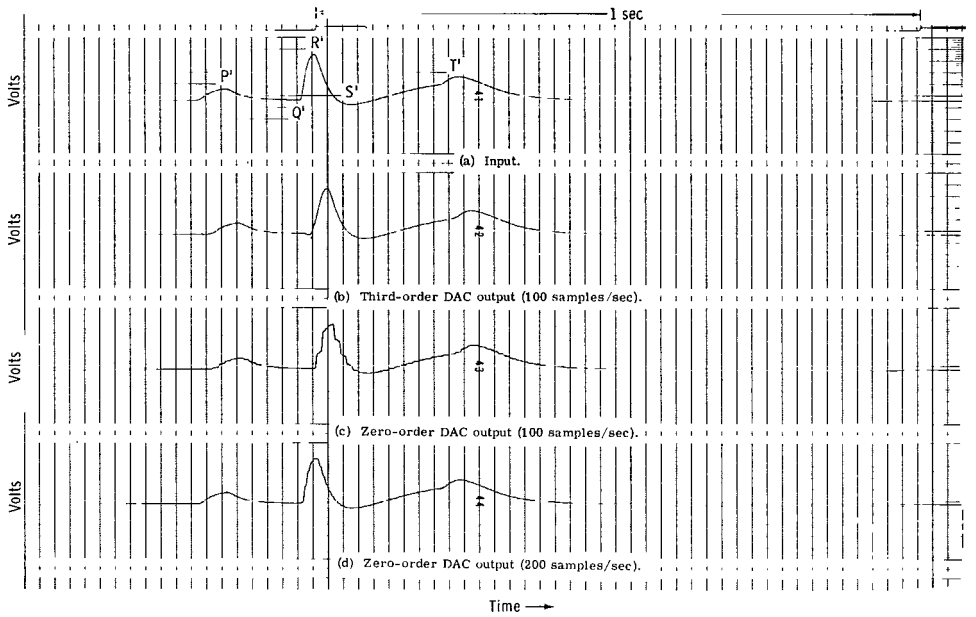


Figure 36. - Expanded view of normal sinus rhythm.

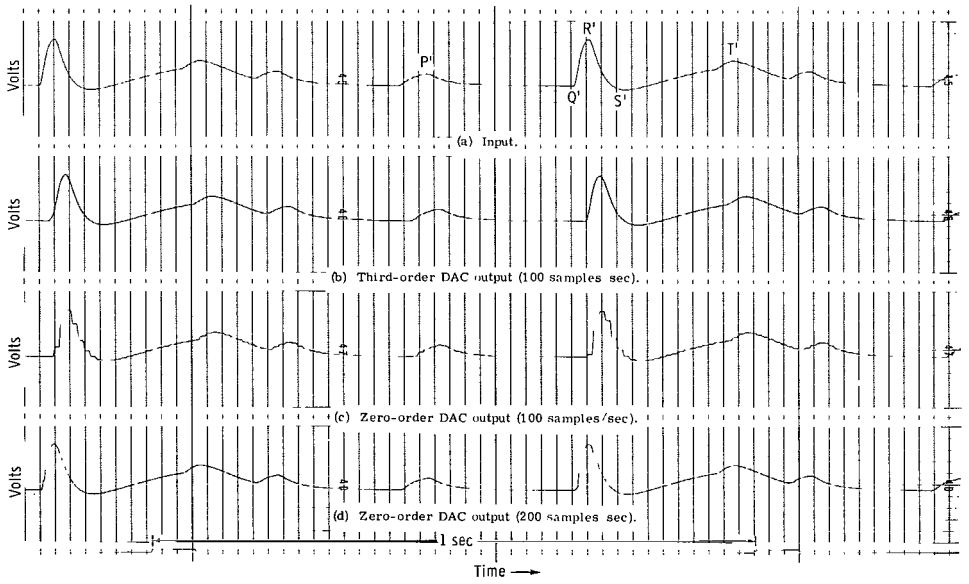


Figure 37. - Expanded view of second-degree block.

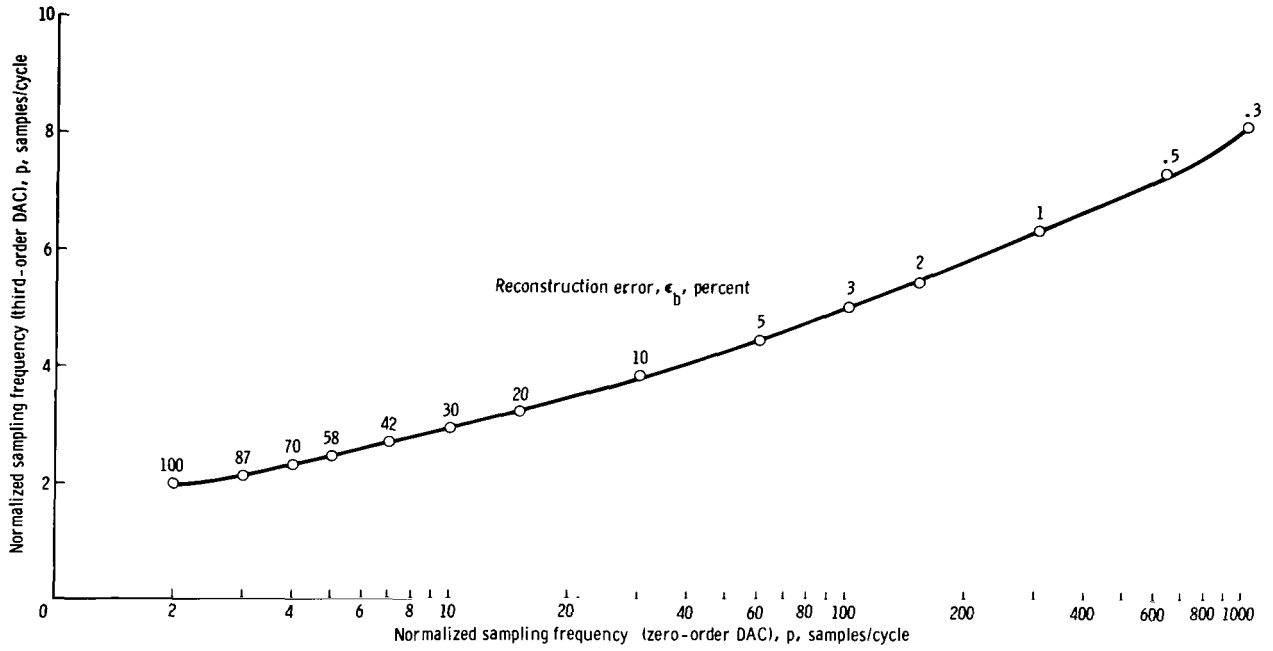


Figure 38. - Plot of sampling frequency required for a third-order DAC to equal the performance of a zero-order DAC at the base-line crossing.

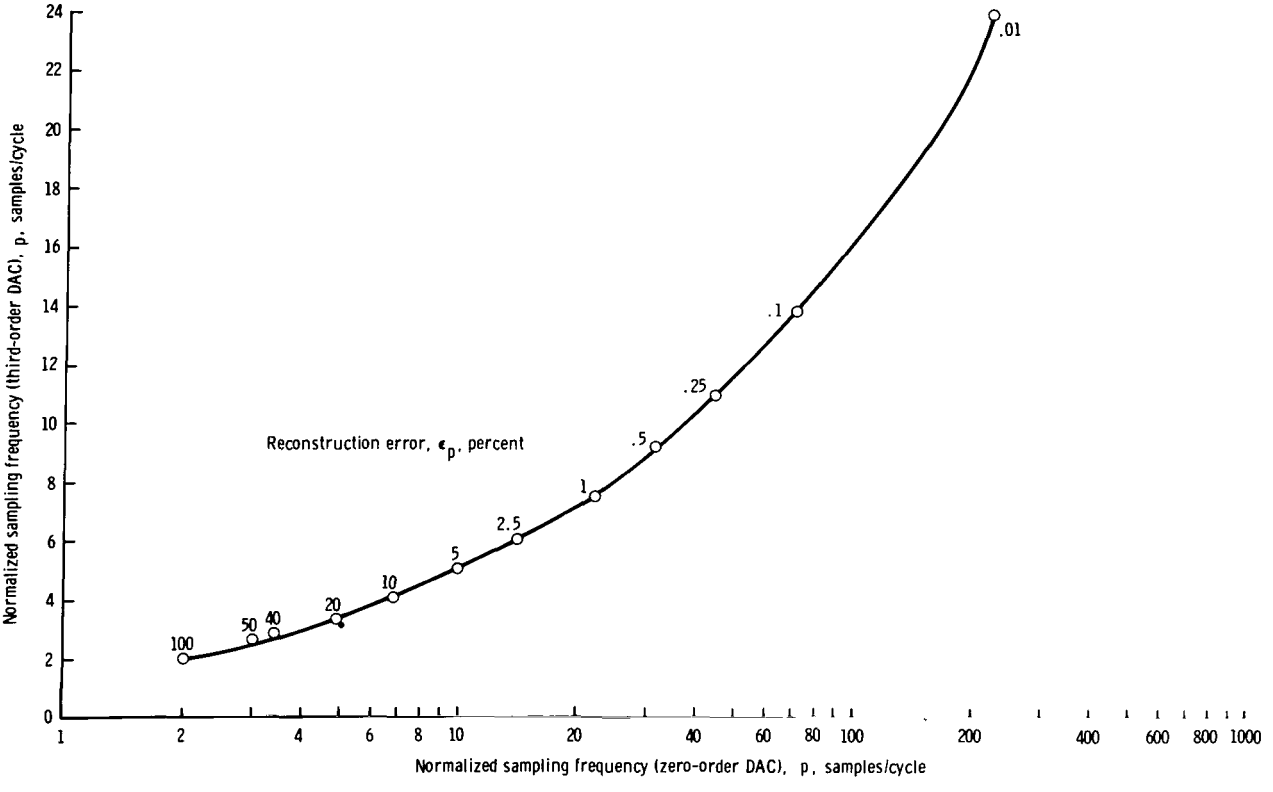


Figure 39. - Plot of sampling frequency required for a third-order DAC to equal the performance of a zero-order DAC at the waveform peaks.

CONCLUDING REMARKS

The experimental results of sample data that were processed by the third- and zero-order digital-to-analog converters indicate a markedly superior performance on the part of the third-order digital-to-analog converter. The experimental results are in close agreement with the results predicted by the theory.

It has been shown that the use of a third-order digital-to-analog converter will allow substantial reductions in the transmission bandwidth, with no decrease in the data quality. If no reductions in transmission bandwidth are necessary, then the use of a third-order digital-to-analog converter will greatly improve the quality of the reconstructed data.

Manned Spacecraft Center
National Aeronautics and Space Administration
Houston, Texas, October 14, 1971
921-10-00-00-72

REFERENCE

1. Dotson, William P., Jr.: Dynamic Reconstruction Errors in Digital-to-Analog Systems with Biomedical Applications. NASA TN D-6296, Apr. 1971.

APPENDIX A

ERROR EQUATIONS

The equations for the peak error ϵ_p and the base-line crossing error ϵ_b for a zero- and a third-order DAC were derived in reference 1 and are shown as follows. The zero ordinate of each figure was shifted to make the error equations as simple as possible.

ZERO-ORDER DAC

Figure A-1 is used to find the instantaneous error midway between two sample points for a zero-order DAC. This error is near the base-line crossing. The instantaneous error at $t = \tau/2$ for the sample-point locations shown in figure A-1 is

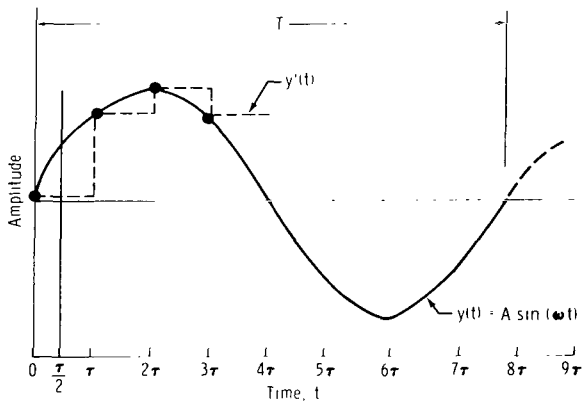


Figure A-1. - Geometry for calculating ϵ_b for a zero-order DAC.

$$\epsilon_b = \left| \frac{y\left(\frac{\tau}{2}\right) - y'\left(\frac{\tau}{2}\right)}{y_{max}} \right| (100) \qquad \text{(A1a)}$$

$$y(t) = A \sin(\omega t) \qquad \text{(A1b)}$$

$$y'(t) = A \sin[\omega(0)] \qquad 0 \le t < \tau \qquad \text{(A1c)}$$

$$y\left(\frac{\tau}{2}\right) = A \sin\left(\omega \frac{\tau}{2}\right) \qquad \text{(A1d)}$$

$$y'\left(\frac{\tau}{2}\right) = 0 \qquad \text{(A1e)}$$

$$y_{max} = A \qquad \text{(A1f)}$$

$$\epsilon_b = 100 \sin\left(\omega \frac{\tau}{2}\right) \qquad \omega = \frac{2\pi}{T}$$

$$\tau = \frac{T}{p} \qquad \text{(A1g)}$$

where p = normalized sample rate in samples/cycle

$$\epsilon_b = 100 \sin \frac{\pi}{p} \tag{A2}$$

Figure A-2 is used to find the instantaneous error at the peaks for a zero-order DAC. The instantaneous error at $t = 0$ for the sample-point locations shown in figure A-2 is

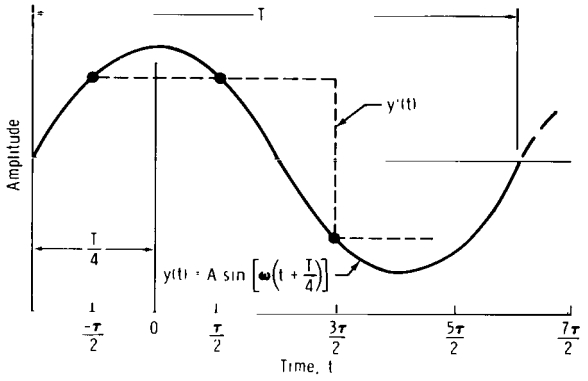


Figure A-2. - Geometry for calculating ϵ_p for a zero-order DAC.

$$\epsilon_p = \left| \frac{y(0) - y'(0)}{y_{max}} \right| (100) \tag{A3a}$$

$$y(t) = A \sin \left[\omega \left(t + \frac{T}{4} \right) \right] \tag{A3b}$$

$$y'(t) = A \sin \left[\omega \left(- \frac{\tau}{2} + \frac{T}{4} \right) \right]$$

$$- \frac{\tau}{2} \leq t < \frac{\tau}{2} \tag{A3c}$$

$$y(0) = A \sin \left[\omega \left(0 + \frac{T}{4} \right) \right] = A \tag{A3d}$$

$$y'(0) = A \sin \left[\omega \left(- \frac{\tau}{2} + \frac{T}{4} \right) \right] \tag{A3e}$$

$$y_{max} = A \tag{A3f}$$

$$\epsilon_p = 100 \left\{ 1 - \sin \left[\omega \left(- \frac{\tau}{2} + \frac{T}{4} \right) \right] \right\} \qquad \omega = \frac{2\pi}{T}$$

$$\tau = \frac{T}{p} \tag{A3g}$$

$$\epsilon_p = 100 \left\{ 1 - \sin \left[\pi \left(\frac{p - 2}{2p} \right) \right] \right\} \tag{A3h}$$

By using trigonometric identities, the equation

$$\epsilon_p = 100\left(1 - \cos\frac{\pi}{p}\right) \tag{A4}$$

can be obtained. Equations (A2) and (A4) are plotted in figure 3(c).

THIRD-ORDER DAC

Figure A-3 is used to find the instantaneous error midway between two sample points for a third-order DAC. This error is near the base-line crossing. The instantaneous error at $t = 0$ for the sample-point locations shown in figure A-3 is

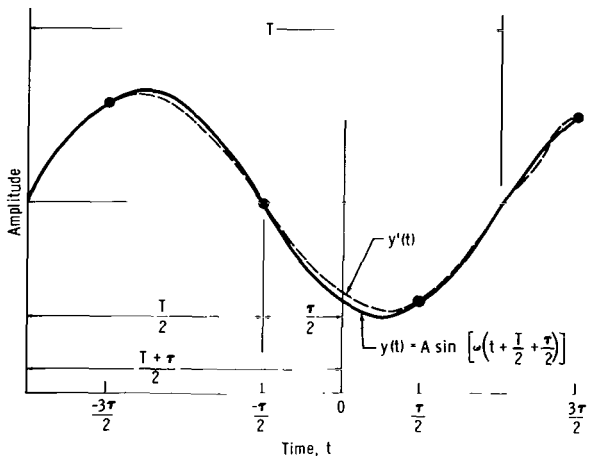


Figure A-3. - Geometry for calculating ϵ_b for a third-order DAC.

$$\epsilon_b = \left|\frac{y(0) - y'(0)}{y_{max}}\right|(100) \tag{A5a}$$

$$y(t) = A \sin\left[\omega\left(t + \frac{T}{2} + \frac{\tau}{2}\right)\right] \tag{A5b}$$

$$y'(t) = Bt^3 + Ct^2 + Dt + E$$

$$-\frac{3\tau}{2} \leq t < \frac{3\tau}{2} \tag{A5c}$$

$$y(0) = A \sin\left[\omega\left(\frac{T}{2} + \frac{\tau}{2}\right)\right] \tag{A5d}$$

$$y'(0) = E \tag{A5e}$$

$$y_{max} = A \tag{A5f}$$

$$\epsilon_b = 100\left\{\sin\left[\omega\left(\frac{T}{2} + \frac{\tau}{2}\right)\right] - \frac{E}{A}\right\} \tag{A6}$$

To find E, solve the set

$$y'\left(-\frac{3\tau}{2}\right) = B\left(-\frac{3\tau}{2}\right)^3 + C\left(-\frac{3\tau}{2}\right)^2 + D\left(-\frac{3\tau}{2}\right) + E = A \sin\left[\omega\left(\frac{T}{2} - \tau\right)\right] \tag{A7a}$$

$$y'\left(-\frac{\tau}{2}\right) = B\left(-\frac{\tau}{2}\right)^3 + C\left(-\frac{\tau}{2}\right)^2 + D\left(-\frac{\tau}{2}\right) + E = A \sin\left(\omega\frac{T}{2}\right) = 0 \tag{A7b}$$

$$y'\left(\frac{\tau}{2}\right) = B\left(\frac{\tau}{2}\right)^3 + C\left(\frac{\tau}{2}\right)^2 + D\left(\frac{\tau}{2}\right) + E = A \sin\left[\omega\left(\frac{T}{2} + \tau\right)\right] \tag{A7c}$$

$$y'\left(\frac{3\tau}{2}\right) = B\left(\frac{3\tau}{2}\right)^3 + C\left(\frac{3\tau}{2}\right)^2 + D\left(\frac{3\tau}{2}\right) + E = A \sin\left[\omega\left(\frac{T}{2} + 2\tau\right)\right] \tag{A7d}$$

$$E = \frac{A}{16}\left\{9 \sin\left[\omega\left(\frac{T}{2} + \tau\right)\right] - \sin\left[\omega\left(\frac{T}{2} - \tau\right)\right] - \sin\left[\omega\left(\frac{T}{2} + 2\tau\right)\right]\right\} \tag{A7e}$$

$$\epsilon_b = 100\left(\sin\left[\omega\left(\frac{T}{2} + \frac{\tau}{2}\right)\right] - \frac{1}{16}\left\{9 \sin\left[\omega\left(\frac{T}{2} + \tau\right)\right] - \sin\left[\omega\left(\frac{T}{2} - \tau\right)\right] - \sin\left[\omega\left(\frac{T}{2} + 2\tau\right)\right]\right\}\right) \tag{A7f}$$

Because $\omega = 2\pi/T$ and $\tau = T/p$

$$\epsilon_b = 100\left(\sin\left[\pi\left(\frac{p+1}{p}\right)\right] - \frac{1}{16}\left\{9 \sin\left[\pi\left(\frac{p+2}{p}\right)\right] - \sin\left[\pi\left(\frac{p-2}{p}\right)\right] - \sin\left[\pi\left(\frac{p+4}{p}\right)\right]\right\}\right) \tag{A7g}$$

By using trigonometric identities, the equation

$$\epsilon_b = 100\left[-\sin\frac{\pi}{p} + \frac{1}{16}\left(10 \sin\frac{2\pi}{p} - \sin\frac{4\pi}{p}\right)\right] \tag{A8}$$

can be obtained.

Figure A-4 is used to find the instantaneous error at the peaks for a third-order DAC. The instantaneous error at $t = 0$ for the sample-point locations shown in figure A-4 is

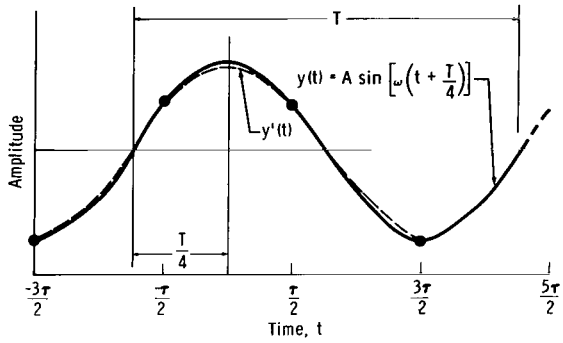


Figure A-4. - Geometry for calculating ϵ_p for a third-order DAC.

$$\epsilon_p = \left| \frac{y(0) - y'(0)}{y_{max}} \right| (100) \qquad \text{(A9a)}$$

$$y(t) = A \sin \left[\omega \left(t + \frac{T}{4} \right) \right] \qquad \text{(A9b)}$$

$$y'(t) = Bt^3 + Ct^2 + Dt + E$$

$$-\frac{3\tau}{2} \leq t < \frac{3\tau}{2} \qquad \text{(A9c)}$$

$$y(0) = A \sin \left(\omega \frac{T}{4} \right) = A \qquad \text{(A9d)}$$

$$y'(0) = E \qquad \text{(A9e)}$$

$$y_{max} = A \qquad \text{(A9f)}$$

$$\epsilon_p = 100 \left(1 - \frac{E}{A} \right) \qquad \text{(A10)}$$

To find E, solve the set

$$y'\left(-\frac{3\tau}{2}\right) = B\left(-\frac{3\tau}{2}\right)^3 + C\left(-\frac{3\tau}{2}\right)^2 + D\left(-\frac{3\tau}{2}\right) + E = A \sin \left[\omega \left(\frac{T}{4} - \frac{3\tau}{2} \right) \right] \qquad \text{(A11a)}$$

$$y'\left(-\frac{\tau}{2}\right) = B\left(-\frac{\tau}{2}\right)^3 + C\left(-\frac{\tau}{2}\right)^2 + D\left(-\frac{\tau}{2}\right) + E = A \sin \left[\omega \left(\frac{T}{4} - \frac{\tau}{2} \right) \right] \qquad \text{(A11b)}$$

$$y'\left(\frac{\tau}{2}\right) = B\left(\frac{\tau}{2}\right)^3 + C\left(\frac{\tau}{2}\right)^2 + D\left(\frac{\tau}{2}\right) + E = A \sin \left[\omega \left(\frac{T}{4} + \frac{\tau}{2} \right) \right] \qquad \text{(A11c)}$$

$$y'\left(\frac{3\tau}{2}\right) = B\left(\frac{3\tau}{2}\right)^3 + C\left(\frac{3\tau}{2}\right)^2 + D\left(\frac{3\tau}{2}\right) + E = A \sin\left[\omega\left(\frac{T}{4} + \frac{3\tau}{2}\right)\right] \tag{A11d}$$

which results in

$$E = \frac{A}{16}\left(9\left\{\sin\left[\omega\left(\frac{T}{4} - \frac{\tau}{2}\right)\right] + \sin\left[\omega\left(\frac{T}{4} + \frac{\tau}{2}\right)\right]\right\} - \left\{\sin\left[\omega\left(\frac{T}{4} - \frac{3\tau}{2}\right)\right] + \sin\left[\omega\left(\frac{T}{4} + \frac{3\tau}{2}\right)\right]\right\}\right) \tag{A11e}$$

where $\omega = 2\pi/T$ and $\tau = T/p$. By using trigonometric identities, the equation

$$\epsilon_p = 100\left[1 - \frac{1}{8}\left(9 \cos\frac{\pi}{p} - \cos\frac{3\pi}{p}\right)\right] \tag{A12}$$

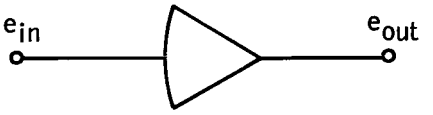
can be obtained.

A comparison of the errors obtained with a third-order DAC and a zero-order DAC can be determined by cross plotting the normalized sampling rate of each and indicating the percent errors at various points, as is done in figures 38 and 39. The figures show that for normalized sampling frequencies above 5 samples/cycle, it becomes advantageous to use a third-order DAC instead of a zero-order DAC. In figure 39 — the worst case of the two — for $p = 10$ on the zero-order DAC, $p \approx 5$ on the third-order DAC for the same accuracy.

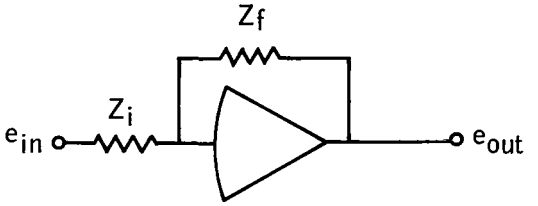
APPENDIX B

SPECIFIC DESIGN FORMULAS

The basic design element in analog circuitry is the high-gain amplifier, which is indicated by the following symbol.

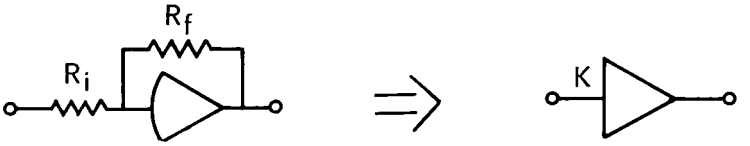


Ideally, the high-gain amplifier has infinite open-loop gain, infinite input impedance, and zero output impedance. Normally, the gain is also assumed to be negative; that is, the amplifier inverts the signal. Under these conditions, for the following circuit configuration, equation (B1) is applicable.

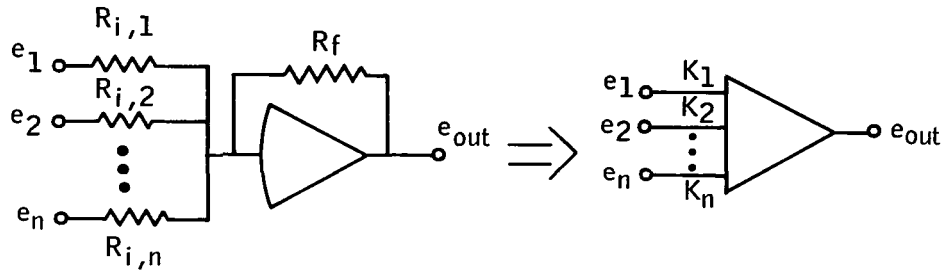


$$e_{out} = -\frac{Z_f}{Z_i} e_{in} = -Ke_{in} \tag{B1}$$

The gain for this circuit configuration, then, is a function of only Z_f and Z_i. Rather than always drawing in the impedance elements, a new symbol is usually defined

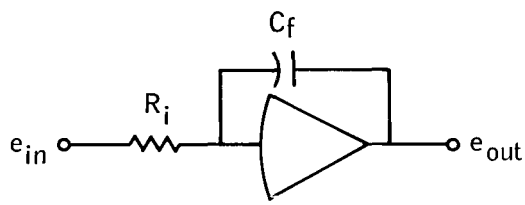


where K is the ratio of the feedback impedance to the input impedance. Summing amplifiers are easily constructed from the previous configuration and have output voltages given by equation (B2).



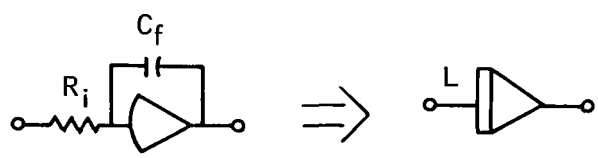
$$e_{out} = -\left(K_1 e_1 + K_2 e_2 + \ldots + K_n e_n\right) \tag{B2}$$

Integrators are formed by changing the feedback element to a capacitor and have output voltages given by equation (B3).



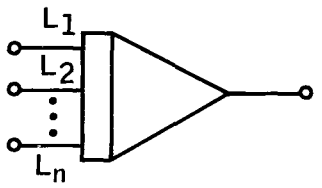
$$e_{out} = -\frac{Z_f}{Z_i} e_{in} = -\left(\frac{1}{s}\right)\left(\frac{1}{R_i C_f}\right) e_{in} \tag{B3}$$

The term $1/s$ is a Laplacian operator that indicates integration. The term $1/R_iC_f$ controls the gain involved in the integration. The previous configuration may be abbreviated to

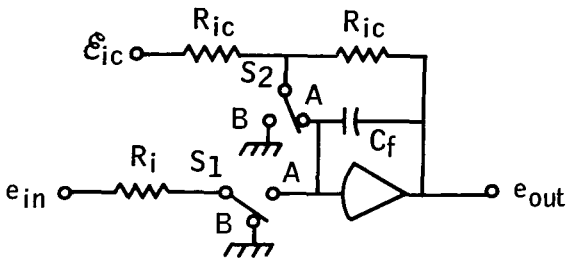


where $L = 1/R_iC_f$.

Integrators can also be configured to form the integral of summed inputs.



Initial conditions must be known before solutions to integrals can be found. Known initial conditions can be placed on integrator outputs by appropriately charging the capacitor in the feedback loop. The time in which this capacitor is being charged is called the reset time. Integrators, then, have additional circuitry that is used for setting or resetting the initial conditions on output. One possible circuit follows.



Mode	S1	S2
Reset	B	A
Operate	A	B

Because of the assumed infinite gain of the amplifier, the point A is at a virtual ground; therefore

$$\frac{\mathscr{E}_{ic}}{R_{ic}} + \frac{e_{out}}{R_{ic}} + C_f \frac{d(e_{out})}{dt} = 0 \qquad \text{(B4)}$$

Equation (B4) can be written as follows by using Laplace-transform notation.

$$\frac{\mathscr{E}_{ic}}{sR_{ic}} + \frac{e_{out}}{R_{ic}} + C_f\left[se_{out} - e_{out}(0)\right] = 0 \qquad \text{(B5)}$$

or

$$e_{out}\left(\frac{1}{R_{ic}} + sC_f\right) = -\frac{\mathcal{E}_{ic}}{sR_{ic}} + C_f e_{out}(0) \tag{B6}$$

$$e_{out} = \frac{e_{out}(0)}{s + \frac{1}{R_{ic}C_f}} - \frac{\mathcal{E}_{ic}}{R_{ic}C_f}\left[\frac{1}{(s)\left(s + 1/R_{ic}C_f\right)}\right] \tag{B7}$$

$$e_{out}(t) = e_{out}(0)e^{-t/R_{ic}C_f} - \frac{\mathcal{E}_{ic}}{R_{ic}C_f}\left(\frac{1 - e^{-t/R_{ic}C_f}}{1/R_{ic}C_f}\right) \tag{B8}$$

$$e_{out}(t) = e_{out}(0)e^{-t/R_{ic}C_f} - \mathcal{E}_{ic}\left(1 - e^{-t/R_{ic}C_f}\right) \tag{B9}$$

It should be apparent that a definite time interval is required to set the initial conditions on the integrator output. At $t = 5R_{ic}C_f$, the output will have reached 99-1/3 percent of its correct value. After this time has elapsed, the integrator may be switched to the operate mode. The reset time then should be

$$\rho \geq 5R_{ic}C_f \tag{B10}$$

For a duty cycle of 99 percent (operate-to-reset ratio), $\rho \leq 0.01\tau$, where τ is the time interval between samples. A further constraint on the integrator circuitry is in its gain. The integrator gain L is

$$L = \frac{1}{\tau} = \frac{1}{R_i C_f} \tag{B11}$$

APPENDIX C

SCALING COMPUTATIONS

The scaling equations are developed by conjecturing a normalized full-scale sine-wave input sampled at a very high rate so that, in the limit, the sequential values of E (fig. 11) approach Y. That is

$$\lim_{p \to \infty} E \longrightarrow Y = \sin \omega t \tag{C1}$$

The first three derivatives of Y can then be found.

$$\dot{Y} = \omega \cos \omega t \tag{C2}$$

$$\ddot{Y} = -\omega^2 \sin \omega t \tag{C3}$$

$$\dddot{Y} = -\omega^3 \cos \omega t \tag{C4}$$

If equations (8) and (15) from the text are equated

$$\dot{Y}(0) = D = \frac{1}{6\tau}\left(-2Y_1 - 3Y_2 + 6Y_3 - Y_4\right) \to \omega \cos \omega t \tag{C5}$$

If equation (C5) is manipulated and multiplied by the scale factor F

$$F6\tau\dot{Y}(0) = F6\tau D = F\left(-2Y_1 - 3Y_2 + 6Y_3 - Y_4\right) \to F6\tau\omega \cos \omega t \tag{C6}$$

If $\sin \omega t$ is a full-scale output, then $F6\tau\omega$ is chosen such that $F6\tau\omega \cos \omega t$ is one-half full scale. (One-half full-scale output is chosen arbitrarily to avoid both of two common error sources in analog devices, which are (1) the nonlinearity errors at full-scale voltage outputs and (2) noise errors at voltage outputs near zero.) Therefore

$$F6\tau\omega = \frac{1}{2} \tag{C7}$$

and

$$F = \frac{1}{12\tau\omega} \tag{C8}$$

Because $\omega = 2\pi f$, $\tau = 1/f_s$, and $p = f_s/f$,

$$F = \frac{p}{24\pi} \tag{C9}$$

Equation (C9) implies that the scale factor depends on the lowest samples/cycle desired. If a rate of only π samples/cycle is desired, $p = \pi$ and $F = 1/24$. The initial condition on $\dot{Y}$ should then be scaled to be

$$\frac{6\tau\dot{Y}(0)}{24} = \frac{\tau\dot{Y}(0)}{4} = \frac{D\tau}{4} \tag{C10}$$

so that

$$\frac{D\tau}{4} = \frac{1}{24}\left(-2Y_1 - 3Y_2 + 6Y_3 - Y_4\right) \tag{C11}$$

Similarly, the scale factor G on $\ddot{Y}(0)$ can be found.

$$\ddot{Y}(0) = 2C = \frac{1}{\tau^2}\left(Y_1 - 2Y_2 + Y_3\right) \tag{C12}$$

where

$$\lim_{p \to \infty} \frac{1}{\tau^2}\left(Y_1 - 2Y_2 + Y_3\right) \longrightarrow -\omega^2 \sin \omega t \tag{C13}$$

and

$$G\tau^2\ddot{Y}(0) = 2G\tau^2 C = G\left(Y_1 - 2Y_2 + Y_3\right) \tag{C14}$$

where

$$\lim_{p \to \infty} G\left(Y_1 - 2Y_2 + Y_3\right) \longrightarrow - G\tau^2\omega^2 \sin \omega t \tag{C15}$$

Because $G\tau^2\omega^2 = 1/2$

$$G = \frac{1}{2\omega^2\tau^2} \tag{C16}$$

and

$$G = \frac{1}{\frac{8\pi^2 f^2}{f_s^2}} = \frac{p^2}{8\pi^2} \tag{C17}$$

For $p = \pi$, $G = 1/8$. Thus

$$G\tau^2\ddot{Y}(0) = \frac{\tau^2\ddot{Y}(0)}{8} = \frac{C\tau^2}{4} \tag{C18}$$

and

$$\frac{C\tau^2}{4} = \frac{1}{8}\left(Y_1 - 2Y_2 + Y_3\right) \tag{C19}$$

Similarly, the scale factor H on $\ddot{Y}(0)$ can be found.

$$\dddot{Y}(0) = 6B = \frac{1}{\tau^3}\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \tag{C20}$$

where

$$\lim_{p \to \infty} \frac{1}{\tau^3}\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \longrightarrow -\omega^3 \cos \omega t \tag{C21}$$

and

$$H\tau^3\dddot{Y}(0) = 6H\tau^3 B = H\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \tag{C22}$$

where

$$\lim_{p \to \infty} H\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \longrightarrow -H\tau^3\omega^3 \cos \omega t \tag{C23}$$

Because

$$H\tau^3\omega^3 = \frac{1}{2} \tag{C24}$$

and

$$H = \frac{p^3}{16\pi^3} \tag{C25}$$

for $p = \pi$, then $H = 1/16$. Thus

$$H\tau^3\dddot{Y}(0) = \frac{\tau^3}{16}\dddot{Y}(0) = \frac{6B\tau^3}{16} = \frac{1}{16}\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \tag{C26}$$

where

$$\frac{3B\tau^3}{8} = \frac{1}{16}\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right) \tag{C27}$$

APPENDIX D

CALIBRATION PROCEDURES

The initial-condition circuitry shown in figure 9 computes numerical approximations to successive derivatives of the original waveform. The derivatives are then used to drive the integrator circuitry. Obviously, if the derivative calculations are in error, the final output will also be in error.

One means of calibrating the initial-condition circuitry is to put a sampled function with known derivatives into the total circuit and then examine the outputs of the initial-condition circuitry. The easiest function to work with in this instance is a step input, so that in the steady state, all derivatives are zero. With this input, the outputs of the initial-condition circuitry should be identically zero; if they are not, the potentiometers in front of the summing amplifiers require adjustment.

The integrator gains may also require adjustment. Their theoretically required gain $1/\tau$ may not be realized because of tolerance limits on the feedback capacitors, input resistors, et cetera. For this reason, potentiometers were included in front of each integrator for fine adjustments.

From an inspection of the circuit shown in figure 11, it should be clear that the integrator chain serves only to fill in estimates of data values within the given sequence of data values Y_2, which is the initial-condition input of the final integrator. It is intuitively obvious, then, that the potentiometers in front of each integrator should be adjusted so that the final output is piecewise continuous. A sampled sine-wave input is easiest to work with in this instance.

The outputs of the three integrators can be checked to see if they are piecewise continuous as follows. First, the output of the integrator will be determined. The output of the first integrator (I1) can be determined by

$$I1 = -\int -\frac{3B\tau^3}{8}\left(\frac{2}{\tau}\right)dt + \frac{C\tau^2}{4} \tag{D1}$$

or

$$I1 = \frac{3B\tau^2}{4}(t) + \frac{C\tau^2}{4} \tag{D2}$$

The output can be checked to determine if it is piecewise continuous by evaluating $I1|_{t=\tau}$ and comparing the result with the initial condition at the next set of data values. That is, the continuity can be checked by asking whether

$$\frac{3B\tau^2}{4} t + \frac{C\tau^2}{4} = \frac{C'\tau^2}{4} \tag{D3}$$

After solving, it is determined that

$$Y_2 - 2Y_3 + Y_4 = Y_2 - 2Y_3 + Y_4 \tag{D4}$$

Therefore, the output of I1 is piecewise continuous.

The output of integrator two (I2) can be found as follows.

$$I2 = -\int \left(\frac{3B\tau^2}{4} t + \frac{C\tau^2}{4}\right)\frac{2}{\tau}\, dt - \frac{D\tau}{4} \tag{D5}$$

or

$$I2 = -\frac{3B\tau}{4} t^2 - \frac{C\tau}{2} t - \frac{D\tau}{4} \tag{D6}$$

The output of I2 can be checked for piecewise continuity by asking whether

$$I2|_{t=\tau} = -\frac{D'\tau}{4} \tag{D7}$$

or

$$-\frac{3B\tau^3}{4} - \frac{C\tau^2}{2} - \frac{D\tau}{4} = -\frac{D'\tau}{4} \tag{D8}$$

When equation (D8) is solved, it is found that

$$-Y_1 + 6Y_2 - 3Y_3 - 2Y_4 \neq 2Y_2 + 3Y_3 - 6Y_4 + Y_5 \tag{D9}$$

Therefore, the output of I2 is not necessarily piecewise continuous.

The output of integrator three (I3) is

$$I3 = -\int \left(-\frac{3B\tau}{4}t^2 - \frac{C\tau}{2}t - \frac{D\tau}{4}\right)\left(\frac{4}{\tau}\right)dt + E \tag{D10}$$

or

$$I3 = Bt^3 + Ct^2 + Dt + E \tag{D11}$$

The output of I3 can be checked for piecewise continuity by determining whether

$$I3\Big|_{t=\tau} = E' \tag{D12}$$

or

$$\left(-Y_1 + 3Y_2 - 3Y_3 + Y_4\right)\left(\frac{1}{6\tau^3}\right)\tau^3 + \left(Y_1 - 2Y_2 + Y_3\right)\left(\frac{\tau^2}{2\tau^2}\right)$$

$$+ \left(-2Y_1 - 3Y_2 + 6Y_3 - Y_4\right)\left(\frac{\tau}{6\tau}\right) + Y_2 = Y_3 \tag{D13}$$

When equation (D13) is solved, it is found that $Y_3 = Y_3$. Therefore, the output of I3 is piecewise continuous.

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