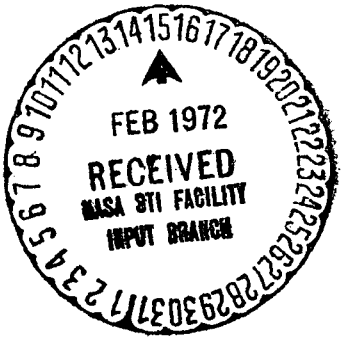


LOCKHEED ELECTRONICS COMPANY, INC.

HOUSTON AEROSPACE SYSTEMS

A Subsidiary of Lockheed Aircraft Corporation

(NASA-CR-115360) BIOMEDICAL COMPUTING FACILITY INTERFACE DESIGN PLAN R.D. Puckett (Lockheed Electronics Co.) Nov. 1971 56 p

CSCL 09B

N72-17136

Unclas

G3/08 16477

Engineering Data Systems
Department No.: 62820F/127704

Project No.: 7005

TECHNICAL REPORT

BIOMEDICAL COMPUTING FACILITY INTERFACE DESIGN PLAN

R. D. Puckett

Engineering Data Systems
Department
Lockheed Electronics Co., Inc.

November 1971

Prepared Under Contract NAS 9-12200 by

LOCKHEED ELECTRONICS COMPANY, INC.
HOUSTON AEROSPACE SYSTEMS DIVISION

FOR

COMPUTATION AND ANALYSIS DIVISION

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION
MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

Engineering Data Systems
Department No.: 62820F/127704

Project No.: 7005

TECHNICAL REPORT

BIOMEDICAL COMPUTING FACILITY INTERFACE DESIGN PLAN

November 1971

Prepared by:

R. D. Puckett
Hybrid Systems Section

Approved by:

T. A. Jagen, Supervisor
Hybrid Systems Section

Approved by:

G. L. Walker, Chief
Systems Development Section
Engineering Systems Branch
CAD-MSC

Approved by:

P. T. Schuyler, Manager
Engineering Data Systems
Department

ENGINEERING DATA SYSTEMS DEPARTMENT
LOCKHEED ELECTRONICS COMPANY, INC.
HOUSTON AEROSPACE SYSTEMS DIVISION

TABLE OF CONTENTS

		Page
1.	INTRODUCTION.	1
2.	OVERALL SYSTEM PLAN	1
	2.1 Phase I Plan	1
	2.2 Phase II Plan.	4
	2.3 Phase III Plan	13
3.	EXPERIMENT INTERFACE CONSIDERATIONS	14
4.	SYSTEMS SOFTWARE.	15
5.	SCHEDULES	16
6.	CONCLUSIONS AND RECOMMENDATIONS	19

Attachments

A	Phase I Cabling Specifications.	A-1
B	Interim 7930 DIO Device Usage Software (Phase I)	B-1
C	Cardiopulminary Exercise Response Test (Phase I)	C-1

1. INTRODUCTION

This document presents the results of a design study performed to establish overall system interface requirements for the Biomedical Laboratories Division's Sigma-3 computer system. Emphasis has been placed upon the definition of an overall implementation plan and associated schedule to meet both near-term and long-range requirements within the constraints at available resources.

2. OVERALL SYSTEM PLAN

The overall system plan calls for implementation of two major and distinct systems: the interface of analog instrumentation signals and the interface of external digital devices and "application" discrete signals with the Direct I/O system of the Sigma-3. The final configuration for these two interface systems, as anticipated, is shown in Figures 1 and 2.

Implementation of the total interface system would be accomplished in three phases containing several subphases.

2.1 PHASE I PLAN

The first phase (Phase I) provides system interface capability to satisfy immediate or near-future experiment/computer linkage requirements. Two subtasks to this phase are:

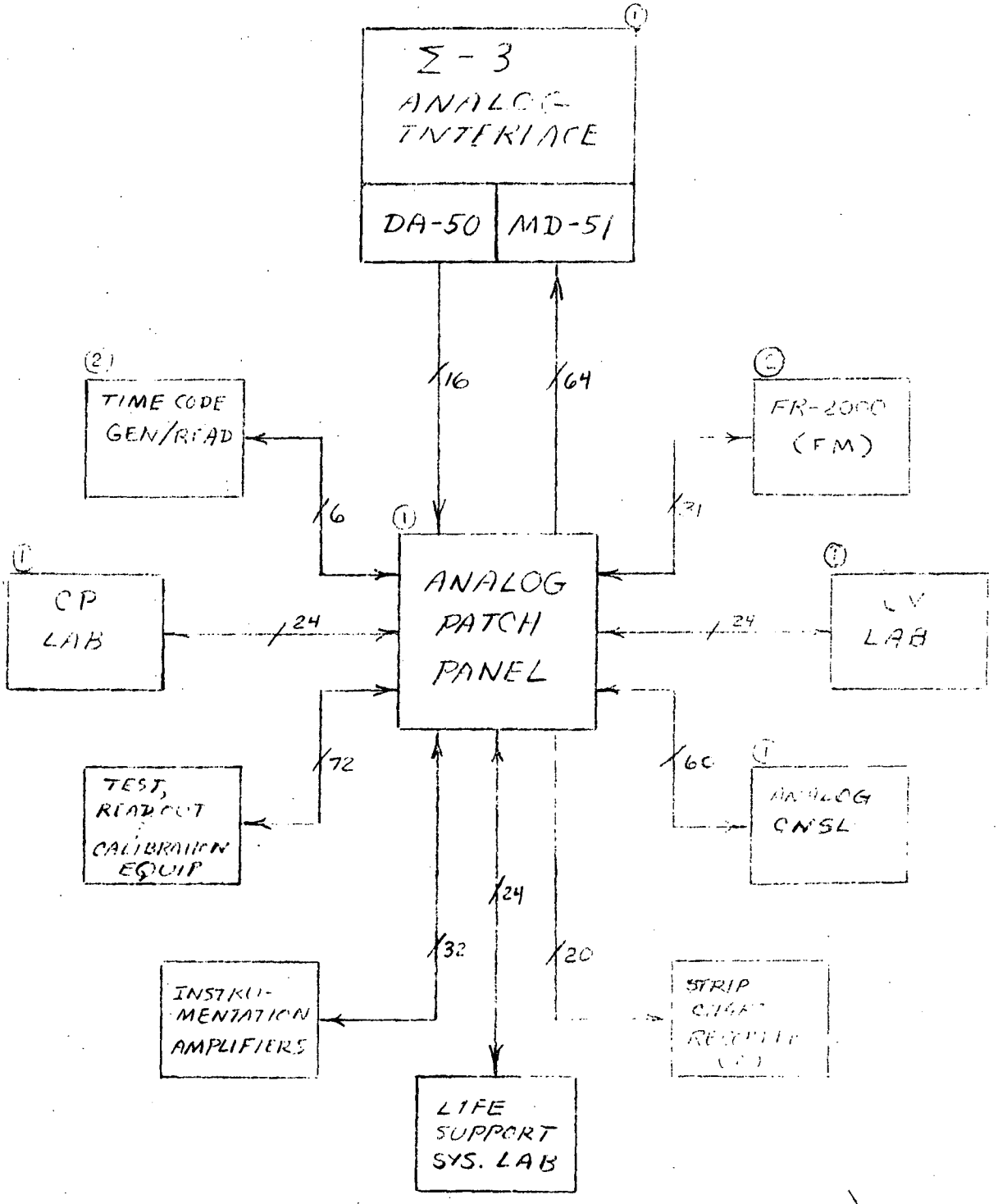
(1) Phase I-A - Establish and provide analog system interfacing.

(2) Phase I-B - Provide interim utilization of the Discrete I/O system.

BY _____ DATE _____

CHKD. BY _____ DATE _____

JOB NO. _____

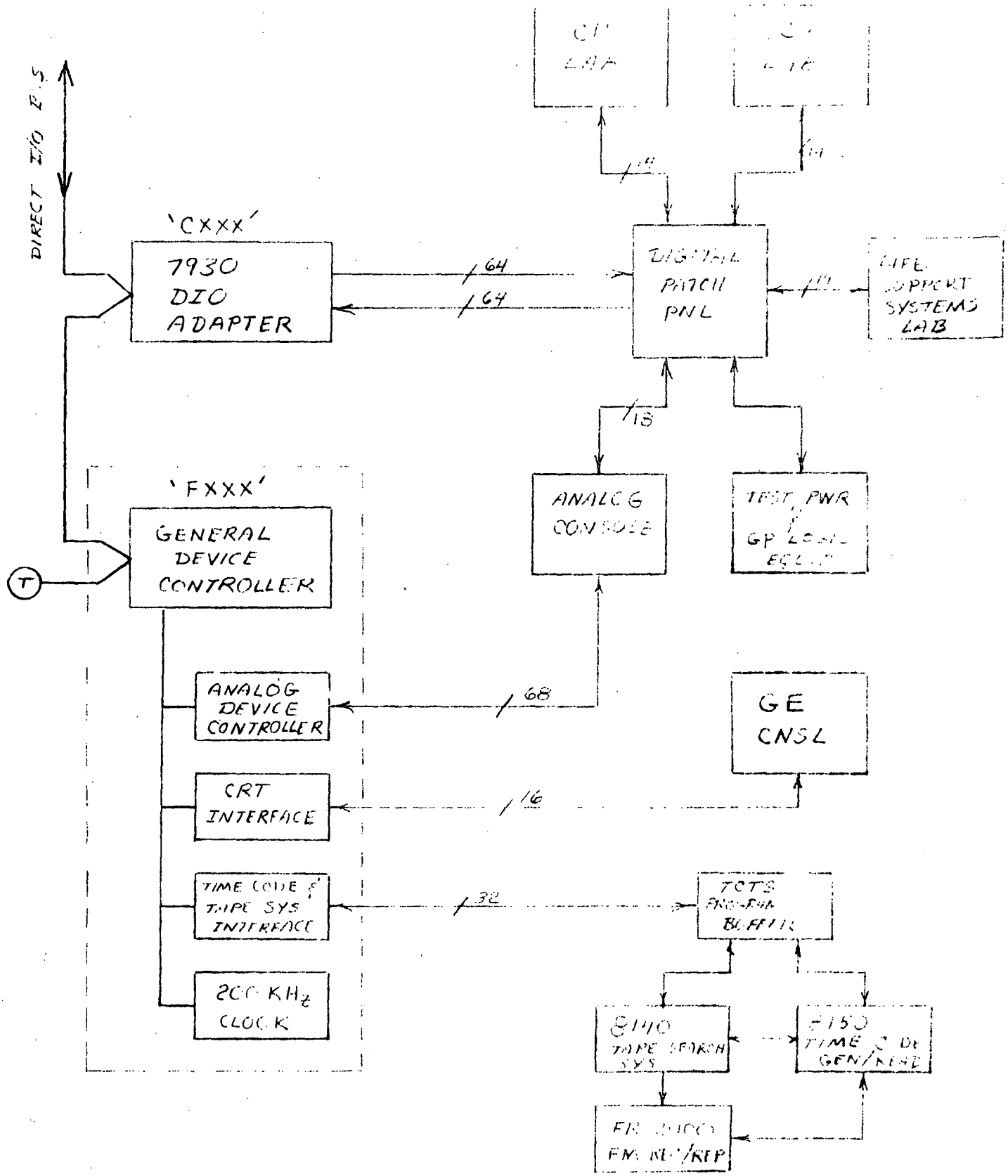


(1) PRIMARILY INSTALLED AND [illegible]

(2) NOT CABLED TO PATCH PANEL
BUT OPERATIONAL

EXPANDED ANALOG INTERFACE SYSTEM CONFIGURATION

Fig. -2



EXPANDED DIO SYSTEM INTERFACE CONFIGURATION

Fig. 3

Phase I-A incorporates the analog patching system shown in Figure 1 and provides central patching access to the following:

- Cardiopulminary Laboratory 24 TNKS
- Cardiovascular Laboratory 24 TNKS
- Sigma-3 analog interface 80 TNKS
- FR-2000 31 TNKS
- Time code generator/reader 6 TNKS
- 680 analog computer 60 TNKS

The remainder of the patchable system would be incorporated in a later phase. Assignment of patching areas on the analog patch panel is shown in Figure 3. Cabling is described in Attachment A.

Phase I-B utilizes the 7930 Digital Input/Output adapter in a hard-wired interim configuration for connecting existing devices. Devices connected to the 7930 DIO system are shown in Figure 4. No patchable discrete I/O is provided in this phase. Cabling specifications are provided in Attachment A. Software information for the Interim DIO configuration is described in Attachment B.

2.2 PHASE II PLAN

The Phase II plan provides expansion of the Direct I/O system on the Sigma-3 for dedicated devices and adds general purpose patchable I/O.

Phase II-A implements the General Device Controller shown in Figure 2. This controller physically consist of two "T" series card chassis utilizing standard XDS logic cards

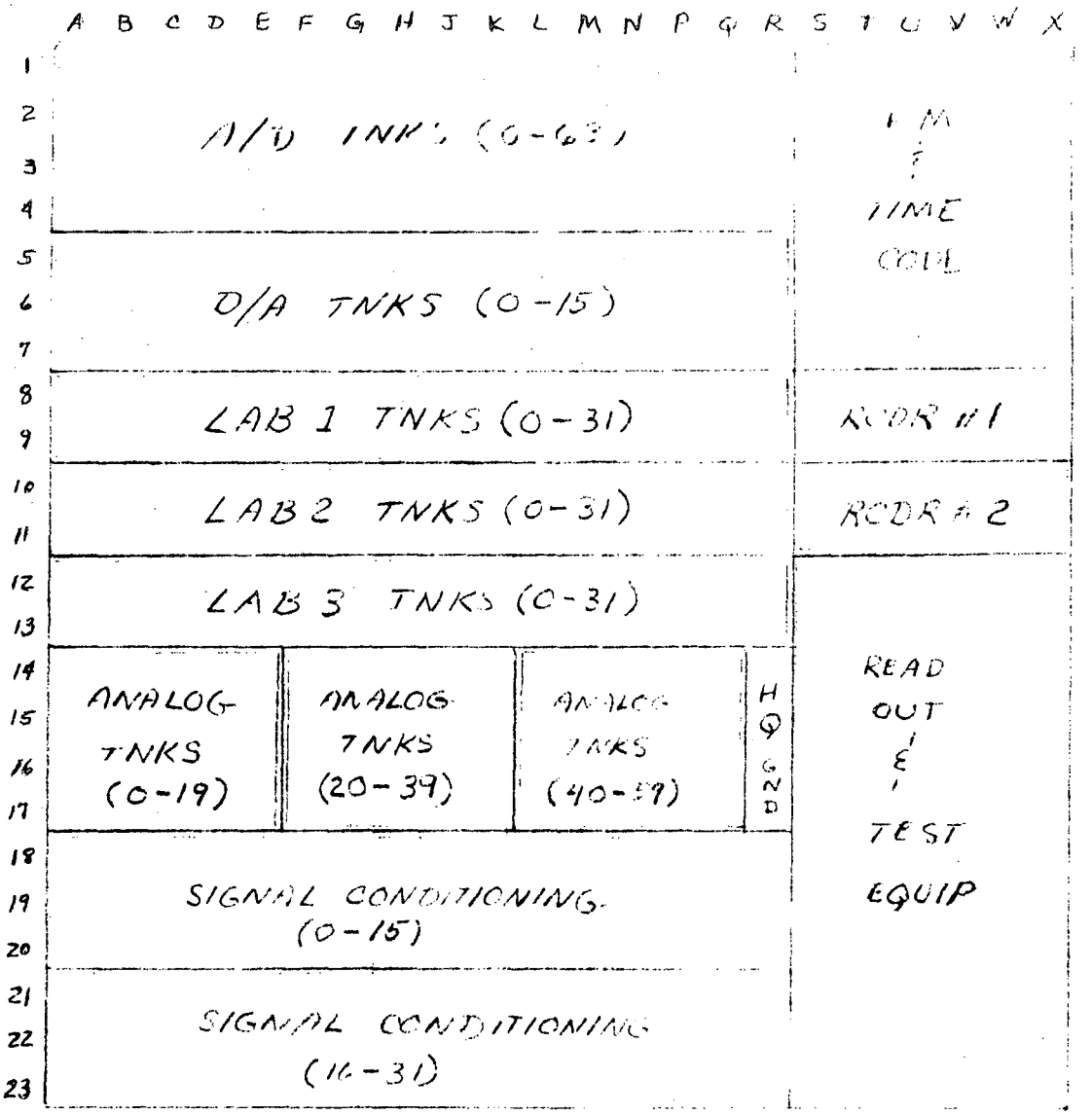
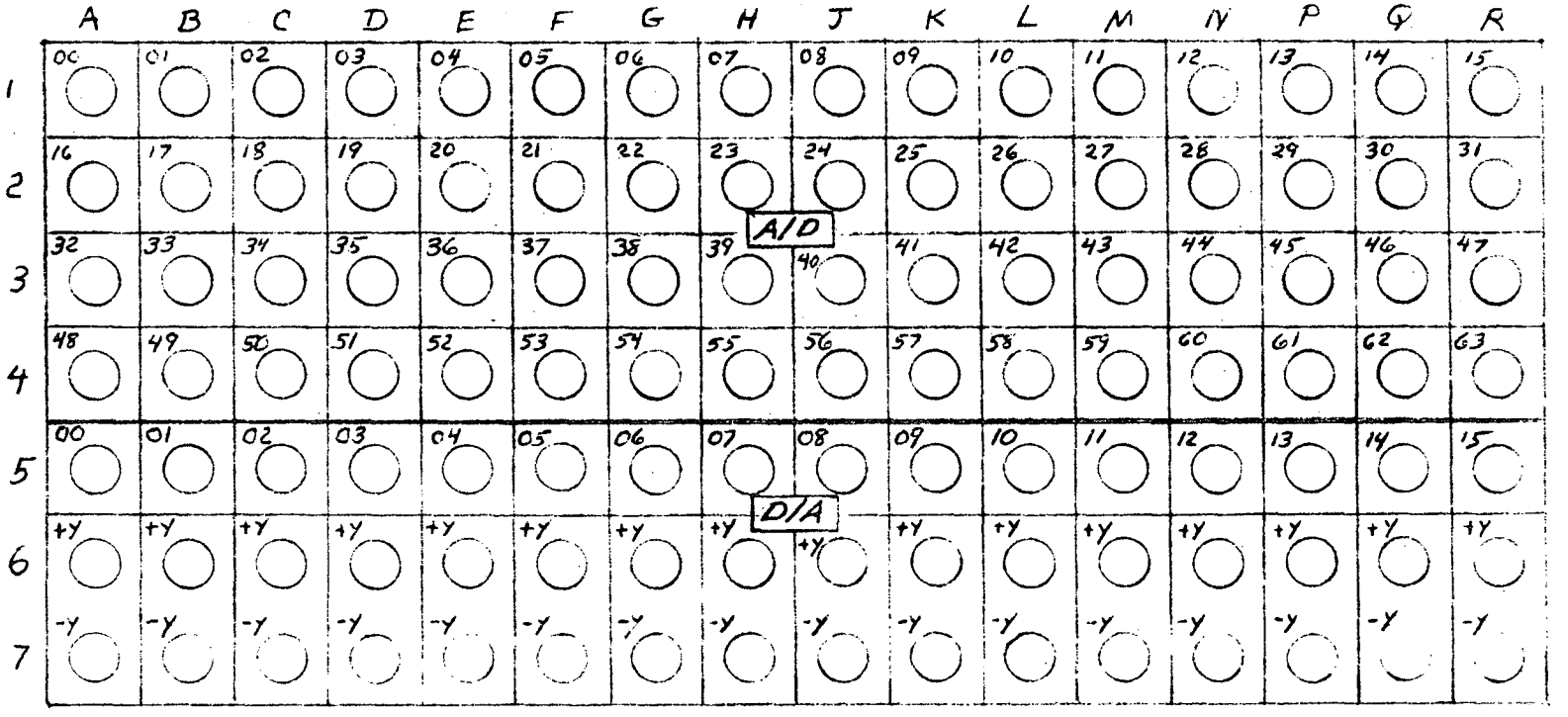


Fig. 3

SIGNAL CONDITIONING ORGANIZATION



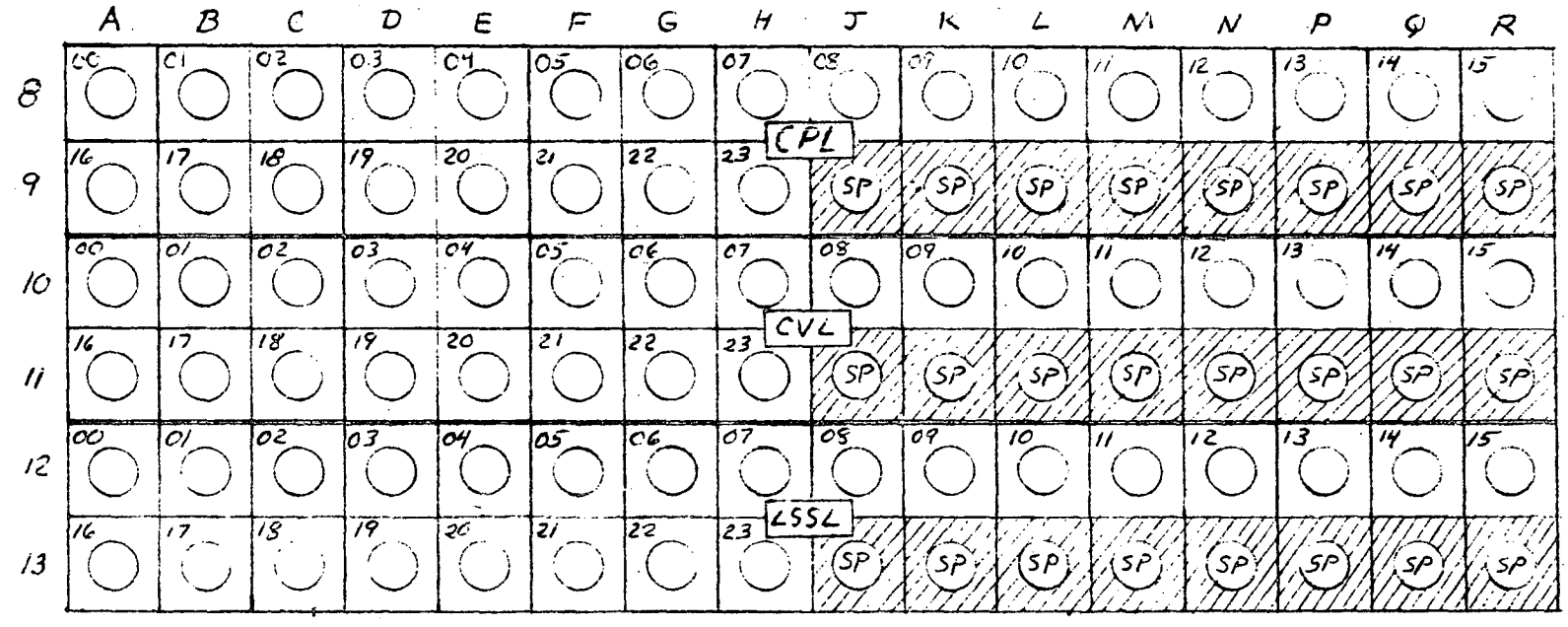
* Numbered holes correspond to respective A/D & D/A channels of Σ-3. Multiplying Twin feature (+Y and -Y) is reserved for future expansion — presently not installed.

Fig. 3-A

Σ-3 ANALOG INTERFACE PATCHING

BY _____ DATE _____ CT _____ SHEET NO. _____

CHKD. BY _____ DATE _____ JOB NO. _____



CPL = CARDIOPULMINARY LABORATORY

CVL = CARDIOVASCULAR "

LSSL = LIFT SUPPORT SYSTEMS "

Fig. 3-B

LABORATORY TRUNK PATCHING

BY _____ DATE _____

CHKD. BY _____ DATE _____

PROJECT _____

JOB NO. _____

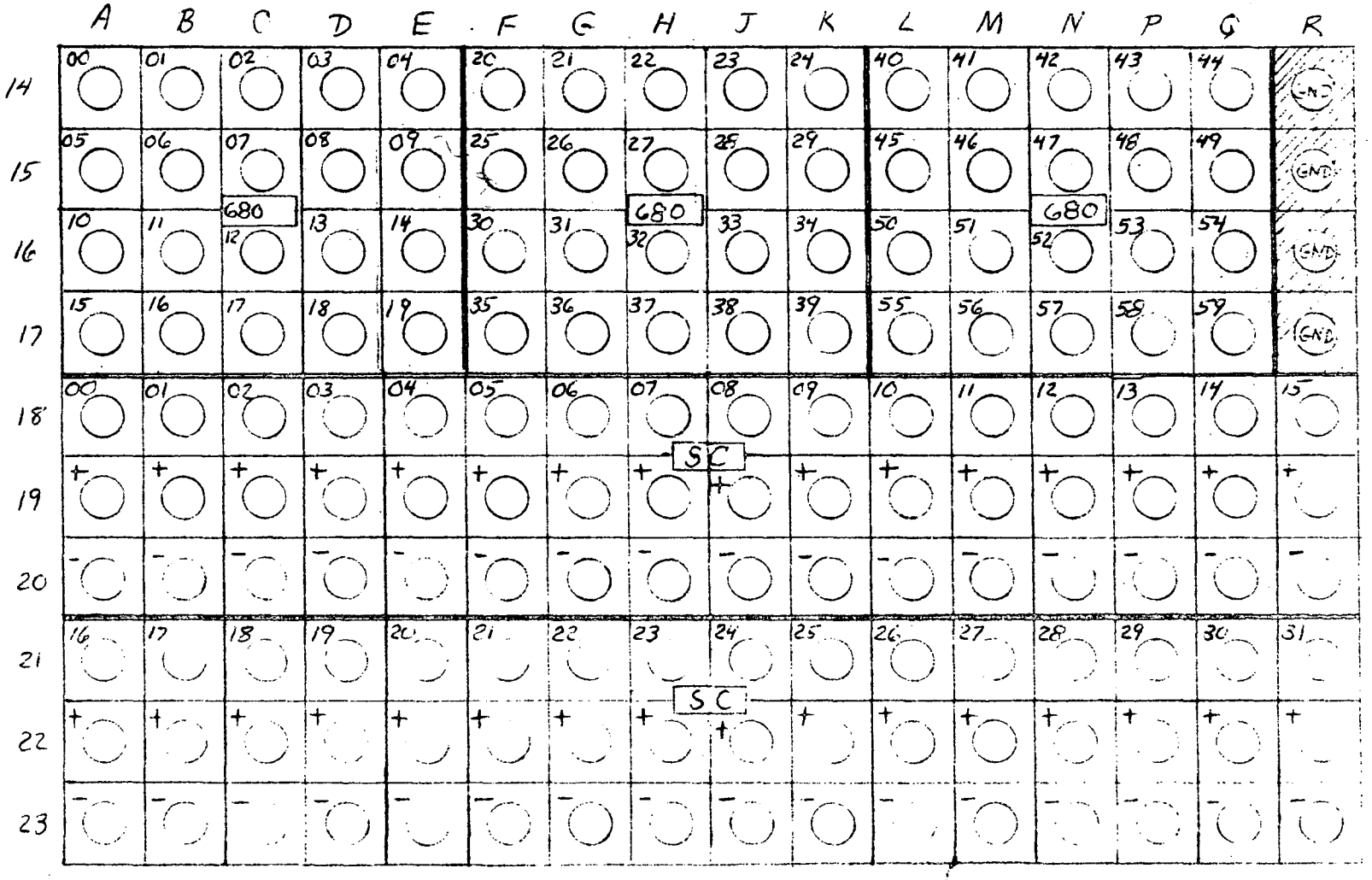


Fig. 3-C

ANALOG TRUNKS & INSTRUMENTATION AMPLIFIER PATCHING

BY _____ DATE _____ CT _____ SHEET NO. _____
CHKD. BY _____ DATE _____ JOB NO. _____

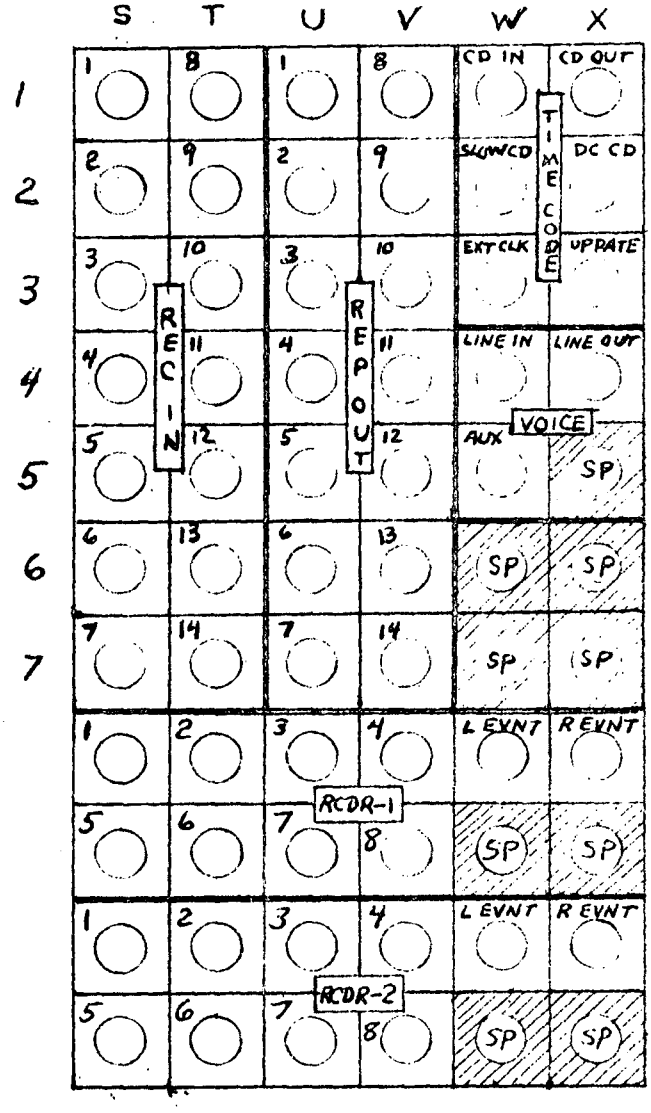
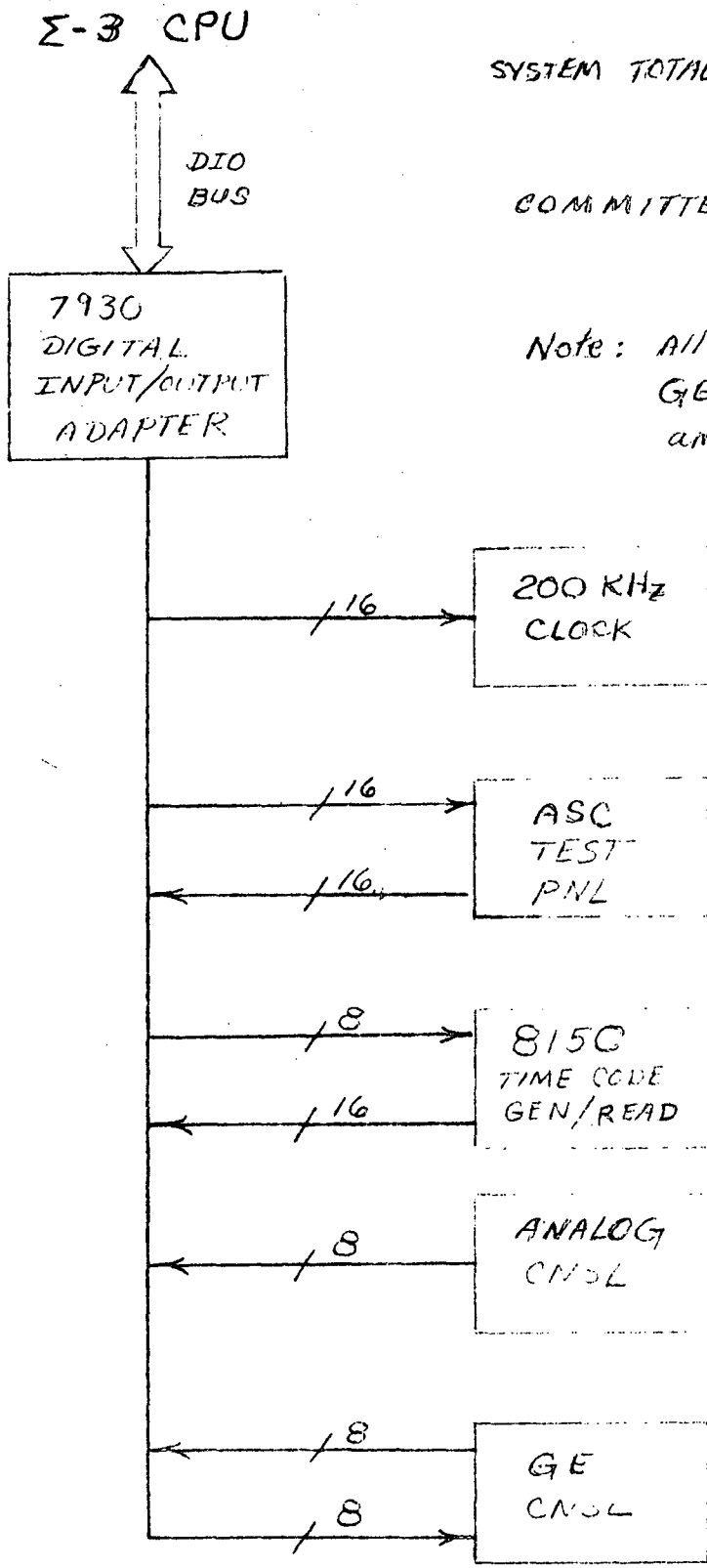


fig. 3-D

FR-2000, TIME CODE GEN./READER & STRIP CHART RECORDER PATCHING



INTERIM 7930 DIO SYSTEM UTILIZATION

fig - 1

and components. It will be located in two spare slots beneath the 7930 DIO in the CPU-2 rack. Functionally this controller will perform or contain the following:

- Interface with the XDS Direct I/O Bus and respond to an effective address of 'FXXX' from WD or RD commands.
- Provide a complete logic and control interface for the 680 analog computer. (analog device controller)
- Provide a data interface to the G. E. Biomedical console.
- Provide an interface for the time code gen./reader tape search system program buffer.
- Contain the 200 KHz clock with expanded modes of operation.

The digital patch panel is installed in phase II-B and incorporates patching for the following:

• 7930 DIO adapter	128 TNKS
• Cardiopulmonary Laboratory	14 TNKS
• Cardiovascular Laboratory	14 TNKS
• 680 Analog Console	18 TNKS

Final expansion of the patchable discrete system will be accomplished in a later phase. Figure 5 shows the proposed layout of the digital patch panel.

In the implementation of Phase II, the 7930 would function as a backup until the General Device Controller is checked out and operational. No significant downtime is anticipated

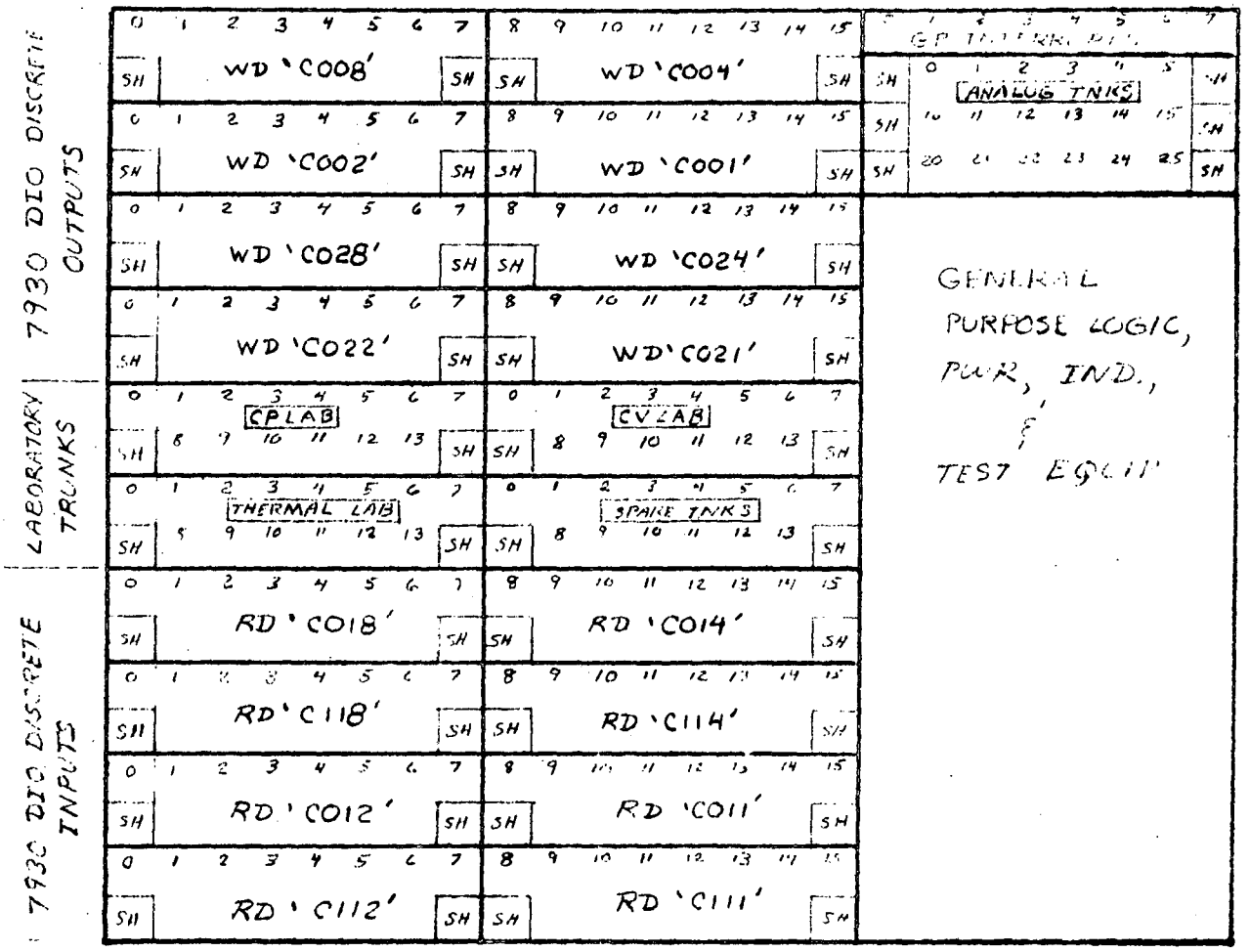


fig. - 5

DIGITAL PATCH PANEL ORGANIZATION

for installation. Software support will be required in checking out the controller.

2.3 PHASE III PLAN

Implementation of the third phase mainly involves expansions to the interface systems established in phases I and II.

Specifically, this phase would involve or add the following:

- Life Support Systems Lab analog and digital trunks.
- Incorporation of test, readout, application, and calibration equipment to the analog patching system.
- Incorporation of test, power, and general-purpose logic equipment to the digital patching system.
- Installation of existing strip chart recorders to the analog patching system.
- Provide the design, fabrication, and installation of an instrumentation amplifier system for direct signal conditioning of laboratory signals.
- Provide the design, fabrication, and installation of the time code/tape search system program buffer.

The last two items represent an in-house design effort. The instrumentation amplifier package is planned for the system to provide immediate signal conditioning of some laboratory signals without utilization of the analog console. Several amplifiers are being examined for this purpose. The design task will chiefly involve packaging design. It should also be noted that the instrumentation amplifier system will provide high common mode noise rejection of laboratory signals while offering high input impedence

that is not easily or conveniently obtained with the 680 analog console.

The second design task in this phase provides a program buffer for the 8150 time code generator/reader and 8140 FM tape search units. This buffer will provide the following under computer control:

- Remote selection of 8150 mode selector, preset, and reset switches.
- Remote selection of 8140 modes and pushbuttons including transport control of the FR-2000 FM recorder.
- Remote programming of start and stop times.
- Remote selection of analog band-pass filters for search and playback speeds.

The buffer will mount as an integral part of the 8140 and 8150 units and will be installed with these units in the FR-2000 rack. Gating and reading time data is accomplished in phase I-B.

Phase III can be accomplished in part during Phases 1 and II implementation; however, the items in the third phase are considered lowest priority. Activities in this phase are presently not scheduled. Design of the instrumentation amplifier package and TCTS buffer will probably begin in the second quarter of 1972.

3. EXPERIMENT INTERFACE CONSIDERATIONS

An examination of present experiment interface requirements for both the Cardiopulmonary and Cardiovascular laboratories

shows that the interface system provided in phase I is adequate. Most of the signals supplied from these labs have adequate buffering. The 680 analog computer would be used for noise rejection and special buffering or signal conditioning before accessing A/D channels on the Sigma-3. The patching system in conjunction with the 680 console provides much flexibility in accomplishing this purpose.

A special requirement for logic control exists for the exercise response test of the cardiopulmonary lab. This requires utilization of the general-purpose programmable logic on the 680 console in conjunction with the 7930 DIO. This application is discussed in detail in Attachment C. In general, the 680 console provides excellent means for supplying convenient programmable logic as the need arises.

4. SYSTEMS SOFTWARE

Systems software encompasses two major areas; namely diagnostic testing/check-out and applications.

Loop test methods are proposed for checking out the 7930 DIO, MD-51 multiplexer/digitizer, and DA-50 digital-to-analog converter. Standard XDS diagnostic software would be utilized for these systems. A patch panel for both analog and digital systems would be hard-wired and dedicated for maintenance purposes. An investigation of setting up and running these programs in conjunction with the facility patching system is recommended.

A check-out software package is desired for checking out periphial devices dedicated to the general device controller. This package should provide ease and simplicity for

executing simple WD and RD instruction with data interfacing and readout under teletype control. Options to provide repeated executions of DIO instructions under selectable clock rates are also desirable. It is envisioned that such a package could be extended for performing diagnostic testing of devices on the DIO. This software should also include interface operations with the 7930 DIO for checking out patched application signals planned in Phase II.

Development of applications systems software for devices on the General Device Controller is no simple task, if full system utilization is sought. The greatest task lies in the development of programs for the 680 analog computer such as setting pots, static checks, etc. Specification of 680 analog console commands are presently being prepared under PCR No. 1 (680 Interface Design). Software programs for utilizing the high frequency clock and time-code/tape-search system is also needed. Software for the biomedical console is currently under development by G. E..

5. SCHEDULES

All activities in Phase I are scheduled for completion by Sept. 27, 1971. All interfaces in Phase I have been installed. Remaining tasks included checkout of the analog patching system and the time code generator/reader computer interface.

A predicted schedule of Phase II operations is shown in Figure 6. The 680 interface design task will consist of a report describing the logic and control interface planned for implementation with the Sigma-3 and proposed General Device Controller. Most of the material in this

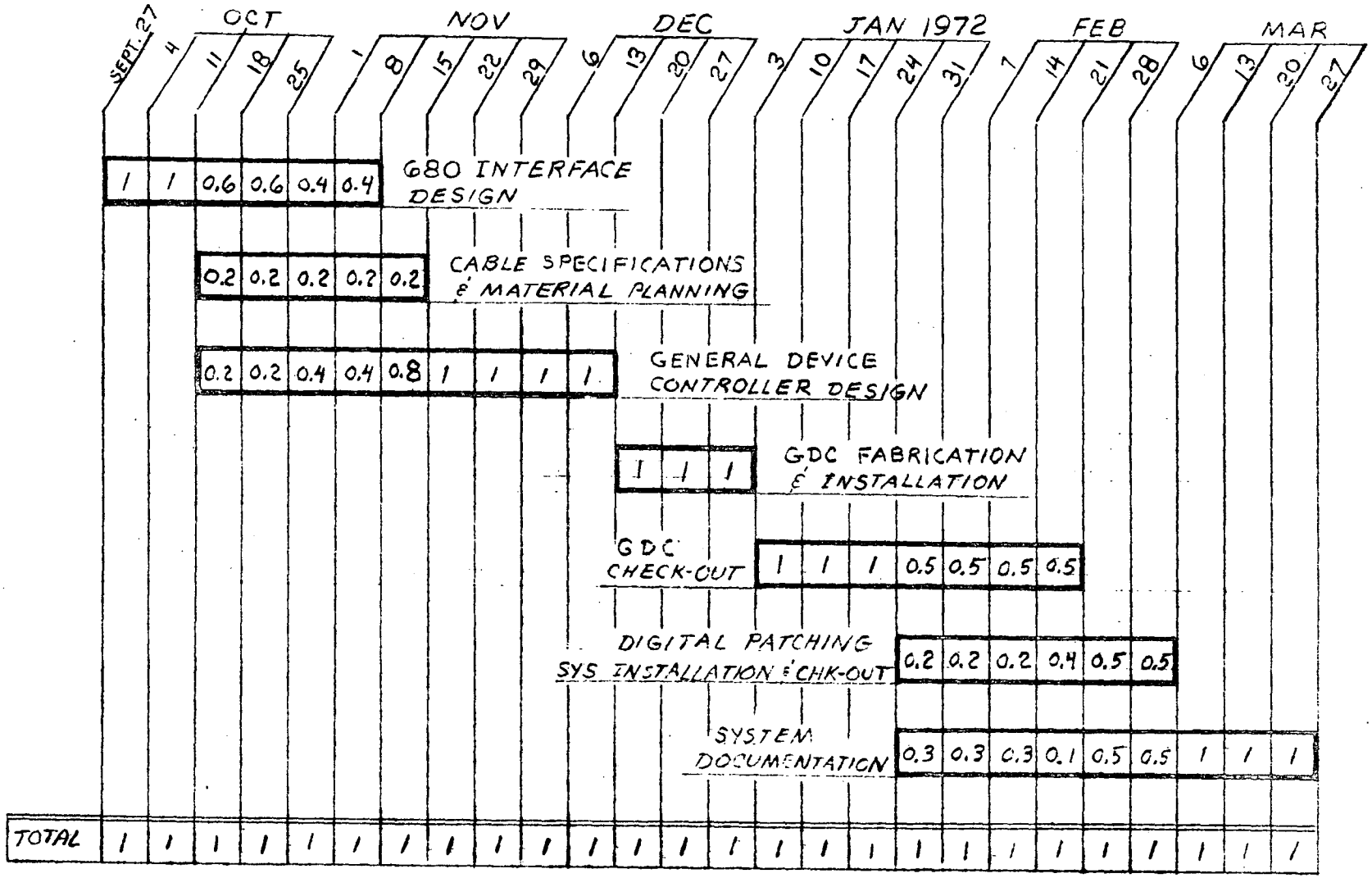


fig - 6

PHASE - II SCHEDULE

report is software in nature in that it will describe the list of 680 I/O commands relevant to Sigma-3 operation.

Cable specifications for the digital patching system and controller are supplied early in Phase II to ensure a timely delivery from Tech Services. Material planning includes the ordering and supplying miscellaneous hardware such as connectors, wire, etc.

The General Device Controller design also includes the detail design of the analog device controller as specified in the 680 interface design report. Fabrication of the controller will require approximately two man-weeks plus one week for installation and preliminary testing. Checkout of the controller will require significant amounts of Sigma-3 machine time. A block of computer time should be scheduled each day for this purpose.

The digital patching system installation would be accomplished as portions of the controller become operational to accept the devices temporarily assigned to the 7930 DIO system.

System documentation will include a detailed description of the General Device Controller as well as software information. The report would be complete to assist maintenance and software personnel. Notes on utilizing the general-purpose patchable DIO signals connected to the 7930 system would also be supplied in the form of application bulletins or memos.

6. CONCLUSIONS AND RECOMMENDATIONS

It is believed that this interface plan reflects the best interest of the branch and principal users of the biomedical computing laboratory. As best as can be determined from examination of laboratory requirements, implementation of the submitted plan will fulfill all foreseeable experiment interface requirements. It is felt that sufficient flexibility exists in the proposed system to satisfy special interfacing tasks as such requirements become known or defined in experiment expansions. It is therefore recommended that this plan be adopted as a scheduled activity; explicity made known and coordinated with the principal personnel involved.

ATTACHMENT A

PHASE I CABLING

SPECIFICATIONS

Phase I – Cabling Specifications

COMMENTS:

System cabling for Phase I is shown in Figure A-1. Detailed terminations of devices on the 7930 DIO system are shown in Figure A-2 with the SIU module assignments.

Table A-I contains a list of abbreviations that will be used for cable identification and labeling,both current and future. Cables would be tagged with two abbreviations and a number signifying with which devices the cable interconnects and the cable number. As an example, a cabled tagged AC/AP-2 would be connected between the 680 analog console and the analog patch panel and represents the third cable in the system (first cable is designated with the number zero).

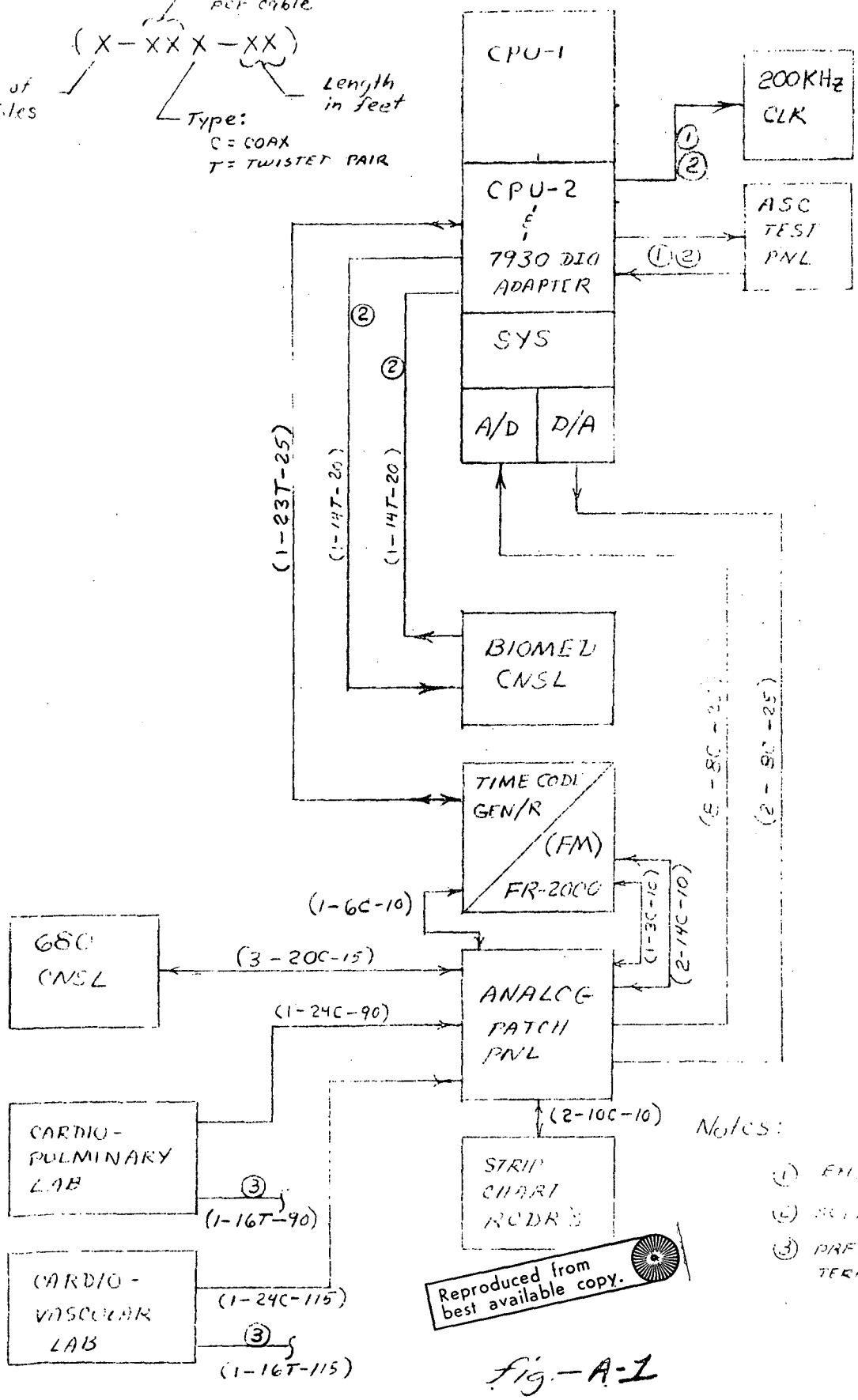
BY _____ DATE _____
CHKD. BY _____ DATE _____

SHEET NO. _____ OF _____
JOB NO. _____

Legend:

(X – XX X – XX)

- X: No. of cables
- XX: No. of conductors per cable
- X: Type: C = COAX, T = TWISTET PAIR
- XX: Length in feet



Notes:

(1) FURNISHED BY VENDOR
(2) INSTALLED BY VENDOR
(3) PRESENTLY NOT TERMINATED

fig. – A-1

PHASE-I
LABORATORY FACILITY CABLING

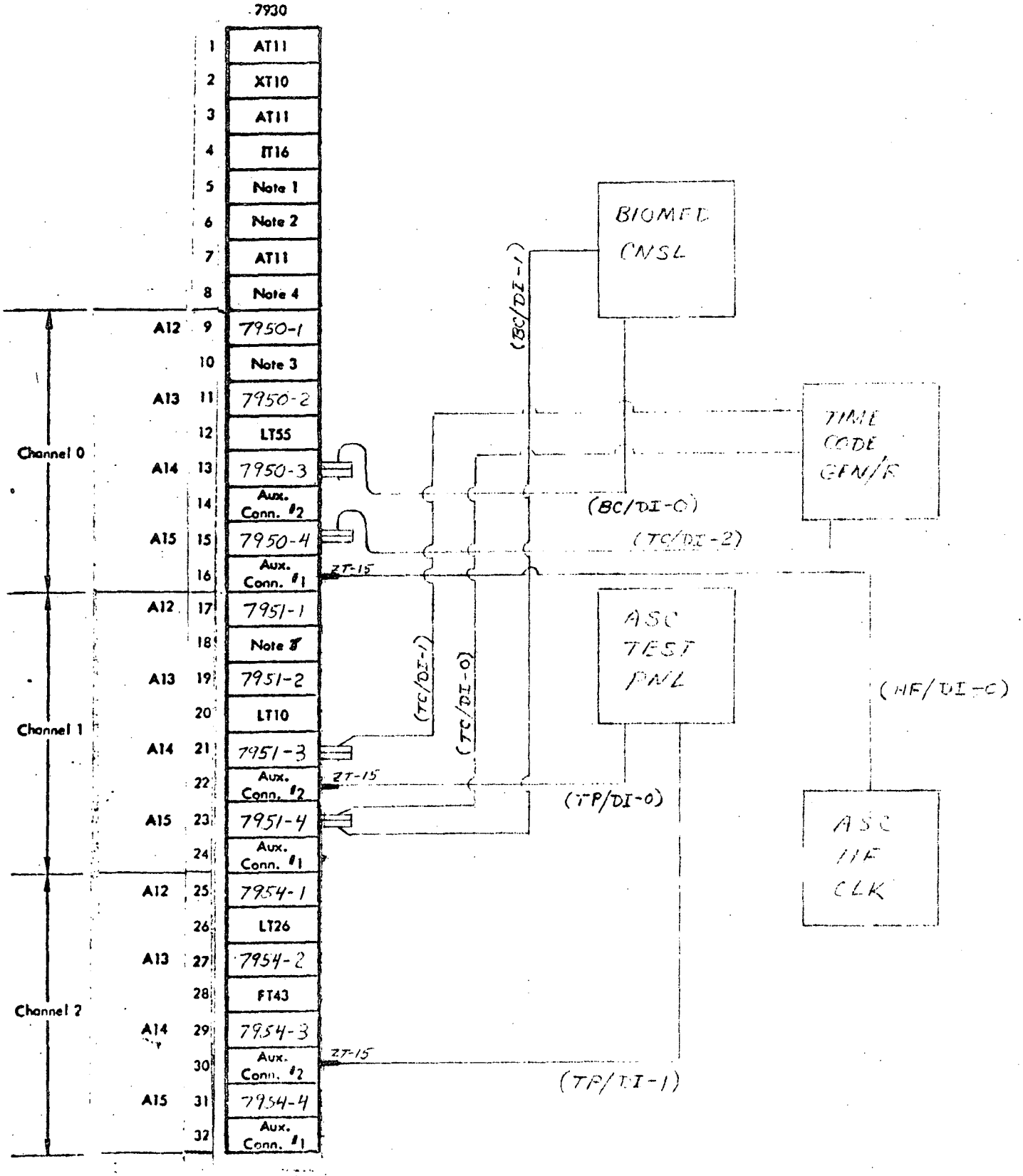


fig-A-2

7930 DIO CABLING ORGANIZATION (PHASE-I)

TABLE A-I.

CABLE IDENTIFICATION LEGEND

TC – Time code generator/reader (8150)

TS – Tape search system (8140) or references time-code/tape-search system in later installations

DA – Digital-to-analog converter (DA-50)

AD – Analog multiplexer and digitizer (MD-51).

CP – Cardiopulmonary Laboratory

CV – Cardiovascular Laboratory

AC – 680 analog console

RC – Strip Chart recorder

AP – Analog patch panel

DP – Digital patch panel

LS – Life Support Systems Laboratory

BC – Biomedical Console

FM – Ampex FR-2000 FM recorder/reproducer.

DI – XDS 7930 Discrete Input/Output system.

HF – 200 K Hz High frequency clock.

TP – Test panel (ASC test panel)

CABLE SHEET

BY RLP DATE 6-25-71
CHKD. BY ____ DATE ____

SHEET NO. 1 OF 4
JOB NO. ____

SYSTEM: A/D CONV. - MUX (MD-51) INPUT

CABLE ID: AD/AP-0,1,2,3,4,5,6,7 LENGTH: 25 feet

TOTAL CABLES: 8 NO. OF COND. PER CABLE: 8

WIRE: RG-174/U CONNECTORS: ET-11(16)
COAX TERM. (64)
(ANALOG PATCH PNL)

WIRE LIST:

AD/AP-0

CONNECTOR PIN NO.		SIGNAL
ET-11	PATCH PNL	
A	1-A	AD00
SS		SH
B	1-B	AD01
RR		SH
C	1-C	AD02
PP		SH
F	1-D	AD03
LL		SH
K	1-E	AD04
GG		SH
N	1-F	AD05
DD		SH
P	1-G	AD06
CC		SH
R	1-H	AD07
BB		SH

AD/AP-1

CONNECTOR PIN NO.		SIGNAL
ET-11	PATCH PNL	
A	1-J	AD08
SS		SH
B	1-K	AD09
RR		SH
C	1-L	AD10
PP		SH
F	1-M	AD11
LL		SH
K	1-N	AD12
GG		SH
N	1-P	AD13
DD		SH
P	1-Q	AD14
CC		SH
R	1-R	AD15
BB		SH

RMKS:

CABLE SHEET

BY _____ DATE _____
CHKD. BY _____ DATE _____

SHEET NO. 2 OF 4
JOB NO. _____

SYSTEM: AD CONV./MUX. (cont.)

CABLE ID: AD/AP-2,3 LENGTH: _____

TOTAL CABLES: _____ NO. OF COND. PER CABLE: _____

WIRE: _____ CONNECTORS: _____

WIRE LIST:

AD/AP-2			AD/AP-3		
CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
ET-11	PATCH PNL		ET-11	PATCH PNL	
A	2-A	AD16	A	2-J	AD24
SS		SH	SS		SH
B	2-B	AD17	B	2-K	AD25
RR		SH	RR		SH
C	2-C	AD18	C	2-L	AD26
PP		SH	PP		SH
F	2-D	AD19	F	2-M	AD27
LL		SH	LL		SH
K	2-E	AD20	K	2-N	AD28
GG		SH	GG		SH
N	2-F	AD21	N	2-P	AD29
DD		SH	DD		SH
P	2-G	AD22	P	2-9	AD30
CC		SH	CC		SH
R	2-H	AD23	R	2-R	AD31
BB		SH	BB		SH

RMKS:

CABLE SHEET

BY _____ DATE _____ SHEET NO. 3 OF 4

CHKD. BY _____ DATE _____ JOB NO. _____

SYSTEM: AD CONV./MUX. (cont.)

CABLE ID: AD/AP-4,5 LENGTH: _____

TOTAL CABLES: _____ NO. OF COND. PER CABLE: _____

WIRE: _____ CONNECTORS: _____

WIRE LIST:

AD/AP-4			AD/AP-5		
CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
ET-11	PATCH PNL.		ET-11	PATCH PNL.	
A	3-A	AD32	A	3-J	AD40
SS		SH	SS		SH
B	3-B	AD33	B	3-K	AD41
RR		SH	RR		SH
C	3-C	AD34	C	3-L	AD42
PP		SH	PP		SH
F	3-D	AD35	F	3-M	AD43
LL		SH	LL		SH
K	3-E	AD36	K	3-N	AD44
GG		SH	GG		SH
N	3-F	AD37	N	3-P	AD45
DD		SH	DD		SH
P	3-G	AD38	P	3-Q	AD46
CC		SH	CC		SH
R	3-H	AD39	R	3-R	AD47
BB		SH	BB		SH

RMKS:

CABLE SHEET

BY _____ DATE _____
CHKD. BY _____ DATE _____

SHEET NO. 4 OF 4
JOB NO. _____

SYSTEM: AD CONV./MUX. (Cont.)

CABLE ID: AD/AP-6, 7 LENGTH: _____

TOTAL CABLES: _____ NO. OF COND. PER CABLE: _____

WIRE: _____ CONNECTORS: _____

WIRE LIST:

AD/AP-6			AD/AP-7		
CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
ET-11	PATCH PNL		ET-11	PATCH PNL	
A	4-A	AD48	A	4-J	AD56
SS		SH	SS		SH
B	4-B	AD49	B	4-K	AD57
RR		SH	RR		SH
C	4-C	AD50	C	4-L	AD58
PP		SH	PP		SH
F	4-D	AD51	F	4-M	AD59
LL		SH	LL		SH
K	4-E	AD52	K	4-N	AD60
GG		SH	GG		SH
N	4-F	AD53	N	4-P	AD61
DD		SH	DD		SH
P	4-G	AD54	P	4-Q	AD62
CC		SH	CC		SH
R	4-H	AD55	R	4-R	AD63
BB		SH	BB		SH

RMKS:

CABLE SHEET

BY RRR DATE 6-25-71
CHKD. BY ____ DATE ____

SHEET NO. 1 OF 1
JOB NO. ____

SYSTEM: D/A CONVERTER (DA-50) OUTPUT

CABLE ID: DA/AP-0, 1 LENGTH: 8' ±

TOTAL CABLES: 2 NO. OF COND. PER CABLE: 8

WIRE: RG-174/U CONNECTORS: ET-11 & COAX TERM. 16 (ANALOG PATCH PANEL)

WIRE LIST:

DA/AP-0			DA/AP-1		
CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
ET-11	PATCH PNL		ET-11	PATCH PNL	
1	5-A	DA00	A	5-J	DA08
15		SH	SS		SH
2	5-B	DA01	B	5-K	DA09
16		SH	RR		SH
3	5-C	DA02	C	5-L	DA10
17		SH	PP		SH
6	5-D	DA03	F	5-M	DA11
20		SH	LL		SH
9	5-E	DA04	K	5-N	DA12
23		SH	GG		SH
12	5-F	DA05	N	5-P	DA13
26		SH	DD		SH
13	5-G	DA06	P	5-Q	DA14
27		SH	CC		SH
14	5-H	DA07	R	5-R	DA15
28		SH	BB		SH

RMKS:

CABLE SHEET

BY BWP DATE 6-25-71 SHEET NO. 1 OF 3

CHKD. BY ____ DATE ____ JOB NO. ____

SYSTEM: Analog Trunks

CABLE ID: AC/AP-0, 1, 2 LENGTH: 15 feet

TOTAL CABLES: 3 NO. OF COND. PER CABLE: 20

WIRE: RG-174/U CONNECTORS: ① AMP/EAI CONN. MOD.C COAX TERMI. (60) (ANALOG PATCH PANEL)

WIRE LIST: ②

AC/AP-0

CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
AMP	PATCH PNL		AMP	PATCH PNL	
1-A	14-A	T00	2-A	16-A	T10
1-F		SH	2-F		SH
1-B	14-B	T01	2-B	16-B	T11
1-G		SH	2-G		SH
1-H	14-C	T02	2-H	16-C	T12
1-C		SH	2-C		SH
1-J	14-D	T03	2-J	16-D	T13
1-D		SH	2-D		SH
1-K	14-E	T04	2-K	16-E	T14
1-E		SH	2-E		SH
1-N	15-A	T05	2-N	17-A	T15
1-U		SH	2-U		SH
1-P	15-B	T06	2-P	17-B	T16
1-V		SH	2-V		SH
1-R	15-C	T07	2-R	17-C	T17
1-W		SH	2-W		SH
1-X	15-D	T08	2-X	17-D	T18
1-S		SH	2-S		SH
1-Y	15-E	T09	2-Y	17-E	T19
1-T		SH	2-T		SH

RMKS:

① EAI PART NO. 00 542:1243-0 OR AMP EQUIV.

② SEE EAI DWG. NO. C00-019-0972-0A FOR CONNECTOR SHELL DETAILS.

CABLE SHEET

BY _____ DATE _____
CHKD. BY _____ DATE _____

SHEET NO. 2 OF 3
JOB NO. _____

SYSTEM: Analog Trunks (Cont.)
CABLE ID: AC/AP-1 LENGTH: _____
TOTAL CABLES: _____ NO. OF COND. PER CABLE: _____
WIRE: _____ CONNECTORS: _____

WIRE LIST:

AC/AP-1

CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
AMP	PATCH PNL		AMP	PATCH PNL	
1-A	14-F	T20	2-A	16-F	T30
1-F		SH	2-F		SH
1-B	14-G	T21	2-B	16-G	T31
1-G		SH	2-G		SH
1-H	14-H	T22	2-H	16-H	T32
1-C		SH	2-C		SH
1-J	14-J	T23	2-J	16-J	T33
1-D		SH	2-D		SH
1-K	14-K	T24	2-K	16-K	T34
1-E		SH	2-E		SH
1-N	15-F	T25	2-N	17-F	T35
1-U		SH	2-U		SH
1-P	15-G	T26	2-P	17-G	T36
1-V		SH	2-V		SH
1-R	15-H	T27	2-R	17-H	T37
1-W		SH	2-W		SH
1-X	15-J	T28	2-X	17-J	T38
1-S		SH	2-S		SH
1-Y	15-K	T29	2-Y	17-K	T39
1-T		SH	2-T		SH

RMKS:

CABLE SHEET

BY _____ DATE _____
CHKD. BY _____ DATE _____

SHEET NO. 3 OF 3
JOB NO. _____

SYSTEM: Analog Trunks (cont.)

CABLE ID: AC/AP-2 LENGTH: _____

TOTAL CABLES: _____ NO. OF COND. PER CABLE: _____

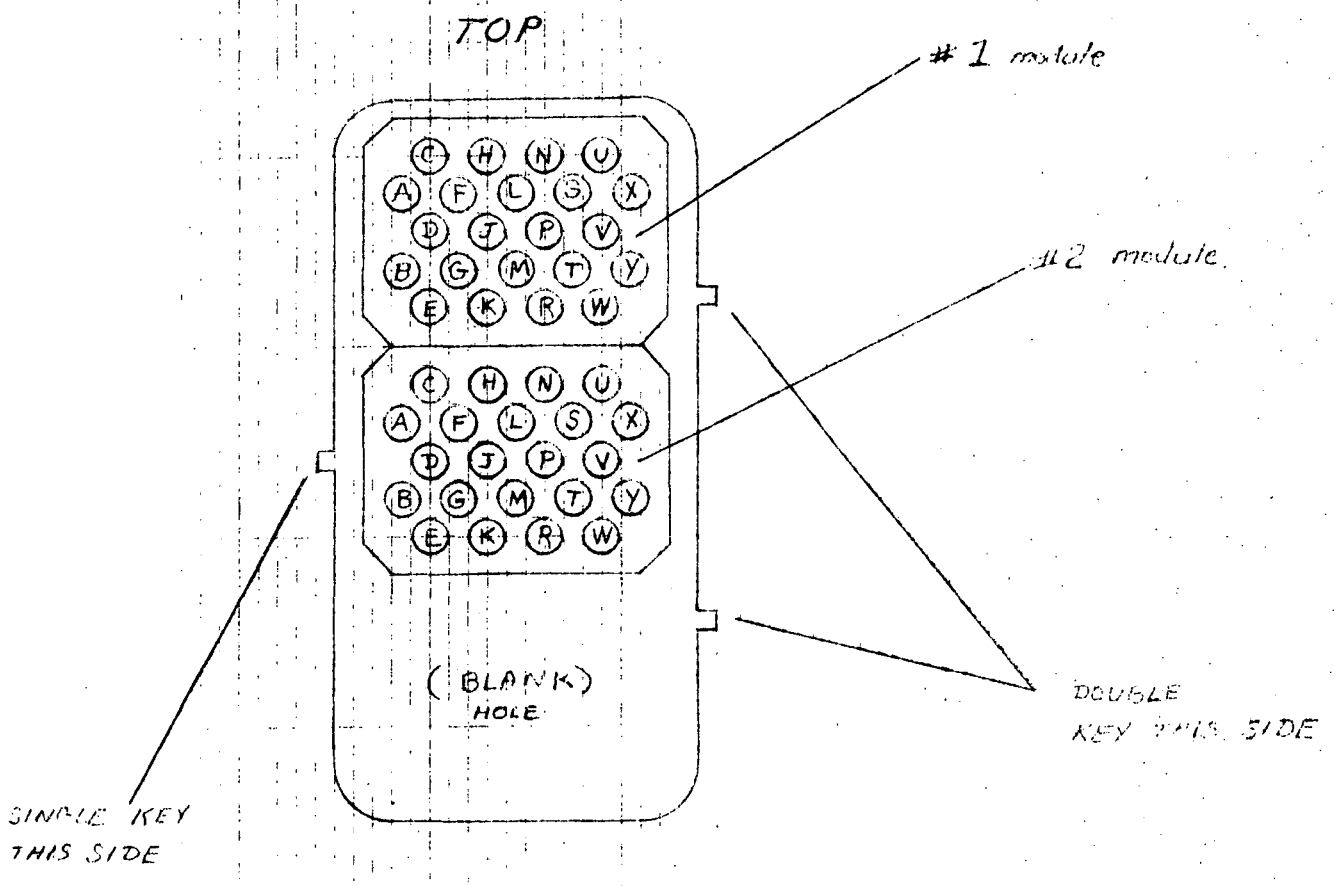
WIRE: _____ CONNECTORS: _____

WIRE LIST:

AC/AP-2

CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
AMP	PATCH PNL		AMP	PATCH PNL	
1-A	14-L	T40	2-A	16-L	T50
1-F		SH	2-F		SH
1-B	14-M	T41	2-B	16-M	T51
1-G		SH	2-G		SH
1-H	14-N	T42	2-H	16-N	T52
1-C		SH	2-C		SH
1-J	14-P	T43	2-J	16-P	T53
1-D		SH	2-D		SH
1-K	14-Q	T44	2-K	16-Q	T54
1-E		SH	2-E		SH
1-N	15-L	T45	2-N	17-L	T55
1-U		SH	2-U		SH
1-P	15-M	T46	2-P	17-M	T56
1-V		SH	2-V		SH
1-R	15-N	T47	2-R	17-N	T57
1-W		SH	2-W		SH
1-X	15-P	T48	2-X	17-P	T58
1-S		SH	2-S		SH
1-Y	15-Q	T49	2-Y	17-Q	T59
1-T		SH	2-T		SH

RMKS:



REAR OR CABLE-SIDE VIEW OF CONNECTOR

ANALOG TRUNK CABLE CONNECTOR ASSEMBLY

CABLE SHEET

BY BVP DATE 6-25-71
CHKD. BY ____ DATE ____

SHEET NO. 1 OF 1
JOB NO. ____

SYSTEM: ① CARDIOPULMINARY LAB TRUNKS (ANALOG)
CABLE ID: CP/AP-O
LENGTH: 90 feet
TOTAL CABLES: 1
NO. OF COND. PER CABLE: 24
WIRE: RG 174/U
CONNECTORS: BNC (24)
COAX TERM. (24)
(ANALOG PATCH PANEL)

WIRE LIST:

CP/AP-O

CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
BNC LBL	PATCH PNL		BNC LABEL	PATCH PNL	
0	8-A	T00	12	8-N	T12
1	8-B	T01	13	8-P	T13
2	8-C	T02	14	8-Q	T14
3	8-D	T03	15	8-R	T15
4	8-E	T04	16	9-A	T16
5	8-F	T05	17	9-B	T17
6	8-G	T06	18	9-C	T18
7	8-H	T07	19	9-D	T19
8	8-J	T08	20	9-E	T20
9	8-K	T09	21	9-F	T21
10	8-L	T10	22	9-G	T22
11	8-M	T11	23	9-H	T23

RMKS:

① EXISTING CABLE TO BE MADE TO ANALOG PATCH PANEL

CABLE SHEET

BY BWP DATE 6-25-71 SHEET NO. 1 OF 1

CHKD. BY ____ DATE ____ JOB NO. ____

SYSTEM: ① CARDIOVASCULAR LAB TRUNKS (ANALOG)

CABLE ID: CV/AP-0 LENGTH: 115 feet

TOTAL CABLES: 1 NO. OF COND. PER CABLE: 24

WIRE: RG 174/U CONNECTORS: COAX TERM (24)

COAX TERM ANALOG PATCH PANEL (24)

WIRE LIST:

CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
CABLE (LAB)	PATCH PANEL		CABLE (LAB)	PATCH PANEL	
0	10-A	T00	12	10-N	T12
1	10-B	T01	13	10-P	T13
2	10-C	T02	14	10-Q	T14
3	10-D	T03	15	10-R	T15
4	10-E	T04	16	11-A	T16
5	10-F	T05	17	11-B	T17
6	10-G	T06	18	11-C	T18
7	10-H	T07	19	11-D	T19
8	10-J	T08	20	11-E	T20
9	10-K	T09	21	11-F	T21
10	10-L	T10	22	11-G	T22
11	10-M	T11	23	11-H	T23

RMKS:

① EXISTING CABLE TO BE MADE TO ANALOG PATCH PANEL AND LABORATORY SITE.

CABLE SHEET

BY BJR DATE 7-15-71 SHEET NO. 1 OF 3

CHKD. BY ____ DATE ____ JOB NO. ____

SYSTEM: TIME CODE GEN/READER INTERFACE

CABLE ID: TC/DI-0,1,2 LENGTH: 25 feet

TOTAL CABLES: 3 IN 1 NO. OF COND. PER CABLE: 23 (TOTAL)

WIRE: 120 Ω TWISTED PAIR CONNECTORS: AMPHENOL #57-30500 (1)
ET-11 (3)

WIRE LIST:

	TC/DI-0			TC/DI-1		
①	CONNECTOR PIN NO. AMPHENOL	CONNECTOR PIN NO. ET-11/0	SIGNAL	CONNECTOR PIN NO. AMPHENOL	CONNECTOR PIN NO. ET-11/1	SIGNAL
	1	8	DI5	9	8	DO7
		22	SH		22	SH
	2	7	DI4	10	7	DO6
		21	SH		21	SH
	3	6	DI3	11	6	DO5
		20	SH		20	SH
	4	5	DI2	12	5	DO4
		19	SH		19	SH
	5	4	DI1	44	12	DATA RDY (READ INH)
		18	SH			
	6	3	DI0			
		17	SH		26	SH
	7	2	DO9			
		16	SH			
	8	1	DO8			
		15	SH			

RMKS: ① TERMINATE ALL SHIELDS ON AMPHENOL CONNECTOR END TO PINS 48 & 49.

CABLE SHEET

BY _____ DATE _____ SHEET NO. 2 OF 2

CHKD. BY _____ DATE _____ JOB NO. _____

SYSTEM: TIME CODE GEN/READER INTERFACE

CABLE ID: TC/DI-2 LENGTH: _____

TOTAL CABLES: _____ NO. OF COND. PER CABLE: _____

WIRE: _____ CONNECTORS: _____

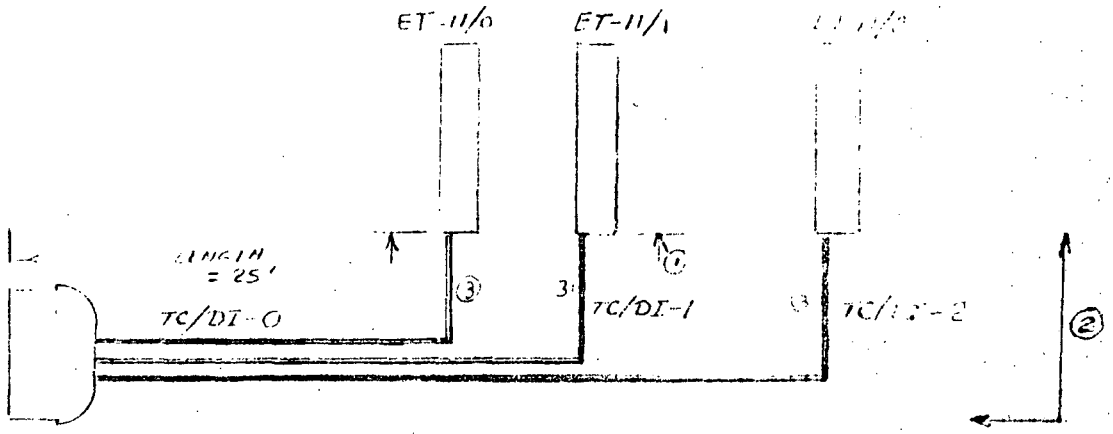
WIRE LIST:

TC/DI-2

CONNECTOR PIN NO.		SIGNAL	CONNECTOR PIN NO.		SIGNAL
AMPHENOL	ET-11/2				
——	1	SPARE			
	15	SH			
——	2	SPARE			
	16	SH			
43	3	DI0	HOLD	COMMAND	
	17	SH			
32	4	DI1	DAYS	GATE	
	18	SH			
33	5	DI2	HOURS	GATE	
	19	SH			
34	6	DI3	MINUTES	GATE	
	20	SH			
35	7	DI4	SECONDS	GATE	
	21	SH			
36	8	DI5	MILLI-SEC	GATE	
	22	SH			
45	10	OUT CLMP			
	24	SH			
46	11	OUT CLMP			
	25	SH			

RMKS:

CHKD. BY ____ DATE ____ / READER INTERFACE CABLE JOB NO. ____



① LENGTH = 25 feet + 1.0 inches

② LENGTH = 25 feet + 4.0 inches

③ Allow 1½ inches of free cable from base at connector before starting cable jacket.

BY AWH DATE 6-25-11

CHKD. BY ____ DATE ____

SHEET NO. ____ OF ____

JOB NO. ____

SYSTEM: BIOMEDICAL CONSOLE

CABLE I.D: BC/DI-0,1 LENGTH: 20 ft or as required by GE

TOTAL CABLES: 2 NO. OF COND. PER CABLE: 14

WIRE: 120 Ω Twisted Pair CONNECTORS: ET-11 (2)

GE

WIRE LIST:

BC/DI-0			BC/DI-1		
CONNECTOR PIN NO. ET-11		SIGNAL	CONNECTOR PIN NO. ET-11		SIGNAL
1		DA 00 (MSB)	A		DA08
2		DA 01	B		DA09
3		DA 02	C		DA10
4		DA03	D		DA11
5		DA04	E		DA12
6		DA05	F		DA13
7		DA06	G		DA14
8		DA07(LSB)	H		DA15
9		UNUSED	K		Unused
10		Output Clamp	L		Output Clamp
11		" "	M		Unused
12		Ready Input	N		Ready Input
13		UNUSED	P		Unused
14		Data Update Stb.	R		Strobe
SHIELDS		DC COMMON	SHIELDS		DC COMMON
(OUTPUT)			(INPUT)		

RMKS: Cable to be supplied by General Electric

ATTACHMENT B

INTERIM 7930 DIO DEVICE

USAGE SOFTWARE

(PHASE I)

DIO EXTERNAL DEVICE USAGE

GENERAL

This section contains software and user information regarding the external devices connected to the DIO. These devices presently consist of the ASC test panel, high frequency clock, biomedical console, and the time code generator/ reader.

These devices will be "hard-wired" to the 7930 Digital Input/Output Adapter but will be incorporated in a device controller at a later date. User documentation for this system will be disclosed upon the establishment of the proposed device controller design. The information contained in this section should therefore be regarded as interim information.

DIO INSTRUCTION SET

Table B-I contains a list of all instructions that are relevent to the external devices connected to the 7930 DIO adapter.

HIGH FREQUENCY CLOCK

This clock supplied by Automated Systems Corporation is presently being configured for 200 KHz operation. The clock is loaded with a 16 bit binary count and upon completion of the load, the clock commences to count down toward zero. On the count of zero, an interrupt is generated. Detailed information on this clock is supplied by ASC.

ASC TEST PANEL

The ASC test panel will eventually be replaced with loop testing methods for checking DIO-SIU operation. This test panel is however convenient and readily available for supplying function switch and indicator flag communication to and from the Sigma-3, respectively.

For function switch operation, the "SINGLE" – "MULT" switch must be in the SINGLE position. The "RDY" toggle switch associated with each group of eight switches normally should be "ON". This "RDY" switch can be used as a ninth switch however. In this mode of operation, condition code CC4 in the Sigma-3 is true when the "RDY" switch is off and vice versa.

TABLE B-I

DIO EXTERNAL
DEVICE INSTRUCTIONS

DEVICE	INSTR.	ADDR.	
CLOCK	WD	'COOC'	Load clock with 16 bits (0-15)
ASC TEST PNL (INDICATORS)	WD	'CO24'	Display data bits (12-15) – A13 selected (test panel)
	WD	'CO28'	Display data bits (4-7) – A12 selected (test panel)
	WD	'CO2C'	Display data bits (4-7) or (12-15) as selected by A12 or A13 switch position respectively.
ASC TEST PNL (FUNCTION SWITCHES)	RD	'C118'	Read function SW's labeled (0-7) on ASC test panel on to data bus bits (0-7)
	RD	'C114'	Read function SW's (8-15) on to data bus bits (8-15)
	RD	'C11C'	Read function SW's (0-15) on to data bus bits (0-15)
BIOMEDICAL CONSOLE	WD	'C002'	Send data (bits 0-7) to GE console
	RD	'C111'	Read GE console data onto data bus bits (8-15)
TIME CODE GENERATOR/ READER	WD	'C001'	Load gating signal & holdoff command from data bus bits (8-15)
	RD	'C013'	Read time data onto data bus bits (0-15)
ANALOG CONSOLE	RD	'C112'	Test single logic line status from analog console and read logic trunks 0 - 7 onto data bus bits 0 - 7.

Utilization of the indicators requires that the "7950-7954" be in the "7954" position. The indicator status appears on the indicator positions labeled 1-4 only, corresponding to the MSB and LSB, respectively, of the particular data byte selected. The remaining indicators, labeled 4-7, are not available for the assigned configuration and would always remain off.

BIOMEDICAL CONSOLE

A G.E. color display console is presently being prepared for interface installation with the Sigma-3. The DIO adapter (7930) will be used to transfer control information to and from this console. Control information will be contained in 8-bit data word transfers transmitted through the instruction/address code described in Table B-I. Operating instructions for the biomedical console will be supplied by G.E.

TIME CODE SYSTEM

Operation of the Systron-Donner time code generator/reader will initially consist of reading time information only. Time information is selected in groups (bytes) for reading by use of the 'WD' 'C001' instruction. The correspondence between time group selection with output data bits used for gating is illustrated in Figure B-1. Upon selection of the appropriate time byte, the corresponding time data is read onto data bus bits 04-15 through a 'RD' instruction. (See Table B-II for BCD time data formats.

The "hold-off" command can be used to block updating of time information until all groups of time are read. This signal must be removed upon completion of time reading.

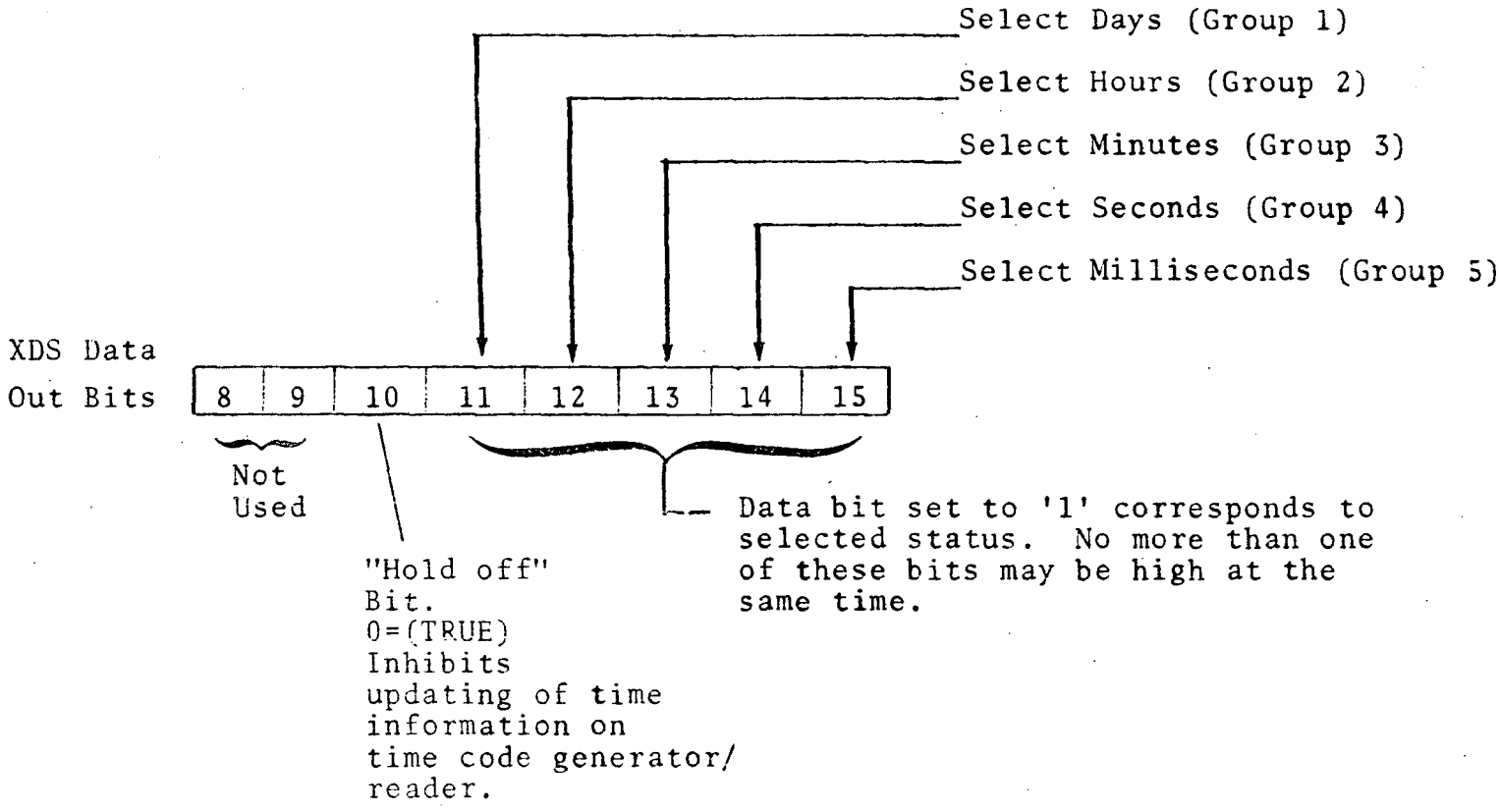


Figure B-I

Time Code Generator/Reader

Control Word Format

TABLE B-II

TIME DATA FORMATS

XDS* Data Bits	Group 1	Group 2	Group 3	Group 4	Group 5
15	Day × 1 "1"	Hr × 1 "1"	Min × 1 "1"	Sec × 1 "1"	Ms × 1 "1"
14	Day × 1 "2"	Hr × 1 "2"	Min × 1 "2"	Sec × 1 "2"	Ms × 1 "2"
13	Day × 1 "4"	Hr × 1 "4"	Min × 1 "4"	Sec × 1 "4"	Ms × 1 "4"
12	Day × 1 "8"	Hr × 1 "8"	Min × 1 "8"	Sec × 1 "8"	Ms × 1 "8"
11	Day × 10 "1"	Hr × 10 "1"	Min × 10 "1"	Sec × 10 "1"	Ms × 10 "1"
10	Day × 10 "2"	Hr × 10 "2"	Min × 10 "2"	Sec × 10 "2"	Ms × 10 "2"
09	Day × 10 "4"	Hr × 10 "4"	Min × 10 "4"	Sec × 10 "4"	Ms × 10 "4"
08	Day × 10 "8"	Hr × 10 "8"	Min × 10 "8"	Sec × 10 "8"	Ms × 10 "8"
07	Day × 100 "1"				Ms × 100 "1"
06	Day × 100 "2"				Ms × 100 "2"
05	Day × 100 "4"				Ms × 100 "4"
04	Day × 100 "8"				Ms × 100 "8"

*XDS data bits 0-3 are not used

If the "hold-off" command feature is not used, a "read-inhibit" command from the time code generator will turn off the condition code flag (CC4) during reading of time data; i.e., the 'CC4' flag set true signifies that the time data was not in the process of being updated when the particular data group was read.

ANALOG CONSOLE

Logic lines are provided connecting logic trunks 0 - 7 from the 680 console to the 7930 DIO. These lines were installed to provide logic control communications for sampling biomedical data from the cardiopulmonary lab.

ATTACHMENT C

CARDIOPULMONARY

EXERCISE RESPONSE TEST

(PHASE I)

CONDITIONING OF TIDAL VOLUME AND RESPIRATORY GAS ANALYSIS SIGNALS FOR COMPUTER INTERFACING.

GENERAL

The problem to be solved is to transfer the maximum tidal volume information, occuring at instant just prior to dumping, along with gas composition signals for that breath allowing sufficient settling delays for the gas composition before computer sampling. The respiratory gas compositions and tidal volume signals are transferred to the computer on each breath.

CIRCUIT DESCRIPTION

A circuit for performing this task on an EAI-680 analog computer is shown in Figure C-1. The circuit consist basically of several RS flip-flops, two A/D comparators, 2 differentiators, an interval or REP-OP timer, and an integrator configured to function as both a track and hold amplifier and a filter. Basic descriptions of these components and operation are covered in the 680 reference handbook.

Tracking and storing the maximum value of the tidal volume signal is accomplished by comparator No. 1 and the integrator amplifier. Whenever the original signal exceeds the stored value appearing on the output of the integrator, the comparator output will prescribe the integrate or tracking mode. When this tidal volume ceases to increase and is dumped, the state of the comparator switches and forces the integrator in the "hold" mode storing the maximum volume signal. The time constant τ_T of the tracking circuit is

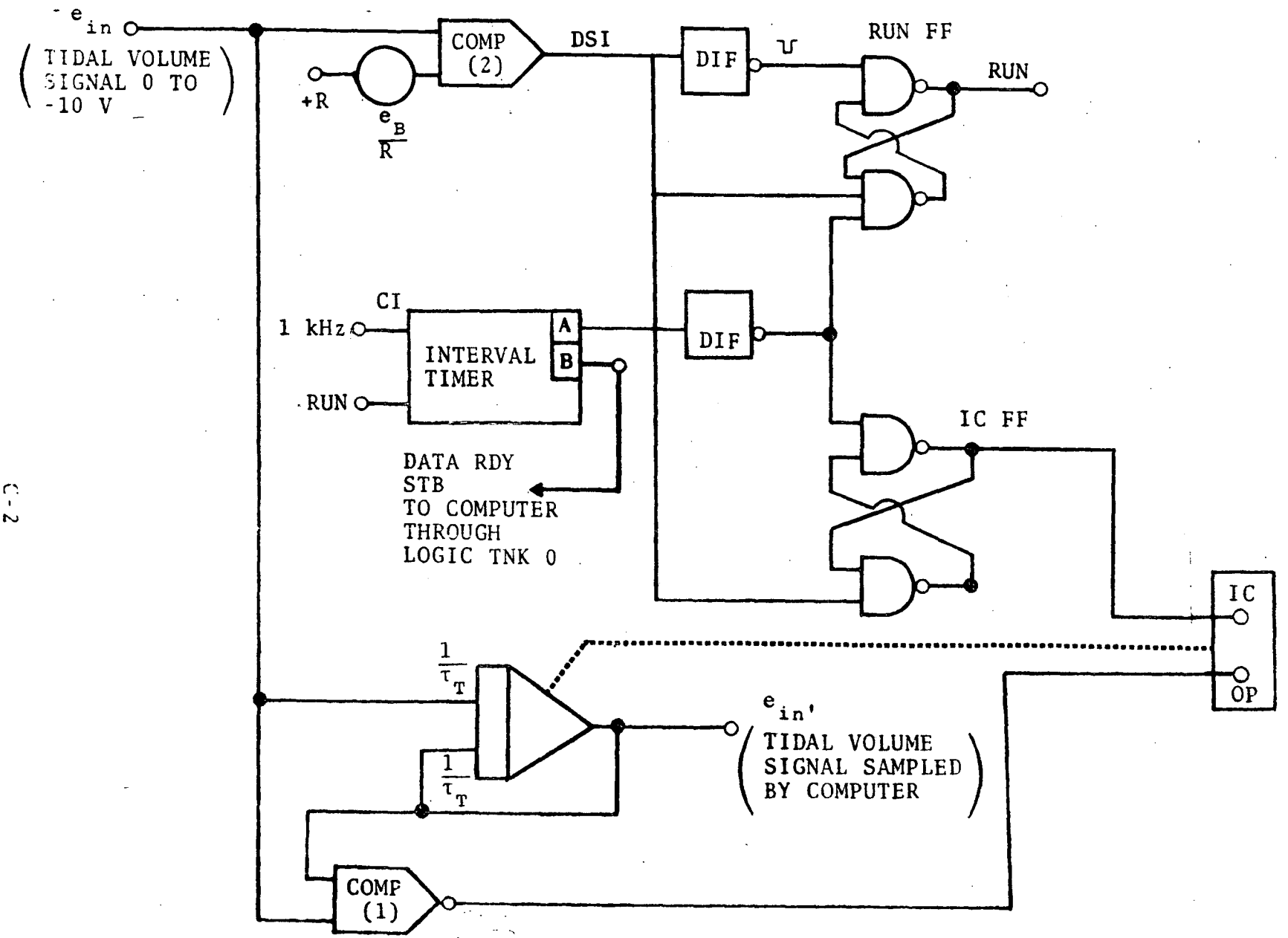


Figure C-1. – Tidal Volume Sampling and Timing Control

arbitrary within reasonable limits and typically would be 0.1 or 0.01 seconds. Initialization of the integrator ($e_{in}' = 0$) is determined by the true state of the IC flip-flop.

The interval timer is used to control the gas analysis delay (τ_D) and the sampling interval (τ_S) for flagging the Sigma-3 that data is ready. These intervals are set with thumbwheels on the 680 console. τ_D and τ_S are typically set to 600 ms and 15 ms, respectively.

Comparator No. 2 is used to initialize the RUN and IC flip-flop and also provide a trigger through the use of a differentiator to start the interval timer counting by establishing a RUN true status. Resetting the RUN flip-flop is also accomplished at the end of the B count at the moment the counter recycles back to the A state. Comparator No. 2 also has a small bias (e_B) that is set above the noise level of the incoming signal to illuminate comparator chatter around zero.

The initial condition flip-flop is effectively set at the end of the B count and is used to initialize the track and hold integrator for the next breath exhalation cycle.

A timing diagram of circuit operation is shown in Figure C-2.

OPERATION PROCEDURES

Setting up the circuit in Figure C-1 for operation requires setting the delay interval (τ_S) with thumbwheels on the REP OP timer corresponding to the A and B interval, respectively. The C interval must be set to zero. The bias or threshold level e_B requires setting one coefficient potentiometer to the desired level. All tidal volume signals

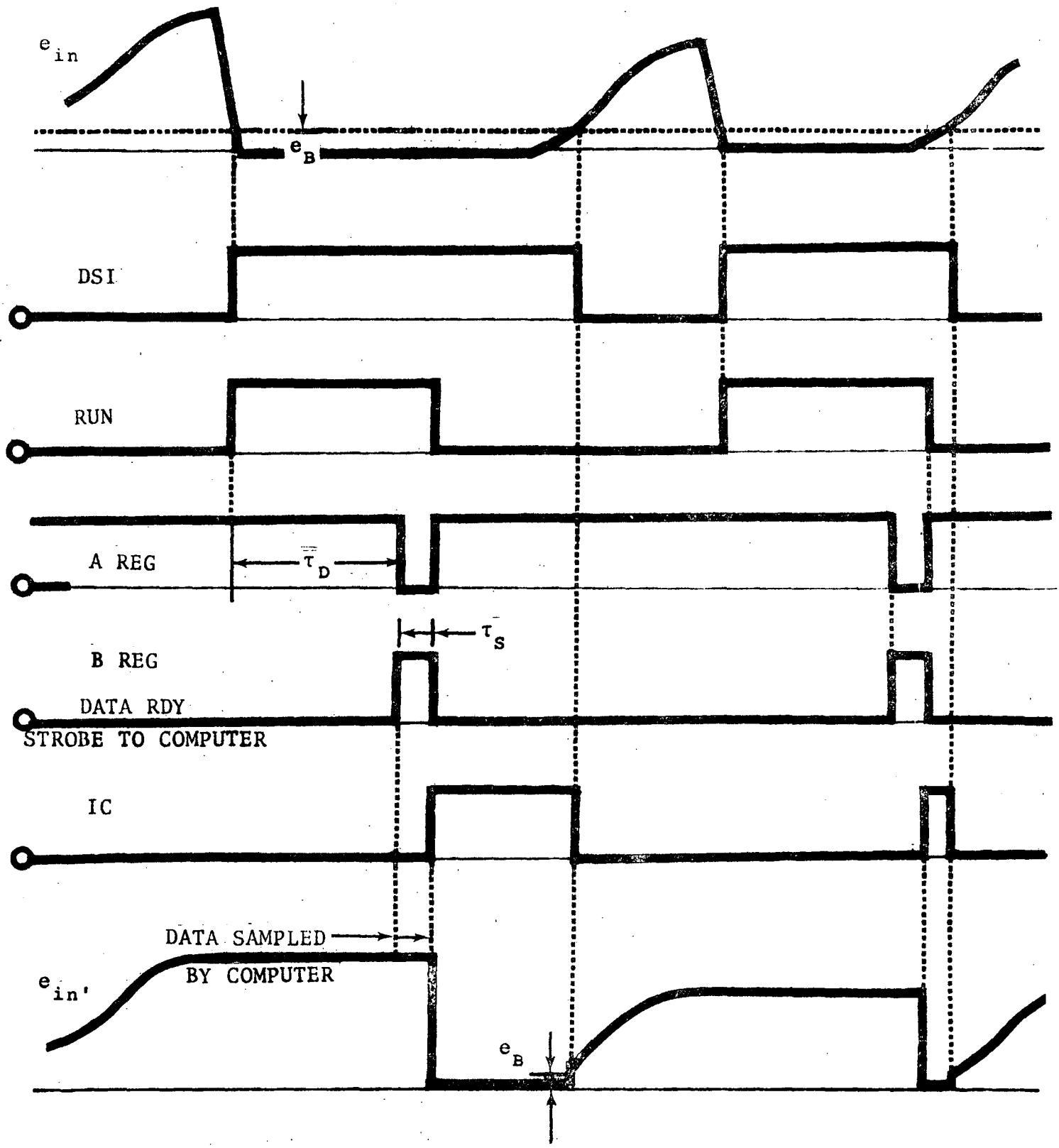


Figure C-2. – Timing Diagram

(Maximum values) below this value would not be sampled by the computer. The 10^6 clock and RUN mode pushbuttons must be activated from the digital control portion of the console. The IC mode must also be selected from the console pushbuttons. The tracking time constant (τ_T) can either be locally pinned or be selected from the time scale pushbuttons. 'N' and SEC selection on these pushbuttons would provide a value of τ_T = 0.1 sec when the gain 10 inputs are used on the integrator amplifier.

Testing of the "data ready" strobe by the Sigma-3 is accomplished by executing a Read Direct (RD) with an effective address of 'C112' through the 7930 DIO system. The condition code flag CC4 will be turned 'ON' when the strobe is not present. Condition code CC3 will always be turned on when the Rd instruction is executed. The pulse width of the data-ready strobe is selected on the basis of the polling rate and A/D converter acquisition time. For a polling rate of 80 per sec, the τ_S interval would be 12.5 ms plus the A/D acquisition time.