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THE MIT OSO-7 X-RAY EXPERIMENT

A Five-Color Survey of the Positions and
Time Variations of Cosmic X-ray Sources

CASE FILE
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16. Abstract

An all-sky, five-color x-ray survey experiment for OSO-7 is described. X-ray measurements are made in five broad energy bands from 0.5 to 60 kev with x-ray collimators of one and three degree FWHM response. Working with the on-board star sensor source locations may be determined to a precision of +0.1°. The experiment is located in wheel compartment number three of the spacecraft. A time division logic system divides each wheel rotation into 256 data bins in each of which x-ray counts are accumulated over a 190 second interval. Measurement chain circuits include provision for both geometric and risetime anticoincidence. A detailed description of the instrument is included in this report as is pertinent operating information.

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Preface

The launch of OSO-7 on Sept. 29, 1971, marked the end of a four-year program to develop a multicolor spaceborne instrument for x-ray astronomy. This program was carried out in the Laboratory for Space Experiments (a part of the Center for Space Research) at the Massachusetts Institute of Technology, Cambridge, Massachusetts. In the six months following launch, an all-sky x-ray survey will be made as well as long term observations on sources of particular interest. This document is the final report on the development program.

The report includes detailed descriptions of the experiment and its implementation. Of particular interest will be the discussion of the four-color proportional counters, which are of unusual design, and the relatively large random access semiconductor memory that matches certain spacecraft and shift register characteristics to achieve very low power operation. Additionally, a comprehensive test history is included in the hope that others can benefit from our problems. Certain difficulties we experienced in the integrated circuit and high voltage diode areas, particularly, would best be avoided in future programs.

Conclusions and recommendations are spread throughout the test in the belief that most readers will have specialized interests and will find it useful to have all comments relating to a particular area in one section of the report. Conclusions and recommendations will usually be found under the heading "Design Comments."

It is not intended to re-hash instrument problems and solutions detailed in our monthly and quarterly progress reports. As is appropriate to a final review, summaries are the rule here. Detailed information is provided on instrument status at launch so that all system information likely to be pertinent to our instrument operation and data reduction effort will be available from one source.

Unless otherwise noted, all specific operating values for the instrument are taken from the Flight Log maintained by MIT throughout the program.

This report was prepared to GSFC Specification S-250-P-1B, "Contractor-Prepared Monthly, Periodic and Final Reports." Both SI (International System) units and common units have been used throughout the program. Where SI units were used, those values are given alone; where common units were used, both values are given.

Contributions to this report have been made by Dr. George Clark (Principal Investigator), Dr. George Sprott (Project Scientist)who prepared Section 2.0, J.J. Gomes (CSR Staff), and T.F. Dawson (CSR Quality Assurance Manager). The manuscript was prepared for publication by Mrs. Jennifer Kelley and Miss Joan Gillen and drafting support provided by Mr. John Donahue; all of CSR. Their assistance was needed and is appreciated.

Richard S. Taylor
Project Engineer
November 15, 1971

Table of Contents

Table of Contents

Table of Contents

Table of Contents

Table of Contents

List of Illustrations

List of Illustrations

List of Tables

List of Drawings

1.0 INTRODUCTION

OSO-7 was launched 5:45 A.M. (EDT) on 29 September 1971. In spite of a hydraulic failure in the second stage of the Thor-Delta N launch vehicle, a successful, if slightly eliptical* orbit was achieved.

The MIT experiment is performing a multicolor survey of the position and time variations of cosmic x-ray sources. Its purpose is to obtain data which will clarify the nature of x-ray sources and their relation to stellar evolution and galactic structure. The experiment is designed to carry out a comprehensive, all-sky survey of sources with intensities greater than 10^{-3} x-ray photons cm^{-2} sec^{-1} ($\sim 10^{-3}$ x intensity of the Crab Nebula), to measure their positions with an accuracy of $\pm 0.1°$ for the brighter sources, characterize their spectra by measurement of their intensities in five broad energy bands from 1 to 60 keV, and to determine their long and short term variability on a time scale ranging from minutes to several months. Predictions based on the distribution and intensities of the approximately forty x-ray sources known at present indicate that many hundreds, and possibly thousands of sources will be observed by the MIT experiment. Thus, the experiment should greatly extend the systematic knowledge of X-ray sources and may reveal new and unexpected phenomena heretofore unavailable to observation.

The Flight Instrument is shown in Figure 1-1. It is located in wheel compartment three of the spacecraft. Two banks of five proportional counters each behind the 1° and 3° collimators are used as x-ray detectors. The collimators serve to limit the view angle of the detectors without reducing the x-ray sensitive area of the counters unacceptably. High voltages for the detectors are generated in the Power Converter.

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*570.81 km x 328.35 km (19 Nov. 1971).

A radiation monitor senses the entrance into regions of high intensity particles (such as the South Atlantic Anomaly) and shuts down the detector high voltages to prevent operation in these regions which would reduce useful counter life. The Power Converter also supplies four low voltages for the electronics system.

The x ray detection rate is many times faster than the available 100 bit per second data transmission rate. Data compression is performed with the aid on the on-board memory, a 19.2 kilobit shift register system.

Each spacecraft wheel rotation is divided into 256 data accumulation intervals or "bins." A particular bin relates to a particular look direction and x-ray events, summed in a bin over the 190 second data format interval are events from that look direction. The bin number, which is identified in the MIT data format, plus the spacecraft aspect solution provides all the information necessary to relate x-ray events to a location on the celestial sphere within the required accuracy. The instrument includes all the control functions necessary for the bin system and data formating, primarily in the form of integrated circuit logic. Low power logic from the Fairchild 9040 series is used in all integrated circuit areas. Approximately 500 integrated circuits and a few hundred discrete transistors are required by the system.

The seven spacecraft commands assigned to MIT control sixteen instrument functions. Individual counters can be logically disabled and the various antico and calibration systems can be enabled or disabled. An automatic calibration system is included, providing for calibration of each counter bank on one orbit out of every thirty-two. All of the electronics, except for the power converter and counter preamplifiers, are contained in the "Electronics Box" (See Figure 1-1).

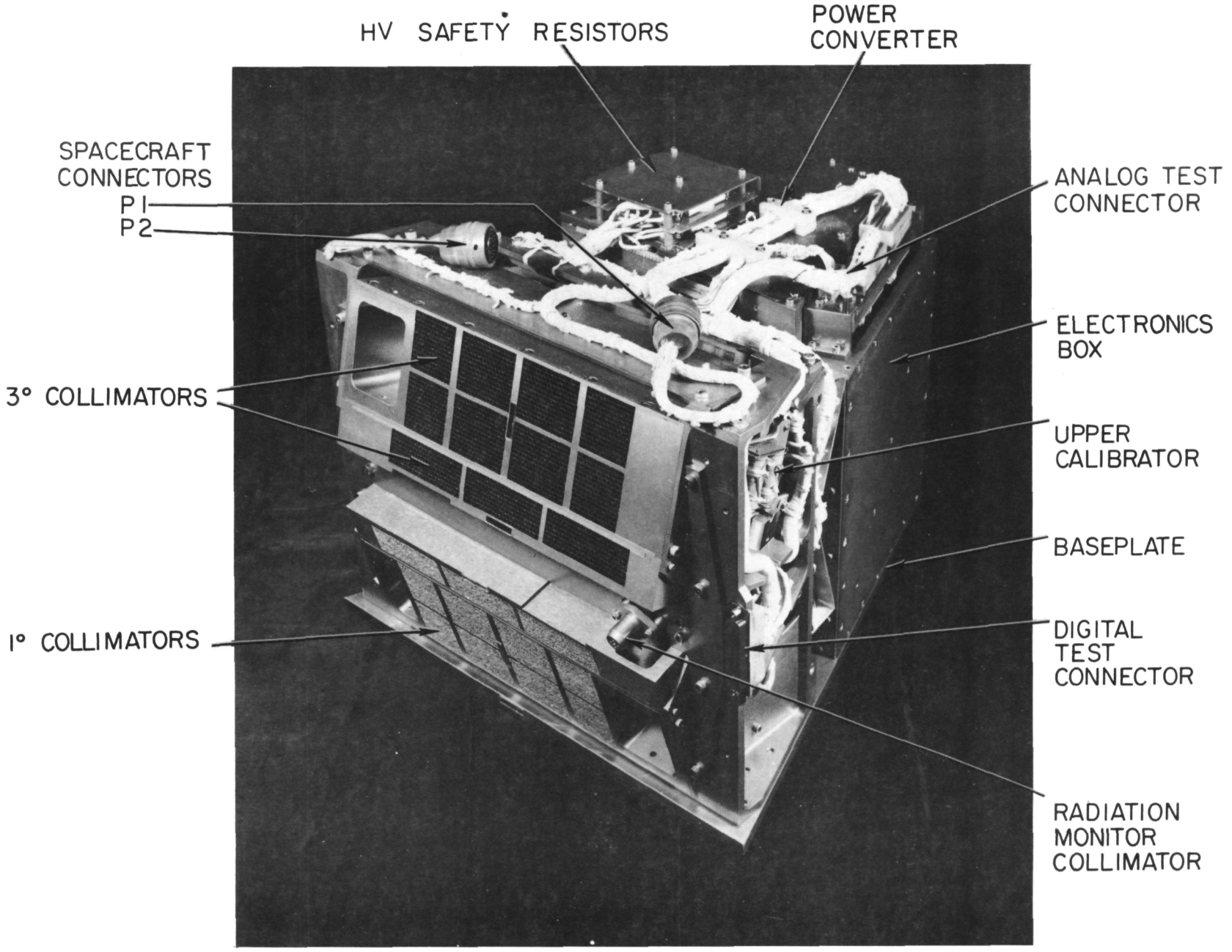

FIGURE 1.1 M.I.T. OSO-7 X-RAY INSTRUMENT

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Two instruments, a prototype and flight model, were made. The Prototype was refurbished to serve as a Flight Spare. The MIT Center for Space Research, Laboratory for Space Experiments (LSE)*, designed and fabricated the instruments under NASA contract NAS 5-11082. The Laboratory is under the direction of Mr. R.H. Baker and Dr. J.H. Binsack. Dr. George Clark, Professor of Physics at MIT, is Principal Investigator, and Dr. George Sprott, Project Scientist. Program Manager for LSE was Mr. Robert Rasche and Project Engineer was Mr. Richard S. Taylor. LSE staff assigned to the program included Mr. T.F. Dawson (Quality Assurance), Mr. T. Egan (Mechanical Design), Mr. D. Humphries (Electronic Packaging), and Mr. J.J. Gomes (Measurement Chain Design).

The Prototype was delivered for bench tests 30 Sept. 1970 and qualification tests completed 20 Mar. 1971. Flight Unit assembly was finished 31 Jan. 1971, acceptance tests completed 29 Mar. 1971 and the instrument delivered 31 Mar. 1971. The refurbished prototype was delivered 7 Sept. 1971.

A short review of experiment science and data handling procedures is the subject of Section 2.0 and the instrument is described in Section 3.0. Section 4.0 summarizes the test history of the program and discusses critical instrument problems and solutions. Instrument operating parameters will be found in Section 3.0.

Instrument operations have proceeded in marked contrast to the drama of orbit insertion. The MIT instrument, operating for two months now, has observed a number of x-ray sources and data processing has begun. Initial results will be published shortly.

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*265 Massachusetts Avenue, Cambridge, Massachusetts 02139.

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2.0 THE EXPERIMENT

2.1 Scope and Purpose

A number of discrete cosmic x-ray sources have been observed since 1962, of which several have been definitely associated with visible objects. Among these is the sun, several nebular supernova remnants, a pulsar, several irregular rapid variables, pulsating sources, Seyfert nebulae, radio galaxies, and quasars. Thus at least eight, and possibly more, distinct types of celestial objects have already been found among the sources observed so far.

The remarkable character of the unexpected phenomena encountered in x-ray astronomy is shown in ScoX-1 which radiates over one thousand times more power in x rays than in visible light or radio waves. The x rays in the 2 to 8 Å wavelength range appear to be generated by free-free emission from a hot plasma at a temperature near 50×10^6 °K. On the other hand, the presence of hydrogen emission lines in its visible spectrum proves the existence of a much cooler region somewhere in the object, and the discovery of intense emission at wavelengths greater than 44 Å strongly suggests a third region of intermediate temperature. Thus ScoX-1 appears to be a complex object with stellar structures of a form never encountered before. It seems likely that it is associated with a gravitationally condensed object like a neutron star or a black hole.

The present experiment was initiated with the aim of achieving an all-sky survey to obtain the time variation, spectra and accurate positions of x-ray sources over a range of intensities down to about 2×10^{-3} times that of the Crab Nebula.

2.1.1 Expected Results - After an assumed operating time of 180 days almost the entire sky will have been scanned, and in those regions with average exposure all sources with intensities greater than 6 x 10^{-3} cm^{-2} sec^{-1} in the wavelength range from 1.0 to 60 keV (i.e. approximately .002 times the intensity of TauXR-1) will appear as four sigma peaks in the resulting celestial x-ray map.

Each detected source will be characterized by a five-color index in the manner of the U-B-V indices of optical astronomy.

Positions of sources will be determined with an uncertainty less than $\pm$.10°. The position of the weakest detectable sources will be determined with an uncertainty of approximately $\pm$1.0°.

The detectors are oriented 15° above and below the satellite's equatorial plane so that, with the expected roll and pitch motion of the OSO, most regions of the sky will be scanned continuously for periods of two or three days at intervals of 30 and 120 days. The detector efficiencies are periodically calibrated in orbit. The data should therefore reveal the existence of variations occurring with characteristic times ranging from minutes to months.

2.1.2 Initial Results - A number of x-ray sources have been observed at the time of writing including ScoX-1 and the Crab Nebula (TauXR-1),but data reduction has not yet proceeded to the point at which preliminary results are available.

2.2 Data Handling

2.2.1 Quick-Look Data Handling - A first quick pass is made through all incoming quick-look data as soon as it is received to check experiment operation, obtain initial star-sensor aspect solutions and to identify elements in the data

for future, more detailed, processing. Programs used in this first pass are summarized below. The OSO Control Center Program was also used to check experiment operation during on-ground testing of the instrument.

2.2.1.1 OSO Control Center Program - A program for the printout of MIT data in real time at the OSO Control Center was written for GSFC* by Ball Brothers Research Corporation (Boulder, Colo.), the spacecraft contractor. A similar program was written to display MIT data during spacecraft tests at BBRC. Two pages of this printout follow (Figures 2-1 and 2-2). A comparison with MIT Drawing 107-800007(Section 3.3.1) will reveal their similarity to the designed format. Engineering and scientific information from the format start and block start lines is printed above each block. The top line of the page provides certain spacecraft and time data. Command Status is displayed in hexadecimal and, again, as a listing. Bin width is shown in counts and must be multiplied by 2.0 μs per count to get durations. Antico rate (and count rate on even orbits) is prescaled and must be multiplied by 12.9 to obtain a rate in Hertz. Analog data is displayed as analog counts in these examples,and reference must be made to the OSO-7 Telemetry Data Conversion Tables (BBRC TN69-23B or to Section 3.5.4) to obtain output values. Analog labeling is determined from the sync level on line 1.

In the format start block, the overflow words are displayed in hexadecimal. The indicated counter assignments (above the hexadecimal display) are in error. The printout should read 2156 above the overflow hexadecimal word. All

*Goddard Space Flight Center, Greenbelt, Maryland.

three aspect pulse indicators are displayed here whereas only the ASPECT display occurs in the block start line. A block sum is provided at the bottom of each counter column to facilitate monitoring of counter rates in the calibrate mode.

2.2.1.2 Azimuth Printer Plots - At MIT's request, GSFC supplied a program to plot MIT's observed x-ray counts as a function bin number on standard computer printout form. This facility was for use only in the first few weeks following experiment turn on. A portion of one of these printer plots is shown in Figure 2-3. Since each bin number represents a different direction in space, the locus of all bin directions for one counter bank form a small circle on the celestial sphere. Thus, what is shown in the printer plot is the count rate as a function of azimuth arc on the small circle. The different symbols refer to different counter numbers with the exceptions that for the 3° counter bank the symbols N, A, K, X, T instead of counter numbers 5, 6, 7, 8, 10 have been used, respectively. A point source of x rays would cause increased counts in 1 or 2 adjacent bins in the 1° counter bank and 4 or 5 adjacent bins in the 3° bank. Direction dependent radiation belt effects occur over a wider range of bins and are easily distinguished from celestial x-ray sources.

This type of plot has become a powerful diagnostic tool and a similar plotting program has now been written for use on the MIT computer.

2.2.1.3 Analysis of Quick-Look History Tapes (Pass I Program) - Each day a magnetic tape containing spacecraft data is sent from the OSO Control Center to MIT by air parcel post special delivery. The tape is received within twenty-four hours of the time it leaves the control

20CT71 ORB 51 GMT 275/16:38:23.915 MIT QUICKLOOK PROGRAM SNTAGO PB XDS SYNC 0000 FR CNT 4

FORMAT=START DAY ORBIT=10 OVERFLOW=0000 BIN-WIDTH= 1256 4329 ANTICO-RATE= 24 PULSES SUN(1) MAG(1) ASPECT(1)

SYNC	BIN	CTR1	CTR2	CTR3	CTR4	CTR5	CTR6	CTR7	CTR8	CTR9	CTR10	COMMAND-STATUS	ALOG1	ALOG2	ALOG3	ALOG4
	0	9	7	5	30	43	4	7		6						
	1	11	5	4	31	37	6	12		7						
	2	8	4	9	19	30	8	4		4						
	3	8	4	5	27	24	7	8		2						
	4	9	3	6	29	31	10	6		6						
	5	9	6	12	28	18	5	11		3						
	6	10	3	8	26	31	3	8		5						
	7	9	4	10	20	27	4	9		5						
	8	7	6	4	22	16	4	10		5						
	9	10	4	13	25	21	6	14		4						
	10	11	1	5	25	13	4	9		6						
	11	8	4	13	24	16	5	4		5						
	12	16	1	9	30	23	2	6		3						
	13	12	7	9	25	20	5	6		6						
	14	11	2	6	23	11	6	6		3						
	15	6	3	5	28	22	2	8		2						
	16	8	9	6	33	16	7	4		3			SYNC3 81	PWR-CND-T 81	BASE-T 81	CAL-ACT-T 81
11	17	13	8	6	27	24	4	7		5						
	18	8	7	11	23	14	3	10		3						
	19	6	3	7	32	11	2	6		5						
	20	10	4	9	25	12	5	8		2						
	21	17	5	7	24	17	4	9		5						
	22	11	2	8	24	14	7	3		7						
	23	10	8	3	25	10	7	11		4						
	24	9	9	9	47	12	7	5		2						
	25	4	10	8	28	11	9	4		11						
	26	7	4	5	26	16	5	9		5						
	27	9	6	8	28	13	6	4		8						
	28	10	4	2	26	13	2	7		5						
	29	14	7	9	28	14	2	7		9						
	30	13	4	5	32	13	4	5		4						
	31	10	6	10	28	15	4	9		3						
		313	160	256	868	608	159	234	0	153	0					

Figure 2-1 Typical MIT Format Start Data Block

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20CT71 ORB 51 GMT 275/1638:23.915 MIT QUICKLOCK PROGRAM SNTAGO PR XDS SYNC 0000 FR CNT 4

FORMAT=START DAY ORBIT=10 OVERFLOW=0000 BIN=WIDTH= 4329 ANTICO-RATE= 24 PULSES: SUN(1) MAG(1) ASPECT(1)

1256

SYNC	BIN	CTR1	CTR2	CTR3	CTR4	CTR5	CTR6	CTR7	CTR8	CTR9	CTR10	COMMAND-STATUS	ALOG1	ALOG2	ALOG3	ALOG4
	0	9	7	5	30	43	4	7		6						
	1	11	5	4	31	37	6	12		7						
	2	8	4	9	19	30	8	4		4						
	3	9	4	5	27	24	7	6		2						
	4	9	3	6	29	31	10	6		6						
	5	9	5	12	28	18	5	11		3						
	6	10	3	8	26	31	3	8		5						
	7	9	4	10	20	27	4	9		5						
	8	7	6	4	22	16	4	10		5						
	9	10	4	13	25	21	5	14		4						
	10	11	1	5	25	13	4	9		6						
	11	8	4	13	24	16	5	4		5						
	12	16	1	9	30	23	2	6		3						
	13	12	7	9	25	20	5	6		6						
	14	11	2	6	23	11	6	6		3						
	15	6	3	5	28	22	2	8		2						
	16	8	9	6	33	16	7	4		3			SYNC3	PWR-CND-T	BASE-T	CAL-ACT-T
	17	13	8	6	27	24	4	7		5			81	81	81	81
	18	8	7	11	23	14	3	10		3						
	19	6	3	7	32	11	2	6		5						
	20	10	4	9	25	12	5	8		2						
	21	17	5	7	24	17	4	9		5						
	22	11	2	8	24	14	7	3		7						
	23	10	8	3	25	10	7	11		4						
	24	9	9	9	47	12	7	5		2						
	25	4	10	8	28	11	9	4		11						
	26	7	4	5	26	16	5	9		5						
	27	9	6	8	28	13	6	4		8						
	28	10	4	2	26	13	2	7		5						
	29	14	7	9	28	14	2	7		9						
	30	13	4	5	32	13	4	5		4						
	31	10	6	10	28	15	4	9		3						
		313	160	236	868	608	159	234	0	153	0					

Figure 2-2 Typical MIT Data Block

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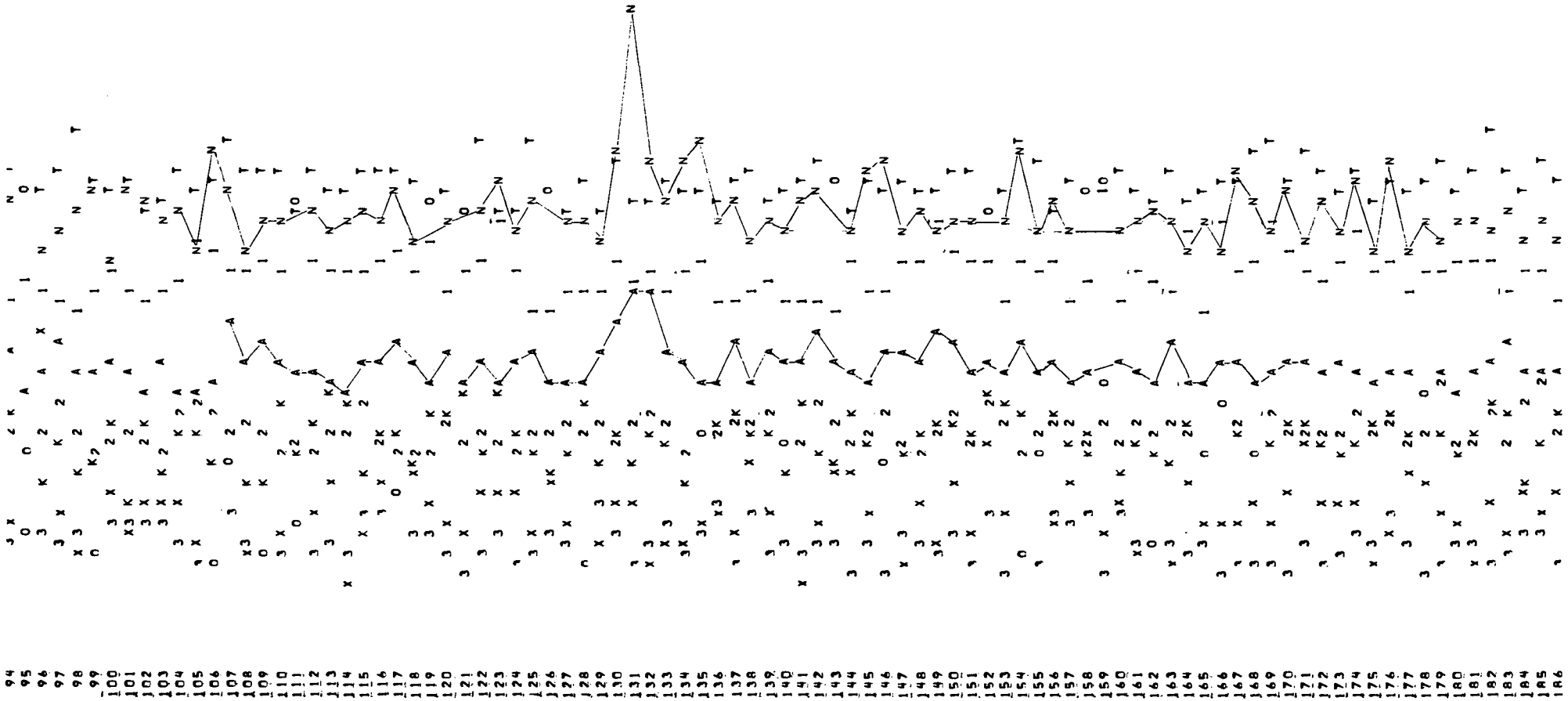

FIGURE 2-3 TYPICAL MIT AZIMUTH PRINTER PLOT. A SOURCE IS OUTLINED IN COUNTERS N AND A

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center. Contained on the tape is all OSO-7 data received by the control center in the previous twenty-four hours. There are typically eight playbacks per day.

Upon receipt of the tape it is read with the MIT Quick-Look Program (Pass I). The primary purpose of Pass I is to obtain an aspect solution to the star sensor data and to decommute the MIT x-ray data. The program generates Calcomp plots of count rates and housekeeping functions versus time and also generates plots of orbit averages of the x-ray count rates versus bin number; the orbit average plots will shown any x-ray sources that are scanned across during the orbit. Pass I also generates a quick-look event tape giving the observed x-ray counts for each format plus the aspect solution for the same time. This tape is then available for further analysis of the data. Figures 2-4 and 2-5 show samples of quick-look time plots and orbit average plots respectively.

2.2.1.4 Format Plots of Quick-Look Data - Using the quick-look event tape as input, the observed counts versus bin number for each counter is plotted on microfilm. This type of plot is similar in purpose to the printer plots described in Section 2.2.1.2 and was inspired by those plots. By having these plots on microfilm the data storage problem which would occur if printer plots were used extensively is avoided. A sample plot in this format is shown in Figure 2-6.

2.2.2 Analysis of Experimenter's Tapes -

2.2.2.1 Star-Sensor Data (Pass II Program) - This is a backup to the GSFC aspect analysis procedure. Raw star sensor data is sent to MIT on special experimenter's tape and the Pass II program finds an aspect solution to this data. The program is for use only in the event that MIT does

not receive good aspect information on the experimenter's tapes. We expect to use this program only in rare instances.

2.2.2.2 Analysis of MIT X-Ray Data (Pass III Program) - There are two major functions of this program:

(1 It decommutes the MIT data and writes this data along with the aspect information in a convenient form on "master event tapes."

(2 It provides plots of the experiment housekeeping functions and x-ray data summary information to be used as a record of experiment operation and as a description of the information contained on the master event tape.

The master tapes will be used for all subsequent analyses of the x-ray data. This will include finding the positions, intensities, and time variations of celestial x-ray sources and constructing a map of the x-ray intensity over the celestial sphere. Copies of the master tapes will be supplied to the National Space Science Data System.

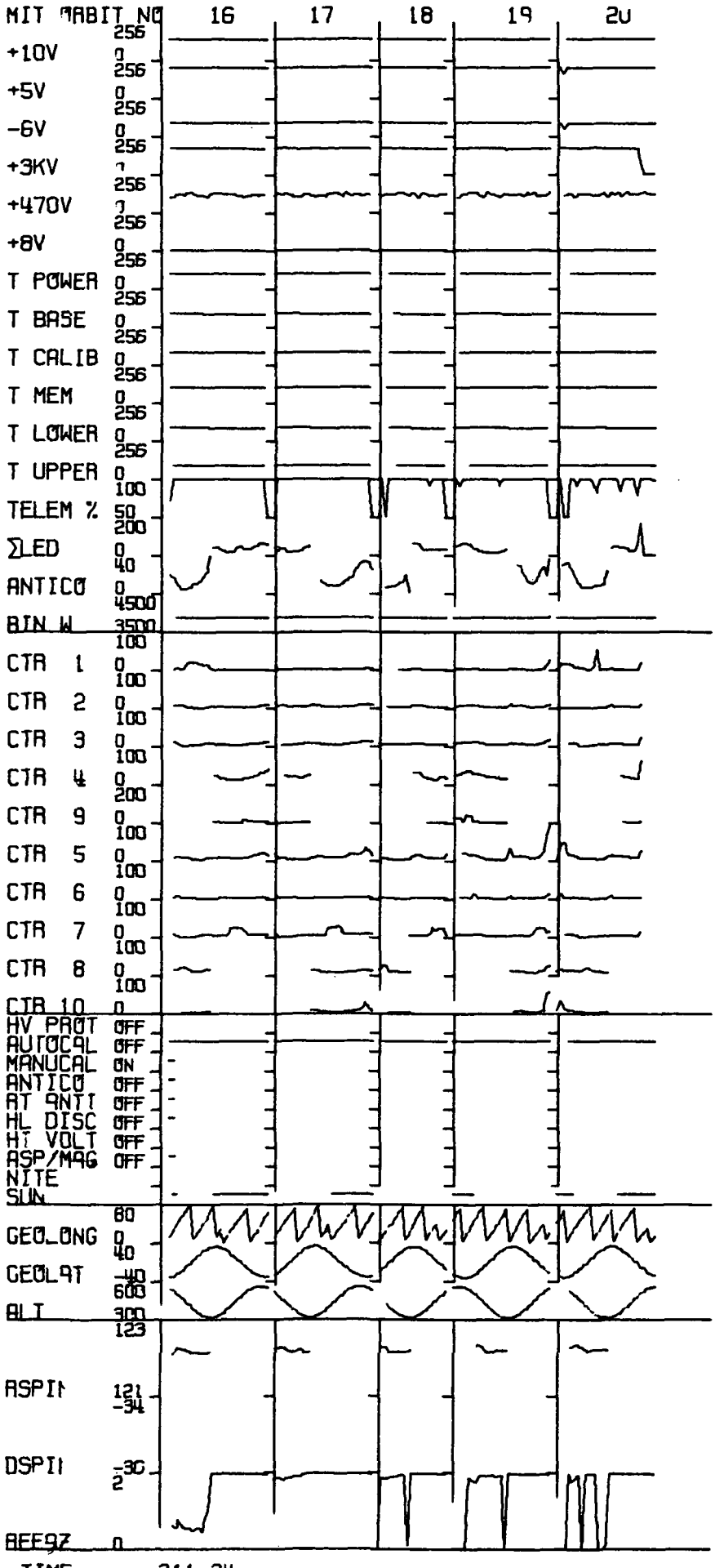

FIGURE 2-4 TYPICAL MIT QUICK LOOK TIME PLOTS

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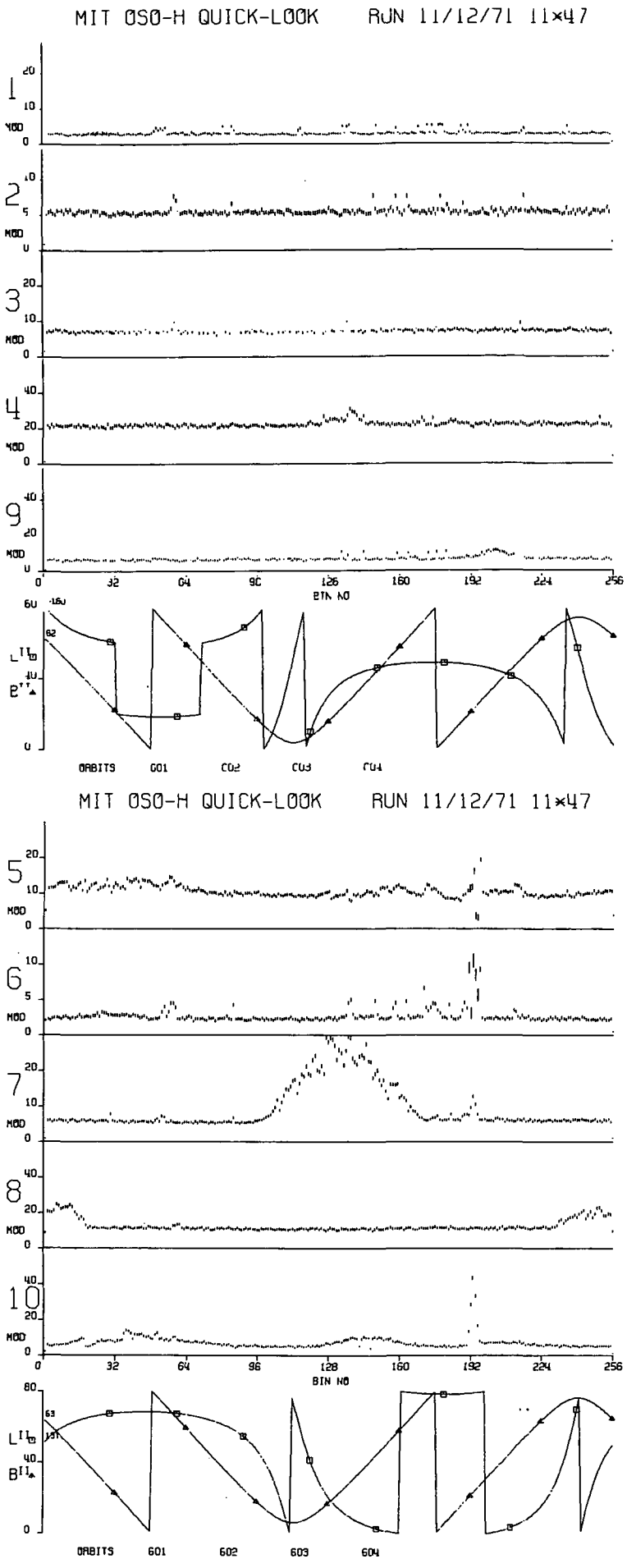

FIGURE 2-5 TYPICAL MIT ORBIT AVERAGE PLOT

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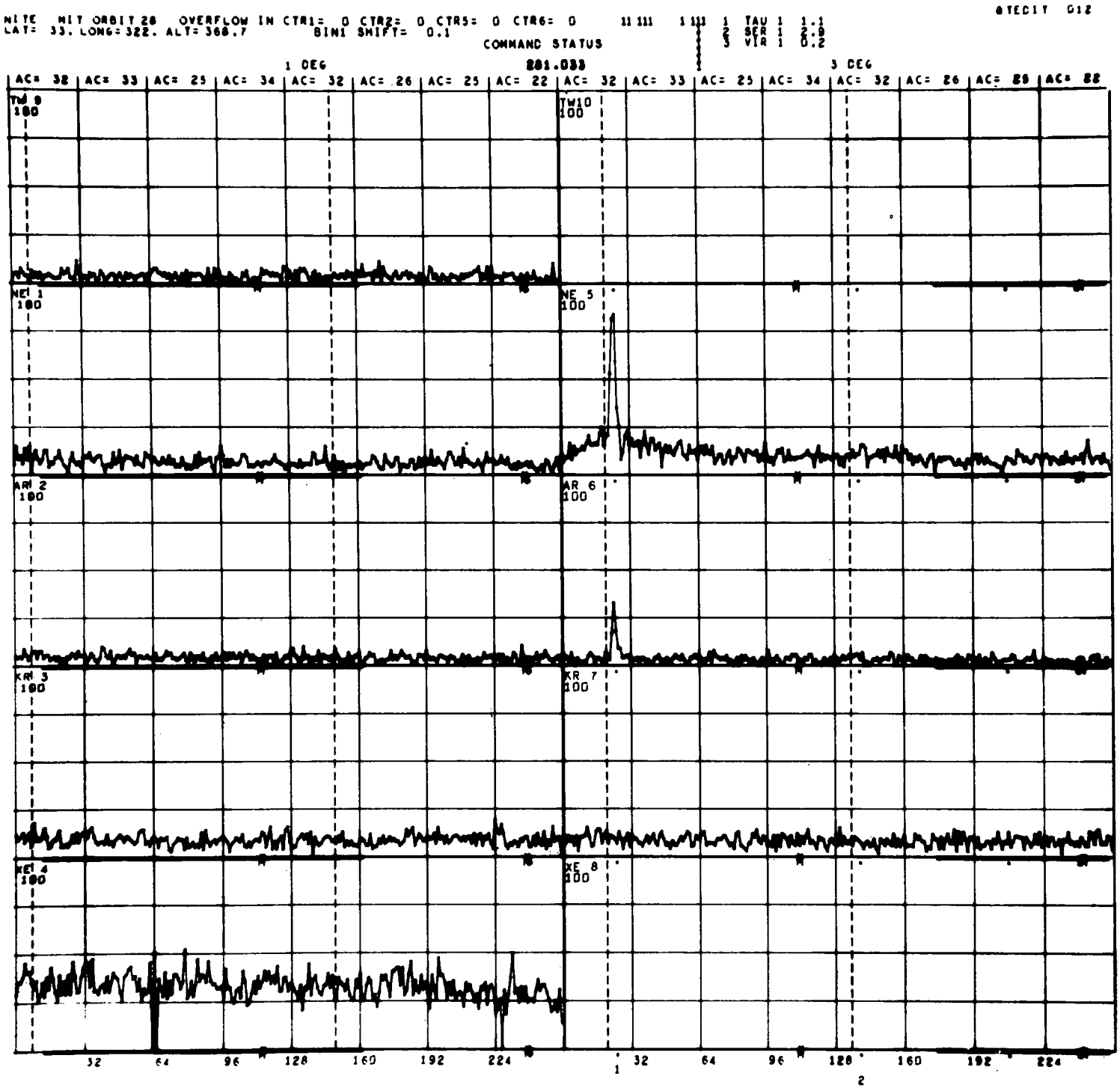

FIGURE 2-6 TYPICAL MIT FORMAT·PLOT OF QUICK LOOK DATA

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3.0 THE INSTRUMENT

An overview of the MIT X-ray Instrument was provided in Section 1.0. The "portrait" of the instrument (Figure 1-1) is here supplemented by "mug shots", Figures 3-1, 3-2, and 3-3, and the top assembly drawing 107-000001. These figures show the instrument (Serial No. 2) that is operating on board OSO-7. The major components of the instrument are identified by callouts.

The function of the instrument is to search for new cosmic x-ray sources and to study these and presently known sources spectrally and for time variations. Through its incorporation into the wheel section of OSO-7 it will scan the major portion of the celestial sphere within six months of launch. Proportional counters, sensitive to five distinct energy ranges, x-ray collimators of 1° and 3° FWHM (full-width-half-maximum) sensitivity and time division "binning" of the wheel rotation are the means to this end. Figure 3-4 details the experiment subsystems.

The proportional counters are housed forward in the instrument behind the collimators. In the photographs they are almost totally hidden by the detector mounting side brackets with only the end wells of Counters 4 and 8 fully visible between the detector brackets and the electronics box.

The counter designs are unique. Spectral sensitivity is achieved by providing five combinations of window and gas fill characteristics (Section 3.1.1). In the lowest energy range a state-of-the-art 0.0003 inch aluminum window with Neon-CO_2 gas fill is used to achieve a spectral sensitivity of 1-1.5 keV. These are Counters 9 and 10 in the instrument and are only partially visible in the figures.

In the upper energy ranges a back-to-back assembly of four counters of differing spectral sensitivity is used. This

back-to-back arrangement is an MIT development. The detector for the highest energy range is furthest back in the assembly and its "window" is the combination of all the gas fill and metallic window material ahead of it in the assembly.

There are two such groups of five counters in the instrument, one located behind the 1° collimator, the second behind the 3° collimator. The total of ten counters operate simultaneously, the pulse outputs feeding low-noise amplifiers and processing circuits (Section 3.1.3). Of the ten simultaneous outputs from the processors which are identified as x-ray events, eight are chosen by the Configuration Logic (Section 3.4) for bin-by-bin accumulation in the memory.

With the exception of the low level measurement chain amplifiers and the high voltage filterboards, which are housed in wells in the counter ends, all of the experiment electronics is contained in the "Electronics Box". This box holds the measurement chain processors which identify certain counter events as x rays, the x-ray data accumulators and the 19.2 kilobit memory, the experiment Configuration Logic and the Format Logic (Sections 3.2 through 3.5).

All instrument high and low voltages are provided by one power converter. Five high voltages between 1 and 2.5 kilovolts, four low voltages between minus 6 and plus 10 volts and a single medium voltage output of 470 volts are supplied (Section 3.6).

On-board x-ray calibration is achieved by uncapping small (less than 1 microcurie) Am^{241} sources that are mounted between the collimators and proportional counters. An electromagnetic shutter (Section 3.1.4) uncaps these sources on command or automatically, as controlled by the Configuration Logic (Section 3.4). The sources are uncapped two at a time by the actuator coils visible in the side views.

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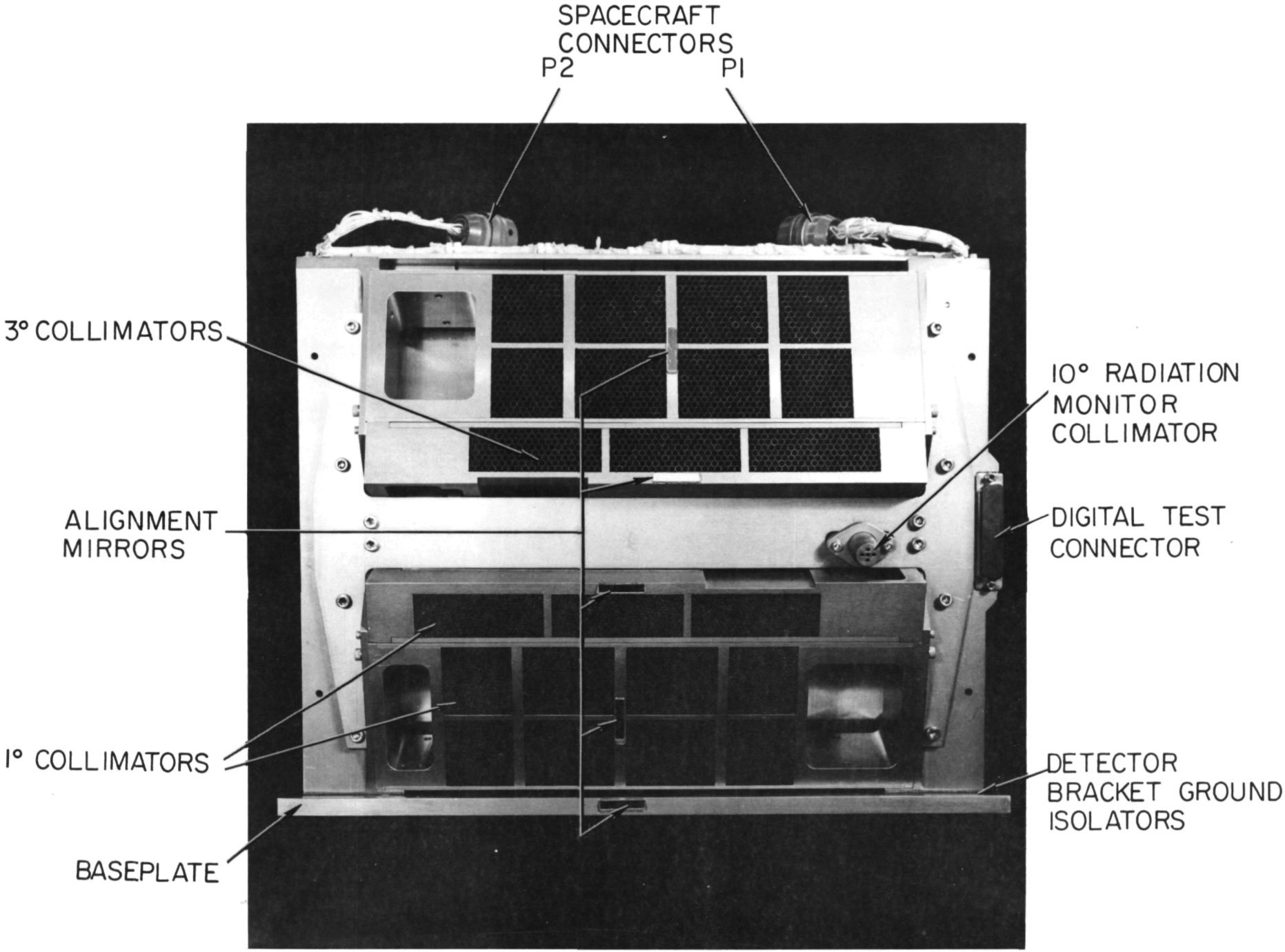

FIGURE 3-1. M. I. T. OSO-7 X-RAY INSTRUMENT. FRONT VIEW

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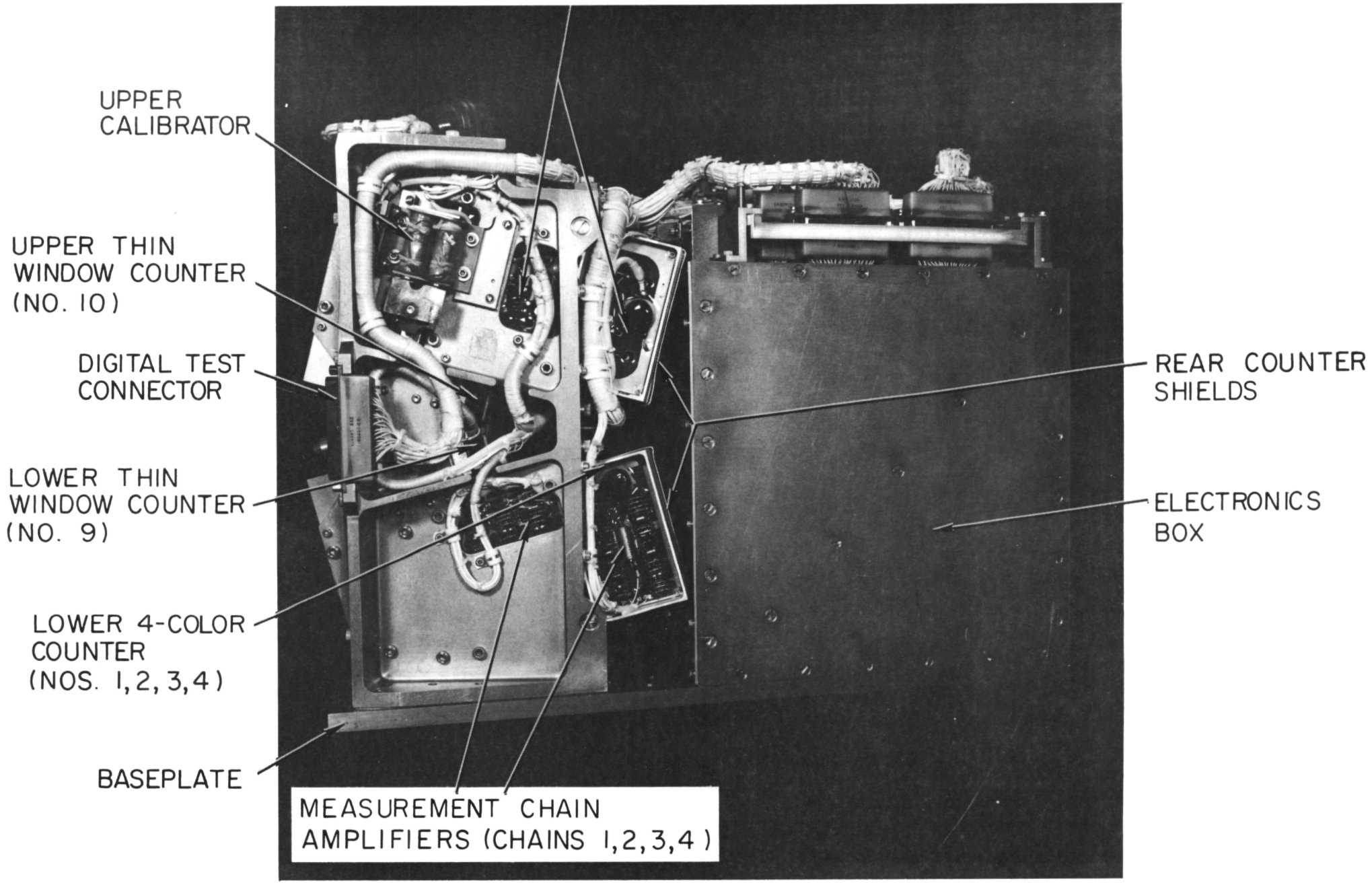

FIGURE 3-2 M.I.T. OSO-7 X-RAY INSTRUMENT. RIGHT SIDE VIEW

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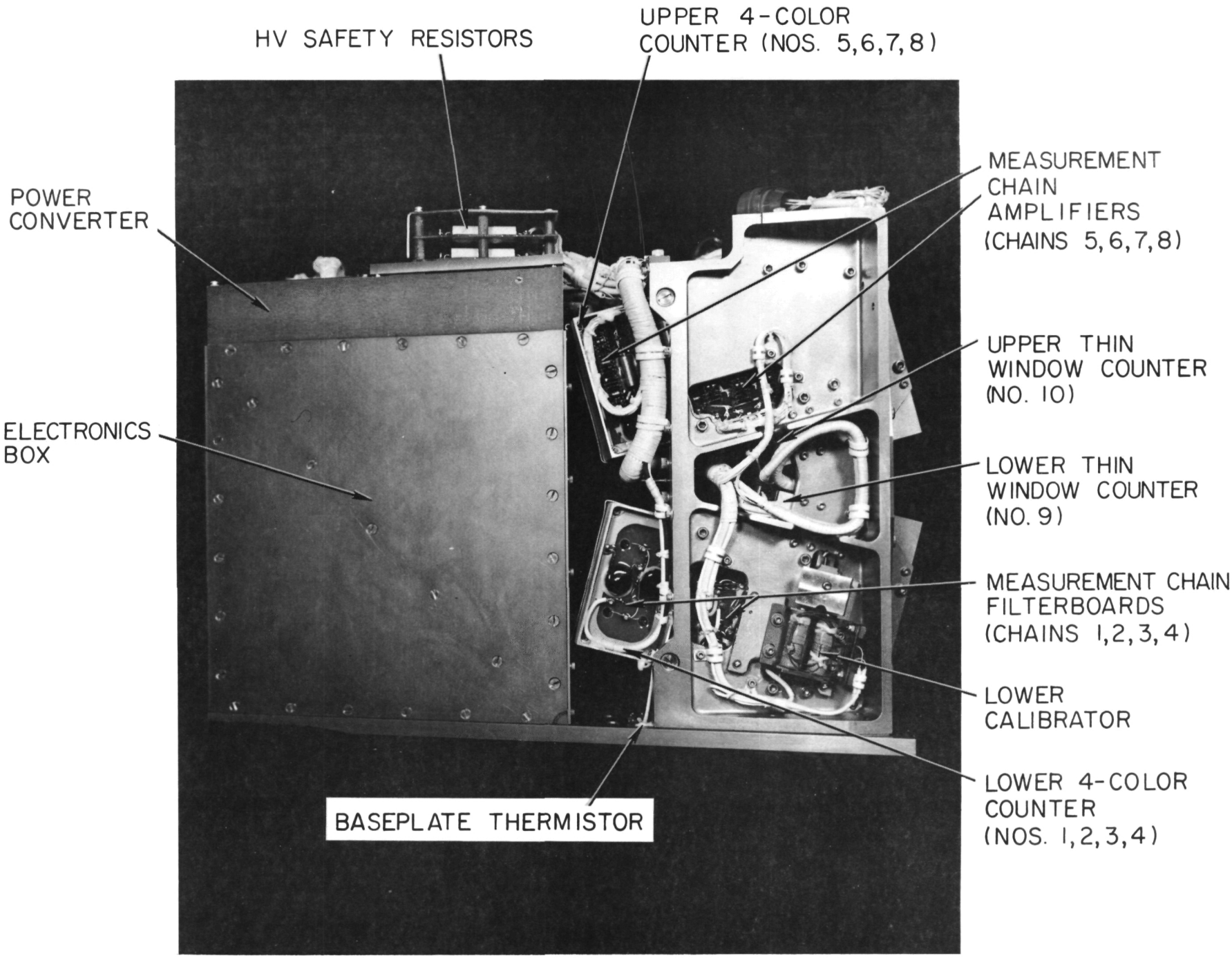

FIGURE 3-3 M. I. T. OSO-7 X-RAY INSTRUMENT. LEFT SIDE VIEW

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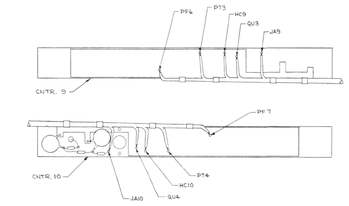
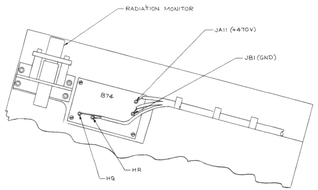
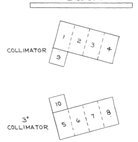
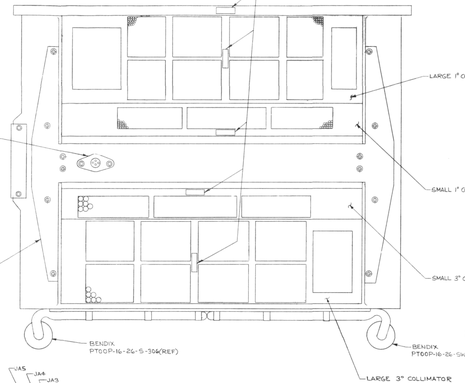
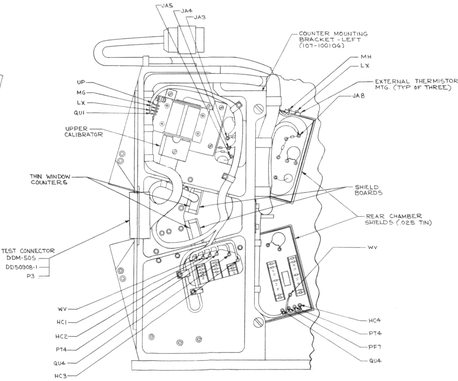




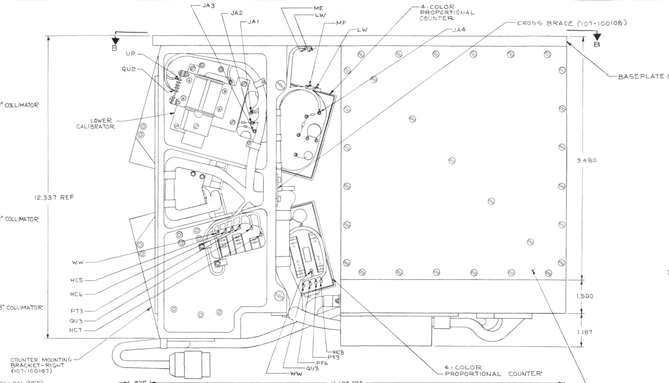
COUNTER DESIGNATIONS

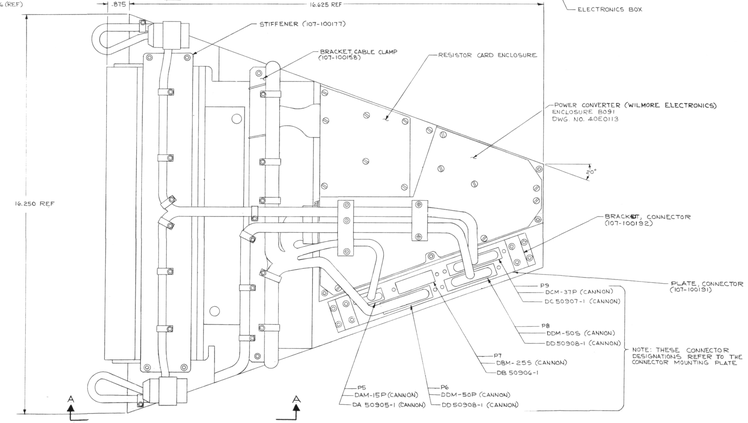


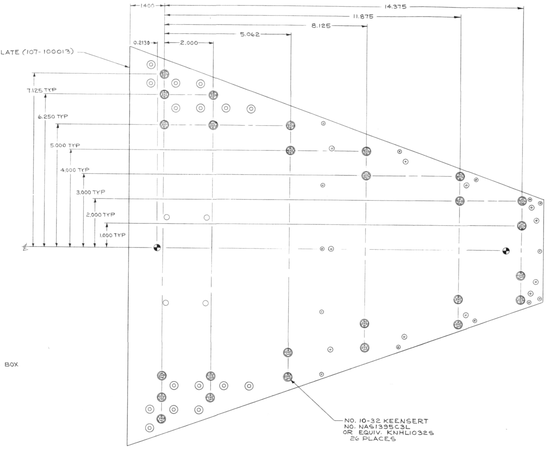




VIEW A-A







VIEW B-B

REVISIONS					
ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED

RELEASED

REV LTR	REV DATE	PART OR ASSY. NO.	NEXT ASSY USED ON APPLICATION

UNLESS OTHERWISE SPECIFIED DIMENSIONS ARE IN INCHES. ANGULAR TOLERANCES ARE IN DEGREES. TOLERANCES ON DECIMALS: TWO PLACES ± .01 THREE PLACES ± .005 FOUR PLACES ± .0005 DO NOT SCALE THIS DRAWING

MATERIAL

APPROVED — DATE

NEXT ASSY USED ON APPLICATION

DRAWN
CHECKED
ENGR APPROVAL
MFG APPROVAL

DO NOT SCALE DRAWING

SIZE	CODE IDENT NO.	DRAWING NO.
D		107-000001

SCALE — SHEET

HOMOLOGUE OF DESCRIPTION

LIST OF MATERIALS

CENTER FOR SPACE RESEARCH
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

ASSY. ELEV.
MIT. 2-14

107-000001

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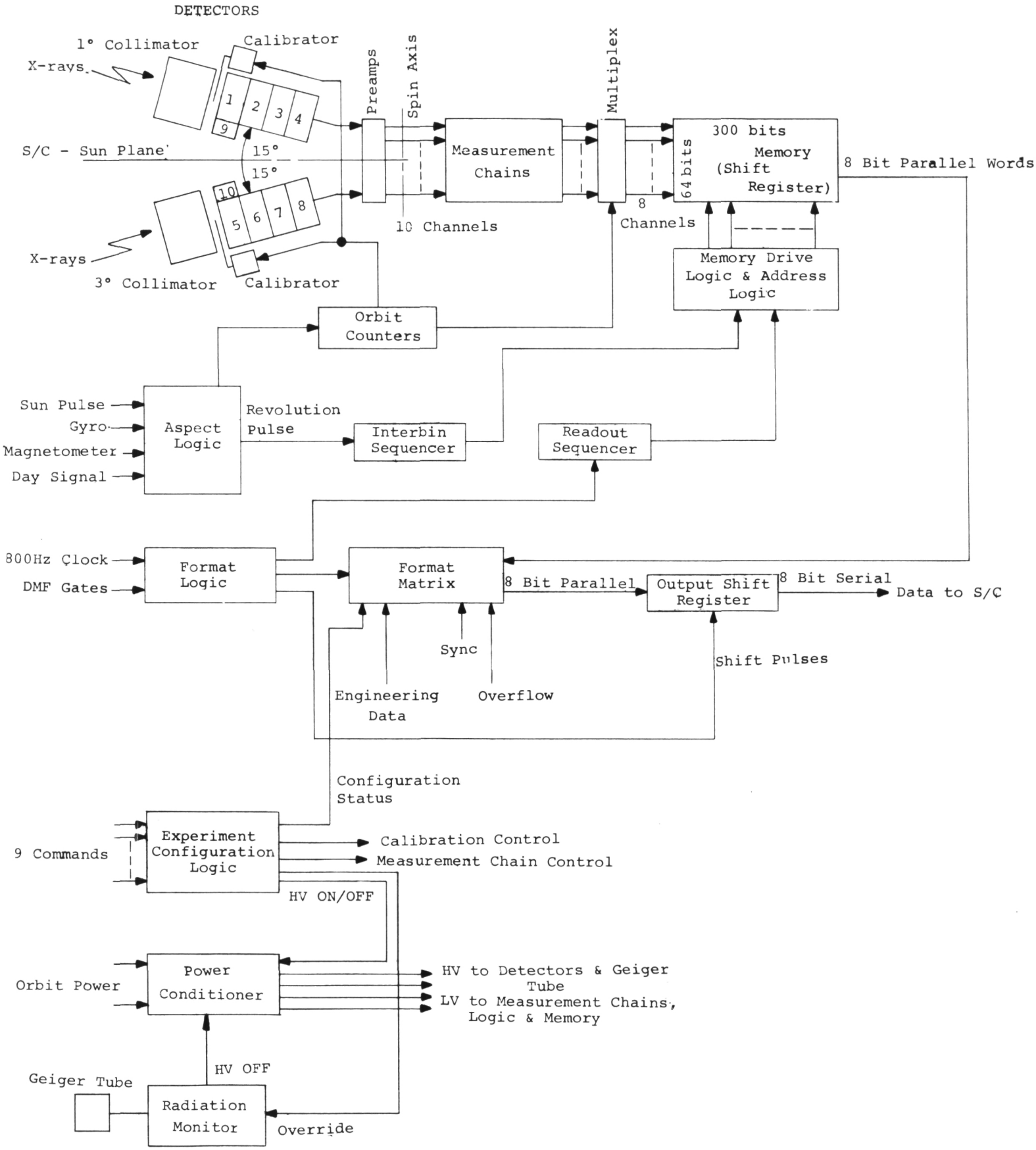


FIGURE 3-4 MIT OSO-7 EXPERIMENT SUBSYSTEMS

The report pages that follow detail the operation of these subsystems and list certain operating parameters that will be helpful to understanding and to future work.

3.1 Detectors

3.1.1 Proportional Counters

3.1.1.1 Operation - The counters are divided into two groups, each of which is comprised of a single-chamber proportional counter having an ultra-thin aluminum window and a four-chamber proportional counter. Figure 3-5 (MIT OSO-7 Counter Systems) shows the mechanical layout of the counter systems together with a tabular specification of the windows and gas fillings.

The design and successful fabrication of the four-chamber proportional counter is considered to be significant new technology resulting from this program and is identified as such for reporting under the "New Technology" clause in the MIT contract. Design of the four-chamber (or "four-color") proportional counter originated in the MIT X-ray Astronomy group from an idea by Dr. J. Stein. The counters were fabricated by LND, Incorporated, Oceanside, New York. Mr. Robert Lehnert and Mr. Peter Neyland of LND made a number of design suggestions that contributed ultimately to the successful fabrication of the counters.

The spectral response of a proportional counter is determined by the x-ray absorption characteristics of its window and gas. If $\mu_W(E)$ and $\mu_G(E)$ are the linear absorption coefficients of the window material and filling gas respectively, then the fraction $f(E)$ of x rays incident on the window with energy E, which produces pulses in the counter, is:

$$f(E) = \exp\left[-\mu_W(E)X_W\right]\left\{1 - \exp\left[-\mu_G(E)X_G\right]\right\}$$

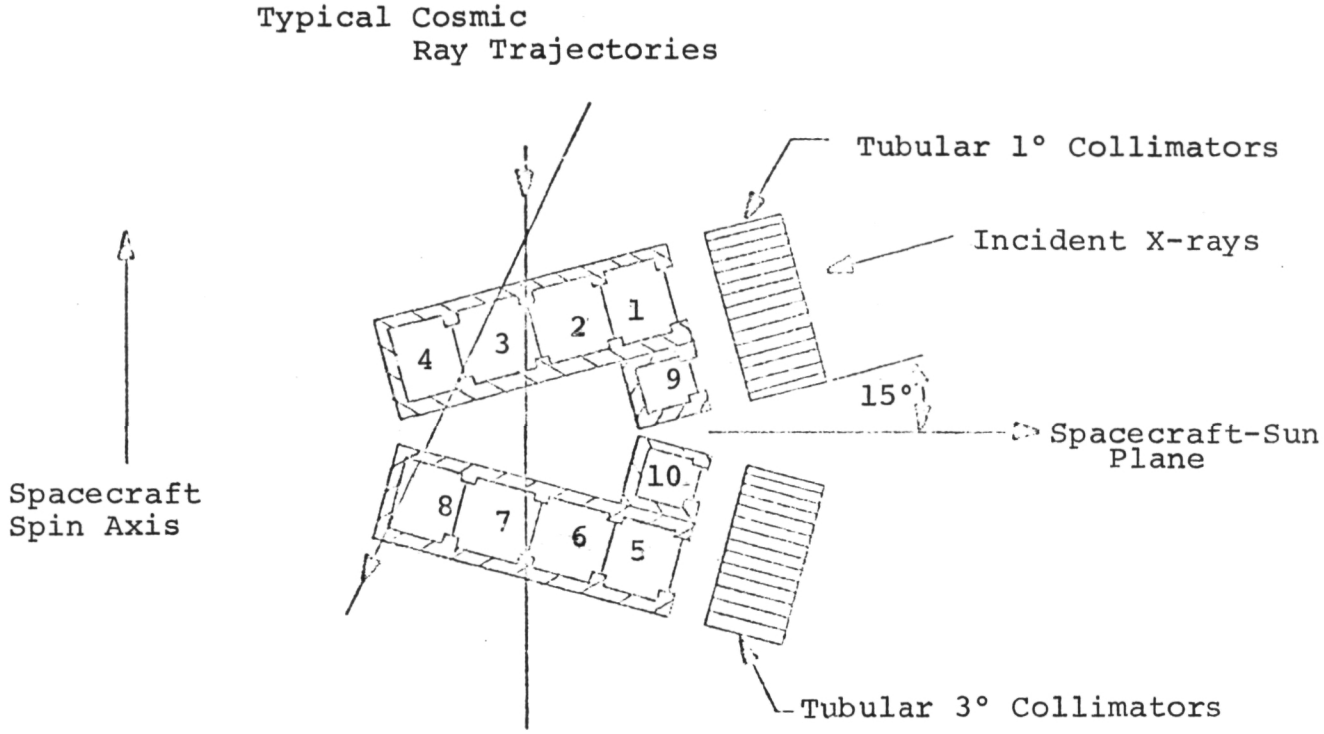
In the case of a particular chamber of the four-chamber counter, the first term in this expression which represents the window transmission becomes the product of the transmission factors for each of the windows and gas fillings between the collimator and the gas in that particular chamber. Since the x-ray mass absorption coefficient of any substance decreases with E except at the characteristic absorption edges, the window absorption generally determines the low-energy cutoff of the counter response while the gas absorption determines the high energy cutoff. The windows and gases of the four-chamber detector were selected according to this principle in order to achieve the four broad ranges of response as shown in Figure 3-6.

X rays in this energy range interact with matter most frequently by the photoelectric process whereby all the energy of an x-ray photon is absorbed in the ejection of an atomic K-shell electron. The ejected electron has an initial kinetic energy given by:

$$E = E_0 - W_K$$

where E_0 is the incident photon energy and W_K is the energy required to eject the electron from the K-shell of the atom. Under the conditions in the four-chamber counter, the electrons ejected by x rays in the 1-60 keV energy range travel only a very short distance from the site of their ejection and in this distance they lose their energy by producing a compact bunch of ions and electrons. The latter are drawn in a bunch toward the anode where they multiply and produce a fast rising pulse of negative charge. The amplitude of the pulse is proportional to the energy E of the original ejected electron.

Two principle causes of background pulses are high energy charged particles which traverse the counters and Comption interactions of high energy gamma rays. Since high energy charged



Chamber Number	Gas	Pressure	Outer Window Thickness	Window Material
1.5	N_e	1.2 ATM	.001 in	B_e
2.6	A_r	2 ATM	.010 in	B_e
3.7	K_r	3 ATM	.010 in	Al
4.8	X_e	3 ATM	.060 in	Al
9.10	N_e	1.4 ATM	.0003 in	Al

Each chamber drives a measurement chain designated by the same number as the chamber.

FIG.NO.3-5

MIT OSO-7 COUNTER SYSTEMS

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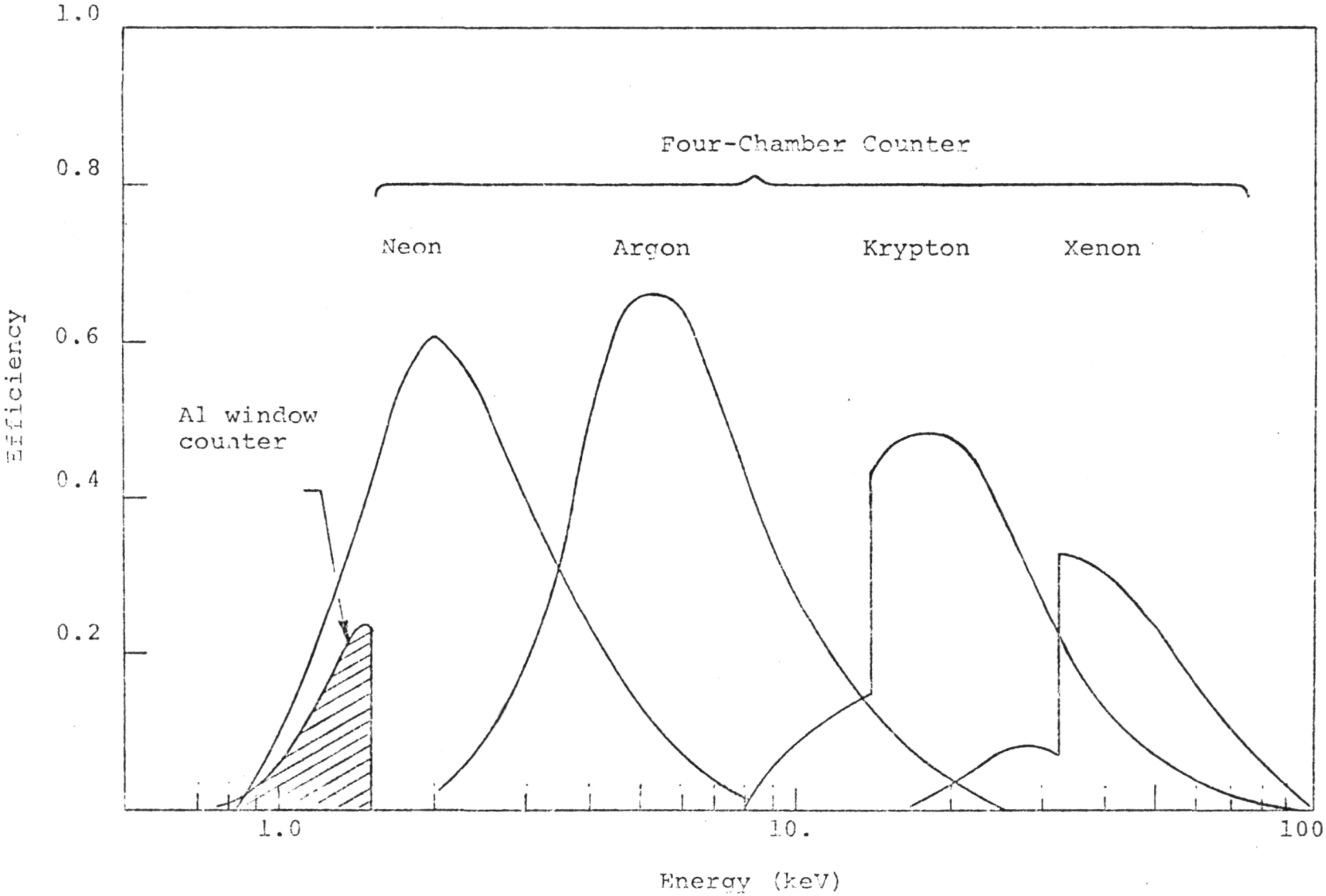

FIGURE 3-6 Calculated Spectral Response of MIT OSO-7 Counters

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particles and gamma rays are abundant constituents of primary or secondary cosmic rays at the spacecraft, measures must be taken to distinguish and surpress the background pulses they cause. Many of these background pulses have sizes outside the range expected for the desired x-ray pulses. They are effectively rejected by the upper and lower edge discriminators contained in each measurement chain.

A high energy particle that produces a pulse in one chamber is likely to traverse an adjacent chamber and produce a coincident pulse there. These events are rejected by a circuit which detects the occurrence of coincident pulses.

Energetic charged particles leave a long trail of ionization within a chamber. The electrons from this trail, therefore, have a variety of distances to travel to the counter anode which causes a spread in their arrival times and, correspondingly, a slower risetime of the resulting pulse. Such pulses from the Krypton and Xenon chambers are surpressed by risetime discriminators which distinguish them from the faster rising x-ray pulses.

The charge gain of a proportional counter is the amount of electronic charge which is eventually produced at the anode of the proportional counter when a photon or x ray of a particular energy is converted in the proportional counter. Thus, the counter, in effect, converts the energy of the x ray into an amount of charge which is directly related to that energy. The gain of a proportional counter increases with the high voltage supplied to the anode and decreases with an increase in the anode wire diameter and pressure of the counter gas. All things being equal, it is desirable to have the charge gain of the proportional counter as high as possible. This is because the conversion is quite clean with respect to noise and, thus, the gain of the proportional counter is comparable to increased "front-end" gain of the amplifying electronics. Since

these electronics contribute a certain irreducible noise level, it is desirable to have the minimum output of interest from the proportional counter appreciably greater than the noise level. Thus, by increasing counter gain, the total measurement system signal to noise ratio is improved. Since minimum signal levels in typical applications are on the order of a few millivolts on down even with satisfactory counter gains, the noise reduction requirements for the total measurement system are not trivial. Gain is limited by the fact that the counter is required to operate in a linear manner over some finite energy range. Over this range it is desired to have the output charge related to the input energy by a fixed constant K. As the gain of the proportional counter is increased, a tendency toward both gain instability and reduced linear range of operation is exhibited. In the limiting case at extreme high voltages, the proportional counter becomes a "geiger tube" and essentially complete breakdown (ionization) occurs in association with an ionizing event regardless of the energy of the incident x ray. In such a case, while the x ray is detected the measurement of energy associated with it is impossible. In the OSO-7 application, not only is the actual gain associated with a given anode important but the relative gains from anode to anode must be closely maintained since the outputs from several anodes in a given chamber of the four-chamber counter are added at the input of the measurement electronics. Identification as to the specific anode detecting the x-ray event is lost and, thus, individual variations cannot be compensated for by means of calibration. Counter gain is controlled not only by high voltage, which is constant for all anodes in a given chamber, but by dimensional control of both the anode wire and the counter chamber geometry. The governing factor in this control is the uniformity of the anode wire.

Linearity is the characteristic of the proportional counter which expresses the degree to which the conversion from photon (x ray) energy to collected charge is related by the constant independent of photon energy. Linearity of proportional counters over an energy range of approximately a decade can be obtained to a satisfactory degree. As indicated above, linearity is obtained as a result of a trade-off with charge gain.

Resolution of a proportional counter is the measure of how uniquely the energy of an incident photon can be determined. Although the charge gain can be considered a constant, the amount of charge produced from a beam of monoenergetic x rays is not the same for all events. A number of factors contribute to this lack of uniqueness. The conversion process in the gas of the proportional counter is statistical in nature. The mechanism of initial charge production and the magnitude of the initial charge vary from x ray to x ray. Special effects exist. These effects are characterized by variations in the electric field near the anode. It is in the field near the anode where "multiplication" takes place and, thus, variations here tend to significantly affect the variations in charge produced from events of the same energy. Also, since the anodes within a given chamber are connected for signal addition as indicated above, resolution is also affected by variations in gain from anode to anode. Electronic noise due to either amplifier noise or noise from the high voltage supply to the proportional counter adds to the signal on a random basis and, thus, further degrades the resolution of the particular unit. This latter noise, as indicated above, being a more or less fixed amount can be reduced in its effect by increasing the charge gain of the counter. However, electronic noise is a major factor in resolution degradation at the lower energy levels.

It is important to recognize that resolution when expressed as a number is defined in terms of resolution at a particular

energy level. It is related to the pulse-height distributions obtained from the proportional counter when subjected to a beam of monoenergetic photons. A typical pulse-height response is shown in Figure 3-7 (Pulse Height Resolution Determination). Here the peak in pulse height amplitudes associated with a beam of x rays of a specific energy E can be seen. The distribution is defined as the width of the distribution at 1/2 its maximum value divided by the energy corresponding to the peak value and is, thus, a number less than one. It is customary to express resolution in percent. It should be noted that most of the variables affecting resolution are not a function of energy. Since this is the case, it is important to discuss resolution in the context of a particular gas pressure voltage combination for the proportional counter and a particular energy of the incident x rays.

The characteristics of the four-chamber proportional counters are summarized in Table 3-1 (Four-Chamber Proportional Counter Charge Characteristics). These characteristics are entirely satisfactory for the scientific objectives of the MIT OSO-7 experiment. These are measured characterisitcs of prototype counters but the high voltages shown in this table are not those used in the Flight Instrument.

3.1.1.2 Mechanical Aspects - Figures 3-8 and 3-9 show the counter assemblies. The four-color unit is shown both assembled and in an "exploded" view. Each of the counter sub-assemblies are held together by brackets with wells that provide space close to the counter anodes for mounting the high voltage filterboards and measurement chain preamplifiers. Each counter chamber contains three 1 mil diameter anodes. Electrical connection to all three is possible at the filterboard (shallow well) end, electrical connection to one only is possible at the pre-amplifier (deep well) end. In addition to providing for mounting

Window Material	Window Thickness	Gas	Pressure	Nominal Resolution	Nominal Charge (Coulombs)	Source	High Voltage
Be	4.5 mg/cm^2	Ne-CO_2	1.2 Atm	22%	.4 x 10^{-12}	Fe^{55}	1250
Be	45 mg/cm^2	Ar-CO_2	2 Atm	25%	.1 x 10^{-12}	Fe^{55}	1730
Al	.010 in.	Kr-N_2	3 Atm	18%	.9 x 10^{-12}	Cd^{109}	2500
Al	.060 in.	Xe-N_2	3 Atm	18%	.55 x 10^{-12}	Cd^{109}	2600

TABLE 3-1 - Four-Chamber Proportional Counter Charge Characteristics

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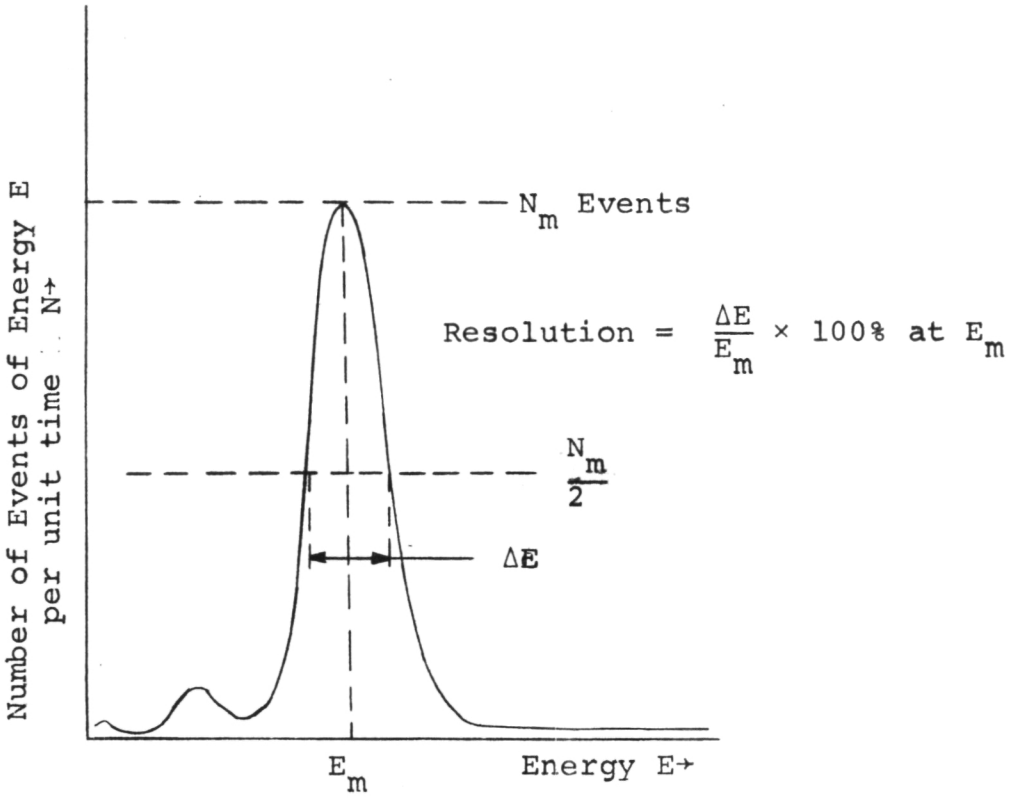

Fig. 3-7. PULSE HEIGHT RESOLUTION DETERMINATION (PROPORTIONAL COUNTER RESPONSE TO BEAM OF X RAYS OF ENERGY E_m)

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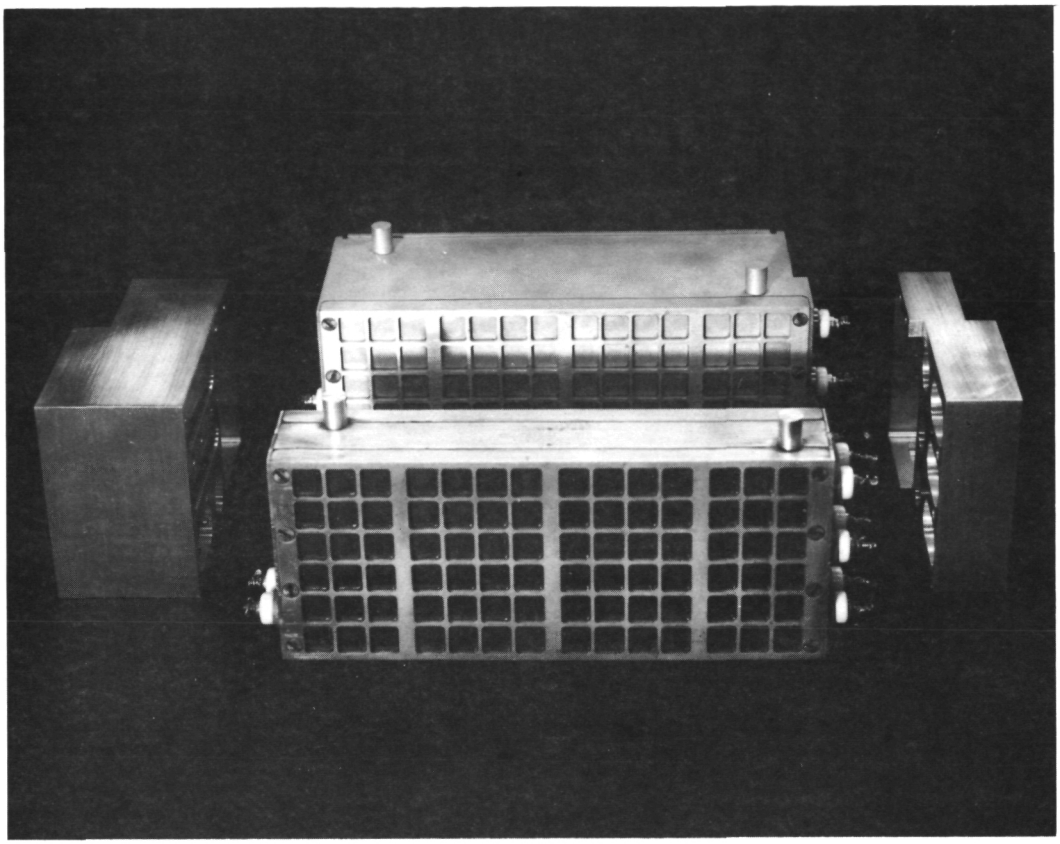
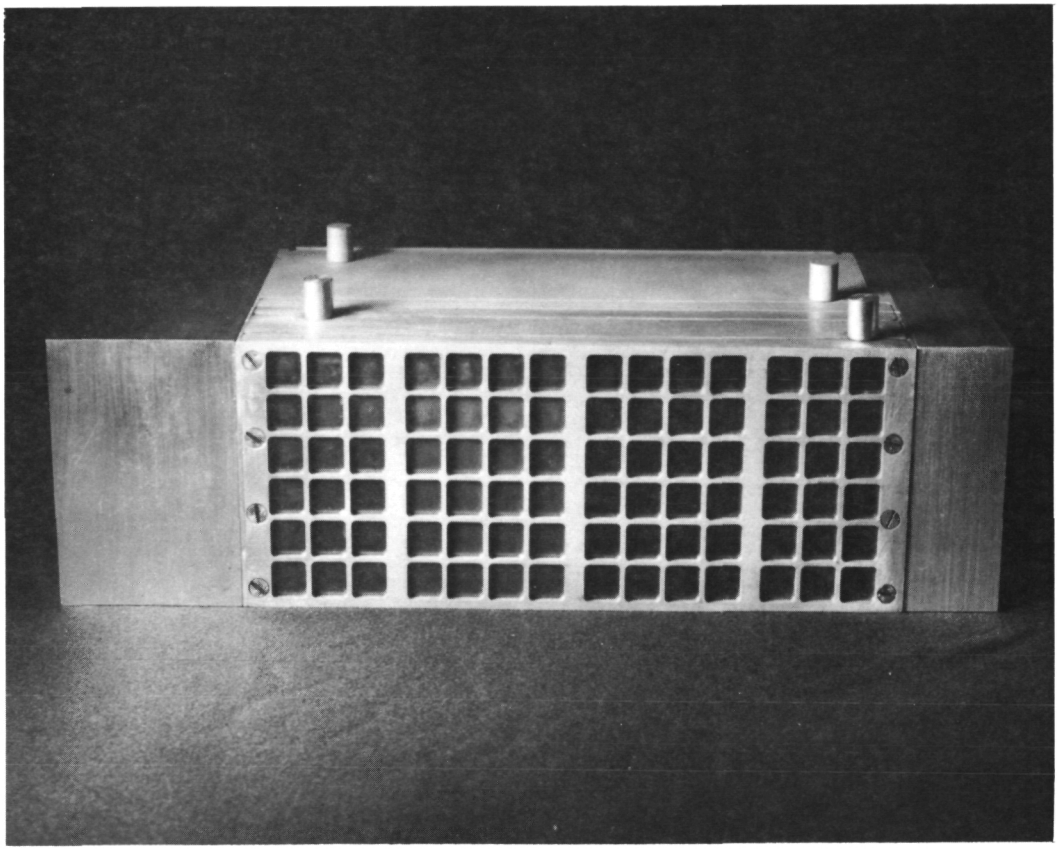


"EXPLODED" COUNTER



ASSEMBLED COUNTER

FIGURE 3-8. M.I.T. OSO-7 FOUR COLOR PROPORTIONAL COUNTER.

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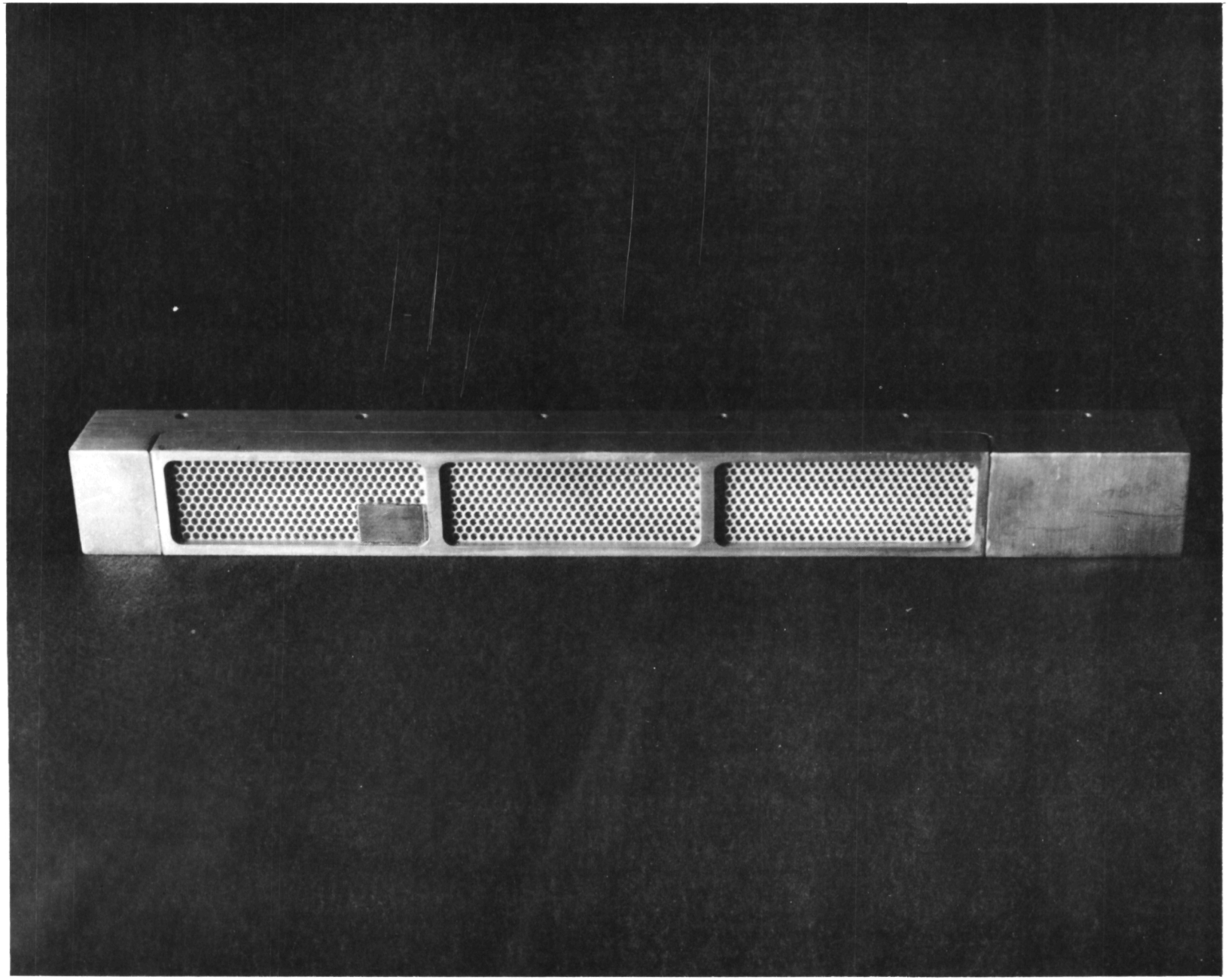

FIGURE 3–9. M.I.T. OSO-7 THIN WINDOW PROPORTIONAL COUNTER.

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the critical circuit boards close to the counter anodes, the wells provide electrical shielding in these sensitive areas.

The thin window counters contain wells in their rear surface for the same purpose. Here, the preamplifier and HV filters are combined on a single printed circuit card the same size as the rear of the counter. This card has electrical components on only one side and these components are located within the counter wells when the boards are mounted. Noise sensitivity is further reduced by the metallic shield plane mounted above the circuit board.

3.1.1.3 Design Comments

3.1.1.3-a Thin Window Counter - Strongback is provided only on the outside of the 1/3 mil aluminum window. An internal pressure of 1.4 atmospheres ensures that normal variations in atmospheric pressure and the designated extremes of test temperature will not reverse the force on the window and cause it to collapse. In the initial design, strongback was used on both sides of the window. This design modification eliminated the internal-external strongback alignment problem (which caused a 10 to 20 percent loss in detection efficiency) and simultaneously increased the effective window area by providing a more efficient hole pattern than was available in the original material.

3.1.1.3-b Four-Color Counter - The four-color counter once was a single mechanical subassembly. The design was changed because continuing fabrication problems made unlikely the delivery to MIT of two fully operational units in time for flight instrument assembly. Apart from breaking the unit into two-chamber pairs, seal lengths were increased wherever possible to improve the reliability of the fabrication process. The cost of the change was an increase

in weight of about 1/2 pound per unit and a decrease in window area of about 10%. Neither cost was unacceptable in view of the possibility of flying a partially functioning four-color counter.

This design change was incorporated late in the program--in fact, after vibration testing of the prototype instrument was complete--and its adoption is considered to be a significant milestone in meeting the full objectives of the program.

3.1.1.4 Operating Voltages - Operating voltages for these counters were chosen to be as high as possible for best gain and resolution while avoiding nonlinearity and breakdown effects. The final values are shown in Table 3-2.

Table 3-2 Proportional Counter Operating Parameters

Counter Number	Pressure (ATM)	Gas Fill	Operating Voltage (Volts)	Safety Resistor (MΩ)	Resistor Voltage Loss (volts)
1,5	1.2	Ne-CO_2	1320	5000	10*
2,6	2.0	Ar-CO_2	1920	5000	10*
3,7	3.0	Kr-CO_2	2510	1000	<5v*
4,8	3.0	Xe-CO_2	2470	1000	<5v*
9,10	1.4	Ne-CO_2	1320	5000	10

As each of these counters is protected by a high voltage safety resistor (Section 3.6.3.2), the actual operating voltage is somewhat lower than these values due to internal and surface leakage currents in the filterboard printed circuit cards. The approximate values of these voltage losses are shown in this table as well.

*Estimate based on calibration spectra with and without resistors.

3.1.1.5 Unusual Operating Characteristics - Certain of the on-board counters exhibited nonstandard operating characteristics. These are summarized below.

Counter 8: Breakdown effects were not avoided entirely at these voltages. One Xe-CO_2 counter (Counter 8) was observed to breakdown ("glitch") such that the gain dropped significantly for various periods as high as 36 seconds (average 16.5 seconds) with an average rate of 8.4 per hour independent of temperature. This was traced to picoampere level discharges along the high voltage insulator surfaces inside the counter. Due allowance will be made for these discharges in the reduction of data from this counter.

Counters 1, 5, 9, and 10: Preamplifier overload caused by huge counter pulses is responsible for certain "extra" counts observed above the high level discriminator cutoff voltage in spectra obtained from these chains. Due to the capacitive coupling between stages in the preamplifier, a second pulse is generated for each input pulse above the preamplifier overload point. The second pulse is not eliminated by the measurement chain high level discriminator because of its long duration compared to a true counter pulse. This effect is most noticeable in Chains 9 and 10. The rate of occurence of these overload pulses in Chains 9 and 10 was determined to be 0.3 ± 0.01 per second which is not significant compared to the expected background.

Counter 3: For reasons which are presently unknown, this counter alone among the tested Kr-CO_2 counters exhibited a 100% gain change over the tested temperature range. Counter gain at 0°C is 1/2 its +30°C value. Gain at the operating temperature of 10-15°C is acceptable and has proven to be stable with time. "Glitching" similar to that observed in Counter 8 was seen twice in this counter. The actual rate was too low to be determined accurately but the same precautions will be taken in data reduction.

3.1.2 Collimators

3.1.2.1 Description - The collimators define the fields of view of the detectors. They are assemblies of uniform cylindrical tubes close-packed in hexagonal arrays. The tubes are of coin silver which has nearly optimum absorption characteristics for 60 keV x rays. The angular transmission functions of these collimators are approximately conical in form with maxima of about 80% or within a few percent of the theoretical efficiency.

Angular response characteristics of the collimators are available in the MIT x-ray calibration notebooks (see Section 4.3.2).

3.1.2.2 Design Comments - Originally, the collimators were of honeycomb cell design. Fabrication was achieved by a two-step process; forming of the metal strips which become the honeycomb and welding of the strips together to form the cells on a row-by-row basis. Few problems were encountered in forming the 3° collimators in this fashion but many in the 1°. One degree samples came only within 10 to 20 percent of the theoretical x-ray transmission efficiency.

This was of serious concern but not calamitious. Much more serious was an angular broadening of the response fucntion due to nonparallel cells.

Severe limitations on the capability of the instrument to resolve weak sources would be incurred by the use of a collimator with such characteristics.

Alternative approaches were, therefore, considered. Professor Clark suggested the accepted approach using hexagonal arrays of readily available uniform coin silver tubes epoxied into a MIT fabricated frame. The self-aligning characteristic of the precisely manufactured tubes makes assembly easy, if repetitious, work and assures a good collimator will result without any need of special and precise assembly jigs.

This collimator design is considered to be new technology and is so reported under the requirements of the MIT contract.

3.1.3 Measurement Chains

3.1.3.1 Description - The measurement chains perform two major functions. These are: a.) linear pulse shaping, and b.) logical identification of x-ray events. A typical measurement chain is shown in Figure 3-10. There are ten such measurement chains in the experiment, one for each proportional counter chamber.

To produce a "logical" x ray for accumulation, the proportional counter signal must meet the following requirements:

a. The pulse amplitude must exceed the level setting of the low-level discriminator.

b. The pulse amplitude must not exceed the level setting of the high-level discriminator.

The voltage output of a proportional counter is typically a few millivolts. The preamplifier and amplifier amplify this signal to the operating range of 0 to 5 volts to provide a pulse which can be processed easily in the remainder of the circuitry. It is important that the amplifier have sufficient bandwidth to pass the proportional counter signal without distortion.

Both level discriminators produce an output pulse when their level setting is exceeded.

It can be shown that if the proportional counter signal has an approximately exponential rise then after it passes through two R-C differentiation circuits, it will cross zero after a time interval which depends on the risetime but not on the amplitude of the original signal. As explained earlier, background signals caused by energetic particles generally have longer risetimes than x-ray signals. They can, therefore, be surpressed by the "risetime discriminator" which senses the zero crossing time and produces an output pulse whenever this time is greater than a certain preset amount.

The complete logical condition for acceptance of an event as an x ray is an output pulse from the low-level discriminator (LLD) without a veto pulse from the high-level discriminator (HLD), the risetime discriminator (RTD), or the anticoincidence network (AN). Note, however, that the HLD, RTD, and AN must wait for signal risetime and the AN must, in addition, wait for the electrons released by the charged particle to arrive at the counter anode. Delaying the LLD pulse by a few microseconds allows time for the other networks to operate. This is accomplished by the timing network (TN). The output gate is arranged to provide an x-ray indicator corresponding to the logical condition above and only after the delay determined by the TN has elapsed.

The anticoincidence network provides an output pulse whenever more than one low-level discriminator is fired. Its output is fed to the output stages of each measurement chain to prevent any x-ray indicators from appearing under this condition.

3.1.3.2 Design Comments - Although the OSO-7 Measurement Chain System operates well and meets the original specifications, a number of changes could be made to improve the system. One particular comment applies to the measurement chain as a whole: most of the logic functions could have been realized in 9040 series DTL logic at a considerable savings in design time, fabrication time, and packaging volume had the instrument power budget been increased earlier in the program.

1. Preamplifier and Amplifier

   a. The basic two-transistor gain stages could be modified slightly to provide increased bandwidth through a different biasing configuration. Had bias control of the first transistor been derived from the emitter of the second, better pulse shape discrimination would have resulted.

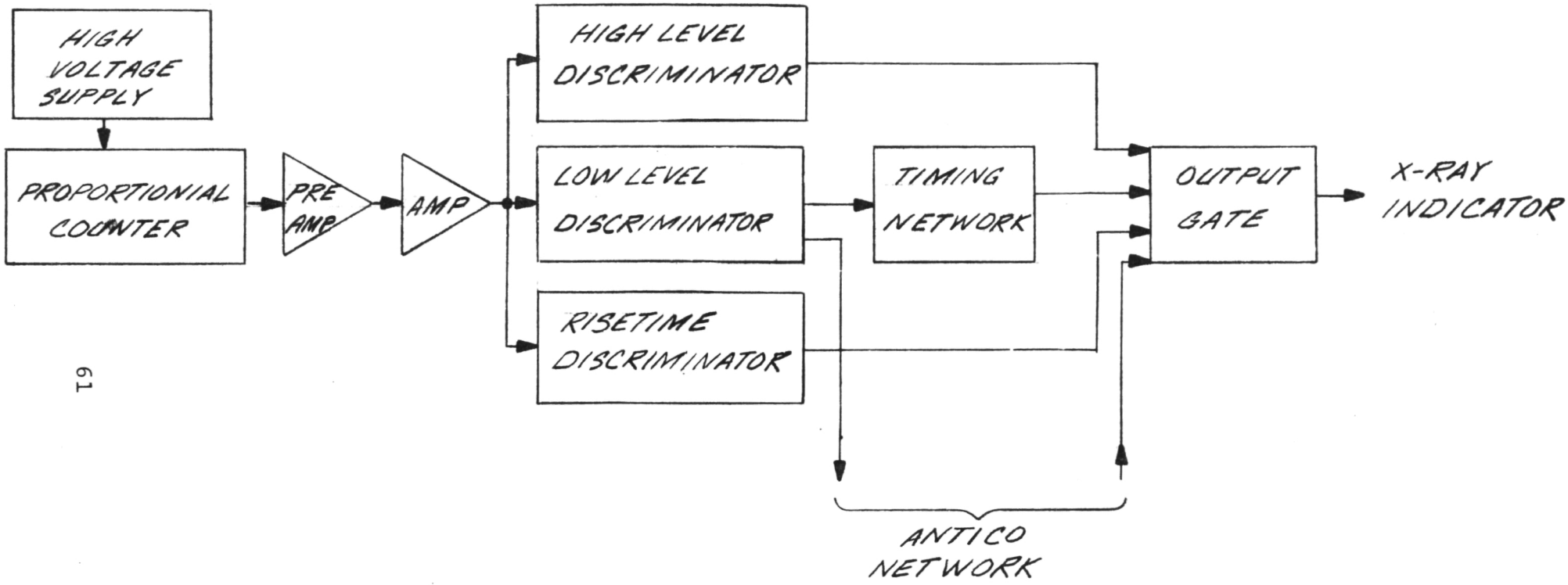

FIGURE 3-10

TYPICAL MIT MEASUREMENT CHAIN

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b. The amplifier output stage should have been designed to provide increased cable driving capacity. This would have eliminated the need to have extremely short GSE cables during ground test.

2. Low Level Discriminator

A fault existed in the design of the original LLD input circuitry that caused a shift in discrimination level immediately following a large pulse. This was due to charging of the large input coupling capacitor through the saturated first transistor of the LLD. At the time this problem was isolated, a first printed circuit layout for this module was complete and layout changes were undesirable. A solution was found in reducing the time constant of the input network to 13 μs to allow the system to completely recover in time for the next count. This fix resulted in pulse shaping which slightly reduced the amplitude of each pulse according to capacitor value. Because of the tolerance of the capacitors, each of the LLD's now fired at a different pulse height even though they were set identically. This caused a lengthy calibration stage later in the program. A further effect was the different treatment of background events and x-ray events since their pulse shapes are sometimes different. This effect is considered small and, in any case, all x rays have the same risetime (pulse shape) in the energy range of interest and, therefore, are treated identically by the LLD.

An additional error was made in the use of tantalum capacitors in the input circuit resulting in a temperature dependent firing point. These capacitors were subsequently changed causing a slight program delay. All of these problems could be avoided by redesigning the LLD to be similar to the zero crossing detector which was configured later in the program.

3. High Level Discriminator

Same comments apply as for low-level discriminator.

4. Output Gate

This module in particular could be greatly simplified by the use of DTL logic elements.

5. Zero Crossing Detector and Driver

Improved temperature stability might be attained utilizing the -6v supply for negative bias.

6. Background Detector

The risetime pulse (triangular) should be routed through buffers to the output test connector for simplified setting and testing of the risetime discrimination system.

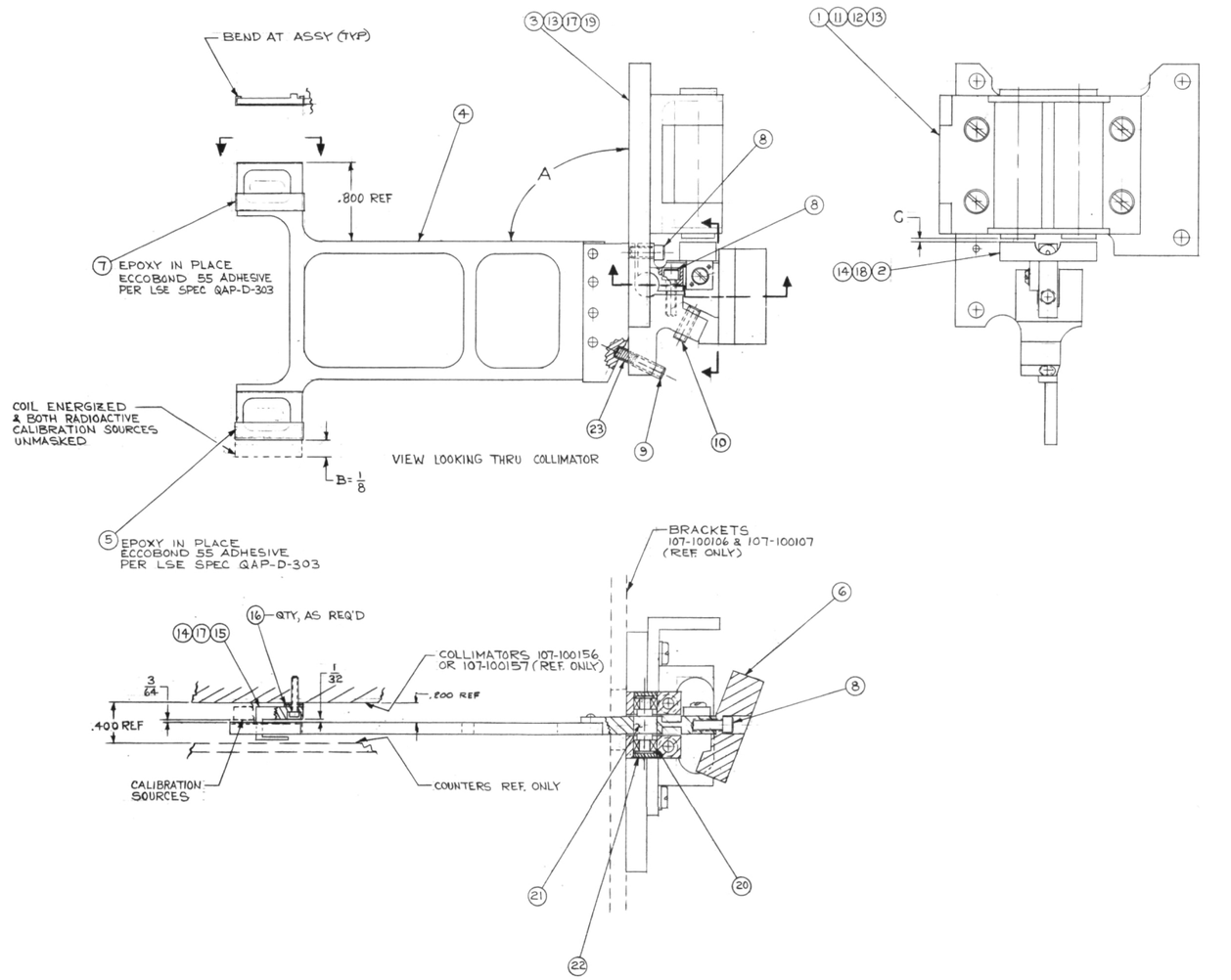
3.1.4 Calibrators - In-flight calibration is achieved with radioactive x-ray sources mounted in the collimator assemblies. The sources are covered with shutters which open automatically once every 32 orbits and expose all the counter chambers to x radiation at rates that are twice the natural background counting rates. These sources aid in monitoring the energy response and absolute efficiency of the counters. Counters 1, 2, 3, 4, and 9 are calibrated during orbit zero. Counters 5, 6, 7, 8, and 10 are calibrated during orbit one.

3.1.4.1 Mechanical Features - Electronically, the shutter assembly is simple. Mechanically, it is quite sophisticated. MIT drawing 107-000104 (overleaf) details its features.

The shutter arm is located between the counter face and collimator rear surface. The calibration source and a fiberglass retainer (Item 15 in the drawing) are attached to the back of the collimator.

The retainer serves to constrain the motion of the outboard end of the arm during vibration and determines the rest and activated arm locations. Its use eliminates any possibility of the arm tip impacting the window surface of the 1 mil beryllium counter which is less than a 0.3 cm (0.1 ") from the arm. The bearing surfaces of the retainers are coated with a few mils of solithane 113-300 for shock absorption. A ball bearing pivot (20, 21, 22) is used and the shutter arm is balanced on the

REVISIONS						
ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED
	A	REVISED & REDRAWN ITEM #5 WAS 107-100138, ITEM 7 WAS BENDIX PIVOT 6048-600, ADDED ITEMS 9, 13, 20, 21, 22 & 23, QTY ITEM 12 WAS 6, QTY ITEM 13 WAS 6	R.F.		1/20/71	



FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION
REF	4	107-100214	WASHER	
23	1	107-100210	SPRING	
22	2	107-100208	BEARING CAP	
21	1	107-100207	SHAFT	
20	2	6418 WITH TYPE L4B	BALL BEARING	MPB CORP
19	4		WASHER, STD #2	STN. STL.
18	1		SOC. HD. SCREW, NYLOK 2-56 x 1/4 LG	NYLON
17	5		SOC. HD. CAP SCREW, 2-56 x 3/16 LG	STN. STL.
16	5	107-100184	SHIM SHUTTER ARM	
15	1	107-100169	RETAINER, SHUTTER ARM	
14	4		DOWEL 3/32 DIA x 1/4 LG	STN. STL.
13	6		DOWEL 1/16 DIA x 1/4 LG	STN. STL.
12	8		WASHER, STD #4	STN. STL.
11	4		SCREW, BIND. HD 4-40 x 3/16 LG	STN. STL
10	1		SOC. SET SCREW 4-40 x 3/16 LG	STN. STL
9	1	107-100209	#4-40 SET SCREW	
8	3		SOC. SCREW 4-40 x 3/16 LG	STN. STL
7	1	107-100212	SHUTTER #2	
6	1	107-100167	COUNTERWEIGHT	
5	1	107-100211	SHUTTER #1	AL
4	1	107-100137	SOURCE, SHUTTER ARM	AL
3	1	107-100129	MOUNT, PIVOT	AL
2	1	107-100123	ARMATURE	
1	1	107-000102	MAGNET ASSY	

LIST OF MATERIALS

RELEASED

UNLESS OTHERWISE SPECIFIED CAPACITOR VALUES ARE IN μf RESISTOR VALUES ARE IN OHMS ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± # ± .# ± # DO NOT SCALE THIS DRAWING

MATERIAL #

NEXT ASSY | USED ON APPLICATION

CENTER FOR SPACE RESEARCH
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

DRAWN R.F. 3/11/70
CHECKED
APPROVED
APPROVED 1/20/71

MIT APPROVED # DATE #

CALIBRATION SOURCE SHUTTER ARM PIVOT ASSEMBLY

SIZE E | CODE IDENT NO. # | DRAWING NO. 107-000104

SCALE 2/1 | SHEET 1 OF 1

107-000104 A

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pivot axis and on the axis in the plane of the arm to minimize bearing stress during launch. Brass core caps are secured to the solenoids to guarantee that some gap will remain between the armature and pole pieces should the arm stops move or wear and thereby prevent the shutter arm from locking magnetically in the open position. Air gap and spring tension are preadjusted to cause the arm to move open at about 5.0 volts and to spring shut at about 1.5 volts.

3.1.4.2 Design Comments - Turning to ball bearing pivots from the Bendix flex pivots originally used complicated the design somewhat but alleviated concern over the ability of the flex pivot to withstand the vibration levels expected (a flex pivot failed during qualification testing). The higher strength of the bearings also eased the balance and low tip mass requirements on the shutter arm. The present arm design is probably as reliable as any mechanical shutter assembly can be. Electronic calibration schemes using sources outside the normal range of the measurement chain discriminators would probably be used in similar circumstances in the future.

3.2 Data Control Logic

This subsystem (referenced elsewhere as the Data Acquisition System - DAS) controls the flow and storage of data within the instrument. Each spacecraft wheel revolution is timed by the MIT instrument using one of three aspect pulses supplied by the spacecraft as reference. The Aspect Logic (Section 3.2.1.1) chooses which pulse. The timed rotation of the spacecraft is converted into 256 timed bins by the Bin Width Logic (BWL) (Section 3.2.1.2). X-ray pulses which occur during each bin interval are accumulated and cataloged by counter and bin number in the memory. Readout of data from that catalog location causes accumulation to begin anew. The length of the MIT

data format (Section 3.3) sets the interval between readouts at 190.08 seconds. As there are 256 bins, the accumulation time per bin is 0.75 seconds.

3.2.1 Aspect Determination

3.2.1.1 Aspect Logic - The control pulse for the Bin Width Logic, the Revolution Pulse, is developed in the Aspect Logic. Three rotational reference pulses are supplied by the spacecraft:

1. Sun Pulse: from the wheel sun eyes,
2. Gyro ("Aspect") Pulse: from the magnetic "blipper" on wheel passing under sail,
3. Magnetometer Pulse: from the wheel magnetometer sensing the Earth's magnetic field. The sensor generates one pulse every time the sensor radial vector passes through magnetic north.

All of these pulses are sampled and a choice made between them according to Table 3-3.

Table 3-3 Truth Table for Aspect System

Sun Pulse Received	Magnetometer Pulse Received	Aspect Pulse Received	Day Pulse	Aspect Output Corresponds to:
0	x	0	0	Magnetometer
0	x	0	1	Magnetometer
0	x	1	0	Aspect
0	x	1	1	Magnetometer
1	x	0	0	Sun
1	x	0	1	Sun
1	x	1	0	Sun
1	x	1	1	Sun

The Revolution Pulse is generated at the leading edge of the chosen reference pulse. The Sun Pulse is the primary day reference and the Gyro (or "Aspect") pulse,the primary night reference. Automatic failure or backup modes using Magnetometer or Gyro pulses are provided. The pulse being used can be identified from the experiment housekeeping data.

3.2.1.2 Bin Width Logic

1. Description - The Bin Width Logic is shown in Figure 3-11. The period of each revolution is measured by the Prescaler and 13-bit Revolution Counter and from this the bin width to be used during the next revolution is determined. Since the Prescaler and the Revolution Counter count a 500 KHz clock, the number stored in this combination at the end of a revolution is the number of 2 microsecond intervals in that revolution. The number stored in the 13-bit Revolution Counter is 1/256th of that value or the width of a single bin.

This number is transferred to the Bin Width Register by the RC-BWR Transfer Gates upon command of the Revolution Sequencer, which controls system timing at revolution starts. When the transfer is complete, the Revolution Counter is cleared and counting for the next revolution begins. The contents of the BWR are then transferred to the Bin Width Counter (BWC) and bin width counting is started. To avoid the requirement of reverse counting capability in the BWC (that is, insert the bin width and count down to all outputs low), the complement of the bin width is placed in the BWC and counting done in the normal (count up to all outputs high) manner. While the methods are logically equivalent, this approach is more efficiently implemented with the logic elements used in the instrument. The BWC counts the same 500 KHz clock as the Prescaler and Revolution Counter. A bin end gate identifies the "all-ones" condition in the BWC and flags the end of the bin.

The BWR holds the bin width count for the entire revolution. All further transfers from the BWR to the BWC during the revolution are handled by the Interbin Sequencer and BWC Recycle Sequencer that control the system during bin starts.

At the end of a revolution (identified by the next Revolution Pulse), the Revolution Counter stops immediately. The Prescaler continues operating to provide timing signals to other parts of the system. It is never reset.

3.2.1.3 Bin Width Logic Errors - The bin width determined by this system is not precisely 1/256th of the revolution period. The following factors are responsible for the discrepancy between the estimate and the exact division.

1. Round-off Error - The 8-bit Prescaler and 13-bit Revolution Counter accumulate N counts between Revolution Pulses. This may be expressed as:

$$N = 256\ B + R \qquad R \leq 255 \tag{3-1}$$

where B is the number of counts per bin and R is the remainder. Rewriting,

$$B = \frac{N}{256} - \frac{R}{256} \tag{3-2}$$

Since $R_{max} = 255$, the round-off error makes all bins short by less than one count in all instances.

$$B = \frac{N}{256} - \frac{255}{256} \cong \frac{N}{256} - 1 \tag{3-3}$$

The clock frequency (500 KHz) has been chosen to make this round-off error less than 1/10 of a bin over a revolution. The worst case situation involves the shortest revolution period, $T_R = 1.5$ seconds.

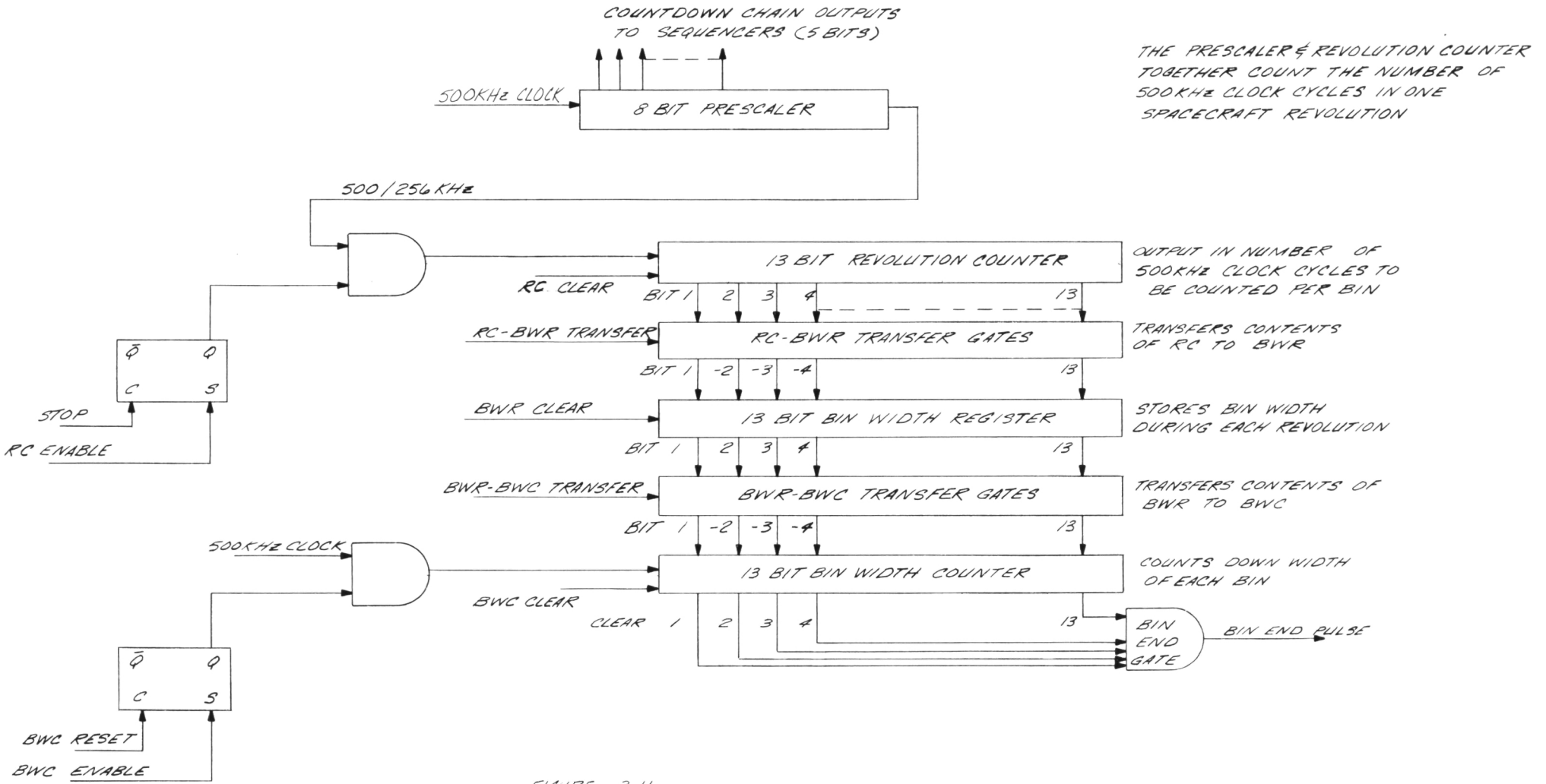

FIGURE 3-11
BIN WIDTH LOGIC

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$$N = 1.5 \times 500 \times 10^3 = 7.5 \times 10^5 \text{ counts}$$

and

$$B = \frac{7.5 \times 10^5}{256} = 2929 + \frac{176}{256} \text{ counts} \qquad (3\text{-}4)$$

The maximum round-off error (E_R) is 1 in 2930 per bin or $E_R = \frac{1}{2930} \times 256$ accumulated over the revolution.

$$E_R = 0.087 \text{ max}$$

over a revolution.

2. Prescaler Carryover - The Prescaler must run continuously to provide clock signals for the various sequencers in the instrument. It is, therefore, not reset at the start of each revolution and revolution counting begins with some arbitrary number in the Prescaler. If the sum of the arbitrary number and remainder is greater than 256, an extra count is added into each bin.

3. Last Bit High Logic Error - Should bit 8 of the Prescaler happen to be high when the Revolution Counter is enabled, an extra count will be added to each bin since the Revolution Counter cannot differentiate between clock and logic signal transitions.

4. Error Summary - In terms of clock counts per bin:

	Maximum	Minimum
Round-off Error	0	-1
Prescale Carryover	+1	0
Last Bit High	+1	0
	+2	-1

It is possible for the bin count to vary +2, -1 count with a stable rotation period. The tendency is for the bins to be too long with a maximum overlength of two counts per bin. As this error accumulates over the revolution, an uncertainty in bin look angle of +17.4% - 8.7% at the end of the revolution results. Since the tendency is for bins to be too long, the last bin will generally be cut short by the Revolution Pulse. For data from this bin to be transferred into memory during accumulation, the next Revolution Pulse must occur after a portion (16 μs) of the final interbin sequence has been completed (see Section 3.2.2). Of the four possible bin counter error situations (+2, +1, 0, -1) only the (-1) situation ensures completion of the data transfer. It would, therefore, be expected that in the presence of stable rotation the background count rate in the last bin would run no more than 25% of the rate in the other bins. The presence of a drifting or jittering rotation rate would change this figure significantly.

5. Converting to Time Units - The actual clock frequency in the instrument is 499.3 KHz at room temperature. To obtain the bin width interval precisely, multiply the telemetered bin count by 2.002 μs not by the nominal value of 2.000 μs. Variation in clock frequency with temperature is less than 1 Hz/°C. Variation with voltage is less than 1 KHz/volt. Voltage variations in the normally operating instrument are less than 0.05 volts.

6. Data Dead Bands - There are short intervals at the start of each revolution and bin in which data is not collected.

Revolution Start - This dead band assumes values between 729 and 863 μseconds. Revolution counting begins at the end of this dead band. It is, therefore, 360° of wheel rotation less the dead band

sector in degrees (a function of rotation rate) that is sectored by the instrument. As the length of this dead band is about 0.1° at a rotation period of 2.0 seconds, it must be considered in the determination of source location.

Interbin Start - This dead band assumes values from 14 μs to 29 μs and is noncumulative over the revolution. This represents less than 1% of a bin, is negligible in terms of data loss, and does not enter into positional calculations.

3.2.2 Sequencers and System Timing - Five sequencers are required to control system timing and data transfers. Each is associated with an instrument event (i.e., revolution start) and all are interlocked to prevent race conditions when more than one is operating at a time. Interlocking is achieved by tying all of the sequencers to a common 32 clock pulse cycle. All sequencers operate from or are locked to the 32 μs cycle defined by the first five bits of the instrument Prescaler.

3.2.2.1 Revolution Sequencer - The Revolution Pulse activates this sequencer. The sequencer interrupts any system functions that may be in process at the end of the revolution, resets all logic systems, clears various counters in the Bin Width Logic, initiates the high speed advance to the first bin (Bin 0) and performs the data transfers attendant to the start of the first bin.

3.2.2.2 Interbin Sequencer - This sequencer is activated by the Bin End Pulse from the Bin Width Logic. It controls data transfers during interbin intervals and activates the Readout Sequencer if appropriate. Should this sequencer, for any reason, be unable to complete its cycle,data accumulated during the previous bin will not be transferred to memory and is lost.

3.2.2.3 BWC Recycle Sequencer - The Bin Width Counter Recycle Sequencer clears and restarts the BWC during interbin intervals. It is started by the Bin End Pulse and completes its cycle at the start of the next bin. The Bin End Pulse is arranged to occur 10 μs before the true end of the bin to provide for the recycle operations. In this way, cumulative errors in bin position due to sequencer dead times are avoided.

3.2.2.4 Memory Index Sequencer - The memory is required to advance at two rates; the bin rate and an address search ("high speed") rate. Memory control in the high speed mode is provided by this sequencer. It operates only until a requested address is located. Operation is initiated by the Revolution or Readout Sequencers as appropriate.

3.2.2.5 Readout Sequencer - Data transfer from the memory to the Format Logic and the memory clearing function are handled here. The sequencer is controlled by the Format Logic request for a readout and by a signal from the Memory Index Sequencer that the readout address has been reached.

Interlocked sequencer timing is the essential design characteristic of this system. Without it race conditions between sequencers would cause intermittent data loss, erratic data accumulation and unreliable system timing. Sequencer timing and interlocking is shown in MIT drawing 107-800012 (overleaf).

3.2.3 Data Accumulation and Storage

3.2.3.1 Memory and Accumulators

1. Operation - When an x-ray event is identified by one of the eight monitored measurement chains, a single level pulse is generated. The event pulse is counted in an eight-bit serial binary accumulator identified with the particular chain. Events are accumulated for the duration of a bin.

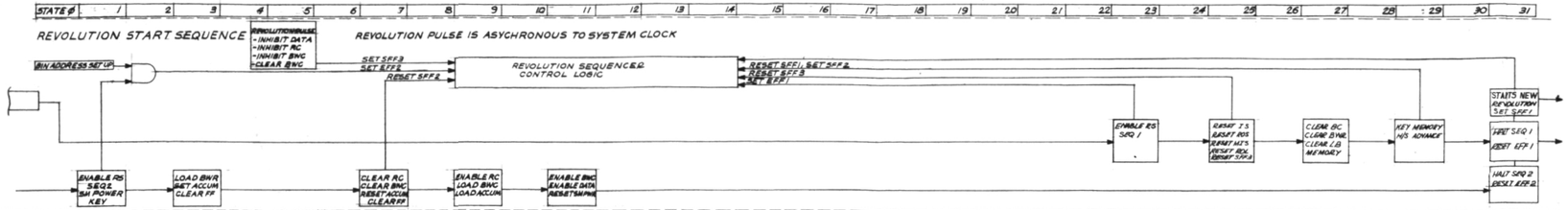
REVISIONS					
ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED

OUTPUT STATES OF THE 5 BIT PRESCALER

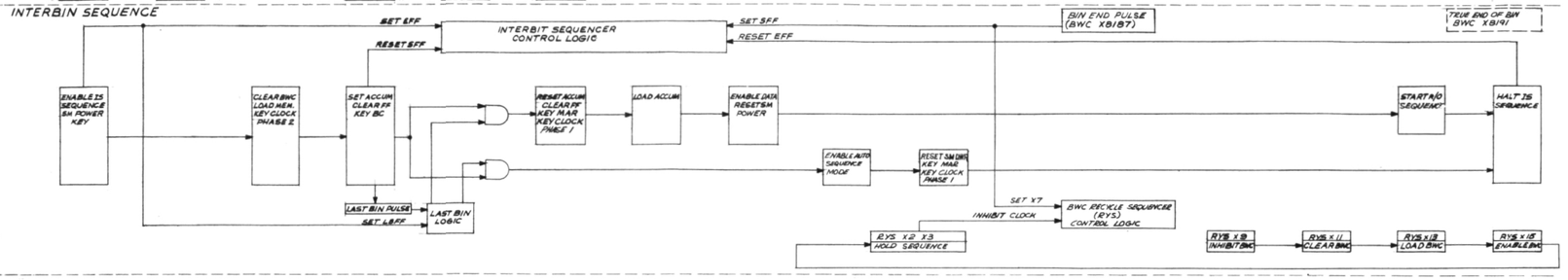
STATE #	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31

REVOLUTION START SEQUENCE

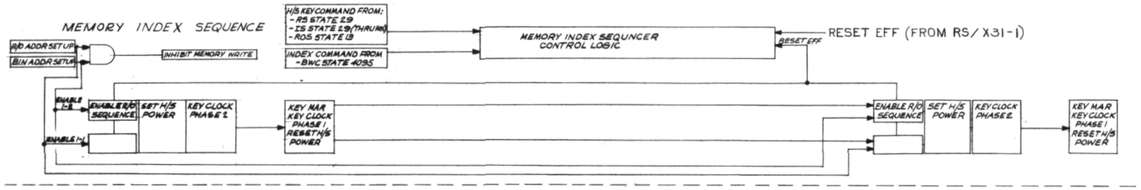
REVOLUTION PULSE IS ASYCHRONOUS TO SYSTEM CLOCK

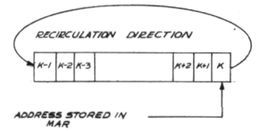


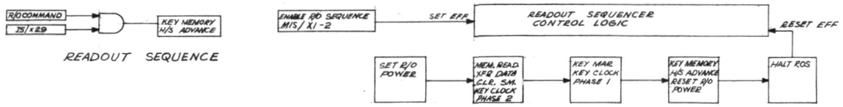
INTERBIN SEQUENCE



MEMORY INDEX SEQUENCE







EVEN CLOCK STATES CORRESPOND TO INTERVALS IN WHICH CCIH IS LOW.
THE BIN END PULSE IS SYNCHRONOUS WITH THE SYSTEM CLOCK BUT MAY OCCUR IN ANY OF 16 POSITIONS, WITH REFERENCE TO STATE 0. IT IS SHOWN IN STATE 22 FOR CONVENIENCE. THIS PULSE ANTICIPATES THE TRUE END OF THE BIN BY 8 μs TO ALLOW BWC RECYCLING WITHOUT DEAD TIME.
MEMORY INDEX SEQUENCE CAN BEGIN ON EITHER STATE 1 OR STATE 17.

RELEASED

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION
			LIST OF MATERIALS	

UNLESS OTHERWISE SPECIFIED CAPACITOR VALUES ARE IN μf, RESISTOR VALUES ARE IN OHMS, ELECTRICAL TOLERANCES = ± 5%

DIMENSIONS ARE IN INCHES. TOLERANCES ON: FRACTIONS ____ DECIMALS ____ ANGLES ____. DO NOT SCALE THIS DRAWING

MATERIAL —

THIS DWG. REPLACES 107-800009

DRAWN JAWDENUCE 10/64
CHECKED 10/64
APPROVED 10/64
APPROVED

MIT APPROVED — DATE —

CENTER FOR SPACE RESEARCH
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

DATA ACQUISITION SYSTEM SEQUENCER TIMING

SIZE E | CODE IDENT NO. — | DRAWING NO. 107-800012

SCALE — | SHEET 1 OF 1

107-800012 B

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Each accumulator is time-shared between all 256 bins. At each bin start, the subtotal for the bin is called from memory, set into the accumulator and new data added for the duration of the bin. At the end of the bin, the new total is returned to memory.

The memory (Figure 3-12) is subdivided into eight identical 2400-bit "submemories" operated in parallel. Each submemory is associated with a particular accumulator and measurement chain. All submemories consist of eight parallel 300-bit shift register chains with input and output gating each associated with a particular bit of the accumulator. Data transfers and indexing occur simultaneously throughout the memory allowing the use of common drive signals.

The eight submemory outputs are paralleled and words from individual submemories readout sequentially.

2. Shift Register Choice - The shift register chains use dynamic (capacitive storage) MOS logic. Data is stored as a voltage level on the gate input capacitance of each register stage or bit. Alternate application of two clock pulses moves the voltage level from stage to stage or, in other words, moves the data from bit to bit down the register chain.

In all dynamic registers data must be shifted no slower than some minimum rate that is a function of MOS gate capacitance and gate leakage current. In most the minimum shift or update frequency is about 1 KHz at +25°C or about ten times faster than the instrument bin rate. One register type was found which, because of a different substrate crystal structure, was able to operate at 100 Hz at +25°C. Incorporation of this device into the MIT memory allowed the use of bin rate updating and thereby simplified the electrical design to a considerable degree. Additional advantages of the device included lower than usual clock and data pulse amplitudes, smaller memory

volume due to higher bit density per register can and no higher cost than conventional dynamic shift registers.

The device used is a special order version of the National Semiconductor* MM 406 dual 100-bit shift register. In addition to normal Goddard screening specifications all registers were tested for operation at 100 Hz at +40°C to provide a guaranteed margin of safety in the minimum operating frequency. Generally, minimum operating frequency halves for every 10°C drop in temperature. This specification, therefore, provides at least a two-octave margin at the expected instrument operating temperature.

3. Memory Design Characteristics, Alternate Choices - Shift register power requirements were determined experimentally and verified by comparison with manufacturer's data for two types of registers as part of the memory design process.

In general, the procedure was to photograph the clock current waveforms recording the peak currents and spike widths. From a straight line approximation to these waveforms it was possible to estimate the energy per clock cycle. Multiplying by frequency gave the power at that frequency. All powers were reduced to a per bit basis, the most useful form,and normalized to 1 MHz. Any dc power drawn by the registers was also normalized in the same fashion (see Table 3-4).

The energy in a triangular current pulse of height I_p and width W is:

$$E = \frac{V_c I_p W}{2} \qquad (3\text{-}5)$$

where V_c is the clock voltage.

Average power at a frequency, f, is:

$$P = \frac{V_c I_p W}{2} \cdot f \qquad (3\text{-}6)$$

*National Semiconductor Corporation, Santa Clara, California 95051.

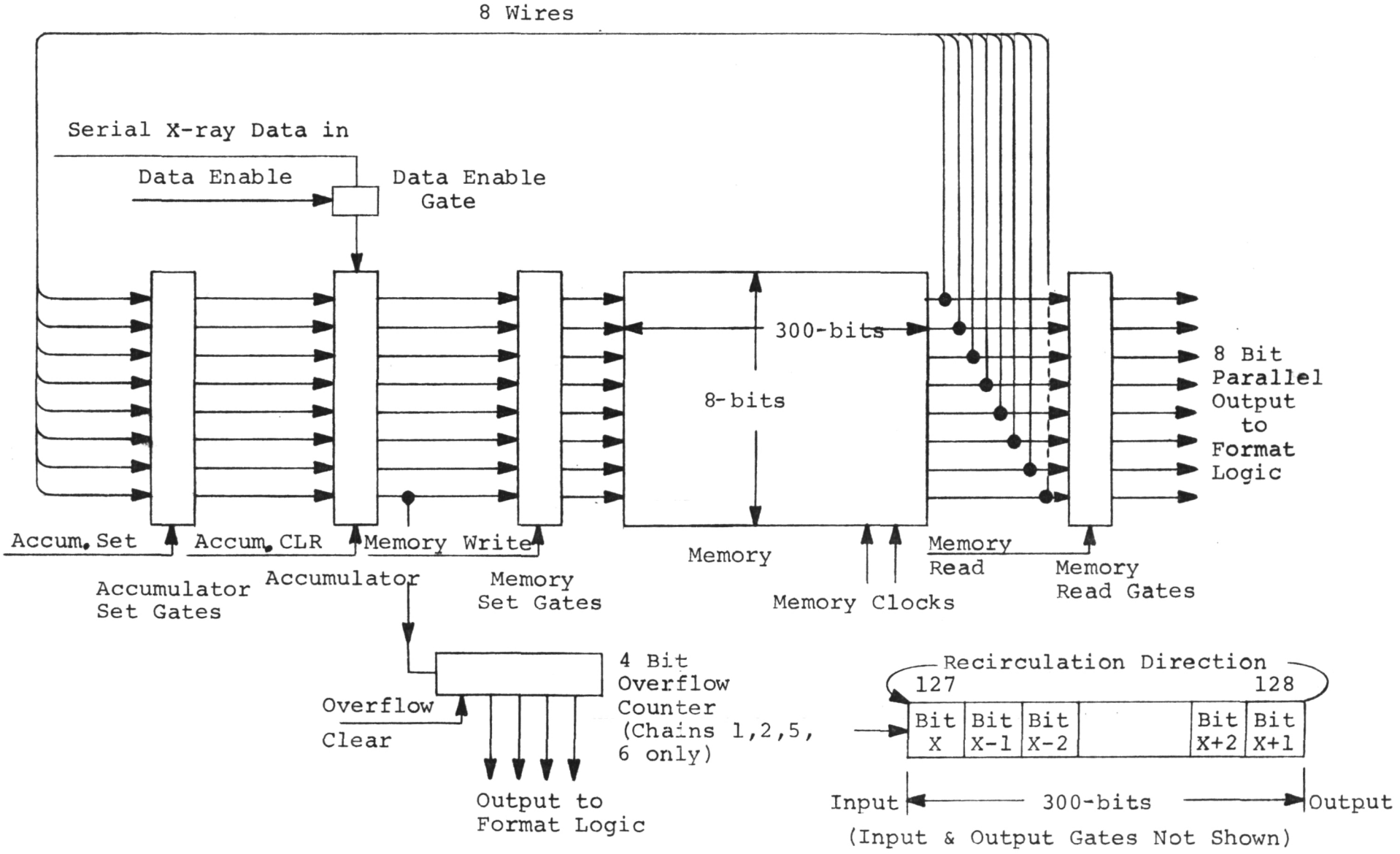

Figure 3-12 Typical Submemory and Accumulator.

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The total energy per clock cycle is the sum of the energy in each of the clock pulses.

The energies and powers calculated here represent energy and power taken from a constant voltage supply and include the 50% loss inherent in any capacitor charging process.

Two memory designs were considered; a random access system and the bin rate system. Experimental data is used in the calculation of total power requirements in both cases.

In the random access memory the shift registers are continuously cycled at the minimum update frequency of the devices. For the MEM 3064 this is 10 KHz.

Table 3-4 Shift Register Per Bit Power Requirements Experimental Results

UNIT	CLOCKS					CLOCK POWER	DC POWER	TOTAL POWER
	V_c volts	ϕ_1 I_p/W ma/ns	ϕ_2 I_p/W ma/ns	ϕ_3 I_p/W ma/ns	ϕ_4 I_p/W ma/ns	P/bit mw	P/bit mw	P/bit mw
MEM 3064	-27	60/100	60/100	60/100	60/100	0.117	-	0.117
MM 406	-16	25/160	19/200	-	-	0.156	0.620	0.776

All power figures are normalized to 1MHz. DC power includes output stage requirements. Output stage voltage is pulse powered (T_{on} = 2.0 μsec).

When a readout to the spacecraft is commanded or when a bin end pulse occurs, the required address is searched out at 1 MHz and then the data transfers to and from the memory are carried out.

The average power required is the sum of the continuous sequencing power, the power consumed during interbin operations and power consumed during readouts. Continuous sequencing requires:

$$P_{seq} = NP_{bit} \frac{f_{seq}}{f_o} \tag{3-7}$$

where

N = memory size (bits)

P_{bit} = power per bit at f_o

f_o = frequency at which P_{bit} is measured

f_{seq} = continuous sequencing rate

The number of interbin operations per second varies with the rotation rate of the vehicle and, therefore, the bin frequency, f_b. On the average, it will be necessary to cycle through only one-half the total chain length, ℓ, to arrive at the required address. Therefore,

$$P_{ib} = \frac{NP_{bit}}{f_o} \frac{\ell}{2} f_b \tag{3-8}$$

where $f_b = \frac{1}{BW}$ = bin repetition frequency.

It is interesting that the average interbin power is not a function of the interbin cycling frequency but rather the number of bins per second. This can be seen in another way from the following development.

During an interbin period, the average power drawn is

$$P_{ib} = \frac{NP_{bit}}{f_o} \cdot f \tag{3-9}$$

where f is the cycling rate between bins. But P_{ib} is duty cycled, occurring only for $\frac{\ell}{2} \cdot \frac{1}{f}$ seconds, f_b times a second. Therefore,

$$P_{ib} = \frac{NP_{bit}}{f_o} \cdot \frac{\ell}{2} \cdot \frac{f_b}{f} \cdot f \qquad (3\text{-}10)$$

$$P_{ib} = \frac{NP_{bit}}{f_o} \cdot \frac{\ell}{2} \cdot f_b \qquad (3\text{-}11)$$

which is the original expression for P_{ib}. This same argument holds for the readout power in this and in the bin rate memory. The average power depends only on the number of cycles per second and not on the distribution of those cycles within that period.

By a similar calculation, the power consumed during readout is:

$$P_{ro} = \frac{NP_{bit}}{f_o} f_{ro} \frac{\ell}{2} \qquad (3\text{-}12)$$

and the total power

$$P_T = \frac{NP_{bit}}{f_o} [f_{seq} + \frac{\ell}{2} (f_{ro} + f_b)]^{**} \qquad (3\text{-}13)$$

Using the MEM3064 and assuming the nominal bin width,

$N = 256 \times 64 = 16.4 \times 10^3$ bits

$P_b = 0.117$ mw/bit @ 1 MHz

$f_o = 10^6$ Hz

$f_{seq} = 10^4$ Hz

$f_{ro} = 12.5$ words/sec

$f_b = \frac{1}{BW_{nom}} = \frac{1}{7.8ms} = 128$ Hz

$\ell = 256$ bits

** To a first approximation which assumes that the interbin and readout operations do not displace any normal sequencing pulses.

then

$$P_T = \frac{NP_b}{f_o} \left[f_{seq} + \frac{\ell}{2} (f_{ro} + f_b)\right]$$

$$= \frac{16.4 \times 10^3}{10^6} \left[10^4 + \frac{256}{2} (12.5 + 128)\right] = 54\text{mw} \qquad (3\text{-}14)$$

For the MM406 in the same memory design,

$$N = 300 \times 64 = 19.2 \times 10^3 \text{ bits}$$

$$P_b = 0.776 \text{ mw/bit @ 1 MHz}$$

and

$$\ell = 300 \text{ bits}$$

$$P_T = \frac{19.2 \times 10^3 \times 0.776}{10^6} \left[10^4 + \frac{300}{2} (12.5 + 128)\right] = 452\text{mw} \qquad (3\text{-}15)$$

In this configuration the MM406 cannot compete from a power standpoint.

In the bin rate memory the revolution period determines the normal sequencing rate. Sequencing occurs at the bin frequency, f_b. Data transfers are made to and from the memory and the memory is stepped one address during the interbin period. This new address is held until the end of the next bin. Readouts to the spacecraft require an address search as in the previous memory. The search can be accomplished at a somewhat lower frequency, a frequency, in fact, no higher than necessary to complete the full 300-bit cycle in less than the minimum bin width. Power consumed during normal sequencing is:

$$P_{seq} = \frac{NP_{bit}}{f_o} \cdot f_b \qquad (3\text{-}16)$$

Readout power is:

$$P_{ro} = \frac{NP_{bit}}{f_o} \cdot \ell \cdot f_{ro} \qquad (3\text{-}17)$$

not $(\ell/2)(f_{ro})$ since it is necessary to return to the original bin address after the readout sequence is complete. That is, each register is sequenced through ℓ bits for each readout.

The total power for this memory is then:

$$P_T = \frac{NP_{bit}}{f_o} [f_b + \ell f_{ro}] \qquad (3\text{-}18)$$

Only the MM406 will operate in this system:

$$P_T = \frac{19.2 \times 10^3 \times 0.776}{10^6} [128 + 300 \times 12.5] = 57.6\text{mw} \qquad (3\text{-}19)$$

or about the same amount of power as the MEM3064 in the random access system. Control logic requirements, DTL - MOSFET interface requirements and relative noise considerations will now be considered. These will be seen as determining the design choice.

The packing density of each of the registers is:

MEM3064: 64 bits in TO-74 or TO-87 - 256 required

MM406: 200 bits in 8 pin TO-74 +2-1/8 watt resistor - 96 required + 320 resistors per can.

At 6 TO-74 cans per in^3, total volume requirements are:

MEM3064: 49 in^3

MM406: 16.0 in^3

or significantly advantageous in favor of the MM406.

The cost of the memory is estimated based on two systems plus one breadboard plus 20% spares:

MEM3064: 702 units

MM406: 320 units

From the manufacturers data (1968 prices):

GI - MEM3064: $50.50 each including $7.00 special testing, 100-999.

NS - MM406: $74.00 each including $15.00 special testing, 100-999.

Costs are, therefore,

MEM3064: $36.5K

MM406: $23.9K

for the two memory types.

The cost and volume advantage clearly go to the Bin Rate System.

Control logic requirements were estimated to be about the same for the two systems. Use of the National MM406 with its lower operating voltages allowed a significant simplification in interface circuits, however (see also Section 3.2.5).

The bin rate system operates the more slowly of the two and one might suspect that it would be the less troublesome from a noise standpoint. The random access design cycles at 10 KHz continuously, at 1 MHz for 128 bits, 12.5 time a second (readouts) and at 1 MHz for 128 bits, 128 times a second for bin data transfers. There are four clock pulses per cycle, creating 1.12×10^5 clock pulses per second.

There is no continuous high frequency updating in the bin rate system. Cycling occurs at the bin rates of 128 bits per second plus the readout rate of 300 bits, 12.5 times a second during readouts. There are two clock pulses per cycle generating a total of 7.6×10^3 clock pulses per second.

The bin rate system does require significantly fewer clock pulses per second and all else equal should be the quieter of the designs. Additionally, it need never operate at 1 MHz (actually never faster than 62.5 KHz) and uses clocks with a slower rate of rise; both factors contributing to low noise operation.

The bin rate system is seen to be advantageous in three of the four criterion and equal in the fourth and, therefore, was chosen for the MIT instrument.

4. Operating Restrictions - The update requirement of the dynamic shift register causes one important memory limitation; loss of even a single Revolution Pulse leads directly to loss of all memory data. Apart from spacecraft aspect pulse failures (for one type of which provision has been in the instrument), such loss occurs only during Day/Night and Night/Day transitions in which a few wheel revolutions are required for the instrument to drop one aspect reference pulse and acquire another. Data taken during these intervals is of indeterminate quality due to the transitions anyway and the loss is insignificant in terms of instrument objectives.

Data loss due to Revolution Pulse jitter will not occur until the jitter reaches at least 10 milliseconds from pulse to pulse.

3.2.3.2 Overflow Accommodation - It is possible that the intensity from certain x-ray sources will exceed the capacity of 255 counts in the eight-bit accumulator. This is most likely in Chains 1, 2, 5, and 6. A four-bit overflow accumulator is provided for each of these chains. These overflow accumulators are reset only upon readout to the spacecraft and not at the end of each bin. It is necessary to deduce from the data the bin(s) in which the overflow occurred. Readout of the overflow accumulators occurs during each Format Start Line.

Although the accumulation time for each bin is the same (neglecting bin 255 which is subject to data loss due to timing errors, see Section 3.2.1.2), the interval during which accumulation occurs is different for each bin because of sequential

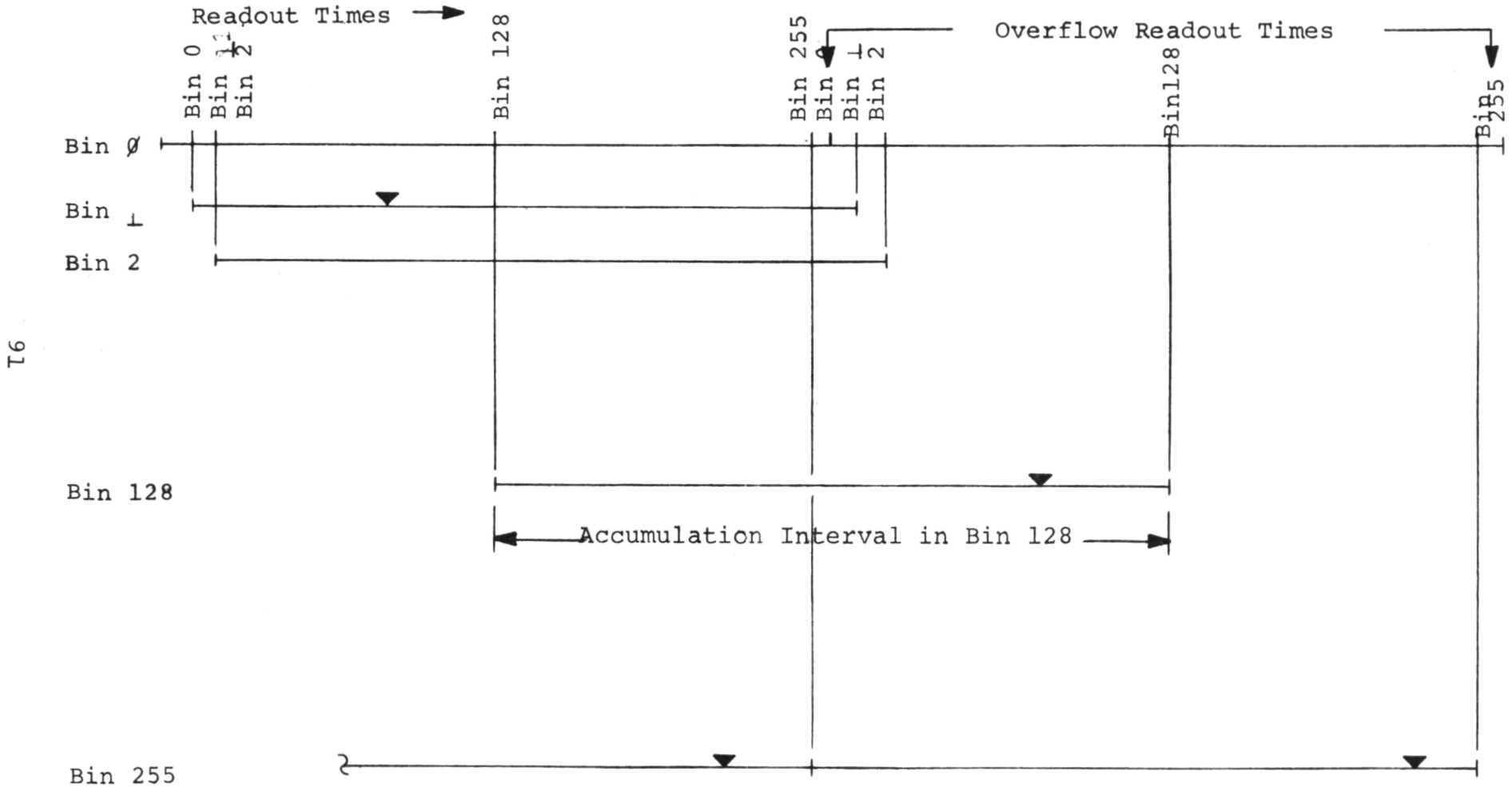
readout in the format. For any bin accumulation begins immediately after readout of that bin and continues (in bin width segments) until the next readout occurs. That is, accumulation intervals are skewed as shown in Figure 3-13. Readout of the overflow counters, on the other hand, always occurs during the Format Start Line (Section 3.3.1) between the readout of bin 255 and bin 0.

Overflows which are time invariant and spatially limited to a single bin are relatively easy to tie down as the figure suggests. If the point of overflow is indicated by the arrow, then readout occurs in the Format Start Line following the arrow. When overflow count rates are time varying and/or spread over a few bins (a very likely situation) or are such that the overflows occur just prior to bin readout, one must go to the bin data to deduce the location and magnitude of the overflow peak since the overflow readout becomes ambiguous. Consulting the bin data is reliable in the trivial case as well and so is recommended in tying down all overflow situations.

3.2.3.3 Memory Addressing System

3.2.3.3-a Description (see Figure 3-14) - The nine-bit Memory Address Register (MAR) defines the addresses of specific locations in the 300-bit shift register chain. At any time, the address stored in the MAR is the address of the information displayed at the output of the shift register chain. The MAR is indexed every time the memory is indexed which is defined as whenever a phase one clock is applied to the shift register chain. Reset of the MAR to zero on every 300th index pulse is automatically performed by the MAR reset logic.

The nine-bit Bin Counter (BC) is electrically identical to the MAR but is indexed during interbin intervals. A requirement for data transfer of bin data subtotals to and from the



▼ = Typical Overflow Occurances in a Single Counter

FIGURE 3-13 ACCUMULATION INTERVALS BY BIN NUMBER

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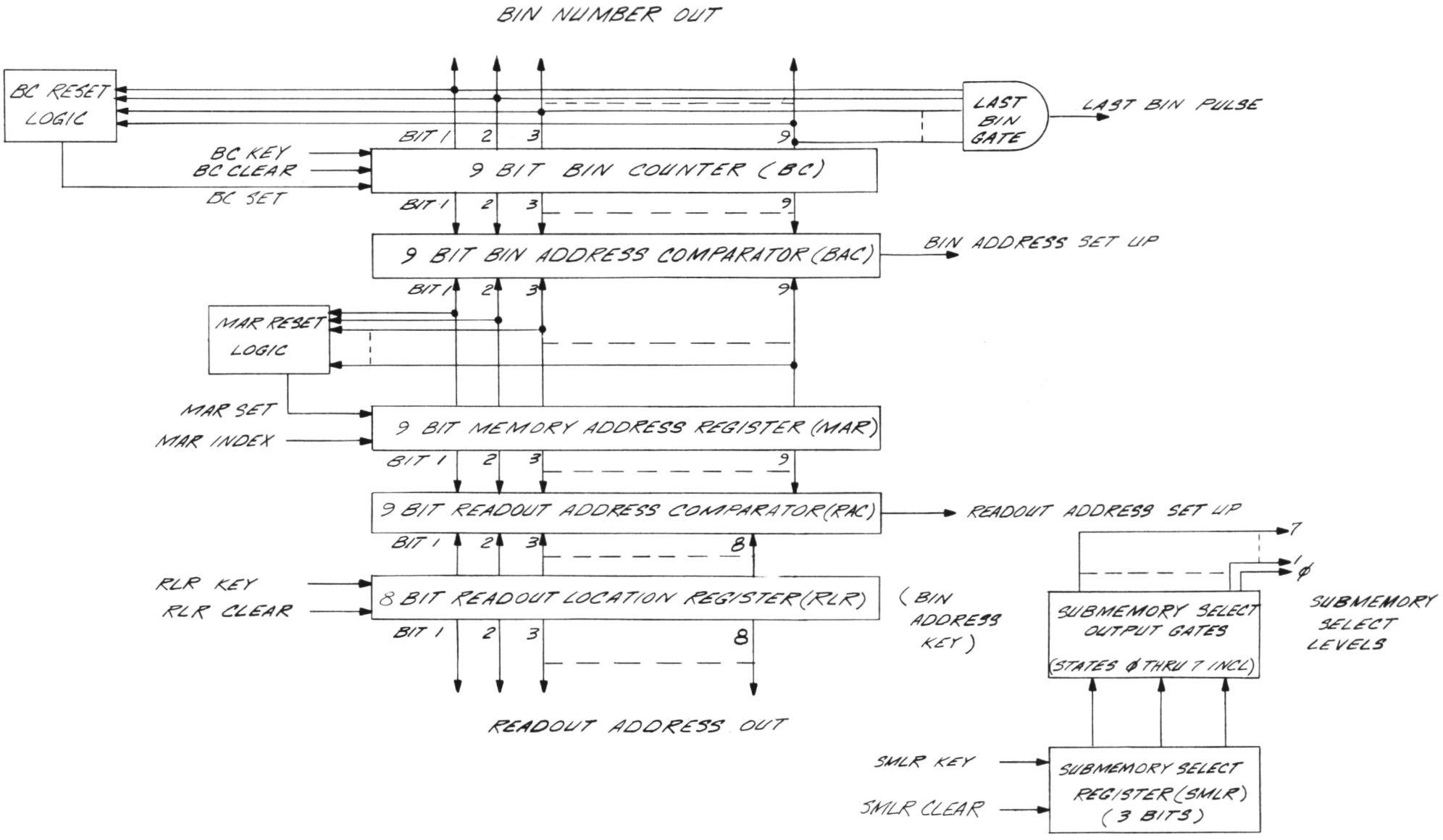

FIGURE 3-14

MEMORY ADDRESSING SYSTEM

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memory is that the "Bin Address Setup Pulse" be logically high indicating that the addresses in the BC and MAR are identical.

The eight-bit Readout Location Register (RLR) contains the readout address to be located in memory when a readout command is received from the Format Logic. No ninth-bit is required because addresses 256 through 299 are unused in the instrument and no need exists to address them. The Readout Address Comparator (RAC) output is logically high when the readout address has been reached,that is, when the addresses in the RLR and MAR are identical.

The Submemory Location Register (SMLR) stores the number of the submemory to be readout (0 to 7) and indexes once per format word skipping word zero (see Section 3.3.1). Outputs from the Submemory Select Gates inhibit all but the selected submemory output.

3.2.3.3-b Operation - Memory operations generally proceed at the bin rate. At the end of a bin, data is transferred into memory from the accumulators and the BC, MAR and Memory are keyed to the next sequential address. Data is then taken from memory into the accumulators and data accumulation begins for the new bin. At nominal spacecraft spin rate, these operations proceed at 128 Hz.

When a readout is commanded, the Memory and Memory Address System wait for the completion of the next bin start cycle. Shortly after the establishment of the new bin address in the BC a command is given by the Interbin sequencer (Section 3.2.2.2) that begins the search for the readout address. The search proceeds at 62.5 KHz and is controlled by the Memory Index Sequencer (Section 3.2.2.4). When the addresses in the MAR and RLR agree (as indicated by a high Readout Address Setup Pulse), the search is halted and the Readout Sequencer (Section 3.2.2.5) keyed. Transfer of data to the Format Logic and subsequent

clearing of the memory at the readout address is done by this sequencer and, subsequently, the Memory Index Sequencer is keyed to return the memory to its original bin address.

Since it is always necessary to return to the original bin address after a readout, the memory must be cycled through its entire length in less than the minimum expected bin width to ensure readout cycle completion prior to the start of the next bin. At 62.5 KHz, this operation takes 4.8 milliseconds or about 100 microseconds faster than the minimum bin width.

In this manner the two asychronous operations of bin rate data transfers and spacecraft readouts are made to occur without interference and at the absolutely minimum rates consistent with meeting instrument objectives.

3.2.4 Antico Counter - Information on total counting rate and geometric antico event rate is useful in verifying counter performance. A ten-bit counter, with a two-bit Prescaler, is provided for this purpose. It is orbit multiplexed to measure total counting rate (sum of low edge discriminator firings) on even orbits and geometric antico rate on odd orbits. A "lock-out" is provided to flag extremely high counting rates and prevent overflow. Lock-out occurs on the binary number 1111000000 (960) or at a rate of 12.4 KHz. Rate sampling occurs every block start line for 0.310 seconds. The accumulation interval extends from the trailing edge of the main frame gate that terminates Word zero in the Block Start Line to the leading edge of the main frame gate that terminates Word four. The number read out in the format is converted to a rate in Hertz by multiplying by 12.9.

3.2.5 Design Comments

3.2.5.1 9040 Logic - The logic system is built primarily with Fairchild* 9040 Series DTL low power integrated

*Fairchild Semiconductor, Mountain View, California.

circuit logic. Although subsequently removed from the Goddard Preferred Parts List for metalization and surface inversion problems (PPL-11, Notice No. 3, June 29, 1971), these parts have performed well here. (However, see also the Failure Analysis Reports in Section 4.4.4.)

A particularly troublesome situation arose, however, from lack of adequate data on asynchronous pulse width requirements in the 9040 J-K flip-flops. Lacking from the 9040 data sheets at the time of the design effort, asychronous pulse requirements were inferred from stated worst case propagation delays and the performance of specific units in the MIT system breadboard. Subsequently, a continuing series of 9040 "failures" in both the prototype and flight instruments led to further investigation along these lines and the discovery (from Fairchild supplied information) that minimum 9040 asynchronous pulse width requirements were far in excess of what was used in many sections of the instrument. The 9040 "failure" pattern was apparently the result of a "weeding out" process that eliminated from the instrument those devices that would not work on the available pulse widths. When the new information became available, all asynchronous input pulse widths were widened as much as possible. This change, and the previous "weeding out" process, eliminated all logic problems traceable to the asynchronous inputs of 9040's in spite of the fact that in some areas pulse widths were still below the stated requirements.

3.2.5.2 Memory - An interesting design feature of the memory, apart from the bin rate cycling technique, is the manner in which the shift registers are used to minimize power converter voltage outputs and interface circuitry. Normal shift register voltage levels are shown in Figure 3-15.

These registers must interface with DTL logic levels which are, of course, zero and plus 4 volts. If the registers were used

as shown, minus 10 and minus 16 volt supply outputs would be needed in addition to the plus 5 and plus 10 volt supplies previously provided for and relatively complex, multiple transistor, discrete interface circuits would be required. Running the shift registers "inverted" (Figure 3-16) eliminated one negative supply and made it possible to meet the interface requirements with only one transistor on the input and output of each shift register chain. In addition, a simplification was achieved in the pulse power circuits (all external register pull up resistors are pulse powered) since the "pull-ups" now returned to ground. No diffi cult implementation problems were encountered as a result of this approach. It was necessary to carefully decouple the plus 10 volt lines at both low and high frequencies so that the very high instantaneous clock pulse currents could be handled without excessive noise on the plus 10 volt supply line. Separate decoupling circuits were provided for each 600-bit group of shift registers.

3.3 Format Logic

Data formating in the instrument is handled primarily by discrete rather than integrated logic as a power conservation move in an area where only slow speed (less than 800 Hz) circuits are required. The format is generated using the spacecraft 800 Hz clock and Main Frame Gate signals only. MIT is assigned spacecraft Main Frame Words 13, 16, 21, and 25. Operation of the logic depends on the existence of a gap of at least one word between each readout word such as exists in the assigned group.

3.3.1 Data Format - The format of the MIT data is shown on inserted MIT drawing 107-800007. The format is composed of 264 lines of nine 8-bit words each. The 264 lines are

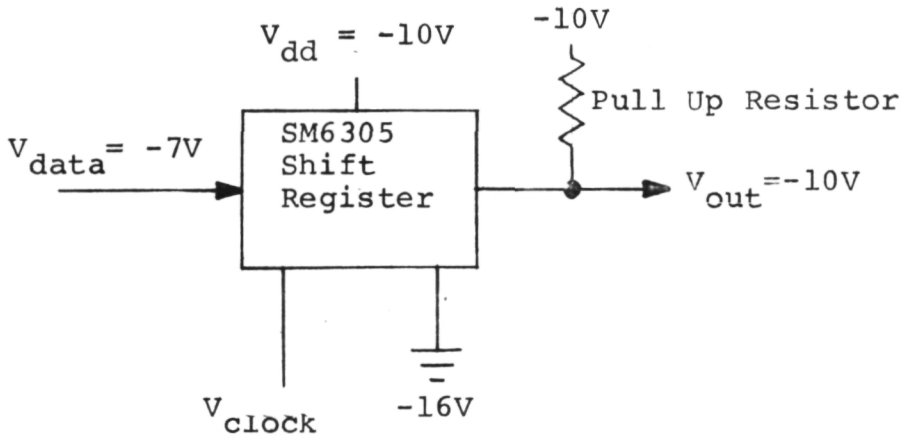

FIGURE 3-15 NORMAL SM6305 VOLTAGES

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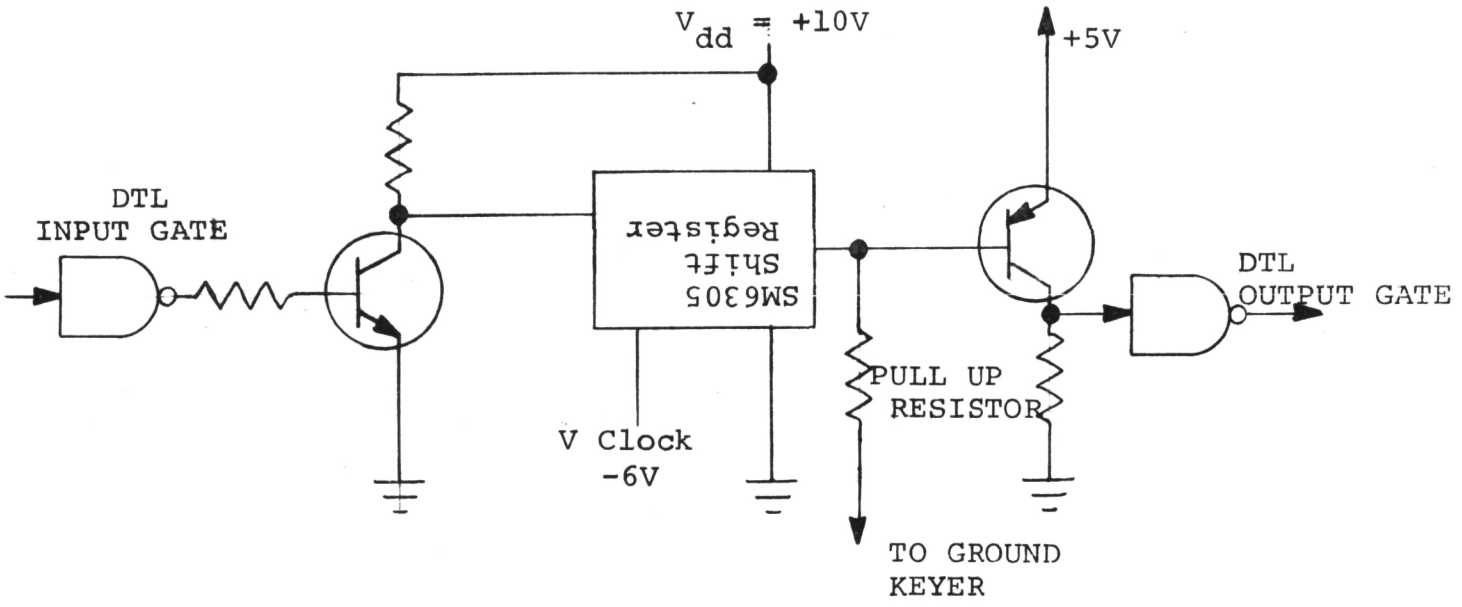

FIGURE 3-16 "INVERTED" SM6305 OPERATION

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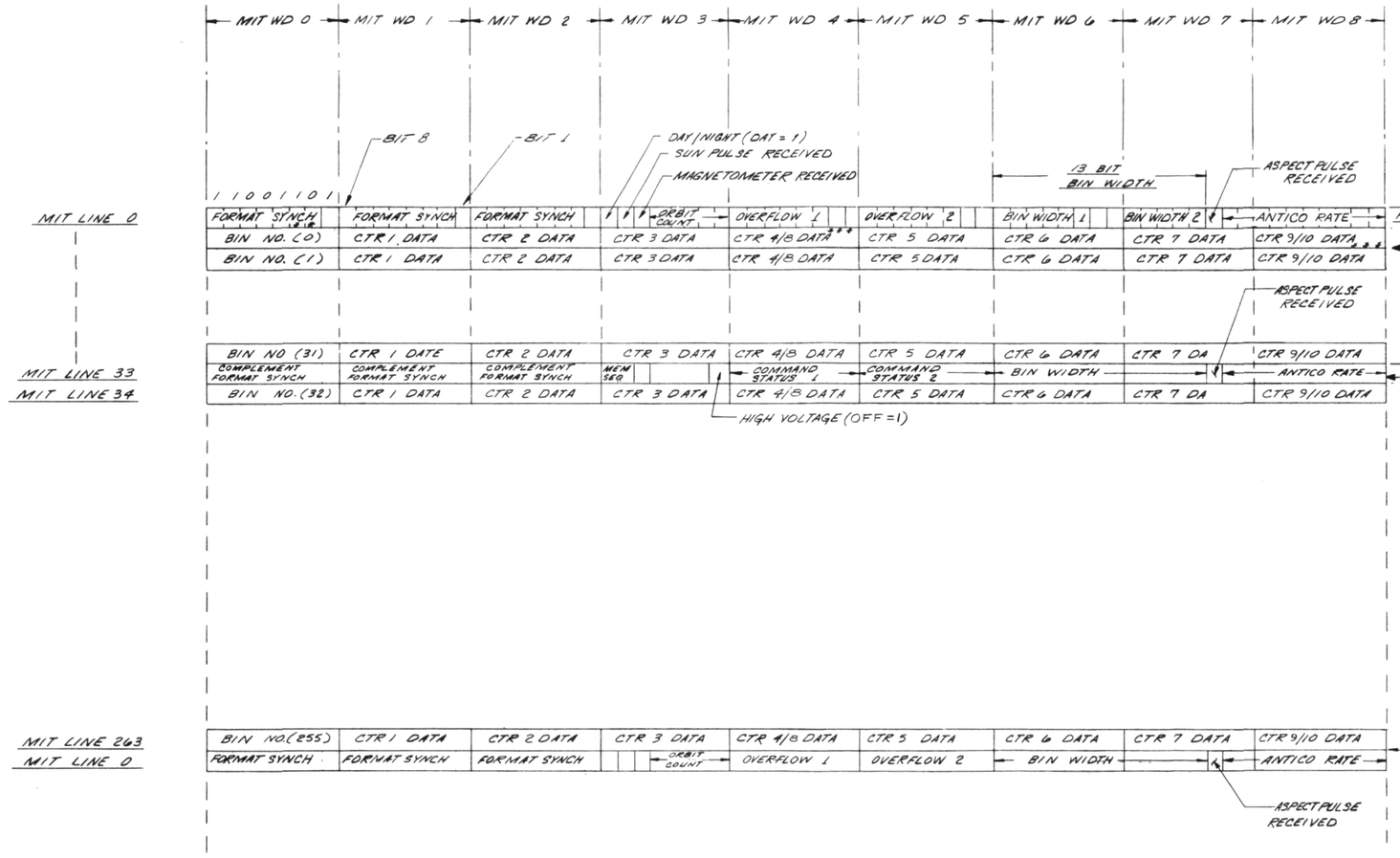
REVISIONS						
ZONE	LTR	DESCRIPTION	DR	CHK	DATE	APPROVED
A7 A7 A1	A	CTR 4/8 DATA WAS CTR 4/9 DATA CTR 9/10 DATA WAS CTR 8/10 DATA CTRS 4/9 ARE ACCUM WAS CTRS 4&8 ARE ACCUM CTRS 8 & 10 WAS CTRS 3&10 107-800007 WAS 107-907	R.P.	J.D.	9-13-68	RPR
	B	HIGH VOLTAGE STATUS INDICATOR RELOCATED FROM BIT 3 WORD 7 DATA BLOCK START LINE TO BIT 1 WORD 3 OF DATA BLOCK START LINE. COMMAND "STATUS 16" "HIGH LEVEL DISC. OFF=1" ADDED. "NO MULTIPLEX" DELETED FROM CMD STATUS BITS 4&5 OF COMMAND STATUS INDICATOR NOTE. "OFF=1" ADDED TO BITS 6&7 OF COMMAND STATUS NOTE.	R.P.	J.D.	1-3-69	Rpr 1-3-69
	C	NOTATION "CALIBRATION IS AUTOMATICALLY PERFORMED EVERY 32 ORBITS WAS" "CALIBRATION IS AUTOMATICALLY PERFORMED DURING ORBIT 31	R.P. 1/6/69	JD	1/31/69	Rpr 2/3/69



NOTE:
IN NUMERICAL QUANTITIES MOST SIGNIFICANT BIT IS AT LEFT AND IS THE BIT SHIFTED OUT FIRST TO S/C

ANTICO WORD ASSIGNMENT.
EVEN ORBIT - COUNT RATE (Σ LLD FIRINGS)
ODD ORBIT - GEOMETRIC ANTICO RATE

OVER FLOW ASSIGNMENT.

COUNTER WORD		BITS
1	OVERFLOW 1	1-4
2	OVERFLOW 1	5-8
5	OVERFLOW 2	1-4
6	OVERFLOW 2	5-8

FORMAT REQUIRES 190.88 SEC.

NOTES:

* COMMAND STATUS WORD

← 1 S/C WORD →

1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16

BIT NO.
1. HIGH VOLTAGE PROTECTION OFF=1
2. AUTO-CALIBRATE OFF=1
3. MANUAL CALIBRATE ON=1
4. COUNTER 9 OFF=1
5. COUNTER 10 OFF=1
6. COUNTER 1 OFF
7. COUNTER 2 OFF
8. COUNTER 3 OFF=1
9. COUNTER 4 OFF=1
10. COUNTER 5 OFF=1
11. COUNTER 6 OFF=1
12. COUNTER 7 OFF=1
13. COUNTER 8 OFF=1
14. ANTICO OFF=1
15. RISE TIME ANTICO OFF=1
16. HIGH LEVEL DISC. OFF=1

** FORMAT SYNCH = 1100 1101
M.S. L.S.

*** DATA FROM COUNTERS 4 & 9 ARE ACCUMULATED ON EVEN NUMBERED ORBITS
DATA FROM COUNTERS 8 & 10 ARE ACCUMULATED ON ODD NUMBERED ORBITS

CALIBRATION IS AUTOMATICALLY PERFORMED EVERY 32 ORBITS
COUNTERS 1,2,3,4,9 ARE CALIBRATED DURING ORBIT 0
COUNTERS 5,6,7,8,10 ARE CALIBRATED DURING ORBIT 1

RELEASED

FIND NO.	QTY REQD	PART OR IDENT. NO.	NOMENCLATURE OR DESCRIPTION	MATERIAL OR SPECIFICATION

LIST OF MATERIALS

UNLESS OTHERWISE SPECIFIED CAPACITOR VALUES ARE IN μf RESISTOR VALUES ARE IN OHMS ELECTRICAL TOLERANCES = ±5%

DIMENSIONS ARE IN INCHES TOLERANCES ON FRACTIONS DECIMALS ANGLES ± ″ ± ″ ± °

DO NOT SCALE THIS DRAWING

MATERIAL —

MIT APPROVED — DATE —

CENTER FOR SPACE RESEARCH
MASSACHUSETTS INSTITUTE OF TECHNOLOGY
CAMBRIDGE, MASS.

DRAWN R Dionne 1/9/67
CHECKED J Rankin 1/5/67
APPROVED [illegible] 1/18/68
APPROVED [illegible] 3/8/68

MIT 030-H DATA FORMAT

SIZE D | CODE IDENT NO. — | DRAWING NO. 107-800007

SCALE — | SHEET 1 OF 1

107-800007 C

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broken into eight data blocks, each of which is, in turn, composed of either a format start line or a block start line and thirty-two data lines. The beginning line of the block is used to transmit synchronization and experiment status information. The following thirty-two lines are used to transmit data. Each data line begins with the number of the bin from which the data about to be read out was accumulated. In sequence, but without identification, the contents of the submemories associated with that bin and each of the eight measurement chains whose outputs have been accumulated are read out. That this sequencing is being performed is verified by the first three bits of MIT Word 3 of every block start line (the Memory Sequence bits). The bin number is transferred directly from the Readout Location Register giving a positive indication of the memory location during readout. The time required to read out one complete data format at four words per spacecraft main frame is 190 seconds. Control of the format is generated within the MIT experiment using only the Main Frame Gate from the vehicle. Output is obtained from an eight-bit shift register. Data is shifted out using the spacecraft 800 Hz square-wave clock and a .01 second (eight cycles of shift clock) main frame gate which indicates that the spacecraft can accept MIT data.

3.3.2 Format Control Logic - The Format Control Logic identifies data words, lines, and blocks and controls data shifting within the experiment. Only two inputs from the spacecraft are used; the 800 Hz clock and the four assigned digital Main Frame Gates. These gates define selected words in the spacecraft data main frame and are displayed in sequence to the experiment on one interface line. Figure 3-17 is a block diagram of this logic system.

The Main Frame Gate pulses are counted by a scale of nine counters whose output states can be described as zero through eight. The outputs of the counter drive a word identification

matrix. This counter operates continuously without external reset. The counter indexes on the trailing edge of each main frame word gate. The logical "AND" of the counter flip-flop outputs determine the identification of a word.

The line control logic performs the functions of: a.) identification of data line, b.) identification of data block or format start lines, and c.) indexing of the Readout Location Register (RLR).

The RLR is a serial counter which is indexed on the trailing edge of MIT Word 8, the last word of an MIT line (see Section 3.3.1). It contains the bin number of the data being read out to the spacecraft on a given data format line. Consideration of the format will indicate that during the last data line of each data block, the five least significant bits of RLR will be read as decimal 31 or in binary as all "ones". This is the test for the last data line in a block. RLR indexing is then prohibited for one line. The trailing edge of Word 8 initiates a block start line. The block start lines are simply counted without reset and every eighth block start is further identified as a format start line. Upon completion of either a block start or format start line, the RLR is indexed and the next thirty-two lines are identified as data lines.

3.3.3 Format Matrix - This diode AND-OR matrix controls the loading of the experiment Output Shift Register (see Section 3.3.4). The eight-bit parallel words from the memory along with experiment status information enter the matrix. Selection from among these inputs is made by the Format Control Logic (Section 3.3.2) in accordance with the location of the next word in the data format.

3.3.4 Output Transfer Logic - This logic system controls the inputs to and shiftouts from the Output Shift Register. It also controls the Submemory Location Register.

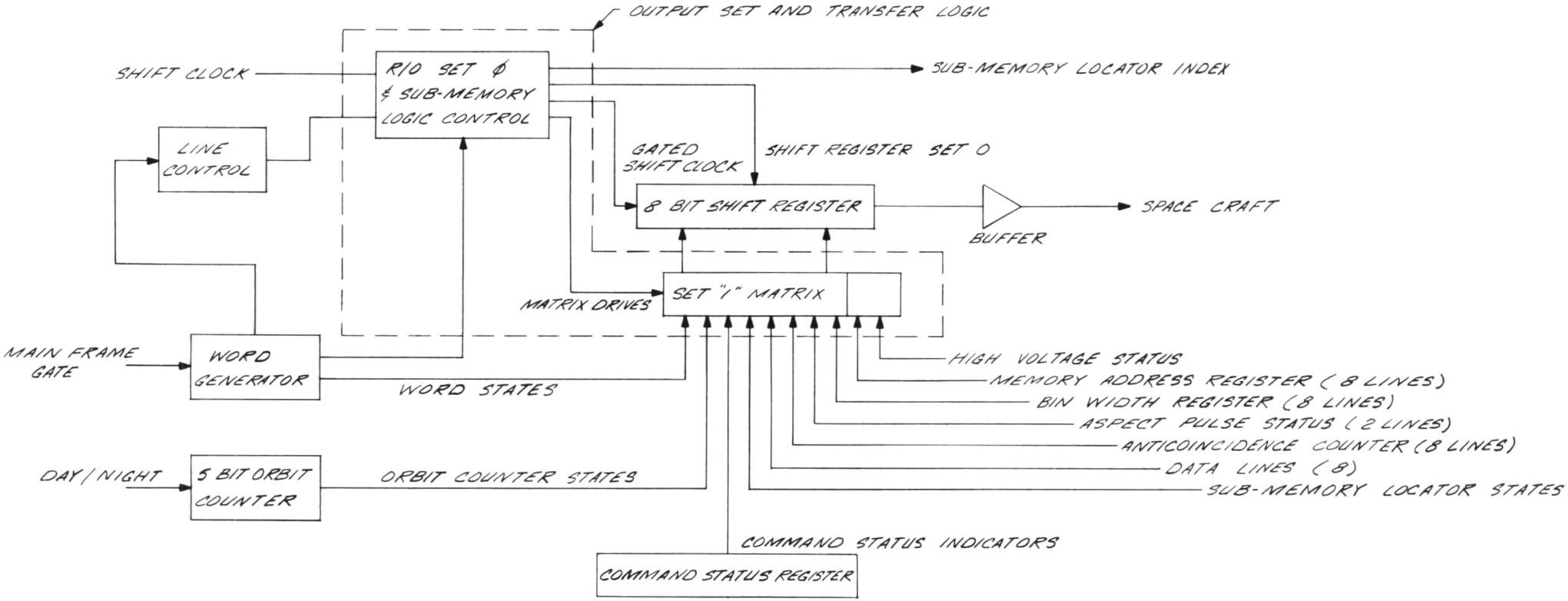

FIGURE 3-17 FORMAT CONTROL LOGIC

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The Output Shift Register (OSR) is set to zero at the beginning of each word gate. "Ones" are then set into the OSR in accordance with the state of the system. In the case of data lines, either the contents of the Readout Location Register or the data from the appropriate address in memory is set in. At the beginning of a data line (Word zero) which coincides with the first 500 KHz clock pulse after the trailing edge of a main frame gate, the Submemory Location Register is set to zero (it has presumably already been indexed to zero at the end of MIT Word 8 but the positive reset improves reliability). A readout enable command is generated causing the contents of the RLR to be set into the OSR. No address search is required for this operation.

The bin number taken from the RLR is shifted out during gated MIT Word zero (Word zero AND Main Frame Gate). The end of the main frame gate initiates a reset of the OSR and the start of search for the address stored in the RLR. Adequate time exists between the time a readout enable command is generated at the end of a readout and the time and next main frame gate occurs to properly complete this search. This is accomplished by separation of the MIT words within the spacecraft main frame. Once the proper location in memory has been found, a Memory Read Command signal is generated. This signal is used to transfer the contents of the memory directly into the OSR. During gated MIT Word One, this number is shifted out to the spacecraft. The reset of the OSR, the index of the submemory, and shiftout on the next gated MIT word is repeated until all eight submemories have been interrogated.

During data block or format start lines, the same sequence is used except that no readout enable signal is generated. Format transfer commands are used instead to transfer the various bits of data from the appropriate registers.

3.4 Experiment Configuration Logic

3.4.1 Command Decode Logic - The command status of the MIT Experiment is shown in MIT Words four and five of every data block start line. The "normal" mode is defined as zero in each of the sixteen bits. Departures from the normal configuration are indicated by "ones" as shown on the format drawing (Section 3.3.1). The purpose of the command system is to provide for meaningful change in experiment configuration on command. This capability permits in-flight scientific evaluation of the experiment performance such as the relative efficiencies of the anticoincidence systems. It also permits engineering evaluation of the experiment operational status necessary to obtain a confidence factor for the data obtained. Of particular importance is the ability to logically disable any of the measurement chains selectively and to disable either the pulse shape discrimination or the self-anticoincidence. The logic which processes the command sequence is called the Command Decode Logic and is shown on Figure 3-18.

The purpose of the command sequence is to set or reset a particular bit in the Command Status Register. This is accomplished by setting the four-bit Command Decode Register to one of its sixteen possible states. Each state corresponds to one of the sixteen bits in the Command Status Register. The Command Decode Register drives the Command Status Bit Select Matrix which enables the chosen bit while inhibiting the clock inputs to all others. The next command in the sequence provides a clock pulse and a set or reset level the the chosen bit causing it to acquire the desired state. The outputs of the command status bits are used directly to implement the various configurations.

The command sequence is always in the following order:
a.) MIT Command 1,which resets the Command Decode Register;
b.) MIT Commands 2 through 5, which set bits 1 through 4 of the

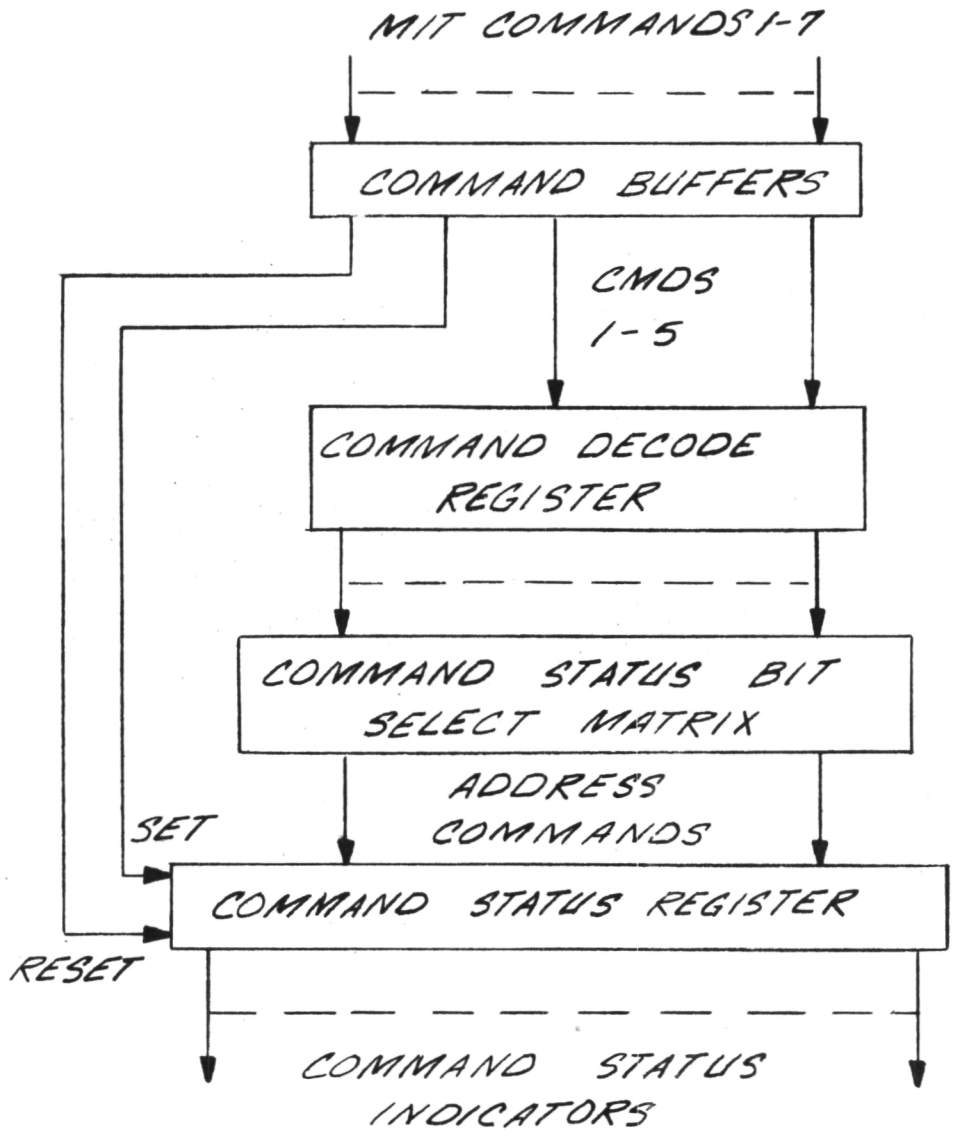

FIGURE 3-18
COMMAND DECODE LOGIC

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Command Decode Register as required; and c.) MIT Command 6, which generates a clock pulse and a set level in the command status register or MIT Command 7 which generates a clock pulse and a reset level in the command status register. Operations a.) and b.) are direct reset and set operations and require no clock pulse. In spite of the multiple command requirement for each configuration change, no difficulty will be encountered in completing an MIT configuration change within the pass at a single station. In fact, the worst case MIT command sequence, the Normal Mode sequence, can be completed within three minutes.

Table 3-5 lists the command sequence necessary to disable or enable each particular subsystem. Spacecraft (OSO System) commands are indicated. Commands WE/EW 56 through 62 are MIT Commands 1 through 7 respectively. All commands in this table may be sent through either spacecraft decoder EW or WE.

Table 3-5 MIT Command Sequences

Subsystems	Send	Then	Then, to Enable	Or, to Disable
High Voltage Protection	56	57	62	61
Auto Calibrate	56	58	62	61
Manual Calibrate	56	57 & 58	61	62
Counter 9	56	59	62	61
Counter 10	56	59 & 57	62	61
Counter 1	56	59 & 58	62	61
Counter 2	56	59 & 57 & 58	62	61
Counter 3	56	60	62	61
Counter 4	56	60 & 57	62	61
Counter 5	56	60 & 58	62	61
Counter 6	56	60 & 58 & 57	62	61
Counter 7	56	60 & 59	62	61
Counter 8	56	60 & 59 & 57	62	61
Geometric Antico	56	60 & 59 & 58	62	61
Risetime Antico	56	60 & 59 & 58 & 57	62	61
High Level Discriminator	56	None	62	61

The MIT Normal Mode sequence (sent at each experiment turn-on) enables all subsystems except the Manual Calibrators. Therefore, each command group in the Normal Mode sequence will end with WE/EW 62.

3.4.2 Orbit Counter - While the command system permits a number of variations in operating configuration in any sequence for any period, there are two operations which are best controlled automatically. These are the measurement chain multiplexing and the introduction of the calibration sources. These operations are controlled by the Orbit Counter.

The Orbit Counter is a five-bit serial counter which indexes at each transition from satellite night to satellite day without reset and, thus, turns over every thirty-two orbits. These orbits are numbered 0-31 in accordance with the Orbit Counter states.

Reference to the MIT Format (Section 3.3.1) shows that MIT Word 4 can contain data from either Measurement Chain 4 or 8 and similarly that Word 8 can contain data from either Measurement Chains 9 or 10. Data from Chains 4 and 9 are accumulated during even numbered orbits and data from Chains 8 and 10 are accumulated during odd number orbits. The state of the least significant bit of the Orbit Counter is used to control this operation. The multiplexing is required by the system power, size, and cost constraints. Primarily, the memory size is constrained to eight submemories rather than ten with appreciable saving in memory storage capability. Also, had not multiplexing been employed, the length of the format would approach a value where "smearing" of data from bin to bin, due to the increased accumulation time and the resultant change in orbit position, would begin to become a problem.

The calibration system discussed below is divided into two subsystems, each of which is normally energized for an entire

orbit once every 32 orbits. To reduce peak power (which is required for an entire orbit),these subsystems are energized alternately on Orbits 0 and 1. The state of the Orbit Counter is decoded by the Orbit Counter Decode Matrix.

3.4.3 Radiation Monitor - The orbit of the OSO spacecraft will enter portions of the inner radiation belt for short periods of time. During this time,the proportional counters, if left energized, would be subjected to such high rates that the counter life which is expressible in a finite number of counts could be significantly reduced.

A halogen-quenched mica window geiger counter is used to monitor the background radiation. Use of the halogen quench provides an essentially infinite life. This quench is not feasible for the larger proportional counters with their metallic windows. When the background rate exceeds a preset rate, the high voltage supply to each of the proportional counters is turned off. When the rate again drops below the threshold, the high voltage is restored. A bit in the format indicates whether or not the high voltage is being applied. The monitor system can be disabled on command.

3.4.4 Calibration System (also Section 3.1.4) - The calibration system is composed of two identical subsystems. Each of these subsystems is essentially a pair of radioactive sources of one or more components contained in a shielded box which have shielding shutters. Opening of the shutter permits the radiation to enter the appropriate proportional counter system.

Opening of the "lower" shutter (near the baseplate) occurs automatically on MIT orbit zero calibrating counter systems 1, 2, 3, 4, and 9. Opening of the "upper" shutter occurs similarly on MIT Orbit 1 calibrating 5, 6, 7, 8, and 10. Automatic

calibration can be disabled on command. Manual calibration (actuation of both shutter systems simultaneously) may be enabled on command. Manual calibration causes the instrument to operate outside its assigned power budget and its use would be abnormal in flight.

3.5 Analog Measurements (Housekeeping Data)

3.5.1 Analog Format - Four analog measurement lines are provided to the MIT Experiment (WASC 35, 36, 42, and 43). One line is used for MIT analog sub-subcommutator sync, the other three monitor a total of twelve instrument voltages and temperatures. The signals found on each of the MIT lines are given in Figure 3-19. Expected limits are indicated where applicable. These levels and the calibration table which follows in Section 3.5.4 may be taken as representative of the Flight Spare Unit (S/N No. 1) but apply accurately only to the Flight Unit (S/N No. 2) which is on board OSO-7.

One such analog format is generated every four MIT digital blocks. Analog data advances from block to block at the end of each digital block start line. More precisely, it changes on the trailing edge of the Main Frame Gate that transfer Word 8 of the block start line to the spacecraft.

Since the Wheel Analog Subcommutator (WASC) and MIT Data Block are not synchronous, as few as six or as many as eight analog words may be read out each MIT digital block. Determining which of these words belong to a common analog block involves recognizing the three block or format sync words in the MIT digital data and taking the four MIT analog words previous to it. WASC-35 which contains the MIT analog sync word may also be identified as the first MIT word after WASC-48, wheel analog sync.

	Line #1 WASC-36			Line #2 WASC-37			Line #3 WASC-42			Line #4 WASC-43		
	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX	MIN	TYP	MAX
Block #1	Sync #1			Plus 10 volts			Plus 5 volts			Minus 6 volts		
	0v	0.2v	0.4v	2.5v	2.7v	2.8v	3.85v	4.00v	4.05v	1.6v	1.7v	2.0v
Block #2	Sync #2			3kv Monitor			470 Monitor			Plus 8 volts		
	0.5	0.7	0.9	3.1	3.2	3.5 (norm)	2.1	2.3	2.5	1.80	1.95	2.00 (orbits 0,1)
				0	0	0.5 (HV OFF)				0	0.25	0.50 (other orbits)
Block #3	Sync #3			Power Converter Temperature			Baseplate Temperature			Calibrate Actuator Temperature		
	1.0	1.45	1.90									
Block #4	Sync #4			Memory Temperature			Lower (1°) Counter Temperature			Upper (3°) Counter Temperature		
	2.0	2.5	3.0									

Figure 3-19 MIT Analog Signals. (All levels in volts.)

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3.5.2 Measurement System

3.5.2.1 Operation - A two-bit binary counter triggered by the trailing edge of the "Block Start Line" pulse cycles the sub-subcommutator through its format (Figure 3-20). Four state decode gates operate the analog gates driving lines 2, 3, and 4 (WASC 35, 42, and 43) and connect one of the four analog inputs to the associated output line. Analog sync is derived from a ladder network and the counter high side outputs. Voltage samples are taken directly from each source. Temperatures are derived from the thermistor network shown in Figure 3-21. Although such a series network does not have the linearity or ultimate accuracy of the more common bridge network, its performance is up to the task and its simplicity is advantageous.

3.5.2.2 Thermistor Locations - Certain of the thermistor locations are identified on the top assembly drawing (Section 3.0) and in Figures 3-2 and 3-3. Most are hidden from view. Here is a list of the six thermistor locations in the instrument:

1. Baseplate - located near the center line of the instrument just to the rear of the detector brackets and about 5 cm (2-1/2 in.) ahead of the electronics box.
2. Memory - located near the center of Motherboard F (see Section 3.7.1).
3. Power Converter - located about 4 cm (1.57 in.) from the wide end of the converter on the printed circuit board just below the top cover and in line with the connector.
4. Calibrate Actuator - located near the bottom of the printed circuit card mounted on upper actuator.

5. Lower (1°)
   Counter - located near the instrument center line over Counter 4 on the baseplate side.

6. Upper (3°)
   Counter - located near the instrument center line over Counter 8 on the top (exposed) side.

In each case the thermistor is located on a mounting card which imposes one-sixteenth inch of fiberglass epoxy (G-10) material between itself and the surface of measurement.

3.5.3 Precision and Accuracy - Precision is determined solely by the spacecraft eight-bit quantization of the analog signal which is 19.6 millivolts per bit.

Accuracy is determined primarily by component variations with temperature and calibration accuracy.

3.5.3.1 Voltage Measurements - Within the most likely operating range of 0°C to +25°C accuracy is determined by changes in divider ratios. For all voltage outputs accuracy to ±1% of the measured parameter is achieved using the calibration curves supplied. Voltage measurements more than ±1 volt from nominal are subjected to additional errors (see Section 3.5.3.3).

3.5.3.2 Temperature Measurements - Based on calibration runs made in thermal-vacuum during acceptance testing, temperatures can be expected to be with ±0.5°C of the calibration curve barring changes in the 5 volt supply.

3.5.3.3 Limits on Calibration Accuracy - The following comments apply to the analog calibration:

1. If the plus 5 volt supply drops below 4.0 volts, all calibration curves are suspect due to saturation voltage changes in the analog gates.

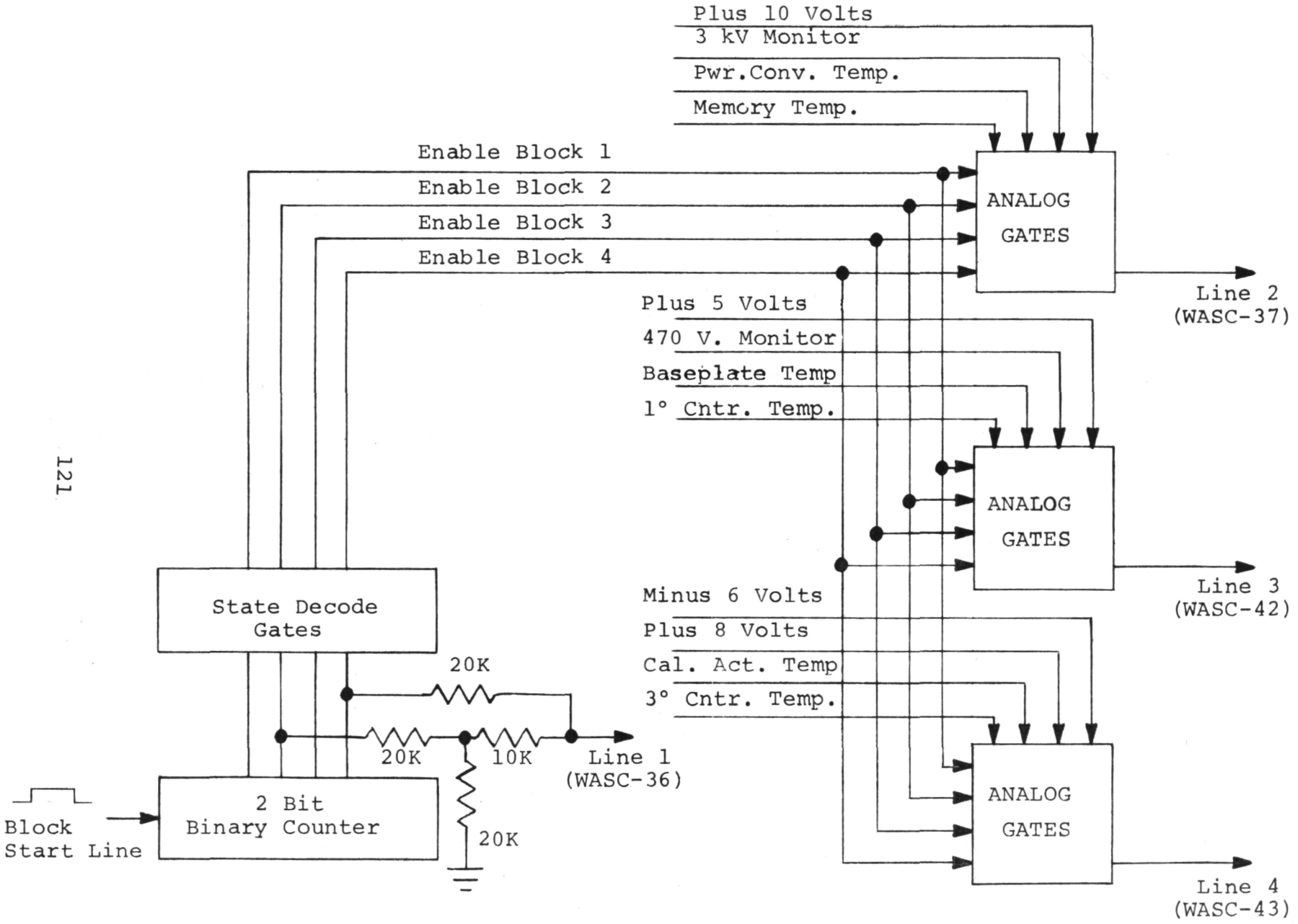

Figure 3-20 Analog Sub-Subcommutator.

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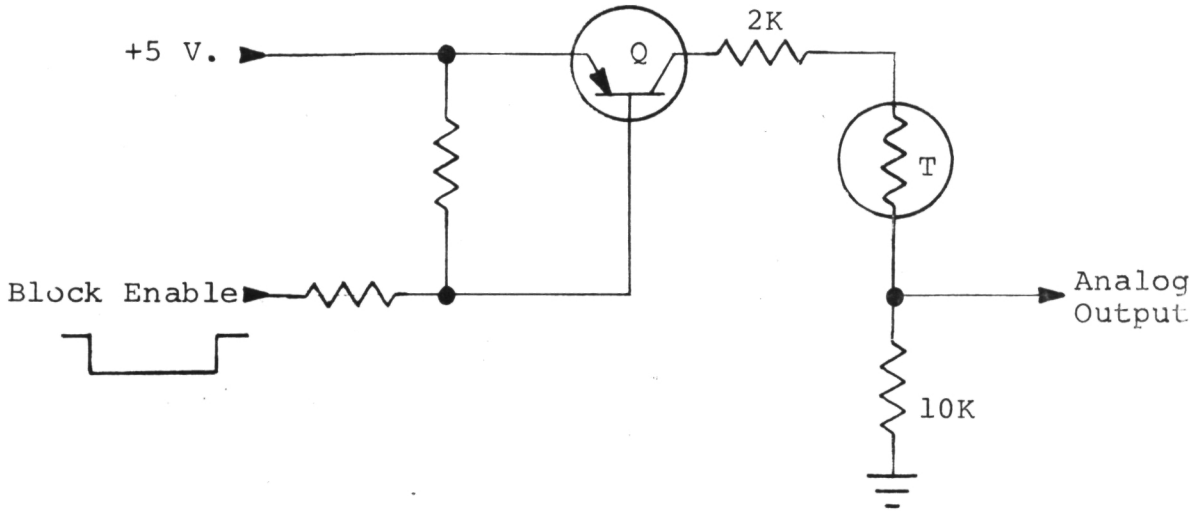

Figure 3-21 Typical Thermistor Network

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2. Changes in the plus 10 volt supply are reflected in the minus 6 volt readout in the ratio 0.69. That is, a change in the 10 volt supply of 1 volt causes a change in minus six volt analog output of 0.69 volts.

3. All curves on Analog Line 4 are functions of calibrator voltage. To a first approximation, linear interpolation may be used between the curves for the ON and OFF conditions. The ON curves correspond to the orbital situation of one calibrator on at a time or a plus 8 volt supply voltage of 7.94 volts.

4. Voltage calibration curves are given values down to zero in spite of lack of linearity beyond ± 1 volt from nominal so that data presented in terms of instrument parameters (e.g., plus 5 volt supply) can be easily translated back to actual sub-subcommutator output voltage.

3.5.4 Calibration Data - Calibration curves for the MIT housekeeping data have been published by Ball Brothers Research Corporation (Boulder, Colorado) in publication number TN69-23, "OSO-H Telemetry Data Conversion Tables".* These curves are straight lines and are expressed algebraically in Table 3-6. The desired voltage (V) or temperature (T) is expressed in terms of both analog output voltage (V_0) and digital counts (C).

Table 3-6 MIT Analog Calibration

Parameter	Analog Output Voltage (V_0)	Counts (C)
Plus 5 volt supply	$V=1.22V_0$	$V=0.0239C$
Plus 10 volt supply	$V=3.64V_0$	$V=0.0713C$
Minus 6 volt supply (Cal. ON)	$V=-3.02V_0+11.95$	$V=-0.0593C+11.95$
(Cal. OFF)	$V=-3.42V_0+11.95$	$V=-0.0672C+11.95$

*Available from Goddard Space Flight Center, Greenbelt, Maryland.

Parameter	Analog Output Voltage (V_0)	Counts (C)
Plus 8 volt supply	$V=3.86\,V_0$	V=0.0758C
Power Converter Temperature	$T=25.80V_0 -28.40$	T=0.506C-28.40
Baseplate Temperature	$T=25.45V_0 -27.45$	T=0.499C-27.45
Calibration Actuator Temperature (Cal.ON)	$T=25.80V_0 -27.85$	T=0.506C-27.85
(Cal.OFF)	$T=29.85V_0 -30.75$	T=0.586C-30.75
Memory Temperature	$T=25.30V_0 -30.40$	T=0.497C-30.40
Lower (1°) Counter Temperature	$T=26.10V_0 -27.40$	T=0.513C-27.40
Upper (3°) Counter Temperature (Cal.ON)	$T=23.80V_0 -28.60$	T=0.466C-28.60
(Cal.OFF)	$T=27.40V_0 -29.30$	T=0.537C-29.30

3.5.5 Design Comments - The use of transistors as analog gates in this system led to a number of interaction and nonlinearity problems which have only been partially overcome. One manifestation of the interactions is seen in the requirements for two calibration curves for all the analog words on WASC-43. The presence of the 8 volt supply causes all voltages on this line to increase by about 10% and requires different calibration for each condition.

Strictly speaking, the calibration curves are accurate only when all supply voltages are near ($\pm$1 volt) their nominal values. Deviations of any voltage will cause slight shifts in all the calibration curves applicable to a common output line. These interactions are due to forward bias of collector-base junctions in "OFF" gates and through "sneak paths" in the Block Enable signals.

MOS Field Effect Transistor Analog gates would seem preferable in this application. Many of the sneak paths would automatically

be eliminated (due to the excellent gate isolation) and voltage offsets removed as well. In most cases,since a negative voltage is available, input-output linearity could be maintained almost down to zero volts. Analog data reduction would thereby be simplified and accuracy improved as well.

The problems associated with location of analog sync have been discussed. A more straightforward approach to sub-subcommutation would, say, trigger the analog format on each spacecraft analog sub-subcommutator sync word (WASC-48, here). Such a signal was not available to the MIT instrument on OSO-7 but should be considered for use in future applications.

3.6 Power Converter

3.6.1 Description - This converter is the only source of supply voltages, both high and low, for the MIT Experiment. It has been configured in such a way as to minimize regulator and converter standby power. Because of the pulsed loads on the converter generated by the active shift register memory of the experiment and the pulse powering of certain subsystems, the design of the converter is not trivial. "Switching" and series-regulator type converters were considered. Switching regulators are inherently efficient and were attractive but not used because of the high frequency required to track the pulsed loads of the MIT instrument and the attendant noise problems. Tight input series regulation is the optimum design to meet the pulsed load regulation and OSO noise requirements. The major load is the plus 5 volt DC load which is composed of integrated circuit logic. The necessary regulation on this line is accomplished solely through the use of the input preregulator. The preregulator produces a regulated voltage exhibiting tight control which serves as the input to regulator systems for the other outputs. The plus 5 volt output is sampled to control the preregulator. Regulation of this line

is extremely important for two reasons. First, the operation of the system is predicated upon the 5 volt line staying above 4.5 volts regardless of the pulsing load which certain subsystems exhibit. Secondly, it is important that the 5 volt line be constrained to no more than plus 5 volts. This poses a constraint on the set point as well as the regulation and is intended to ensure that minimum power is drawn by the experiment. Because of the magnitude of the load on the 5 volt line, a slight change such as from 5.0 to 5.1 volts would result in an increase in experiment power of 135 milliwatts.

In addition to the plus 5.0 volt output, a 10.0 volt, plus 8.0 volt, and minus 6.0 volt output are required. The plus 10.0 volt output,while exhibiting an average current of only 10.5 ma, reaches peak values of 155 ma for periods of 5 milliseconds. Comparable pulse factors exist on the minus 6.0 volt line. The plus 8.0 volt output drives the calibration actuators only and is enabled only when the actuators are needed.

Regulation of the plus 5 volt line is achieved by the input preregulator only (see Figure 3-22). Input-output ground isolation is maintained by the use of a separate transformer winding for the feedback loop. Ground isolation is a spacecraft requirement and is maintained throughout the MIT instrument. The input and output grounds are called power and signal ground, respectively. Chassis ground is maintained as separate entity as well.

The preregulator controls the flux in T1 to precondition all other regulator inputs. Series post-regulation is used in the plus 10 volt and minus 6 volt lines to handle the load pulsing present on these outputs. To minimize loading on T1, and thereby interference with other regulators, a separate drive amplifier is provided for the plus 8 volt supply. As the load voltage regulation requirements are loose (7.5 ± 0.75 v),only input regulation to this amplifier is used, no series post-regulator is required.

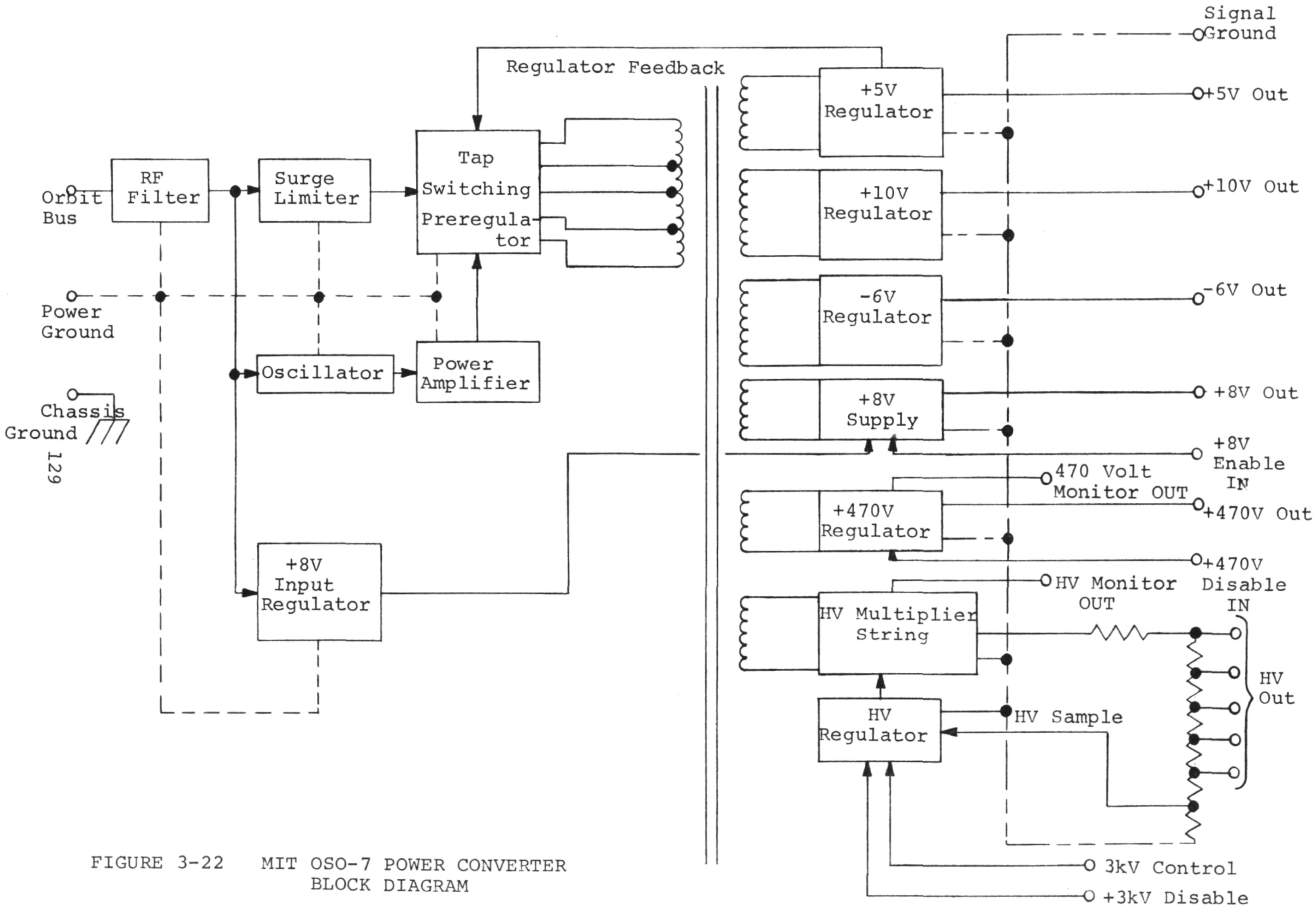

FIGURE 3-22 MIT OSO-7 POWER CONVERTER BLOCK DIAGRAM

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There are two types of high voltage outputs. The first of these is a fixed high voltage at approximately 470 volts. This output is not particularly critical with respect to regulation as it supplies the radiation monitor halogen-quenched geiger tube. The other high voltage output is, however, highly regulated with respect to line changes, noise, and ripple. This high voltage output is subdivided to provide the five high voltages for the five proportional counter chambers used in the experiment (four chambers in the four-chamber counter and one chamber in the thin window counter). Since tight control of the proportional counter's configuration is maintained,a given high voltage can be used in both the upper and lower banks of the experiment. The various high voltages are obtained by precision resistor division from a base voltage of approximately 2700 volts.

The 470 volt and HV outputs can be individually disabled by grounding the 470 volt Disable and HV Disable lines, respectively. The HV output can also be disabled by applying plus 5.0 volts to the HV Control line. Activation of the radiation Monitor (Section 3.4.3) disables the high voltage in just this manner.

OSO specifications caused certain input circuits to be required. Noise requirements led to extensive filtering of the input power, power ground, and signal ground leads at frequencies above 10 KHz. A surge limiter was required to meet turn-on specifications without sacrificing low frequency pulsed load filtering in the input and tap switching was required in the input preregulator to keep the power increase from an orbit voltage of plus 16 to plus 22 volts within bounds. Tap switching occurs automatically at about plus 18.5 volts on the input terminals.

Since the operating characteristics of proportional counters are a critical function of operating voltage, an HV monitor voltage is provided.

This voltage is erected from a winding on the transformer that drives the HV multiplier string and provides a means of inferring HV stability. A similar monitor voltage is provided for the +470 volt output.

The converter is current limited. A short (or no-load condition) on the plus 5 volt output will shut down the converter. Shorts on any of the other outputs will not shut down the converter but will not damage it either. Once the converter has shut down and the short condition cleared, a one minute waiting interval is necessary to allow the input circuits to stabilize ensuring a successful turn-on and keeping the turn-on surge within specification.

3.6.2 Converter Performance

3.6.2.1 Regulator Performance - The following full load data (Table 3-7) was obtained from the Flight Converter incoming test results. All are for an Orbit bus voltage of plus 19.0 volts. A list of high voltage outputs is available in Section 3.1.1.4.

Table 3-7

Full Load Regulator Performance of the MIT Flight Power Converter

Temperature	+5v	+10v	-6v	+8v	470v	HV	HV MON	470 MON
+40°C	4.96	9.96	6.06	$\frac{8.04^{*}}{7.63^{**}}$	474.5	2540	4.37	3.94
+25°C	4.95	9.94	6.05	$\frac{7.94^{*}}{7.55^{**}}$	474.5	2540	4.29	3.90
-15°C	4.94	9.88	6.05	$\frac{7.64^{*}}{7.29^{**}}$	473.7	2540	4.20	3.86

*Auto Calibrate, Orbits 0 and 1.

**Manual Calibrate, both actuators on.

3.6.2.2 Noise Performance - The following data was taken during interface testing at Ball Brothers Research Corporation (Boulder, Colorado). All noise voltages are peak-to-peak values and are generally at the converter operating frequency. A low frequency pulse on power ground and the orbit bus due to reflected load variations is not included in these figures. All are taken at plus 19 volts.

Line	Noise Voltage (millivolts)
Orbit	10
Power Ground	20
Chassis Ground	30
Signal Ground	50

Other parameters include:

Turn-on Surge: 800 ma peak, complete in 0.3 seconds.

Reflected Load Variation: 30 mv peak-to-peak for 5.0 ms during each Digital Main Frame Gate.

3.6.2.3 High Voltage Load Capability - A load test of the Flight Power Converter at 27°C indicated that the high voltage section would drive a 400 Megohm load without loss of regulation (see also Section 3.6.3.2).

3.6.3 Design Comments

3.6.3.1 Ground Isolation - The requirement for isolating signal, power and chassis ground from one another in this converter compounded an all ready difficult noise problem. Interwinding capacity in the main transformer (T1) causes currents to flow between the signal and power ground referenced windings which must be satisfied through the isolated ground lines as a noise voltage. Capacitive coupling between transformer windings and the chassis causes similar currents which

must be satisfied in a like manner through all of the other ground leads. Capacitive bypassing can modify these current paths, but they are sufficiently complex that only a single point ground within the converter would control them completely. A change in interface requirements that would allow signal and power ground to be tied within the converter would have eased the noise problems considerably.

3.6.3.2 Safety Resistors and Converter Load Requirements - It is desirable to protect the converter against counter short circuits. Counter anodes are delicate structures. One anode failure could make the entire counter complement inoperative due to a short circuit on a converter HV output. Series resistors are a convenient means of isolating the counters. Their value can be quite high (well into the 10^9 ohm range) without disturbing the counter voltages as normal counter currents are in the picoampere range. In the MIT instrument, 1000 Megohm resistors are used on the upper HV taps (Counters 3, 4, 7, and 8) and 5000 Megohms on the lower HV taps (Counters 1, 2, 5, 6, 9, and 10). Resistor selection is based on the criterion that two anode shorts must not prevent the operation of the remaining counters. In the upper taps, the converter source impedance is only in the Megohm range and the amount of current the converter can supply is the limiting factor. In the lower taps, the source impedance can be as high as 60 Megohms and the limiting criterion is the acceptable voltage change on the upper taps when the lower safety resistor outputs are shorted.

It was necessary in this instrument to use printed circuit mounting for the safety resistors and other high voltage components. Normal component, printed circuit card, and conformal coating leakage currents combine to cause voltage loss across these resistors. Surface contamination, with the resulting

additional currents, only increases this voltage drop. Consider that only 20 na of leakage through a 1000 Megohm resistor is required to significantly change the operating point of a counter and the magnitude of the problem becomes apparent.

In future applications it would be advisable to limit counter series resistors to 100 Megohm. This would completely eliminate these leakage problems and decrease HV response time as well. Converter HV current handling capability should be specified on this basis rather than from a consideration of proportional counter current requirements.

3.6.3.3 HV Time Constants - The HV safety resistors and filter capacitors determine the HV response time.

Chains	Safety Resistor x $10^9 \Omega$	Time Constant Seconds
1, 2, 5, 6, 9, 10	5	45
3, 4, 7, 8	1	9

No converter HV output will settle completely until all have stabilized due to interactions in the divider chain and feedback loop. Five time constants or 255 seconds must be allowed to elapse after any HV changes before critical counter measurements can be made. At turn-on, this period plus one full data format must go by before data rates may be considered accurate.

3.7 Electronic Packaging

Printed circuits are used throughout the instrument for mounting of electronic components. Rail:Motherboard and Module: Motherboard systems are used for discrete and integrated circuit (14 lead flatpack) mounting, respectively. Except for the

measurement chain low level amplifiers and high voltage filter-boards all MIT fabricated electronics reside in the "Electronics Box" (Figures 3-2 and 3-3).

3.7.1 "Electronics Stack" - Figure 3-23 is a photograph of the prototype Electronics Box with one side removed to show the motherboard stack. This photograph was taken before any epoxy or conformal coating operations had been performed on the boards and is not representative of the final appearance of the stack but it does show the packaging configuration used in the experiment. Flat motherboards, cut to the shape of the rear of OSO compartment three, hold rails and "T" modules for the subsystems. The stack is divided into three groups. The bottom group contains the Sequencer, Bin Width Logic and Format Logic. The middle group (four boards) is the Memory and the upper, the Measurement Chain Logic and a cable routing board. Motherboards are lettered starting with A on the bottom through J on the top. The upper board in the figure which would be K is called the Cable Routing Board and serves to interface the connector cable bundles with the stack.

Interconnections within groups are made by peripheral pins wherever possible. Connections between groups is by cable harness. All cable harnesses run up and down the forward (wide) end of the stack so that the motherboards may be separated like the pages of a book.

Here is a list of the motherboards and the functions performed by each:

Motherboard A: Bin Width Logic (Section 3.2.1.2).

Motherboard A1: Aspect System (Section 3.2.1.1) and Calibrate Actuator coil drives (Section 3.4.4). This is a "submotherboard" located over the narrow end of Motherboard A.

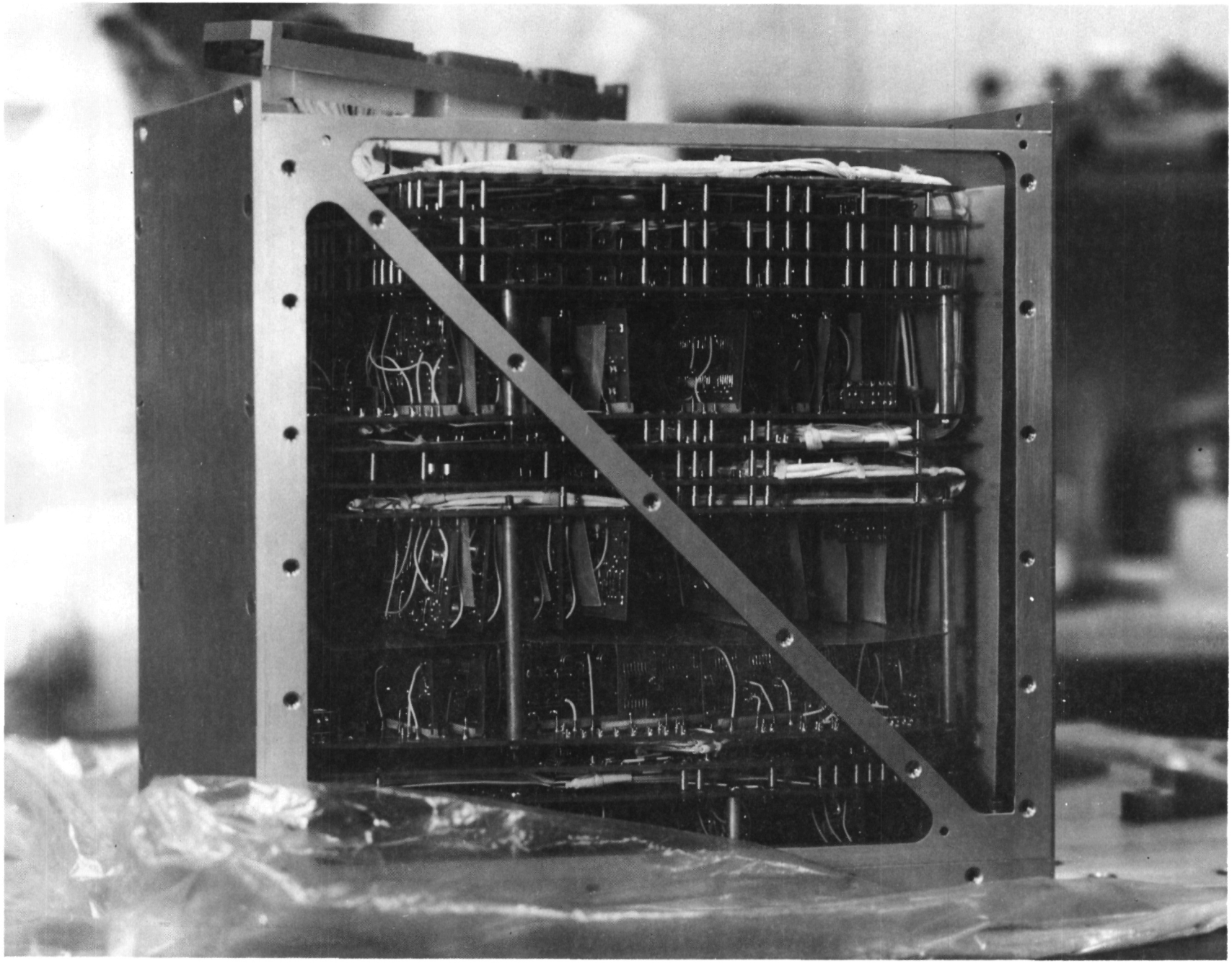

FIGURE 3-23. PROTOTYPE ELECTRONICS BOX. THE ELECTRONICS STACK IS SHOWN PRIOR TO EPOXY OPERATIONS.

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Motherboard B: Sequencers (Section 3.2.2).

Motherboard C: Format Logic (Section 3.3).

Motherboard D: Submemories 0, 1, 2, and 3 (Section 3.2.3).

Motherboard E: Clock Line Drivers for the Memory.

Motherboard F: Format Logic (Section 3.3) and Memory Input Logic.

Motherboard G: Submemories 4, 5, 6, and 7.

Motherboard H: Measurement Chain Logic (Section 3.1.3) for Chains 1, 2, 3, and 4.

Motherboard I: Measurement Chain Logic (Section 3.1.3) for Chains 5, 6, 7, and 8.

Motherboard J: Measurement Chain Logic (Section 3.1.3) for Chains 9 and 10, analog sub-subcommutator (Section 3.5.2) and the experiment dummy load.

3.7.2 Packaging Techniques - Representative packaging techniques are covered. Unfortunately, photographs of all areas are not available.

3.7.2.1 Measurement Chains

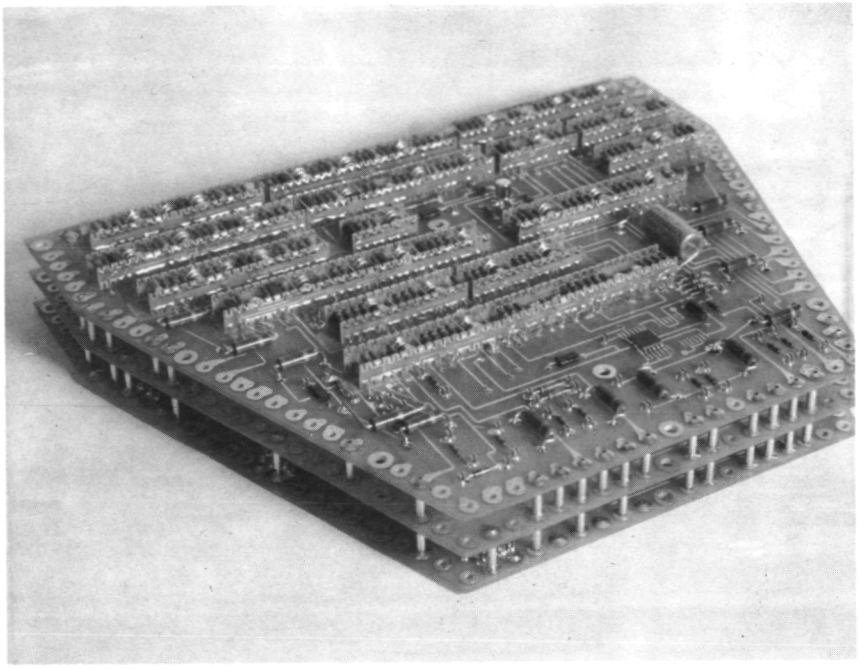
1. Logic - The measurement chain logic is entirely of discrete components and is wholly contained on Motherboards H, I, and J. These motherboards are shown in the top photograph in Figure 3-24. Motherboard J is uppermost and is typical of the construction of H and I. Note the use of peripheral pins for board interconnection.

2. Analog - The bottom photo in Figure 3-24 shows the amplifier and preamplifier boards for a four-color counter. Upper left is an amplifier board for the front three chambers and upper right is a preamplifier board for the same. These stack in the deep end-well of the four-color

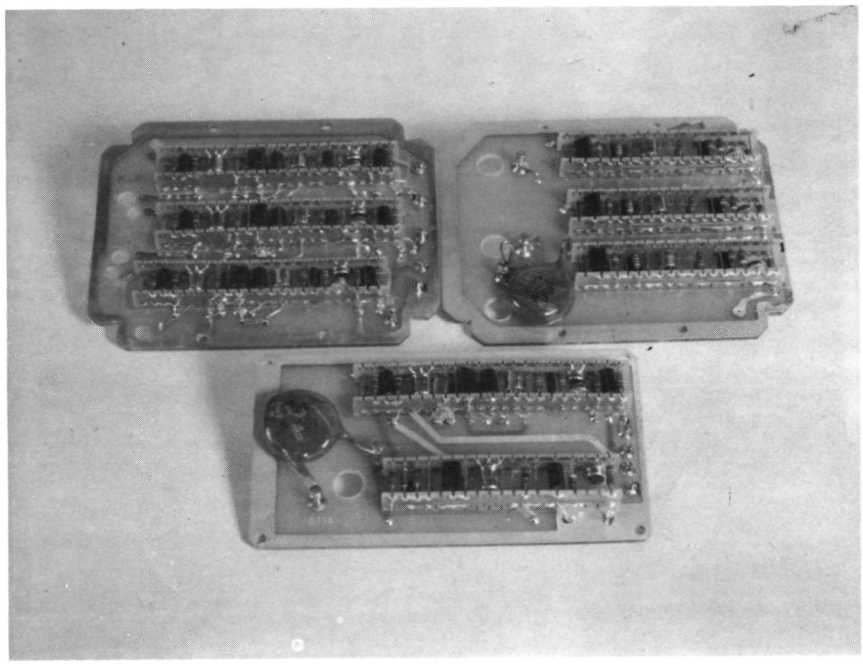
counter (Section 3.1.1.2). Below these is a combination amplifier-preamplifier board for the rear (Xenon) chamber.

3.7.2.2 Memory - Figures 3-25 and 3-26 show details of the Memory construction. Four motherboards are used. Peripheral pin interconnections between the boards carry logic signals. Shielded cable carries the high amplitude clock signals from Motherboard E to Motherboards D and G. As can be seen, "T" modules are used for most memory logic and connections made to the motherboards by flexible wire and bus-bar. Bus-bar is used only for connections from modules that are within 1.2 cm (1/2") of the motherboard. In the submemory detail (Figure 3-26) the boards visible in the center of the picture are "Dual Storage Modules" each of which contain two 300-bit shift register chains with the associated interface circuits and read-write logic. The ground control (pulse power) module is the small rail on the left of the motherboard.

3.7.2.3 Logic System - Motherboard C (Format Logic) is typical of the construction of the logic system and contains examples of all the types of construction used in the MIT instrument. Figure 3-27 shows "T" modules (as are used in the Memory) and Three-High rail construction. Three-High rails contain 3 levels of discrete components. The "T" modules mount both integrated circuits in 14-lead flatpacks and a small quantity of discrete logic. Four-High and Two-High rails are shown in Figure 3-28. This is the only Four-High rail in the system and is a diode-resistor matrix functioning in the format word decode logic. A second arrangement unique in the system is the rail on the "T" module visible just above the Two-High rail. The integrated circuit modules, incidentally, are called "T" modules because in their original form a cross piece was included on the bottom of each module for the mounting of connecting pins.



Signal
Processing
Boards



Amplifier and
Preamplifier
Boards

FIGURE 3-24 MEASUREMENT CHAIN MOTHERBOARDS

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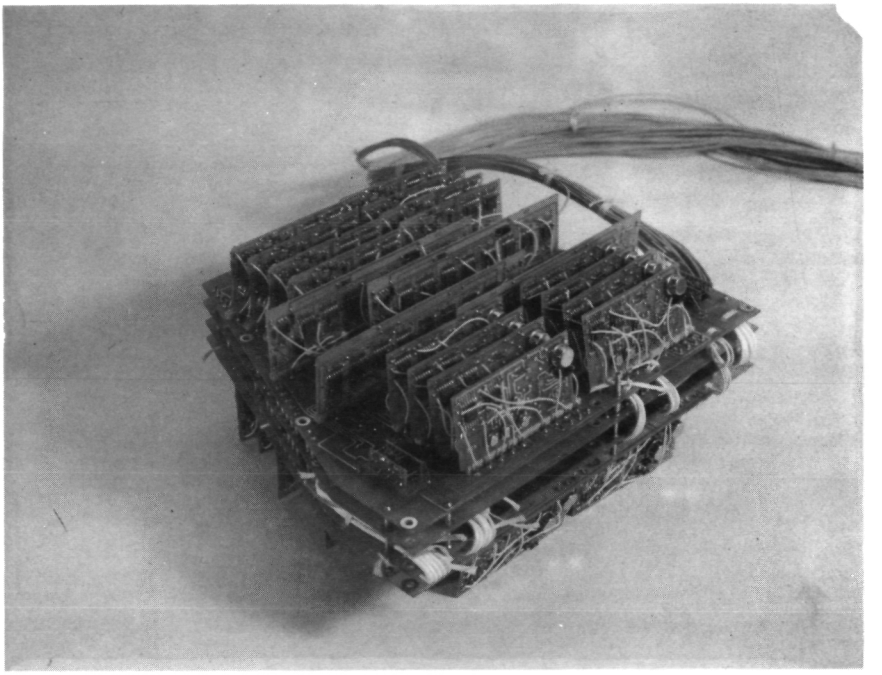

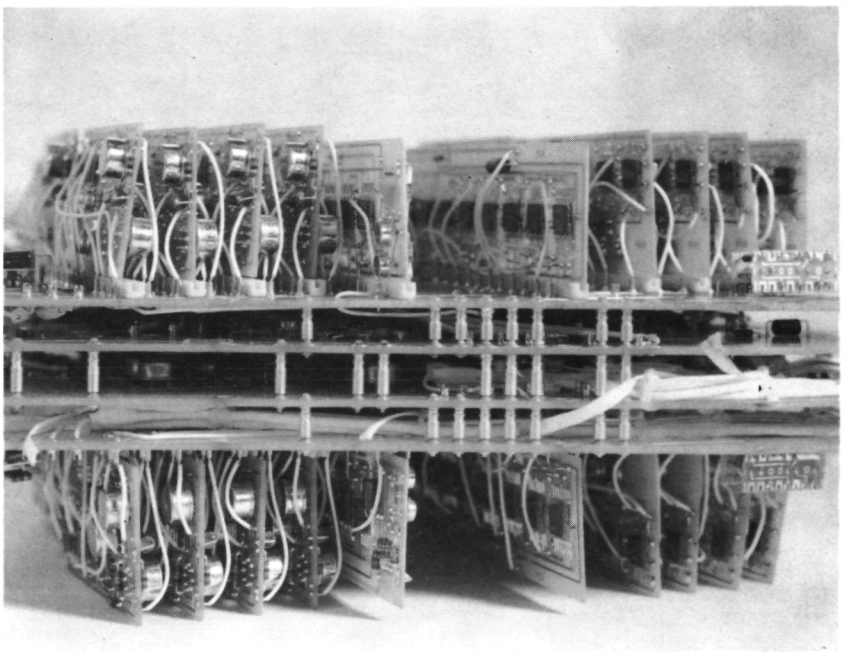

Board
Interconnection
System

Figure 3-25. MIT OSO-7 PROTOTYPE MEMORY

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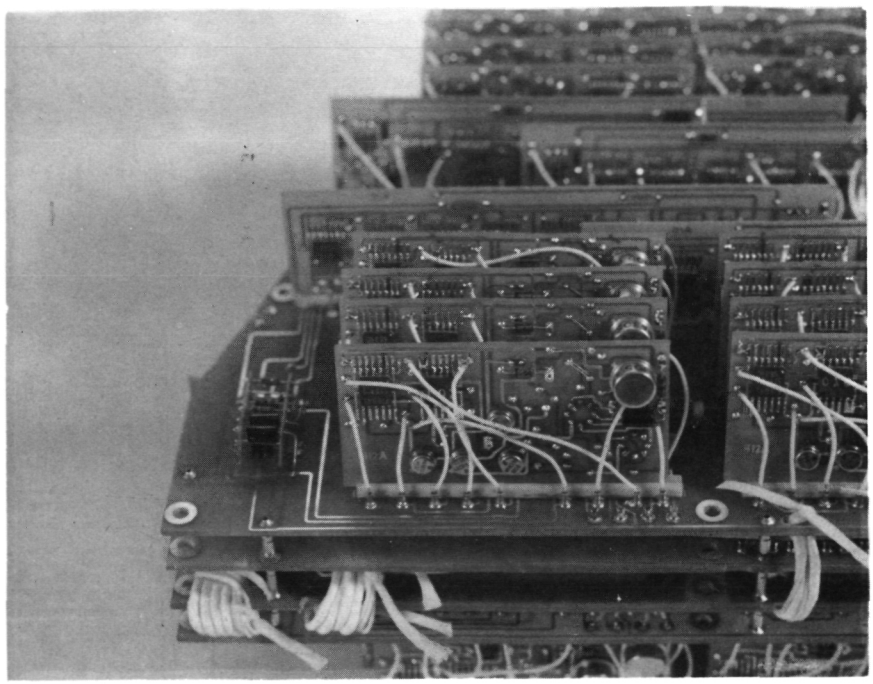

Figure 3-26. TYPICAL 2400 BIT SUBMEMORY

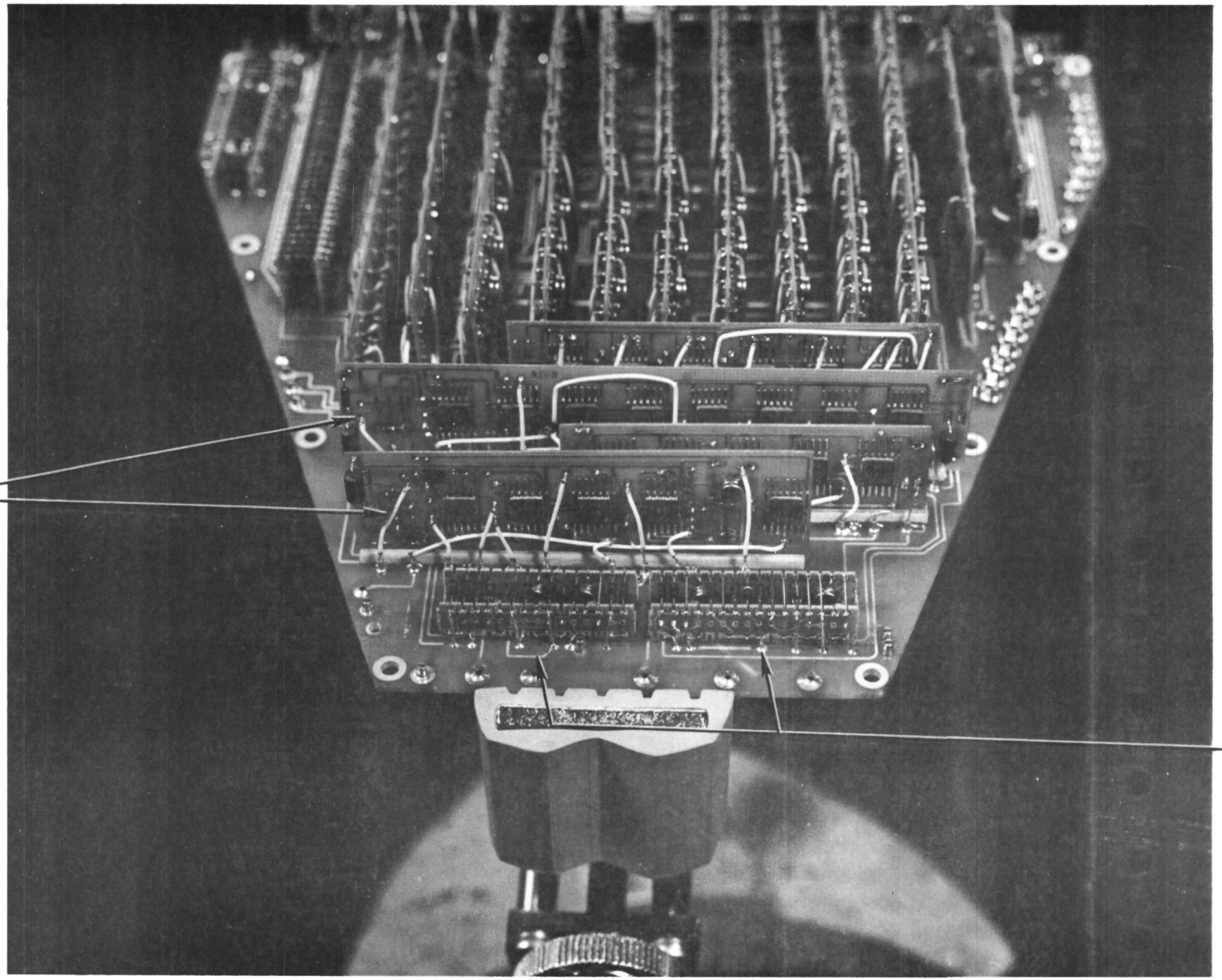

FIGURE 3-27. MOTHERBOARD C T- MODULES AND THREE-HIGH RAILS.

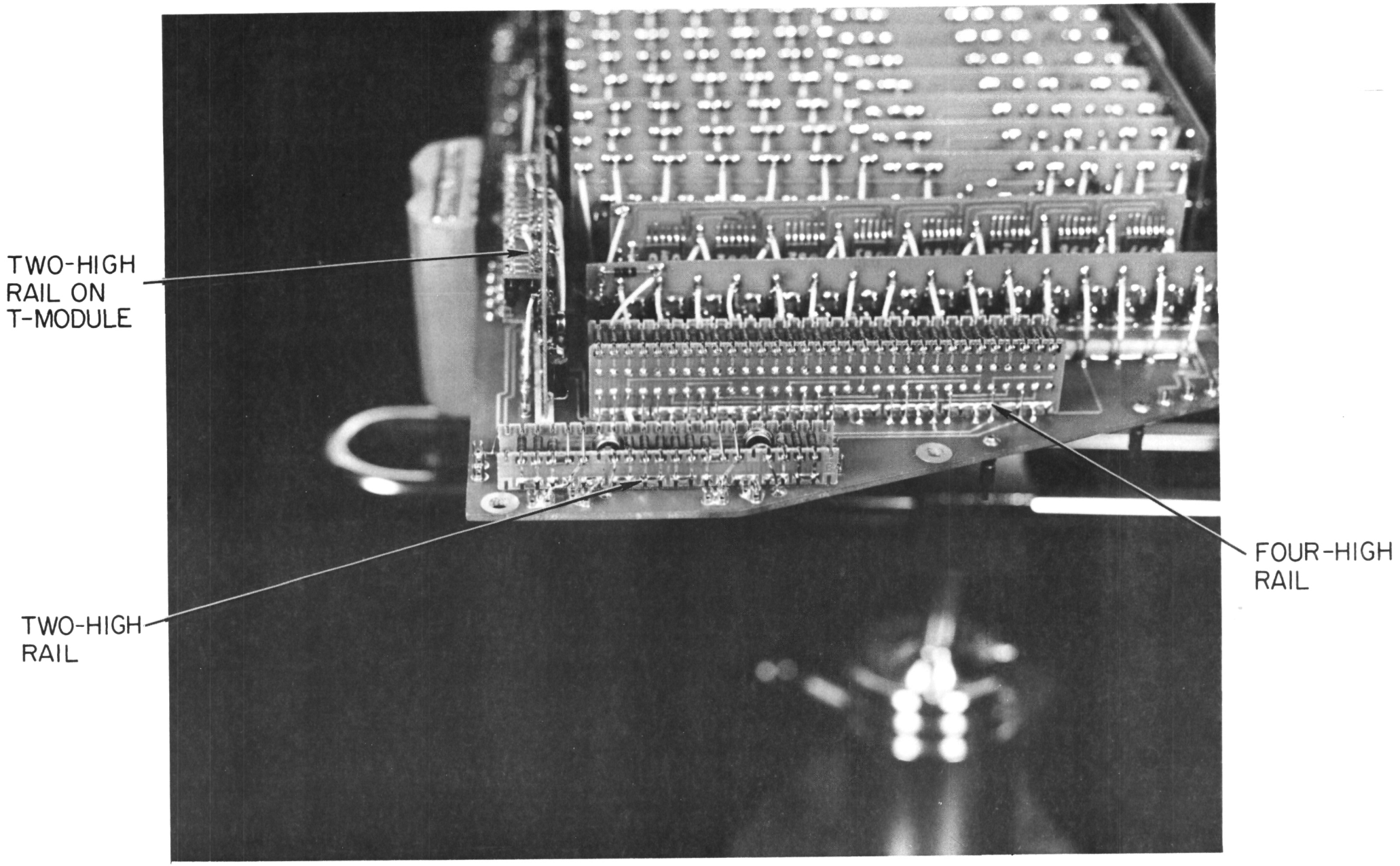

FIGURE 3-28. MOTHERBOARD C – FOUR-HIGH RAIL AND TWO-HIGH RAIL.

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In use, the module formed an inverted "T". As the design evolved, the connecting pins and cross piece were deleted but the name remained.

3.7.2.4 Counters - Counter mounting arrangements are shown in the Top Assembly drawing (Section 3.0) and in Figures 3-2 and 3-3. Each counter is secured by machine screws through the detector side brackets. Electrical connections on both the low voltage (amplifier) end and high voltage (filterboard) end are made by soldering wires from the cable harness to terminals on the motherboards. The Thin Window Counters (9 and 10) are attached to the cable harness by a service loop visible in the central portion of each detector bracket. This loop is just long enough to allow pulling the counters out the front of the instrument (after the collimators and calibration actuator are removed) to provide access to the terminals on the back of the counter. The top assembly drawing shows these terminals.

3.7.2.5 Radiation Monitor - The radiation monitor control logic is mounted in Motherboard J. Its high voltage filter and input integrator board is mounted on the small 1° collimator (see the Top Assembly drawing, Section 3.0). Connections to the Radiation Monitor are made from the same cable bundle that connects to Counter 9.

3.7.3 Ground System - Particular attention was necessary to ground current control because this instrument is simultaneously noisy due to power converter switching and memory pulsing and sensitive because of the high impedance measurement chain inputs. Compounding the problem was the necessity of maintaining the counter bodies and detector mounting brackets at signal ground while isolating them from chassis

ground (at which the baseplate and electronics box sit). Some of the problems involved in maintaining ground isolation have been discussed in connection with the power converter* (Section 3.6). Detector bracket isolation is achieved by the use of a fiberglass epoxy (G-10) spacer and insulating washers between the detector brackets and the baseplate (Figure 3-1). Schemes for operating the entire instrument chassis at signal ground and isolating it from the spacecraft chassis were considered and discarded because of the resulting poor thermal connection between the instrument and spacecraft.

Within the electronics stack all noise producing wires such as the shift register clock lines and all noise sensitive wires such as the measurement chain outputs and high voltage lines were shielded. As an extra precaution, because of the large cable bundles involved, shielding was extended to those digital signals where eight or more such signals could occur simultaneously and to all digital lines at higher than DTL levels. A ground plan was developed that located the signal ground common knot in the memory on Motherboard F. All instrument signal grounds were returned to this point without ground loops from subknots located in the lower and upper motherboard groups, the power converter, and the detector bracket assembly. In a number of cases, primarily involving long runs such as from the stack to the detector brackets, the signal ground wires were themselves shielded and their shields returned to the common knot by the shortest possible path. Shields were carried through the non-shielded connectors to the stack.

These precautions paid off. With the exception of one problem involving noise induced into the measurement chain from the high voltage shields there were no noise problems in the instrument. This in spite of the fact that memory high speed cycling (which is a continuous process) involves 100 nanosecond pulses in excess of an ampere each. The measurement chain problem proved

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*Power ground, signal ground and chasses ground are kept separate at the instrument and tied together at a spacecraft common knot.

to be power converter noise conducted into the HV shield and was solved by moving these shields to a quieter ground point.

3.7.4 High Voltage - The high voltage areas in the power converter, all the safety resistors and the proportional counter filterboards, are conformally coated only, not potted. No high voltage connectors are used, all connections being solder joints on terminals. The instrument is not operable through the corona region although corona will not damage the converter output circuit.

Extreme cleanliness is necessary in the high voltage areas because of the safety resistors. Above 40 percent relative humidity and at laboratory temperatures surface contaminants, such as incompletely removed solder resin, can reduce counter voltages to a few hundred volts rendering them inoperable. Residues which reduce counter voltages even 20 volts are undesirable.

Achieving this level of cleanliness required care during all phases of assembly. In particular the HV areas had to be carefully cleaned prior to conformal coating to prevent entrapment of contaminants. Scrubbing with ethyl alcohol and a nylon brush proved adequate for this purpose.

In a sense, the MIT instrument is self-checking with regard to cleanliness. If the counter gains are normal in the laboratory environment, then the high voltage areas are adequately clean.

3.7.5 Instrument Interface Summary

Table 3-8 Summary of Interface Test Parameters* (Flight Unit)

Parameter	Measured Value	Required Value
Weight	26.85 kg (59.05 lb)	43 ± 5% lb. (MDR 28027)

*All measurements made at Ball Brothers Research Corporation.

Parameter	Measured Value	Required Value
Center of Gravity		
X	50.3 cm (19.8 in)	18.5 Min in
Z	15.2 cm (6.0 in)	5.5 ± 1.0 in
Y	-0.66 cm (-0.26 in)	0 ± 0.5 in
Measurement Dipole Moment ($Gauss-cm^3$)		
X	+50	-250 to +250
Y	-25	-250 to +250
Z	+400	-500 to +200 (MDR 28013)
Magnetometer Filed (Milligauss)	0.5	≤0.75 Max.
Adjacent Field (gauss)		
3" Above	<1	10 Max
2" Side	<1	10 Max
Electrical Power Consumption (Milliwatts) - Normal		
16V	3280	-------
19V	3268	3600 ± 10%
22V	3806	-------
Electrical Power Consumption (Milliwatts) - Calibrators On		
16V	4112	
19V	4275	
22V	4950	
Power Increase (19 to 22 V)	16%	25% Max
Turn-on Surge (Amps)	1.2	1.0 Max (MDR 28027)
Power Line Noise (Millivolts Peak-to-Peak)		
+19 V Line	20	35 Max
Power Ground	20	35 Max
Signal Ground	40	20 Max (MDR 28049)
Chassis Ground	30	200 Max

3.7.6 List of Materials

Table 3-9 List of Materials Used in the MIT Instrument

Material	Manufacturer or Vendor	Remarks
Coin Silver Tubing	Uniform Tubes Inc.	Collimator tubes
Aluminum 2024 -T3 Aluminum 2024 -T351 Aluminum 6061 -T6 Aluminum 2024 -T4	Industrial Aluminum Inc. " " "	Parts are alodined to the 1200 process for 180 seconds in accordance with MIT C-5541. Samples were supplied to BBRC and GSFC.
G10 Epoxy Board	AAA Plastics, and Forrest Products	Printed circuit board & insulating sheets to AAA Plastics
Stainless Steel		Calibrate actuator bearings
99% Tin Sheet	Cambridge Street Metal Co., Inc.	Counter Shields
Nylon Potting Shells	ITT Cannon	Connectors
Hot-Tinned Brass	H-H Smith	1412-8 Locking Terminal Lugs
Teflon	TA Mfg. Corp.	Cable clamps.These are the type of clamps used by BBRC.
Polyolefin	Raychem	Raychem RT876 Low Shrink temperature flexible tubing Type I.
Dacron	Gudebrod Bros. Silk	Style 18D69, Natural, Gudelace(lacing cord).
Polyalkene and Polyvinylidene	Raychem	Raychem Spec.44A Space Flight Wire

Material	Manufacturer or Vendor	Remarks
Nylon	Welkesser Co.	Flexible Nylon grommet strip WG-101
Teflon	Belden Electronic Wire & Cable	RG 196A/u(MIL C-17D) Coax wire
Tinned Copper Wire	Doric Electronic, Inc.	Birnback Bus Wire
Silicone Rubber	Boston Insulated Wire & Cable Co.	High voltage cable purchased and screened per MIT-OSO-H-10(HVW 20)
Polythermaleze	Belden Electronic Wire & Cable	H38 AWG, Beldon #8071
Phosphor Bronze, Grade B2;Gold Plated per MIL-G-45204 Type II Class 1	Advanced Packaging Inc.	#1907-040-1 & #1707-040-1&2 "Cirkut sockets" Meets MIT-OSO-H-10(P XYZ) parts specification.
Brass	Cambion	Cambion Terminals,#'s CP-1018-2-503,1460-2-05, 4871-1-0516,1597-2,all electro-solder plating
Stainless Steel (non-magnetic)	Accurate Fasteners	1. Helicoils per MIL Spec MS21209 2. NYLOCK Stainless Steel(non-magnetic) 3. LONGLOK stainless steel(non-magnetic) 4. Flat head stainless steel(non-magnetic) 5. Phillips head stainless steel(non-magnetic) 6. Dowels 7. Washers 8. Stop-nuts 9. #304 threaded rod
GE SS4004 Silicone Primer	Earl B. Beach	Connector potting

Material	Manufacturer or Vendor	Remarks
GE RTV-60	N.E. Chemical Allied Resin	Soft Potting Compound
Eccobond 55 w/Catalyst 9	Emerson & Cuming Inc.	General Fastening
Shell EPON 828	N.E. Chemicals	Hard potting compound
General Mills Versamid 125	Allied Resin	Catalyst for EPOM 828
Stycast 1090 w/Catalyst 9	Emerson & Cuming Inc.	Spot bonding
Solithane 113-300	Thiokol Chemical	Conformal coating
AM^{241} .62 microcurie	Isotope Products Labs	Calibration Sources
ARMCO Magnetic Ingot Iron	American Steel & Aluminum Co.	Cold drawn flat. Used in Solenoid Core.

3.7.7 List of Components

Table 3-10

List of Electronic Components used in the MIT Instrument

Function	Part #	Manufacturer	Remarks
IC Dual Buffer	U3199325lXC2	Fairchild	1.Part number specifies Fairchild unique processing to include test data. Options required, 168 hour burn in at 5.5 volts and 125° C. 2.Go-NoGo test at Room temperature per MIT-OSO-H-TS-15 3.Devices temperatured cycled per MIT-OSO-H-10 Part Specifications (I932, I9040, I9041, & I9042) 4.Devices baked in for 168 hours at 150° C. Ir measured before and after bake-in at MIT/LSE 5.Devices screened at GSFC's incoming inspection 6.Devices leak-tested at GSFC after we formed the leads
Flip-Flop	U3190405lXC2	Fairchild	
Nand Gate	U3190415lXC2	Fairchild	
Nand Gate	U3190425lXC2	Fairchild	

Function	Part #	Manufacturer	Remarks
IC Flip-Flop Nand Gate	FN9040 FN9042	Fairchild Fairchild	1.Devices 89 FN9040 and 65 FN9042 are SL units acquired from BBNC 2.Devices screened at GSFC. DC parameter measurements at high & low temperatures 3.Devices leak-tested at GSFC or Associated Testing 4.Go-NoGo test at room temperature per MIT-OSO-H-TS-15
IC Flip-Flop Nand Gate Nand Gate	SL10455 SL10456 SL10457	Fairchild Fairchild Fairchild	1.Parts number specifies Fairchild's SL program. 2.Go-Nogo test at room temperature per MIT-OSO-H-TS-15 3.Devices lead forming at MIT/LSE 4.Leak-tested per mil STD 883 at Associated Testing
IC Shift Register Dual 100 Bit	SM6305	NSC	1.Part number specifies a specially processed MM406 which includes a 100% testing of devices for a minimum operating frequency of 100 HZ at 40° C before and after a 250 hour non-operating conditioning at 125° C. Devices were X-rayed in two axes. 2.Devices were tested Co-NoGo at room temperature per MIT-OSO-H-TS-14 3.Operating burn in at 16 volts for 160 hours at room temperature per MIT-OSO-H-10 (I6305)
Shift Register Dual 100 Bit	SM8448	NSC	1.Part number specifies a specially processed MM406 to the following sections & classes of MIL. STD 883 method T5004. a)Section 3.1.1 Class B b)Section 3.1.2 Class B c)Section 3.1.4 Class B d)Section 3.1.6 Class B e)Section 3.1.7a Class B f)Section 3.1.7b-2 Class B g)Section 3.1.8 Class A (parameter measurements)

Function	Part #	Manufacturer	Remarks
			h)Section 3.1.9 Class B i)Section 3.1.10 Class A (parameter measurements) j)Section 3.1.12a-1 Class A (DC Parameter 25° C) k)Section 3.1.12a-2 Class A Max-Min temperature l)Section 3.1.12b Class A (AC Parameters) m)Section 3.1.13 Class A X-Ray 2.Devices tested Go-NoGo per MIT-OSO-H-TS-14 3.Operating burn-in at room temperature per MIT-OSO-H-10 (16300) 4.Operational vibration test of 30 devices at GSFC
Transistor (NPN) Switch	FM2369	Fairchild	1.Screened per MIT-OSO-H-10 part specifications (TB2369 & TB2894) at Associated Testing Lab, Inc. (250 devices) and GSFC (12 devices)
(PNP) Switch	FM2894		
Transistor NPN	2N2524 (NGAE105)	Solitron	1.Screened per MIT-OSO-H-10 part specifications (TB 2524 & TB 2605)
PNP	2N2605(PGAE115)	Solitron	2.Devices X-rayed at Solitron, NSC and Associated Testing Lab,Inc
PNP	JAN2605(NSC2106)	NSC	
Transistor Dual NPN	BD1450	Union Carbide	Specially processed 2N4880 screened per MIT-OSO-H-10 part specification (TB4880)
Transistor Complementary NPN/PNP	MD6001	Motorola	Screened to Motorola's specification # 8003H and MIT-OSO-H-10 part specification (TB6001)
Diode Silicon (General purpose)	DAR899	G.E.	Screened per General Electric's high reliability specification DAR899 and MIT-OSO-H-10 Part specification (D4153). Device screened at GSFC per GSFC testing specifications
Silicon (General purpose)	IN4153	G.E.	

Function	Part #	Manufacturer	Remarks
Resistor	1/8W BB±5%	Allen Bradley	1.Purchased to A-B technical bulletin 5050 dated Nov. 1966. One certificate of compliance out of five orders. 2.Screened per MIT-OSO-H-10 parts specification (RM-8-XYZ)
Resistor	1/4W CB±5%	Allen Bradley	Same screening as 1/8W resistor. No certificate of compliance.
Resistor	1/2W EB±5%	Allen Bradley	Same screening as 1/8W resistor. No certificate of compliance.
Resistor (Precision)	RN55E	Ward Leonard	1.Purchased and screened to MIT-OSO-H-10 (RP XYZ) 2.One certificate of compliance out of three orders
Resistor	MG710	Caddox	1.Metal Oxide resistor on order. Purchase requirements are certificate of compliance and standard gov't phrase on the order. 2.MIT-OSO-H-10 (RF-1-XYZ) Parts specification calls for a MH711. However Wilmore has submitted an MG 710 specification to GSFC.
Thermistor $10K_{\Omega}$ at 25^{O} C	GB41J1	Fenwal	1.Screened per MIT-OSO-H-10 part specification (TR-103) 2.Two certificates of compliance out of three orders.
Inductor	Series 1025	Delevan	1.Purchased and screened to MIT-OSO-H-10 part specification (L-XYZ)
Capacitor Tantulum	Minitan Y,P,B,A,G	Components, Inc.	1.Purchased and screened to MIT-OSO-H-10 Revision A parts specification (CT XYZ)
Capacitor Ceramic	C10 Series ± 10%	U.S.C.C.	1.Purchased and screened to MIT-OSO-H-10 Revision A part specification (CC XYZ) 2.Three out of five orders have certificates of compliance.

Function	Part #	Manufacturer	Remarks
Capacitor Tantalex (Solid-Electrolyte)	KGJ Series	Kemet	1.Purchased and screened to MIT-OSO-H-10 Revision A part specification (CS XYZ)
Capacitor Ceramic Disc (high voltage)	Jet Seal	Erie	1.Screened to MIT-OSO-H-10 Revision (CD XYZ)
Capacitor Ceramic Disc (high voltage)	Epoxy-Impregnated	Sprague	1.Screened to MIT-OSO-H-10 (CD XYZ) part specification 2.Have not submitted this part to GSFC. However Wilmore has it submitted.
Connector	"D" Series NMB-1-A10G	Cannon	1.Screened to MIT-OSO-H-10 part specification (J XYZ)

3.7.8 Quality Assurance Provisions - NASA Quality Publications NPC 200-2, -3, and -4 were invoked with regard to quality program, inspection system and hand soldering requirements respectively. The approved MIT OSO-H Quality Assurance Plan in the MIT OSO-H Quality Assurance Manual dated 3 June 1969 also applies.

3.7.9 Design Comments

1. HV Safety Resistors - It was interesting to learn that resistors as high as 5000 Megohm can be successfully used on fiberglass epoxy printed circuit card. This is clearly an upper limit in critical applications, however, and for future cirtical high voltage applications, resistors no larger than 100 Megohms are recommended (see also Section 3.6.3.2).

2. Proportional Counter Mechanical Interface - It was necessary to replace a proportional counter a total of seven times in the two instruments. In each case extensive

rework of solder joints was necessary at all wire attachment points. In all cases it was difficult to rework, inspect and recoat the joints involved. A connector for low voltages and signals is advisable at this interface point in future applications.

3. Electronic Packaging - The following problems were encountered with the packaging of the electronics stack.

a. Bent peripheral pins - The internal cable harness makes a hinge at the wide end of the motherboards. In spite of care taken to ensure that there was enough slack to allow vertical separation of all peripheral pins, many of those on the wide end of the board became bent during repeated separations and matings.

b. Inaccessible test points - Most connections in the stack were not available for probing while it was under test. This made the debugging phase of the test program unnecessarily long and difficult.

c. Inaccessible components - In a number of areas in the stack it was simply not possible to replace a part without extensive disassembly. Parts near the bottom of "T" modules and parts that fell under cable runs are but two examples.

d. "T" module mounting - While the convenience of testing individual modules prior to assembly of the motherboards was advantageous, the mating of the modules and motherboards was tedious, difficult, and time consuming.

e. Cable harness design - Only about one-third of the motherboard interconnections were possible with peripheral pins. The remainder was handled by an unwieldy cable assembly. Mating of the cable harness with the stack proved to be a major factor in overall assembly time.

The experience on this program argues very strongly against the module and large motherboard concept. A flat layout (with rails if necessary) on boards

about one-third the size of the MIT motherboards that would plug into sockets on a cable frame or "grandmother" board would be definitely advantageous in assembly and testing of the system.

f. Measurement chain stack - Since the discriminators, etc., were adjusted by fixed resistors on the various motherboards, calibration was very difficult, time consuming and somewhat inaccurate due to the lack of accessibility of the adjustments. An accessible panel with locations for the fixed resistors or potentiometers would have been much more preferable.

g. Preamplifier-Amplifier motherboards - Boards for the four-color counters were reasonably satisfactory. The thin window motherboards presented packaging difficulty since the well on the proportional counter was made too shallow. A well mounting configuration similar to the four-color counters should have been used.

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4.0 INSTRUMENT CALIBRATION AND TEST

The MIT instrument requires electrical calibration to set amplifier gains and discriminator settings and x-ray calibration for collimator angular transmission measurements and the determination of the overall transfer function of each measurement chain. Electrical calibration is done prior to installation of the counters in the instrument. X-ray calibration is done with the instrument in flight configuration.

The MIT OSO-7 Ground Support Equipment (Section 4.1) simulates spacecraft signals and has rudimentary data reduction capability. As a trouble shooting aid it provides extensive, continuous data on the operation of critical logic subsystems. The GSE is used throughout instrument calibration and the qualification and acceptance test sequence.

4.1 Ground Support Equipment

The MIT Ground Support Equipment is a system of some 500 transistors and integrated circuits for spacecraft signal simulation and data reduction. It can fully exercise the experiment without the spacecraft, spacecraft simulator or any external data reduction facilities if necessary. When the MIT instrument is integrated with the spacecraft (or simulator), normal spacecraft readouts must be used to verify operation of the experiment although a detailed look at experiment logic operation can be obtained with the GSE any time the rim panel test connector is accessible.

The ground support equipment, exclusive of the test signal buffer and Varian 50 channel digital recorder but including power supplies and power control circuits, is housed in two 14" high travel cases accepting standard rack panels (Figure 4-1).

A block diagram of the OSO-7 GSE is shown in Figure 4-2. The spacecraft simulator provides all signals required by the experiment but does not simulate the analog subcommutator loads. The experiment buffer box accepts the designated instrument test signals, buffs them, and drives the Varian 50 channel digital recorder and the GSE panel lamps.

4.1.1 Spacecraft Simulator - The signals provided to the instrument by the spacecraft simulator are the 800 Hz clock, Main Frame Gate (MFG), Day/Night level, nine commands, and the Magnetometer, Sun and Aspect pulses. The 800 Hz clock simulator (Figure 4-3) consists of an astable multivibrator with appropriate buffering. The frequency and symmetry of the clock are adjustable by means of two potentiometers. The Main Frame Gate simulator (Figure 4-4) counts 800 Hz clock pulses in an eight-bit ripple counter. Serial states 13, 16, 21, and 35, each 10 ms long, are decoded in a diode matrix, appropriately buffed, and supplied to the instrument. Simulated GSE Block Start and Word zero pulses are also generated for use in the GSE self-check function. A front panel switch is provided so that the GSE will operate with its own Main Frame Gate and 800 Hz clock or buffered experiment MFG and clock derived from the spacecraft. Day or Night level is selected from the front panel (Figure 4-5). The command generators (Figure 4-6) are capable of sending all nine commands simultaneously or one or more at a time. When the command execute switch is released, an execute signal is generated and processed by an anti-contact bounce circuit and an astable multivibrator. Buffered, this signal provides power to the selected command lines. The Magnetometer, Sun, and Aspect generators (Figure 4-7) consist of an astable multivibrator, a five bit ripple counter, and a buffer. Pulse

FIGURE 4–1. M.I.T. OSO-7 GROUND SUPPORT EQUIPMENT. (IN PICTURE: PROJECT ENGINEER RICHARD S. TAYLOR).

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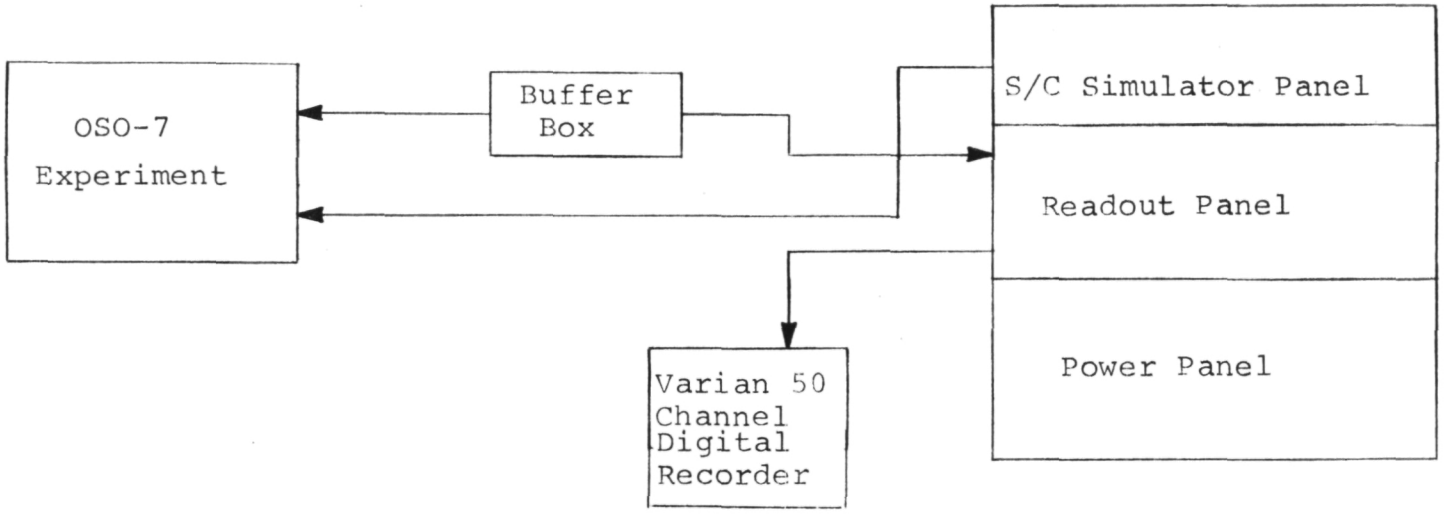

FIGURE 4-2 OSO-7 GSE BLOCK DIAGRAM

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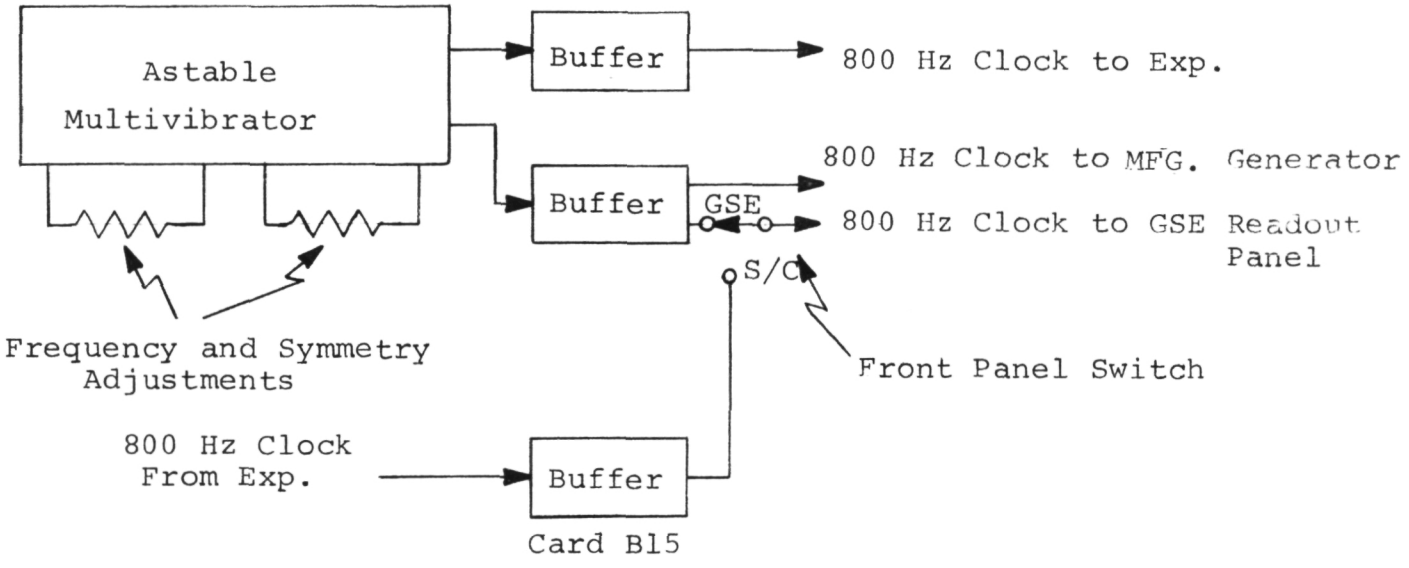

FIGURE 4-3 800 HZ CLOCK GENERATOR

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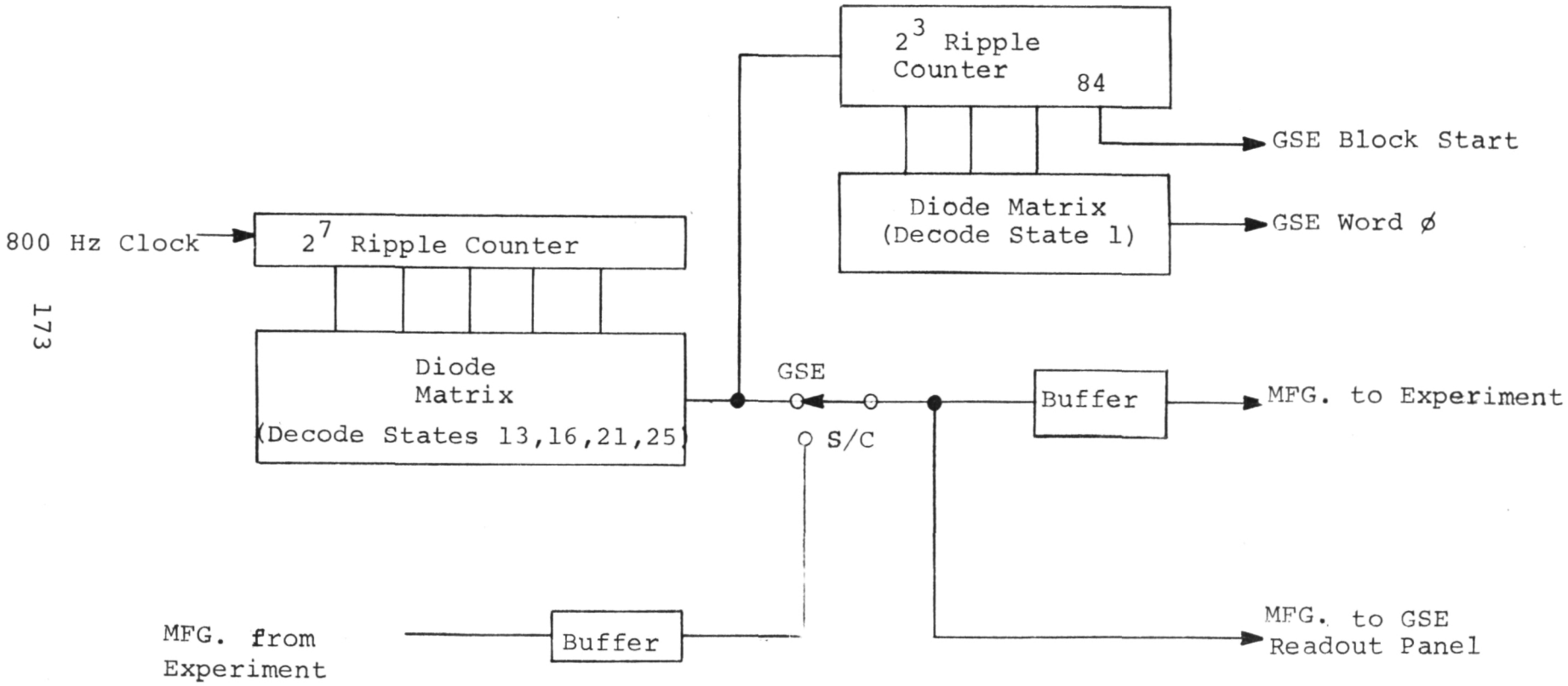

FIGURE 4-4 MAIN FRAME GATE GENERATOR

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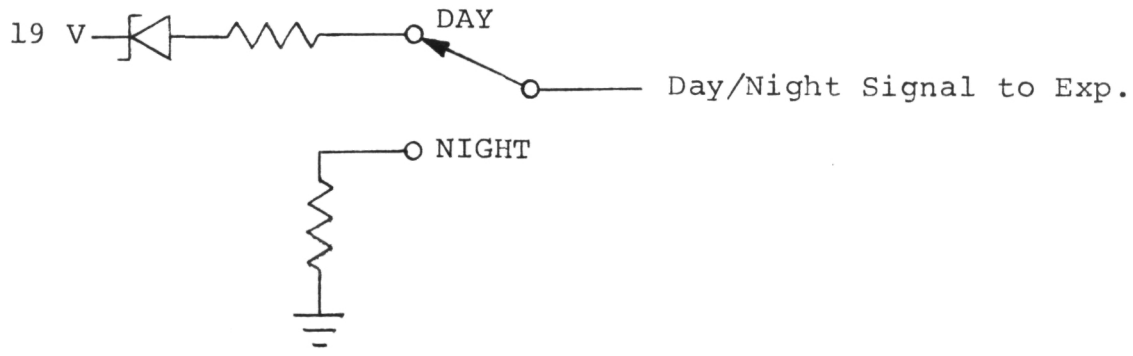

FIGURE 4-5 DAY/NIGHT LEVEL

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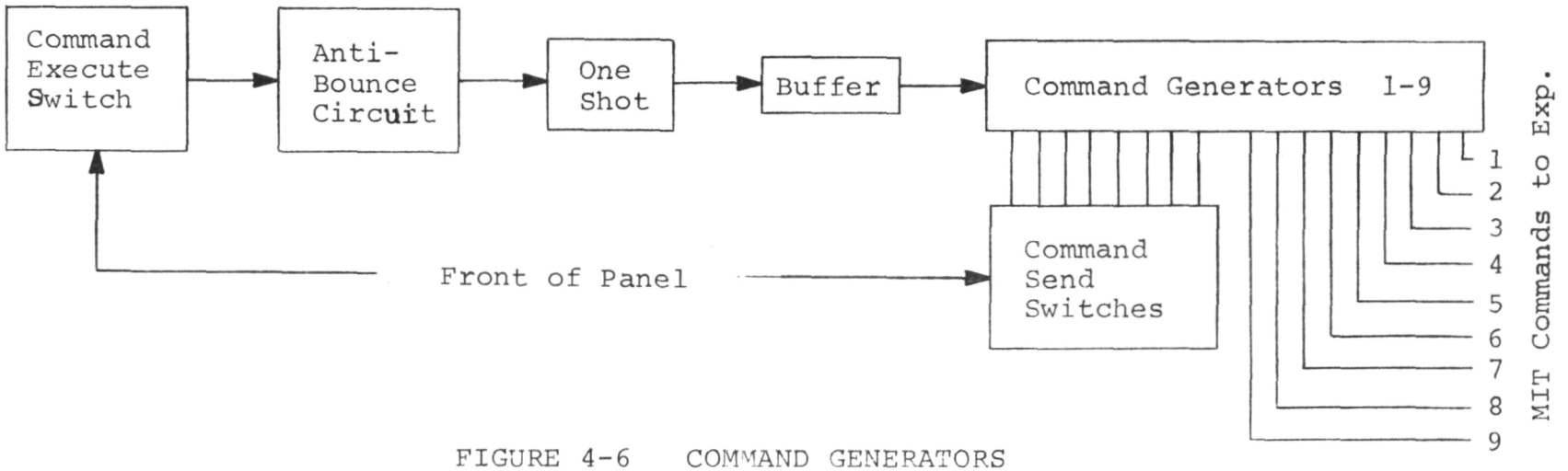

FIGURE 4-6 COMMAND GENERATORS

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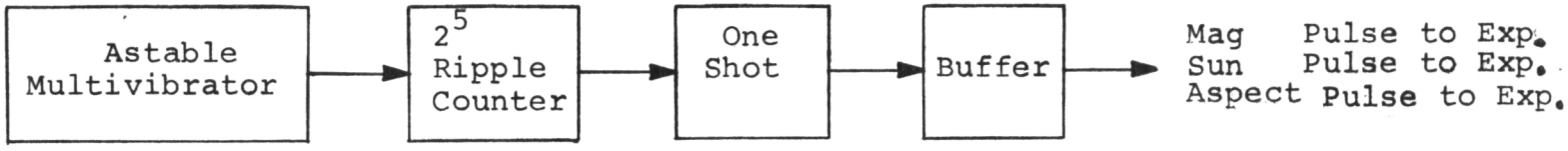

FIGURE 4-7 MAGNOMETER, SUN, AND ASPECT GENERATORS

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periods are independently and continuously adjustable from one to three seconds.

4.1.2 Readout System - Instrument x-ray data is processed by the readout system for real time display on GSE panel lamps and the 50-channel digital recorder. Digital test signals from the front panel connector on the instrument (P3) are wired to test points on the front panel of the GSE and displayed on the digital recorder as well. Analog outputs (Housekeeping data - Section 3.5) are wired through from the instrument to test points on the GSE front panel. Measurement chain test signals (measurement chain analog and digital x-ray data) are available at the top of the instrument at P7, only.

4.1.2.1 Format Data

4.1.2.1(a) Digital

Buffer Box: The experiment buffer box provides buffering of the signals originating at the experiment test connector (P3). Although each buffer is tailored to its signal, most buffers have inputs similar to a low power DTL gate and outputs similar to that of a standard DTL gate. Extremely short signals (the Data Transfer Pulse Revolution Pulse, and the memory output signals) are stretched by astable multivibrators. Such stretching is necessary for the digital recorder to respond to the data and for the display lamps to light. In each case the unstretched pulse is available for observation at a test point on the buffer box.

Readout System: Digital data readout is done on the digital recorder and the GSE panel lamps. Stretched memory data pulses are displayed directly as eight-bit binary words along with a data transfer signal.

This data does not come through the instrument Format Logic and provides direct access to memory output data for comparison with instrument output data (Figure 4-8).

Format output data is desplayed as a BCD word in lights (left of readout panel) and in a variety of ways on the digital recorder according GSE readout mode. Recorder signals in each mode are listed in 4.1.2.2.

In the normal and BCD modes of operation buffed serial data from the experiment is shifted into an eight-bit shift register during a Main Frame Gate (Figure 4-9). At the end of the Main Frame Gate, high speed counts are clocked into an eight-bit binary counter. When the state of the binary counter reaches the same state as the shift register, the high speed counts are gated off by the comparator. High speed counts are routed to the decade counters as well as the binary counter to obtain both an eight-bit binary and BCD readout simultaneously. As soon as the comparator locates data, the decade counter content is latched through to the readout panel lamps. In the BCD mode the decade counter content is also displayed on the recorder. Both displays are held until the next main frame gate leading edge occurs. This causes the decade counter contents to be displayed again but since this occurs during the reset signal, zeros are displayed.

In the Measurement Chain Test mode, high speed counts are routed through the MC test card rather than directly to the decade counters. In this mode, counts are accumulated in any selected format word over a full digital block. This corresponds to observation of the total counts in a particular proportional counter chamber over the full block. Housekeeping data is gated out during the Block Start Line to prevent its accumulation along with the data. To determine which word in the data line will be accumulated, a four-bit binary counter is used. The word zero pulse in the GSE is used to reset this

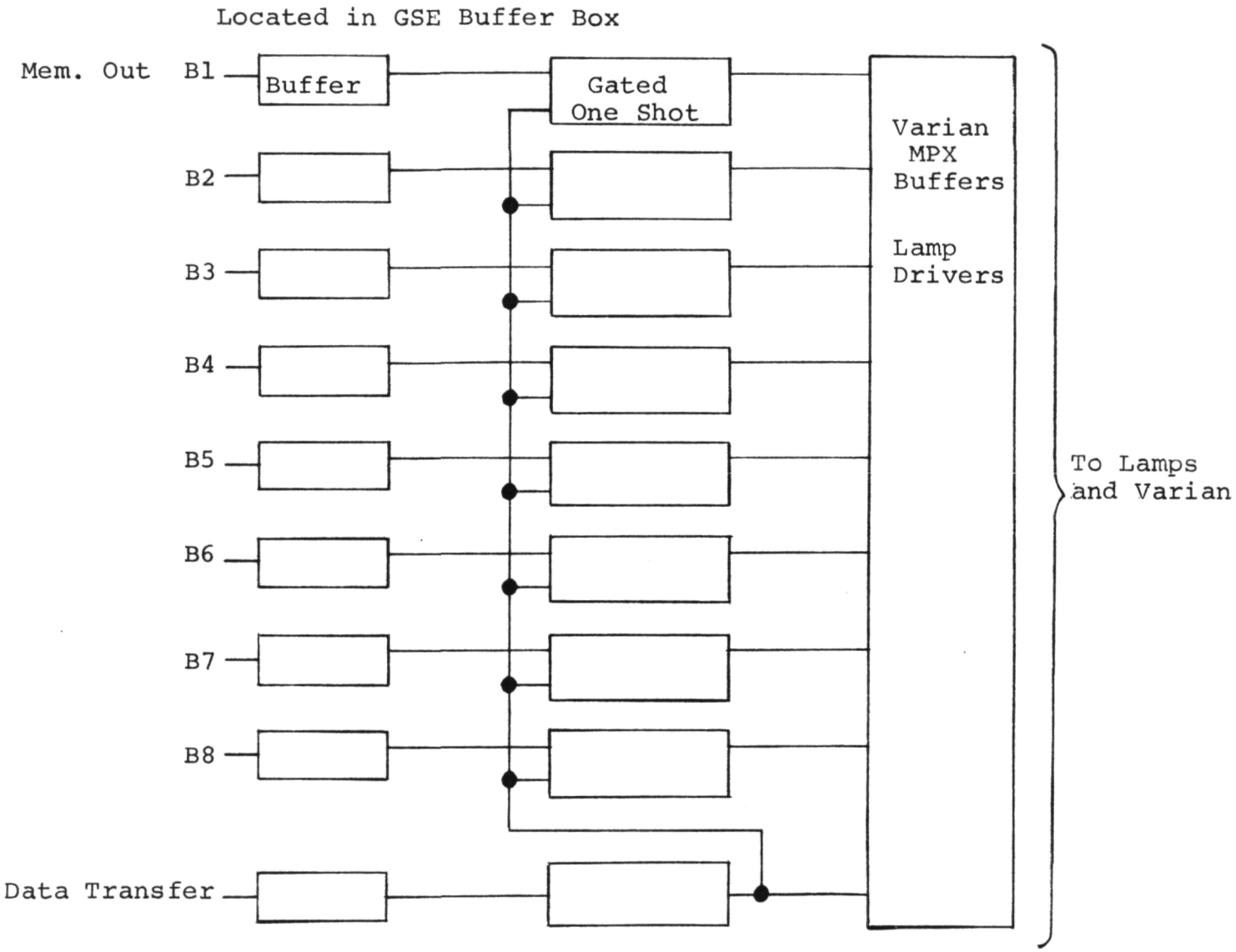

FIGURE 4-8 MEMORY DISPLAY SYSTEM

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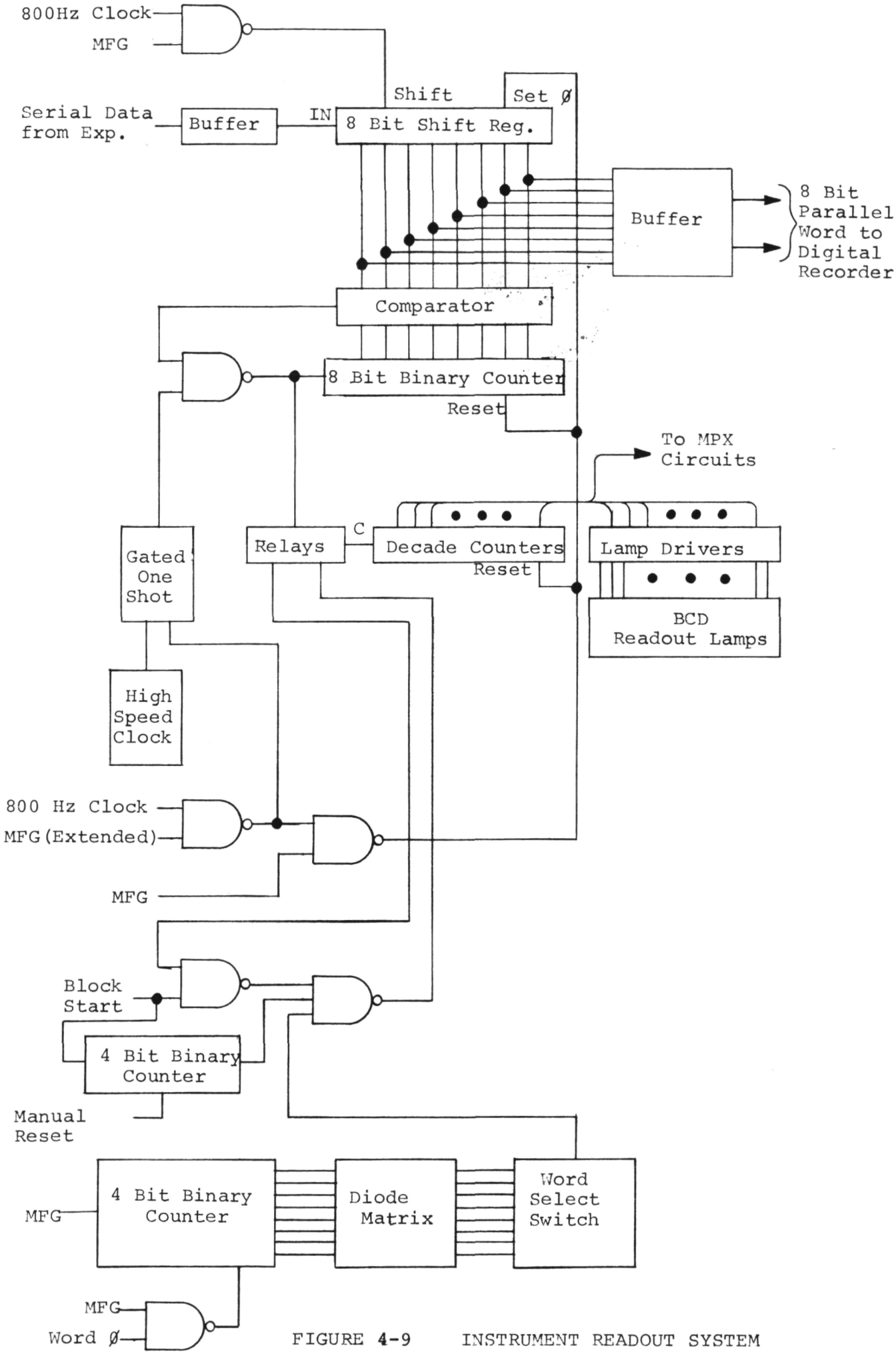

FIGURE 4-9 INSTRUMENT READOUT SYSTEM

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counter each data line. States 1 through 8 are decoded by a diode matrix,and any selected word is gated through to the decade counters by the associated word gate. Reset to the block start counter and the decade counters is manual. The display on the lamps and digital recorder persist until the system is reset by a panel switch.

4.1.2.1(b) Analog - Analog signals from the instrument are wired through to GSE front panel test points. A test meter is used at these jacks to measure analog output signals directly.

4.1.2.2 Engineering Data (and Data Recording)- Engineering data, primarily from the 50 pin test connector (P3) on the instrument is displayed on the recorder in Normal Mode (Figure 4-10). These signals are taken from locations in the instrument that are representative of the operation of complete subsystems. Problem isolation to particular subsystems of the instrument almost always begins with a careful study of this chart.

In BCD (Binary Coded Digital)Mode, the BCD panel lamp display is recorded on the chart in accordance with Figure 4-11. This mode is useful when an easy-to-read real time record of data from all words is desired.

In Measurement Chain (MC) Test Mode, Figure 4-12, the GSE accumulates counts from all bins in a digital block for a particular word and holds the total at the end of the block. The recorder displays this accumulation and records the accumulated total.

4.1.3 Power System - The power system consists of four power supplies with current limiting, overvoltage protection,and suitable metering. Experiment orbit power is obtained from a supply which is adjustable up to 23 v, at which point a voltage limiter cuts-in. A second supply with overvoltage protection supplies GSE plus 19 volts and a plus 10 volt source. The third supply provides minus 6 volts.

Plus 5 volts is developed in the GSE for internal use. The front panel supply adjustments are disabled.

4.1.4 Measurement Chain Simulator - Memory checkout requires a pulse source that can provide a specified number of pulses per timed bin interval. Given the number of pulses per bin and knowing the accumulation interval (one format length or 190 seconds) it is possible to predict the maximum number to which the memory will accumulate before readout occurs. The Measurement Chain Simulator generates these pulses.

The Measurement Chain Simulator (Figure 4-13) is capable of entering from zero to 15 counts every bin (or every other bin) in each of eight data channels (Measurement Chains 1,2,3, 4,5,6,7,and 9) entering the experiment data acquisition system. An astable multivibrator provides pulses which are gated by the bin open pulse from the experiment and the comparator.

4.1.5 Design Comments - The GSE was intended to be inexpensive and, therefore, of necessity, rather limited in capability. It did perform its intended funcitons well, however. The Measurement Chain Test Mode and Normal Mode data display were effective in instrument evaluation and trouble-shooting. Also useful was a mechanism for anticipating Block and Format Start Lines (which contain mostly housekeeping data) in the format and recording them automatically.

Other areas of the GSE could have been made more useful and efficient had sufficient time and capital been available. Here are some suggestions:

1. Automated Command Sequencing - The MIT Normal Mode Sequence contains 64 commands. Each of the 64 must be sent individually every time the instrument is turned on. With time, the more talented among us became adept at playing the command switches, piano-like, and it was possible to send the entire

1. Event Marker
2. Buff D/N Level
3. Buff Day Aspect
4. Buff Night Aspect
5. Buff Magnetometer
6. Buff 800 Hz Clock
7. Buff MFG
8. Vacant
9. SR out B1
10. SR out B2
11. SR out B3
12. SR out B4
13. SR out B5
14. SR out B6
15. SR out B7
16. SR out B8
17. Vacant
18. GSE MFG
19. GSE 800 Hz Clock
20. Serial Data Out
21. GSE Gated Shift Clock
22. Memory Out B1
23. Memory Out B2
24. Memory Out B3
25. Memory Out B4
26. Memory Out B5
27. Memory Out B6
28. Memory Out B7
29. Memory Out B8
30. Data XFR Command
31. Revolution Pulse
32. RS/SFF 3 $\overline{Q}$
33. IS/SFF Q
34. Bin Open Pulse
35. Iso. Last Bin Pulse
36. Iso. Auto Seq. Pulse
37. Iso. ROS/EFFQ
38. Iso. MIS/EFFQ
39. Bin Addr Setup
40. R/O Addr Setup
41. Format Start
42. Block Start
43. Word Ø
44. Buff Command 1
45. " " 2
46. " " 3
47. " " 4
48. " " 5
49. " " 6
50. " " 7

Figure 4-10. Digital Recorder Chart Assignment, Normal Mode

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1. Event Marker
2. Buff D/N Level
3. Buff Day Aspect
4. Buff Night Aspect
5. Buff Magnetometer
6. Buff 800 Hz Clock
7. Buff MFG
8. Vacant
9. SR out B1
10. SR out B2
11. SR out B3
12. SR out B4
13. SR out B5
14. SR out B6
15. SR out B7
16. SR out B8
17. Vacant
18. GSE MFG
19. GSE 800 Hz Clock
20. Serial Data Out
21. GSE Gated Shift Clock
22. Memory Out B1
23. Memory Out B2
24. Memory Out B3
25. Memory Out B4
26. Memory Out B5
27. Memory Out B6
28. Memory Out B7
29. Memory Out B8
30. Data XFR Command
31. Vacant
32. Vacant
33. Vacant
34. Vacant
35. Vacant
36. Vacant
37. DC 10^2 B4
38. DC 10^2 B3
39. DC 10^2 B2
40. DC 10^2 B1
41. Vacant
42. DC 10^1 B4
43. DC 10^1 B3
44. DC 10^1 B2
45. DC 10^1 B1
46. Vacant
47. DC 10^0 B4
48. DC 10^0 B3
49. DC 10^0 B2
50. DC 10^0 B1

Figure 4-11. Digital Recorder Chart Assignment, BCD Mode

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1. Event Marker
2. Buff D/N Level
3. Buff Day Aspect
4. Buff Night Aspect
5. Buff Magnetometer
6. Buff 800 Hz Clock
7. Buff MFG
8. Vacant
9. SR out B1
10. SR out B2
11. SR out B3
12. SR out B4
13. SR out B5
14. SR out B6
15. SR out B7
16. SR out B8
17. Vacant
18. GSE MFG
19. GSE 800 Hz Clock
20. Serial Data Out
21. GSE Gated Shift Clock
22. Vacant
23. Vacant
24. Vacant
25. Antico Events
26. Vacant
27. DC 10^4 B4
28. B3
29. B2
30. B1
31. Vacant
32. DC 10^3 B4
33. B3
34. B2
35. B1
36. Vacant
37. DC 10^2 B4
38. B3
39. B2
40. B1
41. Vacant
42. DC 10^1 B4
43. B3
44. B2
45. B1
46. Vacant
47. DC 10^0 B4
48. B3
49. B2
50. B1

Figure 4-12. Digital Recorder Chart Assignment, MC Test Mode

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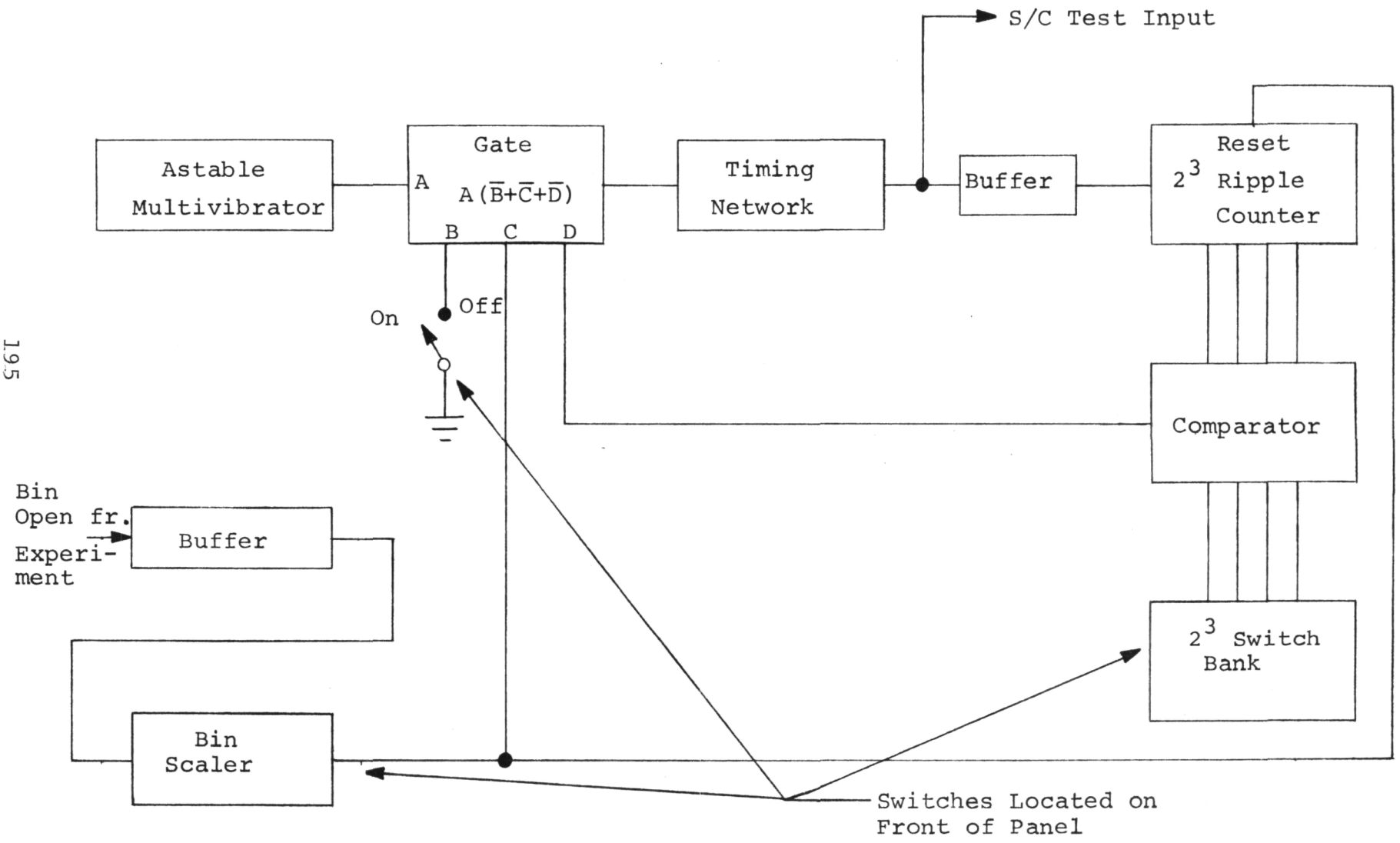

FIGURE 4-13 MEASUREMENT CHAIN SIMULATOR

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sequence in under a minute. An automated system would have reduced this time further, however, and eliminated the possibility of dropping commands.

2. Automated Test Procedures - At best, the completion of the Comprehensive Test Procedure, which checks the entire instrument, takes three hours. It is tedious work. A computer-controlled procedure could have eliminated the tedium, reduced or eliminated operator errors (providing more consistent results), and provided more sophisticated data processing.

4.2 Test Procedures

Formal procedures were developed for subsystem and instrument test to insure consistency and completeness in the test phases. Qualification and acceptance tests, on the prototype and flight instruments respectively, were performed in accordance with the Preliminary Environmental Test Specification for OSO-H Experiments (GSFC:S-326-OSO-2, January 1970) and the approved MIT OSO-H X-Ray Experiment Test Plan (Nov. 2, 1970). A summary of the tests and test results for the two instruments will be found in Section 4.4. The procedures summarized below will be found in full in the MIT test plan.

4.2.1 Electronics Stack - Used throughout temperature testing of the electronics stack, this procedure fully exercises all stack functions. Measurement Chain inputs are simulated with a pulse generator, all other inputs are from the GSE (Section 4.1). Much of this procedure is duplicated in the Comprehensive Test Procedure (Section 4.2.5); however, the Electronics Stack procedure must be used when detailed information on measurement chain operation is required. Information on such as low edge discriminator firing levels

is not available directly through the comprehensive procedure. The stack is tested over a temperature range of -20°C to +40°C using this procedure, before installation in the instrument.

4.2.2 Power Converter Comprehensive - The power converter (Section 3.6) is manufactured to MIT specifications by Wilmore Electronics, Durham, North Carolina. This procedure verifies that operation is to specification under a variety of load and bus voltage conditions. Before each converter is accepted by MIT, operation is checked with this test procedure at temperature extremes of -20°C and +45°C.

4.2.3 Proportional Counter Acceptance Tests - The proportional counters are manufactured by LND, Inc., Oceanside, N.Y. Prior to acceptance by MIT, each counter is tested to this procedure.

Test features include vacuum cycling and storage at -20°C and +50°C. Proportional counter gain is checked after each test phase at ambient temperature and pressure. Additional tests include gain measurements at -10°C and +35°C.

4.2.4 Quick-Look - The Quick-Look Procedure is a full instrument test that may be performed in less than one-half hour. It checks the operation of about 80% of the instrument subsystems primarily through engineering data readouts (analog and digital), input current measurements, and short term data rates.

4.2.5 Comprehensive - The Comprehensive Test Procedure tests all instrument subsystems. It requires three hours to perform. All measurement chain functions are checked and sufficient x-ray data accumulated to provide at least

five percent statistics. A series of these procedures, performed over an interval of weeks or months provides the definitive operating history of the experiment. The procedure was used exclusively in qualification and acceptance testing of the flight and protctype instruments.

4.3 Instrument Calibration

4.3.1 Electrical Calibration - Electrical calibration is necessary in the measurement chains and analog sub-subcommutator system.

4.3.1.1 Analog Sub-Subcommutator System -

4.3.1.1(a) Temperature Sensors - In the thermal vacuum test chamber at GSFC, vacuum chamber thermocouples (which are calibrated to 0.01°C) were located as close as possible to each MIT thermistor. Analog voltage outputs for each instuument thermistor were taken at each temperature and the thermocouple temperatures recorded. This experimental data was compared with an analytical estimate of the calibration and a best fit curve determined for each thermistor.

4.3.1.1(b) Voltage Sensors - An analysis of the analog sub-subcommutator gates indicated that the voltage sensor outputs were insensitive to temperature variation (see also Section 3.5.3) within the expected operating range. Calibration of the analog outputs was performed at ambient temperature and normal supply voltages and extrapolation made to other conditions.

4.3.1.2 Measurement Chains - Amplifier gain and low edge discriminator switching points had to be set in each chain. In addition, Chains 3,4,7 and 8 required setting of the risetime antico trigger point. This calibration is performed with the equipment shown in Figure 4-14. The Northern NS-600 Multichannel Analyzer is the heart of this setup. Precalibration of analyzer channel number in measurement chain output volts and keV (from suitable x-ray sources) allows precise determination of high and low edge discriminator settings and amplifier gain. For each calibration run, all components of the chain under test were assembled as they would be used in the system. Each counter is mated with its associated measurement chain amplifier, discriminator circuits and power converter HV output tap (Figure 4-15). Run in this arrangement, x-ray sources of known characteristics are used to stimulate the counter and gain and discriminator settings changed as necessary to meet system requirements.

Representative calibration data is shown in Figure 4-16. This data is the final setting of the measurement chains on the test bench (14 Dec. 1970). In each case the high level discriminator was set to correspond to a measurement chain output voltage of about 4.9 v and the low level discriminator to about 0.40 volts to use the linear range of the amplifier to the fullest extent possible. Linearity over this range is within one channel in all chains except Krypton (Chain 3 and 7), and low edge values are not shown for the Krypton counters for that reason.

The high voltage safety resistors (Section 3.7.3) were added after calibration was complete and a 5 to 10 volt reduction in all counter high voltages occurred. Filterboard leakage current variations with temperature cause additional high-voltage shifts and introduce some uncertainty into the tabular values. Reference to spectral data taken during

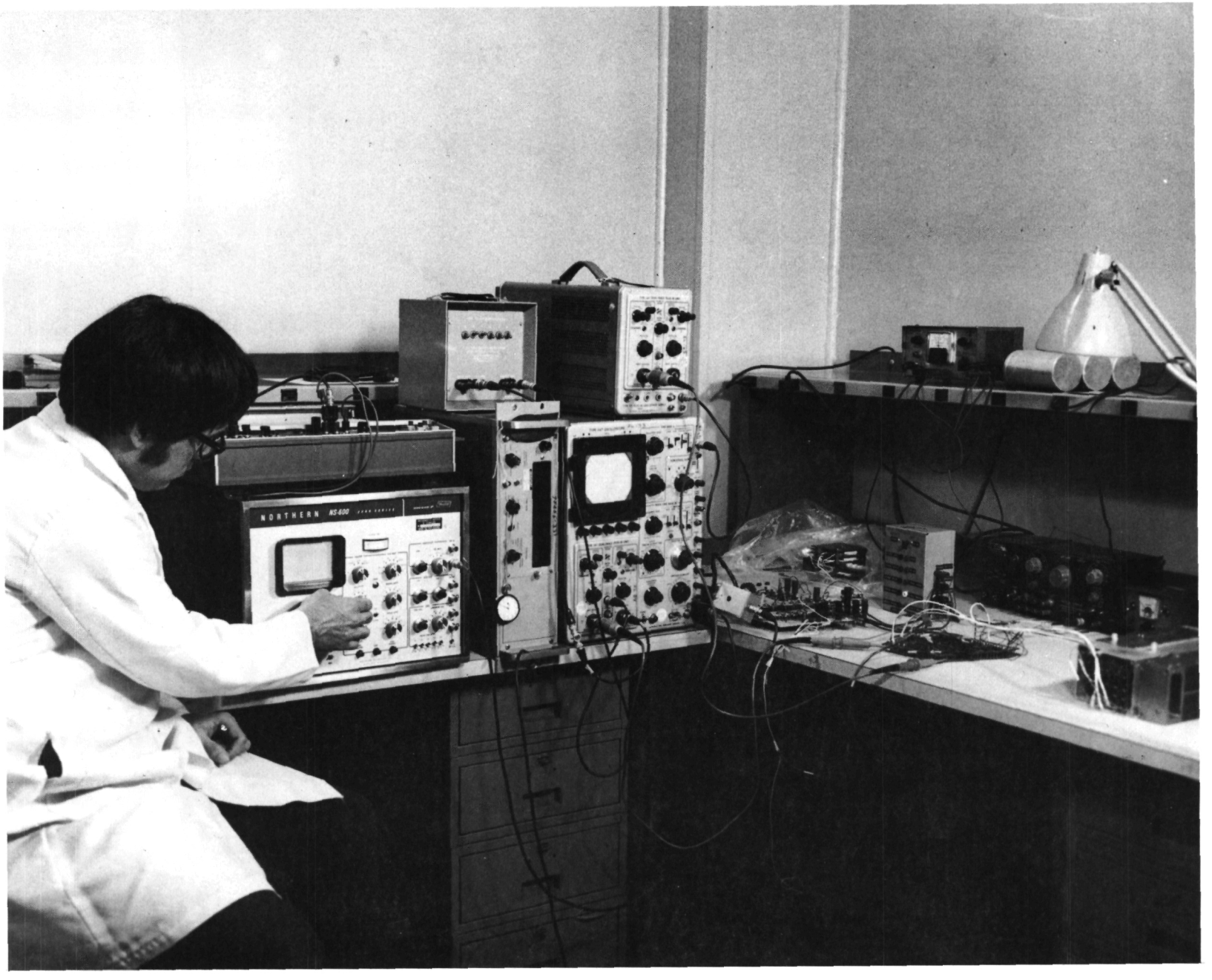

FIGURE 4-14. MEASUREMENT CHAIN CALIBRATION BENCH (IN PICTURE: PROJECT SCIENTIST DR. GEORGE SPROTT).

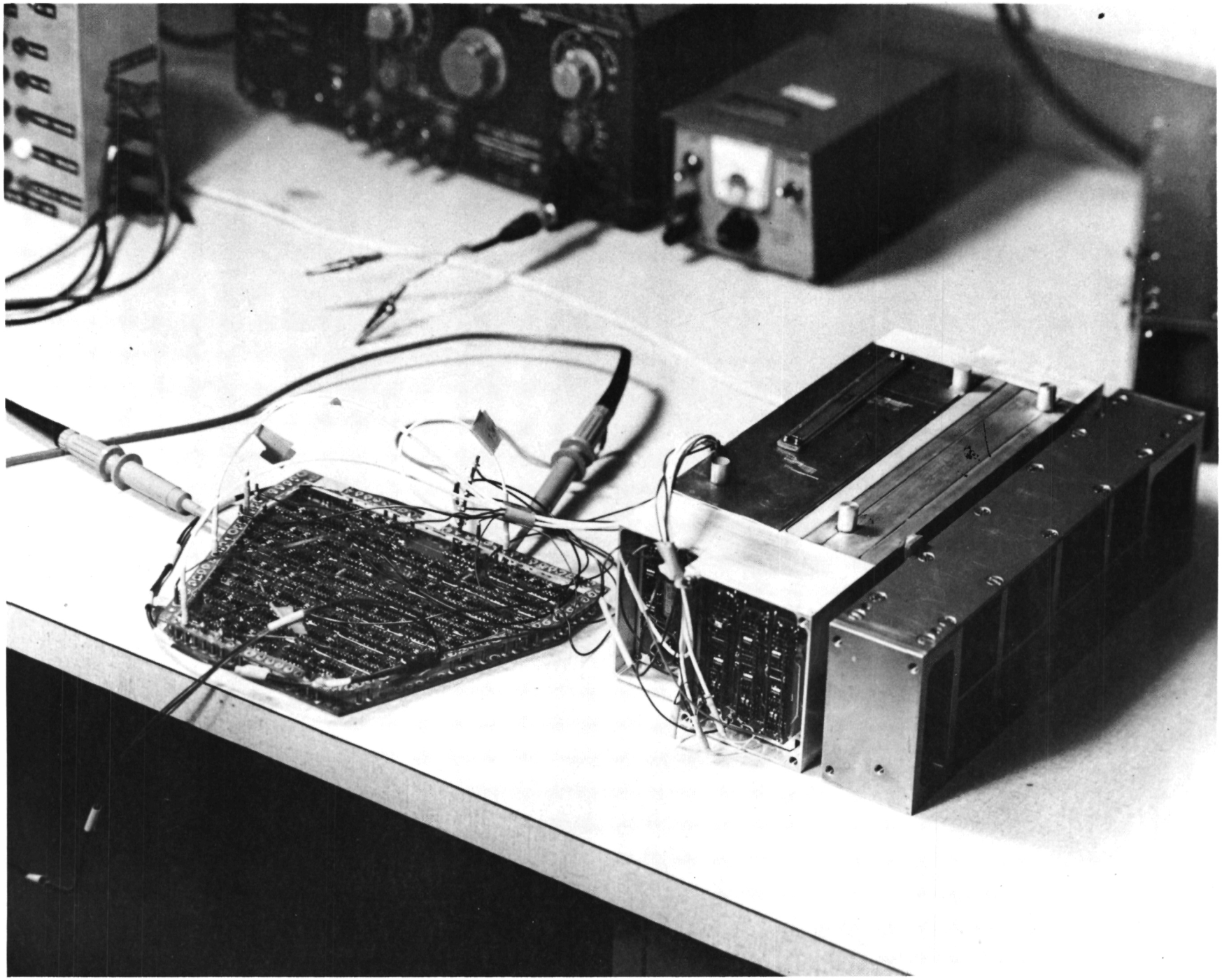

FIGURE 4-15. MEASUREMENT CHAIN SETUP FOR CALIBRATION.

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Chain	Counter S/N	LLD Energy/Channel	HLD Energy/Channel	Gain Setting Energy/Channel
1	6828	0.8 kev/9	8 kev/90	5.9 kev/66
2	6828	1.5 kev/19	8.5 kev/109	5.9 kev/75.5
3	6828		48 kev/82.5	48 kev/82.5
4	6828	6 kev/8.5	60 kev/85	60 kev/channel 85
5	6826	0.8 kev/9.5	8 kev/97.	5.9 kev/71.0
6	6826	1.5 kev/19	8.5 kev/106	5.9 kev/74.
7	6826		48 kev/78	48 kev/78
8	6826	6 kev/9	60 kev/91	60 kev/91
9	7629	0.5 kev/7	3.3 kev/45	3.0 kev/41 3.5 kev/45
10	7631	0.5 kev/7	3.3 kev/44.	3.0 kev/41 3.5 kev/47.5

Figure 4-16 Final Bench Calibration Data (12-14-70). No HV safety resistors installed.

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thermal-vacuum testing at GSFC is necessary to determine each counter operating point with precision.

4.3.2 X-Ray Calibration - There are two aspects of this calibration phase: Collimator angular response determination and measurement of the x-ray spectral response of the counters. Both types of measurement were done with the instrument on the test stand in Figure 4-17. This stand allows rotary motion in two axes and angular measurement to better than one arc minute. The x-ray beam used was supplied by a Dicker Model 816D Constant Potential Diffraction Generator. For most of the work, the beam from the x-ray tube was Bragg-reflected from a lithium fluoride crystal to produce a highly monochromatic beam. The instrument was located 18 meters (60 feet) from the x-ray generator so that the x-ray beam impinging on the experiment would be almost parallel.

4.3.2.1 Angular Response - The number of x-rays passing through the collimator is a function of the angle between the collimator axis and the direction of the incident radiation. The angular response function of the collimators was determined by rotating the instrument in the x-ray beam through varying azimuth and elevator angles and recording the counts received by the instrument's proportional counters. Before each measurement sequence the collimator axis (defined as the normal mirror on each collimator face) was made parallel to the x-ray beam using laser auto collimation techniques. The alignment was rechecked after the measurements were completed. Thus each collimator's x-ray response was measured relative to its own mirror. The relative orientation of the four collimator mirrors and the baseplate mirror was determined by an independent sequence of laser auto collimation measurements. Subsequently,

Ball Brothers personnel measured the angular displacement of the MIT baseplate mirror and the other MIT mirrors to the star sensor reference mirror.

4.3.2.2 X-Ray Spectral Response - The response of each counter to a monochromatic x-ray beam was determined at a number of energies through the 1-60 keV energy range. At each energy the spatial homogeneity of the beam was checked and its intensity and energy distribution measured with a special calibration proportional counter. Then, with the OSO instrument in the beam, the pulse height spectra of the measurement chain output pulses were measured and the total counts from each chain were recorded for the different states of pulse discrimination in which the instrument can be.

The results of all these measurements were duplicated and have been placed in two independent sets of calibration notebooks to guard against loss.

4.4 Test History

In addition to a tabular history of tests, problems and solutions on both the Prototype and Flight Units, a review of those Failure Analysis Reports applicable to the instruments is included as is a summary of the Flight Unit status at launch. Supplementary information pertaining to the more critical of the problems outlined below will be found in those sections of this report dealing with the part of the flight unit involved and in Section 4.4.5. Certain areas of these summaries relate to specific components of the instrument and are not necessarily covered in the technical description. The detailed information is included here for reference.

4.4.1 Prototype/Flight Spare Unit -

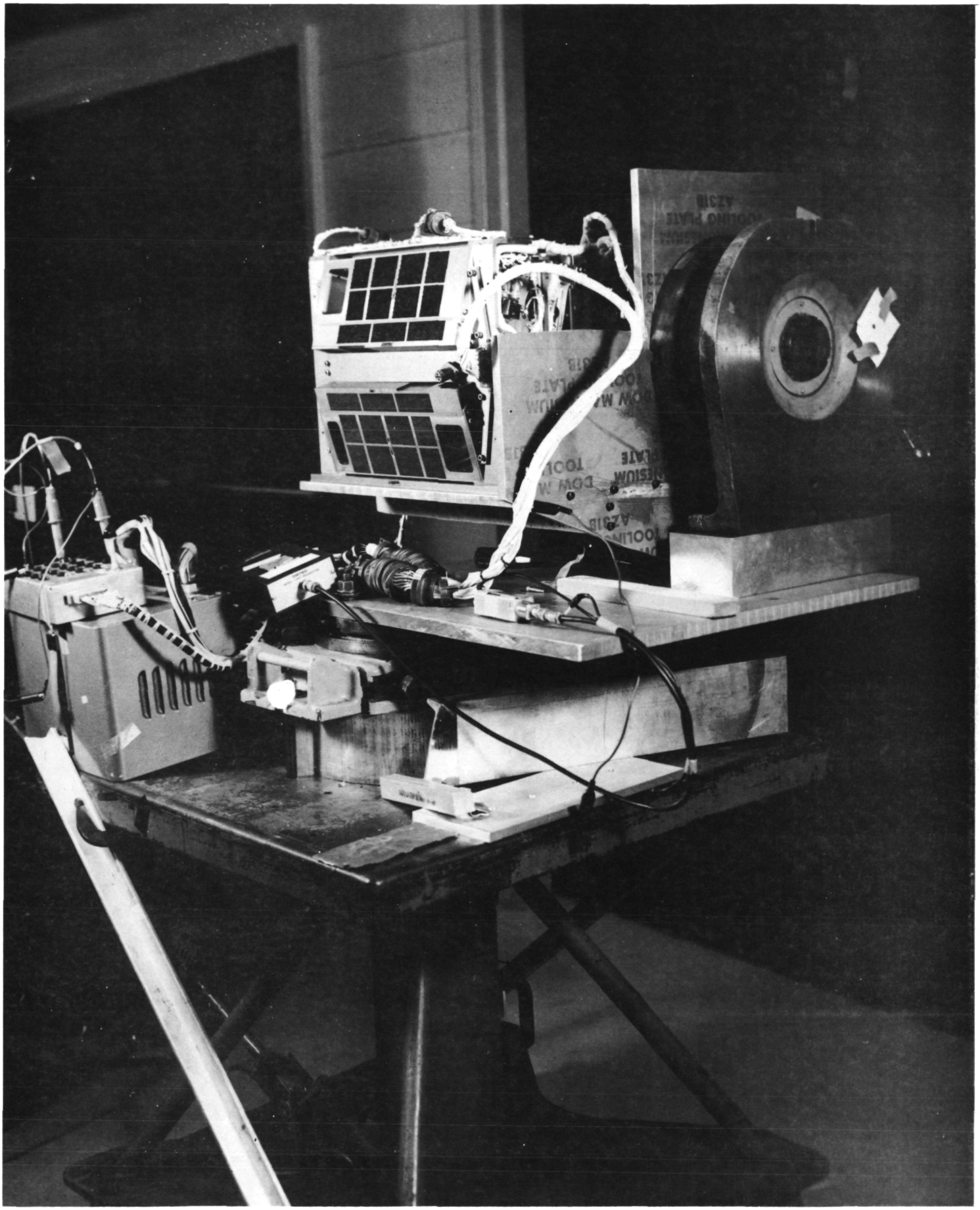

FIGURE 4-17. TWO AXIS TEST STAND.

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Table 4-1 Summary of Prototype/Flight Spare Tests and Problems

1.	9/30/70	Interface Tests BBRC	1. Wt. out of spec. Spec later revised (333). 2. Turn on surge out of spec (333). Device failure in surge limiter. 3. Electrical noise out of spec on launch power, power ground and signal ground lines (333). Added additional filtering to converter and clock line driver motherboard. 4. Instrument memory fills randomly. Traced to S/C simulator aspect pulse jitter (329). 5. Sun pulse flag missing from Format (327). Found a resistive solder joint on MB-A1 (342).
2.	11/29/70	MR B 04981	Circuit socket problems due to conformal coating. Solder joints at offending locations reworked.
3.	12/2/70	MR B 04983	Converter HV control line does not disable converter HV. Replaced Solitron 2N2524, Q37 in converter.
4.	12/8/70	MR B 04984	Measurement chains 1,2,3,4,9 do not drive rate counter. Replaced 2N4880. See also MR B 04994.
5.	12/13/70		Instrument Preshake status (388). 1. Chain 1 - apparently bad anode. 2. Chain 2 - apparently bad amplifier transistor.* 3. Chain 7 - apparently bad amplifier.**
6.	12/14/70	z-z sine and random (qualification level) AVCO, Wilmington	1. No counts chain no.2 (398). 2. Chain 1 counting (393). 3. Chain 5 no counts (393). 4. Chain 7 no counts
7.	12/14/70	MR B 04988	Argon chamber 6825 intermittent shorted anode (see also MR B 04986).
8.	12/14/70	MR B 04986	Neon chamber inoperative prior to shake OK post z-z sine and random. Intermittent anode short. See also MR B 04988.

* Found Q3, Chain 2 amplifier dead (387).

**Found signal input shorted to ground (405).

9.	12/14/70	MR B 04987	Measurement chain 5 not counting post z-z axis shake. Counter window punctured.
10.	12/15/70	x-x sine (Qual level) Wilmington	1. Submemory 5 not clearing (395).
11.	12/16/70	x-x random (Qual level) Wilmington	1. Upper actuator flex pivot broken (394). 2. Chain 8, no counts (419). 3. Two wires in interior cable bundle abraded (419).
12.	12/16/70	y-y sine and random (Qual level) Wilmington	1. Chain 8 not counting.
13.	12/16/70	MR B 04993	Upper calibrate actuator flex pivot broken post x-x sine and random. Actuators redesigned to eliminate flex pivots.
14.	12/16/70	MR B 04992	Lead shield broke loose from upper actuator area during x-x sine shake. Lead piece redesigned to be clamped as well as epoxied in place.*
15.	12/16/70	MR B 04991	Measurement chain 8 not counting after y-y axis sine and random. Measurement problem, chain OK.
16.	12/16/70	MR B 04989	Submemory 5 always reads out high. Found and repaired resistive solder joint.
17.	12/31/70	MR B 00851	Wire abrasion of cable bundle during shake. Rounded metal edges in vicinity of cable.
18.	1/4/71	MR B 04996	Analog line 2, word 2 output low. Replaced FM(Fairchild)2894(see also FATR 1818).
19.	1/22/71	x-x sine (Proto level flite sweep) Wilmington	Instrument fixes OK.
20.	1/22/71	MR B 00858	Front window buckled, counter 6824F. Cause improper installation. Counter cupport wedges modified to prevent recurrence.

*Best guess as to window failure in Chain 5 during z-z shake: lead shutter piece partially lifted during z-z motion and edge impinged on window.

21.	1/26/71	MR B 00860	Instrument not responding to clear command. Found bad solder joint at connector P9. Transferred clear command to another pin.
22.	1/26/71	MR B 00861	Instrument input current about 50 ma high. Replaced gate and FF in Format logic. Failure due to transient on signal ground.
23.	1/26/71	MR B 00859	Calibrators do not pull in. Transformer failure in 8v section of power converter. Replaced transformer.
24.	2/12/71	Acoustic Test(Qual level) GSFC Chamber 241	Instrument OK post test.
25.	2/16/71 10:00p.m.	Start Thermal Vacuum GSFC	EQ3 not rising to full level before pump down (2-68). Gate replaced 4/7/71 (2-120).
26.	2/18/71	Thermal Vacuum	1. Noise in chains 1,2,4,7,10 at turn on. 2. Long pulses chain 1. 3. Memory intermittently goes into high speed cycling. 4. No HLD most chains. 5. No LLD chains 9,10.
27.	2/18/71	MR C 00906	Instrument current jumps 50 ma intermittently. Tied floating gate input in memory to +5 volts (proto and flite).
28.	2/18/71	MR C 00955	Intermittent noise, chains 1,2,4,7,10. Cleaned all HV areas.
29.	2/18/71	MR C 00954	Measurement chain no.1, counting rate low. Cleaned all associated HV areas thoroughly.
30.	2/18/71	MR C 00955	No HLD, Chains 1,2,3,5,6,7,9,10. A measurement problem, not a malfunction.
31.	2/19/71 8:00a.m.	Thermal Vacuum Start cold cycle(-10°C)	1. Manual calibrate inoperative. 2. Chain 7, few digital counts. 3. Chain 4, no digital counts. Chain 3, erratic digital rates.

32.	2/19/71 9:00a.m.	Break Vacuum	
33.	2/19/71	MR B 00834	+8v out of regulation at 0°C. Increased 8 volt control drive from logic (proto and flite).
34.	2/19/71	MR B 00837	Chain 4 counting rate low. All associated HV areas cleaned thoroughly.
35.	2/19/71	MR B 00836	Measurement chain 3 rate abnormal. Not a malfunction, chain not calibrated.
36.	2/19/71	MR B 00835	Measurement chain 3 rate low. Not a malfunction, chain not calibrated.
37.	3/4/71 5:00p.m.	Start thermal vacuum cold cycle (+35°C) GSFC Chamber 241	Instrument on - OK.
38.	3/6/71	Thermal Vacuum cold cycle(-10°C)	Observed rate glitch, chain 3.
39.	3/7/71 10:00a.m.	Thermal Vacuum Hot soak(+35°C)	Gain low, all chains.
40.	3/8/71	MR B 00842	Gain in all measurement chains low at +35°C. Replaced two TX1N4948 in HV converter multiplier string.
41.	3/11/71	Break Vacuum	
42.	3/13/71	Special Thermal Test Cycle (+35°C) GSFC Chamber 241	HV problem investigation
43.	3/14/71	Break Vacuum	Return instrument to MIT.
44.	3/18/71	Acceleration Tests - AVCO Wilmington	Instrument OK, post acceleration.
45.	3/20/71	1. Shipped HV converter to Wilmore for refurb and repair. 2. Began proto refurb work.	

46.	6/3/71	MR B 00839	SM5 always reads out 255. Found & repaired cracked solder joint at QM5 on MB E.
47.	6/9/71	Three axis sine & random vibration (acceptance level) AVCO, Wilmington	No tests between axes. Comp test on return to MIT showed cntr. 1, low gain - no digital, only.
48.	6/10/71	MR B 00838	Chain one low gain replace front chamber assembly.
49.	6/18/71	z-axis random only (acceptance level - 1)	Instrument OK -
50.	6/24/71	MR B 00850	Chain 1 no counts. Found feed thru anode on filterboard end leaky - cleaned and re-installed counter - retest OK.
51.	7/12/71	Thermal Vacuum GSFC Chamber 240 (Qual Level)	Start of test. Instrument on 7/13/71 OK.
52.	7/14/71	Thermal Vacuum	Cold cycle - Instrument OK.
53.	7/15/71	Thermal Vacuum	Hot cycle started - Instrument OK.
54.	7/17/71	Thermal Vacuum (+30°C)	First evidence of chain 1 miscounting. Bit 4 in the chain 1 memory always reads out high in about the first 100 bins.
55.	7/17/71	MR B 00840	+30°C thermal vacuum. Chain 1 bit 4 reads out high in about the first 100 bins or so with no data input to memory. Instrument OK below +28°C.
56.	7/22/71	Thermal Vacuum	Start cold soak at 0°C. Instrument OK.
57.	7/24/71	Thermal Vacuum (0°C)	Chain 4 rates high with risetime antico on, normal with it off. Counter gain verified as stable. Change of performance with temperature is acceptable.

58.	7/27/71	Thermal Vacuum	End of test.
59.	7/29/71	Hot Soak (at MIT)	+40°C soak for 24 hours. Chain 1 memory problem did not recur.
60.	8/3/71	X-ray Calibration	No evidence of Chain 1 problem in a week of +25°C operating time.
61.	8/11/71	Hot Soak	+40°C soak for 30 hours. Chain 1 memory problem did not recur.
62.	8/16/71	Delivery	Instrument delivered to BBRC for interface tests.

4.4.2 Flight Unit -

Table 4-2 Summary of Flight Unit Tests and Problems

1.	12/28/70	MR B 04994	Chains 1,2,3,4,9 not driving rate counter. Replace 2N4880 in counter drive circuit, install current and voltage limiting to protect input bases of device.
2.	1/9/71	MR B 04998	Memory bit 1 does not remain cleared. Widened data pulse from memory to accumulator to provide at least 400 ns guard band.
3.	1/9/71	MR B 04997	No chain 2 counts in data. LLD turned off clamp attenuating output pulse from measurement chain. Added 100K base to ground at the turn-off clamp of all to measurement chains.
4.	1/14/71	MR B 00852	Pulse EQ7 not rising to full value. Gate input diode shorted. Replaced gate (see also FATR No. 1816. Cause of overload not isolated, believed due to operation of Varian Recorder interlock switch. Ref. conducted noise as cause in item 1 above).
5.	1/17/71	MR B 00855	Counting rates in chains 3,4,7,8 abnormally high with the calibrators on. Added shield to face of thin window counters to keep thin window source from illuminating rear chambers.
6.	1/18/71	z-z sine and random AVCO, Wilmington, (acceptance levels)	Instrument OK post shake (161)*
7.	1/18/71	x-x sine and random Wilmington (acceptance level)	HV monitor half voltage (161)

*Indicates Flight Log reference page.

8.	1/18/71	MR B 00853	HV Monitor half voltage. Malfunction not repeated in 700 additional hours of operation including 2+ weeks of thermal vacuum. Cause unknown. Malfunction involves HV monitor only which is not mission critical.
9.	1/19/71	y-y sine and random Wilmington (acceptance level)	1. HV monitor normal (162) 2. Chain 4 counting rate increased about 30% (163) 3. Chain 8 rate erratic.
10.	1/19/71	MR B 00856	Chain 4 shows an increase in calibrator on counting rate throughout shake (rates determined on a bin by bin basis). Pre and post shake 3 minute accumulation rates unchanged. Rate has been stable throughout 700 additional hours of operation.
11.	1/19/71	MR B 00857	Chain 8 erratic counting rate. System counting converter noise. aeasurement chain shield ground moved to an electrically quiet mode.
12.	2/3/71	Start thermal vacuum GSFC-Chamber 240	Chain 10 breakdown (193).
13.	2/5/71	Break vacuum	Replace counter 10 (197).
14.	2/5/71	MR C 00904	Chain 10 no X-ray pulses. Slow window leak causing breakdown in counter. Counter replaced. Failure believed due to faulty window attachment to strongback.
15.	2/10/71	z-z random only (acceptance level)	Instrument OK post shake (203).
16.	2/11/71	Start thermal-vacuum GSFC Chamber 240	1. Instrument OK at turn-on (205). 2. Radiation Monitor not turning off HV (207). 3. Chain 3 gain high (215).
17.	2/14/71	Break vaccum	
18.	2/17/71	Special test cycle, vacuum and cold temp. GSFC Chamber 240	Investigated RM and Chain 3 problems (218).

19.	2/12/71	MR B 00862	Radiation Monitor not disabling HV at 0°C. Design problem. Added 1000pf capacitor to monitor filterboard to increase signal level to monitor logic.
20.	2/12/71	MR C 00903	Chain 3 gain increase at 0°C. Counter gain changes with temperature. Use as is.
21.	2/25/71	Start thermal vacuum. GSFC Chamber 240	1. OK_h at turn-on. 2. 24^h at +30°C OK (235).
22.	2/26/71		1. 24^h at 0°C. Observed +8v loss of regulation known to exist in proto (257) Fix installed 3/14/71 (265) MR B 00834.
23.	2/27/71		1. 120^h at +30°C OK. Studied "long" pulses in neon (246).
24.	3/5/71		1. 120^h at 0°C. 2. Cold turn-on at +16v (251).
25.	3/6/71		1. Cold turn-on at +16v (253).
26.	3/7/71		1. Cold turn-on at +16v (255). 2. Observed chain 8 rate glitches (255). 3. Upper calibration actuator not operating unless "jogged". (256)
27.	3/10/71		Chamber problem. Temporary loss of pressure (261).
28.	3/11/71	Complete thermal-vacuum cycle	
29.	3/7/71	MR B 00847	Upper calibrator not pulling in at 0°C. Actuator spring tension high. Reduce to bring in line with correctly operating lower actuator (266).
30.	3/14/71	Design modification	Tie CO to PF. Noise sensitivity of memory reduced. See MR C 00906 (265).
31.	3/23/71	Design modification	Replace 5000MΩ safety resistors, chains 3,4, 7,8 with 1000MΩ (272).

32.	3/24/71	z-z axis random only (acceptance level) Wilmington	Instrument OK post shake (273).
33.	3/25/71	Start thermal vacuum. GSFC, chamber 241	24^h at 25°C on (276).
34.	3/27/71		48^h at 0°C OK.
35.	3/29/71	Complete thermal vacuum cycle	Instrument OK (285).
36.	3/31/71	Weight BBRC	OK (294).
37.	3/31/71	CG BBRC	+z dimension out of spec (295).
38.	4/1/71	Electrical Interface BBRC	1. Chassis gnd connection missing in S/C. (Installed 4/5/71.) 2. Signal ground noise out of spec. (298).
39.	4/2/71	Magnetic measurements BBRC	1. -z dipole moment out of spec. Was 800 gauss-cm^3, moved to 400 gauss-cm^3 by degaussing (299).
40.	4/5/71	Mechanical Fit BBRC	1. Found interference between connector brackets and instrument detector brackets (299). Connector brackets redesigned.
41.	4/6/71 4/12/71	Instrument Comprehensive Test in S/C BBRC	Instrument loses data randomly. Traced to jitter on simulated aspect pulses and occassional double pulsing from flasher.
42.	8/3/71	T/V cycle in S/C	1. Inst OK except Ch3 gain change with temp higher than expected.
43.	8/16/71	MR B 00843	Ch3 temp sensitivity found to be increasing. Gain OK @ 25°C. Disabled RT Antico, Ch3&4.

4.4.3 Unresolved Malfunction Reports - Only two malfunction reports are considered unresolved.

4.4.3.1 MR B 00853. HV Monitor Half-Voltage - This problem occurred in the Flight Unit on 18 Jan. 1971 and did not reoccur in the more than 1000 hours of operation of the instrument since that time. The cause of the malfunction is still unknown,but only the monitor circuit and not the HV supply is involved; therefore, the problem is not mission critical.

4.4.3.2 MR B 00856. Chain 4 shows an increase in calibrator on counting rate throughout shake. - The cause remains unknown.Chain 4 rates returned to the pre-shake value immediately after vibration testing and have remained there.

4.4.4 Failure Analysis Reports - The following Failure Analysis Termination Reports (FATR) were generated as a result of component failures in this program.

Table 4-3 Failure Analysis Reports Generated by the MIT OSO-7 Program

FATR No.	Date	Task Description
1816	3-22-71	Failure Analysis of one Fairchild F9040 integrated circuit and two Fairchild F9042 integrated circuits.
1818	3-19-71	Failure analysis of one Fairchild FM2894 transistor.
1874	4-29-71	Failure analysis of a Wilmore Electronics Company No. 001 transformer, a Components Inc. P224A capacitor and an Amelco JANTX2222A transistor.

FATR No.	Date	Task Description
1936	6-17-71	Failure Analysis of eight Semtech TXIN4948 diodes.
1937	6-23-71	Failure Analysis of eight Sprague 20C135A2X5E Ceramic disc capacitors.
2019	7-26-71	Limited Evaluation of Two Semtech JANTXIN4948 Diodes.

4.4.5 Critical Problems - In any program certain problems are identified as particularly bedeviling and/or unusually significant in terms of mission success or failure. Often the outcome provides a lesson applicable to future work. These are the problems that were of most concern during the MIT OSO-7 program.

4.4.5.1 Four-Color Proportional Counters - The change subdividing this design into two-chamber pairs with independent gas seals and mounting was initiated relatively late in the program after many attempts were made to remedy deficiencies in the original four-chamber design. The two-chamber pair design proved to be entirely successful and necessary to achieving mission objectives. Section 3.1.1.3 discusses this problem in more detail.

4.4.5.2 Fairchild 9040 Asynchronous Pulse Width Requirements - Direct set and clear pulse width requirements were initially unspecified for these devices and turned out to be far in excess of what could be inferred from available data. Considerable time and effort was spent in removing "bad" 9040's from the system when what was needed was an increase in asynchronous input pulse widths (see Section 3.2.5.1).

4.4.5.3 Effect of Conformal Coating Material on Measurement Chain Calibration - Electrical calibration was performed on the measurement chains (Section 4.3.1). Then the board areas were conformally coated using Solithane 113-300. As a result, preamplifier input capacitance increased, shifting the measurement chain gain downward by about twenty percent. Although recalibration was performed expeditiously, this problem is identified as causing an unnecessary repetition of previous effort.

4.4.5.4 Prototype High Voltage Diode Failure (JANTXIN4948) - The high voltage section of the prototype power converter failed in thermal vacuum at +35°C after 156 hours of operation(MR B 00842). Failure was traced to a pair of Semtech JANTXIN4948 diodes in the high voltage multiplier string. All eight diodes were forwarded to Goddard Space Flight Center for failure analysis. The analysis concluded (FATR #1936) that failure was due to surface inversion in the silicon dice caused by contaminants in the silicon dioxide passivation layer. Surface inversion leds to unacceptably high reverse leakage currents and thereby to the failure of the multiplier string. The remaining six diodes tested satisfactorily.

Subsequently, it was discovered that the manufacturing process occasionally produces voids in the diode case and that the case style of the diode had been changed to eliminate this problem. Discussions with the OSO Project Office and Goddard Failure Analysis and Parts Branch led to the conclusion that development of the surface inversion failure mode was unlikely after 250 to 300 hours of successful operation of the diodes in the converter. Case voids remained a concern although more than 300 hours of successful Flight Unit operation argued against their presence. On an operating time basis it was decided not to replace the high voltage multiplier strings in the prototype and flight converters. Spare multi-

plier modules were fabricated using JANTXIN4948 diodes with the new case style for use in case the problem developed again. An additional step was included in the diode acceptance procedure to screen for the surface inversion failure mode. The problem has not recurred in either instrument.

4.4.5.5 Calibration Actuator - The original design of the calibration actuator incorporated a Bendix flex-pivot in lieu of the bearing and spring finally used. One flex-pivot failed in shake,and the subsequent redesign changed the simple shutter into a sophisticated electro-mechanical design. Section 3.1.4 includes a discussion of the design changes.

4.4.5.6 Consideration of a Collimator Thermal Cover - A concern throughout the program has been the veracity of the thermal analyses determining the orbital temperature variations of the MIT collimators. The MIT instrument is not one thermal mass because of the electrical isolation required between the detector brackets and the baseplate (see Section 3.7.3). Temperature variations of more than a few degrees Centrigrade over an orbit are undesirable because of gain variations with temperatures of Counters 3 and 4 (Section 3.1.1.4).

Consideration was given to the use of x-ray transparent aluminized covers to reduce the heat absorbtion/radiation ratio of the bare collimators, which act as black bodies. The covering considered most useful was a 300 ng cm^{-2} film of kimfoil (polycarbonate) with a 6000 Å layer of aluminum. The decision was made not to use this covering as a result of discussions between the MIT group and Goddard thermal experts, particularly C.G. Dan, Jr., which led to the conclusion that worst case counter temperature excursions would be no greater than $\pm 4°C$ over the orbit.

4.4.6 Flight Unit Status at Launch - The following list shows the location of particular instrument components by serial number. Information is provided only on the most referenced parts. Information on other parts and devices is available in the Q/A records.

Table 4-4 Configuration of Flight Unit and Flight Spare at Launch

Serial Number (Rear of Baseplate)		Flight Unit 2	Flight Spare 1
Counters:	1° thin window	7629	7539
	1° 4-color front	6828F	11172
	1° 4-color rear	6828R	6825R
	3° thin window	7542	7540
	3° 4-color front	6826F	6829F
	3° 4-color rear	6826R	6829R
Sources:	1° thin window	5128-7	5128-1
	1° 4-color	5128-6	5128-4
	3° thin window	5128-5	5128-3
	3° 4-color	5128-4	5128-2
Thermistor	Baseplate	2	31
	1° counter	14	15
	3° counter	11	10
	Memory	1	33
	Power converter	3	4
	Upper actuator	6	5
Radiation Monitor Tube		3526	3508
HV Set Points		(Ne) (Ar) (Kr) (Xe) 1320, 1920, 2510, 2470	(Ne) (Ar) (Kr) (Xe) 1260, 1870, 2490, 2380
Memory Sequence Bits		011	010
Special Changes:		R/T Antico disabled in chains 3 and 4	

4.5 Comments on Test and Calibration Procedures

The test and calibration phase of the program was particularly lengthy. It would have been shortened considerably had certain design problems been discovered prior to the start of thermal vacuum testing. Sequential, rather than parallel, thermal vacuum testing of the Prototype and Flight Units would have helped as well.

1) Prototype calibration was put off until refurbishment because of pressure to deliver the Flight Unit. Had calibration been performed on the Prototype, the effect of the conformal coating material on preamplifier gain would have been determined earlier and the calibration procedures, techniques, and equipment would have been fully debugged before calibration of the Flight Unit. A faster, more accurate calibration of the Flight Unit would have resulted.

2) Temperature cycling of the completed Prototype was omitted to get the instrument into thermal-vacuum as quickly as possible. Had this test been performed, the temperature dependent problems in the Radiation Monitor and plus volt section of the Power Converter and the memory noise susceptibility would have been uncovered before thermal-vacuum testing. Had the Flight Unit been similarly cycled prior to thermal-vacuum, a number of counter and calibration anomalies would have been detected, expeditiously investigated, and disposed of. Design changes, where necessary, could have been incorporated at MIT here they could be done most easily.

3) Although the thermal-vacuum test facilities at GSFC are excellent and the cooperation of the test group there very good, the duration of the test cycle argues in favor of using test facilities closer to home from both the standpoint of travel costs and traveller convenience.

5.0 NEW TECHNOLOGY

The following areas are identified as representing significant new technology originating on this program. The reader is referred to each report section listed for a discussion of the work.

5.1 Four-Color Proportional Counters

Section 3.1.1

5.2 19.2 Kilobit Shift Register Memory

Section 3.2.3

5.3 X-Ray Collimators

Section 3.1.2