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SPREAD SPECTRUM COMMUNICATION LINK USING SURFACE WAVE DEVICES

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16. Abstract This development has resulted in a fast lock-up, 8-MHz bandwidth 8,000 bit per second data rate spread spectrum communication link breadboard that is implemented using surface wave devices as the primary signal generators and signal processing elements. It uses Surface Wave Tapped Delay Lines (SWTDL's) in the transmitter to generate the signals and in the receiver to detect them. The system also incorporates a reentry delay line which increases the effective length of the tapped delay lines eight-fold. A theoretical and experimental analysis of the processing gain achieved by the SWTDL's Circulating Integrator and other components in the breadboard has been performed, establishing design information for future development. The breadboard provides a measured processing gain for Gaussian noise of 31.5 dB which is within one dB of the theoretical optimum. This development demonstrates that spread spectrum receivers implemented with surface wave devices have sensitivities and complexities comparable to those of serial correlation receivers, but synchronization search times which are two to three orders of magnitude smaller.

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LIST OF SYMBOLS

Symbol	Definition
AGC	Automatic Gain Control
CI	Circulating Integrator
CW	Continuous Wave
DEMOD	Demodulator
DPSK	Differential PSK
IF.	Intermediate Frequency
PG	Processing Gain
PLL	Phase Lock Loop
PN	*Pseudonoise*
PSK	Phase Shift Keyed
rf	Radio Frequency
RFI	Radio Frequency Interference
S/N	Signal-to-Noise
SWTDL	Surface Wavt Tapped Delay Line
TBT	Thompson-Butterworth Transitional Lowpass Filter
TDRS	Tracking and Data Relay Satellite
VCXO	Voltage Controlled Crystal Oscillator

PREFACE

The objective of this development was to demonstrate the feasibility of a spread spectrum communication link concept implemented with surface wave devices. A breadboard link with an 8-MHz bandwidth and an 8-KHz data bit rate has been built and evaluated. It has two modes of operation: one with a coherent demodulator and one with a transmitted reference-type demodulator. The evaluation includes operation in Gaussian noise, narrowband RFI, multiuser, and multipath environments.

The receiver has a 30 dB time bandwidth product and is designed to transmit digital data.

The evaluation has resulted in the following conclusions: (explained in more detail in Section 2.0).

- Spread spectrum communication links can be implemented using surface wave devices so that the sensitivity in Gaussian noise is within 1 to 2 dB of the theoretical value, and the synchronization search time is reduced by more than two orders of magnitude relative to serial correlation links.

- The breadboard system operating in the coherent PSK mode has a measured processing gain of 31.5 dB in Gaussian noise out of theoretical 32.5. The majority of this small degradation compared to ideal operation results from internally generated noise in the course of normal system development. The surface wave devices operated near perfectly, contributing very little to the system loss.

- The double pulse (transmitted reference) mode is very simple to implement and has the same synchronization search time advantage as the coherent PSK mode; however, it will only find application in requirements where simplicity is more important than receiver sensitivity, because it has 6 dB less processing gain than does the coherent mode.

- The RFI rejection capability of the breadboard is not the best because of repetitious nature of the signals used in the system. The rejection of narrowband interference is 10 dB less than that of Gaussian noise. This degradation can be reduced in future systems by the use of specially designed surface wave devices and longer PN codes in the re-entry delay line.

From the preceding conclusions, it is recommended that the Coherent PSK mode surface wave spread spectrum communication link be considered for the TDRS application and that the following future developments be carried out toward this end:

- Modify the design to work with the specific frequencies and bandwidths presently planned for the TDRS system.
- Design and build an Engineering Test model of the modified design reducing its complexity and increasing its reliability.
- Test the system in a simulated space environment.

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1.0 INTRODUCTION

Considerable effort has recently been expended in the realization of practical surface wave devices. The purpose of this development is to build on this background knowledge and to take advantage of the unique signal processing capabilities of surface wave devices in order to improve the operation of the wideband links used in space communications. A breadboard using these devices as the sole signal processing elements has been designed, built, and tested by Magnavox. In addition, an analytical study of the surface wave devices and the system design has been performed to establish the design parameters needed to realize effective communication links with performance near the theoretical optimum value.

This final report begins by describing the system design and its operation. The equipment is constructed with two different modes of operation selectable by front panel controls. The operation of each mode is described separately. The operation of the breadboard in a Gaussian interference environment has been analyzed using normalized parameters so that the results presented in this report will be useful for evaluating general systems of this configuration. The synchronization process is analyzed in Section 4.0, illustrating the operation and predicting the synchronization times as a function of system parameters.

The parameters of the breadboard along with a summary of the measured and calculated performance data are tabulated in Section 5.0. Section 6.0 presents a brief cross-system comparison contrasting both modes of the breadboard with a projected prototype surface wave system and a conventional serial correlation receiver. Alignment procedures and setup instructions are presented in Section 8.0.

2.0 CONCLUSIONS AND RECOMMENDATIONS

The successful operation of the breadboard feasibility model and the analysis of the performance led to the following conclusions and recommendations.

2.1 Conclusions

(a) The use of surface wave communication links for spread spectrum communications provide nearly optimum sensitivity with short lockup times and little system complexity.

(b) The breadboard operating in the PSK mode provides 31.5 dB of processing gain in Gaussian noise out of a possible 32.5 dB. The majority of the degradation arises from internally generated noise which will be removed during the course of normal system development.

(c) The surface wave tapped lines provide nearly optimum processing gain with practically no degradation.

(d) Spread spectrum links implemented with surface wave signal processors will operate within 1 to 2 dB of the theoretical limit while reducing the synchronization search time by two orders of magnitude when developed for production.

(e) The Double Pulse Mode to the surface wave communication link will only be used in applications where system simplicity is more important then link sensitivity.

(f) The RFI rejection capability of the breadboard is 21.5 dB*; this rejection can be improved 8 to 10 dB by increasing the PN generator code length and by changing SWTDL design.

2.2 Recommendations

It is recommended that the Coherent PSK Mode Surface Wave Spread Spectrum Communication Link be considered for the TDRS application and that the following future developments be accomplished to achieve this end:

(a) Modify the design to work with the specific frequencies and bandwidths presently planned for the TDRS system.

(b) Design and build an engineering test model of the modified design in order to reduce its complexity and to increase its reliability.

(c) Test the system in a simulated space environment.

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* Interference frequency is set to make receiver most vulnerable.

3.0 SYSTEM CONCEPT

3.1 Design Objectives

The objective of the Spread Spectrum Communication Link development project was to develop a laboratory breadboard model link to convey digital data at a rate of approximately 8000 bits/second, utilizing an rf bandwidth in the vicinity of 8 MHz. A center frequency of 32 MHz results in a 25 percent bandwidth for the surface wave devices, and this is a favorable choice in terms of performance. Lowering the percent bandwidth makes the system more sensitive to temperature, doppler, and frequency offset; raising the percent bandwidth makes impedance matching more difficult and also increases the device insertion loss.

Proof of concept feasibility is the ultimate goal in the project, with a specific performance objective of realizing a large receiver processing gain. The minimum permissible achievement is +22 dB.

Surface wave devices are to be used for transmitter signal generation and for the basic signal processing functions in the receiver. Four pairs of coded surface wave devices (each pair with a different code) are to be included in the breadboard equipment so that tests may be run to evaluate the effects of using different codes to convey the data.

The TDRS application requires that communication be carried out in an environment of Gaussian noise, narrowband RFI, multiuser noise, and specular multipath. Therefore, the system performance is to be evaluated in the face of such sources of interference; and system design parameter specifications are chosen with that in mind.

3.2 Coherent PSK Mode Concept

3.2.1 Basic Principles

Acoustic waves can be launched on the surface of any solid; and if the material is piezoelectric, they can be launched by applying a voltage to interdigitated thin film conductors deposited on the surface. Acoustic-to-electrical conversion occurs when acoustic surface waves pass under interdigitated thin film conductors.

Surface waves travel at a velocity of three microns/nanosecond, approximately 100,000 times slower than electromagnetic waves; and they are accessible at every point along their path. They are nondispersive and propagate with little loss, making possible the construction of rugged, compact, wideband, multiple tap delay lines. These features make surface wave technology attractive for signal processing applications.

When the acoustic wave passes under an array of uniformly spaced taps, the sum of the tap voltages is a periodic signal. The frequency of the signal is a function of wave velocity and conductor spacing; if many taps are used, an output pulse duration of several microseconds results

for each impulse applied to the input transducer. If the relative phase of the tap outputs is changed at intervals along the path, a pseudonoise (PN) phase-modulated rf signal results.

The illustration in Figure 3-1 shows a surface wave encoder/decoder pair designed to generate a 13-bit Barker code at 100 MHz with a bandwidth of 10 MHz; also shown are oscillograms of the encoded and decoded signals.

The matched filter (decoder) output is an rf signal with a prominent triangular envelope peak corresponding to the autocorrelation of the PN sequence selected for the output transducer design. The phase of the rf carrier within the correlation peak is determined by the polarity of the input pulse, and information can be modulated onto the surface wave device output by controlling the phase of an input pulse train. The information is retrieved by sensing the carrier phase in the correlation peaks in the matched filter output.

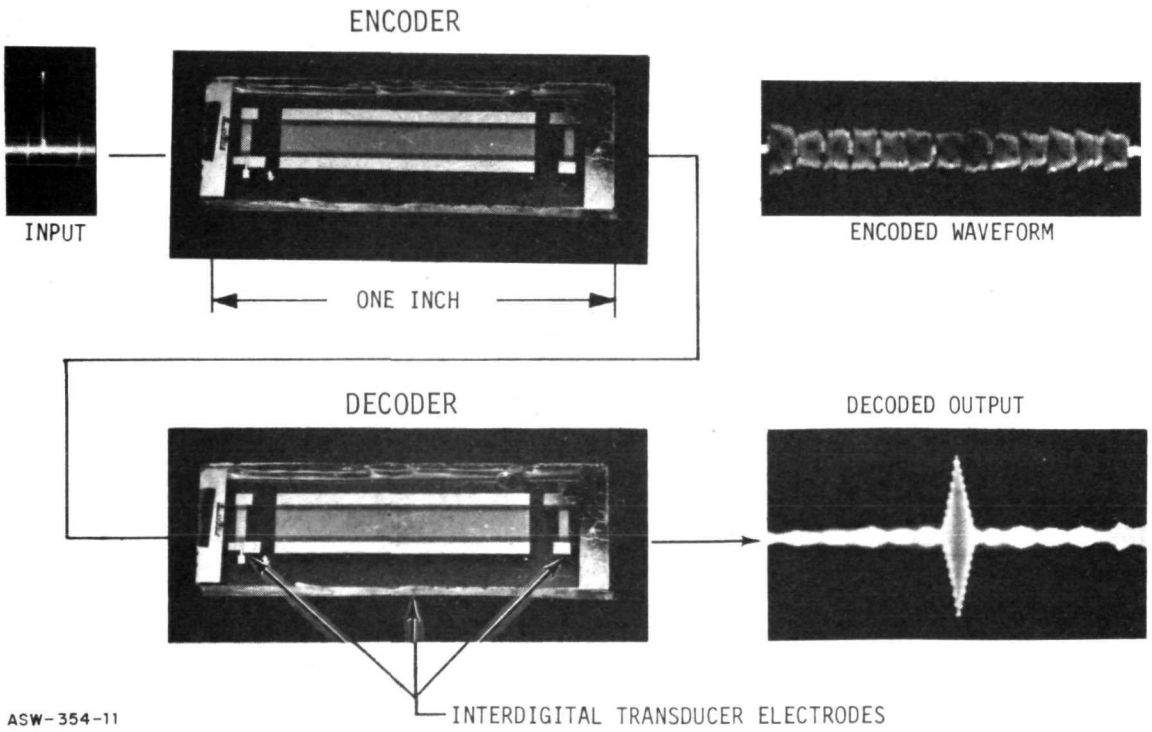

Figure 3-1. Surface Wave Tapped Delay Line Signal Encoding and Matched Filtering

3.2.2 Fundamental Method of Implementation

The size of surface wave devices is a limiting factor in terms of code length for spread spectrum signal generation and matched filter detection applications, but this difficulty is avoided when a re-entry delay line is used to coherently add several consecutive correlation peaks. This accomplishes a linear summation over an interval corresponding to several input pulses to the surface wave tapped delay line encoder, extending the effective code length (time-bandwidth product) in proportion to the number of iterations in the re-entry delay line. The concept is illustrated in Figure 3-2.

The PN sequence generator in the transmitter serially encodes the input data stream, spreading the spectrum of the baseband signal by producing in each data bit interval a sequence of narrow pulses of changing polarity. The encoded baseband pulse stream is applied to a Surface Wave Tapped Delay Line (SWTDL) which further encodes the signal in accordance with the pattern of the interdigital conductors comprising the output transducer. (A code length of 127 is assumed for the tapped delay line output transducer.)

The output transducer is designed in such a way that each narrow input pulse generates a longer PN encoded pulse at the desired center frequency (IF.). When the input pulse repetition period equals the duration of the surface wave device output pulse, a constant envelope spread spectrum IF. signal results.

In the receiver, the spread spectrum signal is first processed by a SWTDL (matched filter) like that used in the transmitter, and a periodic sequence of correlation peaks results. The repetition rate of the correlation peaks corresponds to the repetition rate of the pulse generator used in the transmitter, and the phase in each depends upon both the signal from the PN generator used in the transmitter and the data signal.

The matched filter output is applied to a serial decoder along with the output from a synchronized sequence generator like the one used in the transmitter. Another sequence of constant amplitude correlation peaks appears at the output of the serial decoder, but now the phase of the IF. carrier in the correlation peaks is determined solely by the data being conveyed.

These correlation peaks are applied to a re-entry surface wave delay line. The delay line output grows linearly in amplitude as each input correlation peak adds directly in phase with the signal recirculated from the delay line output. A phase detector* senses the phase of the

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* The phase detector requires a coherent reference for operation in this case. In the coherent PSK mode of operation, the reference is derived by phase locking a local oscillator to the received IF. signal in the correlation peaks at the re-entry delay line output. Since the polarity of the phase lock oscillator signal is arbitrary, the system has phase ambiguity.

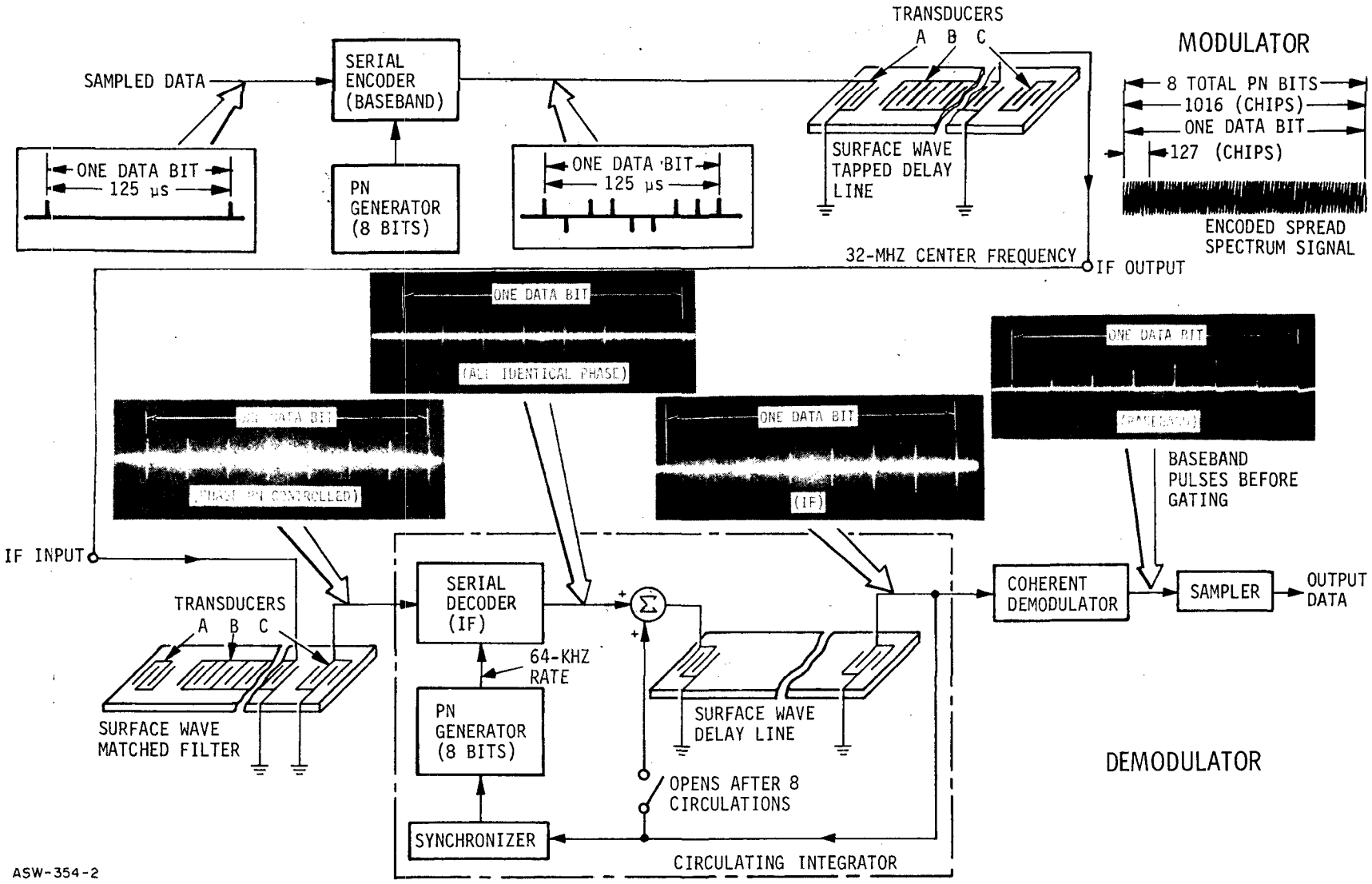

Figure 3-2. Functional Diagram of a Coherent PSK Spread Spectrum Modem

carrier, yielding a sequence of baseband pulses with amplitudes corresponding to those at the delay line output. (The polarity of the baseband pulses is determined by the data; they build in the positive direction for a data "1", negative for a "0".)

The largest peak is sampled and applied to the demodulator output, and simultaneously the delay line is "dumped" in preparation for the next coherent pulse buildup. The dump command is forced to coincide in time with the data intervals.

Although positive feedback is used in the recirculating loop, no stability problem occurs because the line is dumped intermittently. Furthermore, no significant loss in processing gain occurs when the closed loop gain is between 0.95 and 1.05.

Substantial benefits are derived by combining serial and parallel processing techniques as illustrated in this concept. Spread spectrum signals can be generated by simple, compact, rugged, and reliable surface wave devices without the need for rf oscillators. Processing of the high frequency components of the spread spectrum signal is done by surface wave devices, and the logic circuits operate at clock rates less than 100 kHz.

When impulses driving a SWTDL are serially encoded, an effective code length many times that produced by the delay line itself results. This permits achievement of a large demodulation processing gain when a surface wave matched filter is used in conjunction with a recirculating delay line and a serial decoder. Good performance is realized because SWTDL's operate as nearly perfect matched filters, and rapid lockup is obtained because the matched filter processes many code bits in parallel.

3.3 Double Pulse Mode Concept

3.3.1 Principle of Operation

The preceding discussion described the Coherent PSK method of transmitting data in which data bits are represented by the phase of the transmitted signal relative to a fixed reference signal. Bipodal PSK was used, and the carrier for a data "1" was in phase with the fixed reference signal while that for a "0" was 180 degrees out-of-phase with the reference signal. The data was demodulated by establishing a local reference and comparing the phase of the received signal carrier (in the correlation peaks) with that of the reference.

An alternate method is to transmit the reference signal along with the modulated signal; and this is sometimes done, in communication systems, by using a CW reference. Such a system is vulnerable to strong narrowband interference, however, when the reference is extracted at the receiver by a narrowband filter. This potential difficulty can be avoided if an encoded reference signal is transmitted along with the encoded modulated signal, and it is done in this project by a method termed Double Pulse Modulation.

The principle of operation is as follows. The SWTDL encoder at the transmitter is activated by a sequence of pulse pairs rather than a sequence of individual pulses. Polarity of the first pulse in every pair is independent of data, but the polarity of the second pulse is serially encoded by the data. Both pulse pairs are then encoded by an 8-bit PN generator, just as described for the Coherent PSK Mode.

Time spacing between the two pulses comprising the pair is constant and short relative to the duration of the SWTDL impulse response duration; but, it must be made larger than one chip* time. If the proper spacing is chosen, the composite signal appearing at the encoding SWTDL output has a virtually constant envelope. Furthermore, distinctly separate autocorrelation peaks will occur for the signal and the reference at the output of a matched filter built to detect the signal if a code with good autocorrelation characteristics is chosen.

At the matched filter output, the phase of the carrier within the correlation peak representing the leading pulse (reference) in every pair received will be independent of the data, reflecting only the PN generator modulation. The carrier phase within the second pulse in every pair will be either 0 or 180 degrees relative to the first, depending upon the data. Data can therefore be extracted by comparing the relative phase of the pulse pairs.

Since pulse pairs occur at a fixed repetition rate, they can be added coherently in a re-entry delay line just as in the Coherent PSK case previously described. The serial PN generator encoding signal must first be extracted as before; then, the correlation peak pairs will linearly increase in amplitude with each iteration through the delay line during the course of each data bit interval.

Each data bit is then recovered in the last recirculation interval prior to line dumping by delaying the "reference" correlation peak and multiplying it with the "information" correlation peak. This product is appropriately filtered and sampled to reconstruct the data stream.

3.3.2 Double Pulse Mode Implementation

The basic method of implementing the Double Pulse Mode is further described by reference to Figures 3-3 and 3-4. In Figure 3-3 the modulation concept is shown in principle. Two separate outputs are produced by the pulse pair generator, one being a reference pulse sequence of uniform polarity. These are time coincident and encoded in an identical manner by an 8 bit PN sequence yielding two streams of baseband encoded pulses.

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* The term chip time is used to define the individual element size of the code placed on the surface wave tapped delay lines and to distinguish it from the bit times representing either the data or the PN generator code.

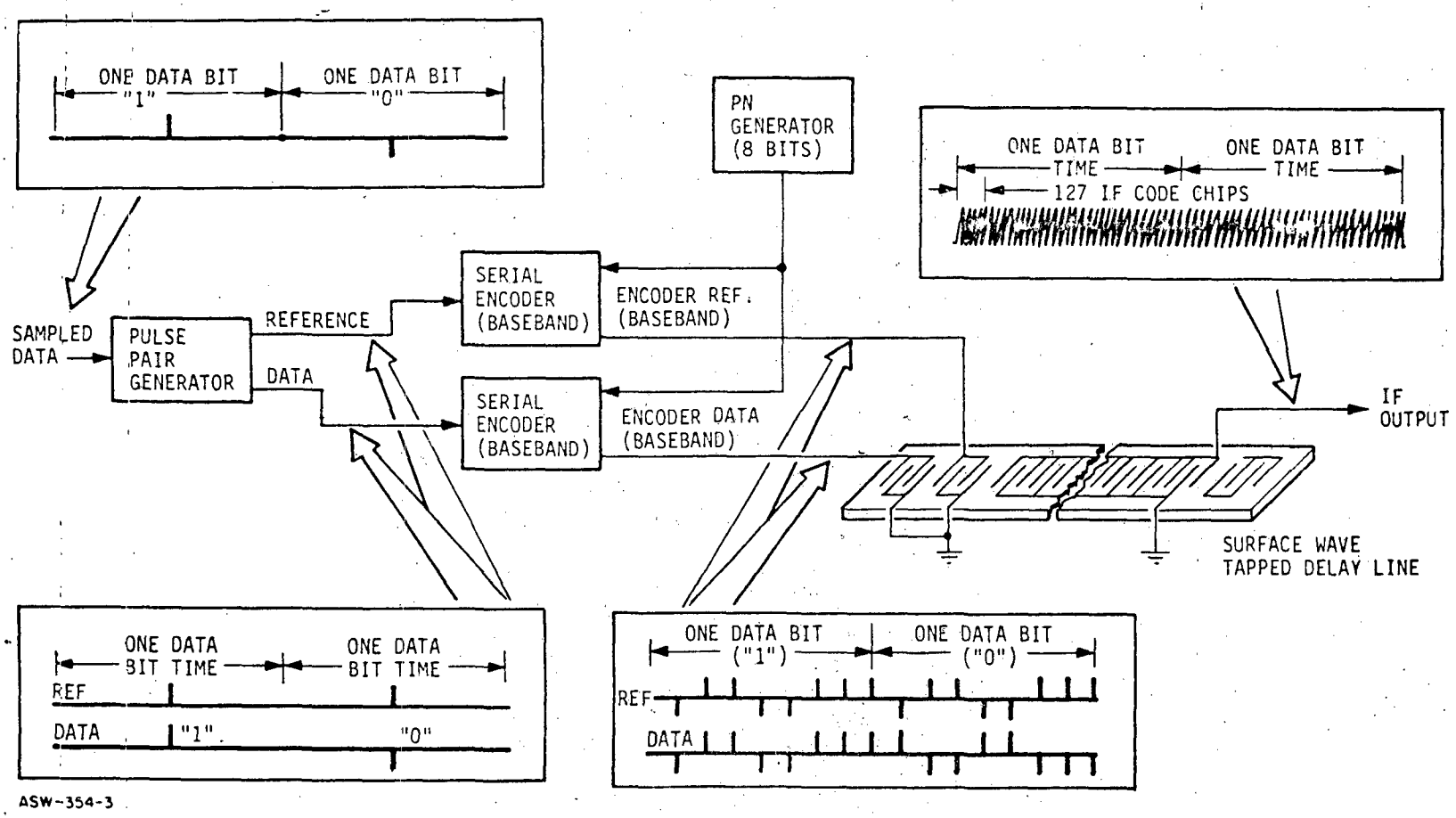

Figure 3-3. Double Pulse Spread Spectrum Modulation Concept

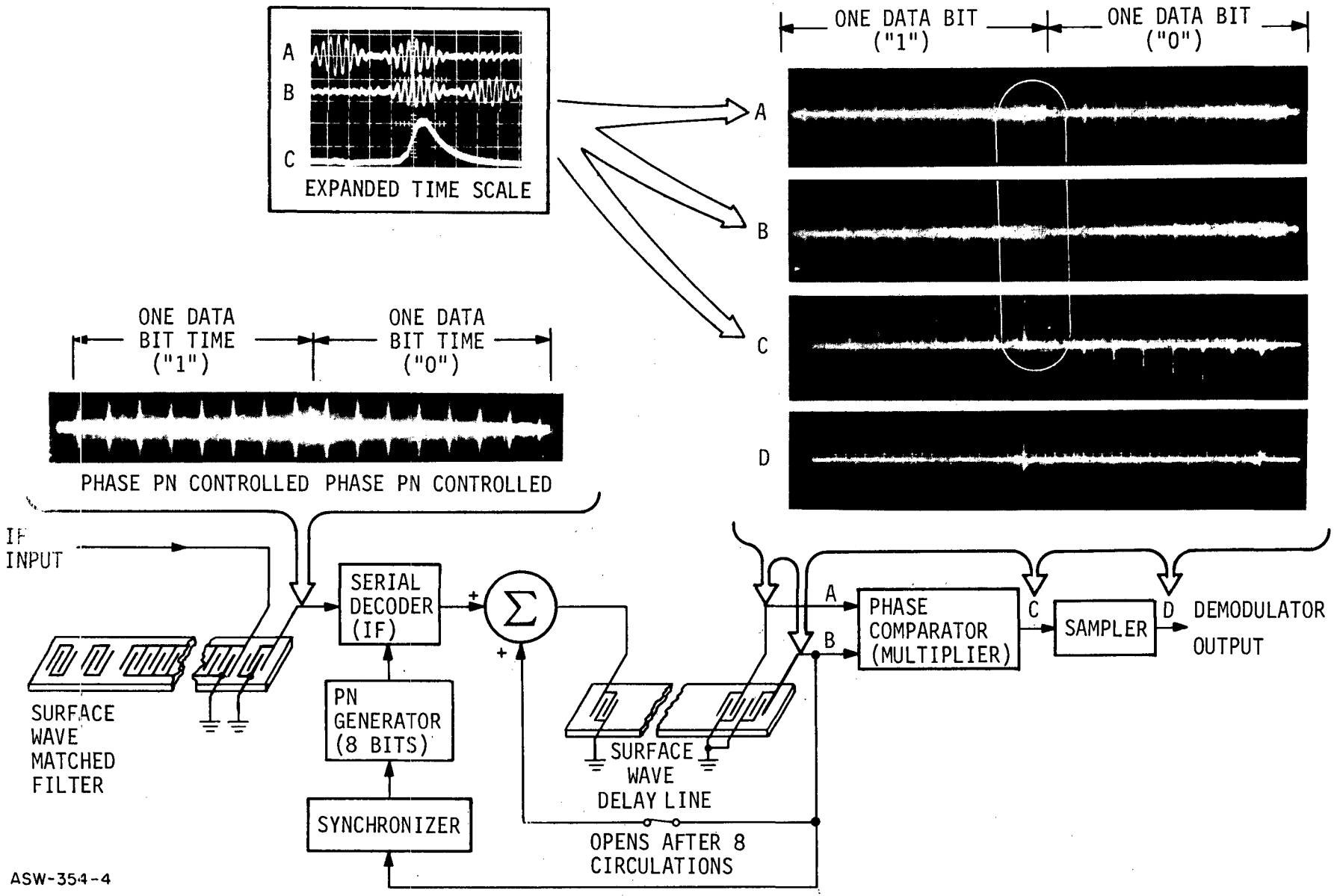

Figure 3-4. Double Pulse Demodulator Concept

When a data "1" is being sent, every pulse of the serially encoded baseband data signal is in phase with its time coincident counterpart in the reference signal stream. When a "0" is sent, the pulses of the two baseband encoded streams are all opposite in polarity.

Time delay is introduced between the two encoded signals by using separate input transducers on the SWTDL. The reference input transducer is placed closer to the output transducer pattern, advancing it in time relative to the data signal. The two signals combine linearly in the acoustic domain, and a constant envelope signal comprising the encoded reference and data signals with a fixed relative delay between them appears at the output transducer.

In the receiver, a matched filter is used which produces a sequence of paired correlation peaks. Since these were modulated by an 8 bit serial PN signal at the transmitter, the matched filter output is next passed through a serial decoder to remove that modulation. (The locally generated PN sequence is synchronized with the one used in the transmitter.)

The serial decoder output is a stream of paired correlation peaks with an envelope identical to that shown at the matched filter output. If the phase of the carrier in each peak were examined, however, it would be seen that: 1) the carrier phase in every reference peak is identical, 2) the carrier phase in the data (information) correlation peaks is constant within each bit interval, 3) the carrier phase for a data "1" is identical to that in the reference, and 4) the carrier phase for a "0" is exactly opposite to that in the reference.

Since the carrier phase remains constant throughout each bit interval in every case, the correlation peaks add coherently in the re-entry delay line and grow in amplitude.

Two output transducers are used in the re-entry delay line with relative spacing the same as that used for the two input transducers on the encoding SWTDL in the transmitter modulator. This causes the reference pulse correlation peaks on line B (see Figure 3-4) to coincide with the information pulse peaks appearing on line A.

Multiplying the signals on the two lines results in a sequence of pulses which increase in amplitude during each bit interval. When a "1" is present the multiplier output pulses are all positive; and for a "0" they are all negative.*

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* The expanded time scale photographs show two pairs of pulses appearing at the delay line outputs. It also shows the filtered and inverted product of the two signals.

Each time, after eight recirculations have been made in the re-entry delay line, the (last) pulse in the multiplier output stream is sampled, and data is reconstructed from these bipodal sampled pulses by conventional means.

4.0 SIGNAL DETECTION ANALYSIS

4.1 Introduction

The spread spectrum modem described in the previous section performs a signal processing function which can be analytically described as a matched filter. A matched filter is defined as a signal processor which provides the best Gaussian noise suppression* for a specific signal; therefore, the purpose of this section is to estimate how well this modem can be made to operate relative to a perfect matched filter. The block diagram shown in Figure 4-1 separates the system into sections according to functions and tabulates sources of signal processing degradation as a function of the practical parameters of each section.

The pulser provides a series of narrow pulses to the SWTDL signal generator which in turn generates the wideband PSK signal. The stability of the pulser must be sufficient so that the SWTDL output is coherent, and the pulse level must be sufficient so that the signal out of the SWTDL is significantly above the transmitter amplifier noise.

The pre-transmission filter reduces the processing gain of the receiver by limiting the bandwidth of transmitted signal. The SWTDL matched filter extracts the signal from the channel, theoretically providing a signal-to-noise improvement (processing gain) equal to the number of taps it contains. The transducers and matching networks must have sufficient bandwidth so that the signal is not distorted, and the taps must be accurately located to match those in the SWTDL signal generator. Temperature variations between the transmitter and receiver, doppler shift, and frequency offset of the input signal also reduce the processing gain below the theoretical value.

The Circulating Integrator (CI) theoretically provides an additional processing gain equal to the number of circulations utilized in the signal detection process. In order to realize the theoretical signal-to-noise improvement, the delay line used in the CI must have wideband transducers with matching networks and a wide dynamic range.

The data is extracted from the rf CI output signal by a demodulation process. In the PSK mode, the demodulator is coherent and provides near perfect performance when the carrier regeneration loop is jitter free and a sharp cut-off filter is used at the output. If the theoretical processing gain is to be achieved, the signal must be sampled with a very narrow, precisely located sampling pulse. This sampling pulse is derived from a baseband phase lock loop built into the receiver.

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* The best signal-to-noise improvement provided by a matched filter is equal to the ratio of the signal modulation rate to the data bit rate. The breadboard signal bandwidth to data bit rate ratio is 33 dB, and an input signal buried in -15 dB of Gaussian noise will result in a +18 dB S/N output if the breadboard works perfectly.

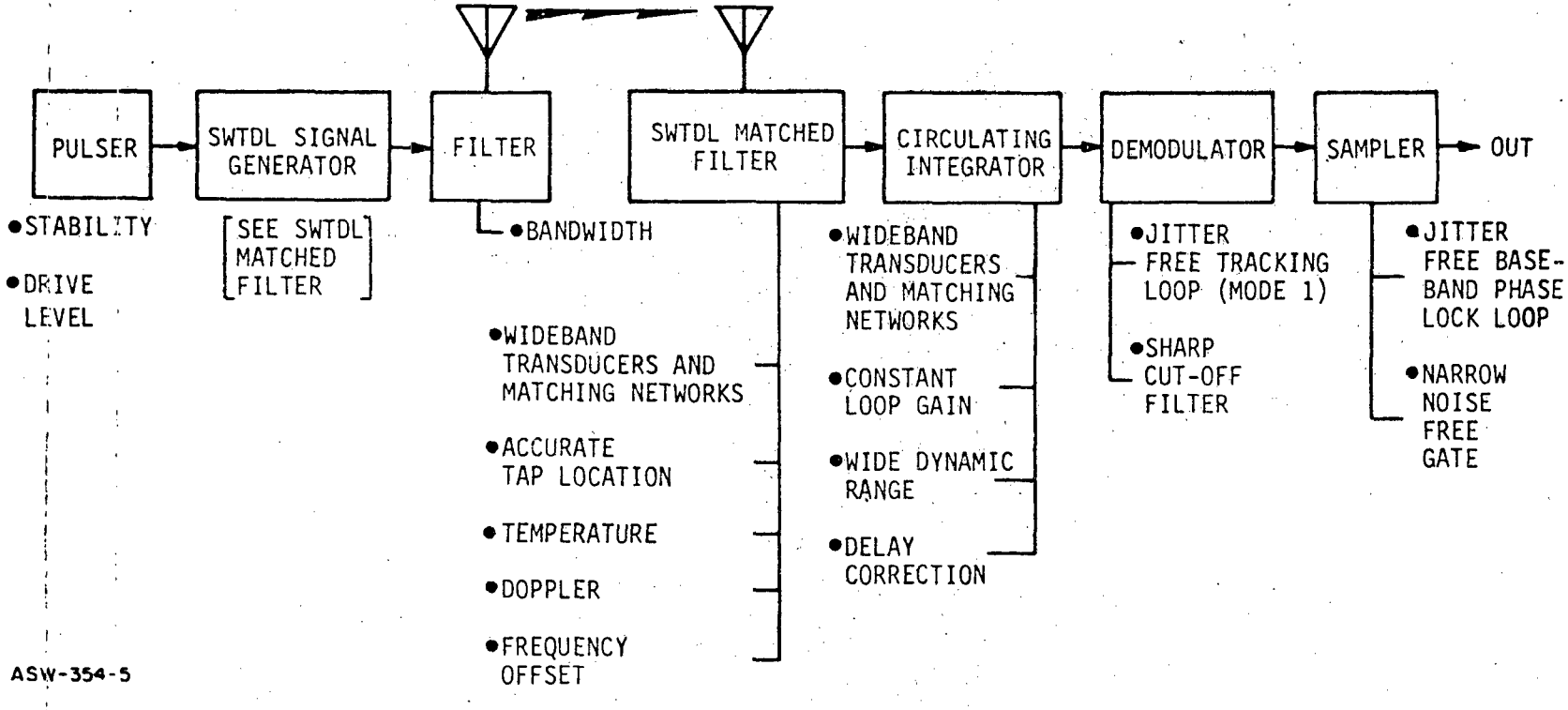


Figure 4-1. Matched Filter Critical Parameters

In the following paragraphs, a theoretical estimate of the performance of each of the system sections is given. The expected loss of processing gain, which can be expected in the breadboard modem, is presented.

4.2 Pulser

A pulser is used in the transmitter to excite the SWTDL's and to generate the spread spectrum output signal. There are three parameters of this pulser which have a direct effect on the system processing gain:

(a) Pulse Rate Stability
(b) Pulse Width
(c) Pulse Level

4.2.1 Pulse Rate Stability

The pulse rate stability required to achieve optimum processing gain depends on the center frequency of the SWTDL and the data bit rate of the system as shown in Figure 4-2. Since the breadboard SWTDL has a center frequency of 32 MHz, a data bit rate of 8 kHz, and a pulser with a short term stability greater than $\pm 10^{-8}$ the processing gain lost due to pulser instability is negligible.

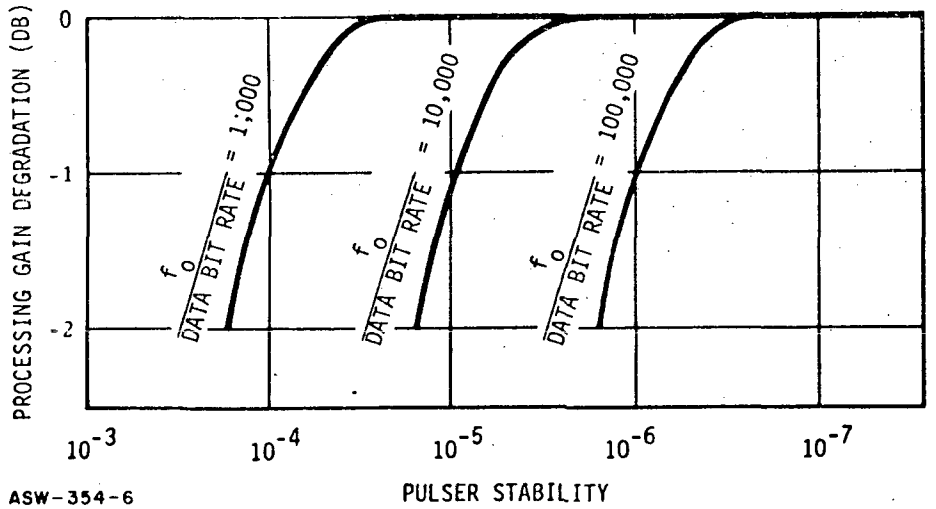


Figure 4-2. Processing Gain Degradation vs Pulser Stability

4.2.2 Pulse Width

The pulse width must be sufficiently narrow so that the spectrum of the pulse train has significant energy in SWTDL bandwidth. Since the breadboard SWTDL's have a center frequency of 32 MHz and a bandwidth of 8 MHz, the 25-ns pulse provided by the pulser has a sufficiently wide spectrum to have a reasonable percentage of energy falling in the SWTDL bandwidth.

4.2.3 Pulse Level

In addition, the pulse amplitude must be large enough to cause the SWTDL signal generator output power to be well above the noise floor of the transmitter amplifiers. Insufficient SWTDL output power degrades processing gain by reducing the actual signal power transmitted by a fixed power transmitter and by adding noise which must be suppressed in the receiver. The resulting processing gain degradation depends on the SWTDL signal generator signal output power to transmitter amplifier noise power ratio as shown in Figure 4-3. This ratio is determined from the pulse level; the pulse width to SWTDL impulse response duration ratio;

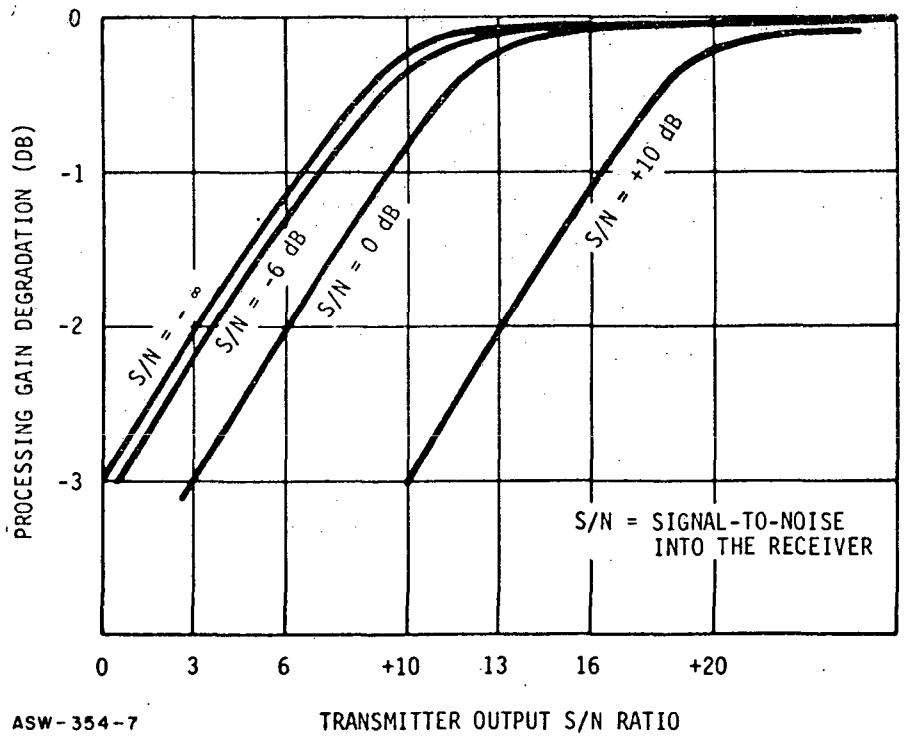


Figure 4-3. Processing Gain Degradation vs Transmitter Output S/N

the percent of pulse spectrum, which falls within the SWTDL bandwidth; the SWTDL insertion loss; the noise figure of the transmitter amplifier; and the bandwidth of the system. The measured breadboard SWTDL signal generator to transmitter noise power ratio is 8.7 dB. This indicates that a processing gain degradation of 0.5 dB will be realized when the signal-to-noise ratio at the receiver input is less than -6 dB.

4.3 Pretransmission Filter and Amplifier

Pretransmission filters are required in spread spectrum transmitters in order to avoid interfering with links operating in adjacent channels. The typical PN encoded SWTDL signal generator produces a PN phase-shift-keyed cosine wave which has a $(\sin x/x)^2$ power spectrum centered about the SWTDL center frequency and extending over the entire frequency range. If a perfect brick-wall pretransmission filter is placed in the transmitter to limit the transmitted signal bandwidth, there will be a loss in processing gain when the signal is processed by the SWTDL matched filter as shown in Figure 4-4. Since the breadboard pretransmission filter is a single-pole filter with a bandwidth of 8.8 MHz, the breadboard will lose 0.5 dB of processing gain due to the pretransmission filter.

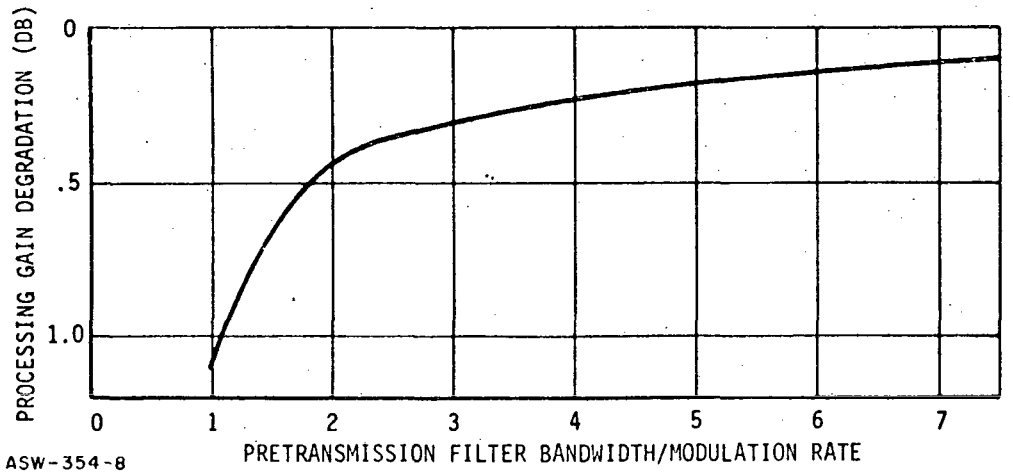


Figure 4-4. Processing Gain Degradation vs Pretransmission Filter Bandwidth

4.4 SWTDL Signal Generator and Matched Filters

4.4.1 Processing Gain in SWTDL's

In communication links similar to the breadboard, the SWTDL is used as a first stage processor for the signals transmitted to the communication link receiver. The SWTDL matched filter receives the desired signal which is contaminated by interfering signals (noise). See Figure 4-5.

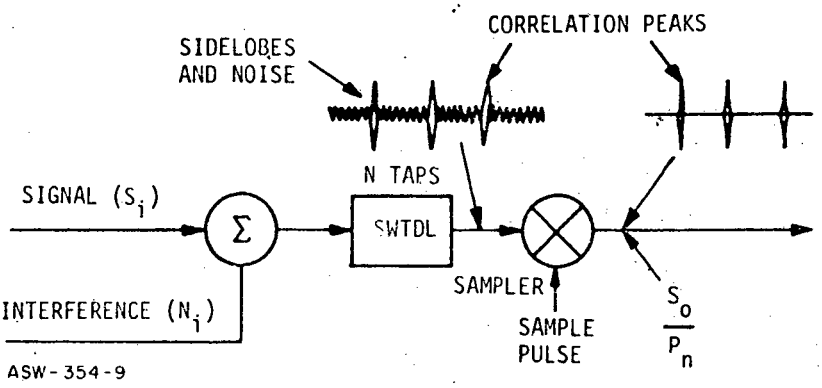


Figure 4-5. Processing Gain of SWTDL

Interfering signals, in this context, may be considered as receiver (thermal) noise, atmospheric noise, narrowband RFI, and wideband jamming signals.

The SWTDL matched filter processes the signal and produces a correlation peak. The information content of the signal is contained in the correlation peak (the correlation peak is a triangular-shaped pulse which rises above a lower rather continuous envelope (noise) signal).

These peaks are typically supplied to the Circulating Integration for further processing, but the processing gain contributions of the SWTDL is measured with the following technique. A sampler samples the correlation peak at its maximum point and the ratio of signal power to noise power in this sample is related to the input signal-to-noise ratio by the matched filter processing gain. The processing gain (PG) is defined as

$$PG = \frac{S_o}{P_n} \frac{N_o}{S_i T}$$

where S_o = sampled output signal power

P_n = sampled output noise power

N_o = input independent noise spectral density

S_i = input power

T = tap-to-tap time delay of the SWTDL matched filter.

In addition to the main correlation peak, the SWTDL matched filter also contains smaller peaks called sidelobes. In a communication system, a properly implemented sampler discriminates against these sidelobes because it only samples at the peak of the triangular-shaped correlation pulse. It is important to note that no signal-to-noise improvement (processing gain) is realized if the sampler is eliminated.

A perfect SWTDL matched filter, followed by an ideal (zero width) sampler, provides a signal-to-noise improvement equal to the number of taps (N) incorporated into the SWTDL. This is shown in the mathematical definition of a matched filter process which states

$$\frac{\text{Sampled Signal Power}}{\text{Sampled Noise Power}} = \frac{h(t) * h(-t)}{n(t) * h(-t)} = \frac{NTS_i}{N_o}$$

where: h(t) = input signal

h(-t) = ideal SWTDL impulse response, ie., the negative time argument of the signal

n(t) = noise

N = number of taps on SWTDL matched filter

T = tap-to-tap time delay of SWTDL matched filter

N_o = input noise power density

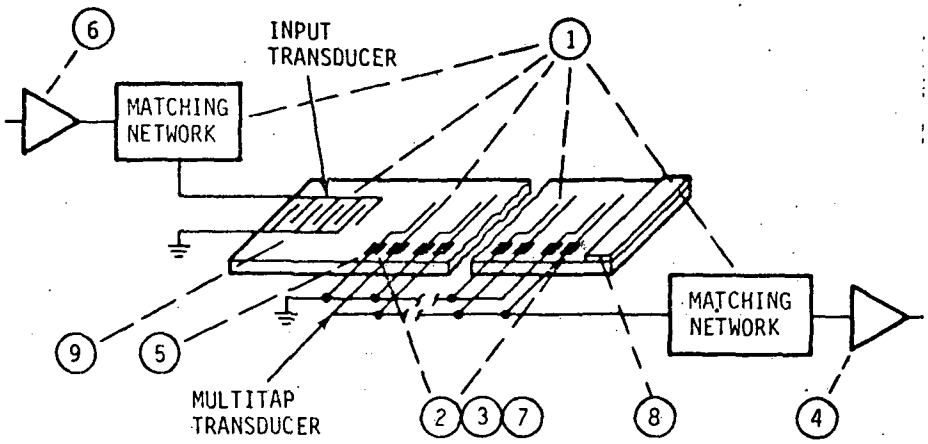
S_i = input signal power

$*$ = time convolution.

Since the input signal-to-noise ratio is $(S_i\ T/N_o)$, the theoretical processing gain is

$$PG = N$$

The processing gain of an actual SWTDL matched filter is less than the theoretical value if the height of the correlation peak (signal power) is diminished or if the noise level is increased by internal noise sources. The possible sources of processing gain deterioration in SWTDL's are depicted in Figure 4-6. The first three items in the illustration reduce the processing gain S/N improvement because the signal correlation



1 BAND LIMIT DISTORTION
2 TAP MISLOCATION
3 NON-UNIFORM TAP WEIGHTING
4 AMPLIFIER NOISE
5 DIRECT RF COUPLING
6 INTERMODULATION PRODUCTS
7 REGENERATED SURFACE WAVES
8 SW REFLECTIONS FROM ABSORBER
9 BULK MODE GENERATION

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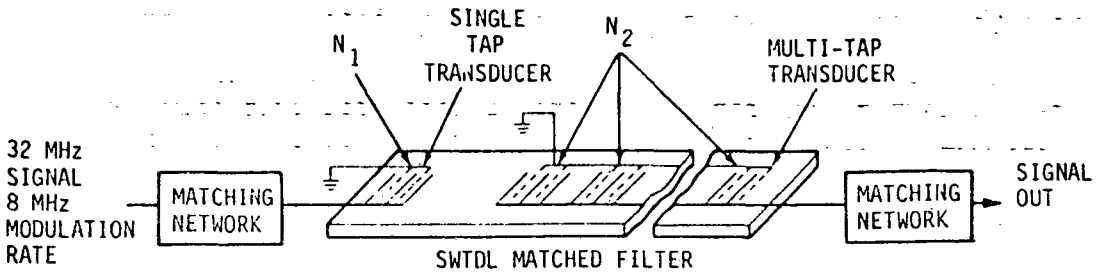
Figure 4-6. Sources of SWTDL Matched Filter Degradation

peak height is reduced. Excessive band limiting of the signal in matching networks and in the SWTDL interdigital transducers cause processing gain degradations by eliminating the sharp peak which results from high frequency components. The correlation peak height will also be diminished if the SWTDL matched filter impulse response is not precisely the negative time argument of the incoming signal. To provide a perfect impulse response, each tap must be precisely located on the SWTDL substrate. The SWTDL must also be precisely fabricated to have consistent gain (or insertion loss).

The last six items in the illustration represent noise contributed by the SWTDL which also reduces the effective processing gain. Typical SWTDL devices are designed with the objective of maintaining these noise levels at 10 to 15 dB below the processed interference level.

4.4.2 Transducer and Matching Network Bandwidth

Band limiting caused by the surface wave transducers and matching networks of both the SWTDL signal generator and matched filter reduces the processing gain. A SWTDL designed for the 32 MHz center frequency, 8-MHz bandwidth signal of the breadboard is shown in Figure 4-7. Nearly



— — —	BW MATCHING NETWORKS	NO. OF GRID PAIRS/TAP	
		N_1	N_2
CONF NO.1	∞	4	1
CONF NO.2	10 MHz	2.5	2.5

ASW-354-11

Figure 4-7. SWTDL Matched Filter

ideal SWTDL matched filters can be constructed by eliminating the matching network and using a four-interdigital-pair input transducer and a single-interdigital-pair per-tap output multi-tap transducer. The processing gain loss of such a SWTDL matched filter (Configuration No. 1) is plotted as a function of pretransmission bandwidth in Figure 4-8. It suffers less than 0.1 dB additional loss of processing gain for any pretransmission bandwidth. It should also be noted that the loss of processing gain shown in Figure 4-8 is over and above the processing gain loss from the pretransmission filter.

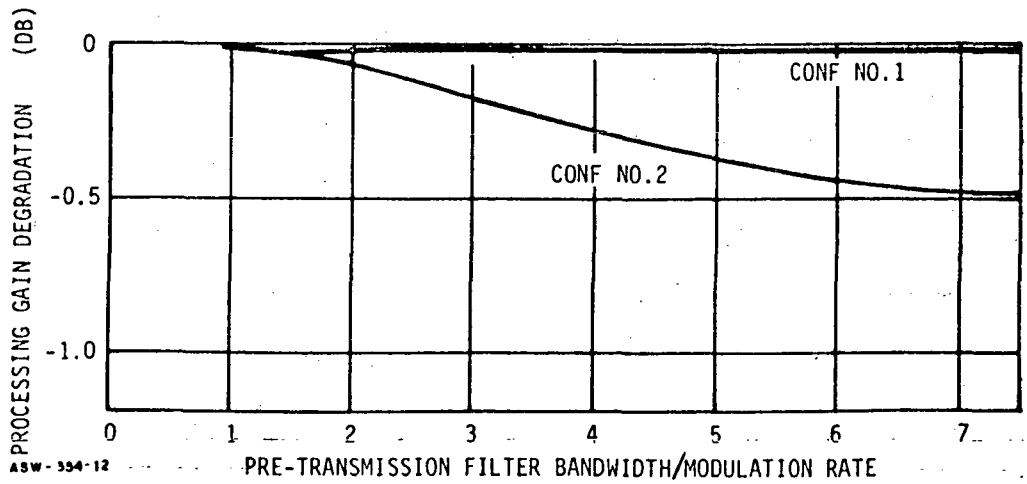


Figure 4-8. Processing Gain Degradation vs Transducer Bandwidth

Surface wave devices have an inherent insertion loss to bandwidth relationship which makes it desirable to operate them at a minimal bandwidth. The insertion loss of the Configuration No. 1 SWTDL is high because it uses wide bandwidth transducers and no matching networks. An extensive theoretical study was made to determine processing gain loss as a function of:

(a) Input matching network bandwidth

(b) Number of interdigital pairs in the input transducer

(c) Number of interdigital pairs per tap in the multi-tap transducer

(d) Output matching network bandwidth

(e) Insertion loss.

The study has shown that Configuration No. 2 is the best SWTDL design for use in conjunction with band-limited channels (pretransmission filter set at the modulation rate). The input transducer and each tap of the output transducer have 2½ interdigital pairs, and the matching networks are Q-spoiled to have a bandwidth of 10 MHz. The results plotted in Figure 4-8 show that this configuration is no worse than Configuration No. 1 if the pretransmission filter bandwidth is equal to the bit rate. With wider pretransmission filter bandwidths, however, correspondingly more loss is contributed to the band limiting in the transducers and matching networks.

4.4.3 SWTDL Fabrication Consistency

The processing gain provided by the matched filter receiver is degraded if the impulse response of the SWTDL signal generator is not precisely the negative time argument replica of that from the SWTDL matched filter. Differences in SWTDL impulse responses can result from uncontrolled fabrication tolerances because the location of taps on the substrate establishes the phase of the output signal. The taps can be located on the substrate in such a way that there is an RMS placement error of less than one micron. With the 32-MHz center frequency used in the breadboard, this represents an RMS phase jitter of less than 0.02 radian causes less than 0.1 dB loss in processing gain.

Another requirement for the SWTDL is that each of the corresponding taps in the signal generator and matched filter have the same insertion loss so that the impulse responses will have the same amplitude distributions. Experimental evidence shows that SWTDL's can be fabricated with a tap weight standard deviation of approximately 5 percent. Such deviations of amplitude will cause less than a 0.2 dB loss of processing gain.

4.4.4 Internal Noise Sources in SWTDL Matched Filters

The sum of all the internally-generated noise can be made to be 10 dB, or more, below the desired signal. Thus, internally-generated noise will introduce less than 0.1 dB of degradation in processing gain. The following paragraphs briefly describe the six primary noise contributors.

Amplifier Noise. - Because the surface wave device has 30 to 80 dB of insertion loss, care must be taken to assure that the output is always well above the thermal noise level of the output amplifier. If a 5 dB noise figure, 10-MHz bandwidth amplifier is used, the thermal noise is -99 dBm. Since the SWTDL matched filter output signals are typically greater than -70 dBm, the amplifier noise is negligible.

Direct RF Coupling. - Radiation of signals directly from the input transducer to the multi-tap transducer is another source of noise, but devices have been fabricated which have more than 90 dB of direct rf coupling attenuation. With a matched filter insertion loss of 50 dB, the output signal is 40 dB above the direct coupling noise and its effect is negligible.

Intermodulation Products. - The intermodulation products of the amplifier which drive the surface wave matched filter also produce a small amount of noise, but these are typically held to approximately 30 dB below the signal. Furthermore, this noise is suppressed by the processing gain of the matched filter, placing it at least 50 dB below the desired signal.

Regenerated Surface Waves. - When surface waves propagate under a multi-tap transducer, the voltage generated at each tap will cause new surface waves to be generated at each of the other taps. If strong coupling coefficient materials like lithium niobate are used, the regenerated waves from multitap SWTDL's may become significant. However, for ST-cut quartz, the coupling coefficient is sufficiently small so that the regenerated noise is at least 60 dB below the desired signal.

Surface Wave Reflections From the Absorber. - Surface waves propagating along a substrate are reflected when they encounter foreign materials on the surface. Such reflections are insignificant when acoustic absorbing materials are placed at the substrate edges so that the reflections are absorbed and scattered out of the region of the multi-tap transducer.

Bulk Mode Generation. - Surface wave transducers generate a small amount of bulk acoustic energy which introduces noise at the multi-tap transducers. However, the level of spurious noise from bulk modes can be made neglible with carefully designed transducers.

Temperature. - The primary performance degradation of SWTDL matched filters with temperature is caused by differences in temperature that may occur between the transmitter and receiver devices. As pointed out previously, the impulse response of a surface wave device depends on the spacing between conductors and the phase velocity of the surface waves propagating on the surface wave device. The overall negative change in SWTDL center frequency (or delay) as a function of temperature has been determined for a number of different materials some of which are summarized in Table 4-1.

TABLE 4-1. MATERIALS

Material	Cut	Propagation Direction	Delay Change in ppm/^{o}C
LiN_bO_3	X	Z	+93
Quartz	Rotated Z	X	-30
Quartz	ST	X	1
Quartz	Rotated Y	X	+18
PZT6	---	-	+6

The actual SWTDL processing gain loss as of a function of temperature has been calculated and verified experimentally. The processing gain loss is simply a function of the center frequency to delay time product and the delay time change in ppm. Therefore, it is desirable to use the minimum center frequency required to achieve the specified bandwidth.

The breadboard SWTDL's were fabricated using ST-cut Quartz which has the lowest known temperature coefficient of time delay. Figure 4-9 shows the processing gain loss in the SWTDL's as a result of temperature differences between the two ST-cut Quartz substrates. The breadboard devices have a time frequency product of 508; and as a result, the worst case processing gain degradation for a 50 degree centigrade temperature difference between the transmitter and receiver is less than 0.2 dB.

4.4.5 Doppler

The time scaling which results from the relative velocity between the transmitter and the receiver alters the characteristics of the signal so that the SWTDL and the Circulating Integrator no longer represent a perfect matched filter. The processing gain degradation resulting in the SWTDL as a function of doppler is plotted in Figure 4-10 for a family of different devices. The important parameter in determining the effect of doppler on SWTDL's is the time-frequency product. The devices

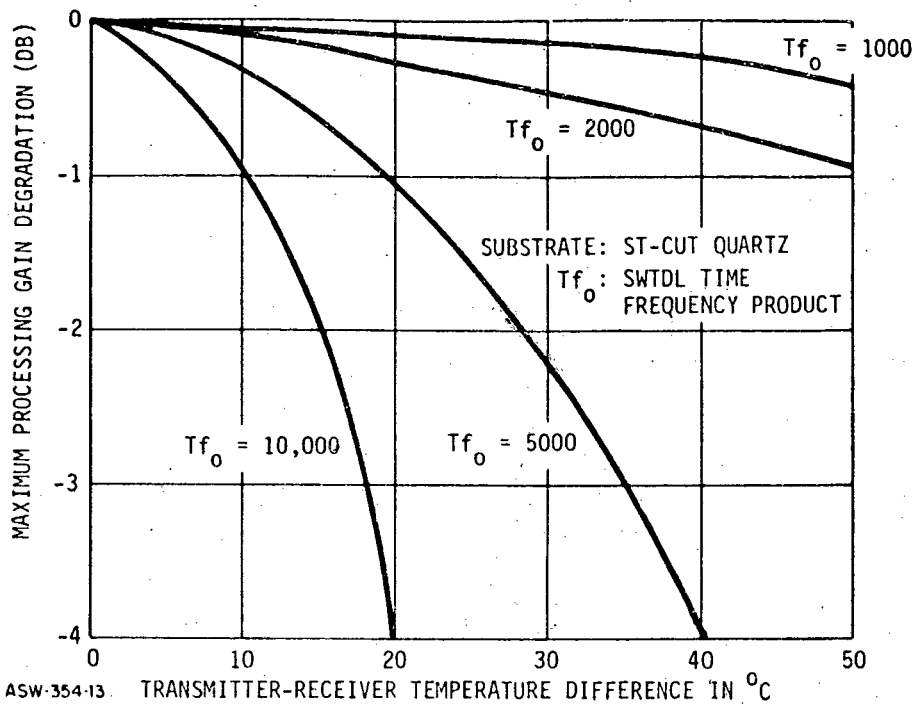


Figure 4-9. Processing Gain Degradation vs Temperature

used in the breadboard have a time-frequency product of 508 as shown in the graph. Even at twice the orbital velocity, the loss of processing gain in the SWTDL is negligible. The loss due to an uncompensated Circulating Integrator is determined from Figure 4-10 by using the bit time-center frequency product. The breadboard has a bit time of 125 μs and a center frequency of 32 MHz, resulting in a time-frequency product of 4000 and approximately a 1-dB degradation at the orbital velocity. This degradation is not necessary because the loss can be recovered by inserting a phase shifter in the loop and compensating for the time scaling. These degradations assume that the down-conversion oscillator is controlled by an AFC loop which holds the frequency offset, due to conversion error, to zero.

4.5 Circulating Integrator

The Circulating Integrator (CI) receives the correlation peaks from the SWTDL and sums them coherently to further improve the signal-to-noise ratio. It is a completely linear process performed in the rf domain before any demodulation takes place. The output is a series of rf correlation peaks similar to the SWTDL outputs except that they do not have a constant magnitude (see Figure 3-2 of Section 3.0). The increasing magnitude of the signal results because the delay of the Circulating Integrator is precisely adjusted so that each of the SWTDL output

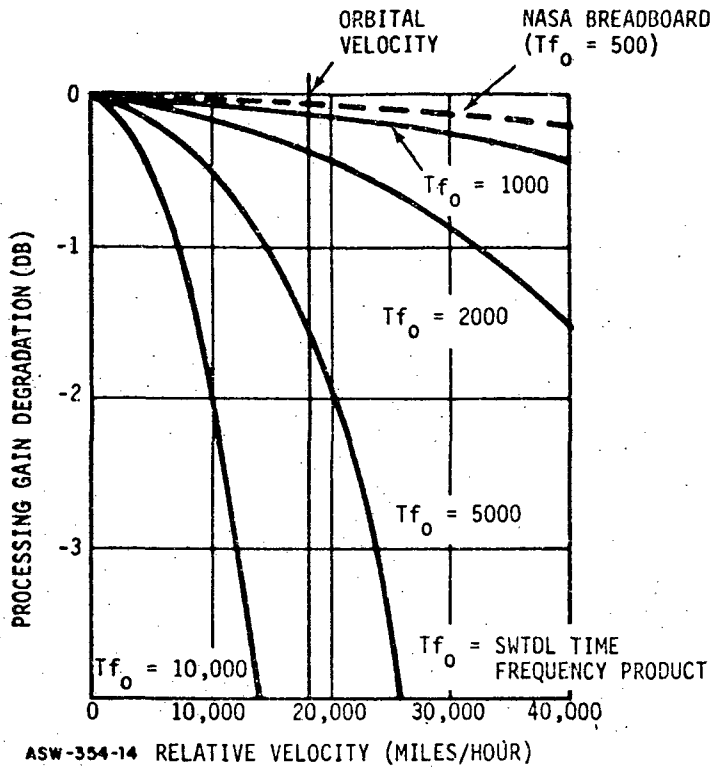


Figure 4-10. Processing Gain Degradation vs Doppler

correlation peaks is folded back and added coherently at the input. The signal is folded back (circulated) eight times; then, the delay line feedback path is opened for one circulation and the summation process is restarted. During the summation process the correlation peaks add coherently so that the final peak is eight times larger than the first; however, the noise adds incoherently and the rms noise voltage of the last circulation is only $\sqrt{8}$ times that of the first. This is the source of the CI processing gain. The theoretical signal-to-noise improvement for a perfect Circulating Integrator is equal to the number of circulations allowed before the feedback circuit is opened (in this case; eight circulations, or approximately eight dB).

The Circulating Integrator can be modeled as a perfect delay line followed by a filter representing the bandnarrowing contributed by the transducers and matching networks in conjunction with a feedback network and summer (see Figure 4-11). The full CI processing gain will not be realized if:

(a) The delay of the delay line is not correct

(b) The filter excessively narrows the spectrum of the correlation peaks

(c) The feedback network does not have well controlled loop gain (gain equals unity for the ideal case).

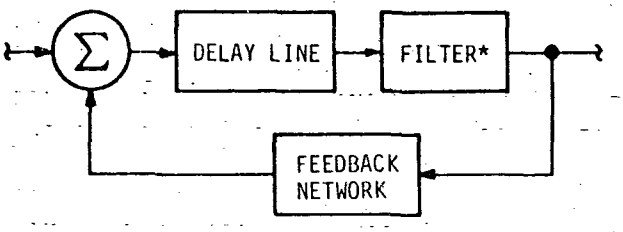


Figure 4-11. Circulating Integrator

The loss of processing gain due to delay line variations is plotted in Figure 4-12 with the center frequency to data bit rate ratio as a parameter. These curves are plotted assuming that the pulser has infinite stability and there is no doppler shift. If this is not the case, the degradations due to the pulser instabilities (see Figure 4-2) and doppler shift (see Figure 4-10) can be added to those due to delay line variations to get the worst case degradation. It is possible to place a wideband phase shifter in the feedback network to compensate for the delay time variations. This is accomplished by using a control system to sense the delay which provides the highest CI processing gain and by adjusting the phase shifter accordingly. This technique has the added advantage that it automatically compensates for doppler shift and long term pulser instability. Delay compensation was not required in the breadboard because the center frequency to data bit rate ratio is 4064 and the delay line delay varies less than 10 ppm over the laboratory temperature range.

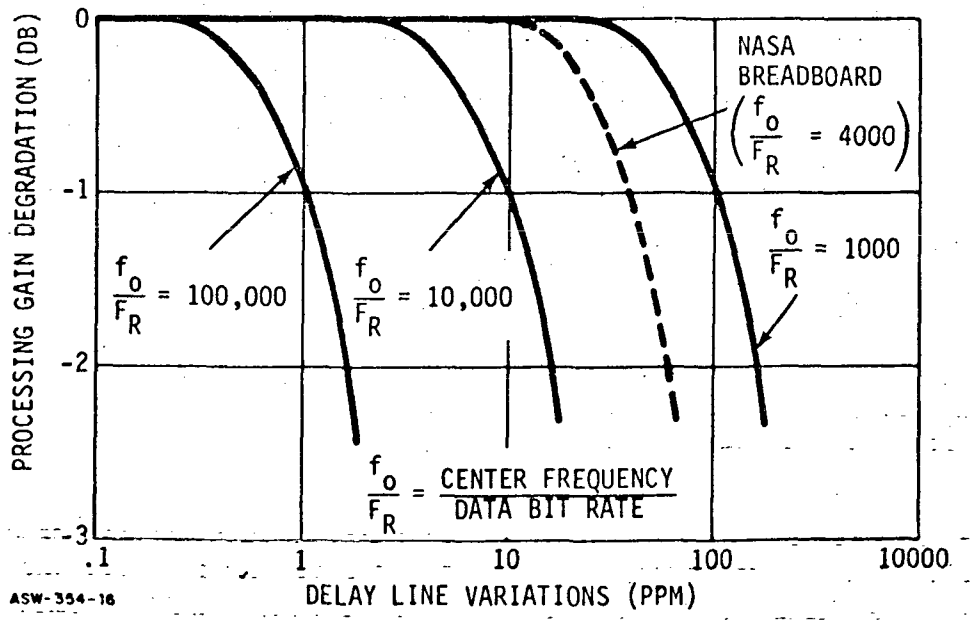


Figure 4-12. Processing Gain Degradation vs Delay Line Variations

Since the delay line used to implement the Circulating Integrator has transducers and matching networks with finite bandwidths, it will narrow the spectrum of the correlation peaks on each circulation. The delay line insertion loss is strongly dependent on the device bandwidth; i.e., if the insertion loss is made low, the bandwidth will be narrow. Therefore, it is important to use the correct delay line bandwidth because excessive insertion loss makes the feedback loop more difficult to implement and adds to the system additive noise. The loss of CI processing gain as a function transducer and matching network filter bandwidth is plotted in Figure 4-13. This curve was calculated for eight circulations using a numerical technique for a delay line with single pole matching networks having bandwidths equal to the transducer bandwidths. The spectrum of the correlation peak train received by the CI in the breadboard has a bandwidth of 7 MHz. (The bandwidth is narrowed below the original 8 MHz by the filtering of the pretransmission filter and the transducers in the SWTDL's.) The delay line used in the breadboard has a bandwidth of 8 MHz which results in a bandlimiting processing gain degradation of 0.4 dB.

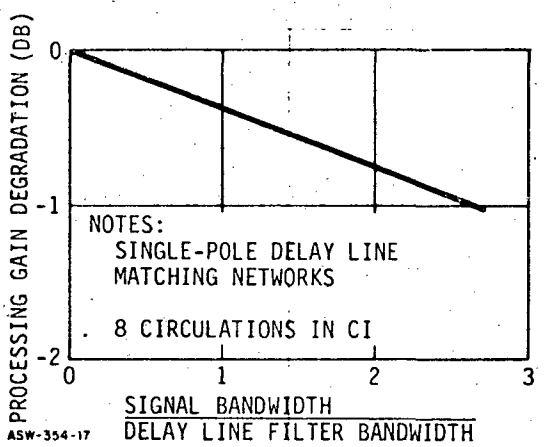


Figure 4-13. Processing Gain Degradation vs Dealy Line Filter BW

The gain of the feedback loop times the insertion loss of the delay constitutes the CI loop gain (see Appendix D). If the full CI processing gain is to be achieved, the loop gain has to be near one; because, a loop gain less than one will result in an attenuated signal while a loop gain greater than one will result in enhanced noise either of which reduces the processing gain. The processing gain degradation as a function of loop gain is plotted in Figure 4-14.

The breadboard has an adjustable loop gain provided for test purposes. If the loop gain is adjusted to within a range from 0.9 to 1.1, the degradation of processing gain to loop gain will be less than .3 dB.

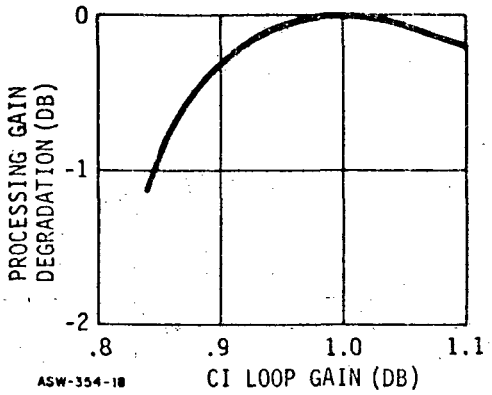


Figure 4-14. Processing Gain Degradation vs CI Loop Gain

4.6 Demodulator

The output of the CI is gated so that only the last and largest correlation peak is provided to the demodulator. Since the data information is contained in the phase of the rf carrier in the correlation peak, it must be demodulated for data recovery. The breadboard contains two demodulators: a carrier tracking coherent demodulator in the Coherent PSK mode and a delayed signal product detector in the double pulse mode. The Coherent PSK mode provides greater signal detection capability, and the Double Pulse mode is far more simple to implement. (A noise-compensated envelope detector is used as part of the 64-kHz PLL, see Appendix C.)

The essential components of the carrier tracking coherent demodulator are shown in Figure 4-15. The gated rf signal from the CI is squared to remove the phase shifts and tracked by a 64-MHz phase lock loop. The 64-MHz output from the phase locked loop is divided down to 32 MHz and multiplied by the gated CI output signal. The result is a series of baseband pulses which go positive or negative in conjunction with the rf polarity of the correlation peaks. If the phase locked loop provides a perfect jitter-free reference carrier, the signal-to-noise ratio of the signal will be improved by 3 dB as it passes through the demodulator. Since this is a linear process, the improvement is the same for all signal-to-noise ratios as shown in Figure 4-16. The signal-to-noise improvement of the coherent demodulator in the breadboard was measured to be 2.5 dB. The 0.5 dB deviation from theoretical is attributed to phase distortions in the output filter and to phase deviations between the regenerated carrier and the CI output signal.

The double pulse demodulator shown in Figure 4-17 is considerably simpler; it consists of an extra tap on the Circulating Integrator delay line, a balanced modulator, and a lowpass filter. The double pulse demodulator is a nonlinear element, and the processing gain degradation is

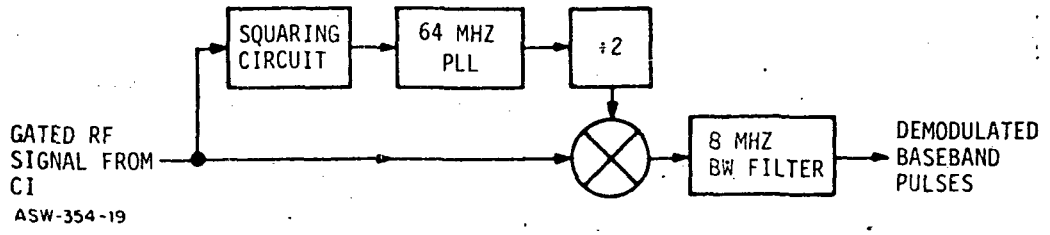


Figure 4-15. Coherent PSK Demodulator

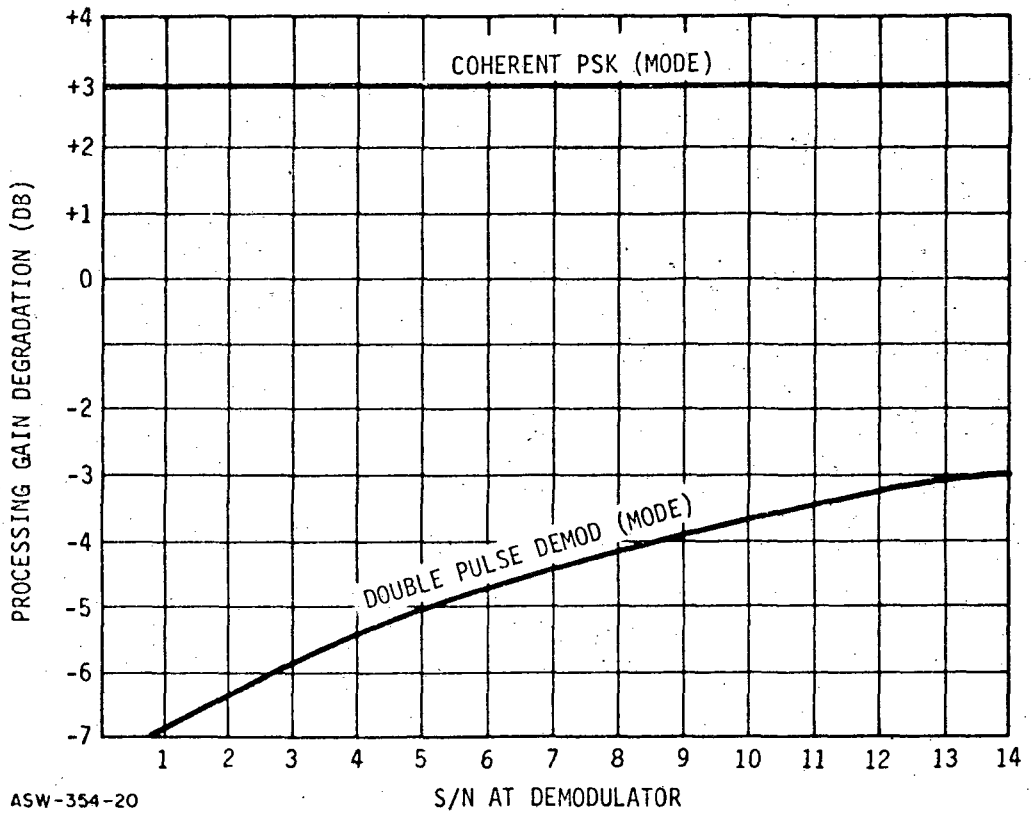


Figure 4-16. Processing Gain Degradation vs S/N at Demodulator

highly dependent on the input signal-to-noise ratio as shown in Figure 4-16. This curve is plotted for the case where the input noise has the same spectral shape as the signal and no post-demodulation filtering is used except to remove the second harmonic components. Since this demodulator is so simple, it is possible to realize the theoretical performance with less difficulty. At the high output signal-to-noise levels where the systems usually operate, the double pulse demodulator contributes 3 to 4 dB of processing gain degradation. It should be noted that the performance is 6 to 7 dB lower than the Coherent PSK demodulator. The

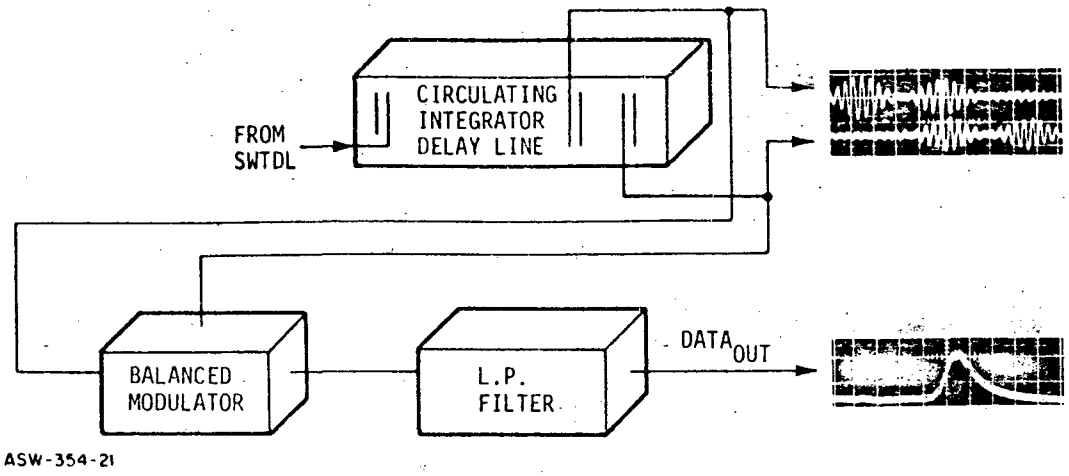


Figure 4-17. Double Pulse Demodulation

breadboard system operates about 5.5 dB better in the Coherent PSK mode than in the Double Pulse mode; the difference is 0.5 dB smaller than expected because the coherent demodulator output was 0.5 dB below theoretical.

4.7 Sampler

The SWTDL matched filter and Circulating Integrator provide processing gain only when the output is properly sampled.* The CI output is an amplitude-modulated rf signal which has a distinct maximum value. If a finite width pulse is used to sample the maximum value, the average sampled signal power will decrease with sampler width (especially if the output pulse is sharp). The average sampled noise power does not vary with sampling pulse width because the envelope of the noise out of the SWTDL is constant. Figure 4-18 shows the processing gain loss due to sampling pulse width for two system bandwidths. The first is for the very special case where the SWTDL has the conductor pattern of Configuration No. 1 of Figure 3-7; and the infinite bandwidth of pre-transmission filters, SWTDL transducers, and CI delay line transducers. In this case, the correlation peak is very sharp and the sampling pulse width is critical. The second case is Configuration No. 2 in Figure 3-7 with the bandwidths of all transducers and filters of the system set to the modulation rate. In this case, the correlation peaks have rounded tops and the sampling pulse width requirement is far less severe.

The sampling pulse width must be sufficiently wide to contain the maximum value of the matched filter output under the worst conditions of

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* The Schwartz inequality used in the derivation of matched filter performance is valid only for one point in time.

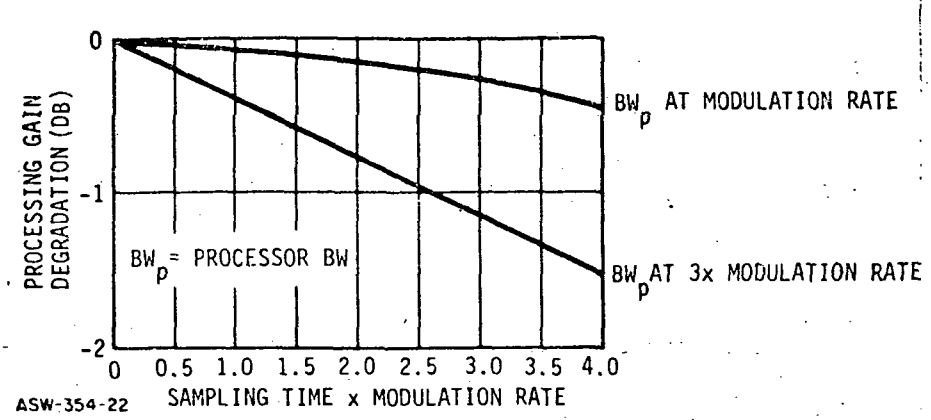


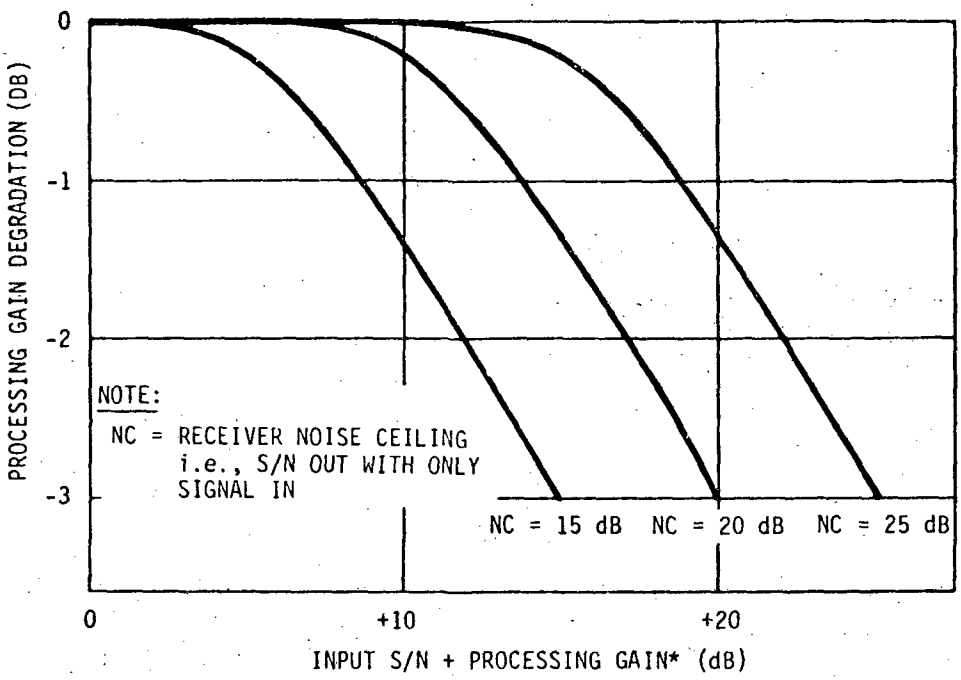
Figure 4-18. Processing Gain Degradation vs Sampling Width

sampler phase jitter. Since the sampler phase jitter of the breadboard is maintained below 10 ns, a 50-ns sampling pulse is used. With a 50-ns sampling pulse and the filters set to 8-MHz bandwidth for an 8-MHz modulation rate, the processing gain degradation is less than 0.1 dB.

4.8 Additive Noise

Noise added any place in the receiver will degrade the processing gain especially at high input signal-to-noise ratios. The noise ceiling of the receiver is defined as the output power from the sampler when only the signal only is applied to the receiver input and dividing that by the sampler output power when no input signal is applied. The receiver noise ceiling provides a basis for estimating the processing gain degradation due to additive noise as a function of input signal-to-noise ratio as shown in Figure 4-19.

The breadboard system has a measured noise ceiling of 26 dB and a processing gain which excludes the additive noise degradation of 31 dB. With a -13 dB input signal-to-noise ratio, the estimated degradation due to additive noise is -0.5 dB.



ASW-354-23 *NOT COUNTING DEGRADATION DUE TO ADDITIVE NOISE

Figure 4-19. Processing Gain Degradation vs System Noise

5.0 SYNCHRONIZATION ANALYSIS

5.1 System Concept

The operation of the Circulating Integrator requires that the receiver PN generator (see Figure 3-2, Section 3) be synchronized with the one in the transmitter. This synchronization is achieved by a search process similar to that used in most serial correlation receivers, except that the search time is decreased by a factor equal to the number of taps in the SWTDL matched filter.

The synchronization portion of the system is illustrated in Figure 5-1. Recognition of synchronization results from the signal out of the CI increasing in amplitude when the PN generator in the receiver is in synchronism with that of the transmitter and decreasing when it is not in synchronism (see Figure 5-2). Even before it is locked, the receiver PN generator operates at a clock rate very nearly equal to the rate of the transmitter PN generator, so that a preset PN generator phase relation is maintained until intentionally altered.

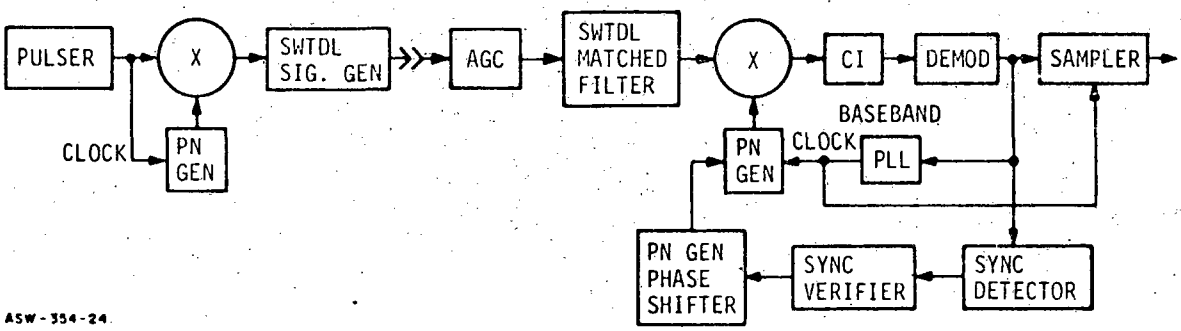


Figure 5-1. Breadboard Sync System

If the initial PN generator phase is not correct, the demodulated CI output will not be large enough to trigger the threshold in the sync detector, and the receiver PN generator will be advanced one state by the PN generator phase shifter (see Section 5.3). This process is repeated until the demodulated CI output exceeds the sync detector threshold. When this occurs, the PN generator is no longer advanced in phase, and the sync verifier is used to further test the synchronization decision. If the sync verifier determines that the synchronization decision was an error, the PN generator is again advanced in phase, and the sync detector continues to search for the synchronized state. When syncronization is verified by the sync verifier, the PN generator in the receiver is locked into phase with that in the transmitter via the baseband phase-lock-loop clock that tracks the pulser in the transmitter.

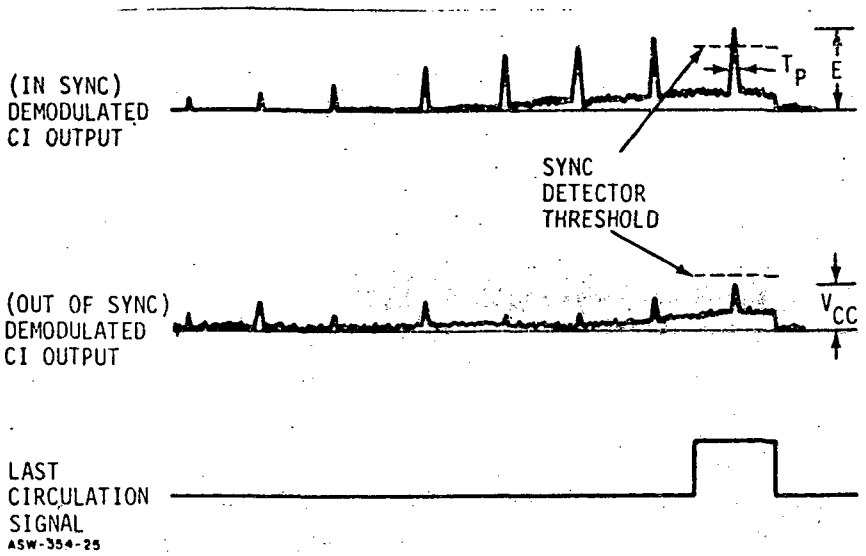


Figure 5-2. Out-of-Sync Circulating Integrator Output

The sync verification circuit increases the lockup reliability without significantly increasing the lockup time. The sync verifier circuit applies a far more stringent test to the CI demodulator output signal, and therefore provides a more reliable synchronization decision. The sync verification is a much slower process than the sync detection, but it is only used on the very few phase states where an initial synchronization decision has been made by the sync detector; and therefore, it does not add excessive time to the synchronization process.

When the phase of the PN generator is in the correct state, the output of the CI is a strong signal that contains the transmitted data. This data will not be read at the receiver output, however, until the baseband phase lock loop that drives the sampler is securely locked onto the demodulated Circulating Integrator output. Since, in the worst-case condition, the baseband phase-lock loop may not begin lockup until the receiver PN generator is in sync with that in the transmitter, the acquisition time of the baseband phase-lock loop must be added to the PN generator phase search time and the AGC setting time to get a total effective lockup time. This time, which depends on the input signal-to-noise ratio, the code length, the code cross-correlation characteristics, and the phase stepping rate can be estimated by the analysis presented in this section.

5.2 AGC

The AGC is an important part of the synchronization process, because it has a settling time and its performance affects the threshold levels in the sync detector. The level of the pulses out of the CI is directly related to the signal power applied to the SWTDL's. For example,

the height of the out-of-sync signal in Figure 5-2 could be higher than the in-sync signal if the signal power of the former were significantly greater. In addition, it is important to note that it is not the total power of signal-plus-noise that is important, but the power of the signal only. A conventional AGC that uses the envelope-detected total input signal plus noise as a reference is, therefore, not optimum because the output signal power will be twice as great with a -12 dB input S/N as it will be with a -15 dB input S/N.

Since such variations in signal power levels cannot be tolerated by the sync detector, the AGC shown in Appendix B was devised. It maintains the signal power level constant, within one dB, for all signal-to-noise ratios varying from minus 15 dB up. The AGC is adjusted to provide precisely the right signal power level at the lowest S/N under which operation is expected to be successful. The small signal power variations experienced at higher S/N will not degrade system operation, because the sync detector can tolerate 1 dB variations under those conditions. If system sync requirements are made more severe, so that the one dB variations cannot be tolerated, other techniques are available which reduce the AGC stability requirements at the expense of synchronizer complexity.

The synchronization process cannot proceed before the AGC has had a chance to stabilize. This settling time is a function of the circuit design and has been set at 8 ms in the breadboard. The details of the operation and performance of the breadboard AGC are described in Appendix B.

5.3 Sync Detection

The sync detector in the surface-wave matched-filter receiver operates differently from those in serial slide-by receivers because the signal has considerably different characteristics. The CI output signal is demodulated by an envelope detector and has the form shown in Figure 5-2. The circuit used to detect synchronization is shown in Figure 5-3.

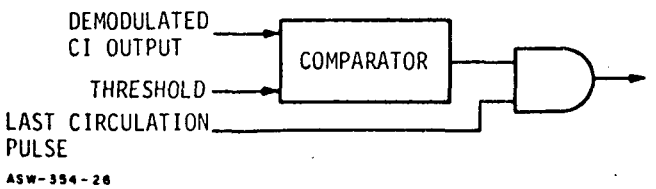


Figure 5-3. Sync Detector

When the receiver PN generator is in-sync, the demodulated CI output signal consists of a series of very narrow baseband pulses that grow continually larger during the eight circulations. At the base of these pulses is the envelope-detected Gaussian noise, resulting from communication channel noise. The separation between the pulses is equal to the pulse width times the number of taps in the SWTDL (in this case 127). When the PN generators are not in sync, the noise level at the base of the pulses remains unchanged, but the baseband pulses do not grow continually larger; and the last (eighth) pulse is considerably smaller than that in the in-sync condition. The last circulation signal, provided by the PN generator, encloses the eighth circulation pulse; and has a duration equal to the pulse-to-pulse separation.

The sync detector is designed to detect the difference in the height of the demodulated CI output signals between the in-sync and out-of-sync conditions. This circuit simply consists of a comparator and an AND gate. The threshold of the comparator is set at a level somewhere between the height of the eighth circulation pulse of the in-sync and out-of-sync conditions. The comparator output is passed by the AND circuit only during the last circulation so that any noise pulses occuring before the eighth circulation will not cause false sync signals.

When the CI output exceeds the threshold, the sync detector provides a logic-level signal to the sync verifier. The two standard measures of performance for sync detectors apply in this case; that is, probability of detection P_D (probability that an indication will be given when the phase is right) and false detection probability P_F (probability that a sync indication will be made when the phase is not correct).

It should be pointed out here that the decisions made by the sync detector are not as final as the terms probability of detection and probability of false detection may imply because the sync verifier passes judgement on the decisions before lock-up action is taken (see Section 5.4). All false sync errors made by the sync detector will be caught by the sync verifier because it continuously monitors the output signal during data transmission.

The relationship between the probability of detection and the probability of false detection, as a function of a signal-to-noise ratio, is shown in Figure 5-4. These curves, which are extensions of Marcums' original derivation of the probability of detection of envelope detected signals, takes into account the fact that the noise is observed for a much longer time than the signal*. The probability of detection is read directly from the figure**. However, the probability of false detection does not take into account the autocorrelation sidelobes of the PN generator code.

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* The false detection probability (P_F) is calculated from the equation shown in the figure, using the value of 'p' read from the graph.

** This assumes a PN generator code with perfect autocorrelation characteristics.

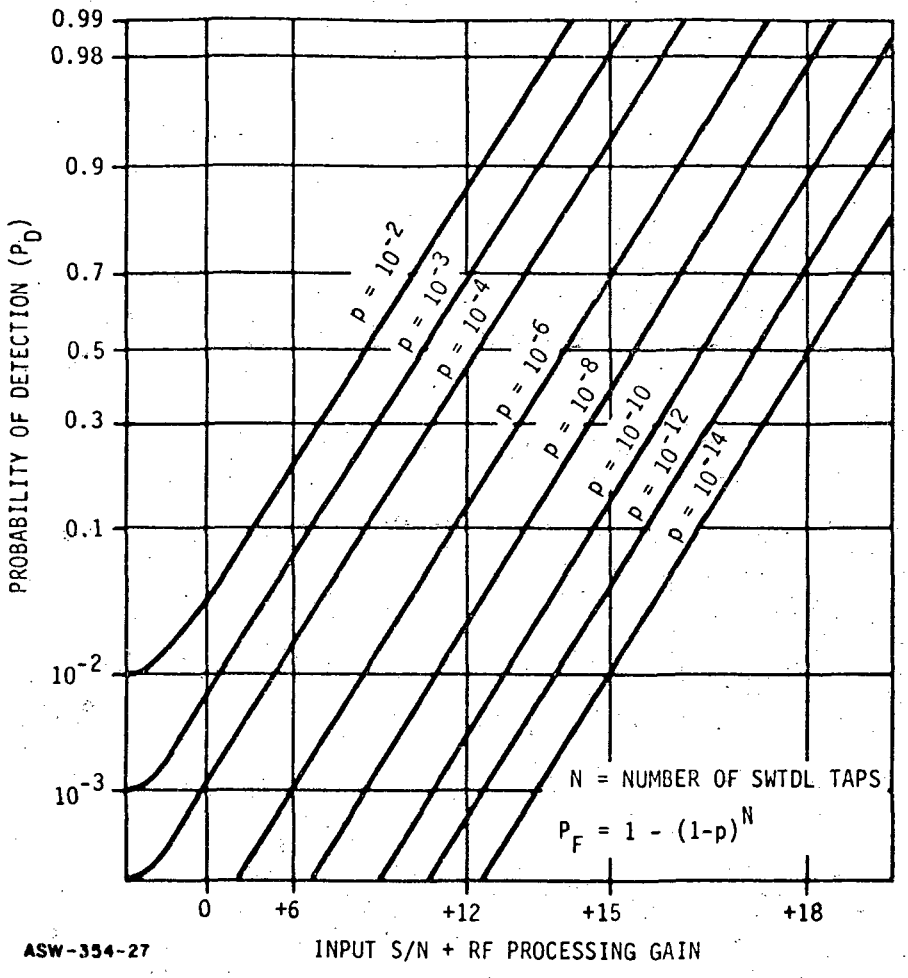

Figure 5-4. Probability of Detection (P_D) vs. Signal-to-Noise Ratio

The PN generator code autocorrelation sidelobes cause a finite CI output, over and above the noise, when the PN generator is out of sync (as shown in Figure 5-2). High autocorrelation sidelobes cause the false sync probability to increase. For example, if the autocorrelation level is zero (the output of the circulating integrator contains only noise), the probability of false detection is that read directly from Figure 5-4. If the autocorrelation sidelobes were as high as the synchronized signal output, the false detection probability for that state would increase to the level equal to the probability of detection in the in-sync signal.

The following procedure is used to determine the total false detection probability:

(1) Determine the autocorrelation sidelobe levels and their probability of occurrence

(2) Determine the probability of false detection with each sidelobe level

(3) Take the mean value of that probability and add it to the zero-signal false detection probability to get the worst-case value.

If the breadboard sync detector threshold is set for a probability of detection of 0.9 (with an input signal-to-noise ratio* equal to -13 dB) and the rf processing gain is greater than 26 dB, the probability of false sync at this signal-to-noise level is less than 0.2, discounting the effect of autocorrelation sidelobes. The autocorrelation sidelobe levels of the breadboard PN generator code, along with their probabilities of occurrence, are shown in Table 5-1. The probability that each sidelobe will trigger the sync detector (read from Figure 5-4) is also tabulated. The sum of the probability of occurrence, times the probability that each sidelobe will trigger the sync detector, represents the mean value of false detection probability contributed by the sidelobes. This value is 0.042, giving a total worst-case detection probability of 0.242 for the sync detector.

TABLE 5-1. PN GENERATOR CODE AUTOCORRELATION CHARACTERISTICS

Code 00101110		
Sidelobe Level (Relative to the Sync Level)	Probability* of Occurrence	Probability** of Causing False Sync at -13 dB input S/N
0.00	0.714	---
0.25	0.286	0.05
0.50	0.143	0.80

* Assumes random data transmission

** Probability of detection set at 0.9.

---

* Signal Power/N_o × Modulation Rate

5.4 Synchronization Verifier

The sync verifier is used to monitor the sync detector output and further test synchronization decisions. The technique of Figure 5-5 involves the use of a shift register and an OR gate to constantly monitor the output of the sync detector. If the sync detector threshold is exceeded, a '1' is placed in the register; whereas, if the threshold is not exceeded, a '0' is placed in the register. The data is advanced one step in the register each time the sync detector is polled. If any 1's exist in the register, the OR circuit does not call for a change in relative phase of the PN generator. When no 1's are held by the register, the OR circuit commands the PN generator phase shifter to advance the PN generator phase one-bit time. The probability that the PN generator will be advanced is a function of the register length, and the probability that the sync detector threshold will be exceeded is shown in Figure 5-6.

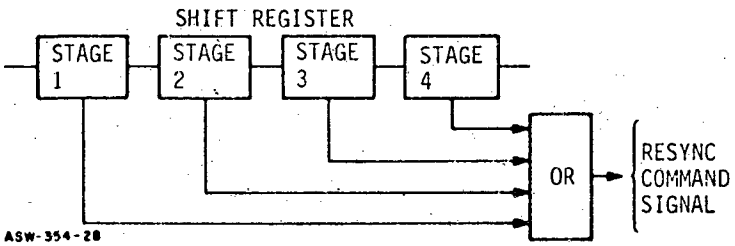

Figure 5-5. Sync Verifier

The operation of the breadboard sync verifier is determined from Figure 5-6, using the previously determined sync detector probabilities of detection and false detection. The probability of loss of sync (P_{LS}) is defined as the probability that the sync verifier restarts the search process when the system is in sync. If the sync detector probability of detection (P_D) is set at 0.9 for a -13 dB input S/N, the four-state sync verifier will have a loss of sync probabilty of 10^{-4}, as determined from Figure 5-6. It should be noted that this probability can be arbitrarily made small by increasing the number of registers used in the sync detector.

The probability of restarting the search when the system is not in sync is defined as the probability of false sync recognition (P_{FR}). Since the sync detector probability of false sync (P_F) is 0.242 for these conditions, the P_{FR} is 0.3; a ten-stage sync verifier would have a P_{FR} of 0.06. Note that the reduction of P_{LS} comes at the expense of P_{FR} probability.

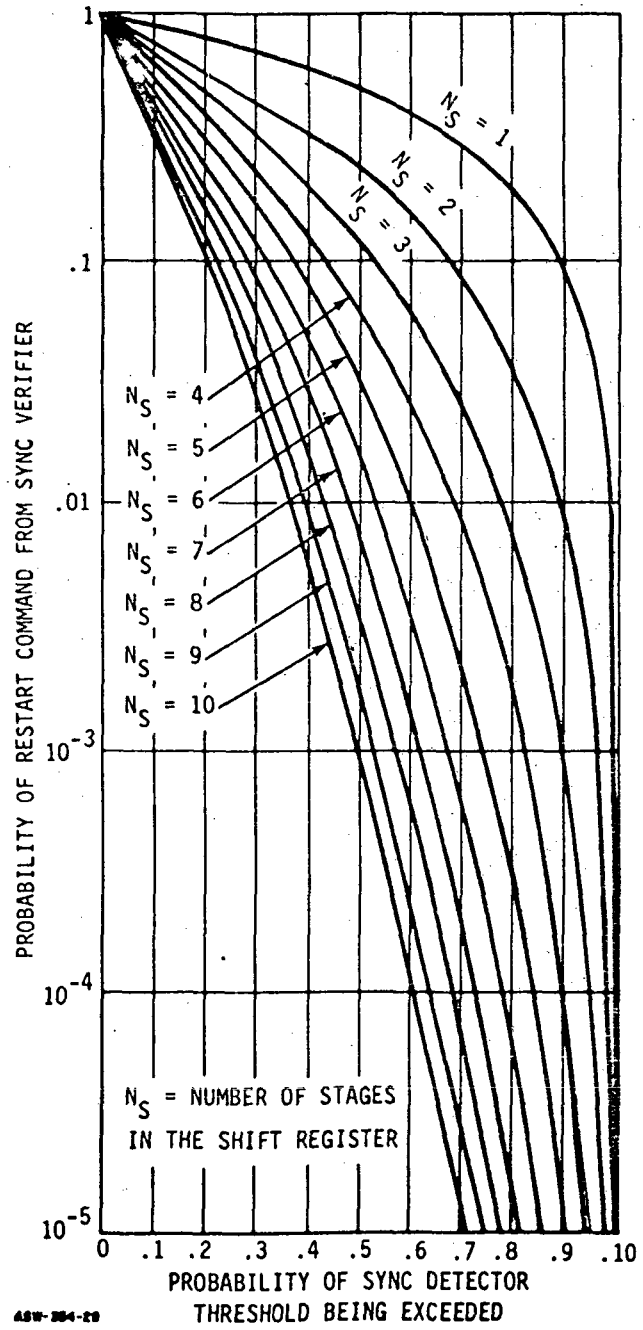

Figure 5-6. Sync Verifier Probability Curves

The sync detector and sync verifier circuits constantly monitor the signal while data is being transmitted; therefore, every false sync state will eventually be detected. The time required to detect a false sync state depends on the observation time (the time it takes to make a decision), and the probability of false sync rejection (P_{FR}). The observation time is equal to the number of shift register stages in the sync verifier, divided by the sync detector polling rate. The breadboard uses a four-stage shift register and an 8-kHz sync detector polling rate; the resulting observation time is 0.5 ms. With a probability of false sync rejection equal to 0.3, the mean number of observations required to reject the false sync state is 3.3, and the mean time required to reject it is 1.66 ms.

The sync verifier will also occasionally reject correct sync states as well, causing the system to momentarily lose lock. With a probability of loss of sync (P_{LS}) equal to 10^{-4}, the mean number of observations occurring before loss of sync is 10,000. Since observation time is 0.5 ms, the mean time between losses for sync is 5 seconds.

It should be noted that this time is increased greatly by increasing the number of registers in the sync verifier. For example, increasing the register length from four stages to five increases the mean time for loss of sync from 5 seconds to 50 seconds. In future systems, it may be desirable to use two to four stages of sync verifier shift register for lockup, and six to ten stage registers for monitoring sync during data transmission. Such a system would provide prompt rejection of false sync states during lockup and very long mean time for loss of sync during data transmission.

5.5 Sync Time Analysis

The probabilities calculated in the previous paragraphs can be used to determine the search time required to establish synchronization between the transmitter and receiver PN generators. This can be added to the measured AGC settling time, and the sampler lockup time, to determine the total time required after a signal is received until the data is accurately read. The technique for calculating this time is best described by the use of the breadboard system using the parameters in Table 5-2 as an example.

The search time depends on the inputs signal-to-noise ratio, the operation of the sync detector and sync verifier, and the length of PN generator code. If the sync detector threshold has been adjusted so that the probability of detection for an input signal-to-noise ratio of -13 dB is 0.9 for an observation time of 125 μs and the PN generator code length (C_N) is eight bits, the mean number of observations required to achieve sync (N_{OS}) is

$$N_{OS} = C_N \left(\frac{1}{P_D} - \frac{1}{2} \right)$$

which for the breadboard is 4.4. The total mean time to detect sync then becomes 0.55 ms using the 125 μs observation time. With the false detection probability equal to 0.24, as calculated in the last section, each sync detection requiring C_N observations will produce $P_F \cdot C_N$ false sync indications. In the case of these breadboard settings, about one false detection per search time can be expected.

The sync verifier with its four-stage register, is used to verify the correct sync detection and reject each of the false sync detections. As pointed out in the last section, the probability of false sync recognition (P_{FR}) of 0.3 leads to a mean time of 1.6 ms to reject a false sync state. Since only one false sync detection per search is expected, the average time required to reject all false sync states is 1.6 ms. This leads to a total mean search time of 2.15 ms and a total mean lockup time of 25.5 ms. The lockup times for other sync detector thresholds, and other numbers of sync verifier stages, can be calculated with the same procedure and yield modified parameters; that is, longer mean times to lose sync. The search time is directly related to the length of the PN generator code; however, doubling the code length does not double the lockup time, since search time is dominated by the AGC settling time and the sampler lockup time.

TABLE 5-2. BREADBOARD SYNC PARAMETERS

Nomenclature	Parameters*	Time
System		
SWTDL	127 taps	
PN Code length	8	
Sidelobe Level and Probability of Occurrence	0 and 0.714 .25 and 0.286 .5 and 0.143	
AGC Settling Time		8 ms
Sampler Acquisition Time		15 ms
Sync Detector		
Probability of Detection (P_D)	0.9	
False Detection Probability (D_F)	0.24	
Observation Time (T_s)	125 us	
Mean Number of Observations (N_{OS}) to Achieve Sync	4.4	
Mean Time to Detect Sync		.55 ms
Mean Number of False Syncs Per Search	1.0	
Sync Verifier		
Number of Register Stages	4	
Probability of False Sync Recognition (P_{FR})	0.3	
Mean False Sync Recognition Time (T_{FR})	1.6 ms	
Total False Sync Rejection Time		1.6 ms
Probability of Loss of Sync (P_{LS})	10^{-4}	
Mean Time to Lose Sync (T_{LS})	5 secs	
Mean Time to Lose Sync with an In-Sync Observation Mode	many hours	
Total Mean Search Time	---	2.15 ms
Total Mean Lockup Time	---	28 ms

* Estimated for an input S/N = -13 dB when the sync detection threshold is adjusted for a $P_D = 0.9$

6.0 BREADBOARD

6.1 Design Parameters

This breadboard system was constructed to investigate the performance of a digital 8-MHz bandwidth, 8K-bit data rate communication link implemented with surface wave tapped delay lines (SWTDL's). Refer to Table 6-1. The SWTDL's designed to be matched filters for the 8-MHz bandwidth, phase-shift-keyed PSK signals are the primary signal processors in the communication link. Since an 8-KHz data rate link using only a SWTDL's would require surface wave devices 50 cm long, the technique using a re-entry delay line as a circulating integrator has been devised. The breadboard system consists of a pulser, SWTDL, signal generator, pre-transmission filter in the transmitter. SWTDL matched filter, circulating integrator, demodulator, and sampler (see Figure 4-1) to perform the signal processing. In addition a synchronizer like that shown in Figure 5-1 is required to establish sync before the signal processing can begin. The synchronizer is discussed in Section 5.0.

6.1.1 Surface Wave Tapped Delay Lines

The SWTDL's are designed with 127 taps spaced at 125-ns intervals and interconnected so that the impulse response is a 32-MHz center frequency signal, phase shift keyed by a 127-chip linear maximal sequence code. This design is chosen because it results in a 7-cm surface wave device which is convenient to fabricate and install. With this design, the SWTDL provides 21.8 dB of processing gain leaving 8.2 dB for the Circulating Integrator (eight circulations). It is also convenient because codes of this length are easily derived.

The SWTDL is fabricated on an ST-cut Quartz substrate which has a temperature coefficient of time delay less than one ppm/degree centigrade. This material has very weak coupling coefficients; and as a result, the unmatched insertion loss of 80 dB is reduced to 59 dB by the use of active matching networks which have a bandwidth of 45 MHz.

6.1.2 Pulser, Transmitter Amplifiers, and Filters

Each time a SWTDL is pulsed, its output is a 15.875-μsec duration burst of spread spectrum signal; a continuous envelope signal can be generated by pulsing the SWTDL at a 64-KHz rate. The phase coherency of the output signal depends on the stability of the 64-KHz pulse rate pulser. The pulser used in this breadboard derives its time stability from a crystal oscillator and has a stability greater than 50 ppm over the laboratory temperature range. The pulser train is a series of 17-ns duration video pulses derives from fast logic gates. These narrow pulses are required so that the pulse train has a significant portion of spectral energy in the 32-MHz region. With this pulse width, about 6 percent of the spectrum falls in the 4-MHz bandwidth at 32 MHz so that the spectral compatibility of the pulser to the SWTDL's is -12 dB. The peak output level of the pulser is 10 volts; but when the duty cycle of the pulse

TABLE 6-1. BREADBOARD PARAMETERS

System	
Type Transmission	Digital
Type Modulation	PNPSK
Time Bandwidth Product	30 dB
Noise Ceiling	26 dB
Transmitter Output S/N	8.7 dB
SWTDL	
Substrate	ST-cut Quartz
Center Frequency	32 MHz
No. of Taps	127
Tap Separation	125 ns
Active Matching Network Gain	21 dB
Transducer BW	10 MHz
Insertion Loss (including active matching gain)	59 dB
Temperature Coef. of Time delay	1 ppm/^{o}C
Pulser	
Pulse Width	17 ns
Pulser Level	+10 volts
Pulser Peak Power	30 dB
Rate	64 KHz
Pulse Duty Cycle	30 dB
Stability	50 ppm
Spectral Compatibility to SWTDL	-12 dB
Pre-Transmission Filter	
Bandwidth	8.8 MHz
Insertion Loss	6 dB
Transmitter Amplifier	
NF	4.5 dB
Gain	30 dB
Output Level	-46 dBm
Circulating Integrator	
No. of Circulations	8
Delay Line BW	8 MHz
Temperature Coef. of Delay	1 ppm/^{o}C
Delay Line Insertion Loss	77 dB
Loop Gain	Adjustable
Demodulator	
Mode 1	Coherent PSK
Mode 2	Differential Product Detector
Sampler	
Rate	8 KHz
Pulse Width	80 ns
RMS Time Jitter at -13 dB Input S/N	10 ns
Sampler Lockup Time	15 ms
Synchronizer	
PN Generator Code Length	8 chips
ACC Settling Time	15 ms
Sync Detection Threshold	Adjustable
Sync Verifier Stages	4

train is taken into consideration, the rms power of the pulser is 0 dBm. With the -12 dB spectral compatibility factor and the 80 dB prematching network SWTDL insertion loss, the output of the SWTDL is -92 dBm, or 8.5 dB, above the -100.5 dBm noise floor of the active matching network* and the transmitter output signal-to-noise level is 8.7 dB. The active matching networks have a gain of 21 dB and the wideband amplifiers contribute another 31 dB to overcome the 6 dB loss of the pretransmission filter and provide a transmitter output power level of -46 dBm.

6.1.3 Circulating Integrator

The Circulating Integrator (CI) is designed to extend the effective integration time of the SWTDL and provides an additional 8.2 dB of signal-to-noise improvement. This requirement implies that the CI must coherently integrate eight SWTDL outputs. The integration is accomplished by adjusting the delay line delay to precisely 15.875 μsec (the period of the pulse train) and feeding back the eight SWTDL outputs with a loop gain near unity. The bandwidth of the delay line transducers is 8 MHz and the insertion loss is 77 dB. The amplifiers used to provide the CI feedback path have gain adjustments provided so that the loop gain can be varied for experimental purposes. The delay line is also made of ST-cut Quartz and has a temperature coefficient of time delay less than one ppm/degree centigrade.

6.1.4 Demodulator and Sampler

The breadboard incorporates two types of demodulators; a different one in each mode. The Coherent PSK mode utilizes a phase lock loop to provide a carrier regenerated from the CI output for coherent demodulation. In the Double Pulse mode, the transmitter sends a reference signal delayed with respect to the information signal. The receiver delays the information signal after it is processed by the SWTDL and the CI multiplies it by the processed reference signal to achieve the demodulated output.

Sampling is required in the breadboard as it is in any matched filter system. A 64-KHz square wave locked in phase with the demodulated CI output is used to provide the 8-KHz sampling pulse. The worst case sampler pulse width has been adjusted to 80 ns and the lockup time of the sampler phase lock loop has been measured to be 15 ms.

6.1.5 Synchronizer

The synchronizer is required to establish the correct phase between the 8-bit PN generator in the receiver and the transmitter. The synchronizer of AGC circuit, a sync detector, a sync verifier, and a PN

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* The active matching networks have a noise figure of 4.5 dB and the pretransmission filter limits the noise bandwidth of 8 MHz. The result is a noise floor of -100.5 dBm (-174-69-4.5=-100.5 dBm).

generator phase-advance circuit. The AGC circuit which sets the signal power must settle down before any synchronization search can take place. The AGC settling time for the breadboard is measured to be 8 ms. The sync detector is a threshold circuit which determines if the PN generators are in phase by measuring the level of the CI output. This threshold is adjustable and is usually set for probability of detection of correct sync of about 0.9.

The sync verifier is a four-stage register which observes the sync detector output to verify sync detector decisions.

6.2 Breadboard Performance Analysis

The performance of the breadboard is analyzed in Gaussian noise to determine its quality and to isolate areas where further improvement is desirable; the results are summarized in Table 6-2. The breadboard processes the 8-MHz bandwidth signal for a period of 125 μsecs for each data bit yielding a time bandwidth product of 1000, or 30 dB. A system with a time bandwidth product of 30 dB is capable of providing a signal-to-noise improvement on the rf PSK signal of 30 dB only if it operates perfectly and if the channel has no infinite bandwidth. In practical systems where the bandwidth of the signal must be limited before transmission by a pretransmission filter, the system has a lower fundamental processing gain. The breadboard system uses an 8.8-MHz bandwidth pretransmission filter which corresponds to a 0.5 dB (see Figure 4-4) reduction in fundamental processing gain; therefore, the maximum rf processing gain which one hope to achieve with this system is 29.5 dB.

The breadboard, like every real system, has practical limitations which do not allow it to provide perfect results. Considerable theoretical and experimental analysis have been performed on this system to isolate the sources of degradation and predict their effect on the breadboard operation. The analytical studies which have excellent agreement with the experimental results indicate that 30 dB processing gain systems, based on the concept of the breadboard, can be produced with processing gains approaching one dB of theoretical. The values summarized in Table 6-2 have, in a large part, been derived and calculated in Section 4.0; but the table is provided as an overview to create a better understanding of the breadboard characteristics.

A pulser stability of 50 ppm is sufficient so as not to contribute measureably to the system processing gain degradation as pointed out in Figure 4-2. However, the pulse level used in the breadboard is small enough that it does contribute 0.4 dB degradation in processing gain; because, the signal out of the SWTDL signal generator is only 8.7 dB above the output amplifier noise floor (see Figure 4-3). The 0.4 dB degradation can be reduced to less than 0.1 dB by improving the SWTDL driving circuits so that the output is at least 13 dB above the noise floor of the output amplifiers.

TABLE 6-2. BREADBOARD PERFORMANCE ANALYSIS

Breadboard	Estimated Degradation at -13 dB S/N (dB)	Performance Value
System		
Time Bandwidth Product	---	30.0 dB
Pretransmission Filters	0.5	---
Maximum Obtainable Processing Gain (PG)	---	29.5 dB
SWTDL Matched Filter		
Band Narrowing	-.1	---
Fabrication	-.3	---
Pulser		
Stability	0.0	---
Level	-0.5	---
CI		
Delay Line Variation	0.0	---
Band Narrowing	-0.4	---
Loop Gain Variation	-0.3	---
Demodulator		
Coherent PSK	+3.0	---
Double Pulse	-3.0	---
Sampler		
System Additive Noise	-0.5	---
Degradation		
Worst Case rf PG Degradation	-1.5	---
Coherent PSK Mode		
Calculated Worst Case PG	---	30.5 dB
Measured	---	31.2 dB
Double Pulse Mode		
Calculated Worst Case PG	---	25.2 dB
Measured	---	24.5 dB
Synchronization Time		
Calculated	---	28 ms
Measured	---	29 ms

The SWTDL matched filter works almost perfectly as demonstrated by analytical and experimental results. With the 10-MHz bandwidth transducers used on the 8-MHz bandwidth signal - which has been passed through an 8.8-MHz bandwidth pretransmission filter - the processing gain loss due to transducer band limiting is less than 0.1 dB (see Figure 4-8). Imperfection in the 127 taps of the multitap transducer contributes no more than 0.3 dB of degradation when the device has been fabricated with good techniques. The total processing gain of these SWTDL's has been measured to be 21.5 dB out of a possible 21.8 dB.

The Circulating Integrator contributes slightly more degradation than the SWTDL's because of the manner in which it operates. For example, the 8-MHz bandwidth transducers on the CI delay line contribute 0.4 dB of processing gain degradation because the signal is passed through them from one to eight times in the course of an operation (see Figure 4-13). The feedback loop involves the use of amplifiers which must have a gain stabilized with time and temperature. If the gain drift of the breadboard amplifier gain is adjusted to within plus or minus 10 percent, a processing gain degradation of 0.8 dB will be experienced in the worst case (see Figure 4-14). Both of these degradations can be further minimized in prototype systems by developing wider bandwidth delay lines and using automatically gain controlled amplifiers.

Each of the two modes of operation in the breadboard uses a different demodulator. The coherent demodulator in the breadboard increases the processing gain of the system by 2.7 to 3.0 dB while it is theoretically possible for it to provide a 3 dB improvement. The loss is attributed to a deviation in phase existing between the regenerated carrier and the CI output and to distortions contributed by the filter in the demodulator. The double pulse demodulator suffers a processing gain loss of about 3 dB. (see Figure 4-16). This difference in signal-to-noise performance from the coherent demodulator arises from the transmission of a reference signal and from the DPSK type demodulation process.

The sampler must sample the demodulated CI output, when it is at the maximum point, with a pulse significantly more narrow than the CI output. The 80-ns sampler pulse operating with less than 10-ns RMS time jitter provides a processing gain degradation less than 0.1 dB (see Figure 4-18).

One of the largest contributors to the breadboard processing gain degradation is the internally generated noise in the system. When only signal is provided to the breadboard, the output signal-to-noise ratio is +26 dB. As a result of this noise ceiling, an input signal with a signal-to-noise ratio of -13 dB will produce an output signal-to-noise ratio of +18 dB (see Figure 4-19) rather than an output signal-to-noise ratio of 17.5 dB as would be expected for 31.0 dB processing gain system. (The worst case processing gain of the breadboard is 31.0 dB when the contribution due to additive noise is not counted.) The measured processing gain of the breadboard as a function of input signal-to-noise

ratio is shown in Figure 6-1 along with the calculated worst case processing gain. Note how the processing gain increases with lower signal-to-noise ratios until the system breaks lock. The fact that much of the processing gain loss can be attributed to additional noise is an important result in that it shows that the performance of communication links based on this concept can be further improved over and above that of the breadboard by the use of only one mode, (incorporating two modes in the breadboard added much complexity, switching lines, etc.) wider dynamic range amplifiers, better shielded components, and lower noise elements such as balanced modulators and summers. It is anticipated that the noise ceiling can be increased to more than 30 dB, which represents a loss of processing gain of less than .1 dB for a -13 dB input signal-to-noise ratio.

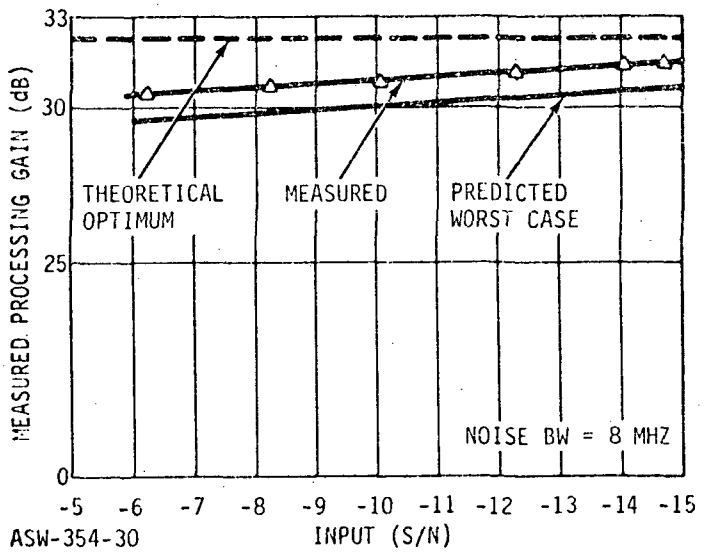

Figure 6-1. Processing Gain Vs Input S/N

The total calculated worst case processing gain of the breadboard (input S/N = -13 dB, coherent PSK mode) is determined to be 30.5 dB by summing the calculated degradations of each of the components. The breadboard processing gain was measured to be 31.2 dB. The processing gain of the breadboard in the double pulse mode is calculated to be 25.2 dB and the measured value is 24.5 dB.

The synchronization time including the AGC settling time, the search time, and the sampler lockup time was calculated in Section 5.0 to be 28 ms. The measured value is 29 ms.

6.3 Narrowband Radio Frequency Interference

When the input signal to the breadboard is mixed with narrowband RFI signal, the breadboard discriminates against that signal and provides an output with an improved signal-to-noise ratio. The amount of RFI suppression realized in the breadboard depends on the time-bandwidth product of the processor and the quality of its performance; but more importantly, it depends on the frequency of the interfering signal relative to the spectral characteristics of the desired signal. Since the time-bandwidth product and the quality of the breadboard performance is clearly indicated by the processing gain achieved in Gaussian noise, this is a good bench mark against which the performance in the narrowband RFI case can be compared.

Note the line structure of the transmitter signal spectrum as shown in Figure 6-2. This line structure arises from two sources; the finite length of the SWTDL code (127 chips) and the finite length of the PN generator code (8 chips). Since these codes are repeated, spectral lines arise at their repetition rate. The breadboard is a matched filter for this transmitted signal; and therefore - by definition of a matched filter ($H(\omega)=H(-\omega)$ - is made up of a series of passbands, each falling on a spectral line of the incoming signal. One would expect that the ratio of RFI rejection to Gaussian noise rejection would be highly dependent on interfering frequency, with some frequencies having little rejection and some with very much. The worst interference is 31.5438 MHz; and the breadboard has 21.5 dB rejection at this frequency which is 10 dB less than the Gaussian noise rejection.

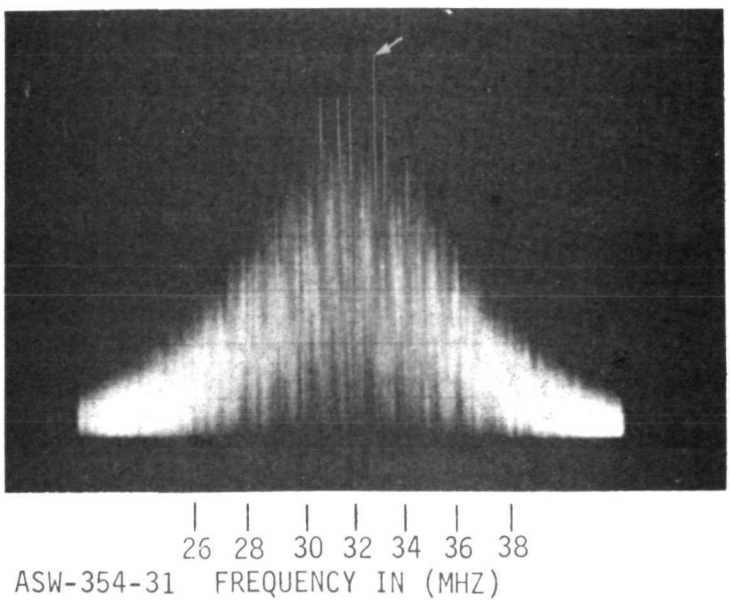

Figure 6-2. Spectrum of Breadboard Transmitted Signal (PSK Mode)

There are two ways in which the RFI rejection of a breadboard system can be significantly improved: designing the SWTDL impulse response to have less line structure and extending the length of the Circulating Integrator code to 64 bits or more. SWTDL's can be constructed with 3 dB less line structure by deviating from a straight PSK modulation. The codes for such SWTDL's are easy to generate and the processing gain for Gaussian noise will still approach the time bandwidth product; however, the signal will not be compatible with conventional signal processors. The RFI rejection is a direct function of PN generator code length. The present breadboard has an 8-bit code, but laboratory tests made with the breadboard for longer codes yielded the results in Figure 6-3. The dashed line shows the estimated rejection with modified SWTDL codes. As the code length increases, the RFI rejection increases until the code becomes long enough that its repetition rate spectral lines are smeared by the bandspreading of the data so as to be no longer distinct. These results indicate that systems using the Circulating Integrator concept can be made to have RFI rejection levels within those of Gaussian noise.

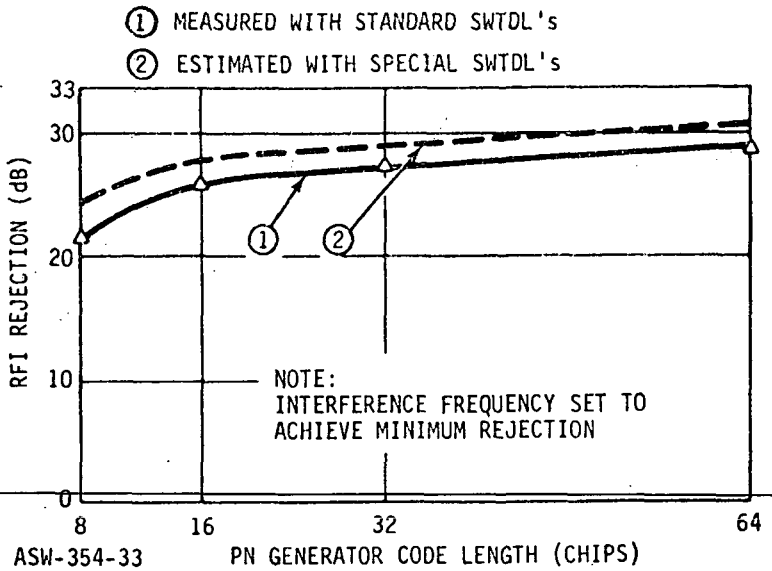

Figure 6-3. RFI Rejection Vs. PN Generator Code Length

6.4 Multiuser Noise

Multiuser noise is that interference which arises from other users operating in the same frequency band. The separation of the desired signal from the undesired signal is achieved on the basis of the codes used in the SWTDL. Appendix A shows the output of the SWTDL matched filters when a signal transmitted by a different SWTDL signal generator is received. If many users, all with different codes and repetition rates are

used, the central limit shows that the resultant interference approaches Gaussian noise. In this case, all the results pertaining to Gaussian noise will be quite accurate and 31 dB of multiuser noise rejection will be achieved. However, if the interference originates from only a few users, all of which have precisely the same repetition rate and are synchronous with the desired signal, multiuser noise rejection will not be as great. The breadboard was tested in such a worst case configuration by superimposing three powerful synchronous channels on top of the desired signal and measuring the output signal-to-noise ratio. With this worst case simulation, the breadboard provided 13 dB of multiuser rejection. To summarize, the multiuser noise rejection of the breadboard varies with the user characteristics and one can expect 13 dB or more in the worst case of synchronous users, and up to 31 dB in the more typical case where the signals are not synchronous.

6.5 Multipath

When a signal is reflected off a specular reflector and returned to the receiver, it is defined as a multipath signal. Multipath signals typically have characteristics nearly identical to those of direct signal, except the time of arrival is delayed. In the TDRS system, multipath signals with time-of-arrival delays of 0.2 to 10 ms are expected.[1] The breadboard was tested with multipath signals equal in amplitude to the desired signals and time-of-arrival delays in this range.

The following results were obtained:

(a) The system provided accurate data reproduction for all delays except those which were a precise multiple of the PN generator code duration.

(b) No provision was made to insure that the system did not read the data from the multipath signal; therefore, reading the data from the multipath signal results in range measurement errors.

(c) The processing gain of the system was not impaired more than 3 dB (the power of the reflected signal) by the presence of the multipath signal.

The failure to operate at delays which are multiples of the PN generator code duration is not a significant problem because the code can easily be increased to a sufficient length so that it is longer than the longest multipath time-of-arrival delay.

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[1] Multipath/Modulation Study Contract No. NAS5-10744 by J. N. Birch, The Magnavox Company, pp 24.

6.6 Size, Power, and Weight Estimates

The breadboard system has demonstrated that the surface wave wideband communication systems provide excellent performance worthy of implementation into future systems. It is, therefore, important to estimate the physical characteristics such as size, power consumption, and weight of such systems. The breadboard system cannot be looked upon as an example of the future configuration because it is a four channel link with two modes and all the intermode switching circuitry; in addition, it was intended to demonstrate the performance and not the actual configuration. Effort was not devoted towards achieving maximum simplicity, miniaturization, power conservation, or weight reduction. Table 6-3 is designed to help estimate the size weight and power consumption of fully developed surface wave links by breaking the system into various components. Estimates are made for the transmitter, Coherent PSK mode receiver, and the Double Pulse mode receiver.

The table does not take into consideration the transmitter and receiver front ends; ie, the power supply, the I.F., the frequency conversion, and the rf sections are not included in the table. The sectioning of the system is performed along the lines of Figure 4-1 in Section 4.0. The size, power, and weight for each section include only the components required to implement them. The printed circuit boards, enclosures, etc, are taken into account with an estimated packaging factor of five, ie, the hardware was assumed to be five times bigger and heavier then the components it supports.

These estimates demonstrate the compactness and simplicity of the surface communication system. The coherent PSK receiver which is by far the most complex of the three will occupy less than six cubic inches, weigh less than a pound, and consume less than one watt of power.

6.7 Extension to Other Bandwidths, Data Rates, and Processing Gains

The concept upon which this breadboard is based can be extended to data rates as low as 800 Hz, to signal bandwidths as wide as 100 MHz, and to processing gains of up to 40 dB. These limits can be further extended by the use of time compressors or digital matched filters in conjunction with the surface wave devices, but in many cases, the addition of these components results in excessive receiver complexity. As a result, the surface wave spread spectrum system provides the greatest advantage when the parameters are within the stated limits.

The maximum achievable effective surface wave propagation path length determines the minimum bit rate which can be received with this system. The breadboard receiver achieves the fast lockup and reduced synchronization complexity by storing the signal for a period equal to one bit time. The signal is stored in the SWTDL and the Circulating Integrator. The SWTDL, which presently stores 15.6-μs segments of signal, can be extended to store 80-μs segments and the Circulating Integrator, which presently stores eight SWTDL outputs, can be extended to store

TABLE 6-3. SURFACE WAVE SYSTEM SIZE, POWER, AND WEIGHT ESTIMATIONS

System Components	Transmitter			Coherent PSK Receiver			Double Pulse Receiver		
	Size (cm^3)	Power (mw)	Weight (gm)	Size (cm^3)	Power (mw)	Weight (gm)	Size (cm^3)	Power (mw)	Weight (gm)
Pulser	3.0	180	6	---	---	---	---	---	---
SWTDL	2.0	0	15	2.0	0	15	2.0	0	15.0
PN Generator and Mode Ckts	0.4	10	1	1.8	40	3.6	1.8	40	3.6
Amplifiers	0.6	100	2	1.8	240	3.0	2.4	360	4.0
Filters	.1	---	5	---	---	---	---	---	---
Circulating Integrator	---	---	---	2.0	0	15	2.0	0	15.0
Demodulator	---	---	---	6.0	480	15	2.0	---	2.6
Sampler	---	---	---	3.0	80	8.0	3.0	80	8.0
Data	---	---	---	0.4	40	1.5	0.4	40	1.2
Synchronizer	---	---	---	0.4	40	1.5	0.4	40	1.2
TOTALS	6.1	290	29	17.4	920	62.6	14.0	560	50.6
Hardware Packaging Factor	30.5	---	145	87.0	---	313.0	70.0	---	253.5
TOTAL	36.6	290	174	104.0	920	375.0	84.0	560	304.1

16. As a result, the total maximum signal storage is practically limited to 16 times 80 μs, or about 1.25 ms (a bit rate of 800 HZ). In time multiplexed systems where the signal is transmitted at a duty cycle of less then one, the data rates can be lowered by the fractional duty cycle (i.e., with a duty cycle of 1/4) and bit rates as low as 200 per second can be achieved.

The upper limits on signal bandwidths are set by the fabrication tolerances. Economical, high quality surface wave devices can be built to operate at 300 MHz with a 30 percent bandwidth so that an upper limit of signal bandwidth is about 100 MHz. The breadboard system does not have a limitation on the lower end of the signal bandwidth over and above the minimum bit rate specification. For example: the breadboard can be modified to process a 100-kHz bandwidth signal as long as the bit rate is maintained above 800 Hz.

There is one limitation to bit rates and signal bandwidths over and above those that have already been stated; for example, a system with a 1000-Hz bit rate and a 100-MHz bandwidth would have a processing gain of 53 dB, which is not practical. Processing gains greater than 40 dB will be obtained with great difficulty regardless of the bandwidth or bit rates.

7.0 CROSS-SYSTEM COMPARISON

The surface wave breadboard communication link development has laid the ground work on which cross-system comparisons can be made. The characteristics of a breadboard Double Pulse Mode, a breadboard Coherent PSK mode, a prototype coherent PSK system with some improvements over the breadboard, and a serial correlation receiver are summarized in Table 7-1. The four systems are compared on the basis of processing gain in Gaussian noise, rejection of narrowband RFI, phase ambiguity, synchronization search time, and system complexity. The processing gain and synchronization search time values for the breadboards are those determined theoretically and experimentally during the course of this development. The values projected for the prototype are estimates based on experience with the breadboard and assuming that the system noise has been reduced and the SWTDL and PN generator codes lengthened and modified for better RFI rejection as suggested in 6.0. The values for the serial correlation receiver are based upon extensive Magnavox experience with the type of receiver. In all cases, the complexity is stated qualitatively, instead of quanitatively, for a comparison is the primary objection of this section.

The surface wave designs offer a number of attractive features which make them candidates for a wide variety of applications including space communications where the following could apply:

(a) The surface wave systems using the Coherent PSK mode can be made to provide a signal-to-noise improvement as good or better than the serial correlation receivers with comparable complexity.

(b) All surface wave receivers reduce the synchronization search time by a factor equal to the number of taps in the SWTDL.

(c) The Double Pulse Mode system is far more simple than the other matched filter receivers, but does not perform as well. It will be particularly useful in applications where fast lockup and system simplicity is more of a premium than receiver sensitivity.

(d) The Double Pulse mode of operation has no phase ambiguity and can be used with straight PSK rather than DPSK data modulation.

(e) The RFI rejection of the breadboard receiver operating in either mode is not as good as that of the serial correlation receivers; however, the prototype surface wave system RFI performance is expected to be made comparable by using special coding on the SWTDL's and longer codes in the Circulating Integrator (refer to Section 6.0).

TABLE 7-1. CROSS-SYSTEM COMPARISONS

— — —	Double Pulse Mode Breadboard	Coherent PSK Mode Breadboard	Coherent PSK Mode Projected Prototype	Serial Correlation Receivers
Gaussian Noise Performance Factor	7 to 8 dB	1 to 2 dB	.5 to 1.5 dB	2 to 3
RFI Performance Factor	11 to 14 dB	8 to 11 dB	2 to 3 dB	2 to 3
Unambiguous Phase	Yes	No	No	No
Synchronization Search Time	T_{ss}/N_T	T_{ss}/N_T	T_{ss}/N_T	T_{ss}
Complexity	Very simple	Moderate	Moderate	Moderate

where:

N_T = number of taps in SWTDL's

$$T_{ss} = \frac{\text{code time bandwidth product}}{\text{data rate}}$$

$$\text{Performance Factor} = \left(\frac{\text{actual rejection}}{\text{time bandwidth product}} \right) \times 2$$

8.0 BREADBOARD DOCUMENTATION

8.1 Introduction

The Magnavox Spread Spectrum Communication Link is a 4-channel, 2-mode surface wave transceiver designed to operate in low S/N, RFI, multiuser, and multipath environments. The breadboard system consists of three separate units; a transmitter, a receiver (rf section), and a signal processor (or controller). Together the receiver rf section and the processor form the spread spectrum receiver. With the addition of laboratory power supplies, the units are fully operational.

8.2 Breadboard System Operation and Description

The breadboard system operates in an 8-MHz rf spectrum (centered at 32 MHZ) and will handle the transmission and recovery of binary data rates up to 8 KHZ. Clock is provided at both the transmitter and signal processor for synchronously transferring data into, and from, external binary registers. Note that low receiver bit error rates (in each mode) are achievable only when the indicator light for that mode is illuminated.

8.2.1 Front and Rear Panel Description

Figures 8-1, 8-2, and 8-3 show the front and rear panel controls, connectors, and test points for each of the three major units. A brief description of each panel item is listed and indexed to the figures.

8.2.2 System Interconnections

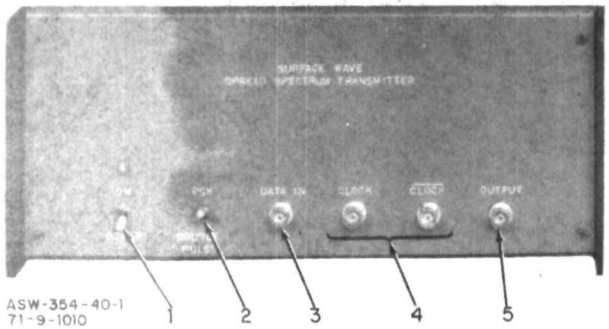
Table 8-1 is a tabulation of all required interconnections of the three breadboard units along with individual power supply connections. To obtain system performance within the breadboard's electrical specifications, the table should be closely followed. Further information on the initial setup interconnections appears in the acceptance test procedure.

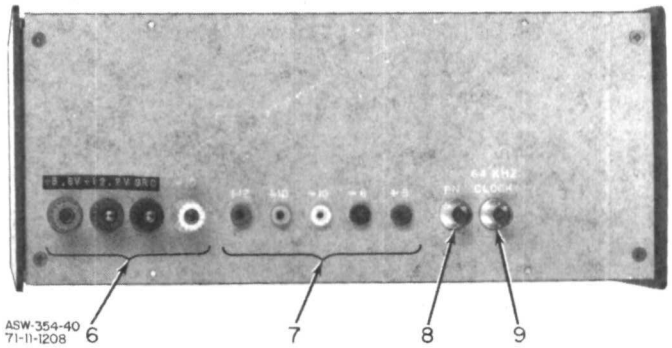
8.2.3 Operating Instructions

Turn-On and Warm-up. - Before applying DC power to the breadboard, turn adjustment pot R6 (CI Loop Gain Adj) on the rear panel of the receiver section to position 1. Allow the transmitter and receiver section to warm-up for approximately 1 to 2 minutes before turning the signal processor on.

With power on all three units, a digital voltmeter (or equivalent) should be used to set all DC power supply voltages to their specified value at the rear panel test point. Since many of the threshold circuits internal to the breadboard depend on these supply voltages, it is important, for the best system performance, that these voltages be set as accurately as possible.

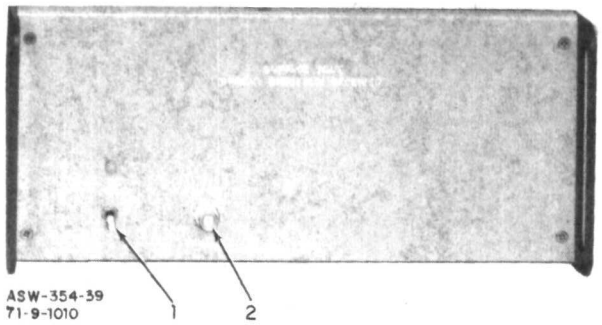
Allow the equipment to warm-up for at least 15 minutes before using.

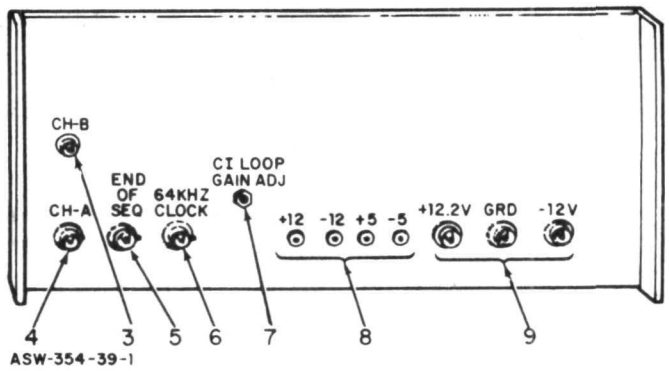




1. POWER ON/OFF SWITCH TO PULSER MODULE
2. MODE OF OPERATION SWITCH
3. BINARY DATA INPUT (COMPATIBLE WITH TTL AND DTL LOGIC)
4. CLOCK AND CLOCK INVERSE OUTPUTS FOR SYNCHRONOUSLY ENTERING DATA TO THE SYSTEM
5. SPREAD SPECTRUM OUTPUT SIGNAL (50Ω IMPEDANCE, 32-MHZ C.F., -46 dBm SIGNAL LEVEL, 8.7 MHZ BANDWIDTH)
6. POWER SUPPLY BINDING POST CONNECTION TERMINALS (THREE VOLTAGES REQUIRED)
7. VOLTAGE TEST POINTS AT SUBASSEMBLY MODULES
8. 8-BIT PN CODE TEST POINT (BNC CONN.)
9. 64-KHZ CRYSTAL OSCILLATOR TEST POINT (5 VOLT SQUARE WAVE)

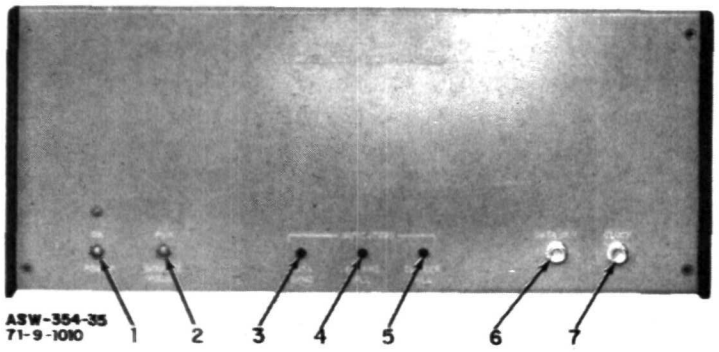
Figure 8-1. Transmitter Front and Rear Panels

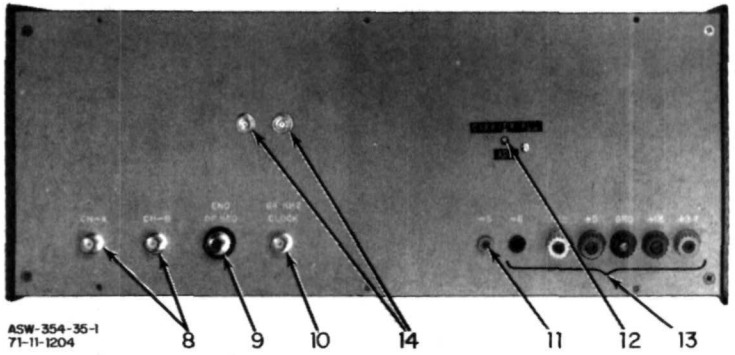




1. POWER ON/OFF SWITCH FOR RECEIVER
2. SPREAD SPECTRUM RF SIGNAL IN (BNC CONNECTOR)
3. CIRCULATING INTEGRATOR CH.-B RF OUTPUT (BNC CONNECTOR)
4. CIRCULATING INTEGRATOR CH.-A RF OUTPUT (BNC CONNECTOR)
5. END OF SEQUENCE BINARY OUTPUT OF 8 BIT PN CODE (BNC CONNECTOR)
6. 64-KHZ CLOCK INPUT FROM PROCESSOR (BNC CONNECTOR)
7. GAIN ADJUST OF CIRCULATING INTEGRATOR FEEDBACK LOOP (TRIM POT)
8. INTERNAL SUPPLY VOLTAGE TEST POINTS
9. POWER SUPPLY BINDING POST TERMINALS (TWO VOLTAGES REQUIRED)

Figure 8-2. Receiver Front and Rear Panels





1. POWER ON/OFF SWITCH FOR PROCESSOR
2. MODE SELECT SWITCH AT PROCESSOR
3. LIGHT INDICATING RECEIVER PN GENERATOR IS LOCKED TO THE TRANSMITTER
4. LIGHT INDICATING BASEBAND PLL IS LOCKED TO CORRELATION PEAK REPETITION RATE (64 KHZ)
5. LIGHT INDICATING CARRIER IS PHASE LOCKED TO CORRELATION RF SIGNAL IN PSK MODE
6. RECOVERED BINARY DATA OUTPUT FROM TRANSMITTER (BNC CONNECTOR)
7. 8 KHZ,5V CLOCK OUTPUT (FOR SYNCHRONOUSLY CLOCKING RECOVERED BINARY DATA TO OUTPUT EQUIPMENT)
8. CIRCULATING INTEGRATOR INPUTS FROM RECEIVER (BNC CONNECTORS)
9. END OF SEQUENCE BINARY SIGNAL INPUT (BNC CONNECTOR)
10. 64-KHZ VCXO BINARY OUTPUT TO RECEIVER (BNC CONNECTOR)
11. INTERNAL SUPPLY VOLTAGE TEST POINTS
12. ERROR VOLTAGE ADJUSTMENT ON CARRIER PLL (TRIM POT)
13. POWER SUPPLY BINDING POST CONNECTION TERMINALS (4 VOLTAGES REQUIRED)
14. DEMODULATOR OUTPUT (BOTH MODES)

Figure 8-3. Signal Processor Front and Rear Panels

TABLE 8-1. SYSTEM INTERCONNECTIONS (SIGNAL AND POWER)

Connections		Remarks
From	To	
Surface Wave Transmitter		
+12.2 VDC Terminal	Power Supply	(1) Use twisted pairs of hook-up wire for best results
+5.8 VDC Terminal	Power Supply	
-10.0 VDC Terminal	Power Supply	
Output (Front Panel)	Adjustable Attenuator	(2) 50 Ω Coax; set attenuator to 15 dB for a spread-spectrum signal level at the receiver input of approximately -60 dBm
		(3) Power Requirements: +12.2V ⟶ 90 ma, -10V ⟶ 45 ma, and +5.8V ⟶ .5A
Surface Wave Receiver		
+12.2 VDC Terminal	Power Supply	(4) Twisted pair of hook-up wire
-12 VDC Terminal	Power Supply	
RF In (Front Panel)	Adjustable Attenuator	(5) 50 Ω Coax (See Remark (2) above)
Ch-B (Rear Panel)	Ch-B at Processor	(6) 50 Ω Coax
Ch-A (Rear Panel)	Ch-A at Processor	(7) 50 Ω Coax (Must be identical in type and length as coax cable used in remark (4)
End of Sequence (Rear Panel)	End of Sequence Connector at Processor	(8) 50 Ω Coax
Clock (Rear Panel)	64-kHz Clock at Processor	(9) 50 Ω Coax
Signal Processor (Controller)		
+12.2 VDC Terminal		(10) Twisted pairs of hook-up wire
-12 VDC Terminal		
+5.8 VDC Terminal	Power Supply	
+24 VDC Terminal		
-6 VDC Terminal		
Ch-A (Rear Panel)	Ch-A at Receiver	(11) See Remarks (6) to (8)
Ch-B (Rear Panel)	Ch-B at Receiver	
End of Seq. (Rear Panel)	End of Seq. at Receiver	(12) Total Power Requirements for receiver and controller: +12.2V⟶ 1.15A, -12V⟶.3A, +5.8V⟶.5A, -6V⟶.3A, and +24V⟶ 100 ma
64 kHz Clock (Rear Panel)	Clock at Receiver	

Initial Alignment. - At the end of the warm-up period, one initial alignment must be made prior to operation. Switch the transmitter and signal processor to the PSK mode. Connect the "gated demod" out at the signal processor rear panel through 50 Ω coax to an oscilloscope. Terminate the coax in 50 Ω at the oscilloscope. Adjust the amplitude of the eighth pulse to 140 mV peak by using the CI loop gain adjust R6 (item 7, Figure 8-1). Observe that the three indicator lights are on. This gated demod pulse amplitude should be checked periodically; room temperature variations will cause the amplitude to vary. The breadboard system is now ready for operation.

Input/Output Interface. - Table 8-2 is a input/output interface listing showing the input and output connections of external equipment to the breadboard system and the interface requirements. The system was designed to handle binary data and is compatible with all DTL and TTL logic elements. For use in modem applications, optional rf input and output interface requirements are also listed.

Mode Selection. - The breadboard is capable of operation in either a Coherent PSK mode or a Double Pulse (differential) mode. The mode switches at the transmitter and signal processor will actuate this mode change. (Note that the amplitude of the gated demod may vary slightly between modes. However, adjustment of R6 should continue to be made in the PSK mode.)

In the PSK mode, all three indicator lights must be illuminated for proper system operation. At very low S/N ratios at the receiver input or at high level RFI, these lights will flicker or go out. Severe degradation in received bit error rate occurs under this situation. For low bit error rates on the recovered data at proper operations, these lights must be constantly illuminated.

In the Double Pulse mode, the carrier light should extinguish while the data sync and 64-kHz PLL lights remain illuminated for proper operation.

Channel Selection. - The code multiplexing scheme used by the breadboard allows the system to be used in any of four channels. To perform the channel change, the top lids on both the transmitter and receiver modules must be removed to expose the surface wave devices as seen in Figure 8-35 and 8-36. The surface wave devices (corresponding to the desired channel) are activated by plugging the unit into the pulser (at the transmitter) and by connecting the three coax cables (at the receiver).

CAUTION

Power must be OFF at both the transmitter and receiver during the channel change!

8.3 Electrical and Mechanical Description

The following paragraphs describe the major units, and their subassemblies, in the breadboard system. Figures and tables are used to illustrate the signal flow, location of components, characteristics, etc.

8.3.1 Transmitter

The block diagram shown in Figure 8-4 shows the major circuit functions comprising the surface wave spread spectrum transmitter. It illustrates the basic principles of operation.

A crystal clock oscillator establishes the signal timing for all operation in the transmitter. The 64-kHz clock operates a PN generator which generates both an 8-bit PN sequence and a data clock for synchronously loading external binary data. These signals along with the input data are applied to the pulser assembly which scrambles the incoming baseband data and generates the appropriate pulse polarity for exciting the SWTDL.

The channel selection is dependent on the SWTDL being actuated by the pulser assembly. The output of the SWTDL is the coded spread spectrum signal which is amplified, filtered, and applied to the output connector on the front panel. This signal level is -46 dBm based on a 50 Ω system.

In the paragraphs which follow, functional description and locations of all transmitter modules are presented.

Oscillator Module and Logic Driver Board (see Figure 8-5). - The crystal oscillator generates a 64-kHz clock (compatible with DTL and TTL logic) which is buffered for driving all transmitter logic using a quad 2-input NAND dual in-line integrated circuit as a logic inverting element. The crystal oscillator has a short-term stability of $\pm 1 \times 10^{-9}$.

8-Bit PN Sequence Generator (see Figure 8-6). - The PN sequence generator is implemented using standard integrated circuit logic, operating basically as indicated in Figure 8-6. An 8-bit code word is parallel loaded into an 8-stage shift register and shifted out at a 64-kHz rate. This is done repeatedly, reloading every eight-bit times. An end of sequence (inverted) output voltage is supplied by the module in addition to the PN sequence output. The end of sequence signal has an 8-kHz repetition rate and is used to clock data into the pulser. The 8-bit code word used in the breadboard is shown in the timing sketch included in Figure 8-6. Each data bit to be transmitted is "multiplied" by this word. (This is done by circuitry in the Pulser Module.)

Pulser Module (see Figure 8-7). - The Pulser Module contains a flip-flop to store each data bit between data entry pulses; and its output is "multiplied" by the 8-bit PN sequence.

TABLE 8-2. INPUT/OUTPUT INTERFACE

Connections		Remarks
From	To	
Surface Wave Transmitter		
Data In	Binary Data Source	(1) Cable - Coax or shielded wire preferred Logic - Compatible with TTL & DTL Data Rate - 8 kHz (Max) Voltage Levels - 0V to +5V
Clock Out	Binary Data Source	(2) For synchronous clocking of data into transmitter Clock Rate - 8 kHz Compatible with DTL & TTL Cable - Coax or shielded wire
$\overline{\text{Clock Out}}$	Binary Data Source (Optional)	(3) Inverse of Clock Out
Output	50 Ω Antenna or Linear Wideband Amplifier (Optional)	(4) 50 Ω Coax Signal Level: -47 dBm
PN (Rear Panel TP)	Oscilloscope, Etc.	(5) Logic Output (DTL & TTL Compatible) Voltage Level: 0V to +5V
64 kHz Clock (Rear Panel TP)	Oscilloscope, Etc.	(6) Same as (5)
Voltage TP's (+12,+10,-10, -6,+5)	Digital Voltmeter (or equivalent)	
Surface Wave Receiver		
RF In	50 Ω Receiver IF or Antenna System	(7) Cable - 50 Ω Coax Dynamic Range: -60 dBm ±20 dB Bandwidth - 8 MHz (Min) Input S/N: -19 dB (Min) Nominal Input Signal Level: -60 dBm
Voltage TP's (+12,-12,+5,-5)	Digital Voltmeter (or equivalent)	

TABLE 8-2. INPUT/OUTPUT INTERFACE (CONT)

Connections		Remarks
From	To	
Signal Processor		
Data Out	Binary Data Register	(8) Cable - Coax or Shielded Wire TTL & DTL Compatible Data Rate - 8 kHz (Max) Voltage Levels: 0V to 5V
Clock Out	Binary Data Register	(9) Synchronous Clocking (See Remark (2) Surface Wave Transmitter) Voltage Levels: 0V to 5V
-5 VDC TP	Digital Voltmeter (or equivalent)	

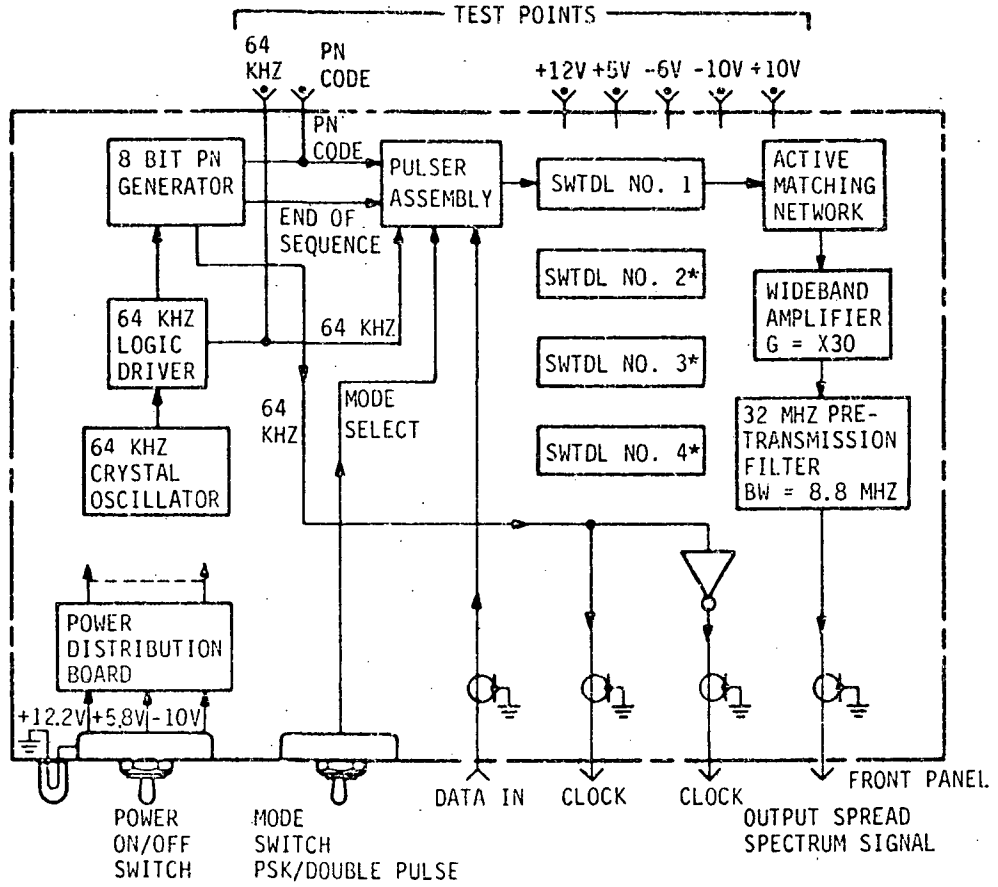


Figure 8-4. Spread Spectrum Transmitter, Block Diagram

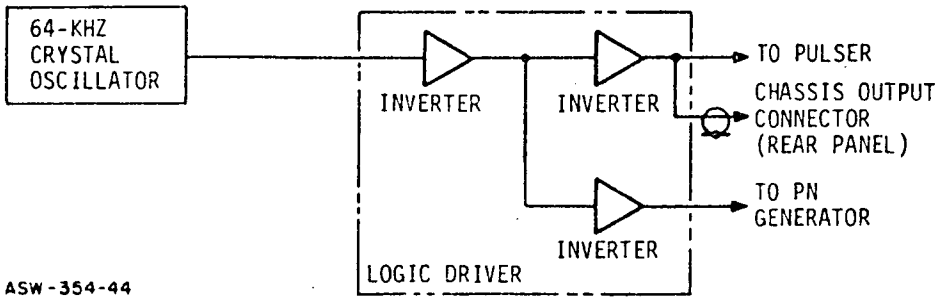


Figure 8-5. Oscillator Module and Logic Driver Board (Transmitter)

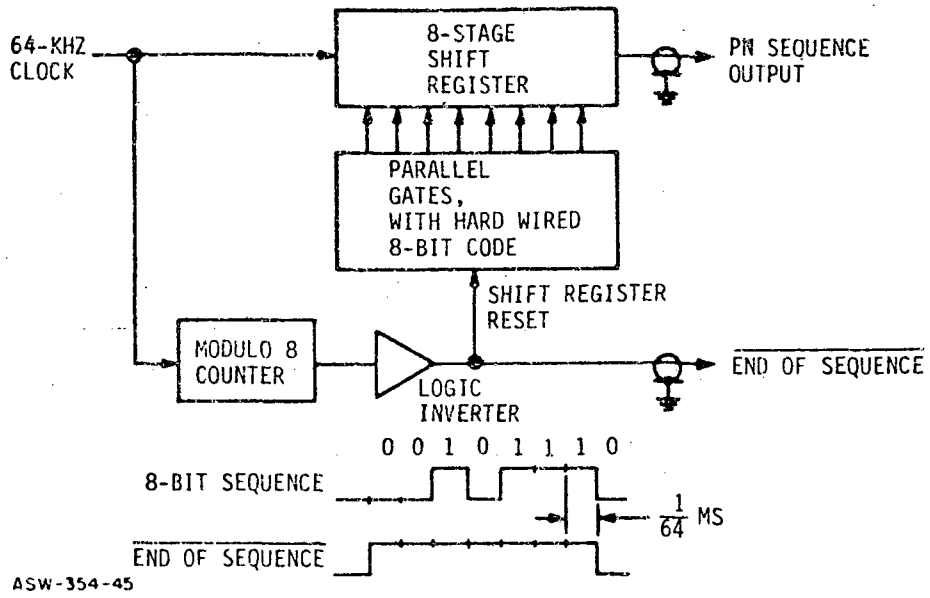
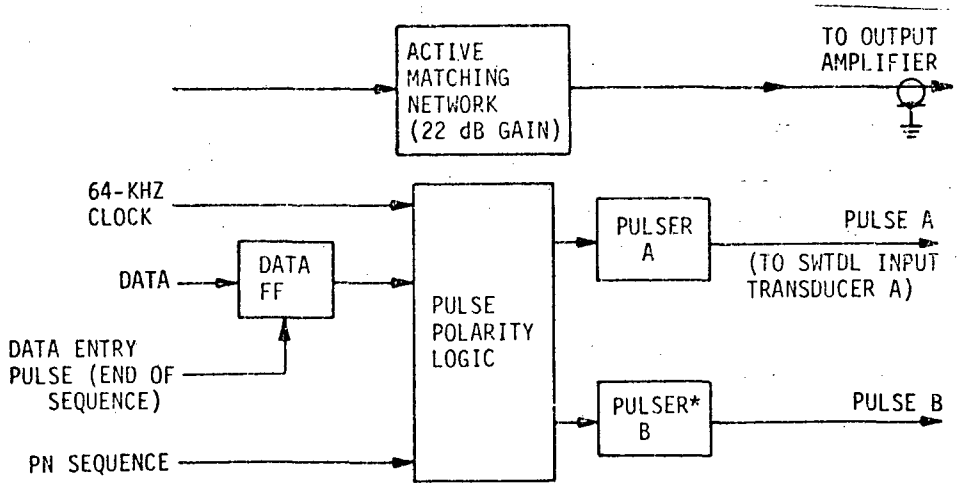


Figure 8-6. 8-Bit PN Sequence Generator (Transmitter)



*THIS PULSER IS DISABLED WHEN THE COHERENT PSK MODE IS SELECTED.

TRUTH TABLE			
DATA FF OUTPUT	PN SEQUENCE	PULSER A OUTPUT	PULSER B OUTPUT
1	1	POSITIVE	POSITIVE
1	0	NEGATIVE	NEGATIVE
0	0	NEGATIVE	POSITIVE
0	1	POSITIVE	NEGATIVE

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Figure 8-7. Pulser Module (Transmitter)

A "truth table" is included in the figure, illustrating the signal states appearing at the two outputs of the pulser polarity logic circuit. Both outputs occur at a 64-kHz bit rate, corresponding to the data "scrambled" by the PN sequence.

Note that for a data "1" both A and B pulser outputs correspond exactly to the PN sequence states. When a data "0" exists, the A pulses correspond to the PN sequence states, but the B pulses are opposite. The B pulse is used only when the Double Pulse Modulation mode is employed providing the "delayed" pulse and is disabled otherwise. The delay results from relative SWTDL placement, outputs A and B actually being time coincident.

The active matching network needed with the SWTDL is contained in the Pulser module as a matter of implementation convenience. No matter which SWTDL module is plugged into the transmitter, this same matching network is connected to its output transducer. An input transducer impedance matching network is included in both pulser circuits, A and B.

SWTDL Module. - All of the four SWTDL's provided with the transmitter are packaged in identical modules, and any one of them can be connected for use in data transmission. All have different codes in the output transducer pattern, but they have identical center frequencies and bandwidths.

Figure 8-8 illustrates the module connections. Input transducer A is activated by the A pulses from the Pulser module, and the B pulses are connected to input transducer B. Since transducer A is closer to the output transducer, its contribution to the SWTDL output leads that of transducer B in the time sense.

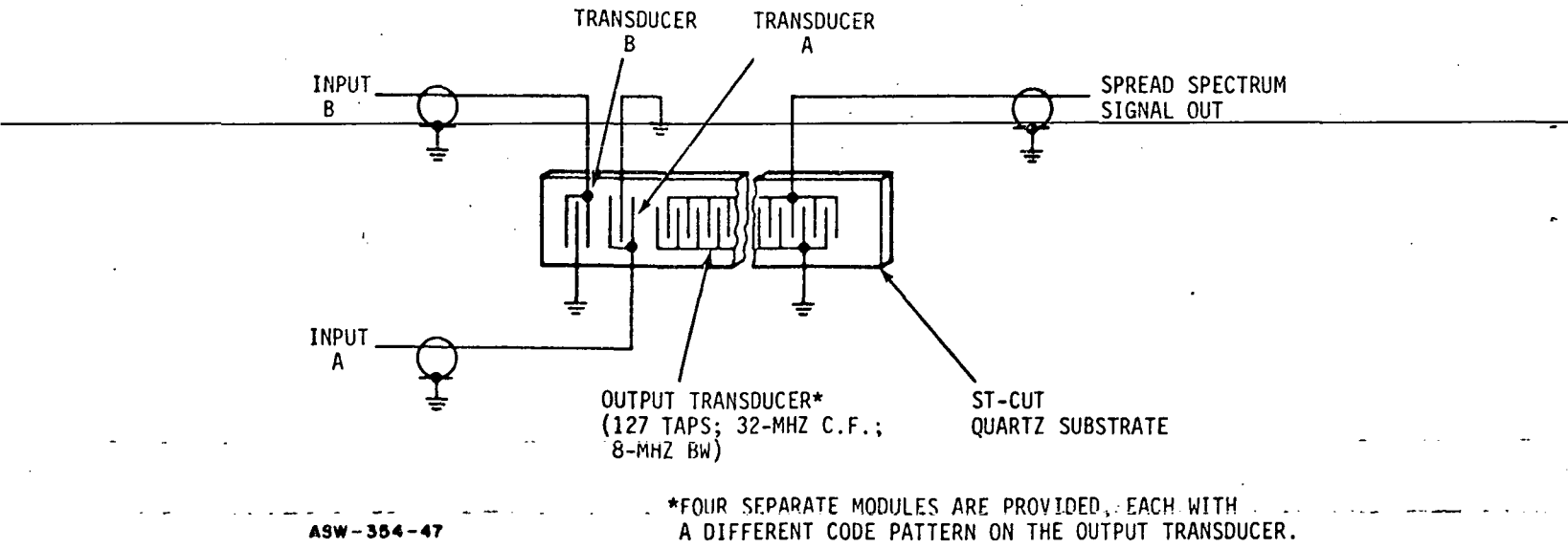


Figure 8-8. Transmitter SWTDL Module

RF Amplifier and Pretransmission Filter. - An rf amplifier module is provided to increase the SWTDL output signal power to a level of about -40 dBm (see Figure 8-9), and the output is passed through a pretransmission filter before being applied to the transmitter output terminal. The filter shown in Figure 8-10 has a net loss of 6 dB, and the transmitter output signal level is approximately -46 dBm.

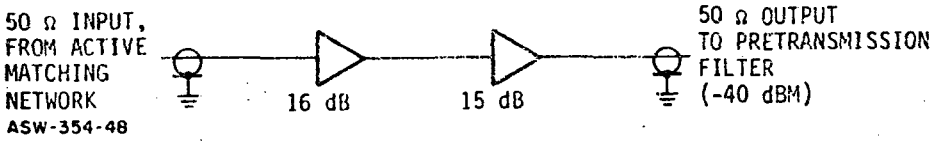


Figure 8-9. Wideband RF Output Amplifier (Transmitter)

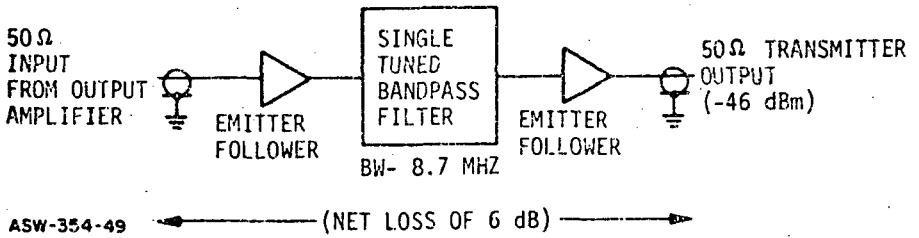


Figure 8-10. Pretransmission Filter (Transmitter)

Power Distribution Board (see Figure 8-11). - A board mounted on the chassis provides additional filtering and regulation for the power supply voltages. Since there is a voltage drop through these circuits, test points are provided at the rear of the chassis to permit the correct module voltages to be set.

8.3.2 Receiver

A block diagram showing the major functional elements of the receiver is shown in Figure 8-12. It contains the rf processing circuitry which includes the receiver front-end, AGC network, matched filter SWTDL's, polarity switch/PN generator, and Circulating Integrator assembly.

The input signal is filtered and amplified then applied to an AGC network. AGC voltage is controlled by measuring the correlation peaks in the signal at the SWTDL output. Thus, the gain is determined primarily by the signal, minimizing the effect of noise upon the automatic gain setting.

The SWTDL signal output, which is maintained at a nearly constant level, is applied to a polarity switch/PN generator module. When the receiver is synchronized with the incoming signal, the PN generator is synchronous with the one used in the transmitter; and it controls the

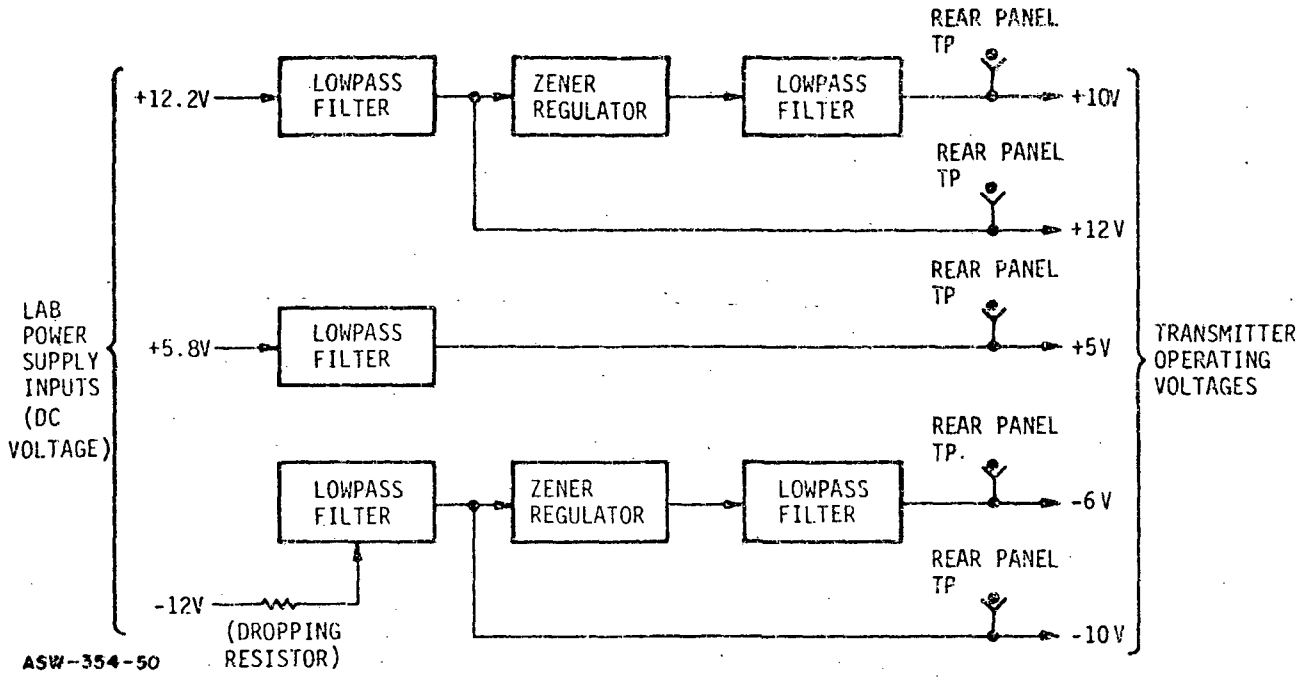


Figure 8-11. Power Distribution Board (Transmission)

polarity switch so as to remove the 8-bit PN modulation from the received signal. Therefore, the polarity switch output pulses (correlation pulses whose phase is determined solely by the data content) are coherently added in the recirculating integrator.

An end of sequence pulse from the PN generator controls a gate in the Loop Amplifier module, momentarily opening the Circulating Integrator feedback loop at the end of each data bit interval. The CI output pulses, therefore, build linearly in amplitude during each bit interval; and they are "dumped" at the end of each bit interval. Synchronization of the PN generator is accomplished at the signal processor (controller) unit following baseband demodulation and clock reconstruction. A functional description of the modules contained in the receiver are presented in the following paragraphs. Paragraph 8-5 discusses the location of each of these system subassemblies.

Receiver Front-End (see Figure 8-13). - The receiver front-end consists of an input single-tuned bandpass filter followed by two wideband low-noise amplifier stages with a total gain of 37 dB and a noise figure of 6 dB. The input filter provides rejection of out-of-band noise to give improved dynamic range in the amplifiers.

AGC Network (see Figure 8-14). - The output of the receiver front-end passes through an AGC amplifier prior to application of the spread spectrum signal to the SWTDL. This AGC amplifier (which consists

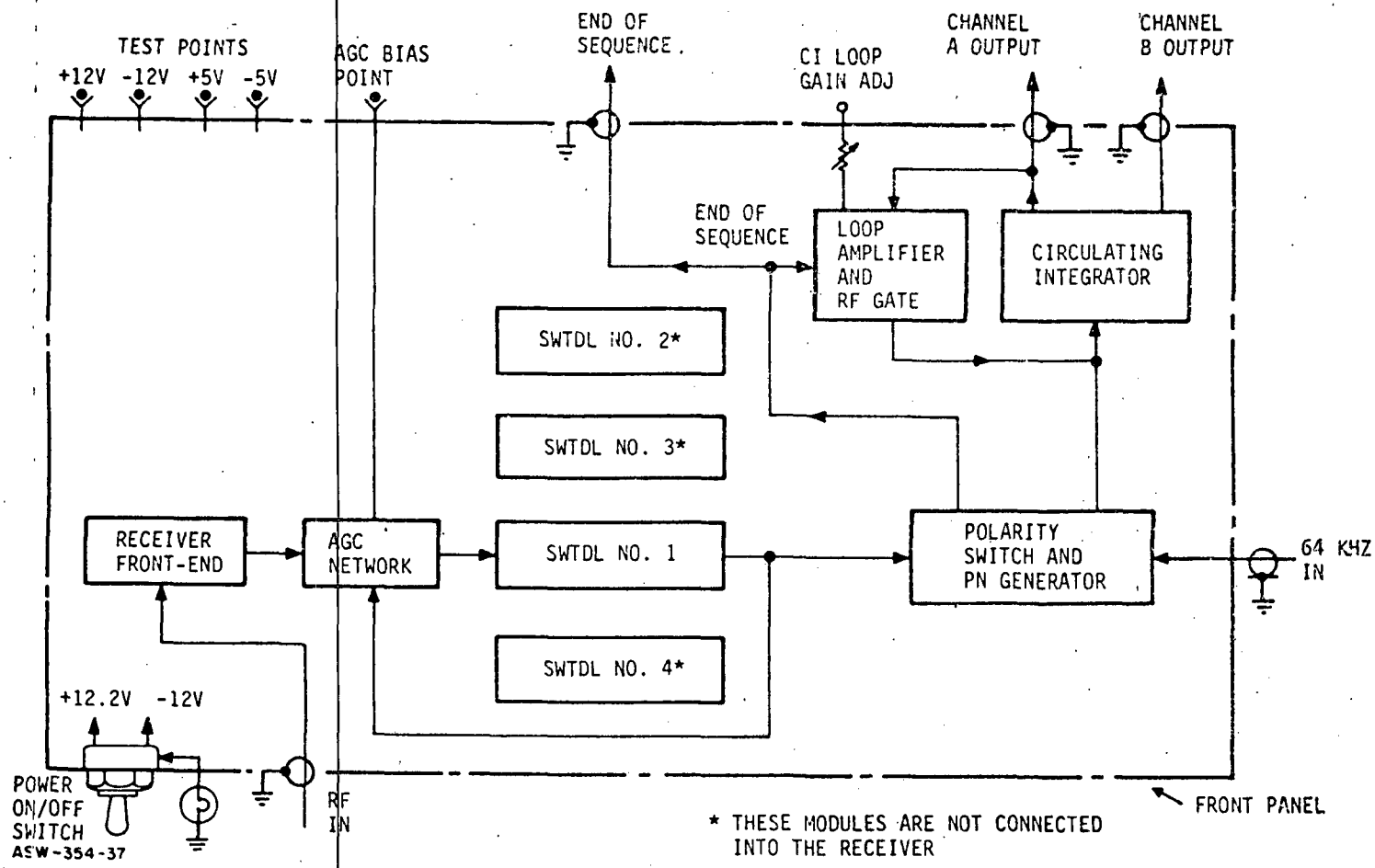


Figure 8-12. Spread Spectrum Receiver, Block Diagram

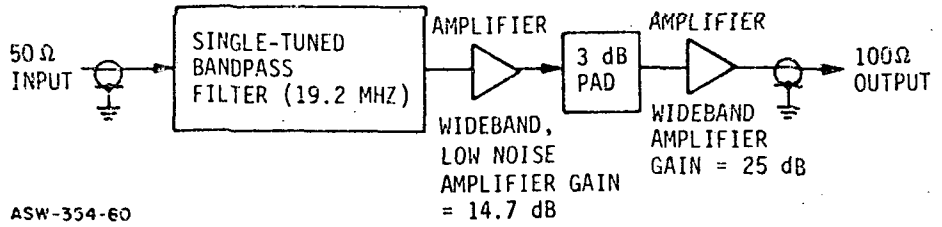


Figure 8-13. Receiver Front-End

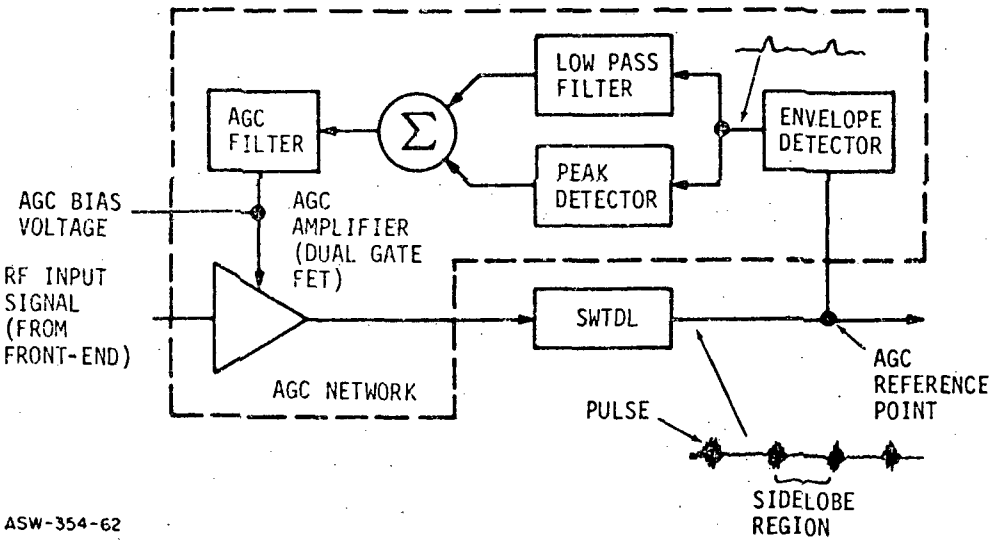


Figure 8-14. AGC Network (Receiver)

of two dual-gate FET's in cascade) provides a linear dynamic gain control range of better than 45 dB for input S/N ratio of -12 dB. AGC control is derived from the SWTDL output (as seen in Figure 8-14). The correlation peaks are envelope detected and then simultaneously peak detected and integrated before being summed at the AGC filter.. Error correction voltage at the AGC amplifier automatically compensates for DC voltage variations at the peak detector in low S/N operation. The result is an AGC amplifier whose change in gain is less than one dB over input S/N ratio changes of +10 dB to -19 dB.

SWTDL Module (see Figure 8-15). - The receiver SWTDL modules consist of input/output matching networks and wideband amplifiers which results in a near zero insertion loss matched filter device. There are four modules each containing surface wave devices identical to those at the transmitter except reversed in input/output direction to form the matched filter response. These SWTDL modules have 50 Ω in and out, 32-MHz center frequency, and have an 8-MHz bandwidth.

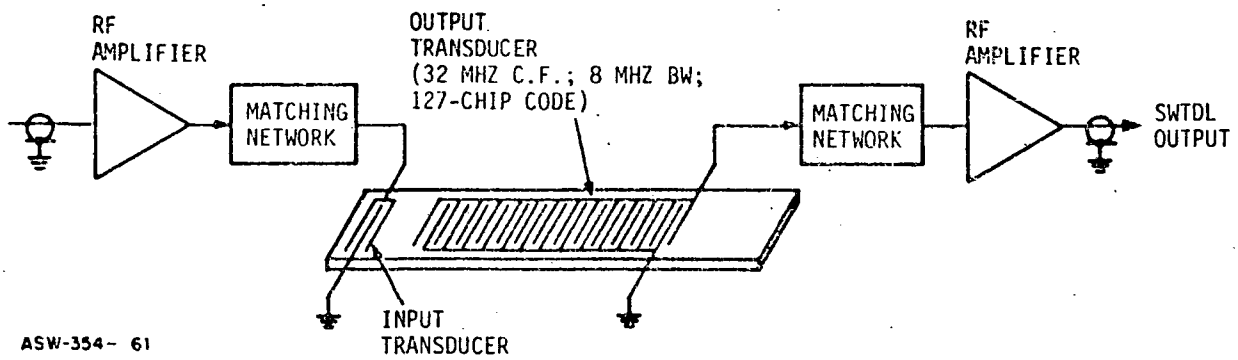


Figure 8-15. SWTDL Modules (Receiver)

Circulating Integrator Assembly (see Figure 8-16). - The Circulating Integrator assembly is composed of the re-entry delay line module and the CI feedback loop module. They are electrically interconnected as shown in Figure 8-16. The incoming rf correlation signal is linearly summed with a feedback correlation signal, and the resultant is applied to a surface wave delay line whose delay precisely equals the time interval between rf bursts. The result is a controlled positive feedback signal in the rf domain with the output correlation signals at outputs B and A increasing linearly in time.

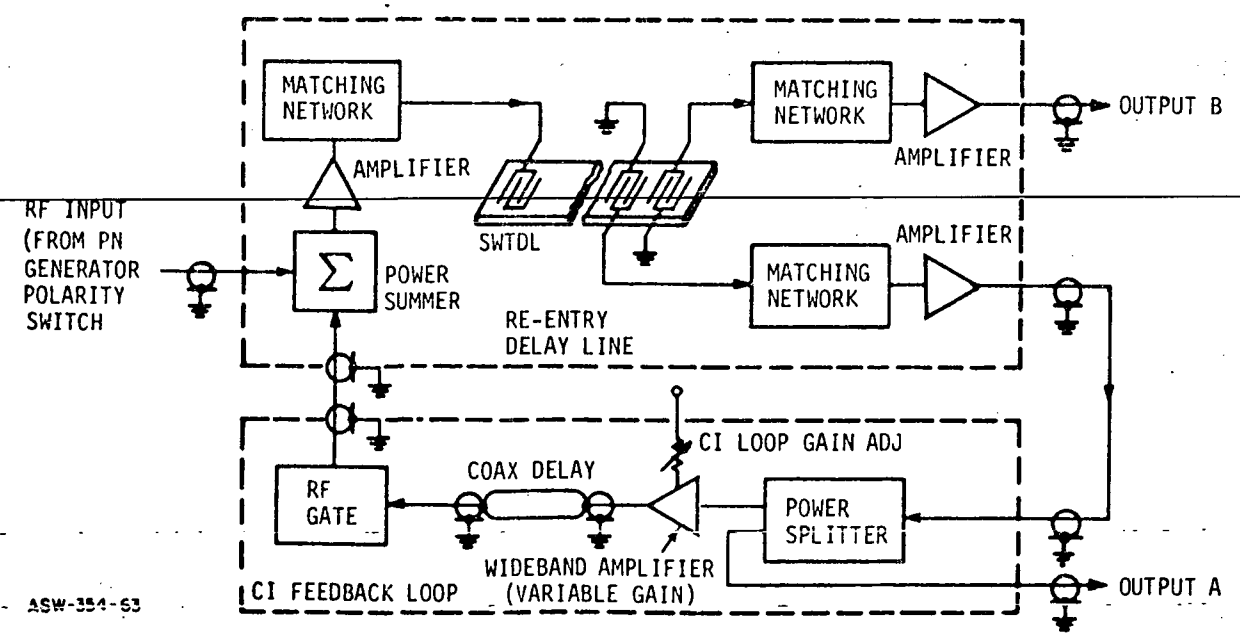


Figure 8-16. Circulating Integrator Assembly (Receiver)

A variable gain wideband amplifier provides an adjustment for loop gain; and, an rf gate opens the loop at the end of eight circulations, corresponding to one data bit. A coax delay was used to fine tune the loop delay to 15.6 μs.

Polarity Switch and PN Generator (see Figure 8-17), - This module de-scrambles the PN phasing on the correlation peaks between data bits, such that the phase polarity is either all 0^{o} or 180^{o} over the eight correlation signals which comprise one data bit. The SWTDL output is either inverted or unchanged in the analog polarity switch, based on the state of the 8-bit PN sequence generator. This PN generator is clocked from the reconstructed 64-kHz signal generated at the signal processor and is synchronized with the transmitter PN code using a pulse injection circuit to advance the PN state. An end of sequence pulse is generated in the PN generator to signify end of a data bit.

The de-scrambled correlation peaks are filtered in a 10-MHz bandpass to remove switching noise and then amplified at the output.

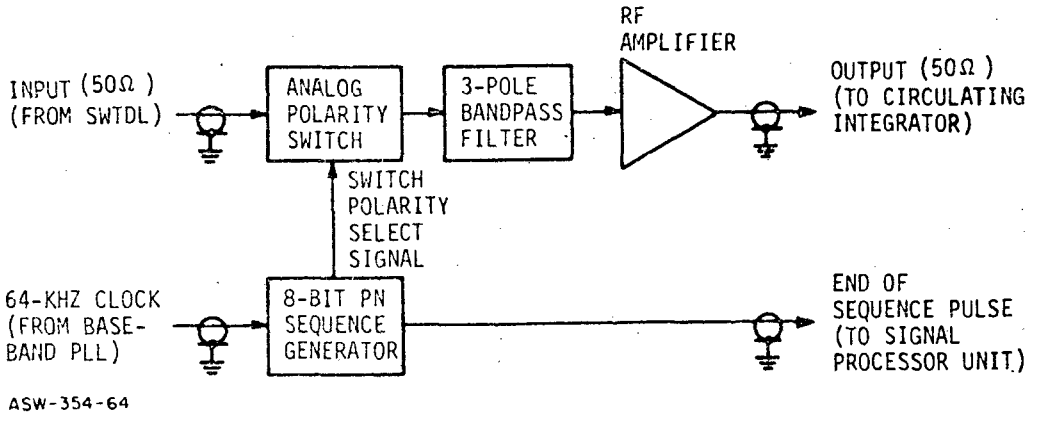


Figure 8-17. Polarity Switch and PN Generator (Receiver)

8.3.3 Signal Processor

The block diagram in Figure 8-18 shows the major circuit elements which comprise the signal processing portion of the spread spectrum communication link. This unit is responsible for the receiver synchronization and demodulation of the correlation signals for recovery of the transmitted data. The processor operates in two distinct modes; a Coherent PSK mode in which the correlating signals are coherently demodulated using a regenerated carrier and a Double Pulse mode in which quasi-coherent correlation peaks are differentally demodulated. In both modes, the demodulated signals are sent to a data reconstruction circuit for recovery of the transmitted binary patterns.

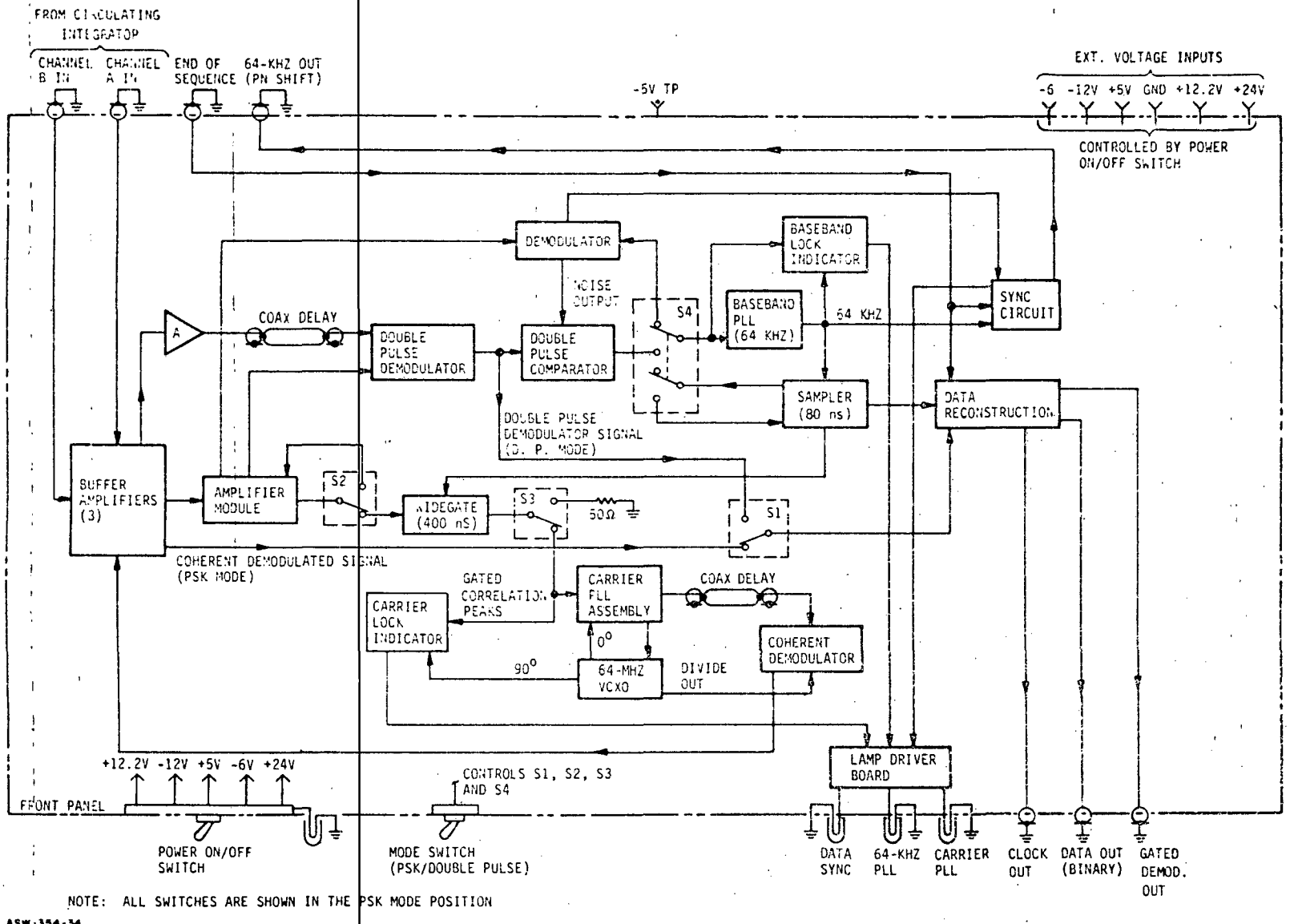


Figure 8-18. Signal Processor, Block Diagram

In the PSK mode, the transmitter 64-kHz clock is reconstructed at the receiver by phase-locking a voltage-controlled crystal oscillator to the envelope demodulated baseband pulses corresonding to the correlation peaks. Synchronization is checked every eight clock periods using a strobed comparator which advances the PN generator (in the receiver section) if threshold criterions are not met. Both the wide gate enable and the 80-ns sample pulse are derived from this 64-kHz reconstructed clock.

In the Double Pulse mode, the baseband 64-kHz clock is derived directly from the demodulator data using an absolute-value comparator to drive the phase lock loop. Receiver synchronization and data reconstruction of the binary signal are identical to that approach described in the PSK mode.

In the following paragraphs, each of the subassembly modules which comprise the signal processor will be described. Refer to figures in paragraph 8-6 for the physical location of the modules in the signal processor unit.

Buffer Amp Module (see Figure 8-19). - This module consist of three wideband variable gain amplifiers having a 50 Ω input and output impedance. They provide proper signal levels to downstream subassemblies.

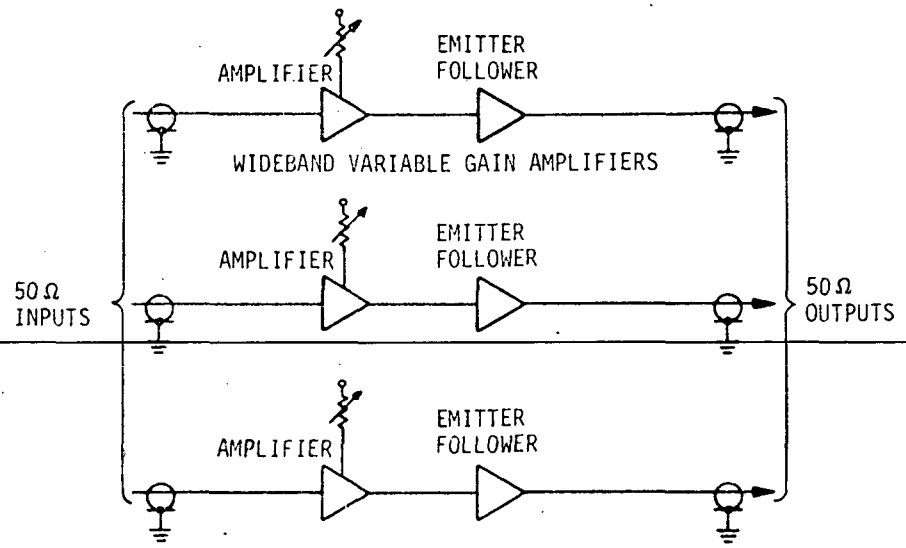


Figure 8-19. Buffer Amp Module (Processor)

Amp Module (see Figure 8-20). - This module buffers and matches signal levels between the PSK mode and double pulse mode.

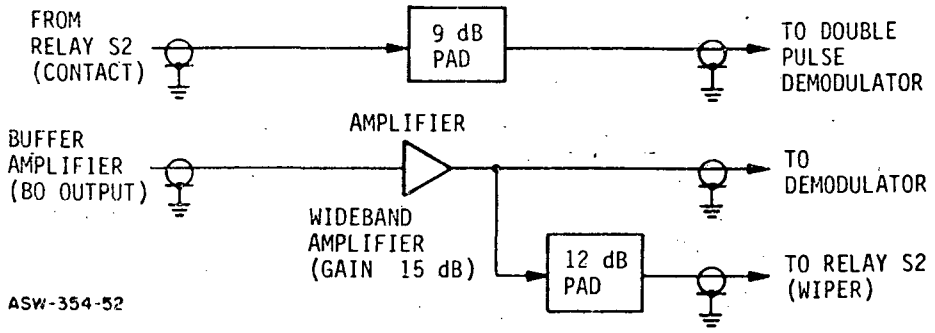


Figure 8-20. Amp Module (Processor)

Demodulator (see Figure 8-21). - Incoming correlation peaks from the Circulating Integrator (by way of the buffer amplifiers and amp module) are envelope detected and then limited using a voltage comparator, resulting in a series of constant amplitude 64-kHz pulses for driving the baseband phase lock loop. A variable threshold voltage (derived from the noise buildup in the Circulating Integrator) improves the resulting S/N ratio at the comparator output by cancelling the noise increase as the demodulated pulses get larger by raising the threshold. The envelope detector output is used in both modes by the sync circuit for sync verification.

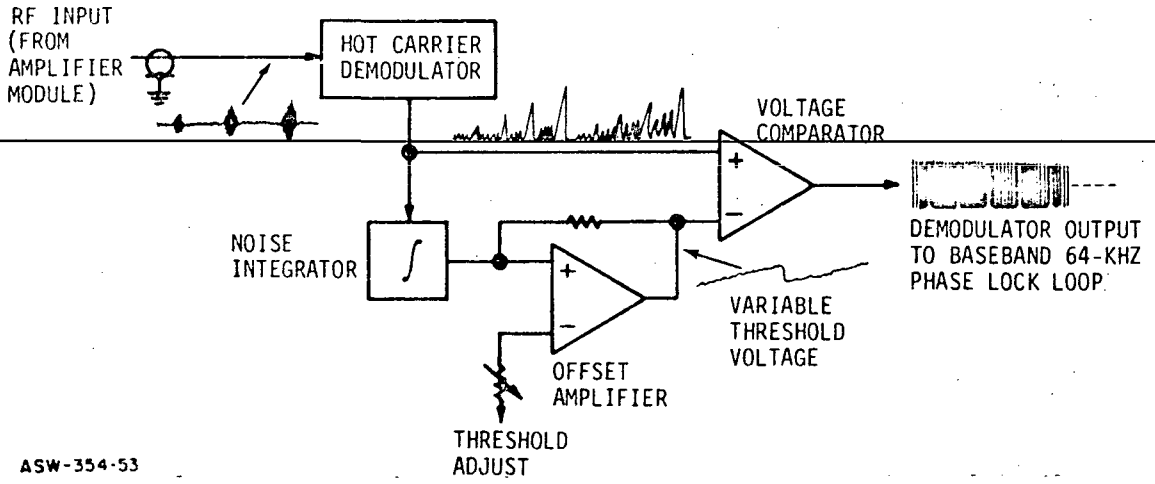


Figure 8-21. Demodulator (Processor)

Double Pulse Demodulator (see Figure 8-22). - The double pulse demodulator product multiplies the double correlation peak rf buildup out of Channel A of the circulation integrator (by way of the buffer amplifier and amplifier module) with its delayed version in Channel B. This results in a series of amplitude increasing pulses whose polarity is a function of the rf phasing of the correlation peaks. Channel B is amplitude limited in the module using a 30 dB dynamic range hot carrier limiter and is used as the LO signal in the product detector. A 3-pole Thompson-Butterworth Transitional (TBT) lowpass filter was used to recover the desired baseband signal with minimal intersymbol interference.

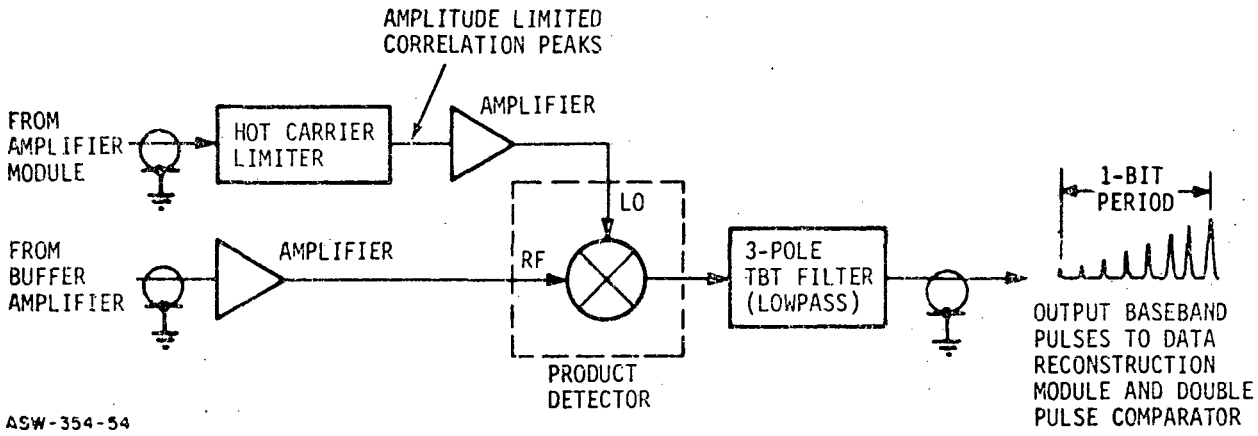
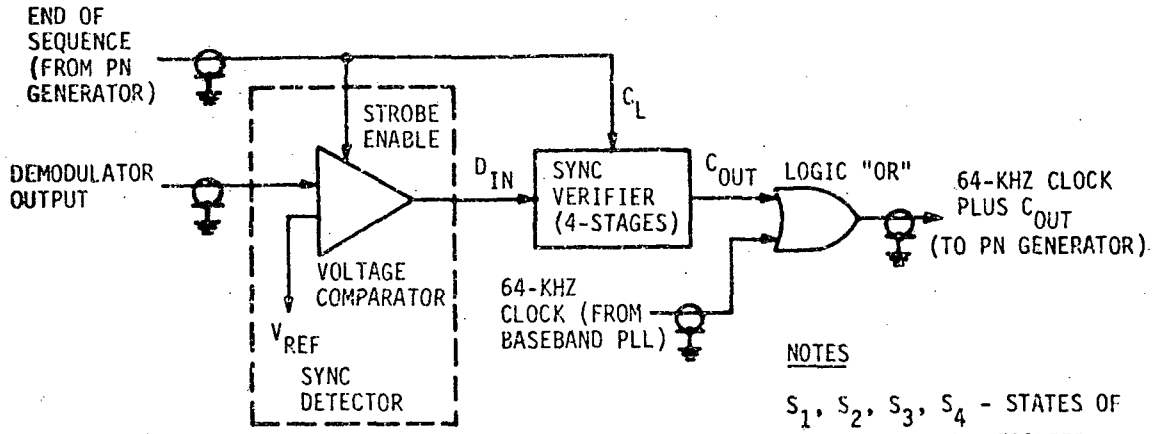


Figure 8-22. Double Pulse Demodulator (Processor)

Sync Circuit (see Figure 8-23). - The sync circuit makes the decision as to whether the receiver is synchronized with the transmitter. It consists of a sync detector (voltage comparator) which looks at the demodulator output once every eight bit times and makes a yes/no decision as to whether a signal was present. The sync verifier weighs the probability of sync versus false fire to determine whether the 8-bit PN generator should be advanced. The truth table shown in Figure 8-23 logically depicts the operation of the sync circuit. Only when all logic states in the 4-stage register are "0" does the C_{OUT} line come high which advances the PN generator. Refer to the sync analysis section (Section 5.0) of this report for more detail.

Double-Pulse Comparator (see Figure 8-24). - The double-pulse comparator is used only in the Double Pulse mode of the system for driving the 64-kHz baseband PLL with constant amplitude pulses derived from the demodulated data. It consists of a double-ended voltage comparator; in which, the output goes high anytime the input signal exceeds a preset voltage threshold (in either the positive or negative voltage direction); a noise integration; and an offset amplifier. Therefore, the circuit operates as an absolute value detector for dual polarity pulses.



NOTES

S_1, S_2, S_3, S_4 - STATES OF 4-STAGE SYNC VERIFIER

f_n - PRESENT STATE OF SYSTEM

f_{n+1} - NEXT CLOCK PULSE STATE

DEMOD OUTPUT $> V_{REF}$ DURING END OF SEQ —— D_{IN} IS LOGIC "1"

DEMOD OUTPUT $< V_{REF}$ DURING END OF SEQ —— D_{IN} IS LOGIC "0"

TRUTH TABLE

f_n					f_{n+1}
D_{IN}	S_1	S_2	S_3	S_4	C_{OUT}
0	0	0	0	0	1
1	0	0	0	0	0
0	1	0	0	0	0
1	1	0	0	0	0
0	0	1	0	0	0
1	0	1	0	0	0
0	1	1	0	0	0
1	1	1	0	0	0
0	0	0	1	0	0
1	0	0	1	0	0
0	1	0	1	0	0

f_n					f_{n+1}
D_{IN}	S_1	S_2	S_3	S_4	C_{OUT}
1	1	0	1	0	0
0	0	1	1	0	0
1	0	1	1	0	0
0	1	1	1	0	0
1	1	1	1	0	0
0	0	0	0	1	1
1	0	0	0	1	0
0	1	0	0	1	0
1	1	0	0	1	0
0	0	1	0	1	0

f_n					f_{n+1}
D_{IN}	S_1	S_2	S_3	S_4	C_{OUT}
1	0	1	0	1	0
0	1	1	0	1	0
1	1	1	0	1	0
0	0	0	1	1	0
1	0	0	1	1	0
0	1	0	1	1	0
1	1	0	1	1	0
0	0	1	1	1	0
1	0	1	1	1	0
0	1	1	1	1	0
1	1	1	1	1	0

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Figure 8-23. Sync Circuit (Processor)

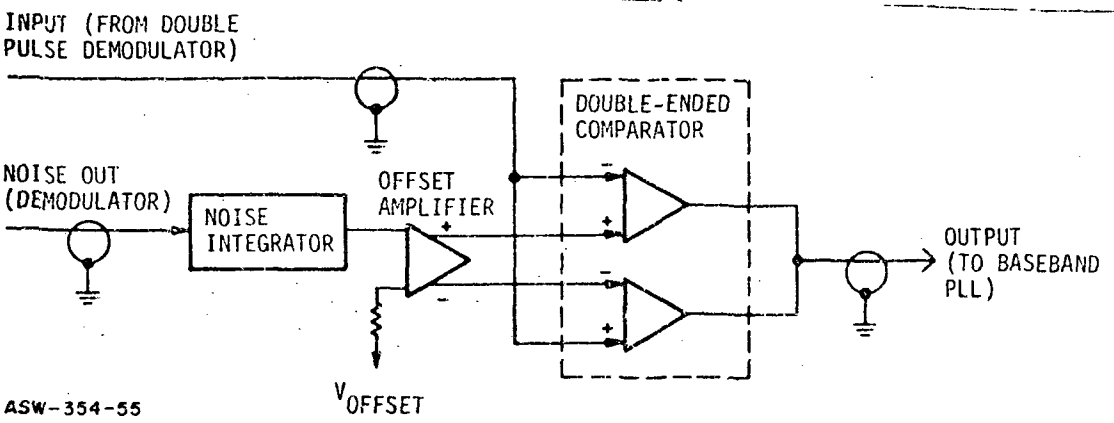


Figure 8-24. Double Pulse Comparator (Processor)

The noise integration at the offset amplifier varies the voltage threshold with noise similiar to that described for the demodulator.

64-kHz Baseband PLL (see Figure 8-25). - The 64-kHz baseband PLL locks to the centroid of the amplitude limited correlation peaks out of the demodulation (PSK Mode) or double-pulse comparator (Double Pulse mode) for reconstructing the 64-kHz clock at the receiver. It is basically a second-order PLL which splits the energy spectrum of the incoming signal using a doubly-balanced wideband mixer and then integrates the error voltage to zero at the input to a 64-kHz voltage controlled crystal oscillator.

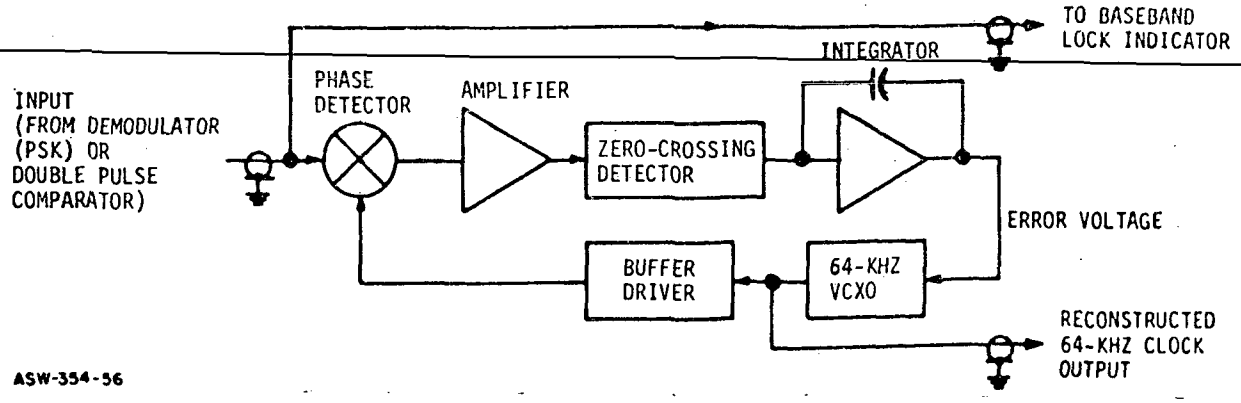


Figure 8-25. 64-KHz Baseband PLL (Processor)

Baseband Lock Indicator (see Figure 8-26). - The baseband lock indicator is a quadrature phase detector which looks at the 64-kHz PLL error voltage and makes a decision as to whether the loop is phase-locked to the envelope of the incoming correlation peaks or not. The output of the 64-kHz PLL is shifted 90^{o} and phase compared with the input signal to the 64-KHz PLL using an exclusive OR logic element. This output signal is then amplified, integrated (τ = 100 ms), and compared to a preset voltage threshold for determining lock.

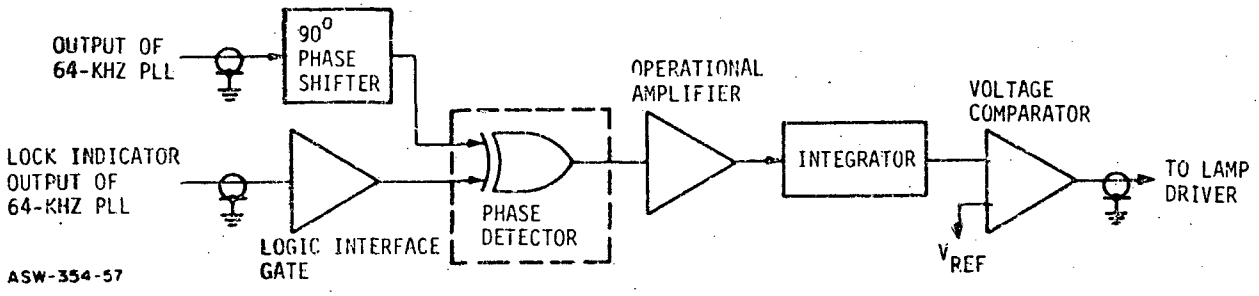


Figure 8-26. Baseband Lock Indicator (Processor)

Wide Gate Module (see Figure 8-27). - The wide gate module gates only the correlation peaks through to the carrier PLL assembly, rejecting all sidelobe noise once synchronization has been achieved. The circuit consist of a delayed 1-shot which turns on an rf gate for a 400-ns period every 15.6 µs. A switch driver is used to enable the rf gate. The signal is amplified in a wideband amplifier and buffered using an emitter follower at the output. Switching noise in the signal path is down 20 dB for the smallest amplitude correlation peak.

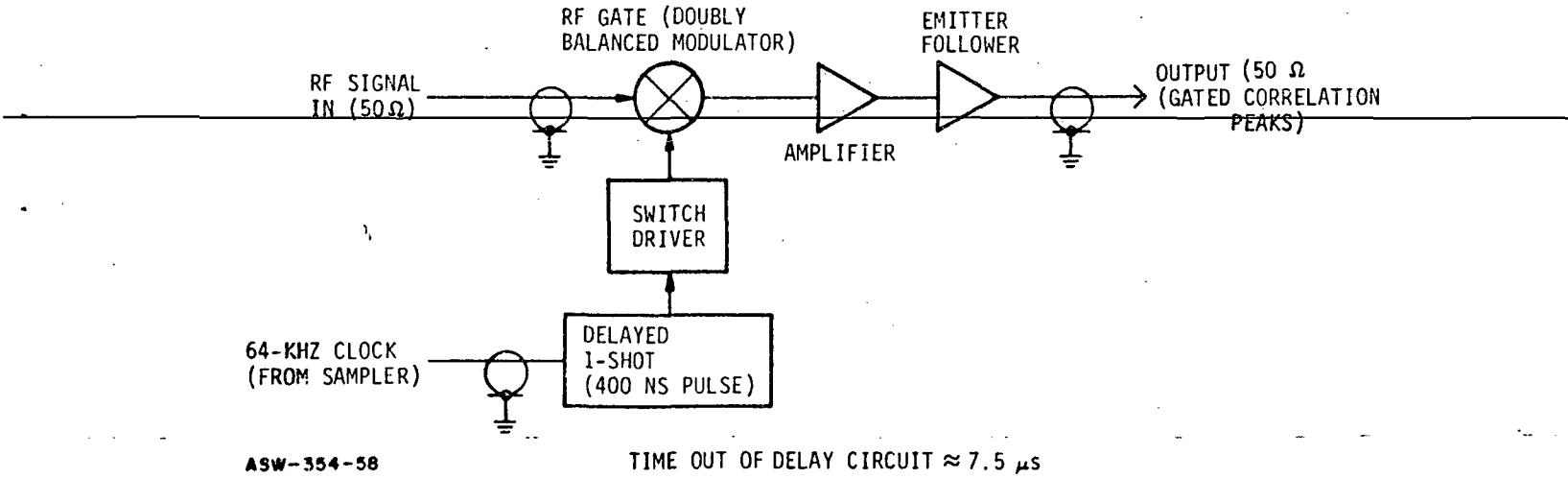


Figure 8-27. Wide Gate Module (Processor)

Sampler Module (see Figure 8-28). - This circuit generates the 80-ns sample pulse which looks at the peak of the demodulated eighth circulation in the Circulating Integrator for determining whether a "1" or "0" was transmitted. It consist of quad 2-input NAND inverter, for buffering and a inversion, a delayed 80-ns 1-shot, and an output logic driver. The module also serves as a buffer for the 64-kHz clock for driving the wide gate circuit. The 80-ns strobe is generated once every clock period, approximately 7.5 μs after the rising edge, and is logically NANDed with the end of sequence at the data reconstruction circuit to select the proper pulse for sampling the demodulated buildup.

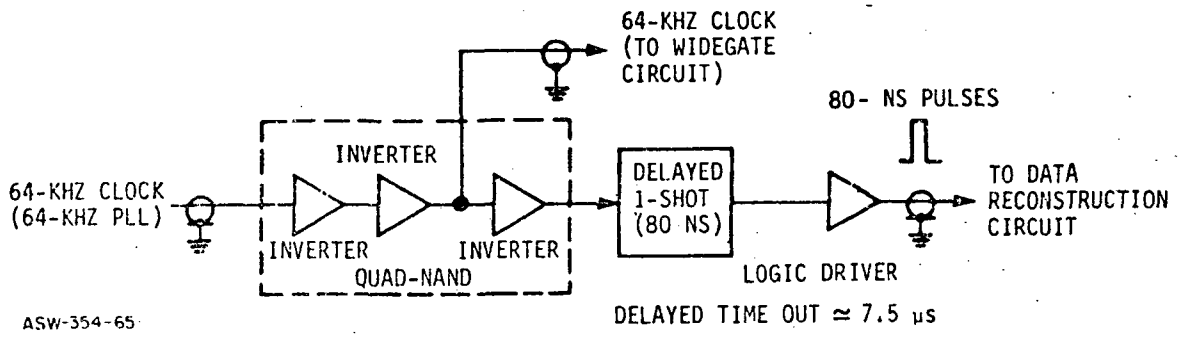


Figure 8-28. 80-ns Sampler Module (Processor)

Carrier Indicator (see Figure 8-29). - The carrier indicator determines whether the carrier PLL assembly is phase locked to the rf correlation peaks out of the wide gate and will light a front panel indicators lamp if lock is observed. The circuit operates as a quadrature phase detector on the doubled 64-MHz correlation peaks by generating a positive DC voltage if the carrier PLL error voltage approaches zero. This signal is amplified, integrated, and voltage compared at the output with a preset reference. If this DC voltage exceeds V_{REF}, a lock is indicated by the front panel lamp.

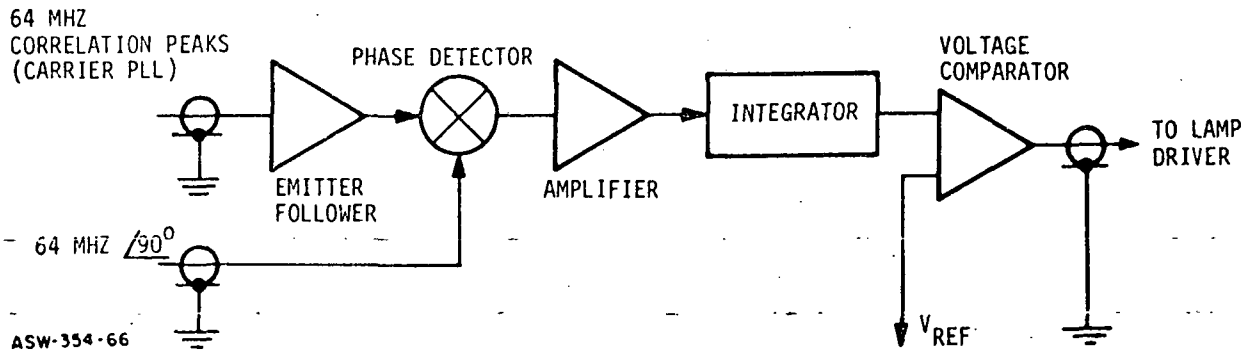


Figure 8-29. Carrier Indicator (Processor)

64-MHz VCXO Module (see Figure 8-30). - The 64-MHz VCXO module generates the doubled frequency rf signal used by the carrier PLL assembly to regenerate the rf portion of the incoming correlation peaks in the PSK mode. It consists of a 64-MHz VCXO, whose frequency is controlled by the carrier PLL, a quadrature power splitter, a hybrid 0-degree power splitter, and three wideband amplifiers at the output. The 0-degree output is phase locked to the incoming signal at the carrier PLL assembly; the 90-degree output is used in the carrier indicator; and the divider output (same phase as 0-degree output) is used as the LO signal in the coherent demodulator module.

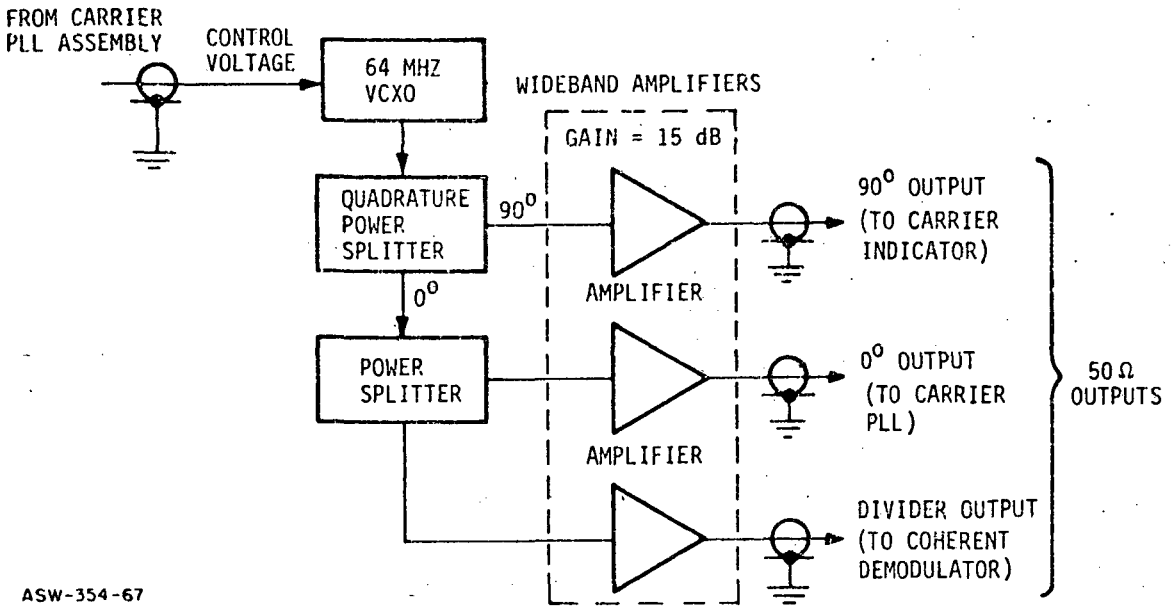


Figure 8-30. 64-MHz VCXO Module (Processor)

Carrier PLL Assembly (see Figure 8-31). - This module is the control portion of the carrier regeneration loop which generates a phase coherent 64-MHz signal for demodulating the correlation peaks in the PSK mode following the matched filter SWTDL and Circulating Integrator. The incoming 32-MHz correlation peaks are power split with one side going through a wideband filter and coax delay to the coherent demodulation and the other side going to the carrier regeneration circuitry. The correlation signal is first limited using a hot carrier limiter, doubled, and filtered to strip off 0-degree and 180-degree phase variations. Finally, it is phase compared with the 64-MHz VCXO output signal which in turn is used to control the 64-MHz VCXO. The phase lock loop is a standard second order, high gain loop with an effective noise bandwidth of 6 kHz.

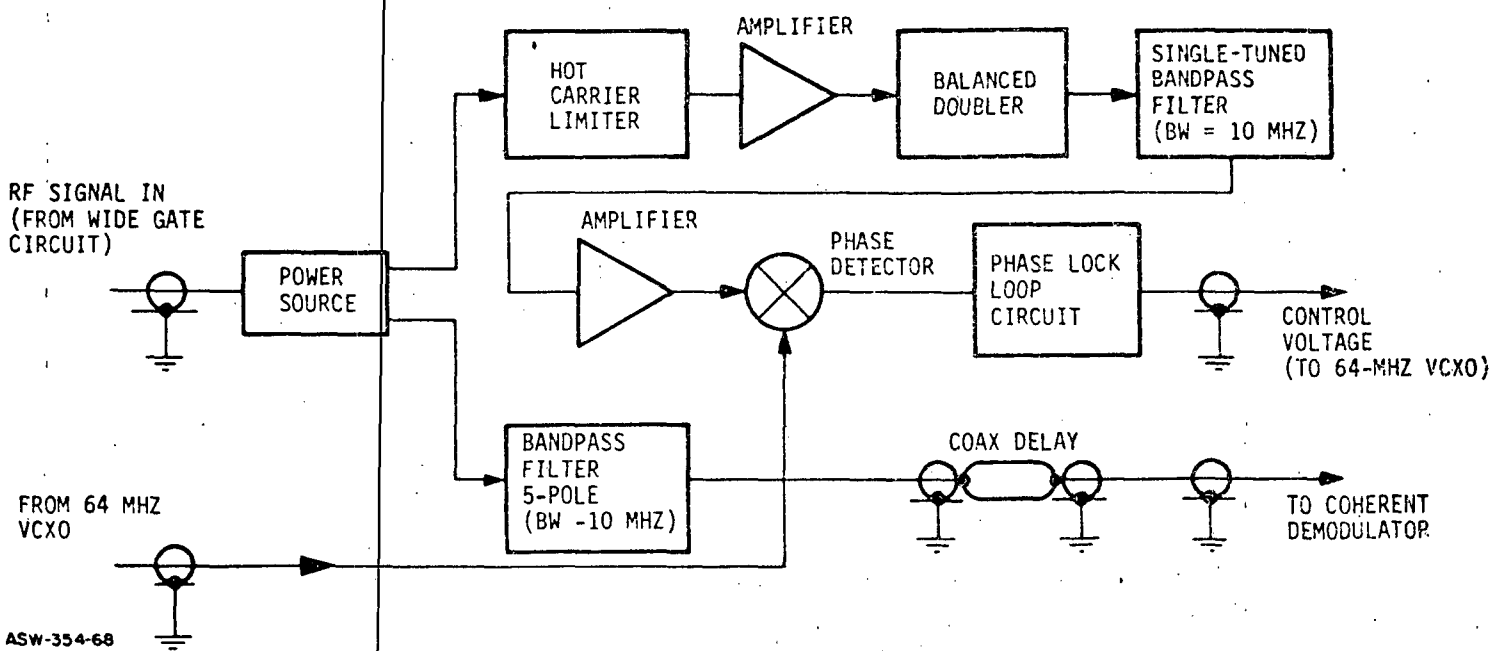


Figure 8-31. Carrier PLL Assembly (Processor)

Coherent Demodulator (see Figure 8-32). - The coherent demodulator performs the baseband demodulation of the rf correlation signals in the PSK mode using the regenerated carrier signal of the receiver as the coherent reference signal in the product detector. The 64-MHz continuous carrier is first divided to give 32 MHz by using a hi-speed flip-flop. It is then amplified, buffered, and applied to the balanced mixer product detector as the LO signal. The 32-MHz correlation peaks (which were filtered and buffered at the carrier PLL assembly) are subsequently down-converted to baseband, filtered in a 5-pole TBT low-pass filter, and amplified at the output. The result is a series of baseband pulses which buildup linearly over an 8-bit (1 data bit) interval as shown in Figure 8-32.

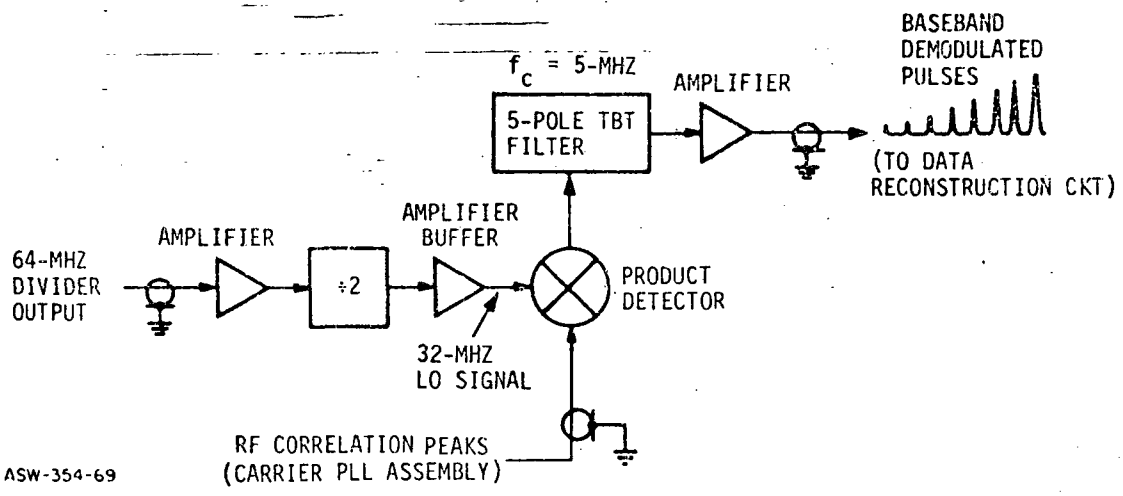


Figure 8-32. Coherent Demodulator (Processor)

Data Reconstruction Circuit (see Figure 8-33). - The data reconstruction circuit samples the eighth and final circulation out of the Circulating Integrator for each data bit, and subsequently reconstructs the transmitted binary data based on the polarity of these demodulated signals (see Appendix E). The incoming demodulated signal (Coherent Demod (PSK) or Double Pulse Demod (DP mode)) is split and applied to two separate rf gates, one with an inversion across it and the other with no inversion. The 80-ns strobe is NANDed with the end of sequence pulse resulting in a 80-ns gate which passes only the peaks of the demodulated eighth correlation peak. Two enabled voltage comparators will subsequently either set or reset theoutput flip-flop depending on whether the demodulator pulse buildup was positive or negative. The two comparators have a near zero slicing level for the best bit detection. The data reconstruction circuit supplies three output; a gated demodulated output to the rear panel, the recovered binary data output to the front panel, and a buffered data clock output to the front panel.

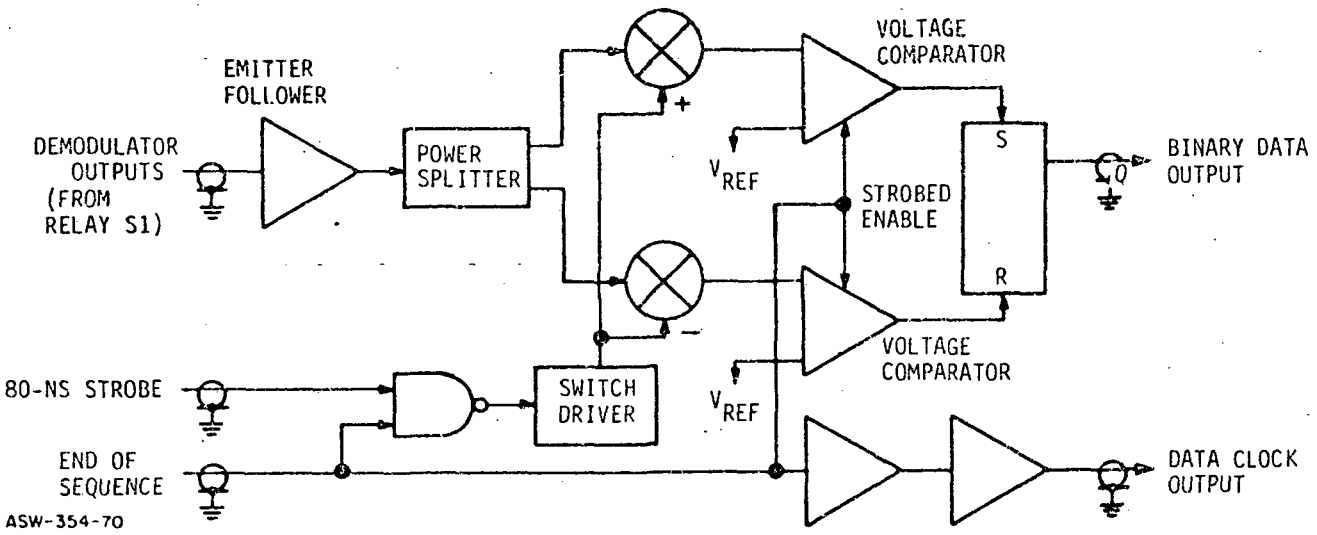


Figure 8-33. Data Reconstruction Circuit (Processor)

Lamp Driver Board (see Figure 8-34). - This is a series of three transistor drivers which actuate 40 mA, 5 volt indicator lamps upon command from the appropriate indicator module in the signal processor.

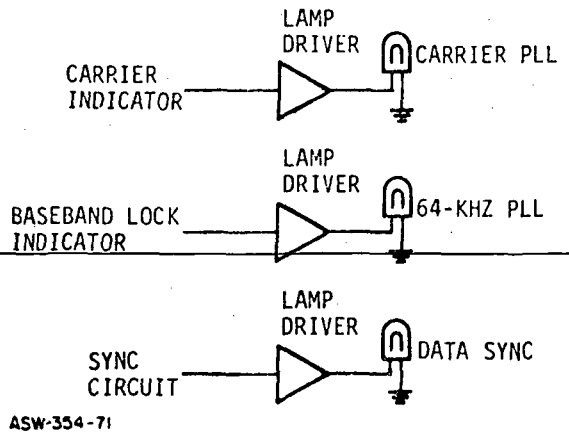


Figure 8-34. Lamp Driver Board (Processor)

8.4 Module Interconnections

Tables 8-3, 8-4, and 8-5 are wiring list tabulations of the individual-subassembly interconnections of the transmitter, receiver, and signal processor, respectively. The list of words under each module in column one as well as the words in parentheses in the second column are

TABLE 8-3. TRANSMITTER MODULE INTERCONNECTIONS

Connection		
From	To	Remarks
SWTDL (1 of 4)	Pulser (Internal Connector)	Hard-wired Coax connectors (SWC Modules plug into pulser for activation of code channel)
Pulser		
Data	Front Panel (Data In)	Coax (1)
Clock	Front Panel (Clock)	Coax (2)
64 KHz	Clock Driver	Coax (3)-hard-wired at driver
PN	PN Generator (PN 3)	Coax (4)
Output	Amplifier (In)	Coax (5)
8-Bit PN Generator		
Clock	Clock Driver	Coax (6)-Hard-wired at driver
E.O.S.	Pulser (CL)	Coax (2)
E.O.S.	Front Panel ($\overline{\text{Clock}}$)	Coax (7)
E.O.S.	Front Panel (Clock)	Coax (8)
PN 3	Pulser (PN)	Coax (4)
PN 4	Rear Panel (PN)	Coax (9)
64 KHz Crystal Oscillator	Clock Driver	Hard-Wired
Clock Driver	PN Generator (CL)	Coax (6)
	Pulser (64 KHz)	Coax (3) Hard-Wired at Clock Driver
	Rear Panel (64 KHz)	Coax (10)
Amplifier		
In	Pulser (output)	Coax (5)
Out	Pre-Transmission Filter (I_n)	Coax (11)
Pretransmission Filter		
In	Amplifier (Out)	Coax (11)
Out	Front Panel (Output)	Coax (12)

TABLE 8-4. RECEIVER MODULE INTERCONNECTIONS

Connections		Remarks
From	To	
Receiver Front-End		
(1) In	Front Panel (RF In)	Coax (1) Hard-wired at Panel
(2) Out	AGC Network (RF In)	Coax (2)
AGC Network		
(1) RF In	Receiver Front-End (Out)	Coax (2)
(2) SWC In	PN Gen/Polarity Sw. (Data In)	Coax (3)
(3) RF Out	SWTDL (In)	Coax (4) - 1 of 4 Devices coaxially connected
(4) TP-3	Rear Panel (AGC Bins)	Hook-up wire
PN Gen./Polarity Switch		
(1) SWTDL	SWTDL (Out)	Coax (5) 1 of 4 Devices coaxially connected
(2) Clock In	Rear Panel (CL)	Coax (6) Hard-wired at Panel
(3) Data In	AGC Network (SWC In)	Coax (3)
(4) Data Out	Re-Entry Delay Line (RF Input)	Coax (7)
(5) End of Seq	Rear Panel (End of Seq)	Coax (8) Hard-wired at panel
(6) End of Seq	CI Feedback Loop (Gate In)	Coax (9)
Re-Entry Delay Line		
(1) RF Input	PN Gen/Polarity Sw (Data Out)	Coax (7)
(2) Control Data In	CI Feedback Loop (Out)	Coax (10) Cable Length critical for proper Loop Delay
(3) Output "A"	CI Feedback Loop (RFIn)	Coax (11) Cable length is critical for proper delay
(4) Output "B"	Rear Panel (CH-B)	Coax (12) Hard-wired at Panel

TABLE 8-4. RECEIVER MODULE INTERCONNECTIONS (CONT)

Connections		Remarks
From	To	
SWTDL		
(1) In (1 of 4)	AGC Network (RF Out)	Coax (4)
(2) Out (1 of 4)	PN Gen/Polarity Sw (SWTDL)	Coax (5)
(3) +12 VDC (1 of 4)	Bias Board	Coax (13) Hard-wired at Bias Board
CI Feedback Loop		
(1) "A" Out	Rear Panel (CH-A)	Coax (14) Hard-wired at rear panel
(2) RF In	RF-Entry Delay Line (Output A)	Coax (11) Cable Length is critical for proper delay
(3) Gate In	Polarity Sw/PN Gen (End of $\bar{S}$)	Coax (9)
(4) Out	RF-Entry Delay Line	Coax (10) Cable length is critical for proper delay
(5) Gain Adj	Rear Panel (Trim Pot)	Coax (15) Hard-wired

TABLE 8-5. PROCESSOR MODULE INTERCONNECTIONS

Connections		Remarks
From	To	
Buffer Amp		
(1) "I" In	Coherent Demod ("I" Out)	Coax (1)
(2) "B" In	Rear Panel (CH-B)	Coax (2) Hard-wired at Panel
(3) "A" In	Rear Panel (CH-A)	Coax (3) Hard-wired at Panel
(4) AO	Amp (In)	Coax (4) Length critical for proper delay of signal
(5) BO	Amplifier Module (In)	Coax (5)
(6) IO	Contact (Relay S1)	Coax (6)
Wide Gate		
(1) In	Contact (Relay 52)	Coax (7)
(2) CL	Sampler (Out)	Coax (8)
(3) Out	Wiper (Relay 53)	Coax (9)
Sampler		
(1) In	Baseband PLL (Output)	Coax (10)
(2) Out	Wide Gate (CL)	Coax (8)
(3) Strobe	Data Reconstruction (Strobe)	Coax (11)
(4) Sampler Time Out	Wiper and Contact (Relay 53)	Coax (12) Hard-wired
64-MHZ VCXO		
(1) C.V.	Carrier PLL Assembly (C.V.)	Coax (13)
(2) 0^{o}	Carrier PLL Assembly (VCXO In)	Coax (14)
(3) Divider Output	Coherent Demod. (In)	Coax (15)
(4) 90^{o}	Carrier Ind. ($/90^{o}$)	Coax (16)

TABLE 8-5. PROCESSOR MODULE INTERCONNECTIONS (CONT)

Connections		Remarks
From	To	
Carrier PLL Assembly		
(1) Delay	Coherent Demod ("R" In)	Coax (17) Length critical to proper delay of signal
(2) VCXO In	64-MHz VCXO (0^{o})	Coax (14)
(3) 64 MHZ	Carrier Ind. (In)	Coax (18) Length Critical
(4) C.V.	64-MHz VCXO (C.V.)	Coax (13)
(5) Data In	Contact (Relay 53)	Coax (19)
(6) Error Voltage	Rear Panel (Trim Pot)	Coax (20) Hard-wired
Coherent Demodulator		
(1) "R"	Carrier PLL Assembly (Delay)	Coax (17) Length Critical
(2) In	64-MHz VCXO (Divider Output)	Coax (15)
(3) "I" Out	Buffer Amp ("I" In)	Coax (1)
Data Reconstruction		
(1) D.Cl	Front Panel (Clock)	Coax (21) Hard-wired at Panel
(2) Out	Front Panel (Data Out)	Coax (22) Hard-wired at Panel
(3) Strobe	Sampler (Strobe)	Coax (11)
(4) Data In	Wiper (Relay S1)	Coax (23)
(5) End of Seq.	Rear Panel (End of Seq)	Coax (24) Hard-wired at Panel
(6) Gated Out	Rear Panel (Gated Demod)	Coax (25) Hard-wired at Panel
Demodulator		
(1) Noise	Double Pulse Comp. (Noise)	Coax (26)
(2) Demod Out	Sync. Circuit (Demod)	Coax (27)
(3) In	Amp Module (Out)	Coax (28)
(4) Out	Contact (Relay S4)	Coax (29)

TABLE 8-5. PROCESSOR MODULE INTERCONNECTIONS (CONT)

Connections		Remarks
From	To	
Amp Module		
(1) In	Buffer Amp (BO)	Coax (5)
(2) 11	Wiper (Relay S2)	Coax (30)
(3) 7	Contact (Relay S2)	Coax (31)
(4) Out	Demodulator (In)	Coax (28)
(5) DP Out	Double Pulse Demod (In)	Coax (32) Cable Length critical
Carrier Ind		
(1) $\angle 90^{o}$	64 MHz VCXO (90^{o})	Coax (16) Critical Length
(2) In	Carrier PLL Assembly (64 MHz)	Coax (18) Critical Length
(3) Out	Lamp Driver Board	Coax (25) Hard wired at lamp driver board
Baseband PLL		
(1) Input	Wiper (Relay S4)	Coax (33)
(2) Ind. Out	Baseband Lock Ind. (Demod In)	Coax (34)
(3) Output	Sampler (In)	Coax (10)
(4) Output	Sync Circuit (CL)	Coax (35)
(5) Output	Baseband Lock Ind. (In)	Coax (36)
Baseband Lock Ind.		
(1) Demod In	Baseband PLL (Ind. Out)	Coax (34)
(2) In	Baseband PLL (Output)	Coax (36)
(3) Lamp	Lamp Driver Board	Coax (37) Hard-wired at lamp driver board

TABLE 8-5. PROCESSOR MODULE INTERCONNECTIONS (CONT)

Connections		Remarks
From	To	
Sync Circuit		
(1) Strobe	Rear Panel (End of Seq)	Coax (38)
(2) Demod	Demodulator (Demod Out)	Coax (27)
(3) PN	Rear Panel (64 KHz clock)	Coax (39)
(4) Sync	Lamp Driver Board	Coax (40) Hard-wired at lamp driver board
(5) CL	Baseband PLL (Output)	Coax (35)
Double Pulse Demod		
(1) Out	Double Pulse Comp (In)	Coax (41)
(2) Gate	Amp (Out)	Coax (42) Cable length is critical for proper delay
(3) In	Amp Module (DP Out)	Coax (32) Cable length is critical for proper delay
Amp		
(1) In	Buffer Amp (AO)	Coax (4)
(2) Out	Double Pulse Demod (Gate)	Coax (42) Cable length is critical for proper delay
Double Pulse Comp		
(1) In	Double Pulse Demod (Out)	Coax (41)
(2) In	Contact (Relay S1)	Coax (43)
(3) Out	Contact (Relay S4)	Coax (44)
(4) Noise	Demodulator (Noise)	Coax (26)
Lamp Driver Board	Baseband Lock Ind. (Lamp)	Coax (37)
	Carrier Lock Ind. (Out)	Coax (25)
	Sync Circuit (Sync)	Coax (40)

the identification designators on each module in the system. The number of the coax which connects these two points is shown in the third column. These tables only describe signal interconnections within each unit, all DC power is hardwired at each module and clearly marked as to the required voltage.

8.5 Module Locations and Adjustment Points

Figures 8-35, 8-36, and 8-37 are top and bottom views of the three surface wave breadboard units showing the location of all individual subassemblies and all internal adjustment points in the system. Those adjustments with asterisks after the call-outs will be the normal operational alignment adjustments. The other adjustments are one time settings which would be replaced with fixed components in a final system. Refer to system block diagrams in Figures 8-4, 8-12, and 8-18 for a functional description of the module interconnections in the system. Also, Table 8-6 is a list of all system adjustment points, the location, and a functional description of what each adjustment performs. The adjustment designations correspond to the callouts in Figures 8-35, 8-36, and 8-37.

8.6 Adjustment Procedure

The following procedures should be performed only after it has been determined from performance checks that the spread spectrum transceiver is not meeting specifications. This excludes the normal operation adjustments specified previously in this report.

The adjustment procedure sequence should start with the transmitter, proceed to the receiver, and finally include the signal processor. If any adjustment in this procedure cannot be made correctly, refer to individual circuit schematics before initiating troubleshooting. It is assumed the system is setup for operation and is warmed up, as specified in the acceptance test procedure, prior to start of the adjustment sequence. Refer to module interconnect tables and subassembly locating in the figures of this section for module output referenced in the alignment procedures.

8.6.1 Transmitter Adjustments

An oscilloscope and digital voltmeters is required for the following adjustments:

(a) With the transmitter in the PSK mode, connect connector thru 50 Ω coax to the oscilloscope (terminate in 50 Ω at scope). Observe a series of correlation peaks nearly equal in amplitude.

(b) Connect digital voltmeter to AGC bias point on rear of receiver section which shall indicate a DC voltage between +.5 VDC and +1.0 VDC.

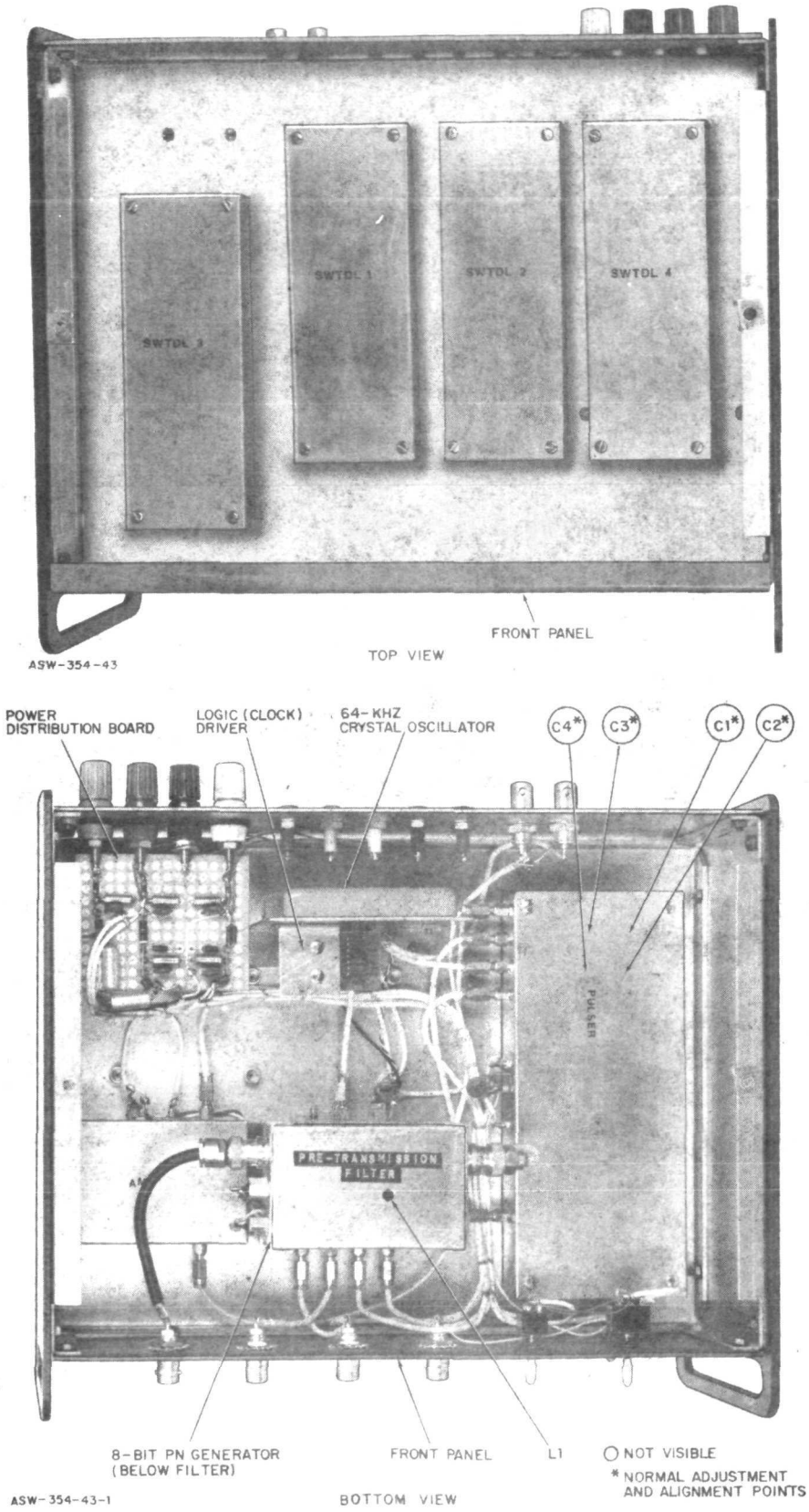


Figure 8-35. Transmitter Module Locations and Adjustment Points

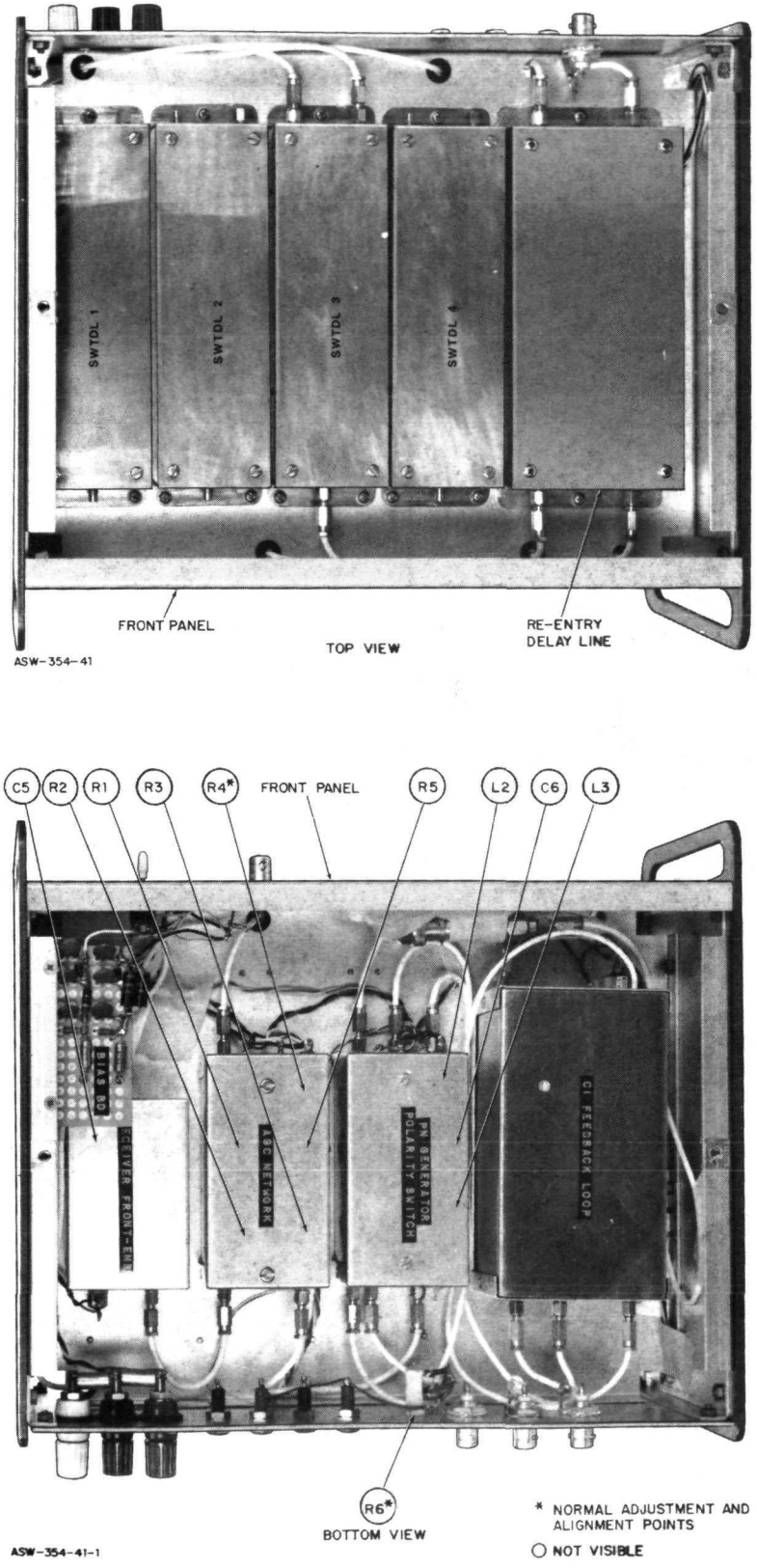
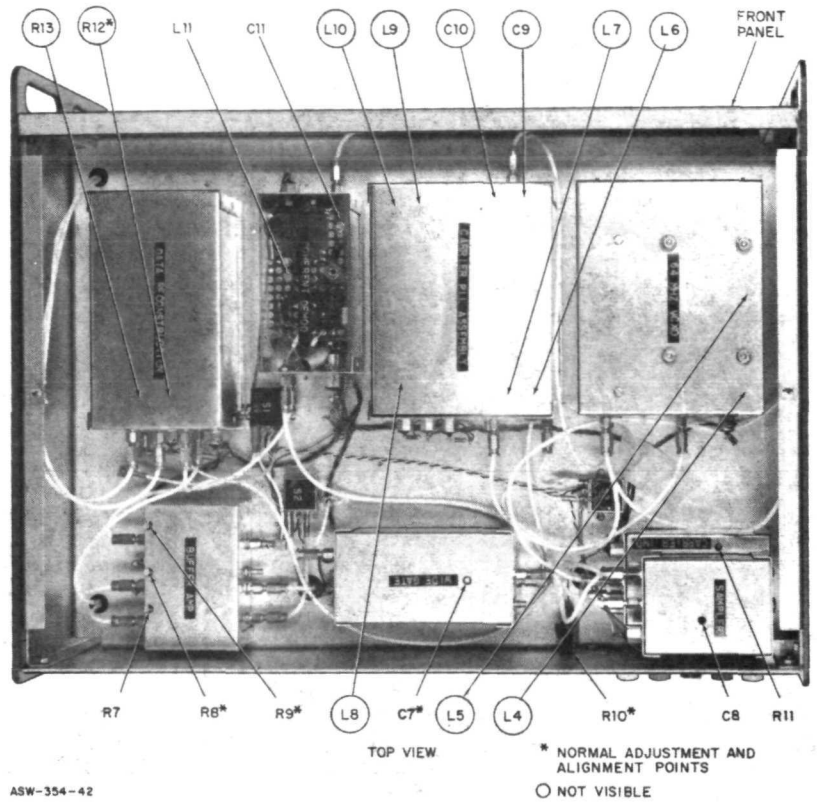


Figure 8-36. Receiver Module Locations and Adjustment Points



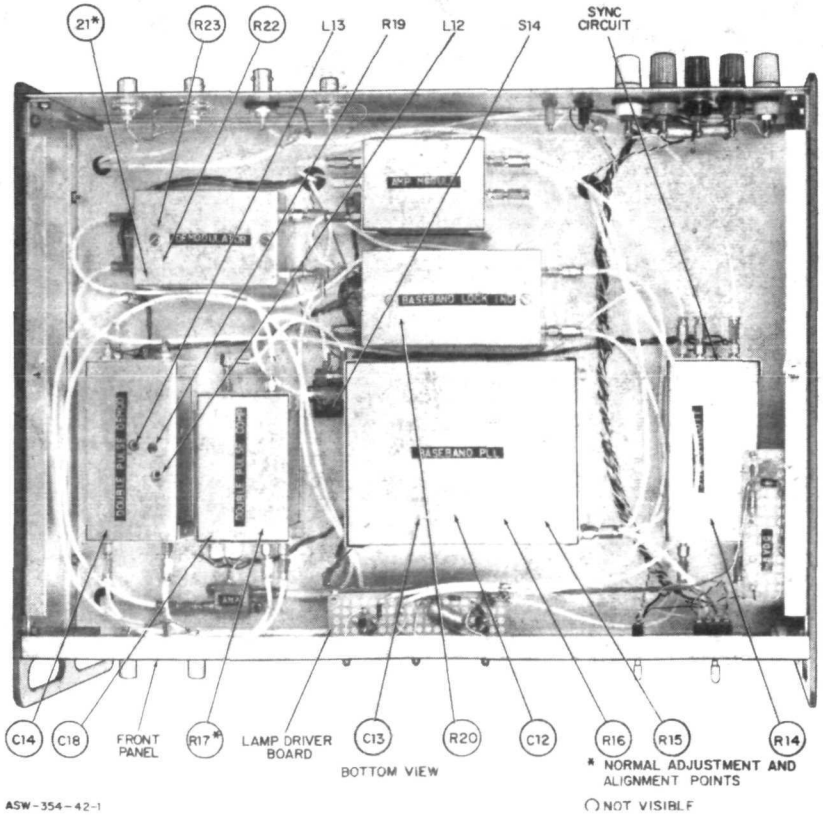


Figure 8-37. Processor Module Locations and Adjustment Points

TABLE 8-6. SYSTEM ADJUSTMENTS

Adj No.	Adjustment Designation	Location	Function
		TRANSMITTER (See Figure 8-36, Bottom View)	
1	C1, C2, C3, C4	Pulser Module	Adjusts the drive level and amplitude balance of the positive and negative pulses which excite the SWTDL.
2	L1	Pretransmission Filter	Variable inductor for peaking the transmitter output filter at 32 MHZ.
		Receiver (See Figure 8-37, Bottom View)	
3	C5	Receiver Front-End	Peaks input bandpass filter at 32 MHZ.
4	R1	AGC Network (Top Board)	Adjust bias current to not carrier diode detector.
5	R2, R3	AGC Network (Middle Board)	Adjusts noise voltage gain and offset.
6	R4, R5	AGC Network (Middle Board)	Adjusts AGC Loop gain and initial bias point on dual-gate FET's.
7	C6, L2, L3	PN Gen/Polarity Sw	Adjustments on frequency center and response for a 3-pole bandpass filter (BW -10 MHZ).
8	R6	Receiver (Back Panel)	Adjusts loop gain of Circulating Integrator.
		SIGNAL PROCESSOR (See Figure 8-38, Top View)	
9	R7, R8, R9	Buffer Amp	Adjusts the gain in three wideband buffer amplifiers.
10	C7	Wide Gate	Determines time out period of delayed 400 μs 1-shot.
11	C8	Sampler	Determines time-out period of delay.

TABLE 8-6. SYSTEM ADJUSTMENTS (CONT)

Adj No.	Adjustment Designation	Location	Function
SIGNAL PROCESSOR (See Figure 8-38, Top View (Cont)			
12	R10	Signal Processor (Rear Panel)	Adjusts carrier PLL error voltage.
13	R11	Carrier Ind.	Adjusts threshold where carrier lock indication is recognized.
14	L4, L5	64-MHZ VCXO	Variable inductors for peaking 64-MHZ signal which has been tripled from 21.33 MHZ.
15	L6, L7, L9, L10, C9, C10	Carrier PLL Assembly	Adjustments on response and centering of two 3-pole bandpass filters (BW-10 MHZ).
16	L8	Carrier PLL Assembly	Peaks single tuned 64-MHZ filter following frequency doubling.
17	C11	Coherent Demod	Adjust drive level to 64 MHZ ÷2 circuit.
18	L11	Coherent Demod	Peaks single-tuned 32-MHZ Filter following the ÷2 circuit.
19	R12, R13	Data Reconstruction	Sets the voltage slice level for the bit detectors.
20	R14	Sync circuit	Sets the voltage threshold for the sync detector.
SIGNAL PROCESSOR (See Figure 8-38, Bottom View)			
21	R15	Baseband PLL	Internal adjustment on 64-MHZ VCXO for centering IF. frequency response.
22	R16	Baseband PLL	Offset adjustment on loop integrator.

TABLE 8-6. SYSTEM ADJUSTMENTS (CONT)

Adj No.	Adjustment Designation	Location	Function
23	C12, C13	Baseband PLL	Adjusts Rise Times in Phase Detector switch driver.
24	R17	Double Pulse Comp.	Adjusts noise voltage offset to proper threshold for circuit operation.
25	R18	Double Pulse Comp.	Sets the gain of the noise voltage.
26	L12, L13, C14	Double Pulse Demod	Adjustments for filter response and centering (BW of filter = 10 MHZ).
27	R19	Double Pulse Demod	Adjusts LO drive level to double-balanced product detector.
28	R20	Baseband Lock Ind.	Adjusts threshold where 64-KHZ lock is recognized.
29	R21	Demodulator	Sets current bias level in Hot carrier detector.
30	R22	Demodulator	Adjust noise voltage off-set to proper threshold for circuit operation.
31	R23	Demodulator	Sets the gain of the noise voltage.

(c) Adjust C1 and C2, individually, to obtain a near equal peak-to-peak amplitude on the correlation peaks. (Note: these adjustment effect the drive level of the positive and negative pulses, respectively.)

(d) The AGC voltage should be at a minimum for the best drive level which corresponds to the highest signal level at the transmitter output.

(e) Switch transmitter to DOUBLE PULSE mode and observe on oscilloscope two closely spaced correlation peaks occuring once every 15.6 μs. Adjust C3 and C4 to match the amplitude of these correlation peaks with the PSK mode correlation peaks.

(f) Balance these adjustments for both data states at the transmitter to insure equal amplitude correlation peaks for either positive or negative pulses in both correlation signals.

8.6.2 Receiver Adjustments

A digital voltmeter is required to perform the following adjustment procedure:

(1) Set system in PSK mode.

(2) Connect the digital voltmeter to the AGC bias point and adjust R4 until the voltage is +0.5 VDC. This level is based on an input signal power of -60 dBm.

(3) Set the receiver input S/N at -15 dB using the acceptance test procedure for processing gain.

(4) Switching the noise at the receiver input in and out, adjust R3 such that the variation in the AGC voltage (between -15 dB S/N and signal only) is less than 40 mV.

(5) Repeat steps (2) or (3) to correct for variations due to R3 adjustment.

8.6.3 Signal Processor Adjustments

There are six major adjustments at the signal processor which include; buffer amplifiers (R8, R9), wide gate (C7), sampler 1-shot (C8), sync circuit threshold (R14), double-pulse comparator threshold (R17), and demodulator threshold (R21). Perform these adjustments in the following order:

(a) Buffer Amplifier Adjustments

(1) Connect a signal generator (HP606 or equivalent) to the input of channel B with a center frequency set at 32 MHz.

(2) Adjust gain of wideband amplifier to 20 dB (X10) by using trim pot R8.

(3) Connect oscilloscope to "data in" at data reconstruction circuit.

(4) Adjust gain with R9 such that the demodulated buildup in the PSK mode matches the buildup in the Double Pulse mode.

(b) Wide Gate Adjustment (PSK Mode)

(1) Connect "data in" terminal to oscilloscope through 50 Ω Coax (terminated at the scope).

(2) Adjust C7 to center the delayed 1-shot around the correlation rf signal.

(c) Sampler Adjustment (Double Pulse mode)

(1) Display simultaneously on the oscilloscope the 80-ns strobe and the demodulated baseband data (located at "data in" of data reconstruction circuit).

(2) Adjust C8 to position the 80-ns pulses on the peaks of the envelope detected correlation signal.

(d) Sync Circuit Adjustment (PSK Mode)

Refer to Section 5.0, Sync Analysis, for instructions on setting the threshold voltage. R14 performs the adjustment.

(e) Double-Pulse Comparator Adjustment (Double Pulse Mode)

(1) Connect the double-pulse comparator output to the oscilloscope. Observe a series of baseband 400 mV pulses spaced every 15.6 μs.

(2) With the receiver input S/N ratio at -15 dB, adjust R17 to include as many pulses as possible before the pattern begins to "tear-up". Over an 8-bit, 125 μs interval this should be approximately 6 of the 8 possible pulses. Disregard noise spikes between correlation pulses as they are non-coherent and will be integrated out by the 64-kHz baseband PLL.

(f) Demodulation Adjustment (PSK Mode)

(1) Connect output marked OUT through 50 Ω coax to the oscilloscope, and terminate into 50 Ω at scope.

(2) Adjust R21 to obtain the same results described in (e), double-pulse comparator adjustment.

Appendix A

SWTDL CODE CORRELATION PROPERTIES

Operation of the system is based primarily on the Surface Wave Tapped Delay Lines (SWTDL), and good performance depends most heavily on their design, quality, and compatibility with the supporting electronics. The link transmitter encodes 8-kHz data signals into 8-MHz wideband signals, and the receiver SWTDL's must extract the data from the noise and undesired signals.

The breadboard system will have four addresses, each selected by insertion of appropriate mated SWTDL pairs (one in the transmitter and one in the receiver). Four mated pairs of SWTDL's have been designed to generate signals with good cross-correlation characteristics and have been carefully fabricated to provide nearly theoretical signal detection in the system. Packaging has been designed to provide easy interchangeability for address selection.

1. CROSS-CORRELATION IN THE SWTDL MATCHED FILTERS

The SWTDL impulse response, continuously repeated to form the transmitted signal, is a 15.6 μs burst of a 32-MHz sine wave which is phase shift keyed by a PN code at an 8-MHz chip rate. The degree of similarity of the four addresses is determined by the cross-correlation characteristics of the PN codes used in the SWTDL construction. Four 127-chip linear maximal sequences were chosen and used to design the four matched pairs of SWTDL's.

Figure 1 shows the single impulse response correlation signals which resulted from using the SWTDL's fabricated for the breadboard system.

Four separate oscillograms are shown in Figure 1, each containing the image of five signals. The first trace (top) in each photograph is the SWTDL output when a single impulse response from the correct transmitter SWTDL is received. The second trace is the output when the correct transmitter SWTDL generates a single impulse response, but with a negative time argument. The third, fourth, and fifth signal traces are the receiver SWTDL output when single impulse responses of each of the other three addresses are received.

The single impulse response of a SWTDL is normally designated as $h_i(t)$ where "i" identifies the device (see Figure 2(a)). The cross-correlation of the impulse responses of two SWTDL's is designated as $\theta_{ij}(\tau$, where "i" identifies one device, "j" identifies the second, and "τ" designates the time relationship between the impulse responses. The cross-correlation is an even function, amplitude modulated, RF signal, 31.2 μs in duration. See Figure 2(b). The properties of $\theta_{ij}(\tau)$ can be observed in the oscillograms of Figure 1.

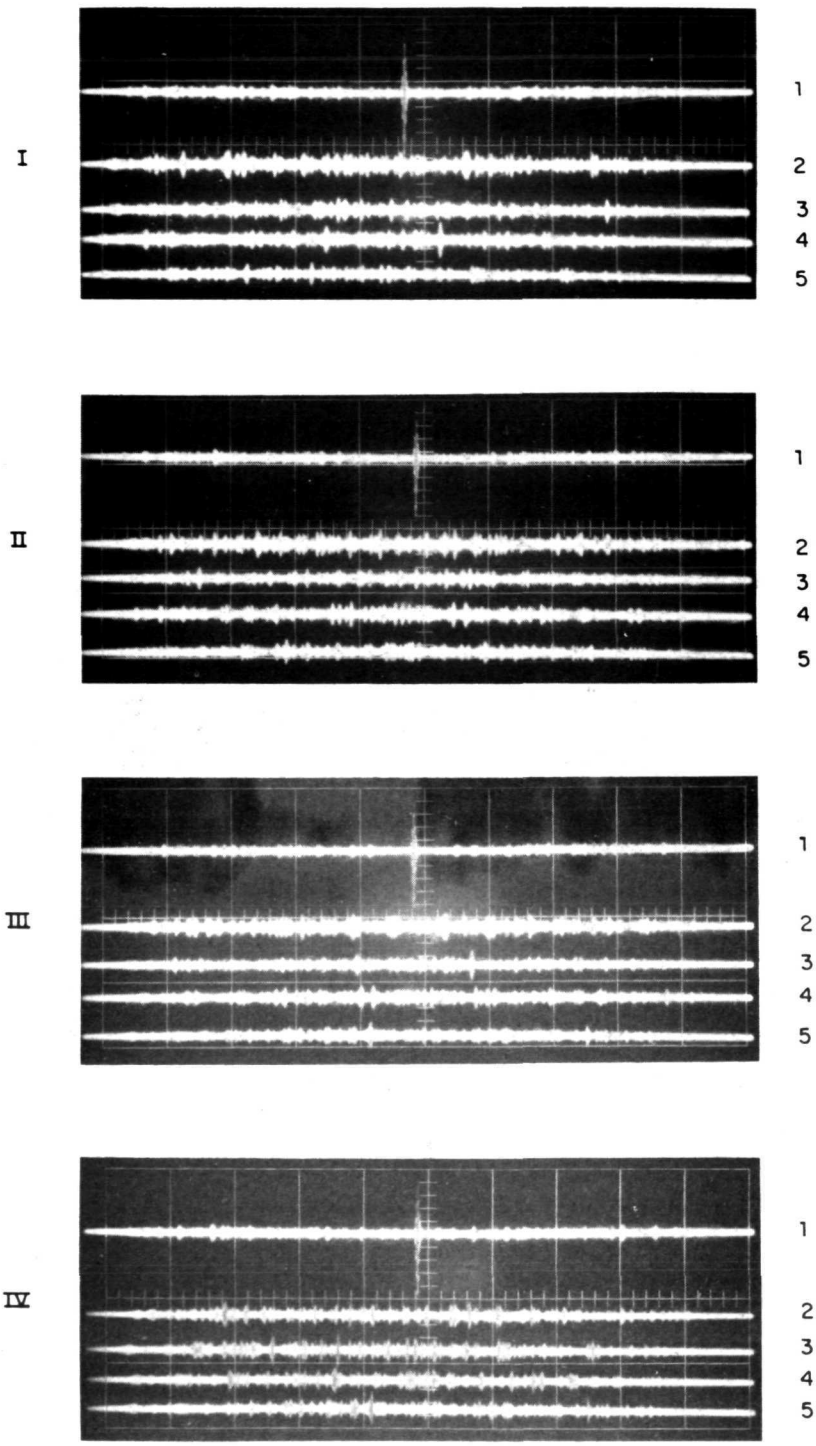


Figure 1. Transmission Signal Cross-Correlations

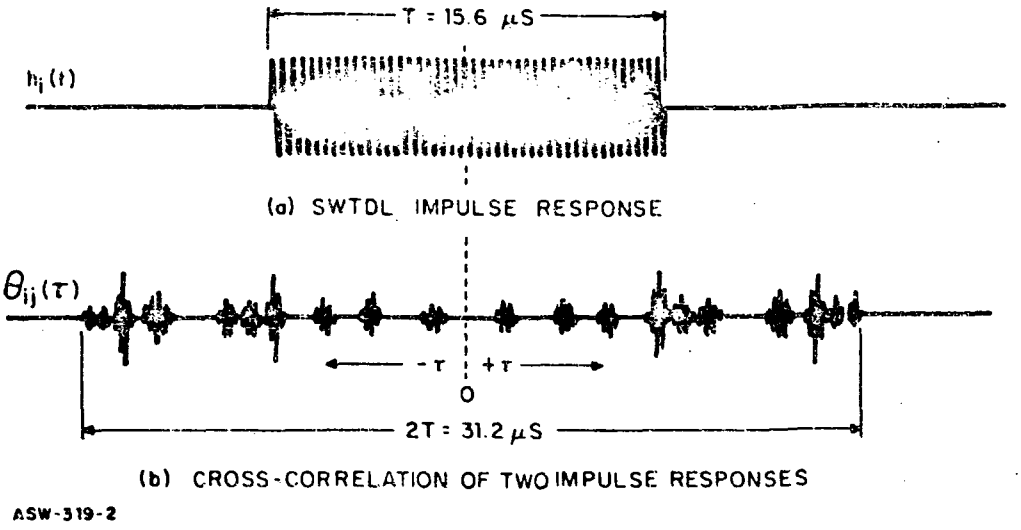


Figure 2. SWTDL Impulse Responses

During system operation, the SWTDL's used to generate the signal are pulsed at a rate adjusted so that the output is a constant envelope signal. Since the polarity of the SWTDL impulse response is reversed when the driving pulse is negative, the transmitter output is a repeated series of 15.6 μs impulse responses, $h_i(t)$, with the polarity alternating in a pseudorandom manner. This signal is expressed as a summation:

$$s_i(t) = \sum_{k=-\infty}^{+\infty} \alpha_k \, h_i(t-T) \qquad (1)$$

where: $\alpha_k = \pm 1$

When the continuous envelope signal $s_i(t)$ is correlated with a second impulse response signal $h_j(t)$, the output is defined as a series of four different finite duration correlation functions $\left(\theta_{ij}^{++}(\tau), \theta_{ij}^{--}(\tau), \theta_{ij}^{+-}(\tau), \theta_{ij}^{-+}(\tau)\right)$, distributed in a pseudorandom fashion as shown in Figure 3.

These finite duration correlation functions which make up the total correlation of the continuous envelope signal with the truncated signal are directly related to the correlation function of two truncated signals as shown in Figure 2.

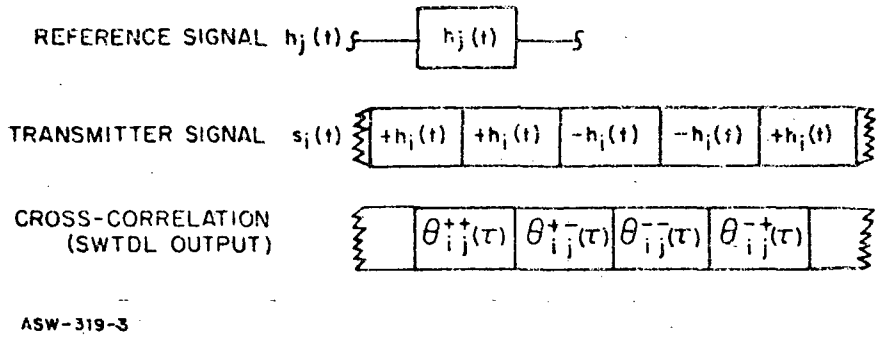


Figure 3. Cross-correlations Resulting From a Continuous Envelope Signal

$$\theta_{ij}^{++}(\tau) = \left[\theta_{ij}(\tau) + \theta_{ij}(\tau-T)\right] \tag{2}$$

$$\theta_{ij}^{+-}(\tau) = \left[\theta_{ij}(\tau) - \theta_{ij}(\tau-T)\right] \tag{3}$$

$$\theta_{ij}^{--}(\tau) = \left[-\theta_{ij}(\tau) - \theta_{ij}(\tau-T)\right] \tag{4}$$

$$\theta_{ij}^{-+}(\tau) = \left[-\theta_{ij}(\tau) + \theta_{ij}(\tau-T)\right] \tag{5}$$

where:

$$0<\tau<T$$

The correlation functions reduce to two complementary pairs:

$$\theta_{ij}^{++}(\tau) = -\theta_{ij}^{--}(\tau)$$

$$\theta_{ij}^{+-}(\tau) = -\theta_{ij}^{-+}(\tau) \tag{6}$$

The autocorrelation for the continuous envelope signal without phase changes has a magnitude of one for linear maximal sequences:

$$\theta_{ii}^{++}(\tau) = \left[\theta_{ii}(\tau) + \theta_{ii}(\tau-T)\right] = -1 \tag{7}$$

It follows that:

$$\theta_{ii}(\tau-T) = -\left[\theta_{ii}(\tau)+1\right] \tag{8}$$

The autocorrelation for reversed sign continuous envelope signals reduces to:

$$\theta_{ii}^{+-}(\tau) = -\left[2\theta_{ii}(\tau)+1\right] \tag{9}$$

2. CROSS-CORRELATION AND THE CIRCULATING INTEGRATOR

The Circulating Integrator (CI) is a re-entry delay line used in the system to increase the processing gain without using SWTDL's with excessively long propagation lengths (see Quarterly Report of March 10, 1971). It consists of an 8-bit PN generator, a balanced modulator, and a unity gain feedback delay line with a delay of T seconds (see Figure 4). The output of the SWTDL is a series of cross-correlation signals, as defined earlier, and is shown in Figure 5.

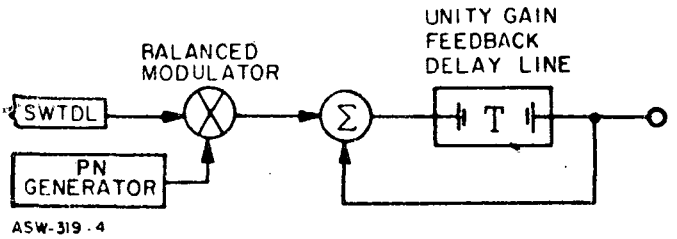


Figure 4. Circulating Integrator

The balanced modulator, controlled by the PN generator, reverses the phase of the correlations to the delay line at T second intervals; the direct and the delayed signals are summed at the input to the delay line. Figure 5 shows how the correlation signals accumulate at the delay line input when the PN generator switches at the beginning of each correlation signal. After a time equal to 8(T), the delay line feedback loop is opened preventing further buildup of the signal.

Using Equation (6), the final input to the delay line $\theta_{CI}(\tau)$ is written:

$$\theta_{CI_{ij}}(\tau) = 4\left[\theta_{ij}^{++}(\tau) + \theta_{ij}^{+-}(\tau)\right] \tag{10}$$

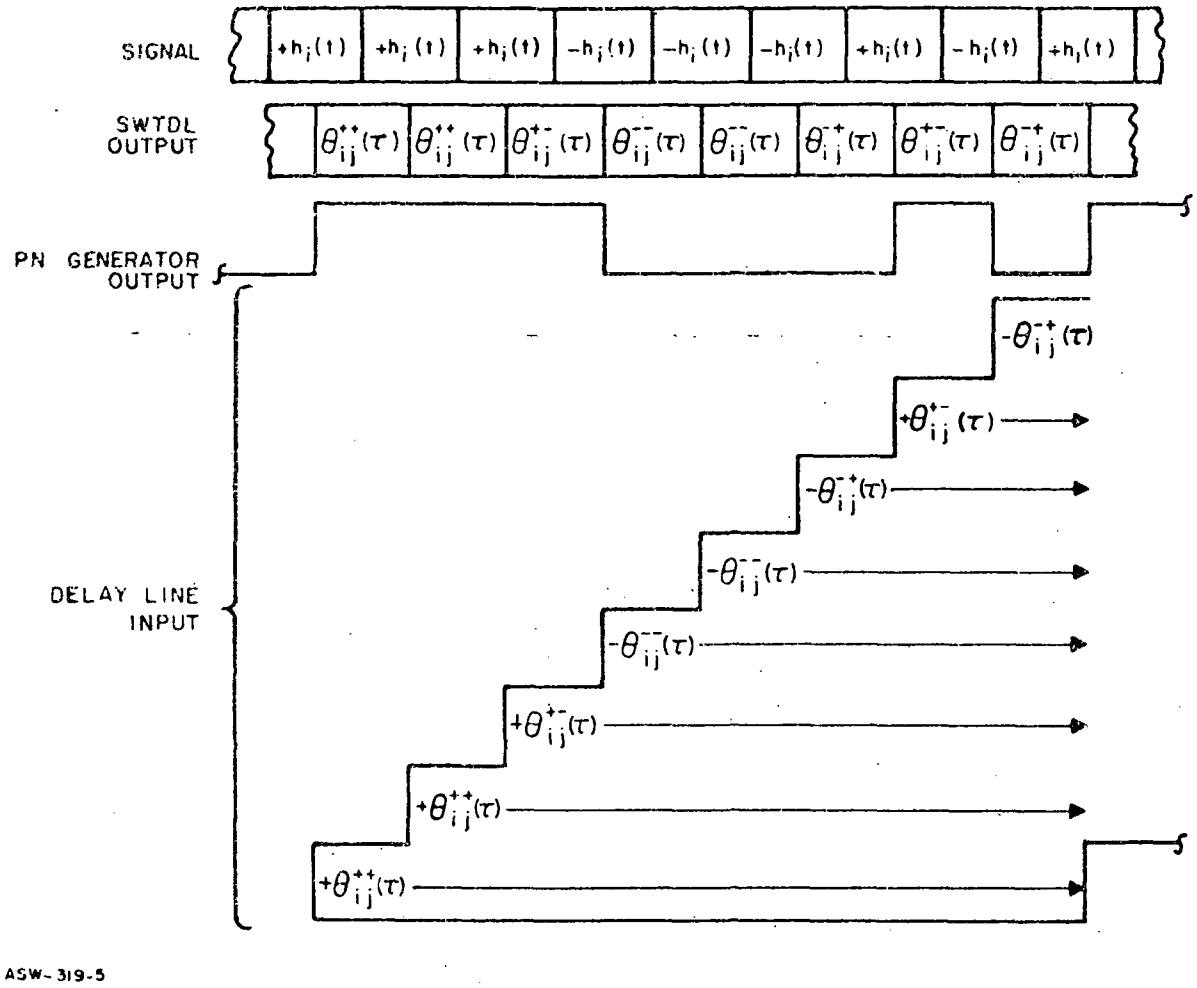


Figure 5. Cross-correlation Signals Into Circulating Integrator Delay Line

This is reduced in terms of the truncated correlation function equations (2) to (5):

$$\theta_{CI_{ij}}(\tau) = 8\left[\theta_{ij}(\tau)\right] \qquad \text{where} \quad 0<\tau<T \tag{11}$$

This was calculated for the special case where the PN sequence generation switches at the $\tau = 0$ point of the SWTDL correlation outputs. This special case was chosen for explanation purposes, but the results are the same for the general case where the PN generator shifts at any value of τ.

When the correct signal enters the SWTDL, the CI output is

$$\theta_{CI_{ii}}(\tau) = 8\left[\theta_{ii}(\tau)\right] \qquad \text{where} \quad 0<\tau<T \tag{12}$$

The following important result shows that the ratio of the CI output with correct and incorrect continuous input signal is simply:

$$\frac{\theta_{CI_{ii}}(\tau)}{\theta_{CI_{ij}}(\tau)} = \frac{\theta_{ii}(\tau)}{\theta_{ij}(\tau)} \tag{13}$$

It has thus been demonstrated that the response of a perfect Circulating Integrator to the correlations of a repeating series of phase reversed impulse responses is precisely equal to the correlation of a single impulse response. This fact allows the correlations properties of the complete receiver to be studied simply by studying the correlation properties of single impulse responses like those shown in Figure 1.

These results also indicate that improved system correlation properties are achievable if an array of SWTDL's is used to generate and detect the signal so that the transmissions will consist of a series of different impulse responses rather than one response repeated with phase reversals. This end could be achieved without an excessive increase in system complexity.

Appendix B

NOISE COMPENSATING AGC

It is important to the operation of the demodulator that the desired signal power be maintained at a constant level while the total input power (signal plus noise) varies due to fluctuating noise levels. Since this system is designed to operate with input signal-to-noise ratios of -15 dB or higher, any AGC which operates from the envelope detected input signal will essentially maintain a constant noise level and the desired signal power will increase about 1 dB for every dB decrease in S/N ratio.

The peak-following AGC circuit shown in Figure 1 reduces the signal power fluctuations which result from varying signal-to-noise ratios at the input.

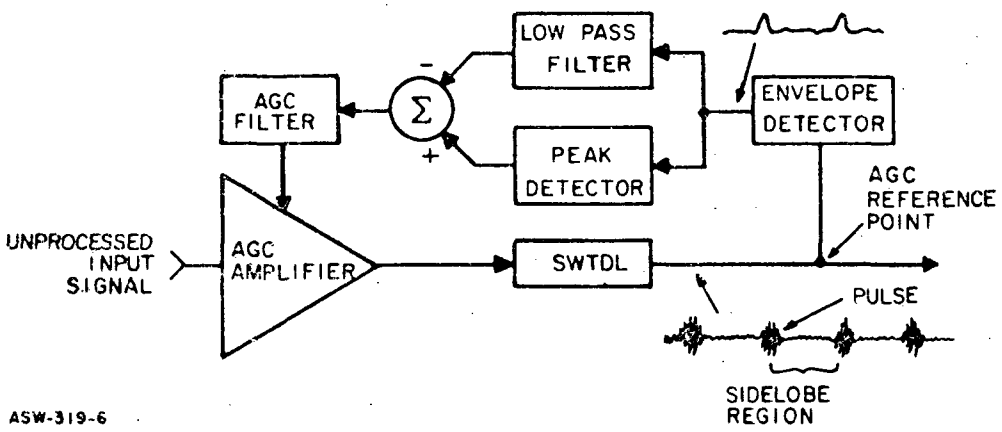


Figure 1. Noise Compensating AGC, Block Diagram

The SWTDL output is an amplitude modulated RF signal containing distinctly detectable pulses which represent the signal energy plus a small component of noise. The nearly constant RF sidelobe region represents primarily noise and a very small component of signal. Since the pulse width is less than one percent of that of the sidelobe region, the average of the envelope detected SWTDL output is essentially the average absolute value of the sidelobes. Both the average envelope detected output and the peak detected output from the SWTDL increase as a function of noise power for a given signal power. The functions have properties such that the difference between the "scaled" low pass filter output and the peak detector output with a given signal power is constant for all signal-to-noise ratios greater than -15 dB.

Since the AGC circuit shown in Figure 1 maintains this difference at a preset level by adjusting the front end gain, it holds the desired signal nearly constant while the noise power varies.

Preliminary experimental data indicates that the AGC circuit shown in Figure 1 holds the desired signal power fluctuations to less than one dB over input signal-to-noise ratios ranging from +20 dB to -15 dB.

Appendix C

NOISE COMPENSATED DEMODULATOR

The noise compensated demodulator (located at the Circulating Integrator output) detects the envelope of the correlation peaks and converts these successively increasing amplitude signals into a series of constant amplitude pulses for driving the baseband Phase Lock Loop (PLL). On the bench model, the baseband envelope of the Circulating Integrator output had been applied directly to the 64-kHz PLL resulting in poor loop tracking performance in low S/N. This was caused primarily by loop bandwidth and damping factor variations due to the varying input signal amplitude.

An improved demodulator has been designed (see Figure 1) which provides a constant amplitude baseband pulse stream and a better output S/N performance in a high noise environment. In essence, the comparator voltage threshold used to determine the presence (or absence) of a signal is a variable which tracks the increasing noise amplitude out of the Circulating Integrator. This is possible since the signal energy represents less than one percent of the total energy in the demodulator output. An accurate indication of the noise power may be determined by integrating this envelope detector in the 8-kHz data rate bandwidth. At the output of the offset amplifier, the voltage threshold provided to the voltage comparator consists of a DC component plus a signal which increases over each 125 μs interval corresponding to a data bit interval.

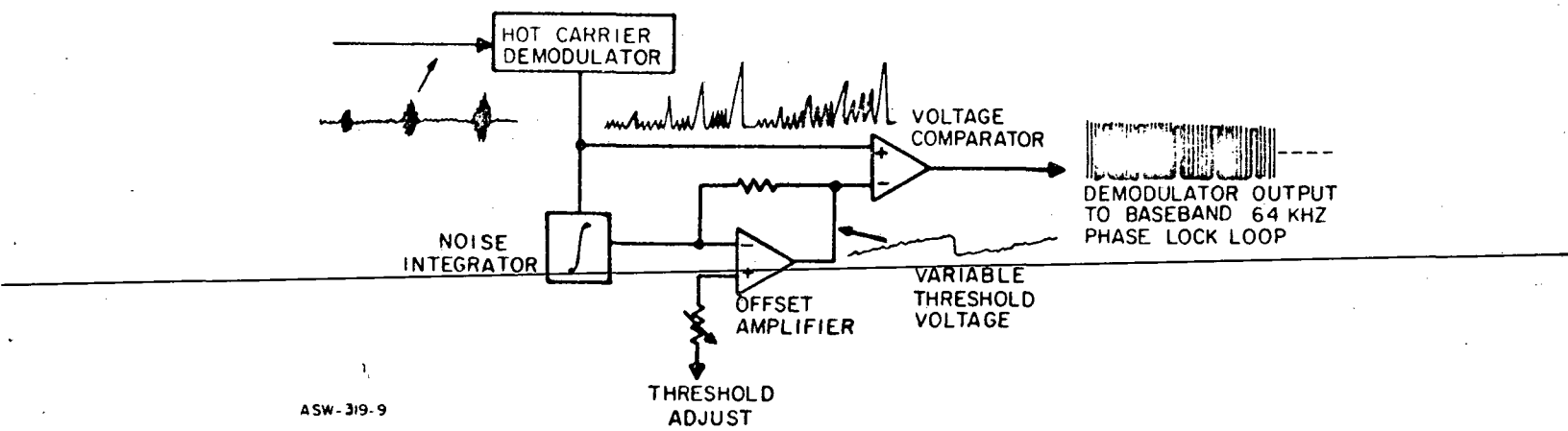


Figure 1. Noise Compensated Demodulator

Laboratory tests conducted on the demodulator indicate a 5 dB S/N improvement over a fixed threshold comparator. The constant amplitude pulses at the comparator output also provide a significant margin of improvement of the baseband PLL performance in a -15 dB S/N environment.

Appendix D

CIRCULATING INTEGRATOR LOOP GAIN

The Circulating Integrator (CI) assembly used in the receiver is shown in block diagram form in Figure 1. It consists of the ST-cut quartz delay line, two active matching networks, a power summer and a gated RF amplifier in the feedback loop. Since the linear summation of successive correlation peaks in the RF domain requires a positive feedback mechanism, it is important to minimize loop gain variations.

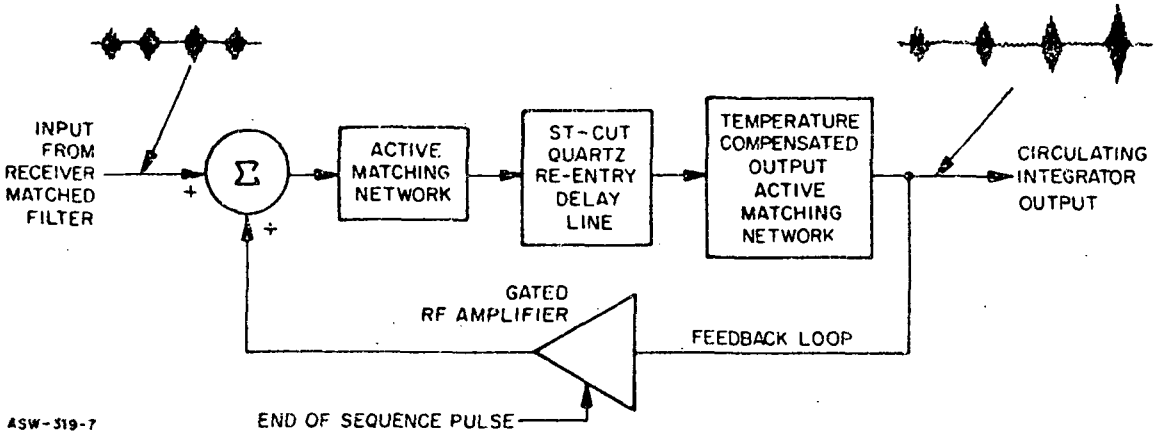


Figure 1. Circulating Integrator Assembly, Block Diagram

Gain variations (due primarily to temperature effects in the active devices) are compensated in the output active matching network. Using a simple thermistor bias control on a dual-gate FET, loop gain variations were held to within ±0.5 dB over a $0^{o}C$ to $70^{o}C$ temperature range.

The effects of gain variation (due to temperature change) in the Circulating Integrator output can be seen by solution of the series expression of its transfer function.

Let (n) equal the number of circulations in the Circulating Integrator, and let (x) equal the gain variations from unity in the loop. Normalizing the input signal to (1), the output at the end of (n) circulations (S_n) is

$$S_n = \sum_{K=1}^{n} (1+X)^K \qquad (1)$$

This is written as

$$S_n = \frac{(1+X)}{X}\left[(1+X)^n - 1\right] \qquad (2)$$

which is approximated by

$$S_n = (1+X)\left[n + \frac{n(n-1)X}{2!} + \frac{n(n-1)(n-3)X^2}{3!} + \ldots\right] \qquad (3)$$

This series approximation represents the signal level at the end of (n) circulations for various loop gains in the Circulating Integrator.

Figure 2 is a family of curves showing the amplitude of the last circulation in the Circulating Ibtegrator as a function of both the number of circulations and of various values of loop gain (as expressed by equation (3)). As seen in Figure 2, a gain variation of ±.05 (±0.5 dB) results in a ±15% (±1.25 dB) variation in the output amplitude of the Circulating Integrator.

The results bring out two important facts regarding stability which were considered in the Circulating Integrator design. First, under worst-case conditions the loop gain should not exceed unity by more than one dB to insure a near linear amplitude build-up. Secondly, for a large number of circulations, a greater amplitude fluctuation results for small loop gain variations which would indicate a practical upper limit to the number of circulations.

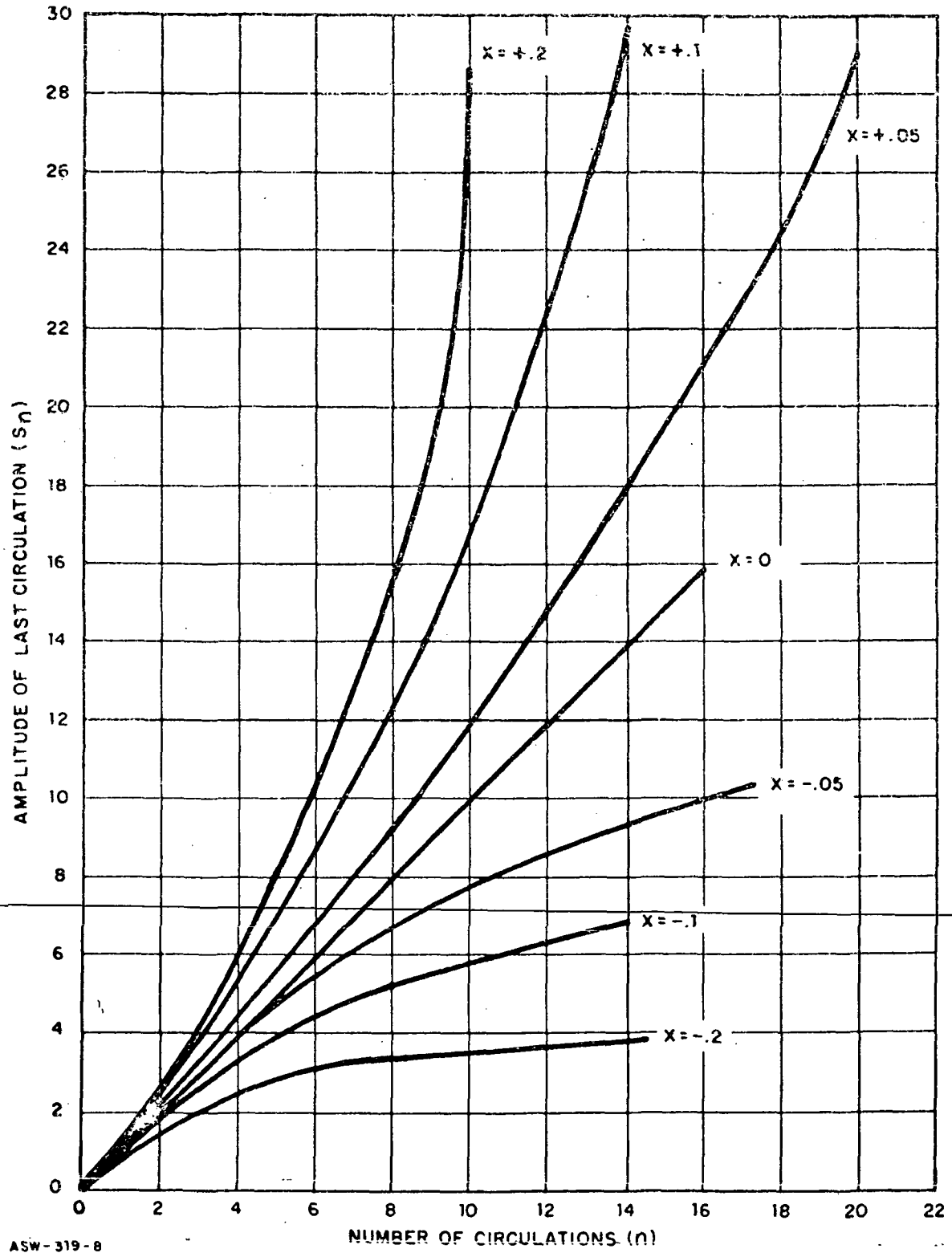


Figure 2. CI Amplitude Versus Gain

Appendix E

DATA RECONSTRUCTION CIRCUIT

The design of the data reconstruction circuit is based upon optimum decision procedures for wideband signals in band-limited Gaussian white noise. This primarily involves a sampled threshold decision following the matched filter and the demodulator. For equal energy anti-podal baseband signals and equal "a priori" probabilities, the optimal one-zero bit detector consists of a sampled comparator with a zero volt slicing level. The optimum sampling time is the instant the correlation peak reaches a maximum.

A block diagram of the new data reconstruction circuit is shown in Figure 1. The incoming signal is split and applied to two balanced mixers used as RF gates which pass only the baseband pulses corresponding to the eighth (final) circulation in the Circulating Integrator. The polarity of one of the two pulses is inverted, and two strobed comparators sample the peaks of the two pulses. The state of the output flip-flop is determined by whichever signal exceeds zero volts during the strobe gate time. If the pulse build-up out of the demodulator is positive (indicating that a logical "1" was transmitted), the flip-flop is set. A negative build-up (logical "0" transmitted) causes the output flip-flop to reset.

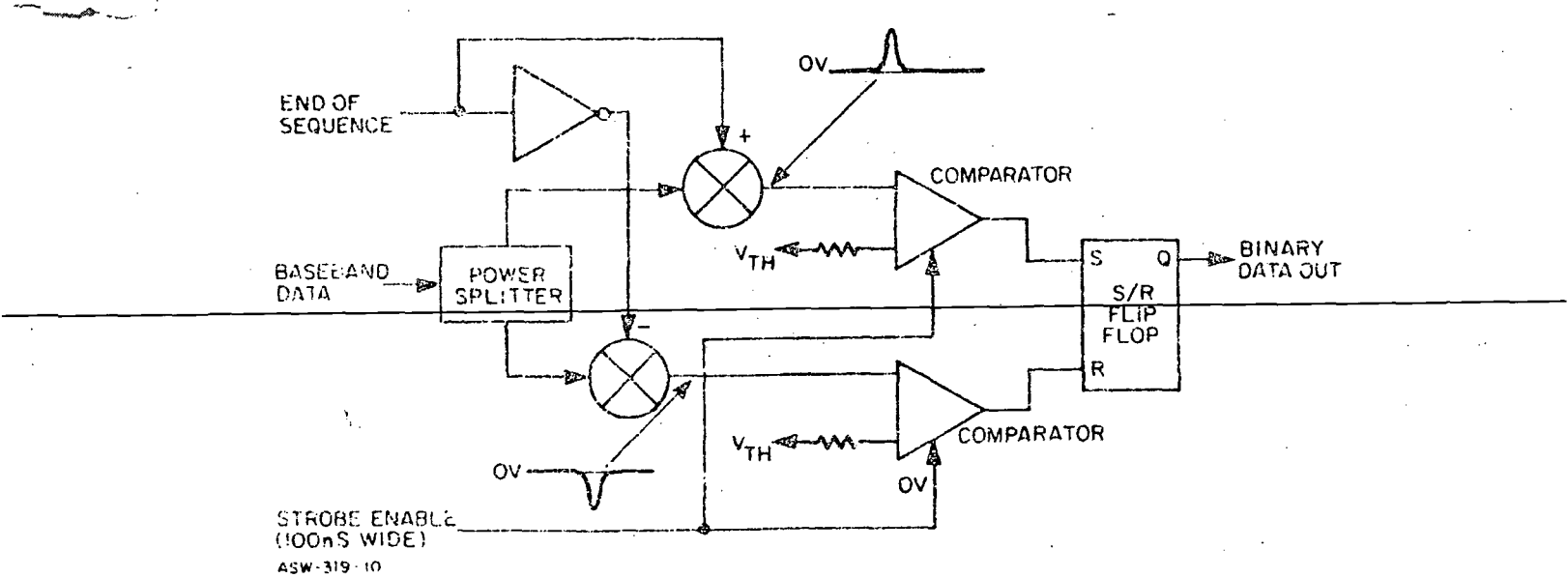


Figure 1. Data Reconstruction Circuit