

**ANALOG TREE-ORGANIZED
MULTI PLEXER**

**CASE FILE
COPY**

Quarterly Technical Report No. 1

November 5, 1971

JPL Contract No. 953117

(Subcontract under NASA Contract NAS7-100)

(Task Order No. RD-4)

Prepared by

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ERRATA SHEET FOR TEXAS INSTRUMENTS

REPORT NO. 03-71-95

<u>Page</u>	<u>Correction</u>
9	In third paragraph, change Table II to Table I.
10	In third paragraph, change ATOM to atom.
18	"± 3 V peak-to-peak" is a measurement condition for Crosstalk. "I _{on} = 1 mA" is a measurement condition of Input Current.
20	In figure 8, add an equals sign between 10.5 V and V _{PO} .
27	There should be spaces between 10 K and C _S , 100 K and C _L , 25 K and C _{drive} .
30	In last line, R _S (C _S + C _L) should be R _L (C _S + C _L). In figure 17, change C _{RD} to C _{DR} .
34	In first part of Equation 26, add t _c to the denominator.
35	In second paragraph, change Equation (29) to (28).
37	Omit "all devices.....geometry" in figure 37.

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TECHNICAL CONTENT STATEMENT

This report contains information prepared by Texas Instruments Incorporated under JPL subcontract. Its content is not necessarily endorsed by the Jet Propulsion Laboratory, California Institute of Technology, or the National Aeronautics and Space Administration.

ABSTRACT

This report describes the design of an Analog Tree-Organized Multiplexer (ATOM) which is intended for use in the telemetry system of an interplanetary space craft. The ATOM will be fabricated by a monolithic, dielectric isolation process, and will contain silicon junction field-effect transistors (JFET) as the active elements.

A theoretical analysis of the effect of the radiation environment described in JPL Specification No. CS505479A on the performance of the ATOM is described. The analysis indicates that the expected radiation environment will cause only minor changes in the preradiation characteristics of ATOM.

The design of the JFET in the ATOM to meet the electrical requirements in JPL Specification No. CS505479A, when fabricated by either the double poly-dielectric isolation process or the raised dielectric isolation process, is described. The effect of the heat treatment required for the dielectric isolation process on the diffusion profile of the JFET is described.

The layout of the ATOM circuit for fabrication by either the double poly or raised dielectric isolation process is also described.

The raised dielectric isolation process is recommended by Texas Instruments to be used in fabricating the ATOM. The final selection of the fabrication process will be made by JPL.

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SECTION I

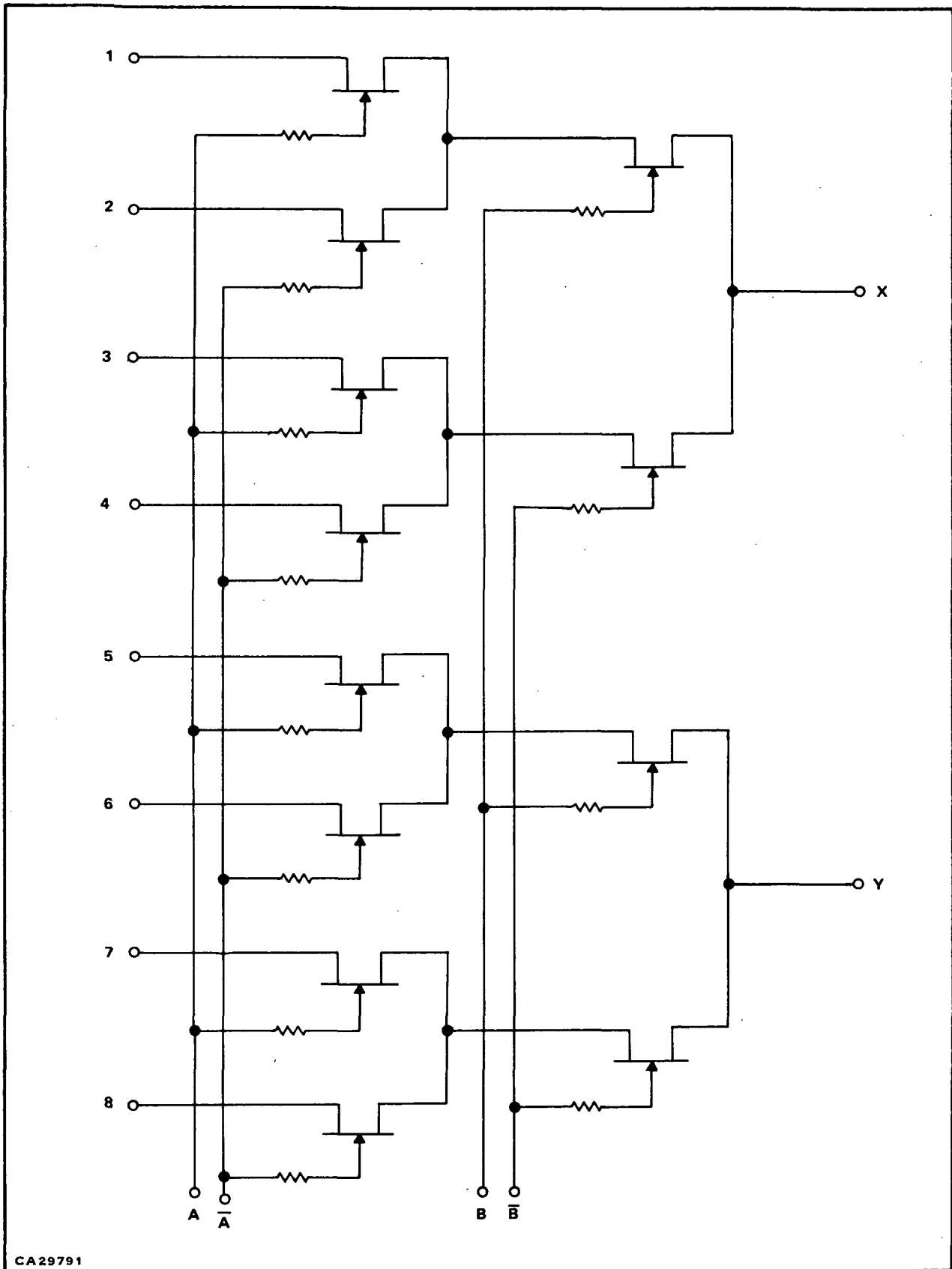
INTRODUCTION

The purpose of this contract is the design, fabrication, and electrical testing of the Analog Tree-Organized Multiplexer (hereafter referred to as ATOM), illustrated in Figure 1. The dual four-channel ATOM is intended for use in the analog data-sampler (multiplexer) section of the measurement processor (telemetry) subsystem of an interplanetary space craft. The measurement processor is required to have a useful life up to 12 years for outer-planet missions. The assigned design priorities which correspond to this mission are reliability, electrical performance, simplicity of fabrication process, and cost. The multiplexer may consist of up to 1000 channels, which would be achieved by pyramiding ATOM switches. Ten levels of tree switching (the ATOM contains two levels), containing 171 ATOMs, make a 1024-channel multiplexer.

The results of a study of the radiation environment specified by JPL Specification No. CS505479A on the ATOM are included in this report. The specified radiation environment is expected to have a minor effect on the preradiation characteristics of the ATOM.

The ATOM circuit illustrated in Figure 1 will be fabricated on a monolithic, dielectrically isolated, silicon bar and will have gold beam-lead connections to the outside world.

This report describes the design and layout of the ATOM for fabrication by either the double poly-dielectric isolation process or a raised dielectric isolation process. The final fabrication process selection will be made by JPL.



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Figure 1. ATOM Circuit Configuration

SECTION II

RADIATION EFFECTS STUDY

A. INTRODUCTION

This section describes the results of a theoretical study of radiation effects on the junction field-effect transistor which will be used as the active device in the ATOM.

B. RADIATION ENVIRONMENT

The radiation environment assumed for this study is described in Table II of JPL Specification CS505479A; this radiation-environment description is included here, for completeness, as Table I.

1. Shielding Considerations

In Section 3.9.6 of JPL Specification CS505479A, the following statement appears:

Aluminum in the range of 0.015 to 0.5 inch thickness shall be assumed to be representative of the amount of shielding provided by the housing and by materials within the housing.

In accordance with this statement, a preliminary estimate was made of the effect of such shielding on the electron and proton fluence spectra. The results of this estimate are shown in Figure 2. Here, the unshielded proton and electron spectra are compared with the spectra modified by shielding having the two extreme values of thickness, 0.015 and 0.5 inch. The modified spectra were obtained, point by point, by computing the average energy loss of a particle having an incident energy equal to the abscissa of a particular point in the unmodified spectrum and then translating that point to the left by the amount equal to the computed loss.

Energy-loss computations were made by reference to a standard table of stopping-power values for electrons and protons in aluminum.¹ Neither the unmodified nor the modified spectra of Figure 2 is the density type in the sense of describing the particle fluence per unit energy interval, $d\phi/dE$; rather, they represent discrete values of fluence within energy channels centered about the energies represented by the abscissas. These discrete points are connected by line segments in the

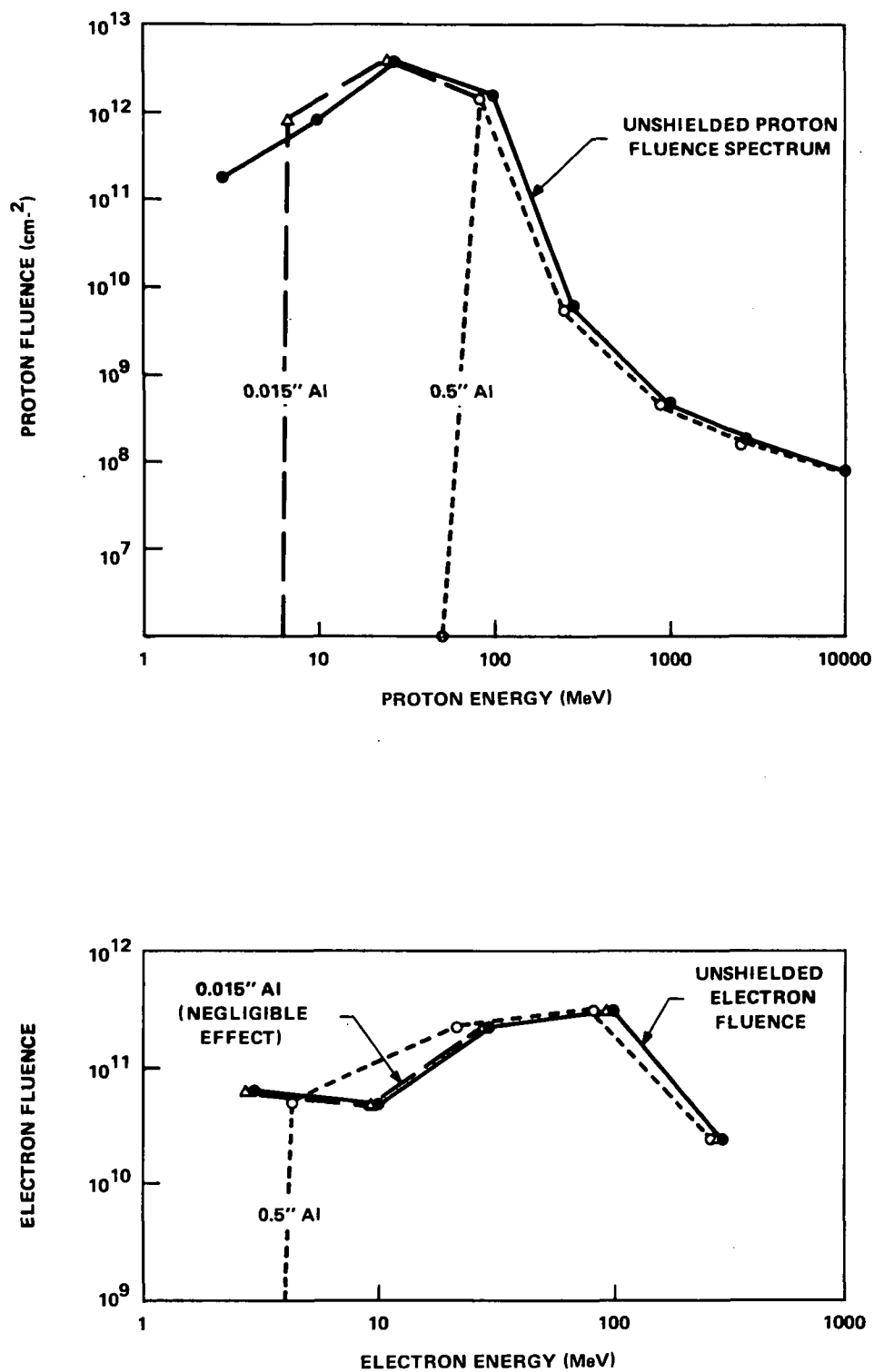
Table I. Radiation Environment

Radiation Type	Energy (MeV)		Peak Flux (Particles/cm ² sec)	Fluence (Particles/cm ²)
A. Electron	3		2.6 X 10 ⁹	6.4 X 10 ¹⁰
	10		1.2 X 10 ⁸	5.1 X 10 ¹⁰
	30		2.2 X 10 ⁷	2.2 X 10 ¹¹
	100		3.2 X 10 ⁷	3.2 X 10 ¹¹
	300		2.5 X 10 ⁶	2.5 X 10 ¹⁰
B. Proton	3		2.9 X 10 ⁷	1.7 X 10 ¹¹
	10		3.9 X 10 ⁶	9.6 X 10 ¹¹
	30		2.6 X 10 ⁶	3.9 X 10 ¹²
	100		2.4 X 10 ⁷	1.6 X 10 ¹²
	300		9.1 X 10 ⁷	6.1 X 10 ⁹
	1000		3.0 X 10 ⁷	4.7 X 10 ⁸
	3000			2.0 X 10 ⁸
	10,000			9.9 X 10 ⁷
	Energy Spectrum Energy Interval (MeV) Percent		Flux (Neutrons/cm ² sec)	Fluence (Neutrons/cm ²)
C. Neutron	< 0.5	11	3.5 X 10 ³	1.5 X 10 ¹²
	0.5 – 1.5	25		
	1.5 – 2.5	35		
	2.5 – 3.5	25		
	> 3.5	4		
	Energy Spectrum Energy Interval (MeV) Percent		Dose Rate (Rad/hr)	Dose (Rads)
D. Gamma	0.2 – 0.5	7	1.0 X 10 ⁻¹	1.0 X 10 ⁴
	0.5 – 1.0	24		
	1.0 – 2.0	17		
	2.0 – 3.0	50		
	> 3.0	2		

illustration simply for graphical clarity. Figure 2 shows that modification of the spectra by shielding is extensive only in the case of the 0.5-inch shield and incident protons. Because it is inappropriate to assume that the 0.5-inch shield uniformly surrounds the object devices, we have decided to ignore the shielding completely and to proceed with the worst-case analysis, assuming that the unshielded spectra characterize the radiation incident on the ATOM JFET.

C. IONIZATION CURRENT

A steady-state current is generated in a semiconductor device by incident radiation as a result of the production of electron-hole pairs in the semiconductor and their subsequent collection. The magnitude of this current can be calculated from the rate of ion-pair production for a given



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Figure 2. Effect of Shielding on Proton and Electron Fluence

collection volume and an assumed collection efficiency. For charged particles such as electrons and protons, the ion-pair production rate can be calculated from the energy loss in the collection volume, assuming a fixed energy required to produce an ion pair in the semiconductor. For silicon, the latter quantity is 3.6 eV/ion pair.

1. Collection Volume

To calculate the ionization current collected by a pn junction, it is usual to assume that all electrons and holes contribute to the current generated within a diffusion length of the edge of the space-charge region. In the present case, we shall make the worst-case assumption that the collection volume equals the entire dielectrically isolated "tub." The dimensions of this structure are indicated in Figure 3. The tub consists of a rectangular region (with sloped sides) about $26 \times 28 \text{ mils}^2$ along the sides with a thickness of 1 mil, or $25.4 \mu\text{m}$.

2. Ionization-Current Computation

The ionization current due to an incident ionizing particle flux, ϕ , is given by

$$I_{pp} = \frac{q_e \xi(E) \phi(E) A_{cv} t_{cv}}{\epsilon} \quad (1)$$

where:

- q_e = electronic charge
- $\xi(E)$ = stopping power of target material
for particle of incident energy, E
- A_{cv} = collection area
- t_{cv} = collection volume thickness
- ϵ = energy required to produce one
ion pair = 3.6 eV in silicon

The needed values for the stopping power are obtained from a standard tabulation of this quantity for electrons and protons.¹ In consulting the tables, we make the approximation of using the $\xi(E)$ values given for aluminum, in place of silicon.

Using Equation (1) to compute the ionization-current contributions from each of the several particle energies gives the results shown in Table II. The total predicted ionization current, due to both electrons and protons, is $9.6 \times 10^{-9} \text{ A}$.

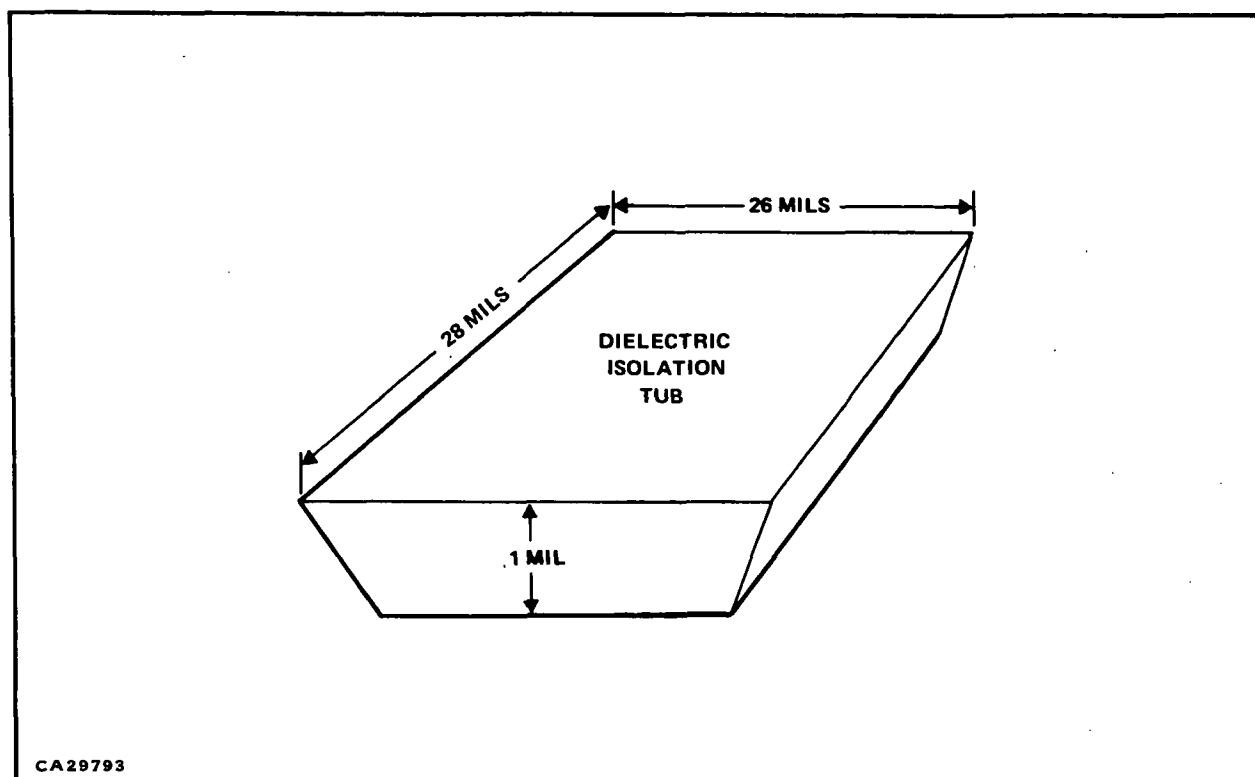


Figure 3. ATOM JFET Collection Volume

D. DISPLACEMENT EFFECTS

Sufficiently energetic neutrons, charged particles, or γ radiation can produce more or less permanent damage in semiconductor materials and devices by displacement of crystalline lattice atoms. The observed effects of lattice atom displacements in semiconductor materials are diminution of minority carrier lifetime, majority carrier concentration (in silicon), and carrier mobility. These changes in material parameters are manifest in degradation of device performance. In bipolar transistors, decreases in current gain and increases in saturation voltage and leakage current are most conspicuous. In the junction field-effect transistor, increase of "on" resistance is the primary effect with decrease of V_{po} as a second-order effect.

The mechanism of lattice atom displacement damage can be described briefly. Incident radiation interacts with the crystalline semiconductor material to produce lattice atom recoil events which are more or less uniformly distributed in the radiation path. In the case of incident particles, charged or uncharged, the recoil events result (mostly) from elastic scattering interactions. In the case of incident γ rays, the recoils are produced by Compton electrons, which are the primary interaction products. The recoiling lattice atoms, if sufficiently energetic, can dislodge other lattice atoms, producing secondary recoil events. This cascade of atom displacements establishes a distribution of crystalline defects consisting of lattice vacancies and interstitial atoms. These defects

Table II. Ionization Current

Protons —			
E_p (MeV)	ϕ ($\text{cm}^{-2}\text{s}^{-1}$)	$\xi(E)$ ($\text{MeVg}^{-1}\text{cm}^{-2}$)	I_{pp} (amp)
3	2.9×10^7	85.0	3.06×10^{-9}
10	3.9×10^6	34.0	1.64×10^{-10}
30	2.6×10^6	14.2	4.58×10^{-11}
100	2.4×10^7	5.6	1.67×10^{-10}
300	9.1×10^7	2.8	3.17×10^{-10}
1000	3.0×10^7	1.75	6.51×10^{-11}
Total I_{pp} for Protons = 3.82×10^{-9}			
Electrons —			
E_e (MeV)	ϕ ($\text{cm}^{-2}\text{s}^{-1}$)	$\xi(E)$ $\text{MeVg}^{-1}\text{cm}^2$	I_{pp} (amp)
3	2.6×10^9	1.6	5.2×10^{-9}
10	1.2×10^8	1.95	2.90×10^{-10}
30	2.2×10^7	2.75	7.50×10^{-11}
100	3.2×10^7	5.5	2.18×10^{-10}
300	2.5×10^6	13.5	4.19×10^{-11}
Total I_{pp} for Electrons = 5.82×10^{-9}			

may then move about within the crystal and interact with one another, or with defects existing within the crystal prior to irradiation, to form more or less stable defect complexes. These defect complexes contribute one or more electron energy levels, usually within the band gap, the presence of which modifies the location of the Fermi level. The presence of electron trapping levels, together with the concomitant adjustment of the Fermi level position within the band gap, produces the observed changes in the semiconductor lifetime, carrier concentration, conductivity, and mobility.

Clearly, many variables are involved in a completely general description of this damage mechanism for the various radiation types over wide ranges of incident energy. One such variable, for example, is the spatial distribution of primary recoil events. Electrons produce uniformly dispersed displacements, whereas neutrons generate dense clusters of displacements within which the behavior of a vacancy or interstitial differs considerably from that of its counterpart in isolation. Another variable is the nature and concentration of preirradiation defects and impurities. The carrier-removal rate for neutrons in silicon depends, for example, on the oxygen concentration in the target, which can vary over two orders of magnitude without conspicuously affecting electrical characteristics of the host crystal.

For engineering purposes, and in particular for predicting radiation effects on semiconductor devices, it would be desirable to have experimental data giving lifetime, conductivity, and mobility as functions of the initial values of these parameters and of radiation type, energy, and fluence. Unfortunately, such comprehensive data are not available. Many radiation studies have been made to determine the spectra of defect energy levels and their introduction rates for the various radiation types.² However, the work of correlating these studies, eliminating conflicting results, and reducing the data to a useful engineering form has progressed to practical conclusions only, perhaps, for the case of neutron irradiation. Buehler's curves, of n- and p- type silicon resistivity as functions of preirradiation resistivity and of neutron fluence,³ exemplify the type of information needed for the other semiconductor-material parameters and the other radiation types. In the absence of such information, radiation-effects predictions must be approached theoretically, accepting the uncertainty which this entails.

The objective of this portion of the ATOM JFET radiation-effects study is to estimate the displacement effects, due to the radiation environment described in Table I, on the channel resistivity and junction leakage current in the proposal JFET structure. The method used here consists in *converting* the radiation-environment description into an equivalent reactor spectrum neutron fluence, i.e., equivalent with respect to displacement density, and using Buehler's curves and other experimental neutron data to estimate channel resistivity and junction leakage current increases in the ATOM JFET. Implicit in this method is the assumption that certain fluences of two distinct types of radiation (e.g., electrons and neutrons) will produce equal channel resistivity changes, provided that they produce equal densities of lattice atom displacements. This assumption ignores the systematic differences in displacement distribution and the differences in subsequent interactions with impurities and defects which these distribution differences promote. There appears to be, however, no alternative method with which to treat, on an equal footing, all four radiation types over their complete, corresponding energy ranges.

1. Equivalent Reactor Spectrum Neutron Fluence

The equivalent reactor spectrum neutron fluence is derived by computing the expected lattice atom displacement density for each of the four radiation types in the environment of interest (Table II), summing the results, and computing the reactor spectrum neutron fluence required to produce a displacement density equal to that sum. The formulas used for these computations were taken, for the most part, from *Radiation Damage in Solids*, D. S. Billington and J. H. Crawford, Chapter 2, pp. 11-54.² The formula for lattice atom displacement density has the general form

$$N_d = N_A \sigma_d \phi \bar{\nu} \quad (2)$$

where:

- N_d = displacement density (cm^{-3})
- N_A = target ATOM density (cm^{-3})
- σ_d = displacement cross section (cm^2)
- ϕ = radiation fluence (cm^{-2})
- $\bar{\nu}$ = average number of displacements
per primary recoil event

The displacement cross section is defined as the target atom cross section for an interaction with the incoming radiation capable of giving the target atom a kinetic energy in excess of the threshold energy for lattice displacement. In silicon, the threshold energy lies between 13 and 31 eV; the lower value was used in this analysis.

For electrons and protons, the displacement cross section is derived by integrating the Rutherford differential elastic scattering cross section over residual particle energies from the displacement threshold energy to the maximum energy of transfer. For γ rays, the Compton cross section must be substituted, in the integration, for the Rutherford scattering cross section.

The average number of displacements per recoil ATOM, $\bar{\nu}$ is derived from the model of Kinchin and Pease,² with the result

$$\bar{\nu} = \frac{\bar{E}_p}{2E_d} \quad (3)$$

where:

- $\bar{E}_p$ = average primary recoil energy
- E_d = displacement threshold energy = 13 eV for silicon

The average recoil energy, $\bar{E}_p$, is computed from the theoretical probability distribution of E_p for the radiation type of interest.

In Table III, the expressions for σ_d and ν used in this analysis are tabulated for the four types of radiation. For neutrons, σ_d is approximated, following Billington and Crawford, by an experimental value for the total scattering cross section. For X rays, σ_d is obtained from a graphical presentation, published by Oen and Holmes,⁴ of a quantity called σ_d^c , the Compton displacement cross section. This quantity includes ν ; no separate equation for ν is needed in this case.

Table III. Formulas for Computation of Displacement Density

Radiation Type	Displacement Cross Section, σ_d	Avg Number of Displacements per Primary Recoil, $\bar{\nu}$
Electrons	$\frac{\pi b'^2 E_p (\text{Max})}{4 E_d}$ $b' = \sqrt{1 - \frac{v^2}{c^2}} \left(\frac{2 Z_1 Z_2 e^2}{\mu v^2} \right)$ (Relativistic Rutherford scattering)	$\frac{1}{2} \ln \frac{E_p (\text{Max})}{E_d}$
Protons	$\frac{\pi b^2 E_p (\text{Max})}{4 E_d}$ $b = \frac{2 Z_1 Z_2 e^2}{\mu v^2}$	$\frac{1}{2} \ln \frac{E_p (\text{Max})}{E_d}$
Neutrons	$\cong \sigma_s, \text{ total scattering cross section}$ $\cong 2 \times 10^{-24} \text{ cm}^2$	$\frac{E_p (\text{Max})}{4 E_d}$
γ -Rays	$\sigma_d^c, \text{ compton cross section given}$ by: Oen & Holmes JAP 30 p. 1289	$\bar{\nu} \text{ included in } \sigma_d^c$

The results of the displacement-density computations are given in Table IV for each energy range of each radiation type. According to these results, the displacement density is greatest due to protons, followed by that due to neutrons, electrons, and γ rays. The sum of displacement densities for all radiation types is $4.1 \times 10^{15} \text{ cm}^{-3}$. It is important to note that about half of this displacement density is due to the protons of energies 10 and 30 MeV. This circumstance suggests that protons in this energy range should be regarded as the greatest menace to satisfactory performance of the ATOM, for planning experimental device irradiations to simulate the radiation environment.

To compute the displacement density due to reactor spectrum neutrons, we must use an expression for γ which differs from that given in Table III for monoenergetic neutrons to account for the energy distribution of reactor spectrum neutrons. Following Billington and Crawford, we take

$$\bar{E}_p = \frac{E_p (\text{Max})}{2 \ln \left(\frac{E_p (\text{Max})}{E_d} \right)} \quad (4)$$

as the formula for average primary recoil energy, for the reactor spectrum neutron case. Using Equation (4) in Equations (3) and (2) gives, for the displacement density due to reactor spectrum neutrons,

$$N_d = 42.5 \phi_{\text{RSN}} \quad (5)$$

where:

ϕ_{RSN} = reactor spectrum neutron fluence

Equating the RHS of Equation (5) to the total displacement density gives:

$$42.5 \phi_{\text{RSN}} = 4.1 \times 10^{15} \text{ cm}^{-3}$$

or

$$\phi_{\text{RSN}} = 9.6 \times 10^{13} \text{ cm}^{-2}$$

the equivalent reactor spectrum neutron fluence.

2. Increase of Channel Resistivity

Figure 4 exhibits a family of curves, published by M.G. Buehler, for the resistivity of n-type silicon following exposure to reactor spectrum neutrons.³ These curves were calculated from the formula

$$\rho_n = \rho_{no} \exp \left(\frac{\phi}{444 n_o^{0.77}} \right) \quad (6)$$

where:

ρ_{no} = preirradiation resistivity

n_o = preirradiation carrier concentration

ϕ = neutron fluence

Equation (6) can be used to predict the ATOM JFET channel resistivity following exposure to the equivalent reactor spectrum neutron fluence, $\phi_{\text{RSN}} = 9.6 \times 10^{13} \text{ cm}^{-2}$. This prediction is exhibited in Figure 5; the postirradiation channel resistivity is plotted for an initial (preirradiation) resistivity ranging from 0. to $1.0 \Omega \text{ cm}$. This range includes the tentative design value for this parameter of about $0.6 \Omega \text{ cm}$. Within this range, the maximum channel resistivity increase is about 20%; near the tentative design value, it is about 12%.

Table IV. Summary of Computed Displacement Densities

Protons		Neutrons	
E_p (MeV)	N_d (cm ⁻³)	E_n (MeV)	N_d (cm ⁻³)
3	5.4×10^{14}	0.5	2.3×10^{13}
10	1.03×10^{15}	0.5 – 1.5	1.03×10^{14}
30	1.5×10^{15}	1.5 – 2.5	2.9×10^{14}
100	2.05×10^{14}	2.5 – 3.5	3.1×10^{14}
300	2.8×10^{11}	>3.5	5.8×10^{13}
1000	7.1×10^9		
3000	1.1×10^8		
10000	1.7×10^8		
TOTAL	3.3×10^{15}	TOTAL	7.8×10^{14}

Electrons		γ -Rays	
E_e (MeV)	N_d (cm ⁻³)	E_γ (MeV)	N_d (cm ⁻³)
3	5.2×10^{11}	.2 – .5	2.5×10^8
10	6.2×10^{11}	.5 – 1.0	3.3×10^{10}
30	3.6×10^{11}	1.0 – 2.0	1.2×10^{11}
100	6.6×10^{12}	2.0 – 3.0	6.6×10^{11}
300	6.2×10^{13}	>3.0	4×10^{10}
TOTAL	1.2×10^{13}	TOTAL	8.5×10^{11}

Total for all radiations = 4.1×10^{15} cm ⁻³			
Equivalent reactor spectrum neutron fluence, $\phi = 9.6 \times 10^{13}$ cm ⁻²			

3. Increase of Junction Leakage Current

The best available approach to estimating junction leakage current in the ATOM JFET consists in scaling experimental data from neutron-irradiated diodes. Data are available from 20-mil-diameter diodes, having base resistivity of about $0.5 \Omega \text{ cm}$. From these data, a leakage current density of $3.2 \times 10^{-11} \text{ amp/mil}^2$ was derived, corresponding to a neutron fluence of $6 \times 10^{13} \text{ cm}^{-2}$. For the ATOM JFET, we estimate a junction leakage current of $4.7 \times 10^{-8} \text{ amp}$ at $6 \times 10^{13} \text{ cm}^{-2}$ and $7 \times 10^{-8} \text{ amp}$ at $9 \times 10^{13} \text{ cm}^{-2}$.

E. CONCLUSIONS

The prescribed radiation environment will produce, in the ATOM JFET of present, tentative design, the following effects:

- Ionization current of about 10^{-8} ampere
- Increase in channel resistivity of about 12%
- Junction leakage current of about 7×10^{-8} ampere

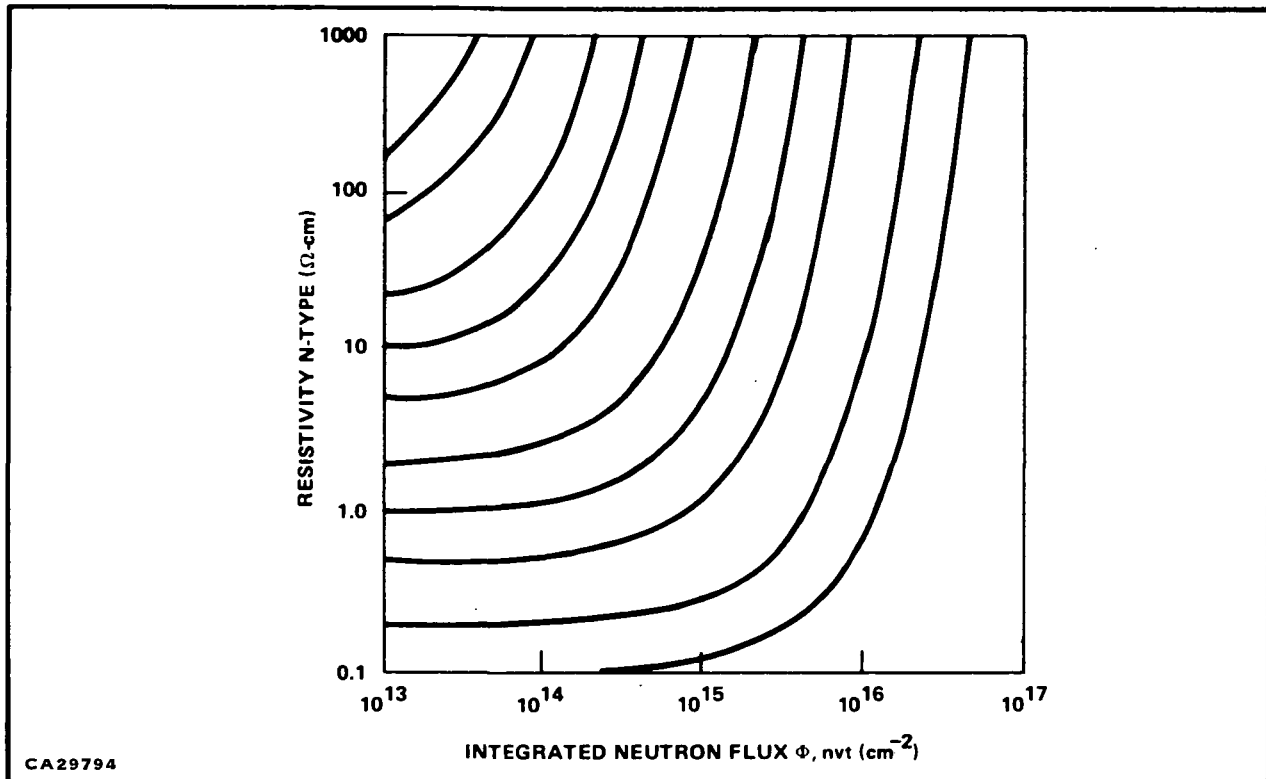


Figure 4. Resistivity as Function of Neutron Fluence

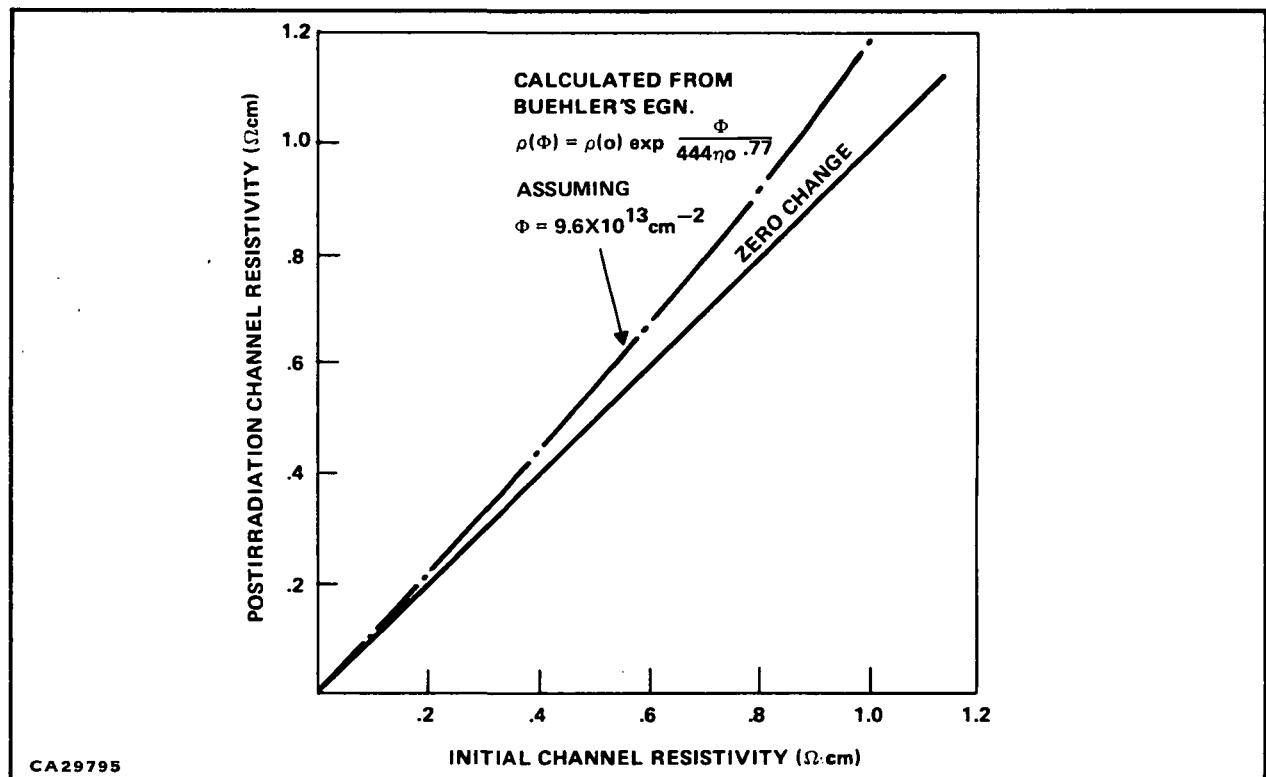


Figure 5. Predicted Channel Resistivity Change Due to Displacements Produced by Electrons, Protons, Neutrons, and γ Rays

We conclude that the radiation environment does *not* appear to be a serious threat to satisfactory performance of the ATOM JFET. Because of the uncertainties in the method used to estimate displacement effects, however, we recommend that postirradiation operation of the ATOM device be validated by experimental irradiations. Such irradiations should include medium-energy (10 to 100 MeV) proton irradiations because protons appear to be the most damaging component of the environment.

SECTION III

ATOM DESIGN

A. ATOM/JFET REQUIREMENTS

The electrical requirements of the ATOM are given in Table V. Electrical specifications used to determine the JFET parameters were the overvoltage requirement, the error voltage requirement, and the control voltages. These electrical parameters specify the resistivity of the channel and the relative dimensions of the JFET illustrated in Figure 6. The crosstalk and settling time of the ATOM are a function of device capacitance, and are optimized by fabricating the JFET with the minimum possible gate length and source-to-drain contact spacing.

1. Overvoltage

The overvoltage requirement of 30 volts sets the minimum allowed breakdown voltage of the gate-channel junction. This breakdown voltage will be controlled by the channel resistivity and the depth of the upper gate channel junction.

2. Control Voltage

The control voltage specifications, the allowed input signal swing, and the gate drive circuitry determine the maximum allowed pinch-off voltage of the JFET and the "on" voltage for the JFET. The approximate equivalent circuit which determines the gate channel junction voltage at which the JFET is defined as "on" is illustrated in Figure 7. The worst-case "on" condition occurs when the voltage at the input, defined as "on," is +3 volts and the voltage to the other input on the same clock drive line is -3 volts. For this condition, the gate channel junction of the "on" transistor is reverse biased by 5.5 volts. The worst-case "off" condition is represented by the approximate equivalent circuit in Figure 8. The worst-case "off" condition occurs when the voltage on the input of the "off" transistors is -3 volts and the ATOM is operating at a low repetition rate. For this case, the bias on the gate channel junctions (-10.5 volts) is the maximum allowed pinch-off voltage of the JFET. The designed maximum "off" voltage influences the required width of the JFET. The allowed pinch-off voltages for the JFETs in the ATOM will be

$$8.5 \text{ V} \leq V_{po} \leq 10.5 \text{ V} \quad (7)$$

to allow a suitable spread in the pinch-off voltage of the JFETs fabricated by the dielectric isolation process.

Table V. Electrical Requirements For ATOM
(Operating Temperature Range: -35 to $+100^{\circ}\text{C}$)

Parameter	Applicable Terminals	Measurement Conditions	Min	Value Norm	Max	Units
Control Voltages (V_c) ON	A, $\bar{A}$, B, $\bar{B}$	Pulsed at 10 pps to 50 K pps	+4.5	+5.0	+6.0	V
OFF		dc	-14.0	-15.0	-18.0	V
Input Voltage (V_i) Overvoltage	1 thru 8 1 thru 8, X, Y X, Y	At 10 μA , with A, $\bar{A}$, B, $\bar{B}$, grounded $R_s < 10 \Omega$	0 +30 -0.4		± 3.0	V
Output Error Voltage (V_e) $V_e = V_i - V_X$, Y Setting Time	X, Y X, Y	$R_L = 100 \text{ K } \Omega$ $R_s = 10 \text{ K } \Omega$ $C_s = 100 \text{ pF}$			± 3.0	mV
Crosstalk	X, Y	1.0 kHz, sine wave,			2.0	μs
Input Current (I_{on})	X, Y	± 3 volts peak to peak		1.0	-60	db
Voltage Drop (V_d)	1-4 to X, 5-8 to Y	$I_{on} = 1 \text{ mA}$, $V_{con} = +4.5$ volts			10.0 0.1	mA V
Gate Resistors	A, $\bar{A}$, B, $\bar{B}$		15.0	20.0	25.0	K Ω

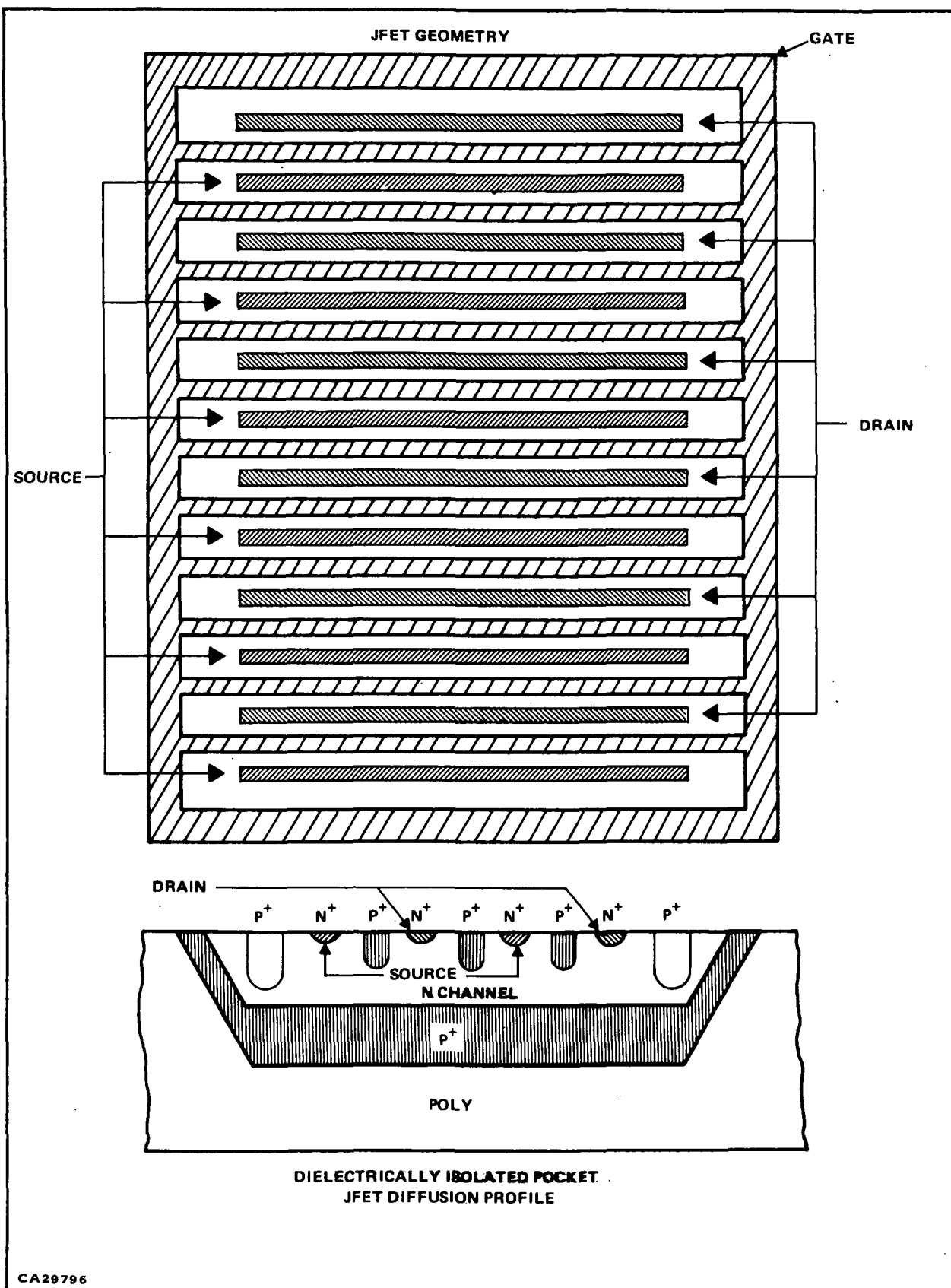


Figure 6. Dielectrically Isolated JFET

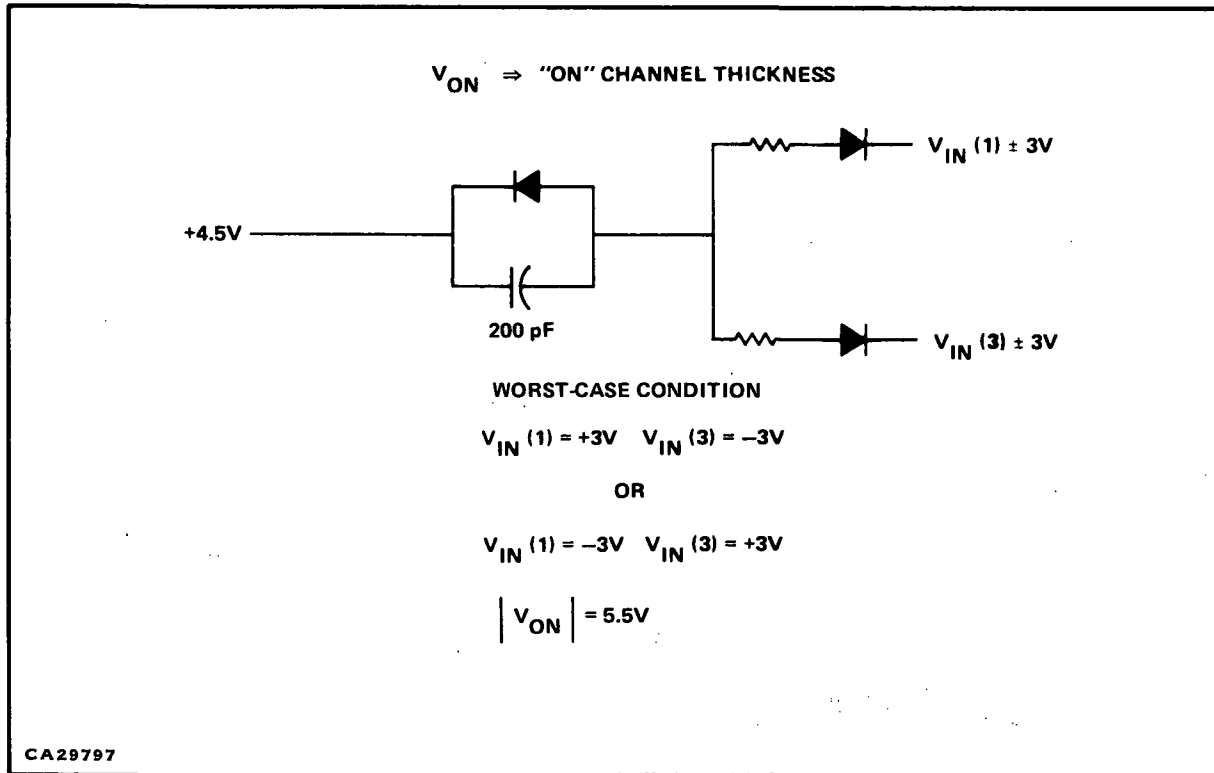


Figure 7. Input and Control Voltages for "On" Condition

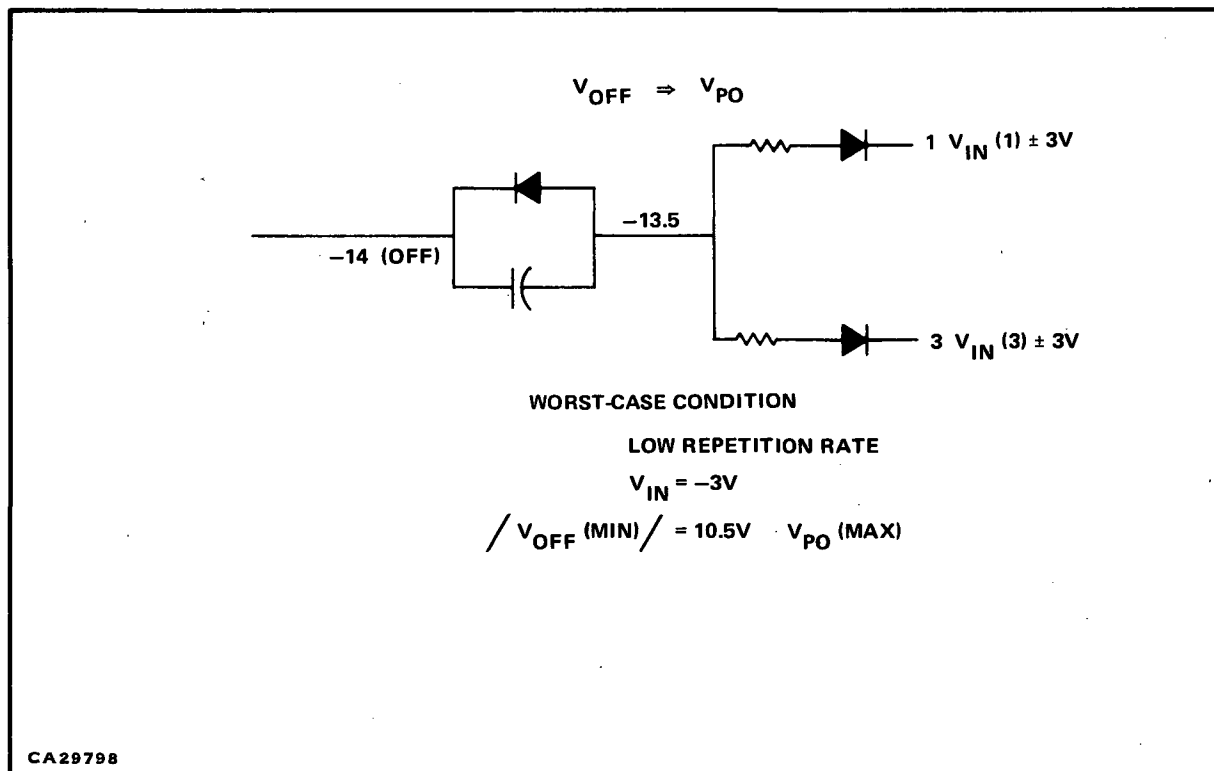


Figure 8. Input and Control Voltages for "Off" Condition

3. Output Error

The output-error specification determines the required "on" resistance of the JFET. The circuit in Figure 9 represents the equivalent circuit used to determine the "on" resistance requirement. The error voltage from Figure 9 is

$$\text{error} = e_{\text{in}} - e_{\text{o}} = e_{\text{in}} \left[\frac{R_s + 2 R_{\text{on}}}{R_L + R_s + 2 R_{\text{on}}} \right] \quad (8)$$

The required maximum error voltage is 10^{-3} volts, which is satisfied for

$$R_{\text{on}} \leq 45 \, \Omega \text{ at } T = 100^\circ\text{C}, V_{\text{gc}} = -5.5 \text{ V}.$$

4. Crosstalk

The crosstalk of the ATOM is defined as the ratio of the voltage at the output to a ± 3 -volt peak, 1-kHz input signal, applied simultaneously to each of the "off" inputs. The source and load impedance conditions are illustrated in Figure 10. There are three direct crosstalk paths in the ATOM and eleven indirect crosstalk paths through the gate circuit. The approximate equivalent circuit of the JFET being used to evaluate the crosstalk is illustrated in Figure 11.

The two major direct crosstalk paths in each half of the ATOM are illustrated in Figure 12. Each of the two paths can be represented by the equivalent circuit shown in Figure 12. The load

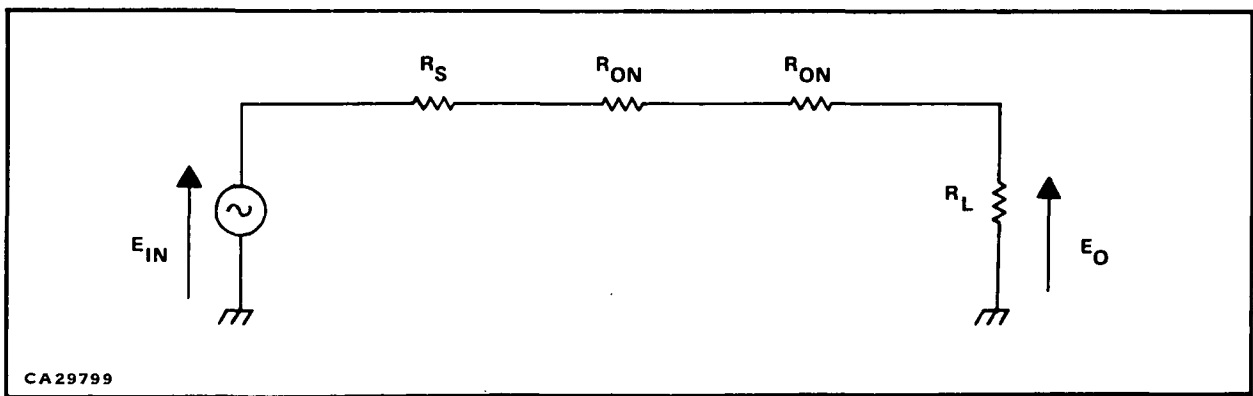


Figure 9. Output Voltage Error

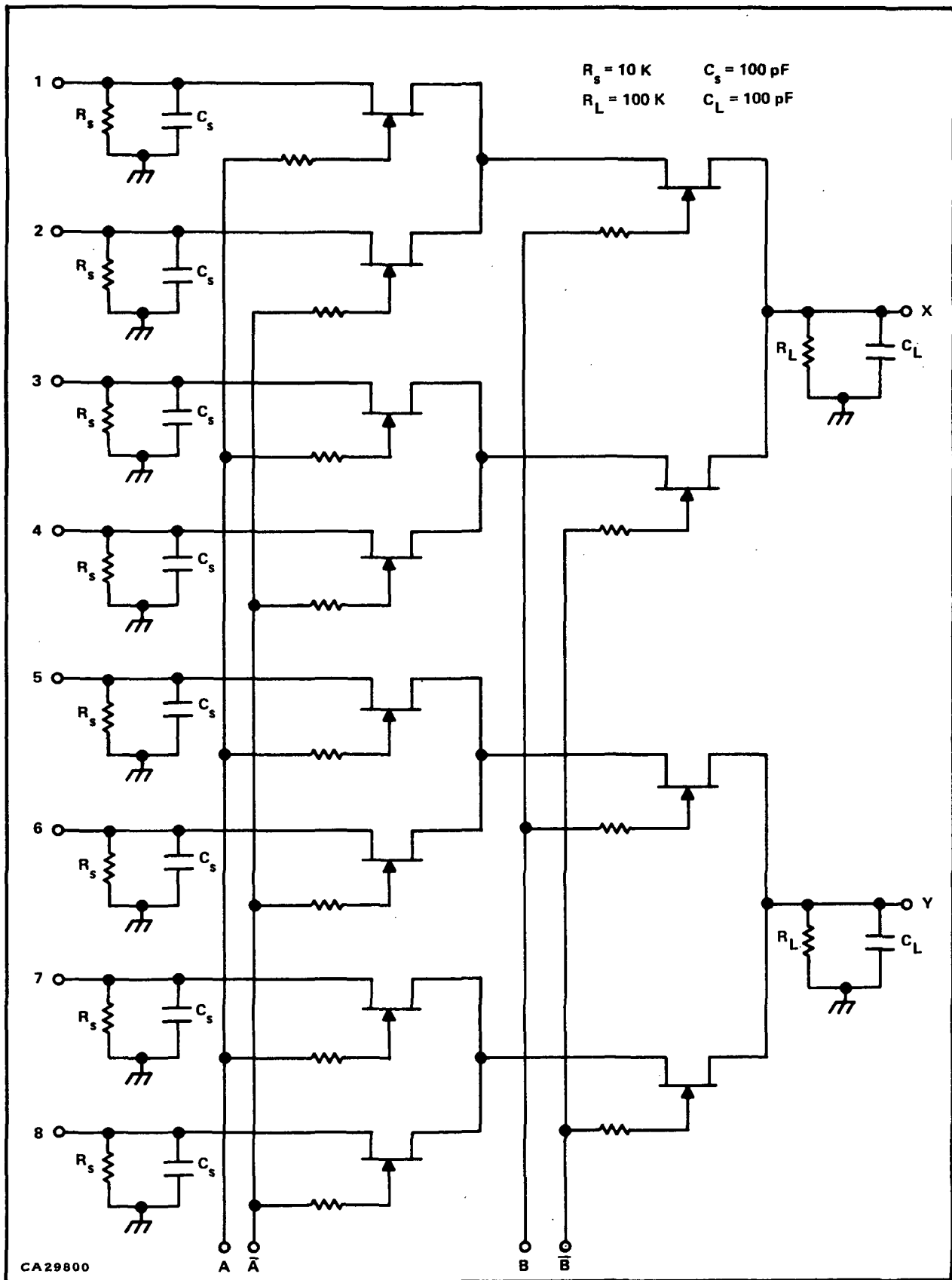


Figure 10. ATOM Circuit Configuration for Cross-Talk Measurements

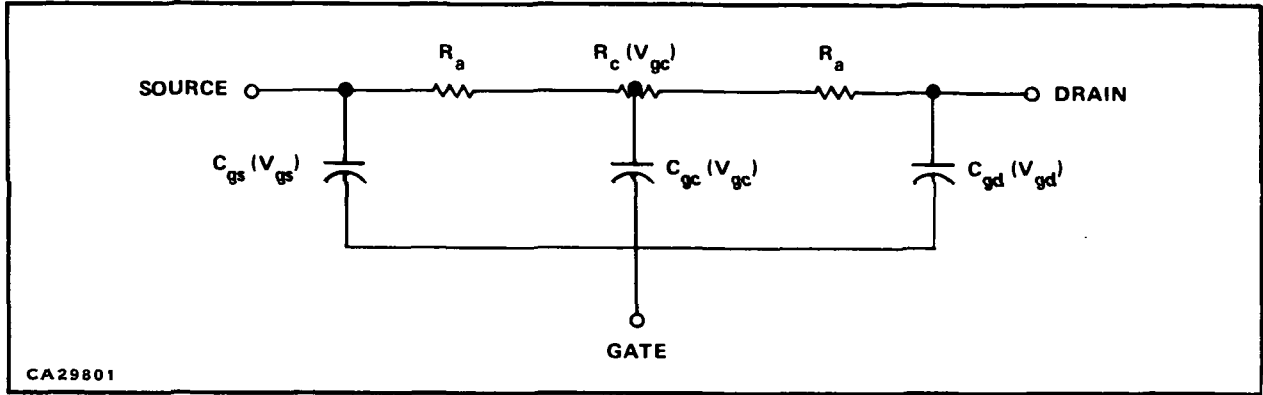


Figure 11. JFET Equivalent Circuit

impedance represents the approximate reduced load impedance resulting from the source impedance of the "on" channel. The output voltage resulting from the two major crosstalk paths is given by

$$e_o/e_{in} = \frac{2 ab}{1 + 2 (a + b + ab)} \quad (9)$$

where:

$$a = Z_g/Z_f$$

$$b = Z_L'/Z_f$$

Z_g = is the gate impedance

$Z_L' = Z_L Z_s / (Z_L + Z_s)$ is the modified load impedance

Z_f = is the impedance of C_{gs} when the JFET is off .

Crosstalk will be measured only under conditions where "a" and "b" are much less than unity. For this case, the crosstalk expression can be simplified to give

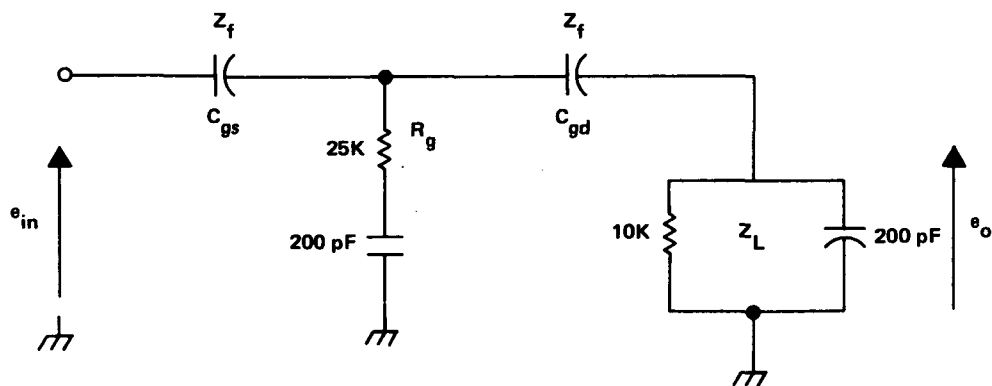
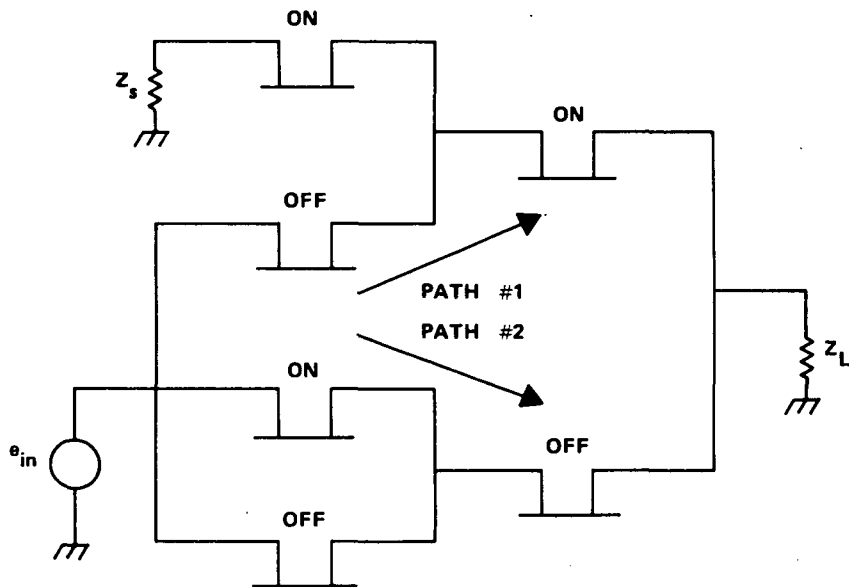
$$e_o/e_{in} \approx 2 (Z_g/Z_f) (Z_L'/Z_f) \quad (10)$$

At input frequencies of 1 kHz and below,

$$|Z_g| \approx [\omega C_g]^{-1} = [\omega (200 \text{ pF})]^{-1} \quad (11)$$

thus,

$$|e_o/e_{in}| \approx 2 \omega Z_L' C_{gs}(\text{off}) \left[\frac{C_{gs}(\text{off})}{200 \text{ pF}} \right] \quad (12)$$



EQUIVALENT CIRCUIT OF PATH #1 OR PATH #2

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Figure 12. Direct Cross-Talk Paths and Equivalent Circuit

The main indirect crosstalk paths in the upper half of the ATOM are illustrated in Figure 13. In addition, there will be coupling from the lower half of the ATOM through the gate circuit to an output in the upper half of the ATOM. The indirect crosstalk can only be eliminated by reducing the impedance at the gate drive points: A, $\bar{A}$, B, $\bar{B}$. The indirect coupling paths are through the gate capacitance of an "on" JFET. This capacitance will depend on the input signal and bias voltage, and may be as much as a factor of 6 larger than $C_{gs}(\text{off})$. The curve in Figure 14 illustrates the gate-to-source capacitance of a discrete JFET as a function of gate bias. The capacitance increases greatly below the pinch-off voltage because the depletion width is decreased and the area of the capacitor increases to include the entire channel region.

The approximate magnitude of the feedthrough in Path 1 of the gate circuit can be estimated from the equivalent circuit illustrated in Figure 13. The transfer function of this circuit at frequencies of 1 kHz and less can be approximated by

$$e_o/e_{in} = \omega C_{gc}(\text{on}) (10K) (C_{gc}(\text{on}) / C_g) \quad (13)$$

The worst-case magnitude of $C_{gc}(\text{on})$ occurs when the gate channel junction is near zero bias and may occur for only a portion of each cycle of the 3-volt input signal. The effective magnitude of $C_{gc}(\text{on})$ required to keep crosstalk in any one path to less than 2×10^{-4} at 1 kHz with $C_g = 200 \text{ pF}$ is

$$C_{gc}(\text{on}) \leq 25 \text{ pF} \quad (14)$$

Crosstalk in the ATOM is a complex problem; it will require the use of a computer-analysis program for evaluation.

5. Settling Time

The settling time of the ATOM depends on several boundary conditions, which include:

- Drive capacitance and gate resistor
- Source admittance
- Load admittance
- Input voltage being switched "to"
- Output voltage being switched "from"
- JFET gate-to-channel capacitance

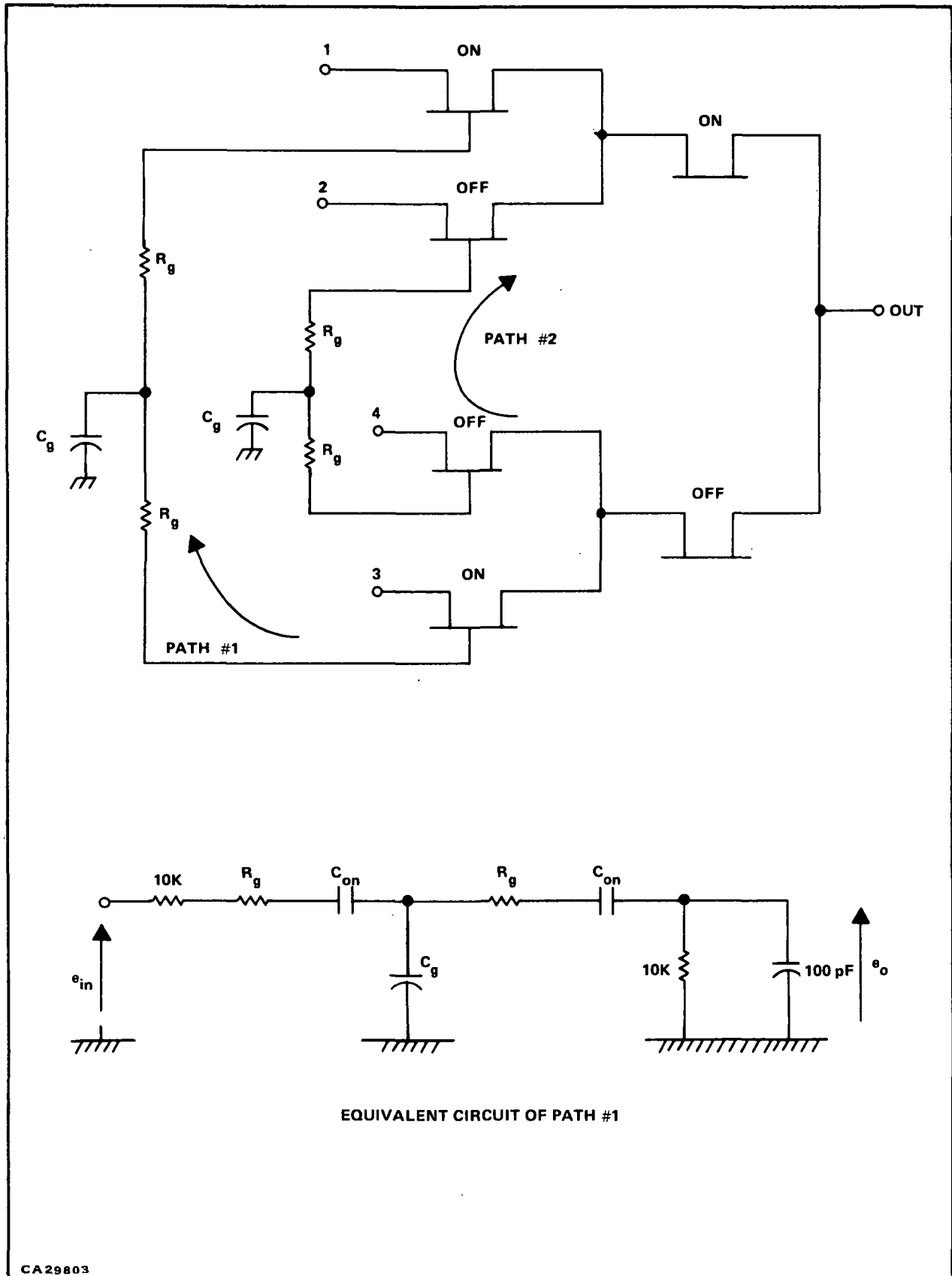


Figure 13. Indirect Cross-Talk Paths and Equivalent Circuit

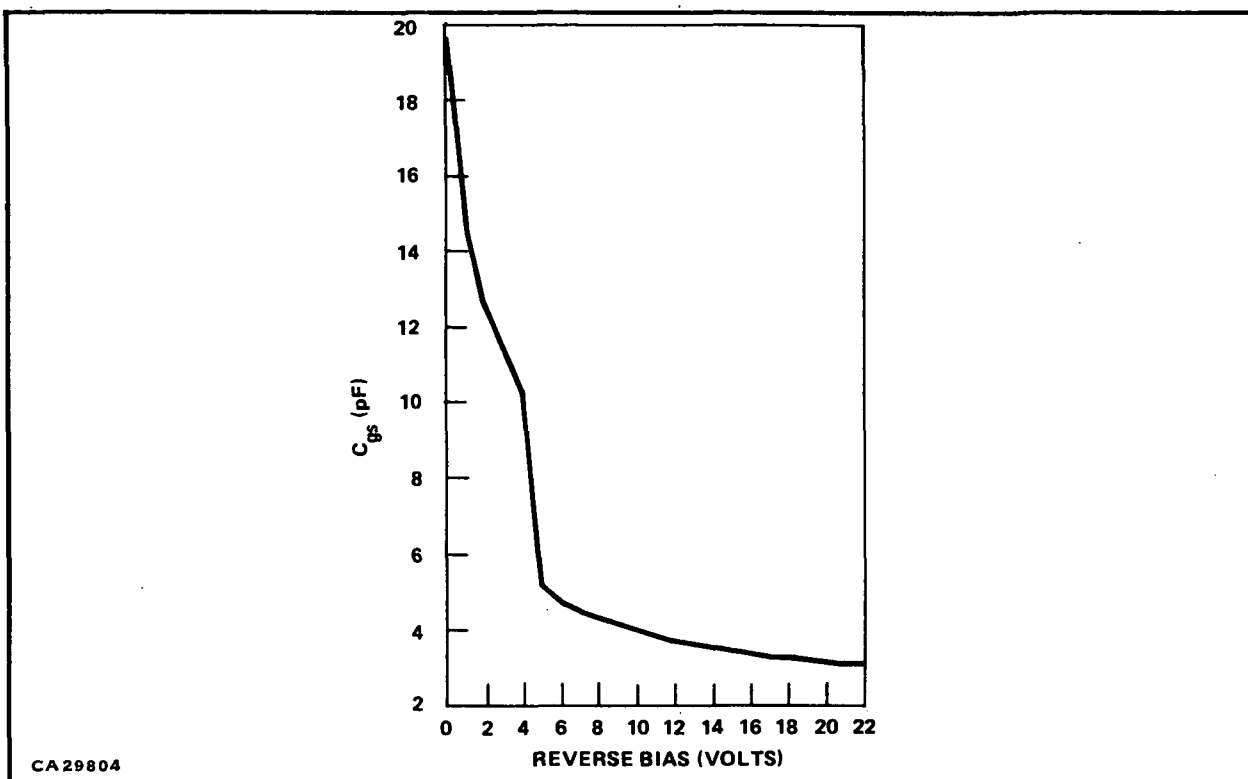


Figure 14. Gate-to-Source Capacitance as Function of Gate Bias

The settling time of the ATOM has been evaluated for the conditions illustrated in Figure 15 and listed below.

$$\begin{aligned}
 V_{in} &= 0 \\
 R_S &= 10K \quad C_S = 100 \text{ pF} \\
 R_L &= 100K \quad C_L = 100 \text{ pF} \\
 R_g &= 25K \quad C_{drive} = 200 \text{ pF} \\
 \text{Switching sequence: } &4, 3, 2, 1
 \end{aligned}$$

The worst-case settling time transients are observed when either the number two or four input is switched "on." Curves (a) and (b) in Figure 16 represent the output voltage of the ATOM when the number two input is switched "on." The output-voltage waveform is displayed on two time and voltage scales to illustrate the relatively short device and drive circuit time constant as well as the relatively long input and output circuit time constant. Curve (c) in Figure 16 represents the difference between the voltage at the input and output terminals of the ATOM. The settling time of the ATOM can be measured from Curve (c) as the time at which the voltage magnitude is less than 30 mV. This occurs for the case illustrated at $t = 0.35 \mu\text{s}$. The output voltage corresponding to $t = 0.35 \mu\text{s}$ is 0.23 volt. The effect of the circuit parameters on the waveform of the output voltage illustrated by Curves (a) and (b) can be explained by the approximate settling time equivalent

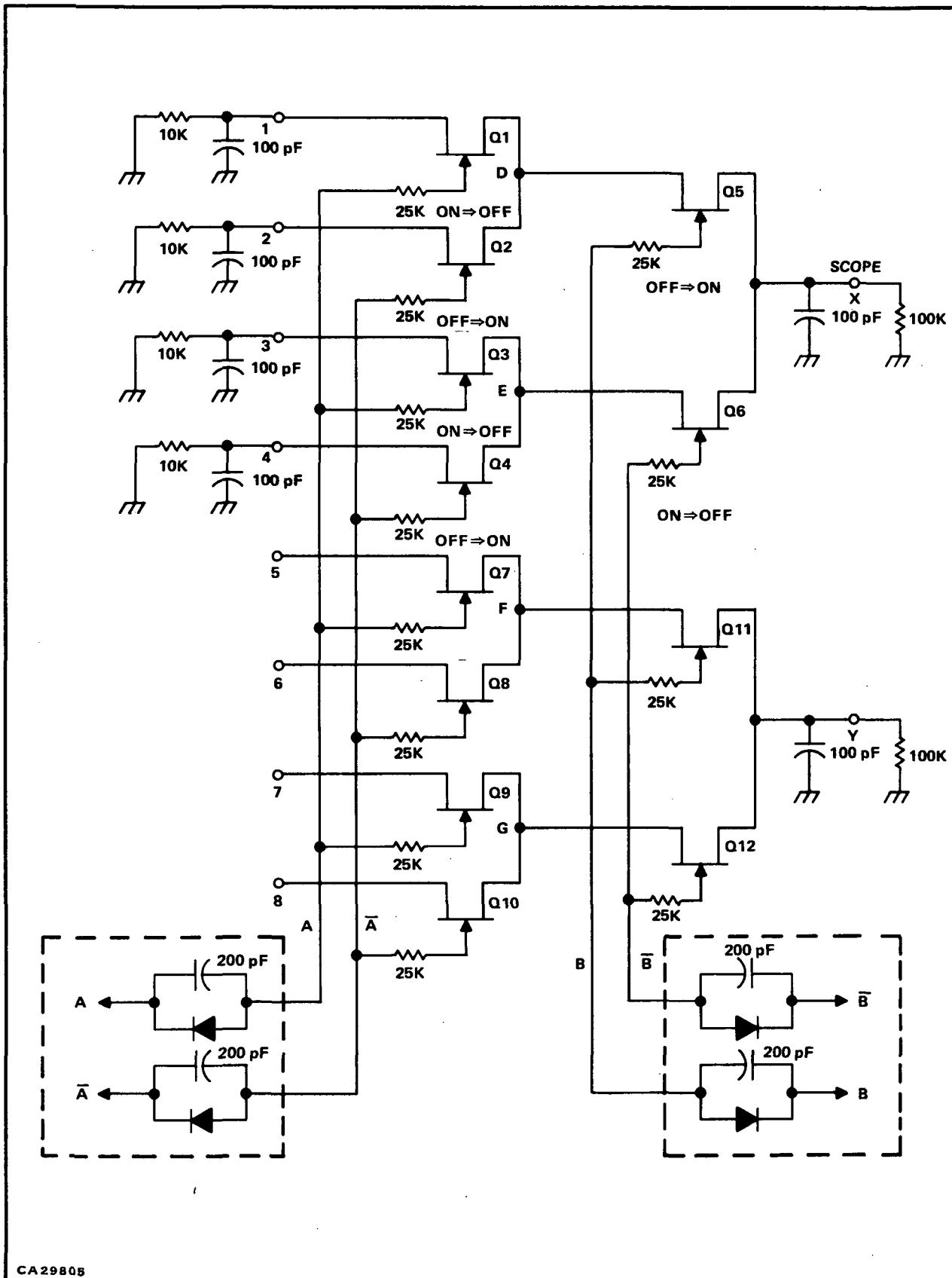
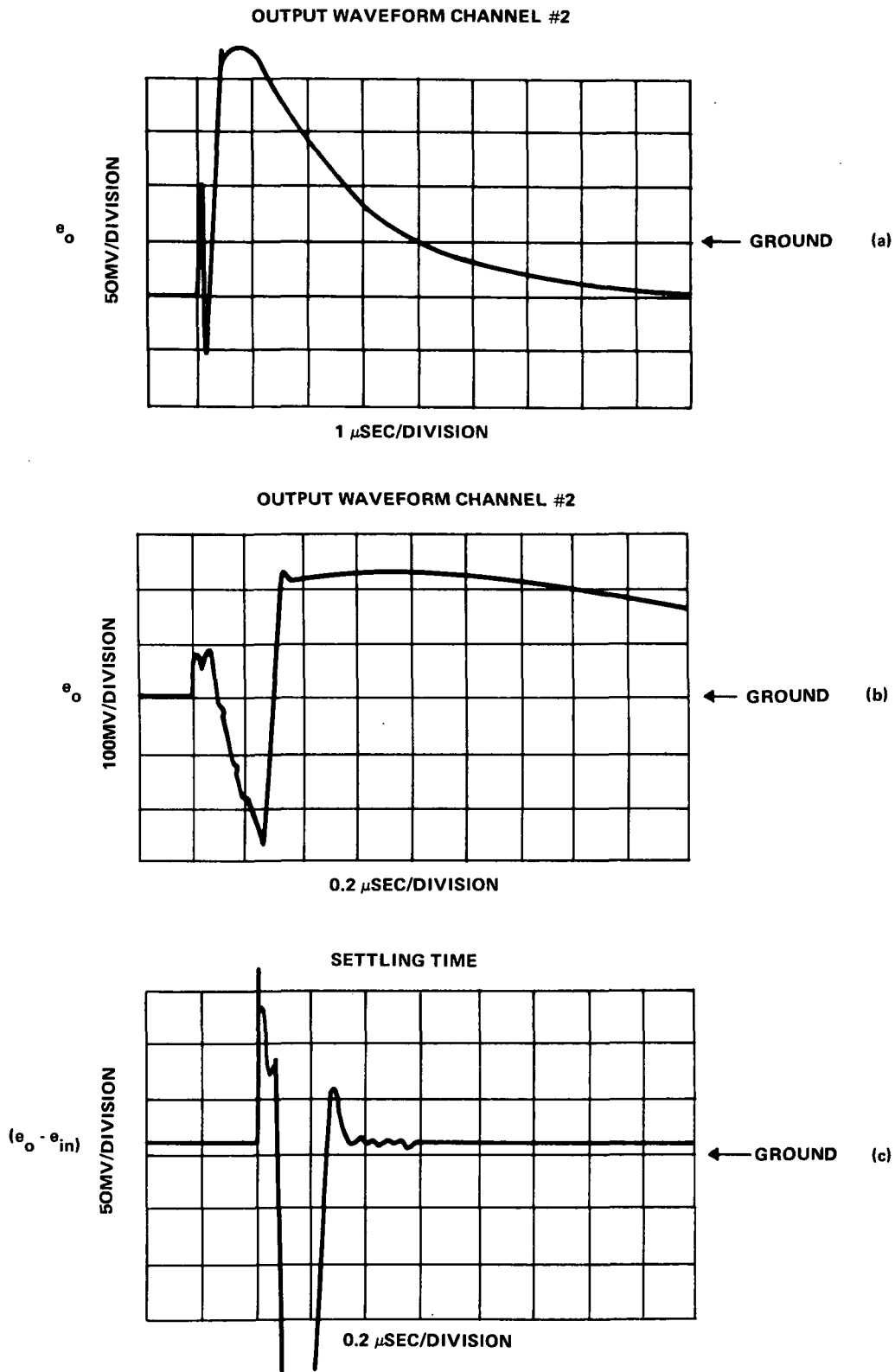


Figure 15. ATOM Circuit Configuration for Settling-Time Measurements



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Figure 16. Settling-Time Measurements

circuit illustrated in Figure 17. At $t = 0$, the charge on capacitors C_L , C_S , and C_{dr} is approximately zero and the device capacitance, C_{gs} , is charged to -13 volts. During the initial transient phase, the gate capacitance, C_{gs} , is discharged and the drive capacitance charged with a time constant of

$$t_g \approx R_g C_{gs} \quad C_{gs} \ll 100 \text{ pF} \quad (15)$$

During the discharge of C_{gs} , a current flows in R_L , C_S , and C_L , and the output voltage increases positively. The initial negative swing of e_o is caused by other JFETs being turned "off."

The output voltage rises to 0.23 volt at $t = 0.35 \mu\text{s}$. At this time, C_{gs} is essentially discharged, the JFET "on," and the input and output voltage differ by less than 30 mV . Current flow in the gate circuit continues to charge the 200-pF drive capacitor and the output voltage increases slowly until the charging current is not sufficient to maintain the output voltage on the effective 200-pF load capacitance. The output voltage then decays with a time constant

$$t_L \approx (10\text{K}) (200 \text{ pF}) = 2 \mu\text{s} \quad (16)$$

until, at $t \approx 5 \mu\text{s}$, the output voltage drops below 30 mV . These data illustrate that, for zero input voltage, the settling time is controlled by the $R_g C_{gs}$ time constant, while the time required for the output and input voltages to drop below 30 mV is controlled primarily by the $R_S(C_S + C_L)$ time constant.

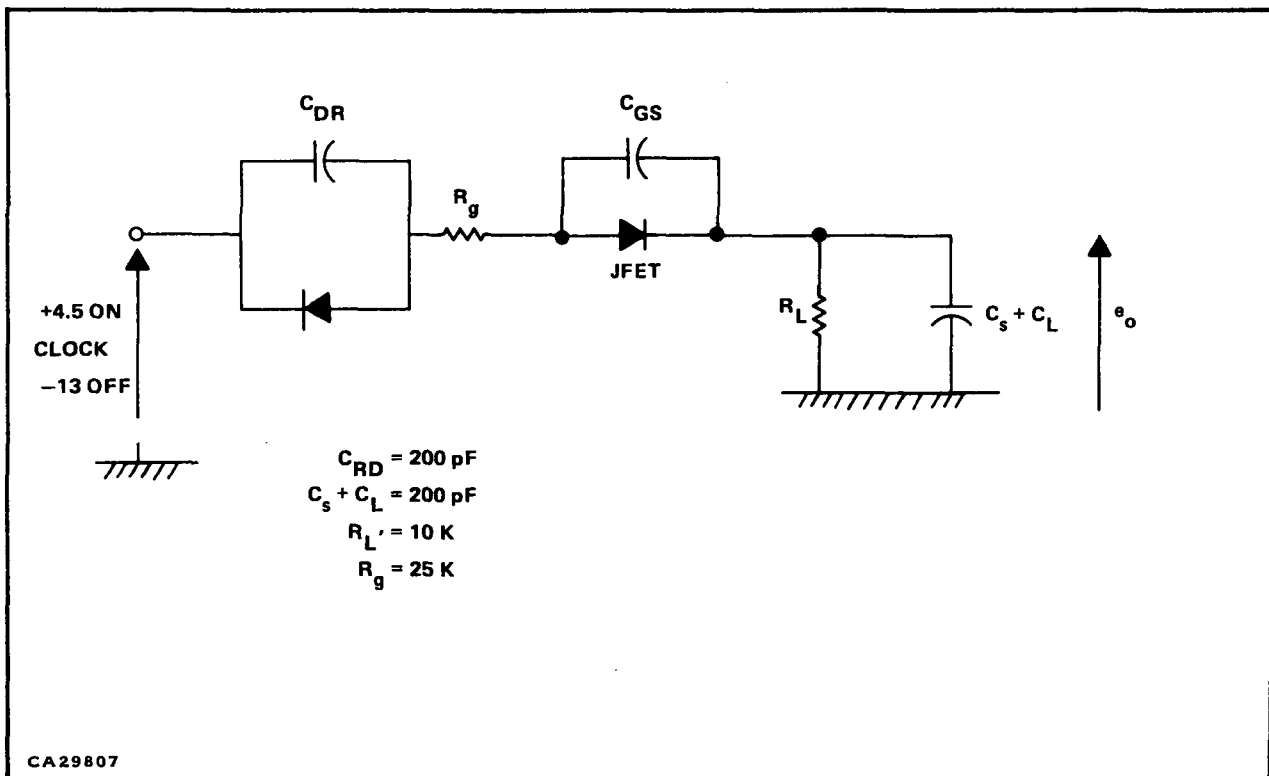


Figure 17. Settling-Time Equivalent Circuit

B. JFET DESIGN

1. Ideal JFET

The geometry terms used in the design of the JFET cell are defined in Figure 18. The initial design analysis relating the pinch-off voltage and "on" resistance of the JFET to device geometry and channel resistivity was made assuming abrupt one-sided p^+n junctions for both the front and back gates, uniform channel doping, and equal horizontal and vertical diffusion of the front gate. The minimum device geometries set by the photoresist process are:

$$L_g = 0.2 \text{ mil} \quad (17)$$

$$W_s = W_d = 0.2 \text{ mil} \quad (18)$$

$$a = 0.3 \text{ mil} \quad (19)$$

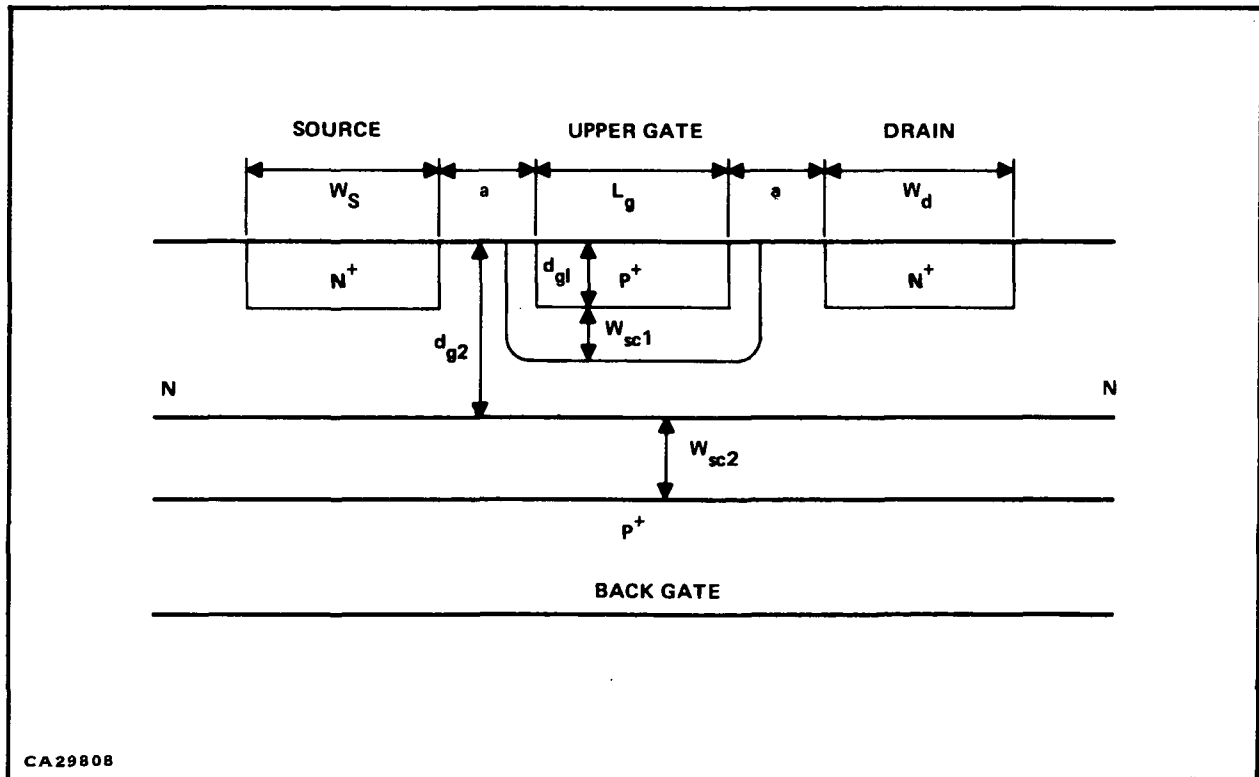


Figure 18. JFET Geometry Definitions

a. Breakdown Voltage

The required minimum BV_{DSS} of 30 volts places restrictions on the depth of the upper gate 5,6 and on the channel resistivity. The curves in Figure 19 illustrate the breakdown voltage of a p^+n junction as a function of the doping concentration of the n -region and the depth of the p^+n junction. The minimum allowed upper gate depth, d_{gl} , and channel resistivity, ρ_c , which satisfied the required 30-volt breakdown voltage, are

$$d_{gl} = 0.06 \text{ mil} \quad (20)$$

and

$$\rho_c \geq 0.4 \Omega/\text{cm} \quad (21)$$

The maximum upper gate depth is set by the minimum spacing of the source drain contacts from the gate diffusions window at 0.11 mil. Thus, the upper gate channel junction will be located at

$$0.06 \leq d_{gl} \leq 0.11 \text{ mil} \quad (22)$$

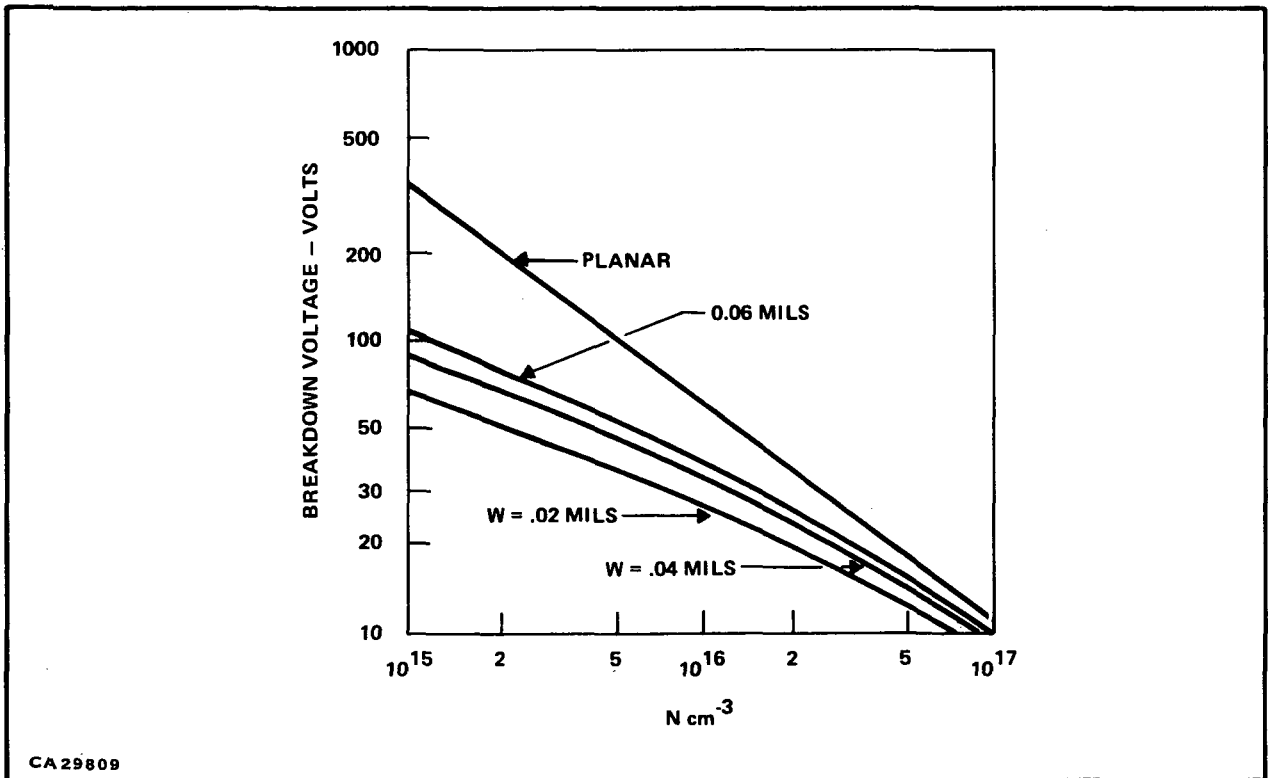


Figure 19. Breakdown Voltage as Function of Channel Doping Concentration and Upper Gate Diffusion Depth

b. Pinch-off Voltage

The minimum "off" control voltage (-8.5 volts) on the gate-channel junction determines the maximum allowed pinch-off voltage, V_{po} , and the maximum allowed spacing of the upper and lower gate-channel junctions. The junction spacing⁷ is related to the required pinch-off voltage by

$$d_{g2} - d_{g1} = 2 \left[\frac{2\epsilon_s(V_{po} + V_{bi})}{q N_c} \right]^{1/2} \quad (23)$$

or

$$d_{g2} - d_{g1} = 2 \left[\frac{(V_{po} + V_{bi})}{5 \times 10^{-13} N_c} \right]^{1/2} \text{mils} \quad (24)$$

where:

d_{g2} = depth of back gate channel junction

V_{bi} = built-in voltage

N_c = channel doping

ϵ_s = permittivity of silicon

q = electronic charge

The premultiplier "2" assumes equal depletion from the front and back gate.

Once the channel resistivity has been specified from breakdown-voltage requirements, the difference in the depth of the front and back gate channel junctions can be adjusted to control the pinch-off voltage. In the case of an actual diffused junction, the Lawrence and Warner curves,⁸ which relate the capacitance and depletion widths of a diffused junction to the applied bias voltage, can be used graphically to determine the depletion of the channel by the front and back gate-channel junctions.

c. "On" Resistance

The required "on" resistance, R_{on} , of the JFET is determined from the allowed output-error voltage. The output-error-voltage requirement is satisfied for

$$R_{on} \leq 45 \Omega \quad (25)$$

The "on" resistance⁷ is related to the device geometry by

$$R_{on} = \frac{\rho_c (L_g + 1.4a)}{Z_c} = \frac{(394) (L_g + 1.4a)}{q \mu_n N_c Z_c t_c} \quad (26)$$

where:

L_g = channel length in mils

a = spacing between gate diffusion and source or drain contact in mils

ρ_c = channel resistivity in Ω/cm

μ_n = channel mobility $\text{cm}^2/\text{V-s}$

q = electronic charge in coulombs

Z_c = channel width in mils

and

t_c = channel thickness (at $V_{gc} = V_{on}$) in mils

The channel thickness is given by

$$t_c = d_{g2} - d_{g1} - 2 W_{sc} \quad (27)$$

where:

W_{sc} = width of gate channel depletion region

The channel thickness at V_{on} can be expressed by

$$t_c = \frac{2}{(5 \times 10^{-13} N_c)^{1/2}} \left[(V_{po} + V_{bi})^{1/2} - (V_{on} + V_{bi})^{1/2} \right] \text{ mils} \quad (28)$$

The "on" resistance is then given by

$$R_{on} = \frac{8.75 \times 10^{+14} (L_g + 1.4a)}{\mu_n Z_c N_c^{1/2} \left[(V_{po} + V_{bi})^{1/2} - (V_{on} + V_{bi})^{1/2} \right]} \quad (29)$$

The minimum allowed values of L_g and a are set at 0.2 and 0.3 mil respectively by geometry limitations. The maximum value of channel doping, N_c , is set by the required gate-to-channel breakdown voltage. The value of V_{po} and V_{on} is set by the gate drive voltage, the applied signal voltage, and the sampling rate. The channel mobility is set by N_c , and is temperature dependent. The worse-case condition for "on" resistance occurs at 100°C ⁹

where:

$$\mu_n(100^\circ\text{C}) = 0.6 \mu_n(27^\circ\text{C}) = 650 \text{ cm}^2/\text{V-s} \quad (30)$$

Equation (29) illustrates that the required gate width (and, hence, the device area) for given minimum values of L_g and a is minimized by increasing the difference in V_{po} and V_{on} . The ATOM drive circuit allows "on" transistors to become reverse biased to a worst-case magnitude of -5.5 volts. The worst-case "off" voltage is -8.5 volts. This greatly reduces the possible difference in V_{po} and V_{on} .

The JFET channel width must be selected to satisfy R_{on} for the minimum channel doping, minimum channel mobility, and worst-case drive conditions. The relationship between "on" resistance, channel width, and the channel doping for

$$\begin{aligned} L_g &= 0.2 \text{ mil} \\ a &= 0.3 \text{ mil} \\ V_{on} &= -5.5 \text{ volts} \\ V_{po} &= -8.5 \text{ volts} \\ V_{bi} &= -0.92 \text{ volt} \\ \mu_n &= 650 \text{ cm}^2/\text{V-s} \end{aligned}$$

is given by

$$R_{on} = \left(\frac{1.55 \times 10^{12}}{Z_c N_c^{1/2}} \right) \Omega \quad (31)$$

The channel-width requirement for $\rho_c = 0.6 \Omega\text{-cm}$, $N_c = 10^{16} \text{ cm}^{-3}$

is given by

$$Z_c = \frac{1.55 \times 10^{12}}{(40) \times 10^8} = 390 \text{ mils} \quad (32)$$

The basic JFET cell has a linear dimension of 1.0 mils. The required 390-mil channel length can be realized by 20 cells with a channel width of 19.6 mils. The ideal JFET would fit in a dielectrically isolated pocket with dimensions of 21 X 21 mils.

For a dielectrically isolated, diffused JFET, the separation of the front and back gates required to satisfy the pinch-off voltage requirement, the channel thickness at the "on" voltage of the JFET, and, hence, the required channel width will be a function of the diffusion profile of the gate channel junctions.

The dielectric isolation process will control the diffusion profile of the gate channel junction and must be specified before the gate channel junction separation and the channel width are selected. The following section contains a description of the JFET design for the two dielectric isolation processes under consideration.

2. Dielectrically Isolated JFET

a. Double Poly Process

The double poly-dielectric isolation process is illustrated in Figure 20. The n-type epitaxial layer which will be used as the channel of the JFET is not involved in the grinding or material-removal processes, and its resistivity and thickness are only a function of the variables of the epitaxial deposition. The epitaxial film is deposited early in the fabrication process, and receives a heat treatment equivalent to 1375 minutes at 1100°C during the remaining steps of the fabrication process. This heat treatment results in the diffusion of the p^+ substrate into the n-type epitaxial film. This diffusion has an erfc (x) shape¹⁰ with a diffusion coefficient (D), time product of

$$[Dt]^{1/2} = 2 \times 10^{-4} \text{ cm} \quad (33)$$

for the boron in the p^+ substrate. The diffusion of the p^+ substrate ($2 \times 10^{19} \text{ cm}^{-3}$) into the n-type epitaxial film is illustrated by the curves in Figure 21. The p^+ junction moves approximately 0.34 mil during the dielectric isolation process. The initial thickness of the epitaxial film will be set at 0.48 mil to allow the final desired location of the p^+ n junction at 0.14 mil from the surface to be achieved.

The p diffusion into the n-type epitaxial material beyond the p^+ n junction compensates the channel doping, causing a skewing of the channel doping, as illustrated in Figure 22. This compensation causes a computed effective increase in channel resistivity of 20%. The increased

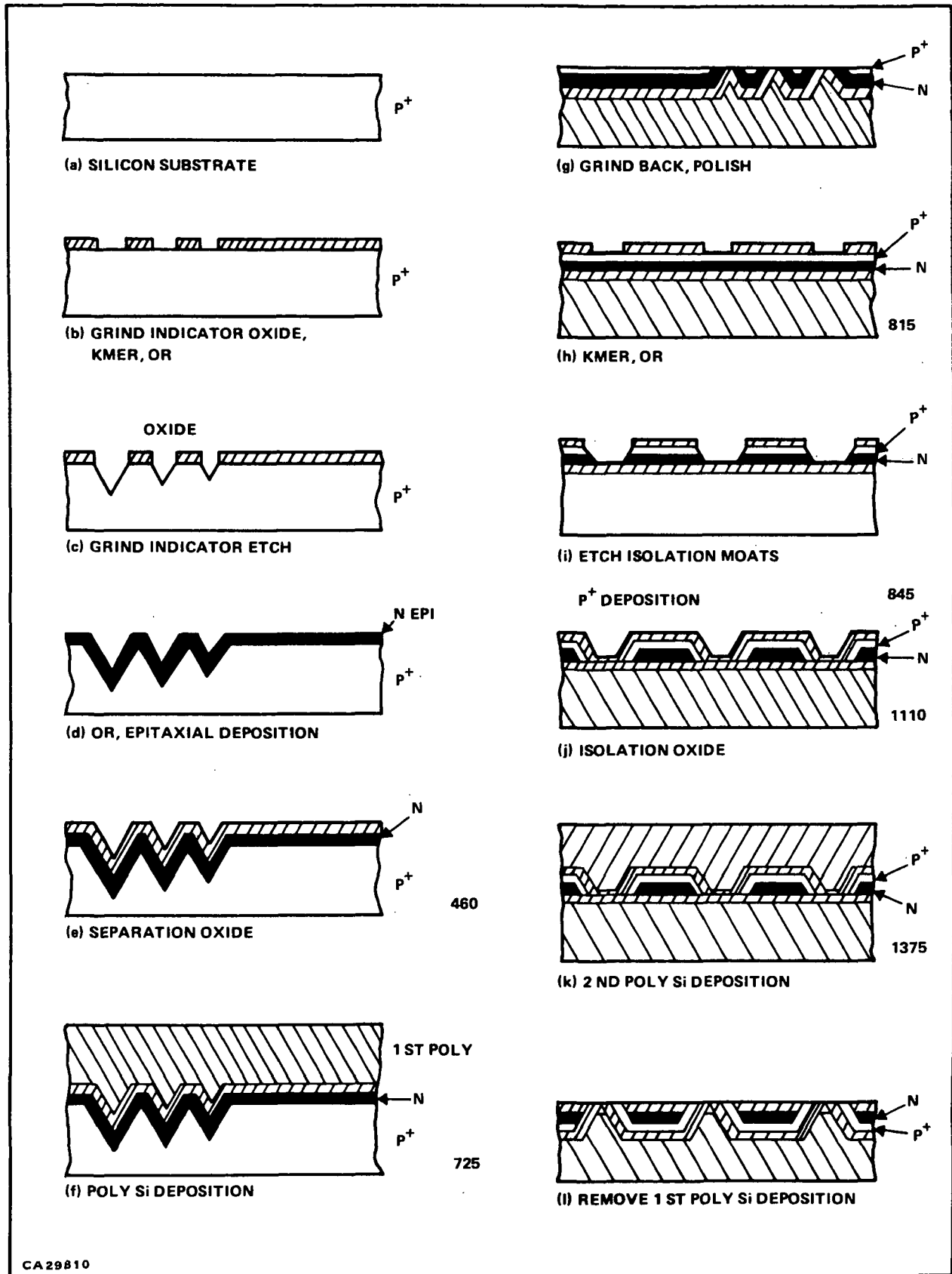


Figure 20. Double Poly-Dielectric Isolation Process

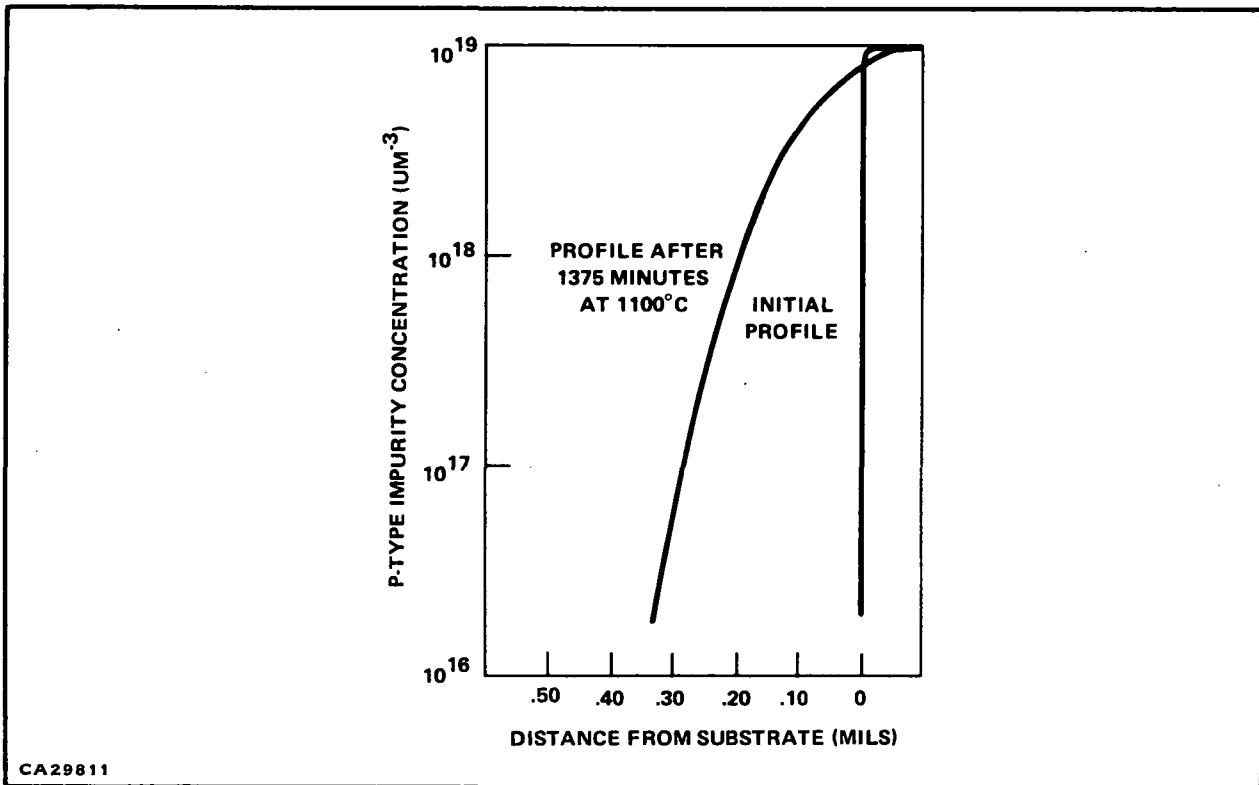


Figure 21. Concentration Profile of Back Gate Junction

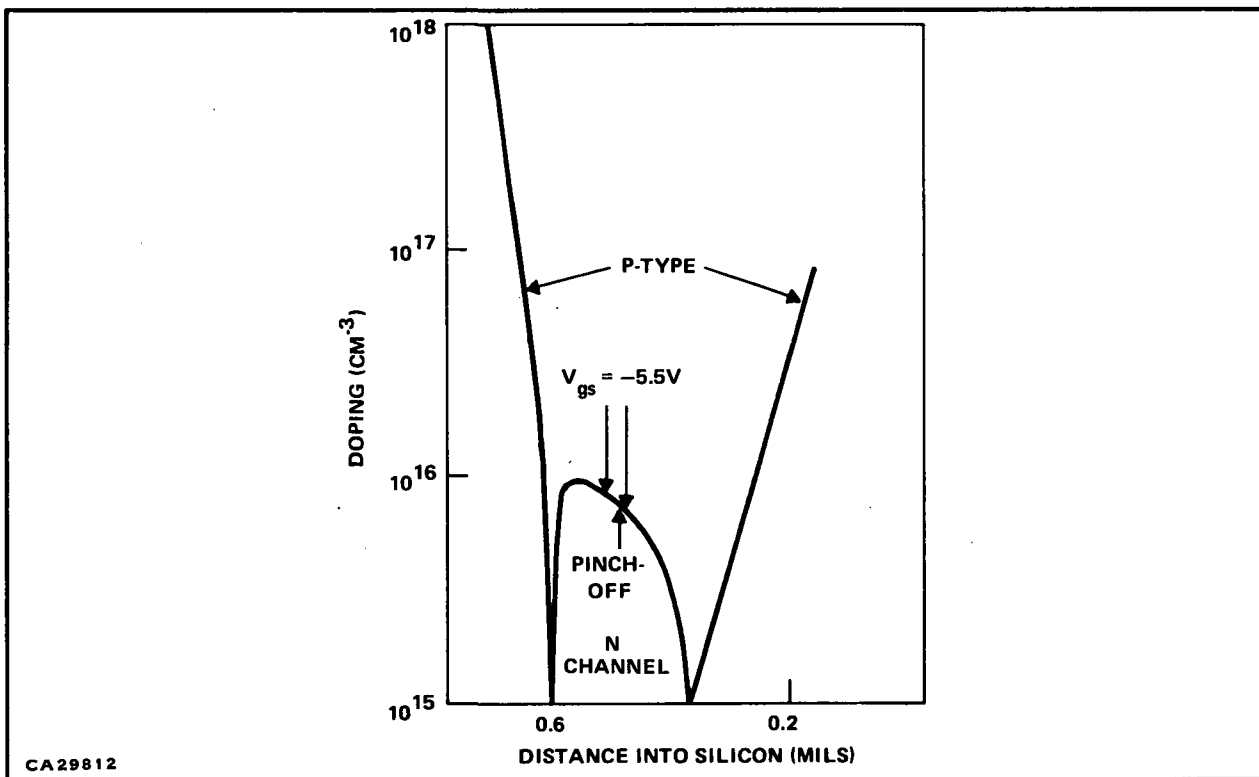


Figure 22. Concentration Profile of JFET Fabricated by Double Poly-Dielectric Isolation Process

effective channel resistivity can be compensated by an increase in channel width. There is some uncertainty regarding the exact shape of the diffusion tail, and if the diffusion tail drops off slower than predicted by the assumed $\text{erfc}(x)$ shape, a larger increase in channel resistivity would be observed in the actual devices.

b. Raised Dielectric Process

The raised dielectric isolation process is illustrated in Figure 23. The n-type epitaxial film to be used for the channel of the JFET will be deposited after all of the mechanical material-removal steps and after most of the high-temperature processing steps have been completed. The diffusion of the p^+ substrate into the epitaxial film during the raised dielectric isolation process is compared to the diffusion of the substrate in the double poly process by the curves in Figure 24.

These curves illustrate that the back gate channel junction of the JFET fabricated by the raised dielectric isolation process will more closely approach the abrupt junction of the ideal JFET than the back gate channel junction of the JFET fabricated by the double poly-dielectric isolation process. The diffusion profile of the gate channel junctions of the JFET fabricated by the raised dielectric isolation process is illustrated in Figure 25. Compensation of the channel resistivity would not be a problem in the raised structure.

c. Design of Dielectrically Isolated JFET.

The "on" resistance of the JFET is related to device parameters through

$$R_{\text{on}} = \frac{\rho_c (L_g + 1.4a)}{Z_c t_c} = \frac{(394) (L_g + 1.4a)}{q \mu_n N_c Z_c t_c} \quad (34)$$

where:

L_g = channel length in mils

a = spacing between gate diffusion and source, or drain contact in mils

ρ_c = channel resistivity in $\Omega\text{-cm}$

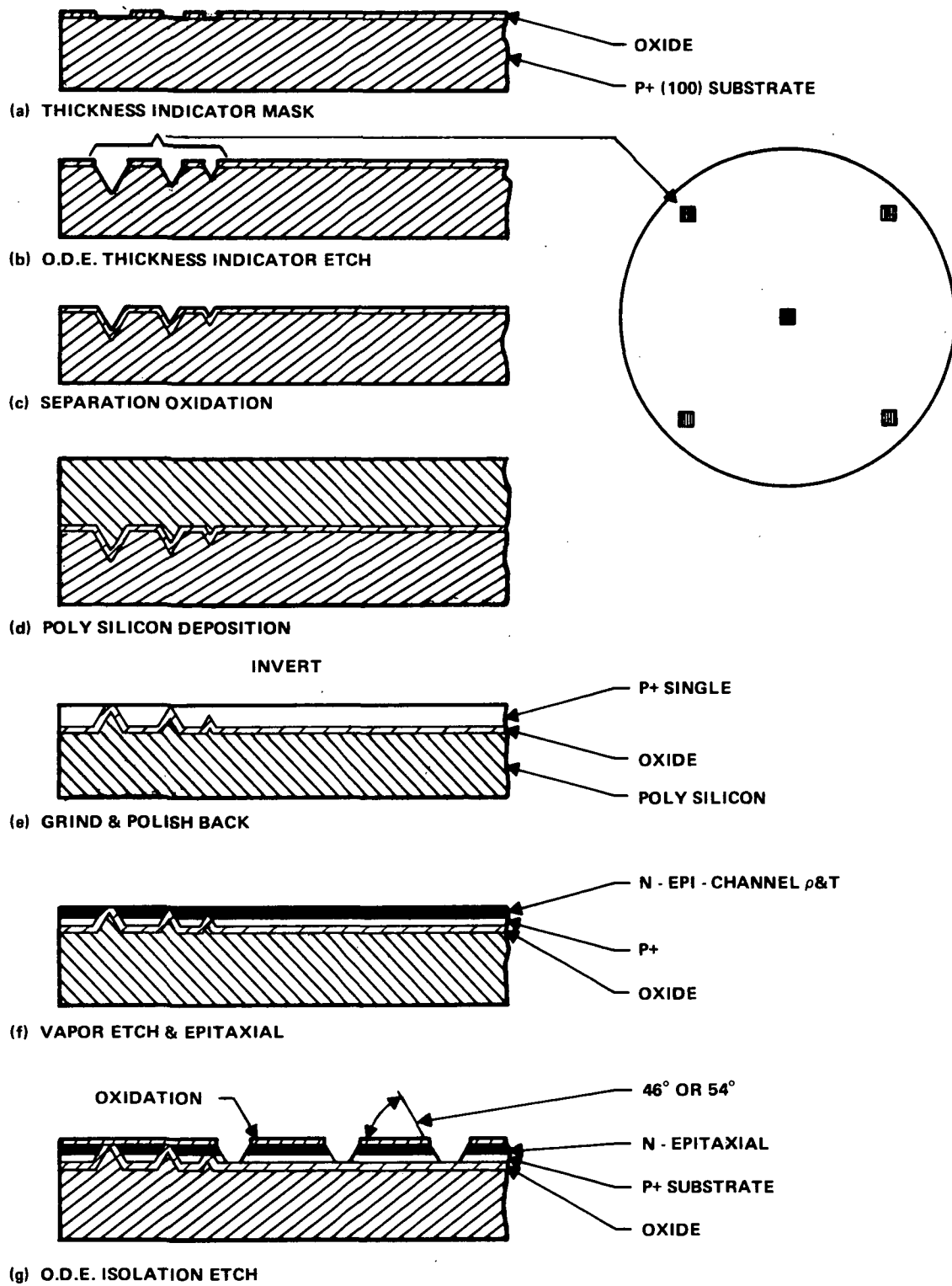
μ_n = channel mobility in $\text{cm}^2/\text{V-s}$

q = electronic charge in coulombs

Z_c = channel width in mils

and

t_c = channel thickness (at $V_{gc} = V_{on}$) in mils



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Figure 23. Raised Dielectric Isolation Process

The channel width required to meet the "on" resistance specification of 40Ω at 100°C is related to the "on" channel thickness by the simplified expression

$$Z_c = 73.2/t_c \text{ mils} \quad (\text{Double Poly})$$

$$Z_c = 58.7/t_c \text{ mils} \quad (\text{Raised Structure})$$

These relationships are illustrated by the curves in Figure 26. The difference in the expressions used for the double poly and raised structure is related to the increase in channel resistivity of the double poly structure by the p^+ diffusion tail.

The relation between V_{po} , V_{on} , and t_{on} can be expressed analytically for an ideal JFET. This relation for a practical device can be read from the Lawrence and Warner Capacitance Curves,⁸ which relate depletion into the channel to bias voltage for an $\text{erfc}(x)$ diffusion into a uniformly doped substrate.

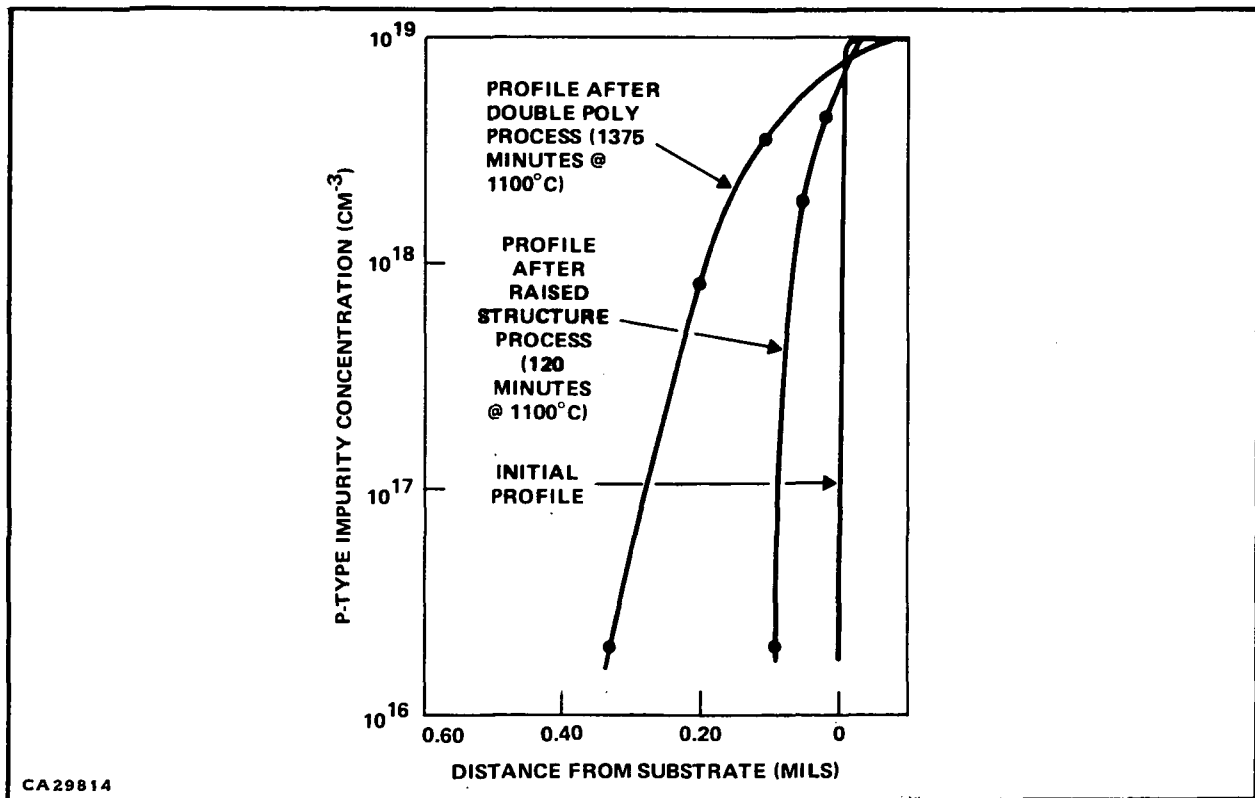


Figure 24. Comparison of Concentration Profile of Back Gate Junction for JFETs Fabricated by Raised and Double Poly-Dielectric Isolation Process

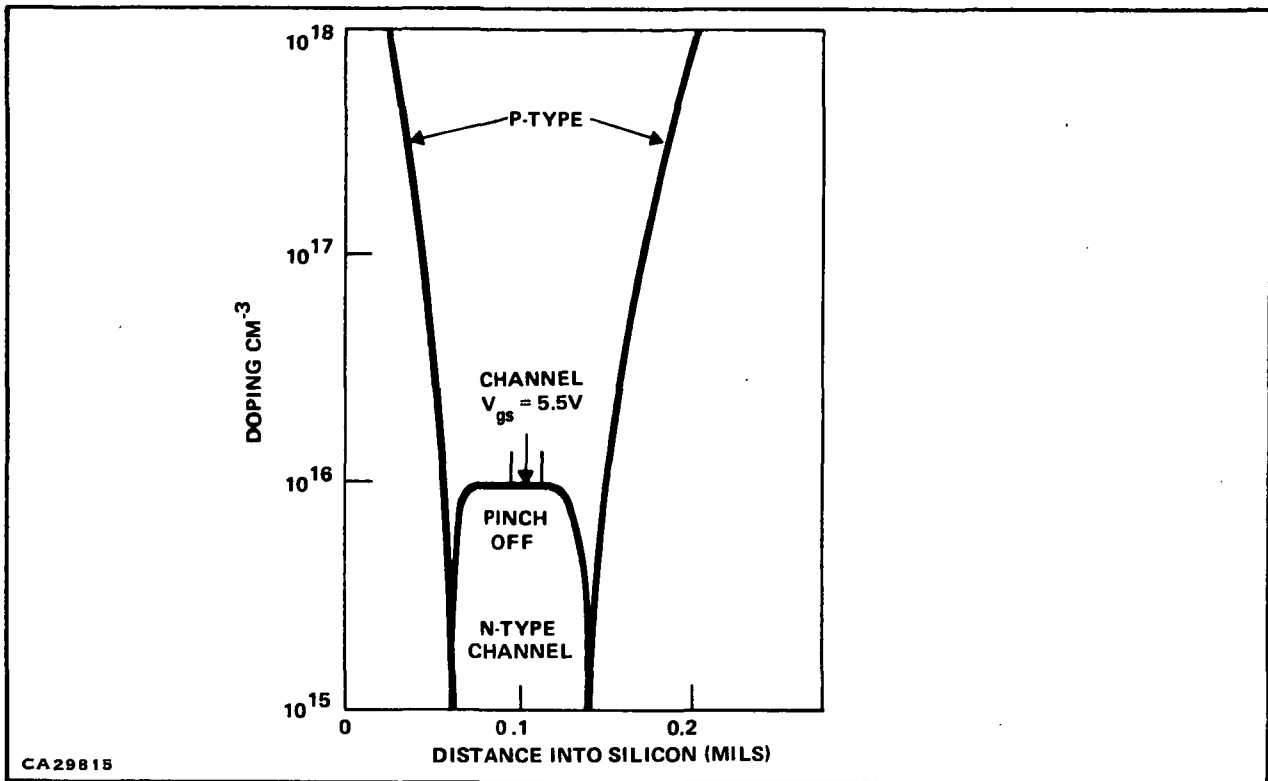


Figure 25. Concentration Profile of JFET Fabricated by Raised Dielectric Isolation Process

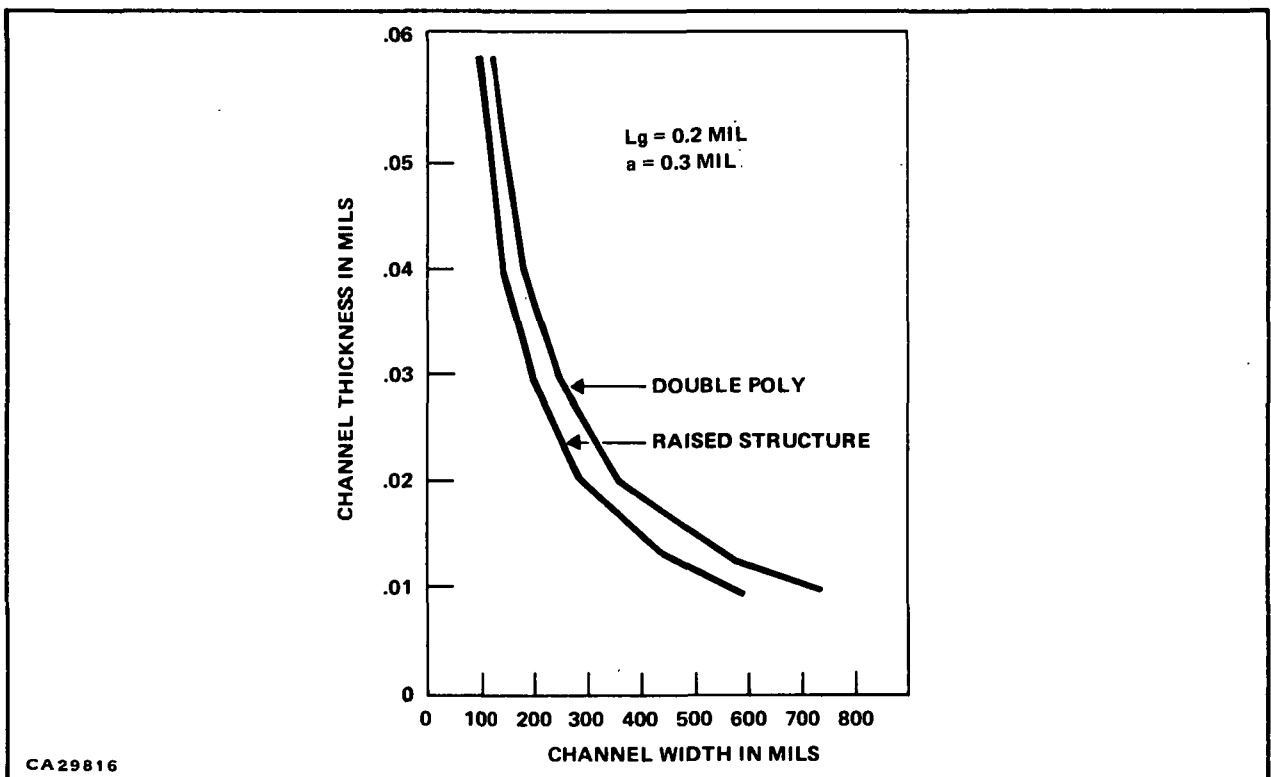


Figure 26. Channel Width as Function of "On" Channel Thickness for Channel Resistance of 40 Ohms

The relation between V_{on} and t_{on} for a given V_{po} can be constructed from these curves and the relation

$$t_{on} = t_{po} - W_{sc1} - W_{sc2} \quad (35)$$

where:

t_{po} = depletion-region thickness required to pinch JFET "off"

W_{sc1}, W_{sc2} = widths of front and back gate depletion into channel

The curves in Figures 27 and 28 illustrate the relation between t_{on} , V_{po} , and V_{on} for both the raised and the double poly structures. The "on" channel thickness and required channel width obtained from these curves for the required $V_{on} = 5.5$ volts, $V_{po} = 8.5$ volts are given by

t_{on} (mil)	Z_c (mils)	
0.129	570	(Double Poly)
0.135	440	(Raised Structure)

The curves in Figures 26, 27, and 28 illustrate the rapid decrease in the required channel width and the increase in design accuracy as V_{on} is reduced from V_{po} .

d. Dielectrically Isolated JFET Geometry

The JFET geometry to be used if the ATOM is fabricated by the double poly-dielectric isolation process is illustrated in Figure 29. The JFET has an effective channel width of 570 mils, and will be realized with 23 cells having a width of 24.8 mils. The JFET will require a dielectrically isolated pocket with dimensions as follows:

Pocket Width = 26 mils

Pocket Length = 24 mils

The gate of the JFET will be contacted with metallization along one side of the device. The source and drain metallization will be brought to buss bars at opposite edges of the device.

The JFET geometry which will be used if the ATOM is fabricated by the raised dielectric isolation process is illustrated in Figure 30. The JFET has an effective channel width of 440 mils, which will be realized with 21 cells having a width of 21 mils. The JFET will require a dielectrically isolated pocket with dimensions as follows:

Pocket Width = Pocket Length = 22 mils

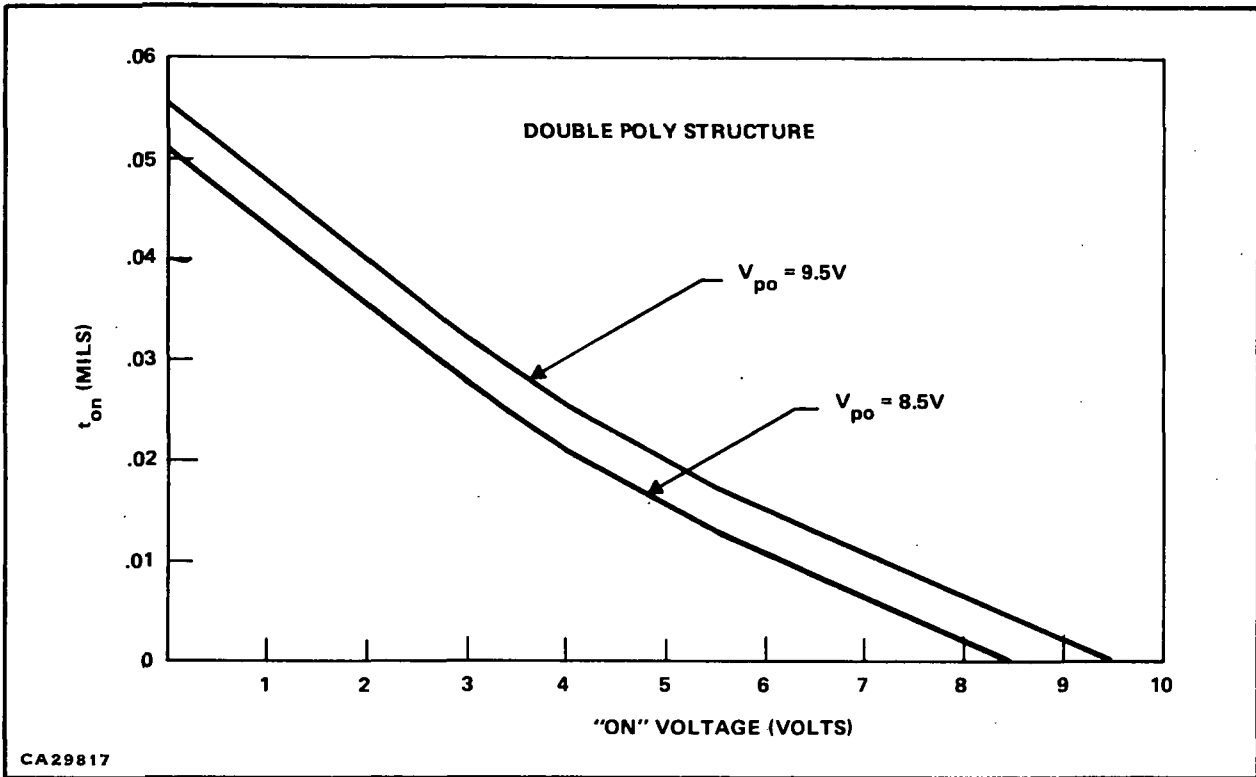


Figure 27. "On" Channel Thickness as Function of "On" Voltage

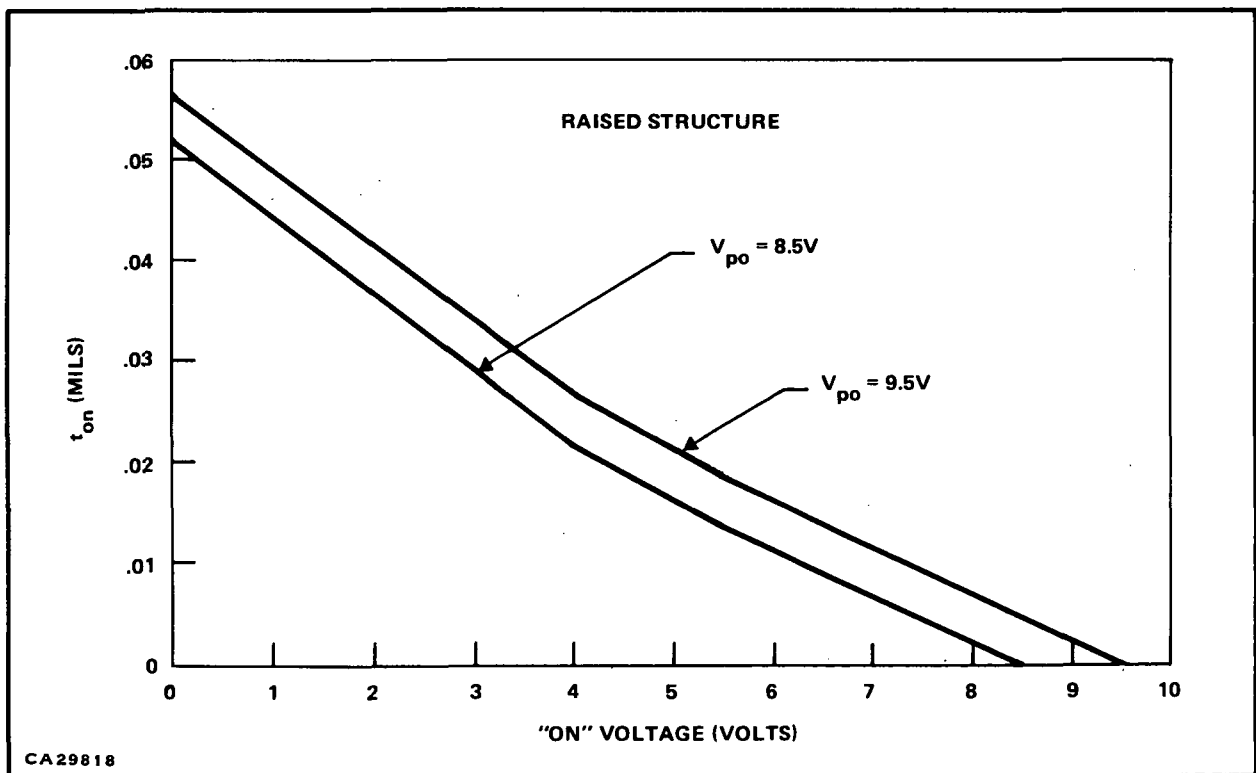


Figure 28. "On" Channel Thickness as Function of "On" Voltage

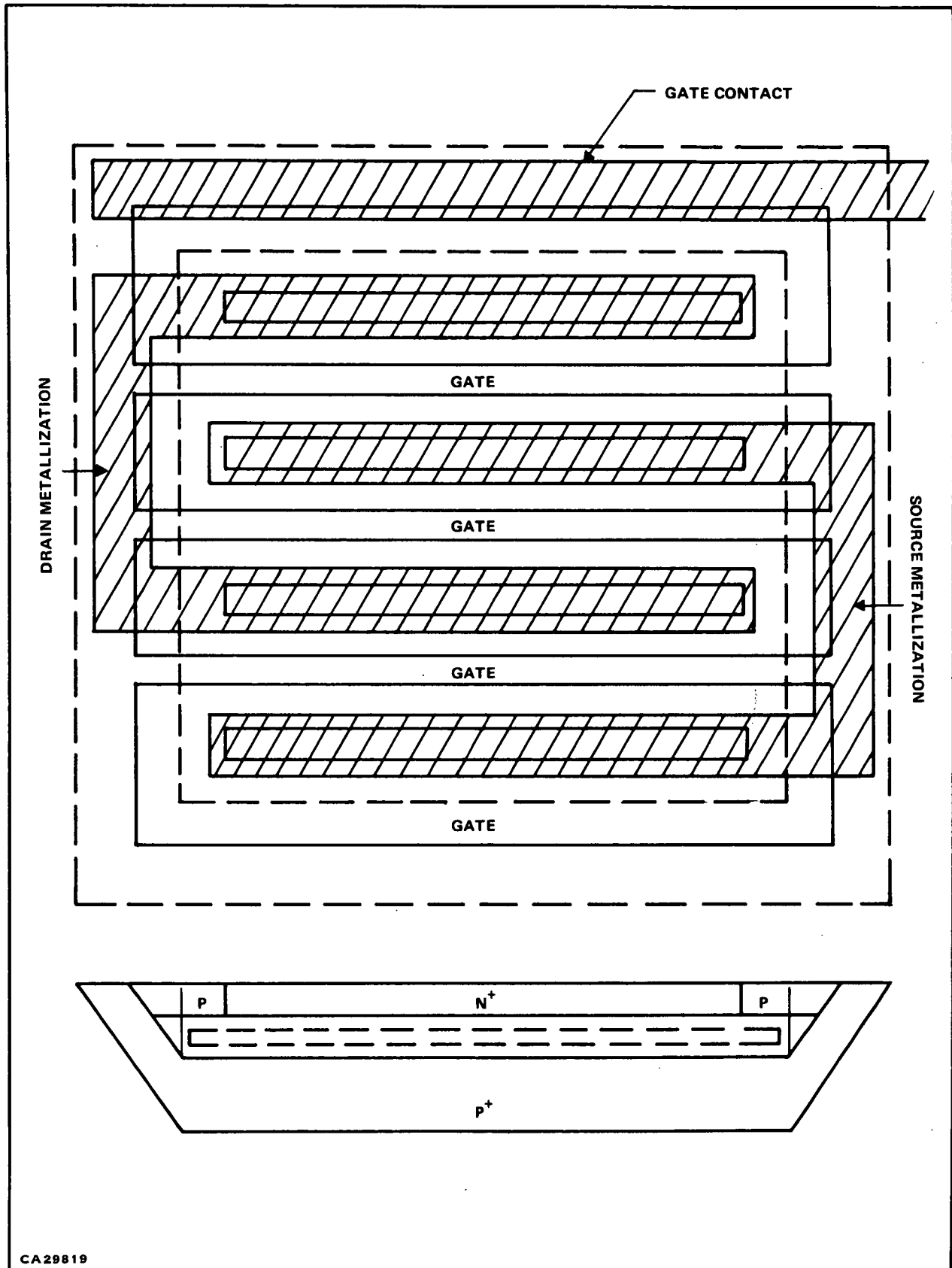
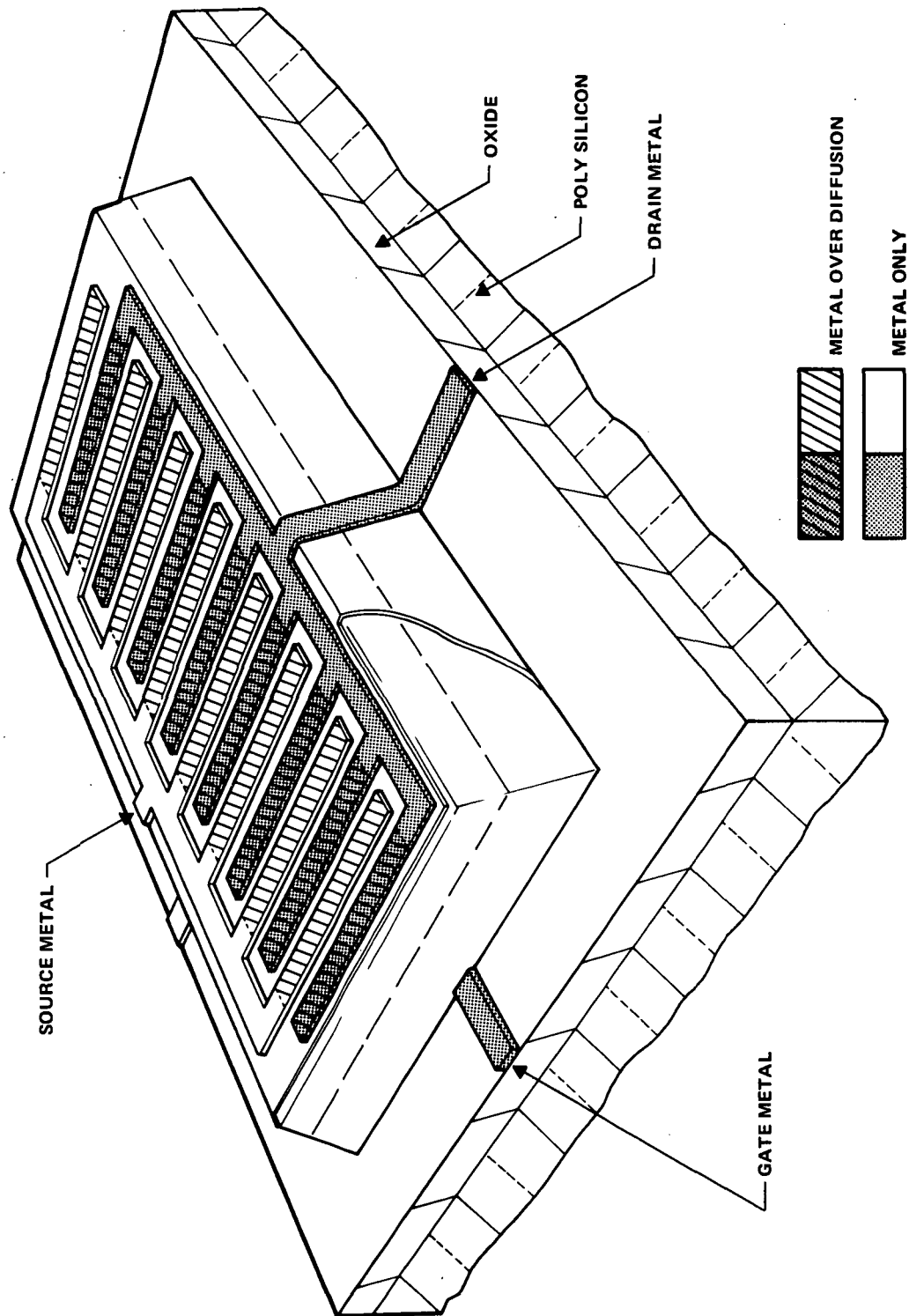


Figure 29. JFET Fabricated by Double Poly-Dielectric Isolation Process



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Figure 30. JFET Fabricated by Raised Dielectric Isolation Process

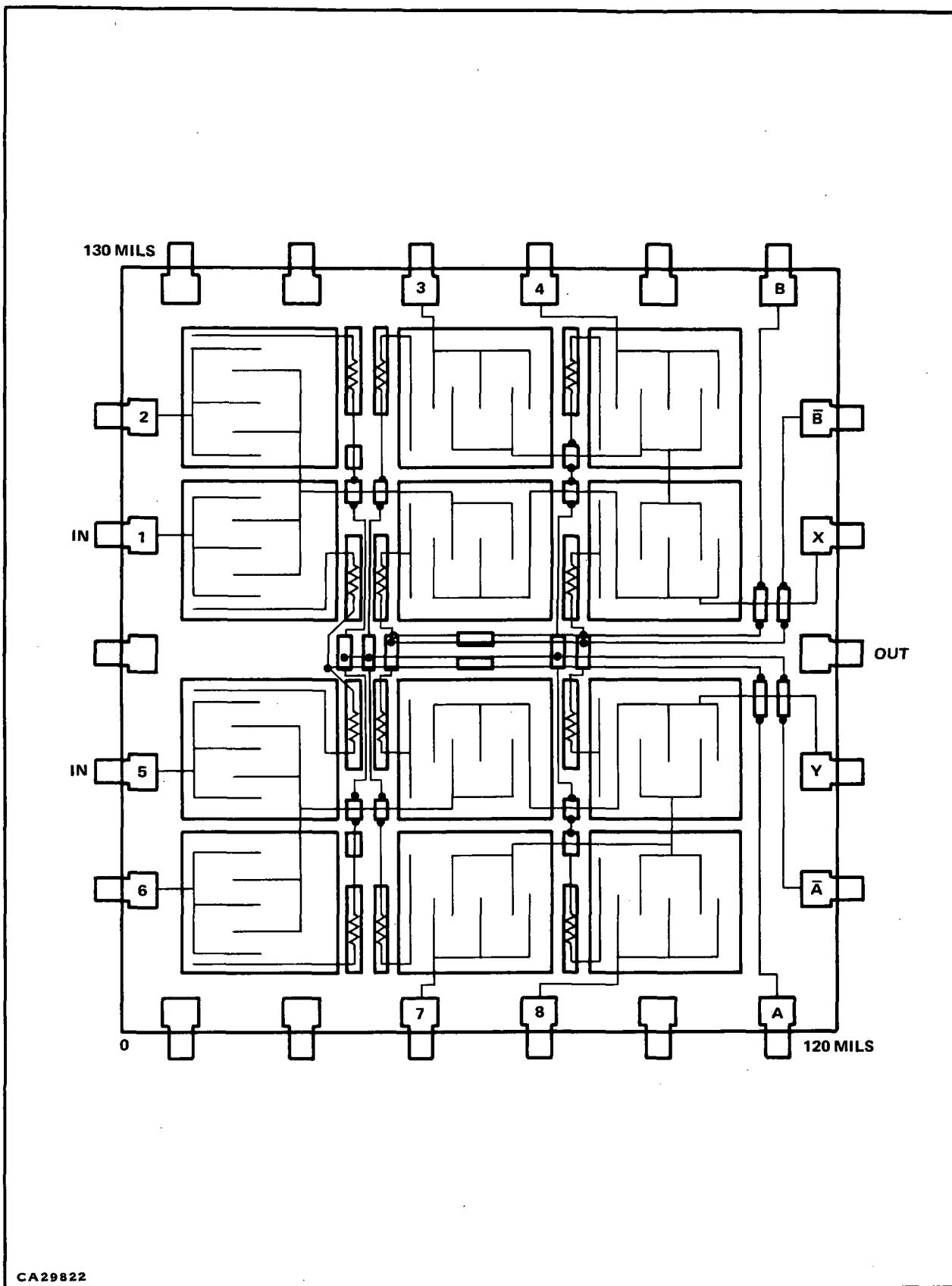


Figure 32. ATOM Circuit Layout for Double Poly-Dielectric Isolation Process

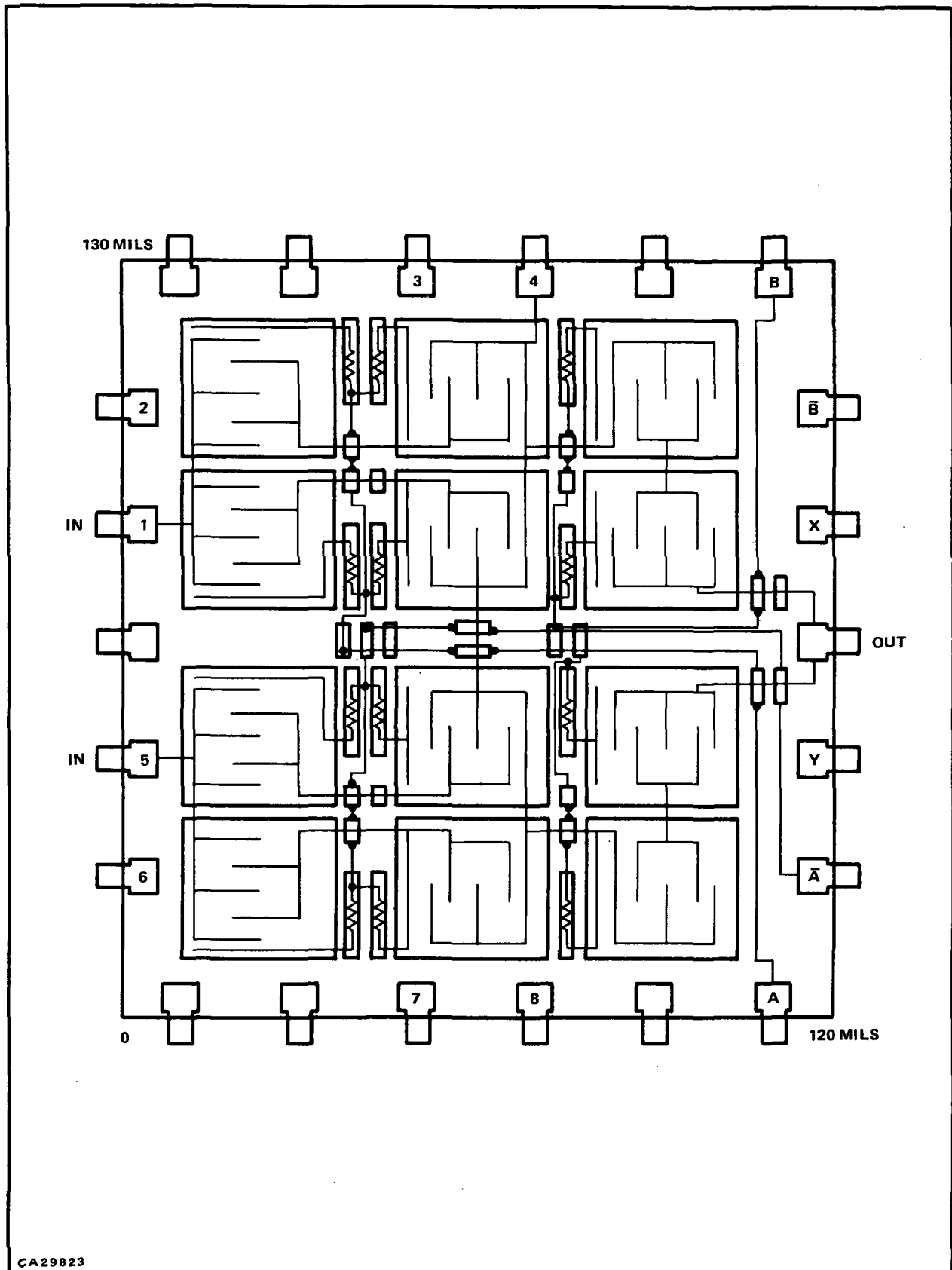
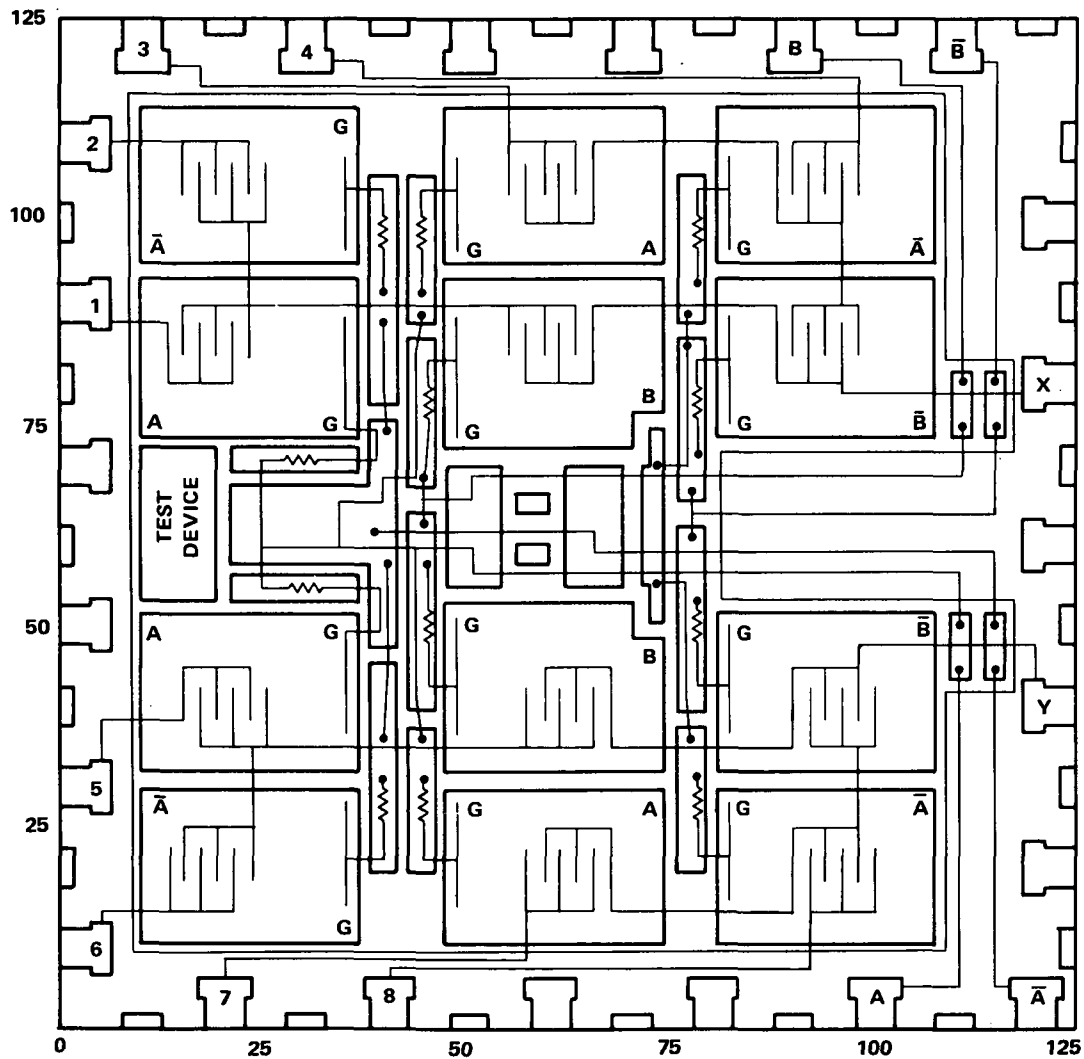


Figure 33. Quad Circuit Layout for Double Poly-Dielectric Isolation Process



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Figure 34. ATOM Circuit Layout for Raised Dielectric Isolation Process

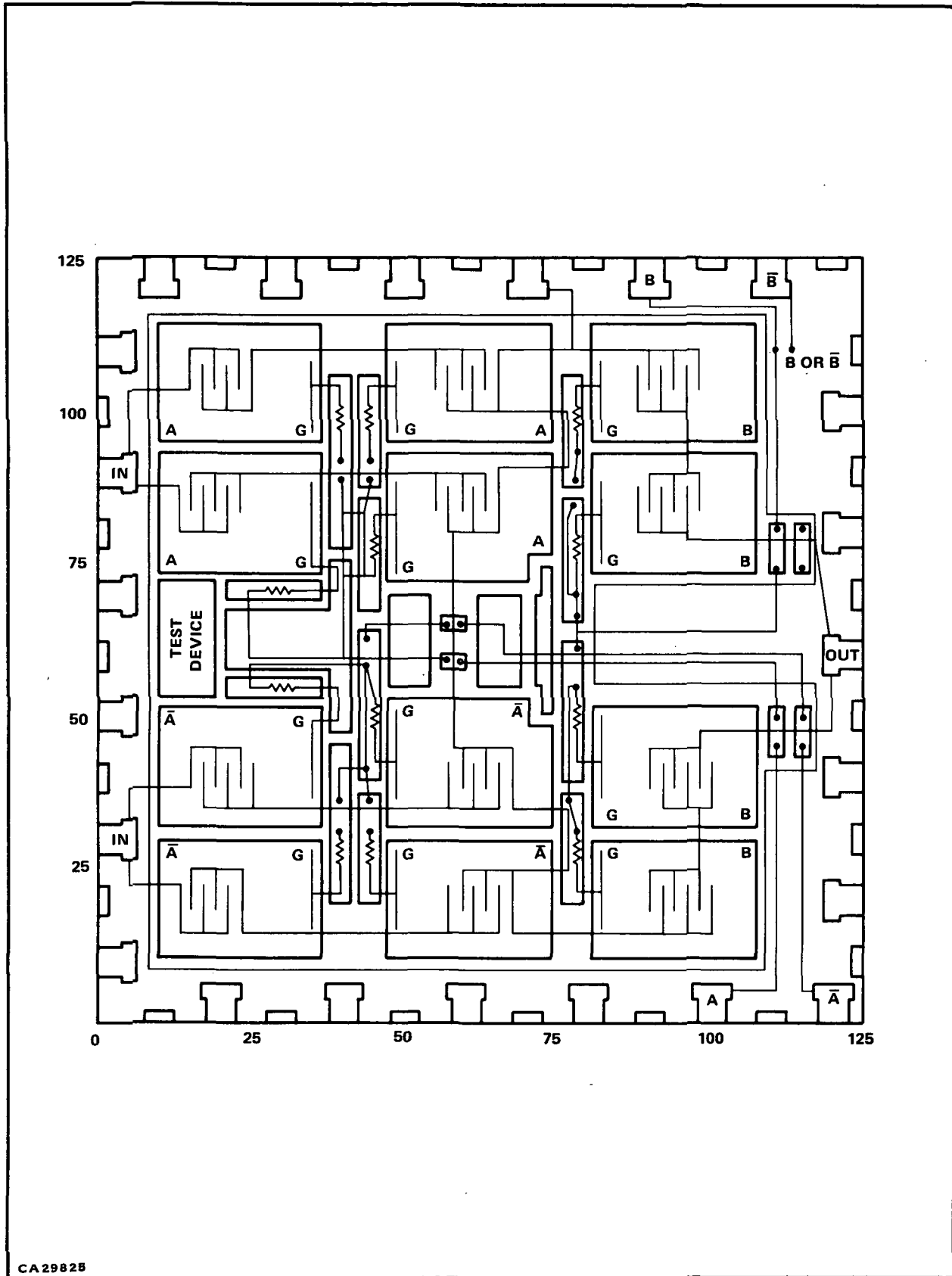


Figure 35. Quad Circuit Layout for Raised Dielectric Isolation Process

JFETs and the width and separation of the metallization on the raised layout required for metal definition in the valleys. The metal in the valleys will be a minimum of two mils in width and will be separated from other metal by a minimum of two mils. The metal definition on the top of the raised mesas will follow the 0.5-mil width, 0.4-mil spacing used in the layout of the double poly bar.

D. TEST DEVICES

The test device proposed to be included on each ATOM bar is illustrated in Figure 36. This test device will have n and p contact regions of 2 X 2 mils, which can be probed prior to metallization. The long gate structure will allow the sheet resistance of the channel to be measured as a function of gate bias. This measurement can be used to characterize the channel resistivity thickness product and the pinch-off voltage of the device. The nominal pinch-off voltage of a slice can, thus, be set prior to metallization. The 0.2 mil channel on the test device will approximate the actual channel of the JFET. Capacitance structures will require a minimum area of 50 to 100 mils² and should not be included on each test bar. The capacitance and tetrode test devices illustrated in Figure 37 will be included at several locations on each slice to assist in evaluating the epitaxial film on the slice.

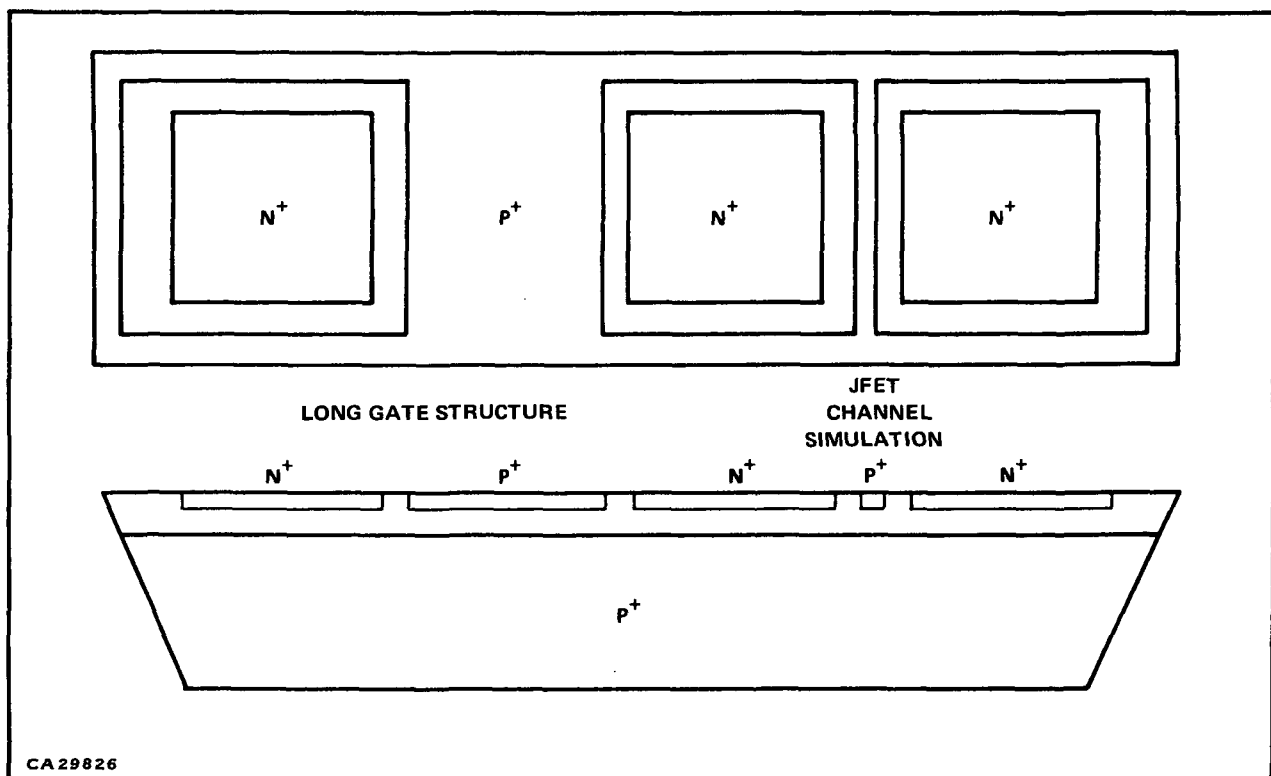
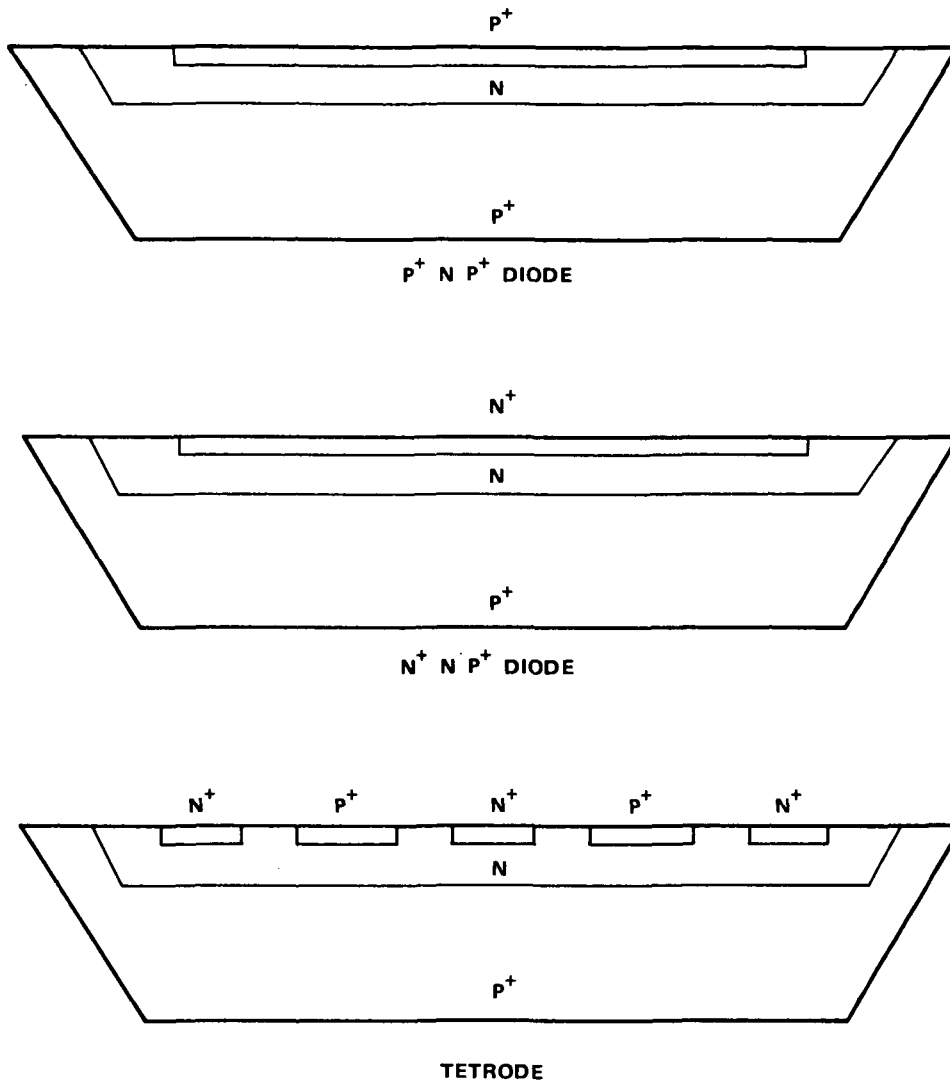


Figure 36. Test Device To Be Included on ATOM Bar



ALL DEVICES HAVE CIRCULAR OR ANNULAR GEOMETRY.

CA29827

Figure 37. Test Devices for Slice Evaluation

SECTION IV

CONCLUSIONS/RECOMMENDATIONS

The ATOM design and layout have been carried out for both the raised dielectric isolation process and the double poly isolation process. The double poly process is a standard production process and was the initially proposed dielectric isolation process. The heat treatment after the epitaxial deposition which is required for isolation by the double poly process

- Linearly grades the back gate channel junction
- Diffuses the back gate junction several lengths of a mil
- Increases the channel resistivity

Control of the diffusion profile of the back gate channel junction over the entire slice is anticipated to be a problem.

The raised structure is a relatively new dielectric isolation process which avoids the complication and heat treatment of the double poly-dielectric isolation process. The epitaxial channel material is deposited late in the dielectric isolation process and has little heat treatment after deposition. The characteristics of the JFET fabricated by the raised process are expected to approach those of a discrete JFET.

The primary problem expected in fabricating the ATOMs by the raised dielectric isolation process is the reliability of the metallization which must run up a 57° ramp to a height of 0.5 mil and the definition of the metal in the etched valleys. Preliminary studys have shown that the metallization problems associated with the raised dielectric process, if any, can be solved by design rules controlling the width and spacing of the metallization in the valleys.

The raised dielectric isolation process is recommended for fabrication of the ATOM because it offers fabrication simplicity, the JFET characteristics do not depend on the details of a diffusion tail, and the JFETs will approach the characteristics of a discrete JFET. In addition, the ATOM can probably be fabricated by the raised process with a higher yield than by the double poly process.

SECTION V

NEW TECHNOLOGY

Not required, as authorized by Contract Unilateral Modification No. 2 of the subject contract, which grants a waiver under 14 CFR Section 1245.104, and Section IV of the New Technology Article is applicable to the subject contract.

SECTION VI

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