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# SOLAR BUS REGULATOR
# AND BATTERY CHARGER FOR
# IMP'S H, I, AND J

## JOHN PAULKOVICH

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## ABSTRACT

Interplanetary Monitoring Probe (IMP) spacecrafts H, I, and J utilize a Direct Energy Transfer (DET) type of power system operating from a solar array source. A shunt type of regulator prevents the bus voltage from exceeding a preset voltage level. The power system utilizes a single differential amplifier with dual outputs to control the battery charge/shunt regulator and the discharge regulator. A two-voltage level, current limited, series charger and a current sensor control battery state-of-charge of the silver-cadmium battery pack. Premature termination of the battery charge is prevented by a Power Available gate that also initiates charge current to the battery upon availability of excess power.

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# SOLAR BUS REGULATOR
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### IMP'S H, I, AND J

## INTRODUCTION

To take advantage of the available solar array power it is desirable to operate at a fixed voltage rather than to allow the voltage to be dependent upon the battery voltage. Previous Interplanetary Monitoring Probe (IMP) spacecrafts used a shunt charge system in parallel with the solar array as shown in Figure 1. Battery voltage varied from 19.8 volts (full charge voltage) to 12.00 volts (under-voltage trip point). Power available to charge the battery and to supply the load is dependent upon the battery charge voltage. Figure 2 illustrates a typical solar array I-V curve, also illustrated are the power curve and voltage operating range. When battery voltage is up to 19.8 volts then we can utilize up to 97.5% of the available solar array power of this particular solar array, but unfortunately when solar array voltage is loaded down to 12 volts due to high power requirements the solar array power is reduced to 62% of available power, this change in voltage level could very likely be a point of diminishing returns. Let's take a hypothetical case. If we assume that the battery is fully charged (battery voltage at 19.8 volts) and the spacecraft loads amount to 98% of the available power, the bus voltage will remain at 19.8 volts. The excess power amounting to 2% will be dissipated in the shunt regulator. Suppose that there is a momentary demand of power such that we dip into the battery to supplement this additional power. The battery which has been setting at 19.8 volts will now drop to approximately 16 volts, nominal battery load voltage. At this 16 volt level, power from the solar array has decreased to approximately 82% of the available solar array power. Even when momentary high power demand is no longer present, the battery will be "locked" in a discharge mode. As battery voltage decreases, less and less solar array power is utilized and the condition continues to avalanche. The most desirable condition would be to maintain operation at the peak power point of the solar array, but this requires elaborate sophisticated circuitry. Additional weight and complexity outweigh the advantages. The next best thing to do is to maintian operation at a fixed potential on the solar array, this is the system selected for the IMP's H, I, and J spacecrafts.

## FIXED POTENTIAL SOLAR BUS REGULATOR

Figure 3 illustrates a block diagram of the power system. A series charge method is incorporated to charge the battery, a shunt regulator is shown to
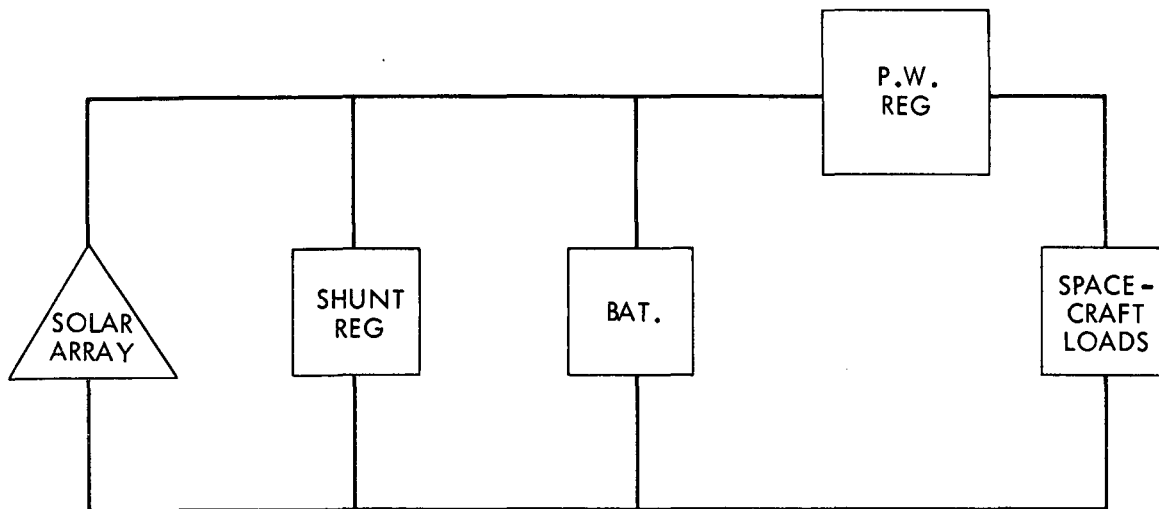
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Figure 1. Block Diagram of Previous IMP's Charge and Power System.

prevent the main bus from increasing excessively and the boost regulator comes "on" if load demand exceeds solar array power or if shadow conditions exist. What are the problems associated with this type of circuit? First the series charger or shunt regulator must not be "on" if we are operating in the boost mode. Boost should not be "on" if we are charging the battery. If excess solar power is low and the battery needs charging then the shunt regulator should not be wasting this essential energy.

Regulation of main bus voltage is the primary objective. When excess power is available we want to charge the battery first and then dump the excess. When insufficient power is available then the shunt and charge circuits should be "off" and boost regulator should come "on" to maintain the bus voltage. Bus voltage on the IMP spacecrafts is a nominal 28 volts ± 2%. If main bus voltage is exactly 28 volts then neither circuit should be "on" and solar array current goes directly to the load. When neither circuit is "on" then operation is in a so called "dead band". It was decided that a ± 0.5% dead band would be sufficient. It is also desirable to have a single bus sensing control circuit to control both shunt/charge and boost regulators.

CONTROL CIRCUIT, MAIN BUS REGULATOR

Figure 4 illustrates what we selected as desirable output characteristics from a control circuit. Shunt/charge output from the control circuit is zero until the bus voltage gets to 28.0 volts + 0.5% and then increases linearly to
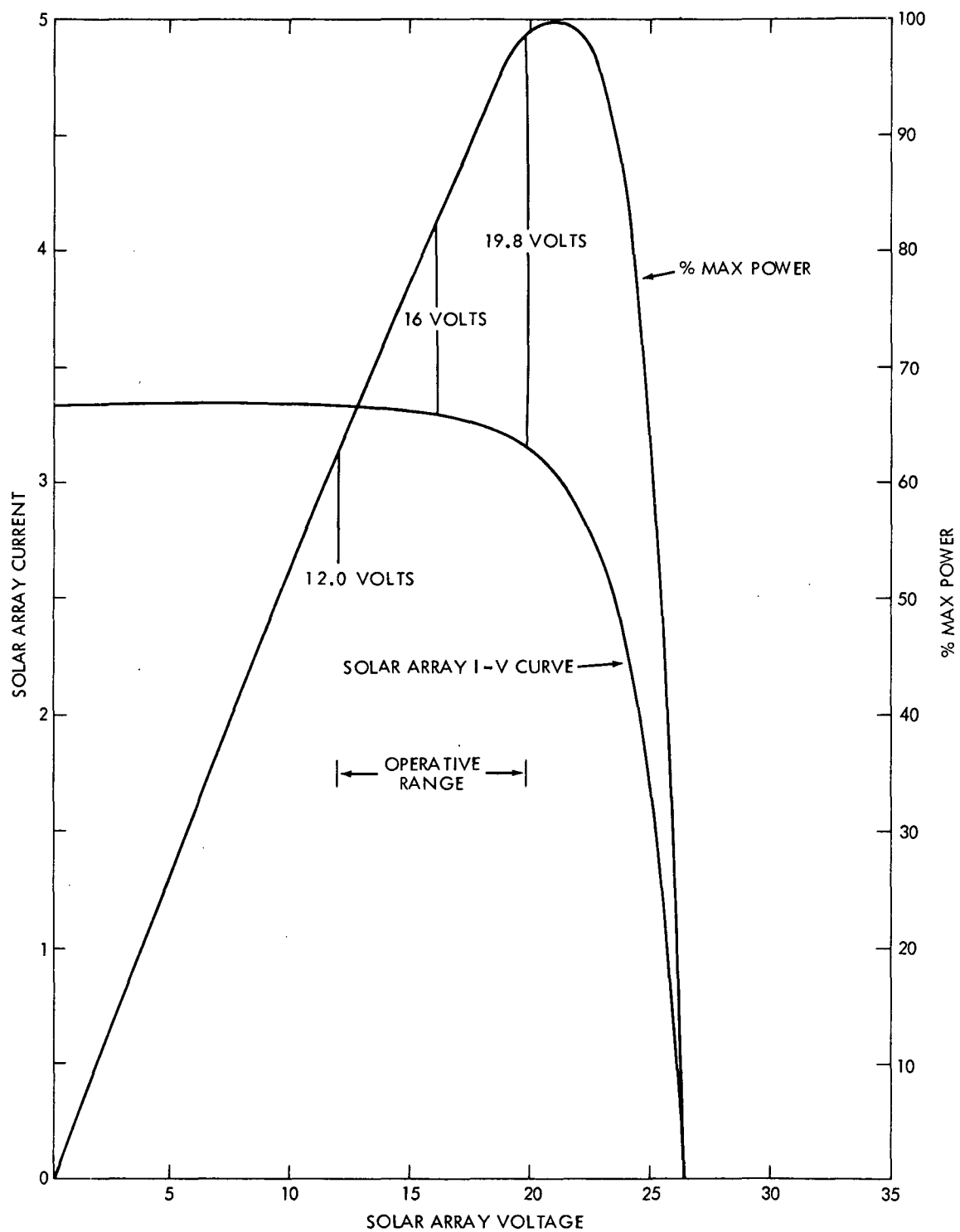
Figure 2. Typical Solar Array I-V Curve.
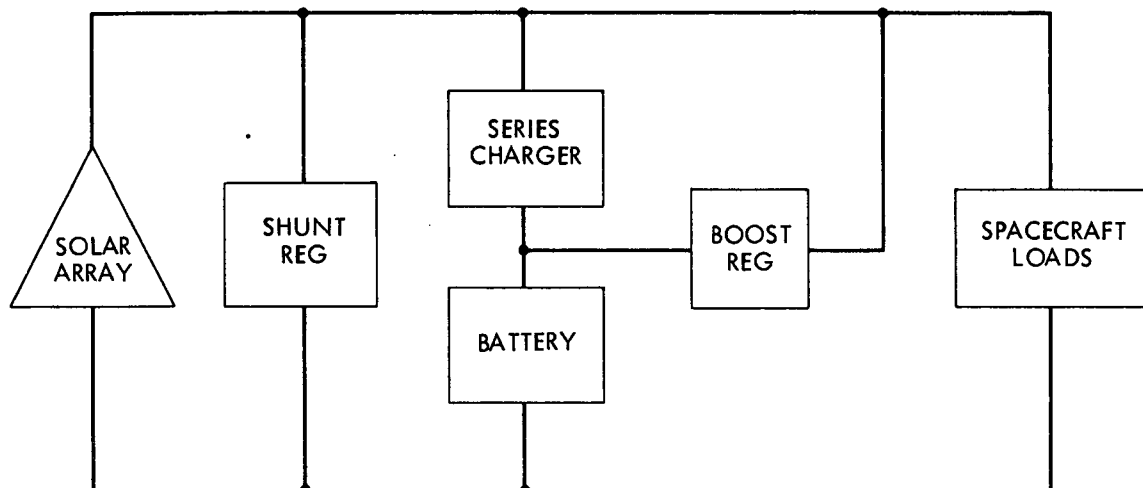
Figure 3. Block Diagram of a Power System That Presents a Constant Potential Load on The Solar Array.
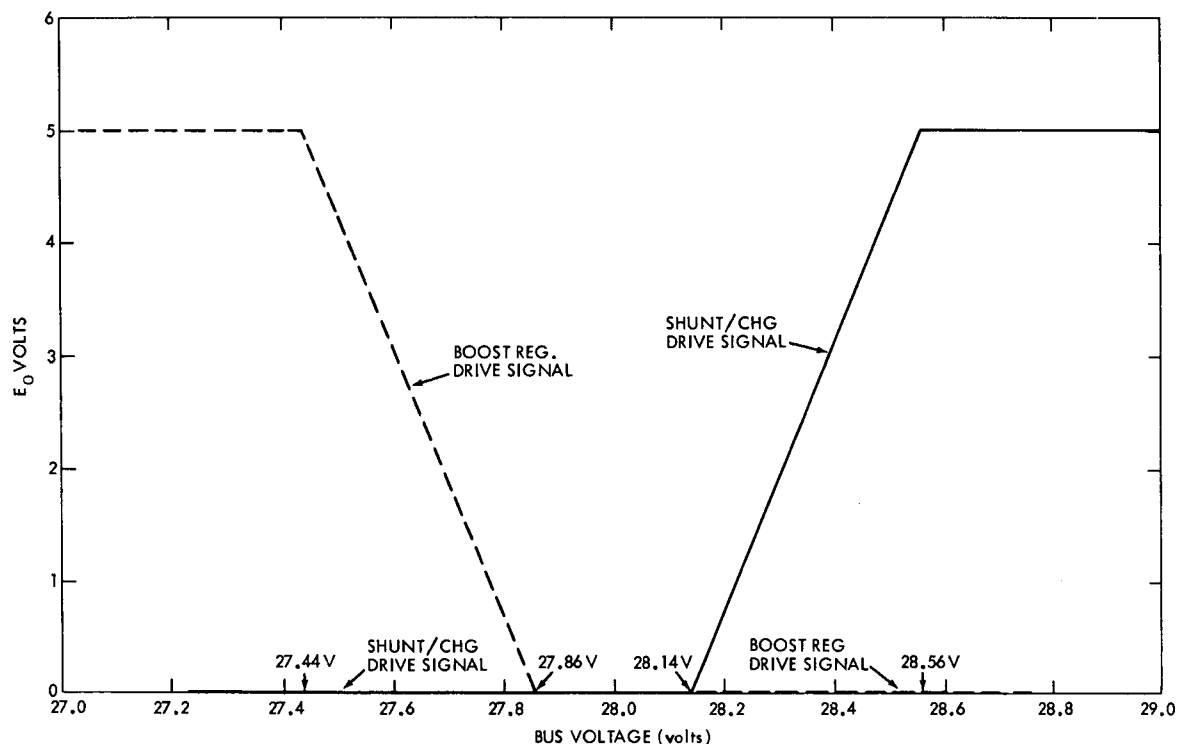


Figure 4. Desirable Output Characteristics From a Control Circuit.

approximately 5 volts at 28.0 volts + 2%. Boost output from the control circuit is zero above 28.0 volts. As the bus voltage drops below 28.0 volts -0.5% boost output increases in a linear manner and should be approximately 5 volts when bus voltage is 28.0 volts -2%.

The circuit designed to accomplish these characteristics is illustrated in Figure 5 and output characteristics are illustrated in Figures 6 and 7. A single reference is used in this circuit. Transistors Q1 and Q2 form a differential amplifier. R1 and R2 are collector load resistors for Q1 and Q2. R6 is the emitter current source for the differential amplifier. Output transistors Q3 and Q4 are cross-coupled between R1 and R2. R7 and R8 represent inputs to the shunt/charge and boost regulators respectively. R3 and R9 compose the voltage divider to the differential amplifier, R4 and R5 are degeneration resistors. If we assume that the bus voltage is exactly 28.00 volts and that base voltage at Q1 is equal to base voltage at Q2 then collector currents of Q1 will be equal to the collector current of Q2. Since R1 is equal to R2, then voltage at the collector of Q1 will be equal to the voltage at the collector of Q2, or zero volts with respect to each other. Under this condition base emitter voltages of Q3, Q4 will be zero, collector currents will be zero, and no voltage will appear across resistors R7 or R8. As bus voltage slowly decreases, Q2 reduces conduction and Q1 increases conduction. Voltage across R2 decreases and voltage across R1 increases. As the difference in voltage approaches 0.5 volts (base-emitter conduction) Q4 starts to conduct. As the voltage is reduced even further, current of Q4 will increase linearly until Q2 turns "off". With Q2 "off" all the current as determined by the current source resistor R6 flows through R1. Emitter follower configuration of Q4 will cause a current to flow through R8 approximately equal to:

$$\frac{V_{R1} - (\text{emitter base voltage of } Q4)}{R2}$$

Resistors R1, R2 were selected for the proper dead band ±0.5%. Degeneration resistors R4 and R5 control the voltage slope, this was selected for 5 volts across R7, R8 (10 k ohm resistors) at the ±2.0% deviation points. Output characteristics shown in Figure 6 bears a very close resemblance to the desired characteristics of Figure 4. Figure 7 is a complete plot of output characteristics of the differential amplifier from zero volts to approximately 32 volts while Figure 6 is an expanded plot around the 28.0 volt region.


BATTERY CHARGER CONSIDERATIONS

The IMP spacecrafts uses a silver-cadmium battery pack composed of 14 series cells of 10 ampere hours capacity. Silver-cadmium cells were selected because of the spacecraft magnetic requirements and 10 ampere hours is sufficient for the normal shadow periods encountered.
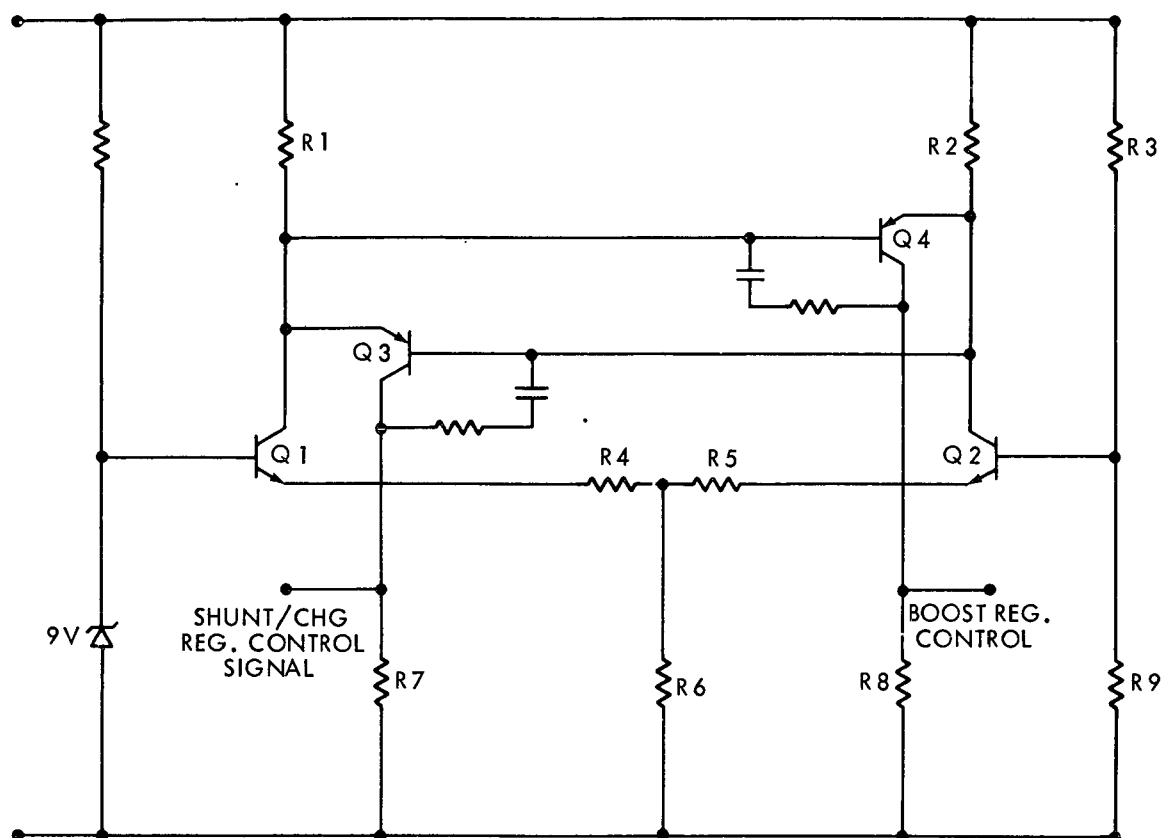
Figure 5. Bus Voltage Sense Differential Amplifier With Two Independant
Outputs.

IMP spacecrafts will be in rather long sunlight periods due to the orbit con-
figuration. Since the battery will have plenty of time to charge, a current limit
of one ampere is incorporated into the charger. There is no sense in slugging
the battery with a high current rate when its not necessary. Also since this
spacecraft will be in these long sunlight periods it is desirable to disable the
battery charger when the battery is fully charged or reduce the charging po-
tential to the open circuit voltage. If the battery is maintained at its charging
potential over long periods of time an unbalance cell condition will be gradually
encountered. This unbalance could cause voltages of some of the cells to reach
their gassing potential and thus build up excessive pressures. To prevent these
excessive pressures from occurring a method of determining when the battery
is fully charged is necessary. Laboratory tests indicate that if a silver-cadmium
battery is charged at a constant potential of 1.505 volts per cell until the charge
current drops to C/100 (where "C" is the ampere-hour capacity) the battery will
be charged to better than 90% of its capacity. The charge cycle can then be
terminated and the battery placed on standby to supply or supplement any load
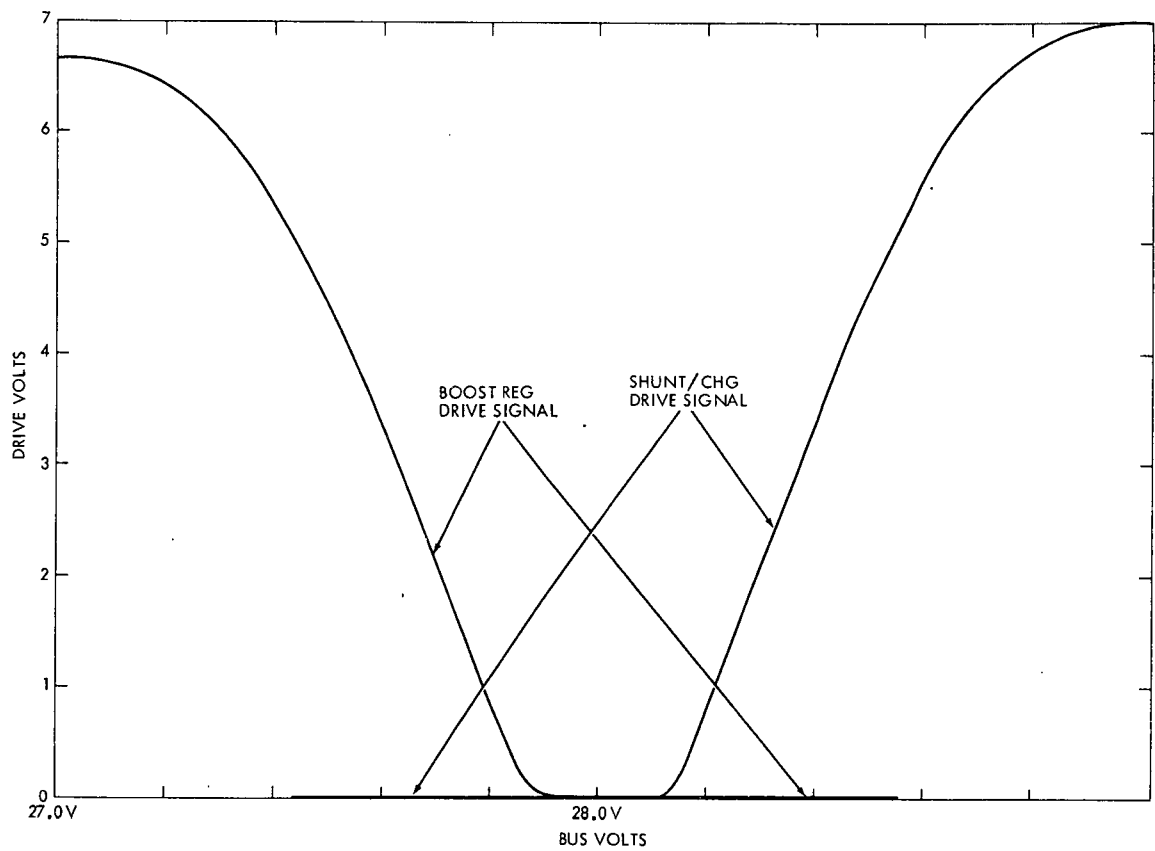demands.

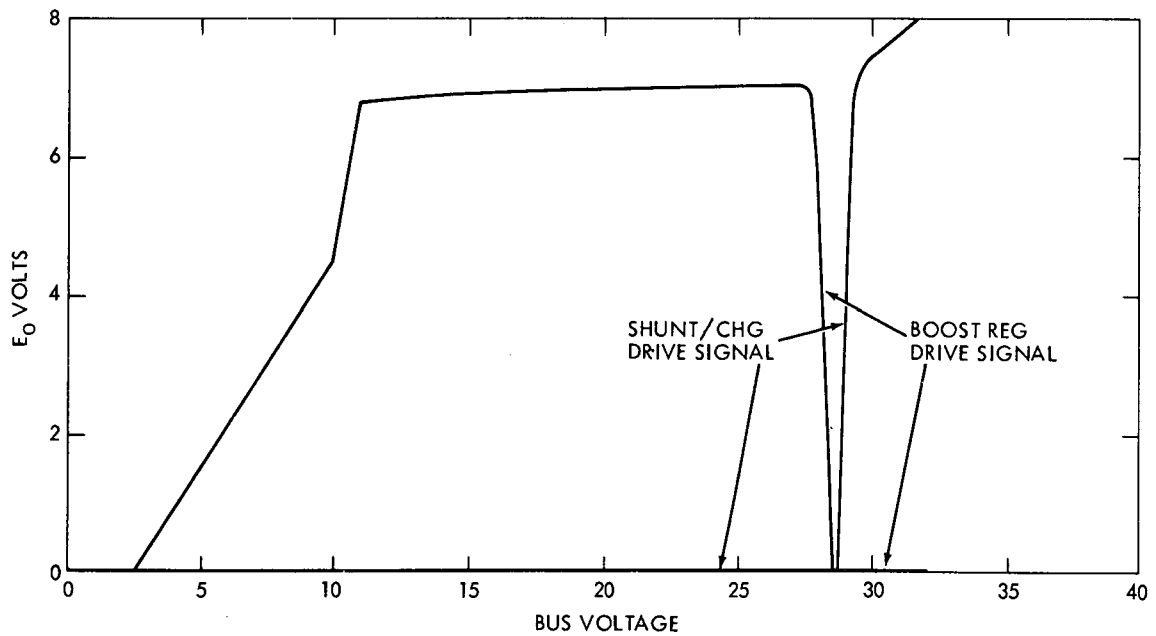Figure 6. Differential Amplifier Output Characteristics, Expanded Scale.



Figure 7. Differential Amplifier Output Characteristics vs Bus Voltage.

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## IMP's H, I, AND J POWER SYSTEM

Figure 8 illustrates a block diagram of the spacecraft power system. The bus voltage sensor provides drive to either shunt/charge or boost circuits depending upon whether bus voltage is greater or less than 28.00 volts. When bus voltage is less than 28.00 volts -0.5% then the boost circuit is driven "on" to maintain bus voltage within 28.00 volts -0.5% and 28.00 volts -2.0%. The battery supplies power to the boost regulator. When the bus voltage is greater than 28.00 volts + 0.5% then the bus voltage sensor will drive the battery charge preference and shunt drive circuit. This circuit is basically composed of two separate drivers, one drives the battery charge circuits and the other drives the shunt circuits. Inputs to these drivers is slightly off-set to ensure that the charge circuits will operate first and then the shunt circuits, thus giving preference to the battery charger if excess power is available. The battery charge preference circuit provides drive to the Battery charge/current limit circuits and also provides a power available signal to the "power available gate".
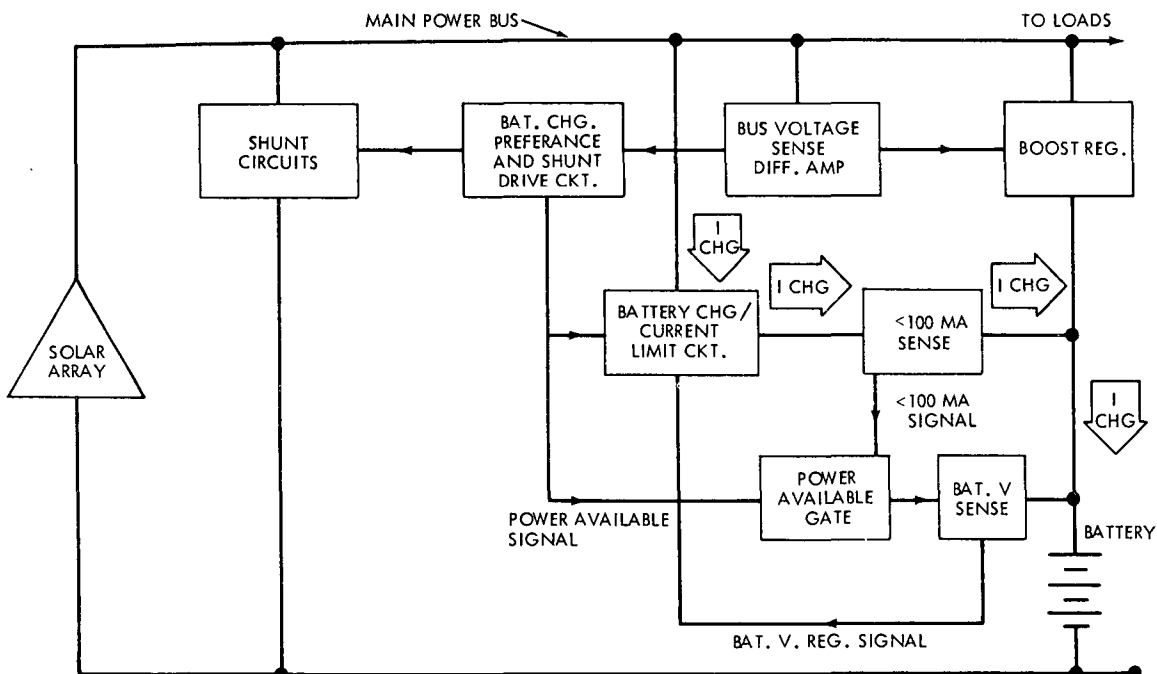


Figure 8. IMP's "H", "I", and "J" Power System, Block Diagram.

Main charging current comes from the main power bus through the "battery charge/current limit" circuit, through the "current sensor" and finally to the "battery". The "current sensor" provides a signal to the "battery voltage sensor" through the "power available gate" if charge current is less than 100 milliamperes. This signal alters battery charging potential from 21.2 volts to 19.9 volts which is just slightly greater than the open-circuit voltage of the battery. The "power available gate" helps to prevent premature tripping of the battery

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voltage sensor to the open-circuit voltage by inhibiting the "power available gate" if no drive is present to the charger.

Figure 9 illustrates the main components of the shunt/charge regulator. Q7a and Q7b, dual transistors in a TO-5 case, and associated components, form a differential amplifier. The two bases are off-set slightly so that Q7b is off with no signal input. Signal from the bus voltage sensor (Figure 5) is applied to the base of Q7b (terminal $e_{in}$). As Q7b starts to conduct, Q4b starts to conduct, this in turn creates a voltage drop across R29. The other end of R29 goes to the battery. Q4b collector also goes to the base terminal of Q17. Q17 is actually three transistors in a darlington configuration with a total beta in excess of 30,000 and therefore presents negligable loading on R29. As Q17 turns on it supplies current to the battery through R67, current sensing and limiting resistor. As Q7b is driven on harder, Q4b is turned on harder thus increasing charge current to the battery and increasing the voltage drop across R16 and R29. At some point D14 and Q4a start to conduct driving dump transistors represented by Qd. With D14 and Q4a conducting a voltage limit is set to the base of Q4b determined by the D14-Q4a diode drops. This current limit establishes a maximum voltage across R16 and R29. This voltage across R29, neglecting base-emitter junctions, is applied to R67 and determines maximum charging rate to the battery. Any increase in drive to $e_{in}$ has negligable effect on the drive to Q4b and is diverted to Q4a, shunt drive transistors. R27 and C6 provide negative feedback in the shunting circuits for stability.

R67 which is the current limiting resistor is also used to monitor battery current to determine when the current has diminished to 100 milli-amperes. The current sensing circuit is composed of transistors Q10a, Q10b, Q12a and Q12b and associated circuitry. The current sensor utilizes a differential amplifier connected in a common base configuration (Q10a and Q10b). This in turn drives a second differential amplifier Q12a and Q12b. Q12a drives Q8 through Q9. When Q8 is turned "on" then additional resistors (R40 and R43) are placed in parallel with the upper leg of the voltage divider (39) of the battery voltage sensing differential amplifier. This voltage divider is composed of R39 in the upper leg and R61 in the lower leg. Q11a and Q11b and associated circuitry form a battery voltage sensing differential amplifier. When Q8 turns "on", series resistor R40 and R43 are connected in parallel with R39 and thus altering charge voltage from 21.1 volts to 19.9 volts. Capacitor C7 delays the transition from 21.1 volts to the 19.9 volt level by a few seconds.

OPERATION OF THE CURRENT SENSOR

Transistors Q10a, Q10b, Q12a and Q12b and the associated circuitry compose a current sensor. Q10a and Q10b are connected in a common base

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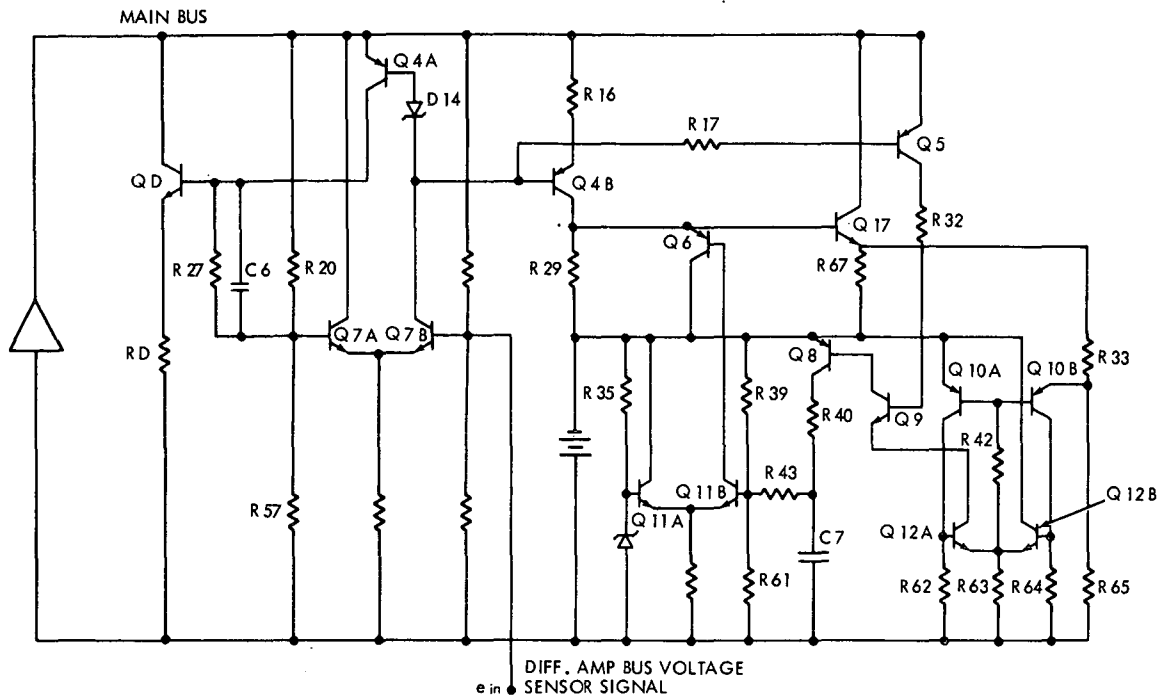
Figure 9. Simplified Schematic of The Major Components in The Shunt/charge Regulator.

configuration and form a differential amplifier. This method is most adaptable for current sensing when operated from a single ended supply. If we assume that there is no charge current through R67 (Q17 off) then the voltage across R67 will essentially be zero. Voltage divider resistors R33 and R65 bias emitter of Q10b in the cut-off direction. Q10a collector current flows through R62 and to Q12a base while Q12b is "off". R42, base drive resistor to Q10a and Q10b, also provides negative feedback to the circuit to make it less beta dependent. Zero current through R67 being less than 100 ma should set the operation of the battery charger to 19.9 volts.

This would be the case of we assumed Q9 to be "on". The purpose of Q9 has not been described. Q9 and Q5 form a "power available gate". That is, if drive is available to Q4b then Q5 is also turned "on" and in turn driving Q9 into conduction. Q9 must be "on" for the current sensor to drive Q8 into conduction to lower the charger potential.

When the battery is charging at some rate greater then 100 ma then Q10b emitter will be more positive than Q10a. Q10b conducting more than Q10a turns "on" Q12b and biases "off" Q12a. As the battery charges, its current decreases. As the current decreases the voltage drop across R67 approaches the voltage drop on R33. Q10a which was "off" begins to conduct as Q10b diminishes conduction. Q12a base is approaching conduction as voltage of Q12b is decreasing.

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When the voltage drop on R67 is equal to the voltage drop on R33 then Q10a and Q10b will conduct equally. Q12a and Q12b will both be conducting. Q12a will turn "on" Q8 through enable transistor Q9.


## PURPOSE OF THE POWER AVAILABLE GATE

When a sil-cad battery is charged to more than 60% of its ampere-hour capacity its open-circuit voltage will be approximately 1.40 volts per cell. If available solar array power decreases to less than 100 milli-amperes the current sensor will alter the charger to 19.8 volts or 1.41 volts per cell. Battery will remain in this state of charge unless some means are incorporated into the charger to prevent this false tripping to the open circuit voltage prematurely. A "power available gate" performs this function satisfactorily. The "power available gate" should really monitor presence of dump current instead of excess current as is done on the IMP spacecrafts but due to the high nominal power levels and power fluctuations encountered the difference is insignificant permitting simplification of the circuitry. When the average excess current decreases to less than 100 milli-amperes the spacecraft current fluctuations would actually cause the charge currents to vary between zero and some level. When excess current goes to zero the charger turns "off" the power available gate transistor Q5 disabling the current sensor drive to Q8. With Q8 "off" C7 will charge to the same potential as the base of Q11b. Presence of available power will turn "on" Q4b and Q17 permitting up to one ampere to go to the battery. Battery potential will increase toward 21.1 volts plus. Since battery voltage increases abruptly, and base voltage of Q11b increases abruptly and the capacitor C7 holds its charge for a moment, then there exists a potential across R43. Base of Q11b being more positive in potential than the voltage on C7 gives a partial effect of R43 being in parallel with R61 permitting charge voltage to slightly exceed the preset charge level. This shot in the arm permits the battery to take a momentary charge even if the battery is fully charged. This momentary charge permits the current sensor to trip to the charge mode. When the battery is not fully charged, the charger will charge the battery until the current decreases to 100 milli-amperes at which time the current sensor will cause the charge voltage to change to the 19.8 volt charging level. This "shot in the arm" effect improves the charger characteristics, when the charge current goes to zero then in all likelihood the boost regulator has dipped into the battery. Reinstatement of charge current will guarantee start of charge at the upper voltage level permitting the battery to charge through its normal cycle.

## IMP's H, I, AND J, SOLAR BUS/BATTERY CHARGE REGULATOR

Figure 10 illustrates the complete schematic of the "solar bus/battery charge regulator". Power from the solar array comes into the circuit on pins 1 through 6 on the right hand connector (main bus). Shunt portion of the current goes to the connector on the left side of the schematic, pins 34 through 45. These pins are connected to the collectors of 12 dump transistors located strategically around the spacecraft to radiate excess power to outer space. Only one dump transistor and resistor is illustrated for simplicity.

Charge portion of the current comes from the main bus, pins 1 through 6, through diode connected transistors Q14 and Q15, then through Q17 the series pass transistor, through R67 the current limiting and sensing resistor, and finally to the battery, pins 7 through 12 of the right side connector.

The main bus voltage sensing differential amplifier is composed of transistors Q1a and Q1b. These transistors drive Q2 and Q3, the shunt/charge drive transistor and discharge regulator drive transistor respectively.

Transistors Q11a and Q11b compose the battery voltage sensing differential amplifier. When battery voltage reaches the preset potential Q11b starts to turn "on" providing drive to Q6. Q6 bypasses the current of the voltage establishing resistors (R22, R23, R29) and thereby reducing the drive to Q17 and in turn reducing charging current rate. When the battery is fully charged Q6 will shunt the drive as necessary to maintain battery voltage at the preset level.

Transistors Q10a and Q10b compose a single ended current sensor. The "current sensor" drives transistors Q12a and Q12b (a second differential amplifier). Q12a drives Q8 (if Q9 is "on") to alter the charging potential to the open-circuit potential of the battery.

### SHUNT MODE OPERATION

During shunt operation, a drive signal from the differential amplifier drives Q7b, Q7b provides drive to Q4a. Q4a in turn provides drive to a darlington pair composed of Q13a and Q13b. This darlington pair provides drive to all dump transistors through isolation diodes D2 through D13. The dump transistors will conduct as necessary to maintain main bus voltage within 28 volts + 0.5% and 28 volts plus 2%. The 12 dump transistors are all connected in an emitter follower configuration and thus ensuring equal power distribution.

Figure 10. Schematic, IMP's "H", "I", and "J", Shunt/Charge Regulator.

## BATTERY ISOLATION

Q14 and Q15 are germanium transistors connected in a diode configuration to prevent battery current from flowing through transistors Q16a, Q16b, and Q17 in the reverse direction if solar array power should be zero and the boost regulator disconnected. Diode D16 protects Q4b in the same manner.

Resistor R27 and capacitor C6 provide negative feedback to the shunt regulator for stability. Resistor R66 and capacitor C10 provide negative feedback in the charge portion of the regulator for stability.

## SUMMARY

The Solar Bus and Battery Charge Regulator of the IMP's H, I, and J spacecrafts will permit the battery to charge at one ampere rate until battery voltage reaches 21.1 volts. Battery current will taper off until it is down to 100 milliamperes at which time charge voltage will change to 19.9 volts. Charge voltage will remain at 19.9 volts until a demand is placed upon the battery at which time charge voltage will be reset to the 21.1 volt level. Upon availability of excess power the battery will again charge at the upper voltage level until battery current again reduces to 100 milli-amperes. The shunt portion of the regulator will dump all excess power not required by the battery and spacecraft.

This system of battery charging essentially treats the battery with tender loving care. The maximum charge rate is limited to one tenth of the ampere hour capacity, and when battery charge rate is reduced to one hundreth of the ampere-hour capacity battery charge potential is altered to a voltage slightly above the battery open circuit voltage. This reduces the charge current to zero and the battery essentially sits on standby at this lower voltage level. This lower voltage limit maintains the battery in a full charge state and at the same time prevents cell unbalance from occurring in the battery pack. Hopefully, with this type of treatment, the battery will last many years.

IMP I BATTERY CHARGE / SOLAR BUS REG PARTS LIST

| | | | | | | | | | | |
|---|---|---|---|---|---|---|---|---|---|---|
| R1 | 6.2K | 1w CC | R36 | 1.5K | RNG5D | TBD | C1 | 1200pf | 100V | |
| R2 | 2.74K | RNG5D | R37 | 6.49K | RNG5D | TBD | C2 | 1200pf | 100V | |
| R3 | 2.74K | RNG5D | R38 | 220K | 1/2w CC | | C3 | 1 MFD | 75V 350D | |
| R4 | 1.30K | RNG5D TBD | R39 | 11K | RNG5D | | C4 | 1 MFD | 75V 350D | |
| R5 | 6.81K | TRIM RNG5D TBD | R40 | 64.9K | TBD | | C5 | 680pf | 200V | |
| R6 | 8.08K | RNG5D | R41 | 120K | 1/2w CC | | C6 | 1200pf | 200V | |
| R7 | 100Ω | 1/2w CC | R42 | 10 MEG | 1/2w CC | | C7 | 22 MFD | 75V | |
| R8 | 150Ω | 1/2w CC | R43 | 49.9K | RNG5D | | C8 | 55 MFD | 45V 16K503AB5 | |
| R9 | 150Ω | 1/2w CC | R44 | 5.6K | 1w CC | | C9 | 55 MFD | 45V | |
| R10 | 2.05K | RNG5B | R45 | 5.6K | 1w CC | | C10 | 1000pf | 200V | |
| R11 | 2.37K | RNG5D | R46 | 5.6K | 1w CC | | | | | |
| R12 | 8.87K | RNG5D | R47 | 5.6K | 1w CC | | D1 | 1N939B | | |
| R13 | 20K | 1/2w CC | R48 | 5.6K | 1w CC | | D2 | 1N645 | | |
| R14 | 3.09K | RNG5D | R49 | 5.6K | 1w CC | | D3 | 1N645 | | |
| R15 | 20K | 1/2w CC | R50 | 5.6K | 1/2w CC | | D4 | 1N645 | | |
| R16 | 499Ω | RNG5D TBD | R51 | 5.6K | 1w CC | | D5 | 1N645 | | |
| R17 | 180K | 1/2w CC | R52 | 5.6K | 1w CC | | D6 | 1N645 | | |
| R18 | DELETE | | R53 | 5.6K | 1w CC | | D7 | 1N645 | | |
| R19 | 220Ω | 1/2w CC | R54 | 5.6K | 1w CC | | D8 | 1N645 | | |
| R20 | 14K | RNG5D | R55 | 5.6K | 1w CC | | D9 | 1N645 | | |
| R21 | 14K | RNG5D | R56 | 2K | 2w CC | | D10 | 1N645 | | |
| R22 | 2.7K | SENSISTOR 1/8w | R57 | 14K | RNG5D | | D11 | 1N645 | | |
| R23 | 2.7K | SENSISTOR 1/8w | R58 | 26.7K | RNG5D | | D12 | 1N645 | | |
| R24 | 100K | 1/2w CC | R59 | 14K | RNG5D | | D13 | 1N645 | | |
| R25 | 1K | 1/2w CC | R60 | 10K | RNG5D | | D14 | 1N966B | | |
| R26 | 10K | 1/2w CC | R61 | 9.09K | RNG5D | | D15 | 1N966B | | |
| R27 | 110K | 1/2w CC | R62 | 100K | 1/2w CC | | D16 | 1N645 | | |
| R28 | 1K | 1/2w CC | R63 | 51K | 1/2w CC | | D17 | 1N939B | | |
| R29 | 2.49K | RNG5D | R64 | 100K | 1/2w CC | | | | | |
| R30 | 10K | 1/2w CC | R65 | 22.1K | RNG5D | | Q1 | 2N2060-2 | | |
| R31 | 2.7K | 1/2w CC | R66 | 100Ω | 1/2w CC | | Q2 | 2N2907A | | |
| R32 | 1 MEG | 1/2w CC | R67 | 2Ω | NHG-5 DALOHM | | Q3 | 2N2907A | | |
| R33 | 274Ω | RNG5D TBD | | | | | Q4 | G2N3350 | | |
| R34 | 634Ω | RNG5D TBD | | | | | Q5 | SMO292 | | |
| R35 | 3.9K | 1w CC | | | | | Q6 | TX2N2905A | | |
| | | | | | | | Q7 | 2N2060-2 | | |
| | | | | | | | Q8 | SMO292 | | |
| | | | | | | | Q9 | 2N718-A-2 | | |
| | | | | | | | Q10 | G2N3350 | | |
| | | | | | | | Q11 | 2N2060-2 | | |
| | | | | | | | Q12 | 2N2060-2 | | |
| | | | | | | | Q13 | GMHM2201 | | |
| | | | | | | | Q14 | G2N1908 (HR) | | |
| | | | | | | | Q15 | G2N1908 (HR) | | |
| | | | | | | | Q16 | GMHM2201 | | |
| | | | | | | | Q17 | G2N1724/1 | | |

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