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SOLID STATE K_u-BAND POWER AMPLIFIERS

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16. Abstract

A proposed solid-state K_u-band power amplifier utilizing a circularly symmetric array of IMPATT diodes mounted in a single radial line power combiner is discussed and its performance predicted. The proposed amplifier configuration consists of a TM_{030} mode radial line cavity containing 20 IMPATT diodes, with separate input and output ports provided by a ferrite circulator. Some of the pertinent specifications are:

a. Center frequency: 15.0 GHz
b. 1 dB bandwidth: 100 MHz
c. Power output at full gain: 10 watts
d. Gain at maximum output power level: 10 dB
e. DC power input maximum: 250 watts
f. Third order intermodulation product suppression: 30 dB

Conventional IMPATT amplifier techniques preclude the achievement of the above gain, power output, efficiency, and IMP suppression specifications simultaneously; therefore, several novel techniques with the potential of reducing the intermodulation product level are discussed.

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PREFACE

The proposed amplifier configuration consists of a TM_{030} mode radial line cavity containing 20 IMPATT diodes with separate input and output ports provided via a 5-port ferrite circulator having two of its ports internally loaded by matched terminations. The proposed design results in a compact unit in which all of the IMPATT diodes are (1) of the same type, (2) identically mounted, and (3) subjected to the same incident RF power.

Because of its radial symmetry with all diodes equidistant from the central coupling port, this design should be capable of simple modification to substantially increase its bandwidth. It is expected that it will manifest a graceful death feature if a small number of the diodes should fail. This basic amplifier configuration has growth potential to a much high power output capability since with smaller diode packages or bare chip IMPATT diodes, many more diodes and higher efficiency diodes can be incorporated.

In any power amplifier a basic tradeoff exists between power output and efficiency on the one hand and linearity and intermodulation product levels on the other hand. With a standard approach to IMPATT amplifier design and power combining techniques, the power output, efficiency, and intermodulation produce level specifications listed in Section 1 would be incompatible. As a result, considerable attention is given to the problem of intermodulation products in paragraph 3.4 of this report. Techniques for potentially reducing the intermodulation product level by (1) linearizing the power input versus power output characteristics, and (2) controlling the

phase of the second harmonic output which is reflected back to the individual diodes are discussed and will be investigated during Phase II.

With the exception of the intermodulation product level, which will be in doubt until experimental verification is achieved, the proposed design is expected to satisfy all specifications.

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1. PROGRAM OBJECTIVES

The program to develop a Solid State K_u-Band Power Amplifier consists of an analytical design and diode characterization phase (Phase I) and an amplifier development phase (Phase II). This report documents Phase I of this program which resulted in the delivery of a Design Data Package on 26 November 1971. Included in the Design Data Package were complete electrical, thermal, and mechanical characteristics of the amplifier and complete engineering drawings of the first experimental model proposed for development during Phase II.

This amplifier has been designed to satisfy the following specifications:

Center frequency	15.0 GHz
1-dB bandwidth	100 MHz
Ripple within passband	±0.2 dB
Power output at full gain	10 W
Maximum dc power input	250 W
Gain at maximum output power level	10 dB
Maximum noise figure at full gain	15 dB design goal; 30 dB maximum
Maximum volume	0.75 ft^3
Maximum weight	3 lb
Maximum input and output VSWR	1.2
Input and output connectors	UG-419/U
Operating temperature range	-30°C to +50°C

Intermodulation products generated by two CW signals, separated by 10 MHz in frequency at any frequency in the amplifier passband, each signal amplitude at the input being 0.5 W, shall not exceed 10 mW at the amplifier output terminal when the amplifier is operating at full 10 dB gain.

DC power input - To ensure compatibility, the required dc power source will be supplied by the Contractor as an accessory. Input to the dc power source will be 110 to 120 V, 60 Hz.

2. TECHNICAL APPROACH

2.1 DESCRIPTION OF THE AMPLIFIER

The amplifier design chosen consists of a 5-port waveguide circulator, radial line power combiner with a TEM coaxial output line at its center, and an array of 20 diodes bound in individual elemental amplifier circuits called "plugs" arranged in circular form near the outer diameter. The individual plug, in turn, includes the diode, its matching section designed to set the prescribed gain at the 1/2-watt nominal output level, a second harmonic phase reflection filter (HRF), and a stabilization-bias circuit.

The overall amplifier circuit can be characterized simply by reference to figure 1. This figure gives the circuit for one diode only; due to the symmetry of the system, the same circuit will apply to all other diodes individually.

For a given center frequency and load impedance level, one can find a radial coordinate R_{Diode} at which looking inward toward the load, the impedance will be real. By picking an appropriate cavity height D, this real impedance can be adjusted. Then, the radial distance out to the outer wall of the radial line can be made to a quarter wave at the outer frequency. We can then calculate the amplifier gain defined at the radius of the diode circle. The plug will be thought of as an extended diode whose "parasitics" are adjusted to give an impedance which, when referred to a 50-ohm load, will give rise to the desired voltage reflection gain

$$\left|\rho\right| = \left|\frac{Z_{plug} - 50}{Z_{plug} + 50}\right|$$

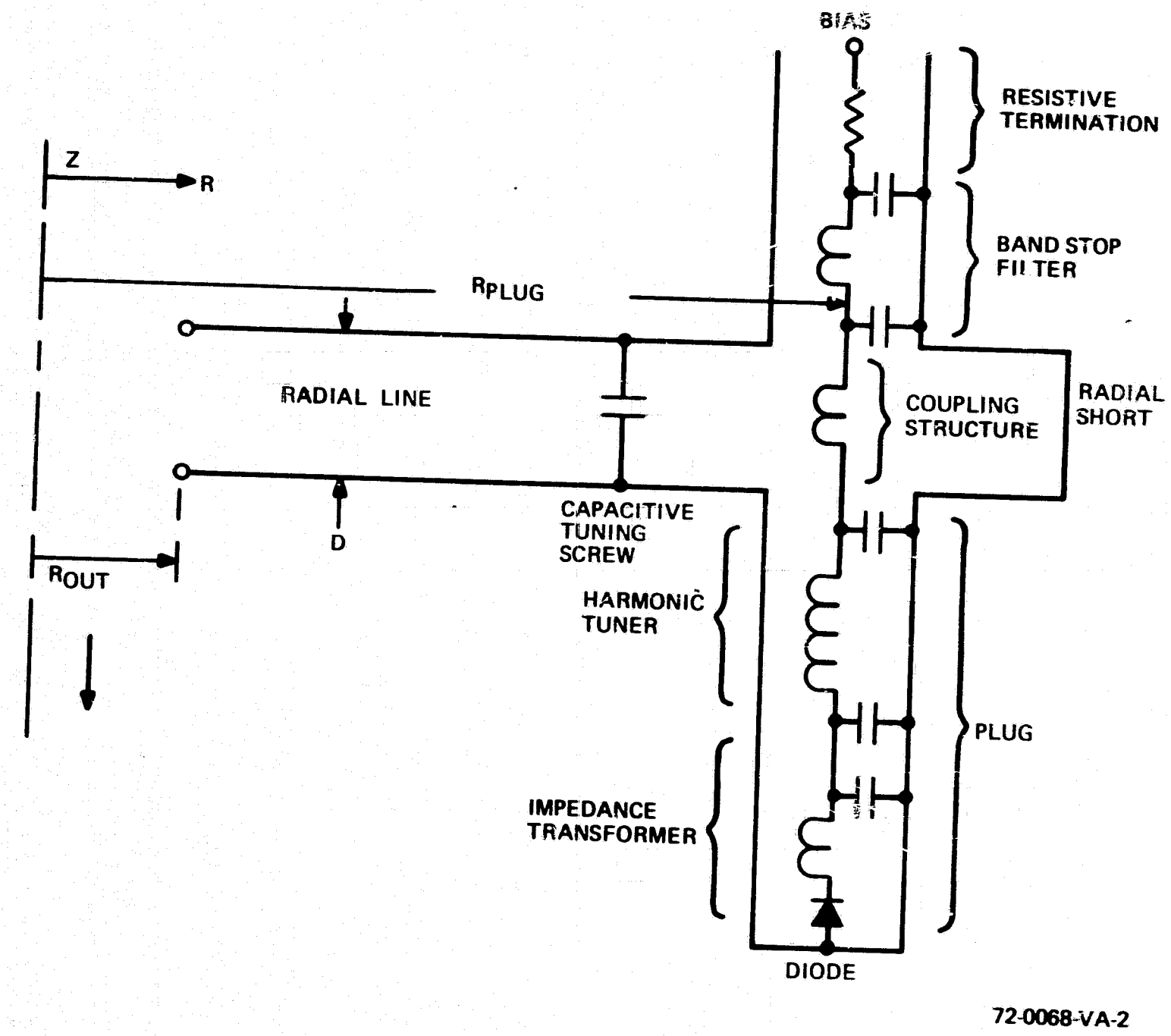


Figure 1. K_u-Band Amplifier Equivalent Circuit

The appropriate equation governing the field variation in the radial line combiner, assuming no azimuthal or axial field variation, are, setting $k = \frac{2\pi}{\lambda}$,

$$E_z = A H_o^{(1)}(kr) + B H_o^{(2)}(kr) \tag{1}$$

$$H_\phi = \frac{1}{j\omega\mu} \frac{\partial E_z}{\partial r} = \frac{j}{\eta} \left[A H_1^{(1)}(kr) + B H_1^{(2)}(kr) \right] \tag{2}$$

where $\eta = 377\Omega$.

These can be further expressed in terms of radial angle functions which for large argument approach the ordinary trigonometric functions; viz,

$$\theta(X) \triangleq \tan \left[\frac{N_o(X)}{J_o(X)} \right] \tag{3}$$

$$\psi(X) \triangleq \tan^{-1} \left[\frac{J_1(X)}{-N_1(X)} \right] \tag{4}$$

The field variation then becomes

$$E_z = G_o(kr) \left[A\ e^{j\theta(kr)} + B\, e^{-j\theta(kr)} \right] \tag{5}$$

$$H_\phi = \frac{G_o(kr)}{Z_o(kr)} \left[A\, e^{j\psi(kr)} - B\, e^{-j\psi(kr)} \right] \tag{6}$$

$$\text{where } G_o(kr) \triangleq \sqrt{J_o^2(kr) + N_o^2(kr)} \tag{7}$$

$$\text{and } Z_o(kr) \triangleq 7 \sqrt{\frac{J_o^2(kr) + N_o^2(kr)}{J_1^2(kr) + N_1^2(kr)}} \tag{8}$$

$Z_o(kr)$ can be thought of as a radially varying characteristic wave impedance of the line. It is independent of the cavity height. These functions are plotted for the range of kr values of interest in figure 2. Another function

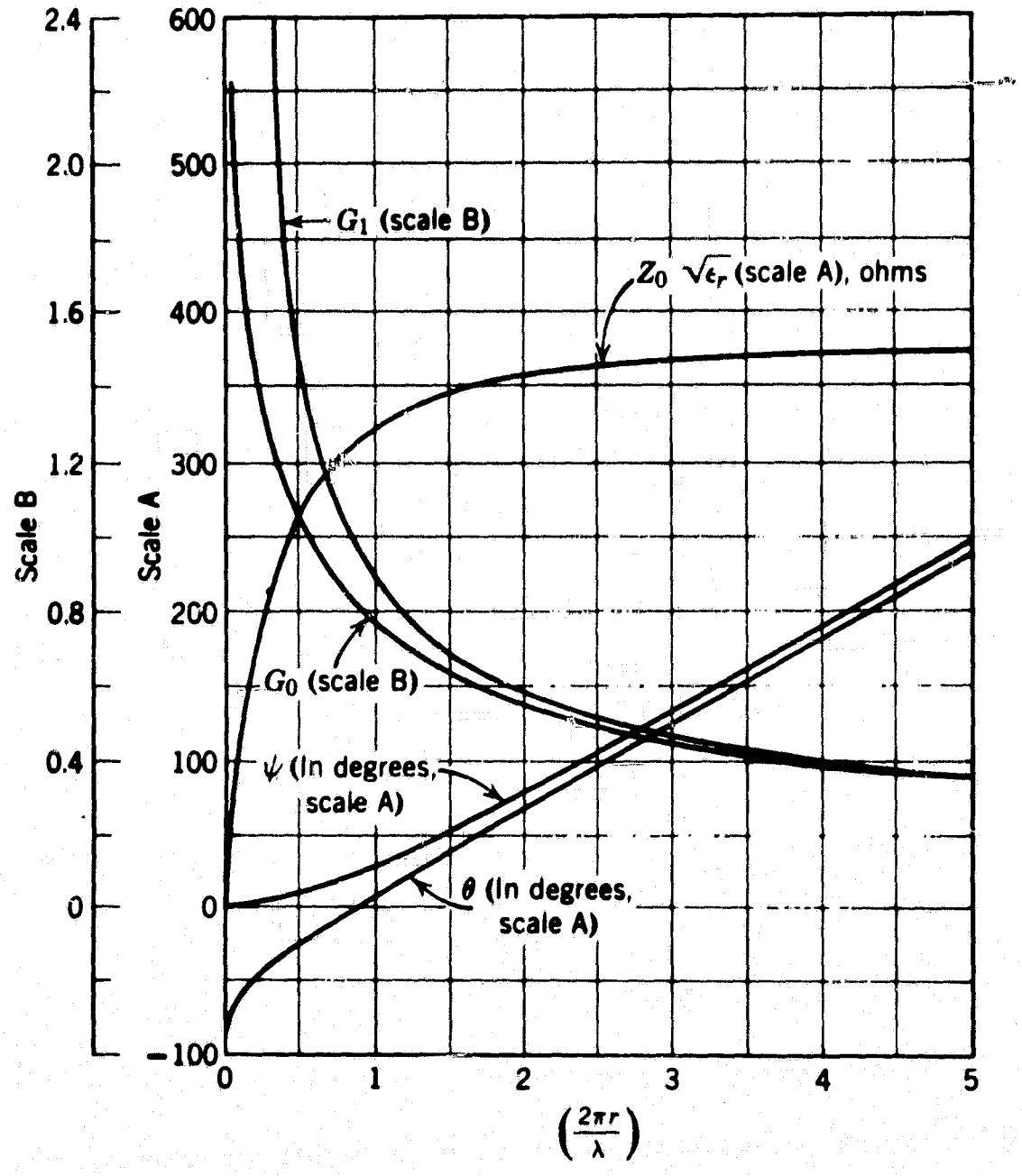


Figure 2. Radial Transmission Line Quantities

of interest can be called the total characteristic impedance and is given by

$$Z_{o_{TOT}}(kr) = Z_o(kr) \left(\frac{D}{2\pi r}\right)$$

This total characteristic impedance (figure 3) is in terms of total potential across the cavity and current rather than a point function wave impedance. $Z_{o_{TOT}}$ has a pole at the origin.

Looking inward toward an assumed 50-ohm load in the coaxial output line, one can compute the real and imaginary part of the impedance, as seen by a given diode plug. This will be given in general by

$$Z = \frac{D}{2\pi r} \left[H(kr)\right] \qquad (10)$$

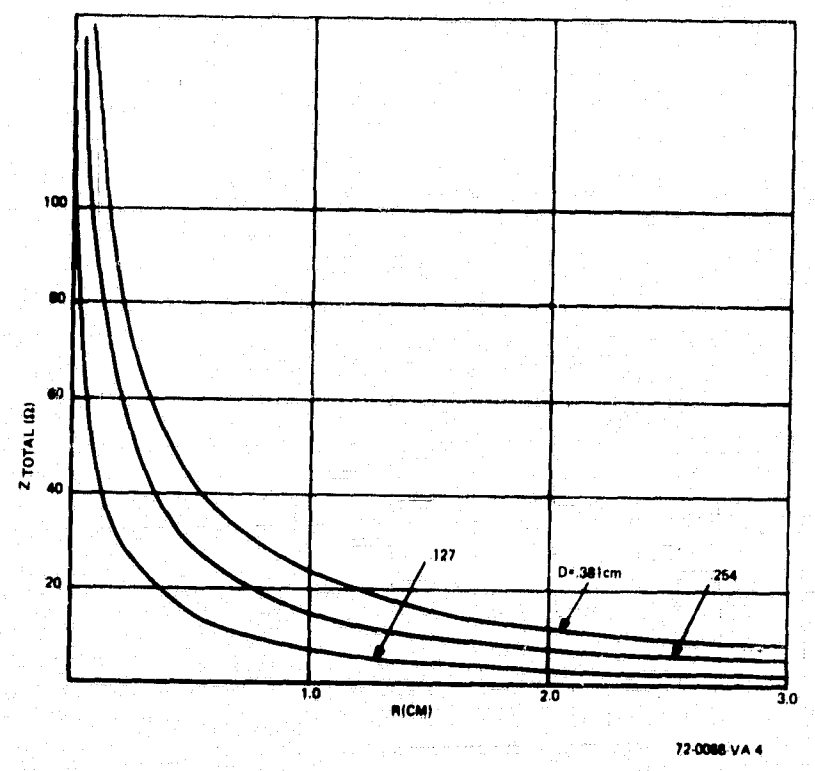


Figure 3. Total Characteristic Impedance vs Radius (F=15.0 GHz)

where

$$H(kr) = \frac{Z_L \cos\left[\theta(r)-\psi(r_{load})\right] + jZ_o \sin\left[\theta(r)-\theta(r_{load})\right]}{Z_{OL} \cos\left[\psi(r)-\theta(r_{load})\right] + jZ_L \sin\left[\psi(r)-\psi(r_{load})\right]} \qquad (11)$$

where $Z_{OL} = Z_O\,(kr_{load})$, r_{load} is the equivalent radial coordinate of the 50-ohm load, and $Z_L = 50 \times \frac{2\pi r_{load}}{D}$, the wave impedance equivalent of the 50-ohm load at $r = r_{load}$.

For a cavity height D of 0.254 cm, load impedance of 50 ohms, r_{diode} = 2.25 cm and center frequency of 15 GHz, the impedance looking toward the load is plotted versus r_{load} in figure 4 with frequency as a parameter. It can be seen that we have a region of relatively constant real impedance of about 50 ohms with a zero of reactance. It is important to recognize that this is the impedance looking toward the load per diode and is given by multiplying (1) by $N_d = 20$, the number of diodes. This arises from the fact that the 20 diodes are arranged in parallel, such that the overall impedance seen by them all is 1/20 of that seen by any given one.

Thus, we can set a point in the radial line at which the individual plugs see a real impedance in the neighborhood of 50 ohms. The radial line length from the diode ring out to the short should in this case be a quarter wave long. The plug gain should then be referred to a real impedance of 50 ohms.

At the radii of output, diode and short, kr is large enough such that $Z_o(kr)$, $\theta(kr)$, and $\phi(kr)$ approach their corresponding values in free space or in a parallel plane guide.

As a matter of interest, the impedance looking toward the load has been evaluated also assuming a 50-ohm load with a VSWR mismatch of 1.2:1, indicating a real impedance range of about 45 to 70 ohms at the desired diode radius. This is shown in figure 5. Figures 6, 7, and 8 show this same impedance for the 50-ohm load in Smith chart form for r_{load} = 0.65, 0.70, and 0.75 cm.

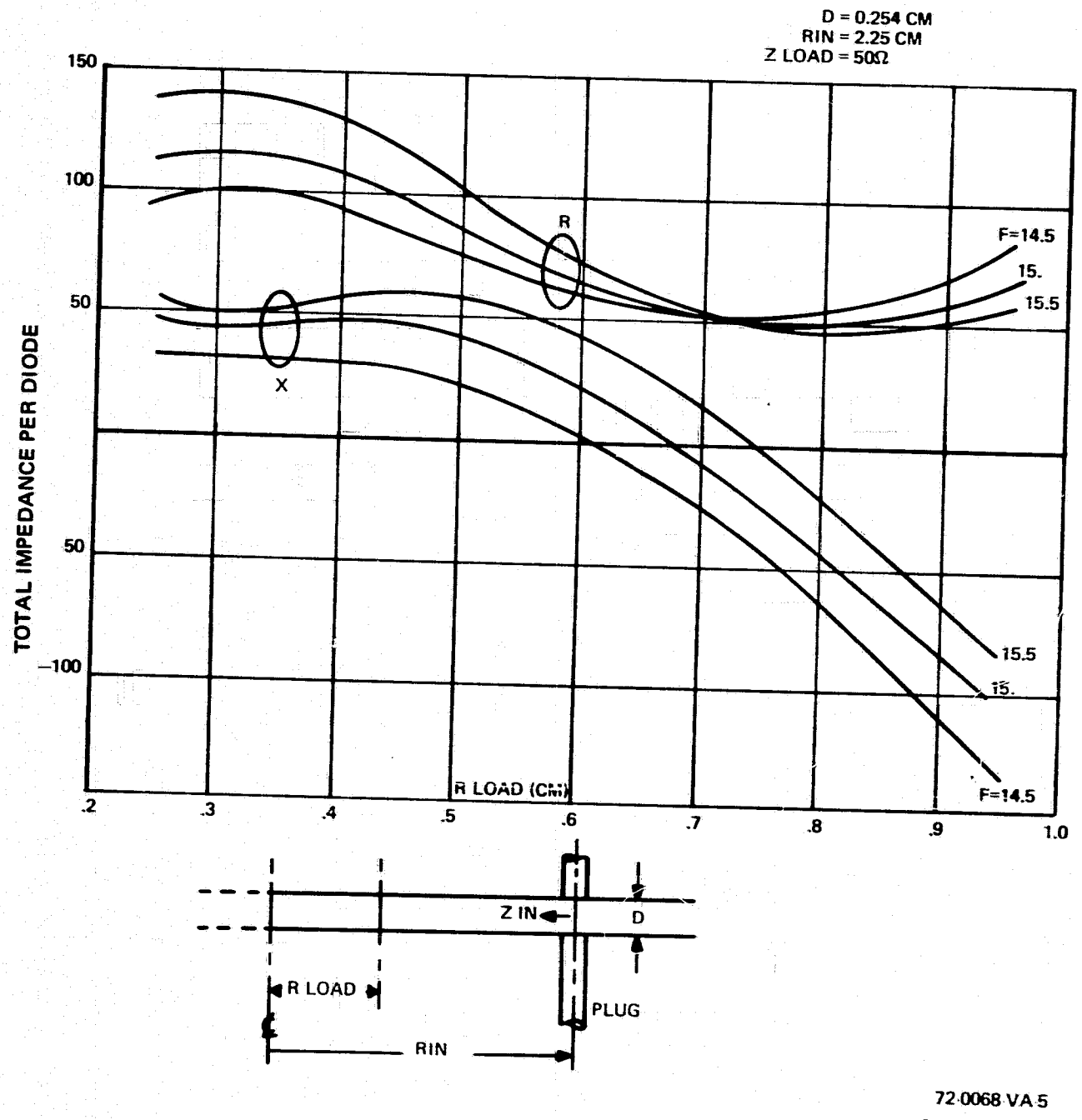


Figure 4. Impedance of Radial Power Combiner at Plug Radius

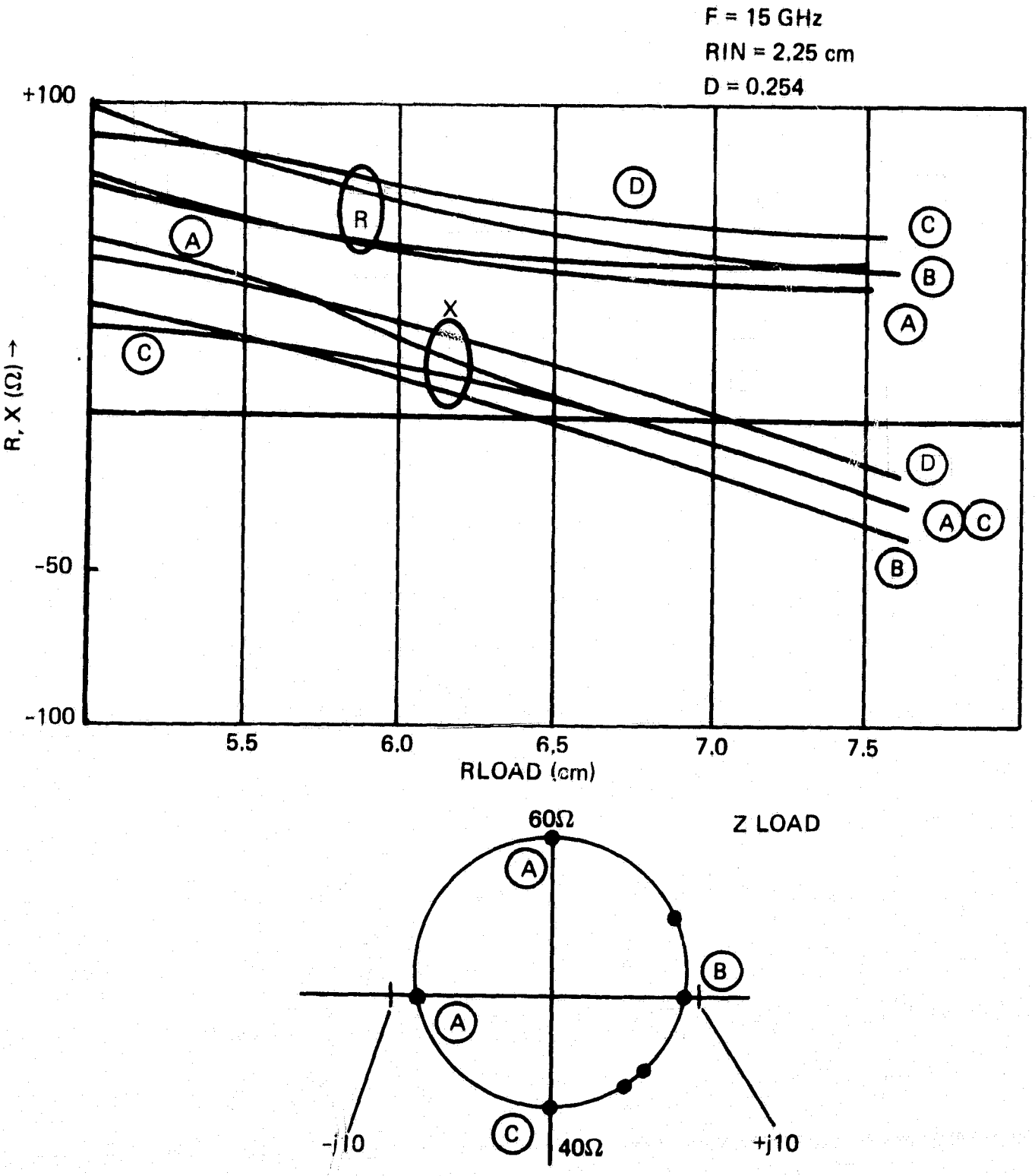


Figure 5. Impedance of Radial Power Combiner at Plug Radius for a Mismatched Load

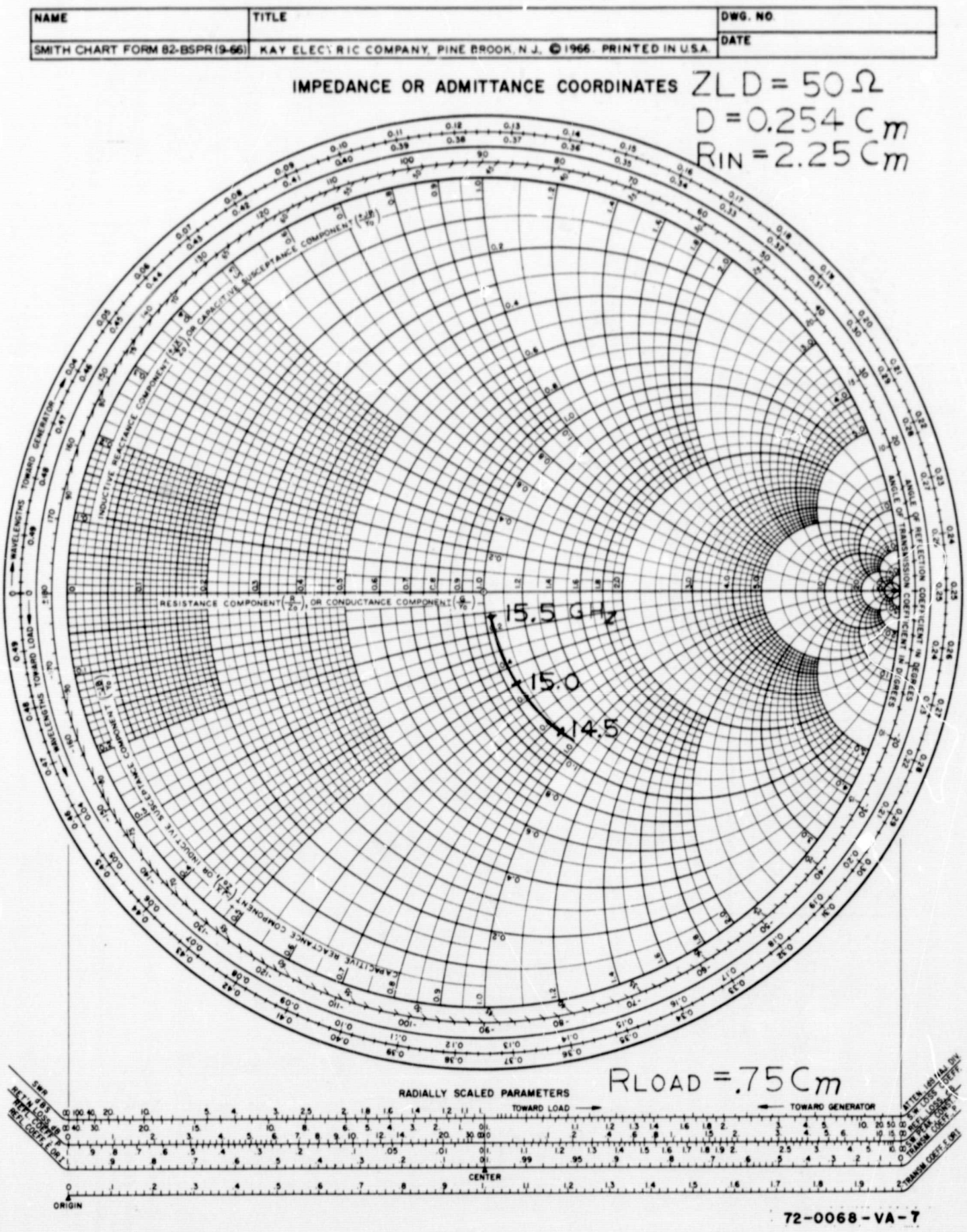


Figure 6. Smith Chart Plot of Radial Line Impedance for R_{LOAD} = 0.75 cm

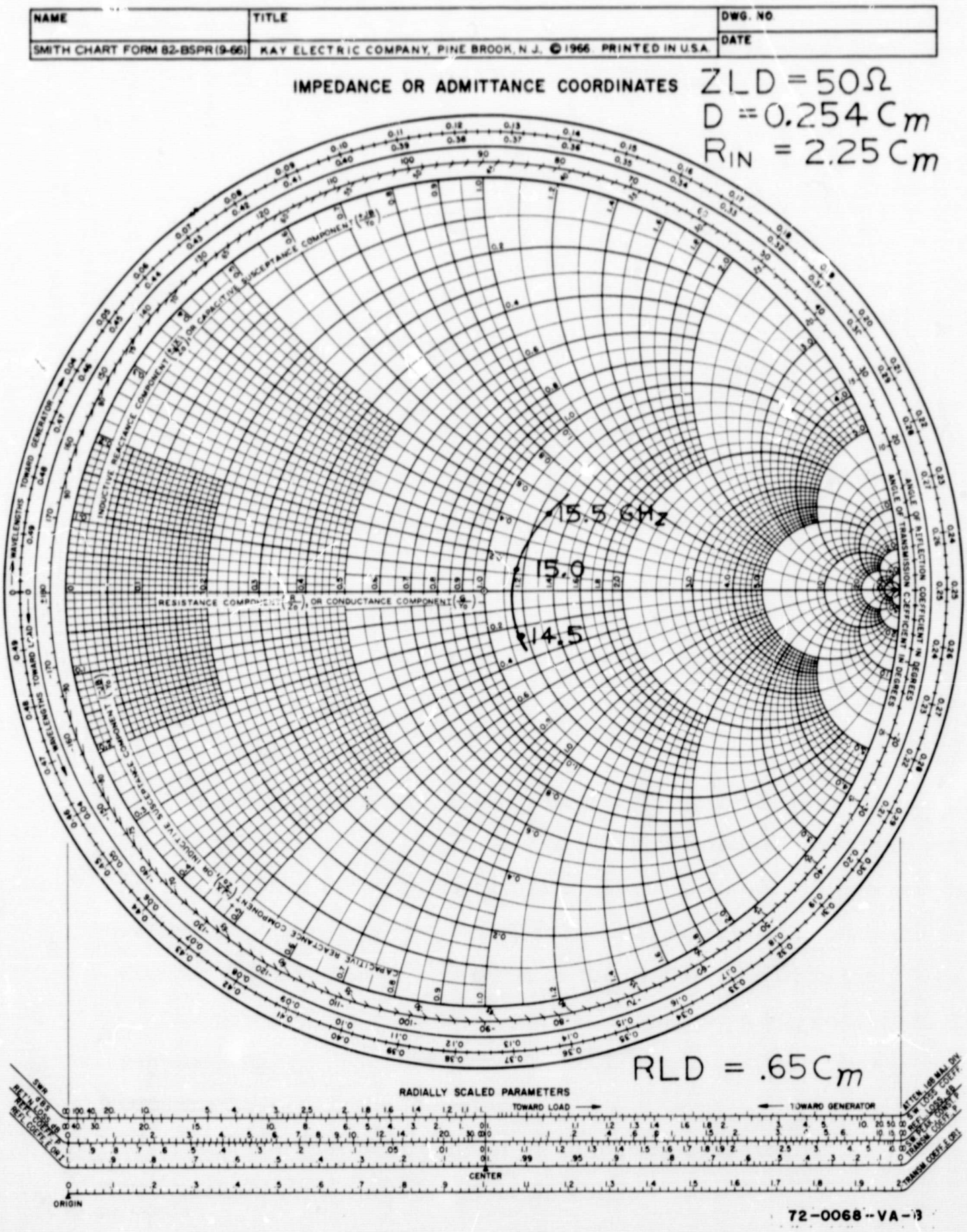


Figure 7. Smith Chart Plot of Radial Line Impedance for $R_{LOAD} = 0.65$ cm

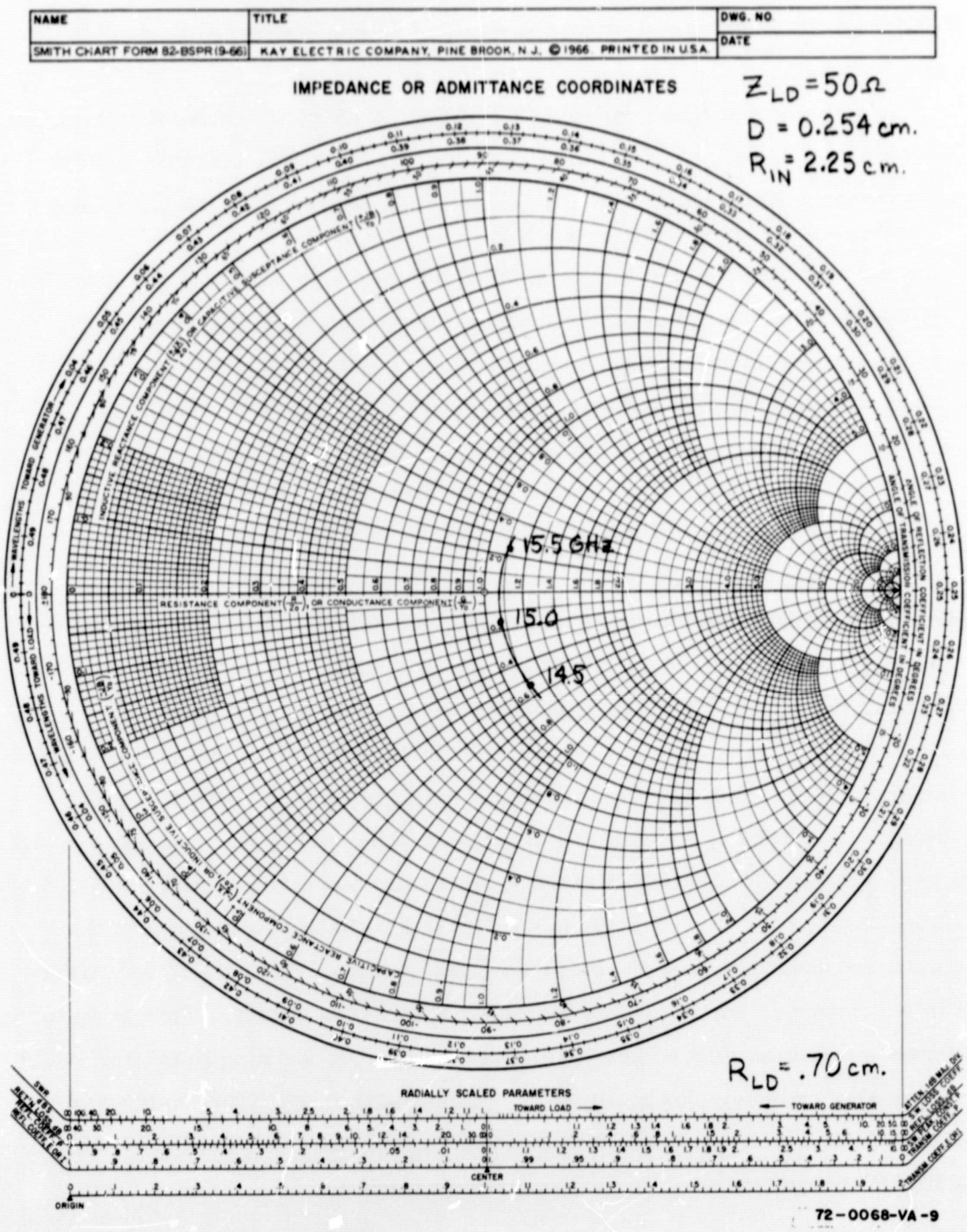


Figure 8. Smith Chart Plot of Radial Line Impedance for R_{LOAD} = 0.70 cm

The large signal plug gain was chosen as 13 dB at center frequency with the stipulation that:

- The large signal gain would be within ±0.2 dB over the band of interest
- It would fall off out of band sufficiently fast to avoid stability problems
- That the gain variation requirement could be met with the harmonic reflection filter incorporated in the plug.

Plug designs were achieved using the diode package parameters associated with the Raytheon type 16 and an Alpha Industries type 191 as models. The former has a large series inductive component due to the large lead inductance. The latter's lead inductance is much less and, therefore, calls for a different internal design of the plug.

Plug gain in the 12 to 13 dB range evaluated in terms of the measured large signal values of a sample GaAs diode were obtained. Typical curves are shown in figure 9. Here gain curves are shown with and without the presence of the harmonic reflection filter.

The input impedance of such a plug was computed versus frequency and is shown in figure 10. This indicates that in conjunction with figure 4, we can choose a radius of a ring of plugs at which the plug and load impedances can be specified, and therefore, at which the plug gain can be set. The combination of these two impedance functions then will determine the overall gain performance of the amplifier with the radial power combiner included. The bandwidth of the entire device is then seen to be limited, by both the plug gain and the impedance variation shown in figure 4. This latter variation is a function of the radial electrical length to the output. This is in turn dependent on the number of and size of the plugs. If the plug diameter could be materially reduced, for example, we could pick a point one-half wavelength radially closer to the output at which again one could find a 50-ohm real impedance point, with less frequency variation.

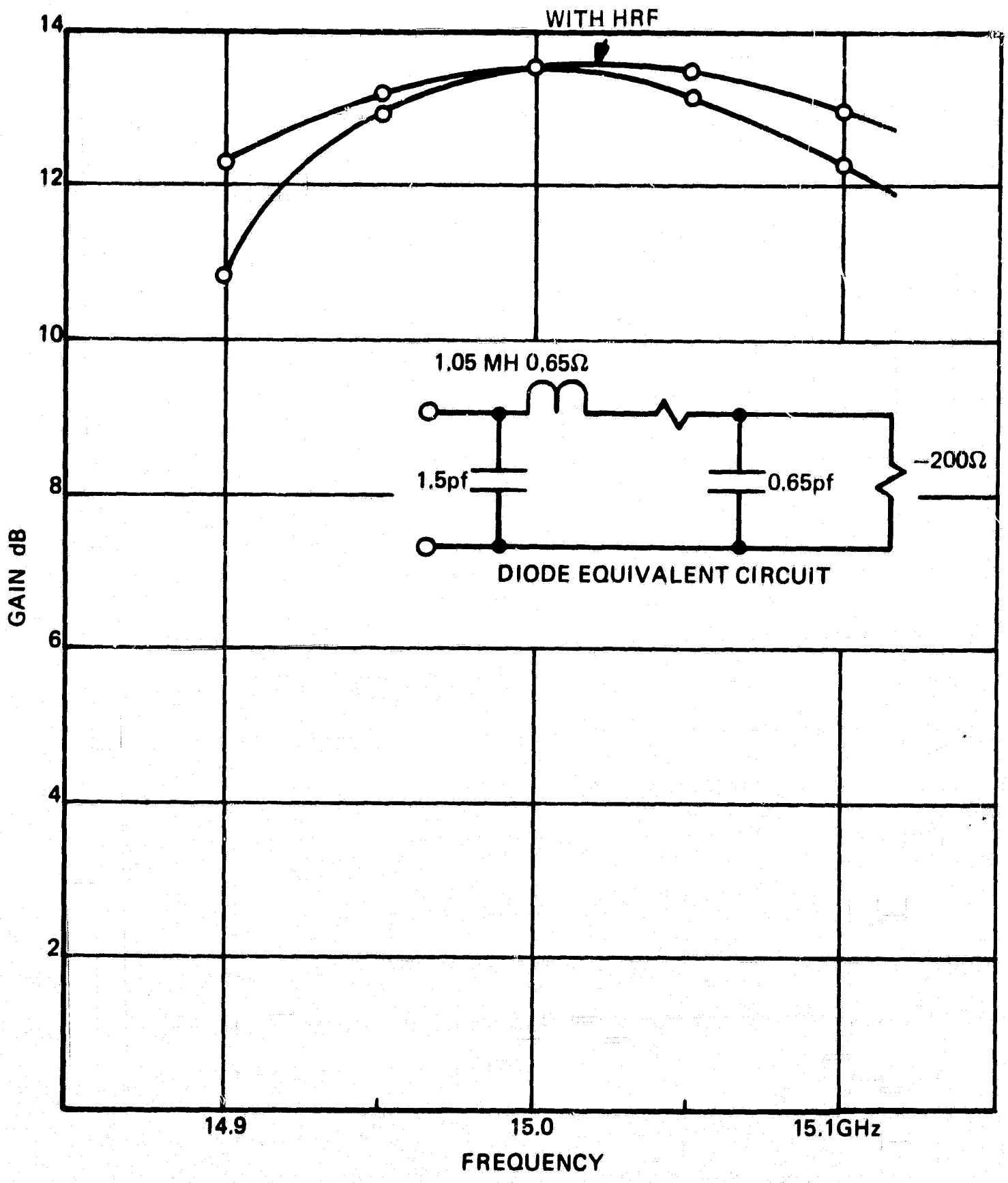


Figure 9. Plug Gain With Diode in Alpha Type 191 Package

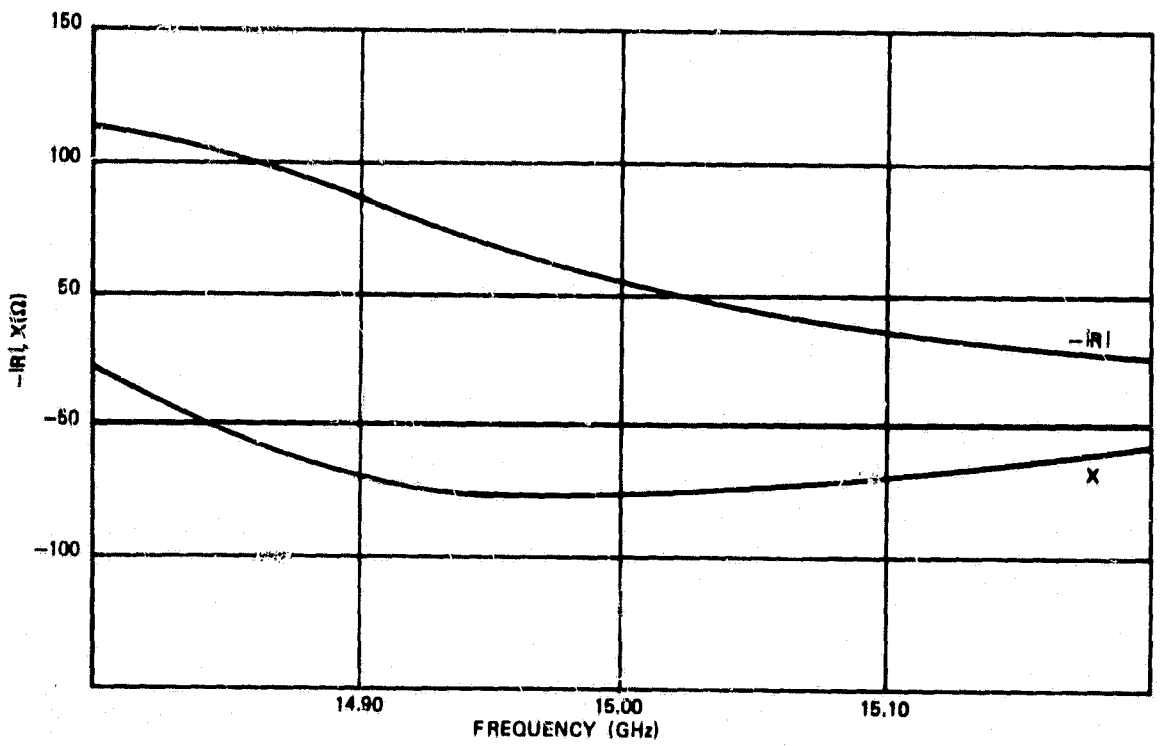


Figure 10. Impedance of Plug (a Package)

Plug gain is largely a function of the diode impedance. If the diode package can be operated at resonance, then the plug gain will be simply

$$G_{PLUG} = 20 \log_{10} \left| \frac{R_d - 50}{R_d + 50} \right| \qquad (12)$$

since X_d passes through zero at resonance.

A sketch of the plug with its diode mount, impedance transformer, harmonic reflection filter, stabilization load resistor, and bias lead is shown in figure 11.

2.2 DESIGN OF AMPLIFIER "PLUG"

The "plug" is the fundamental component of the radial line amplifier. In fact, the entire composite amplifier may be considered primarily as a multiplicity of elementary reflection amplifiers whose input and output signals are distributed and combined by a single radial line manifold structure.

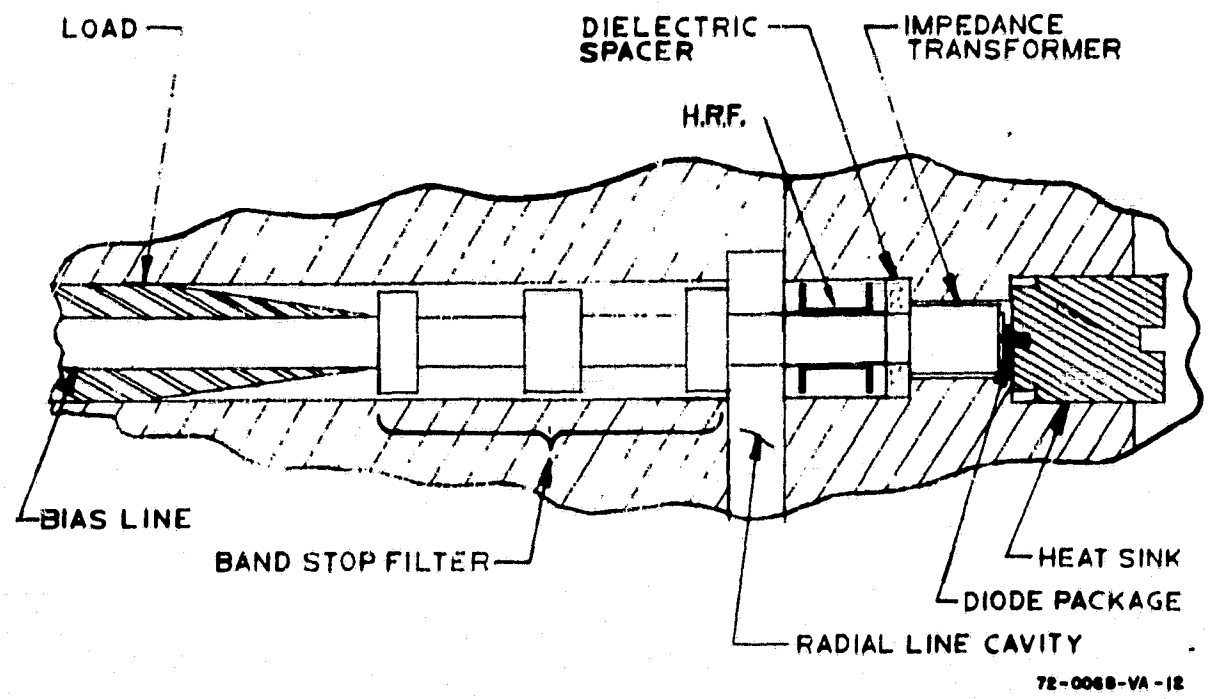


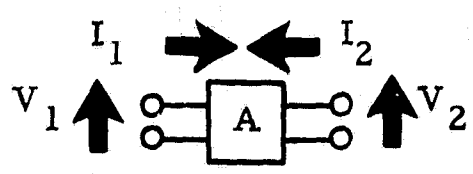
Figure 11. Schematic of Amplifier Plug

The radial line itself is discussed elsewhere in this report so the discussion here will be limited to the design of the individual plugs.

Several criteria were employed in the design of the plug.

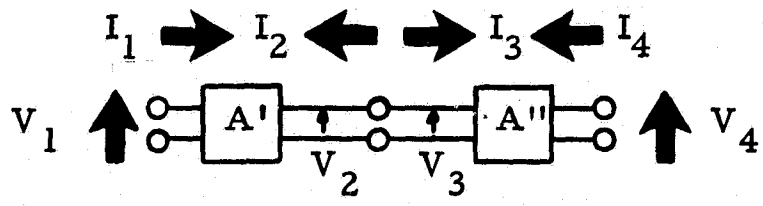
- Unity coupling to the radial line power combiner is assumed. Calculations have shown that such a characteristic is realizable by a judicious choice of radial line height, plug radius, and wall reactance.
- An individual plug gain of 13 dB was chosen to allow for power combining losses, circulator losses, and mismatches.
- A basic 50-ohm coaxial line structure was chosen to simplify individual plug testing and fabrication.
- Each plug was to be individually stabilized to prevent spurious out-of-band oscillation (due to the inherently broadband negative resistance of the IMPATT diode).

The analysis of the plug was done using a ladder analysis computer program. The circuit is broken up into a set of 2-ports in a ladder arrangement with branching and parallel paths allowed. Each 2-port is modeled by an "A" matrix.



$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A \end{vmatrix} \begin{vmatrix} V_2 \\ -I_2 \end{vmatrix}$$

For a pair of cascaded 2-ports



$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A' \end{vmatrix} \begin{vmatrix} V_2 \\ -I_2 \end{vmatrix}, \qquad \begin{vmatrix} V_3 \\ I_3 \end{vmatrix} = \begin{vmatrix} A'' \end{vmatrix} \begin{vmatrix} V_4 \\ -I_4 \end{vmatrix}$$

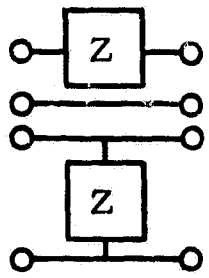
$$V_2 = V_3 \qquad I_2 = I_3$$

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A' \end{vmatrix} \begin{vmatrix} A'' \end{vmatrix} \begin{vmatrix} V_4 \\ -I_4 \end{vmatrix}$$

So the equivalent A matrix for a cascaded set of n A-matrices is

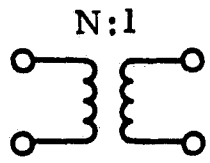
$$\begin{vmatrix} A \end{vmatrix}_{TOTAL} = \begin{vmatrix} A_1 \end{vmatrix} \begin{vmatrix} A_2 \end{vmatrix} \cdots \begin{vmatrix} A_n \end{vmatrix}$$

The A matrices for some simple elements are shown.

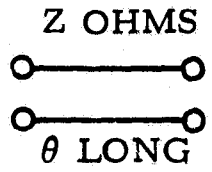


$$\begin{vmatrix} 1 & Z \\ 0 & 1 \end{vmatrix}$$

$$\begin{vmatrix} 1 & 0 \\ \frac{1}{Z} & 1 \end{vmatrix}$$



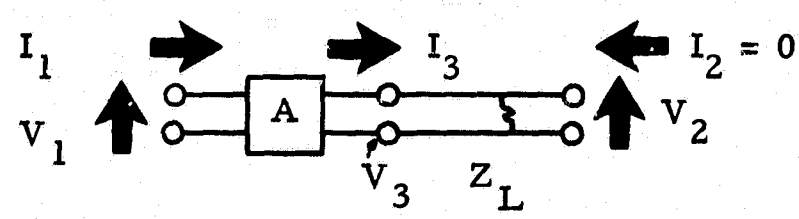
$$\begin{vmatrix} N & 0 \\ 1 & \frac{1}{N} \end{vmatrix}$$



$$\begin{vmatrix} \cos\theta & jZ_o \sin\theta \\ \frac{j}{Z_o}\sin\theta & \cos\theta \end{vmatrix}$$

Lossless Transmission Line

The input impedance of Z_{in} of a network terminated in Z_L can be computed from its A matrix as follows.



$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A \end{Vmatrix} \begin{matrix} 1 & 0 \\ \frac{1}{Z_L} & 1 \end{matrix} \Vert \begin{matrix} V_2 \\ 0 \end{matrix} \end{vmatrix}$$

$$\begin{vmatrix} V_1 \\ I_1 \end{vmatrix} = \begin{vmatrix} A_{11} + A_{12}/Z_L & A_{12} \\ A_{21} + A_{22}/Z_L & A_{22} \end{Vmatrix} \begin{matrix} V_2 \\ 0 \end{matrix} \end{vmatrix}$$

$$Z_{in} = \frac{V_1}{I_1} = \frac{A_{11} + A_{12}/Z_L}{A_{21} + A_{22}/Z_L}$$

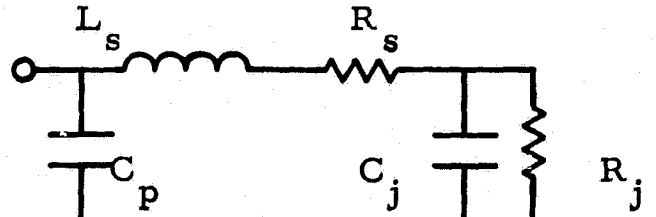
The reflection coefficient referred to a real source impedance Z_o is

$$\Gamma = \frac{Z_{in} - Z_o}{Z_{in} + Z_o}$$

and the reflection gain G is given by

$$G = 20 \log_{10} (|\Gamma|)$$

The plug was designed to provide a gain of 13 dB over a small frequency range from a 50-ohm source. The diode parameters used were those of a chip operating under high-power conditions as in Alpha type No. 191 package. This diode package model is given in figure 12.



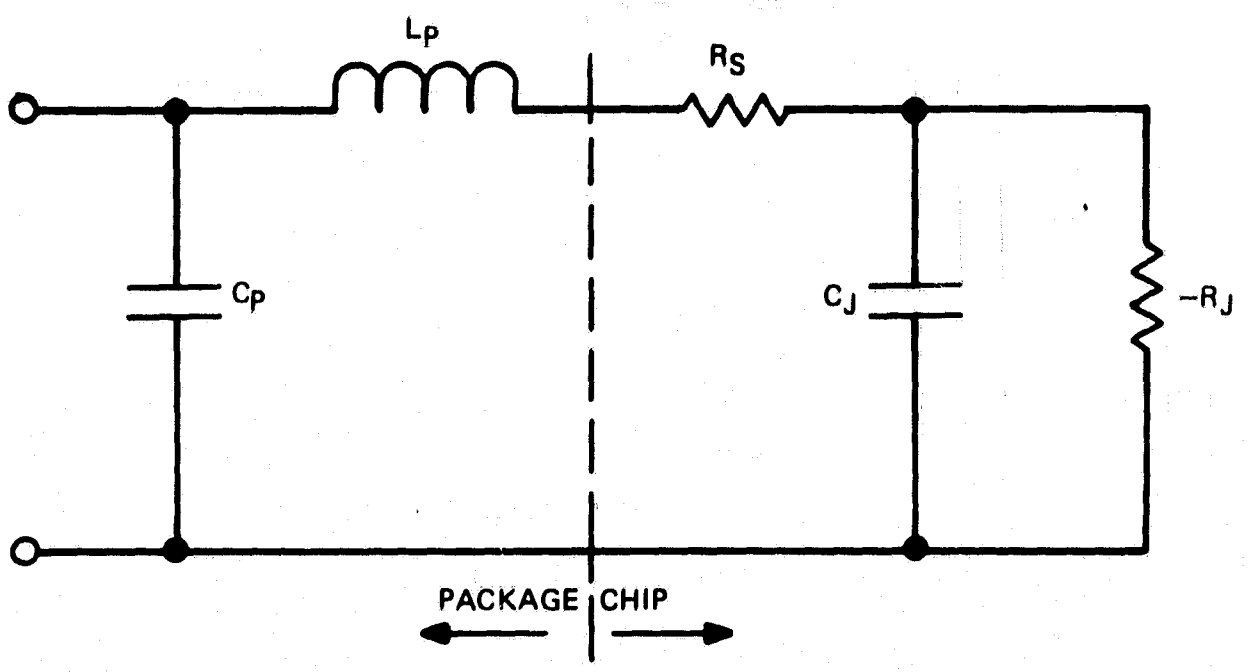
Given a particular set of diode and plug parameters $|X|$, a gain versus frequency curve can be calculated. If we define

$$\text{error}\Big|_{|X|} = \sum_{\text{freq}} W_f * (\text{Gain}_{\text{Desired}} - \text{Gain}_{\text{Calculated}})^2$$

where W_f is a weighting function we have a measure of the performance of the plug over a set of frequencies. Each element that is considered variable - these can be line impedances and lengths - is changed by a small amount and a new error is calculated. An incremental error

$$\frac{d\ \text{Error}}{d\ V_j}\Bigg|_{j = 1,\ \#\ \text{of variables}}$$

can then be computed. A minimization routine then varies the elements to reduce the error term.



CHIP PARAMETERS:

$R_J \sim 200\Omega$ $\quad$ $R_S \sim .5\Omega$

$C_J \sim .8PF$

PACKAGE PARAMETERS:

	L_P	C_P
RAYTHEON TYPE 16	.4 NH	.3 PF
ALPHA TYPE 191	.15 NH	.105 PF

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Figure 12. Packaged IMPATT Diode Equivalent Circuit

The Fletcher-Powell[2] minimization routine is essentially a steepest descent type program in which the direction or line of travel (in a space whose base vectors are the variables in the Error function) is modified by a "best guess" of the Hessian matrix. The new information obtained at the minimum along the line is then used to update the Hessian and the process continues until convergence is obtained.

This type routine works well if the initial plug design is reasonably close to one corresponding to a solution. A flow diagram of the complete program is shown in figure 13.

The harmonic tuning filter and band-stop filter were also designed using a computerized procedure. The harmonic tuning filter was based on a quasi-lumped element design in order to conserve line length. Its characteristic is given in figure 22.

The band-stop filter is a two-section π network which presents a very low impedance to the fundamental and is effectively transparent to harmonics and subharmonics. Its characteristic is given in figure 14.

2.3 STABILIZATION CONSIDERATIONS

To ensure unconditional stability, we must provide that the real part of the cavity impedance presented to the plug reference radius exceeds in magnitude the negative resistance of the plug. In most cases it is sufficient to impose the side condition that the corresponding reactive components of these impedances be nonconjugate anywhere in the band where $|-R| > R_{LOAD}$. In fulfilling these requirements note must be taken of the other possible resonant modes in the radial line cavity.

In the amplifier design we have provided means for fulfilling these conditions. The first is a frequency-dependent stabilizing load resistor housed in the bias circuit. The second is an array of radial mode absorbing strips and slots in the top plate of the radial line cavity.

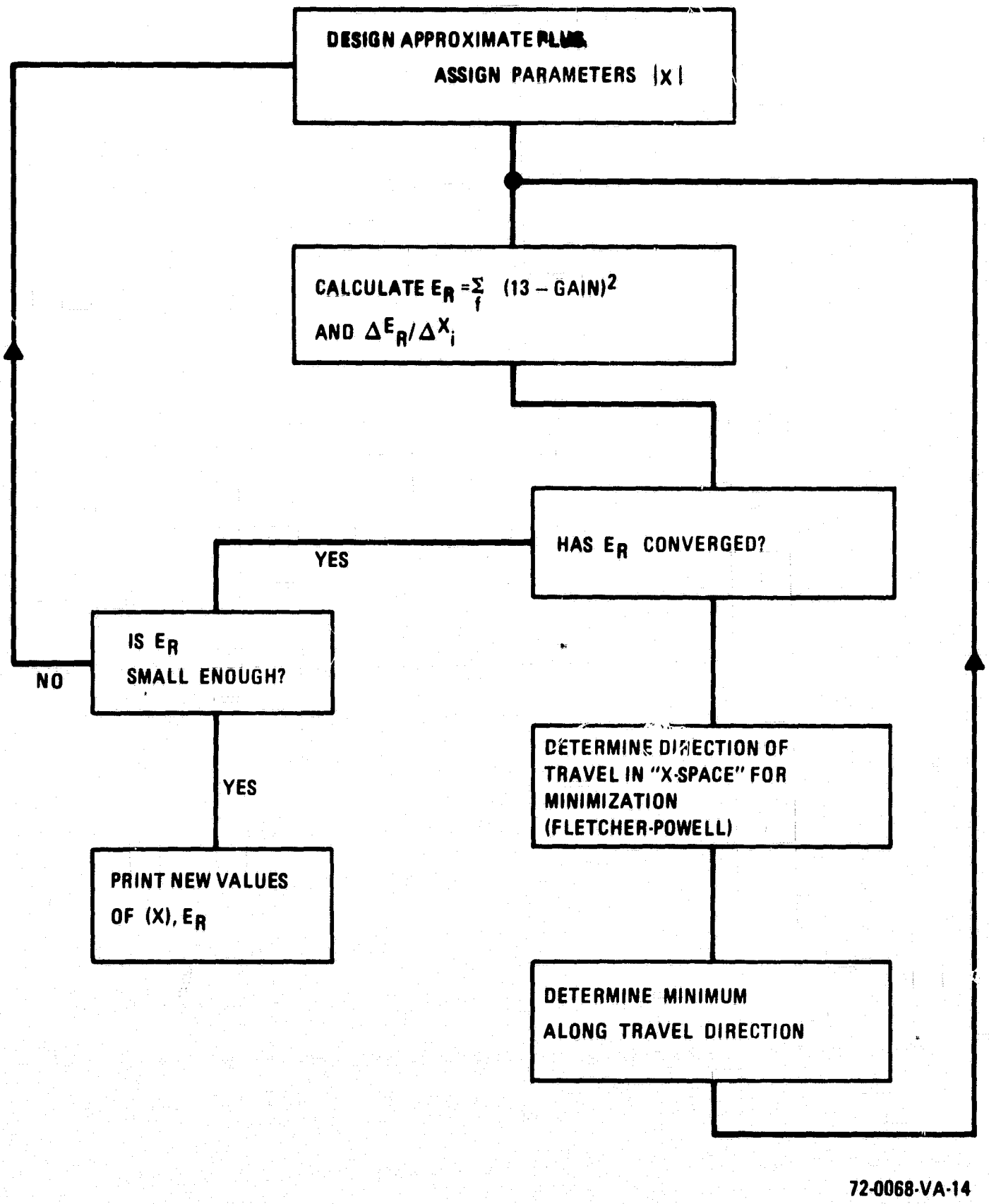

Figure 13. Optimization Routine Flow Diagram

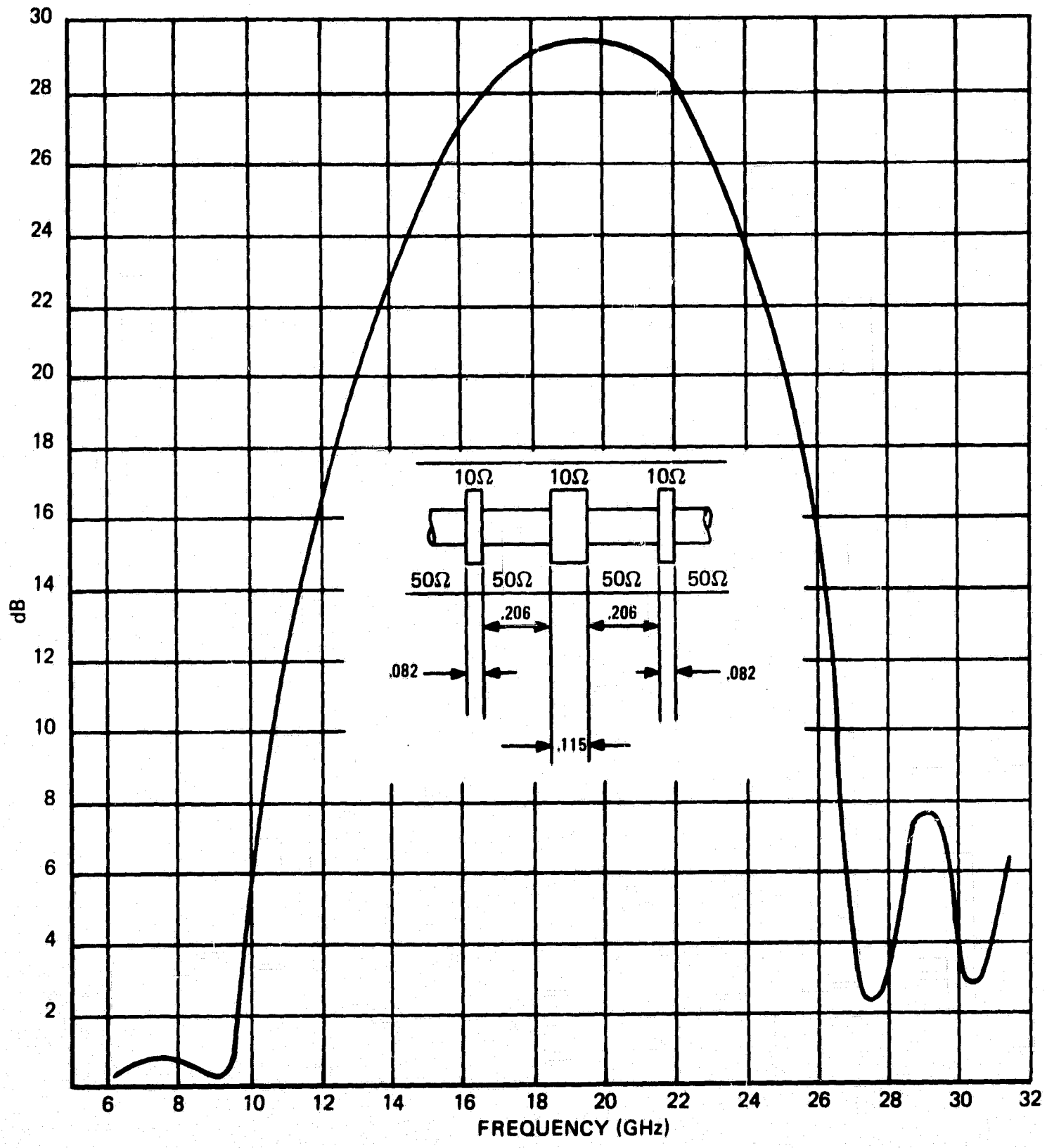

Figure 14. Band Stop Filter

The stabilizing load resistor is comprised of the series combination of a band-stop filter centered in the band of interest and a non-dc conducting microwave load material - an iron-loaded dielectric such as MMF - 14. A typical band-stop filter characteristic is plotted in figure 14 for the three-element configuration shown in figure 11. This provides rejection of close to 30 dB in the band of interest and very high return loss on the low-frequency side. Examination of figures 4 and 10 indicates that the resistive components of plug and load impedance are nearly equal on the low side, the reactive components are of the same sign and, therefore, nonconjugate. Gain of the entire amplifier has been computed over the frequency range from 8 to 16 GHz with no indication of gain peaks other than the desired one. The stabilization resistor will tend to add up to 50 ohms in series to the impedance as seen by the plug in the passband of the filter, thus providing stabilization on the low-frequency side. On the high side, the plug negative resistance falls off steadily as seen in figure 10.

The higher modes of interest are shown in table 1. The $TE_{\ell mn}$ modes will all fall in a frequency range far above the range of interest because they have a half wave of axial field variation. The cavity height D = 0.254 cm requires that these modes be at a frequency greater than 59 GHz. A similar argument eliminates the $TM_{\ell mn}$ modes for which $n > 0$. The $TM_{\ell m}$ modes for which $\ell > 0$ will be damped by radial conductive strips because these modes have azimuthally directed current components. The TM_{01} mode resonance is below the -R band of the diode, while the TM_{02} can be damped by the stabilization resistor filter described above. The TM_{030} case is not so clearly defined. The calculation obviously does not take into account the presence of the plugs and load, and the TM_{03} is the radial line mode used to couple the plugs to the output.

TABLE 1

$TM_{\ell mo}$ CAVITY MODES

ℓ	m	$X_{\ell m}$	F(GHz)
0	1	2.405	4.55 **
1	1	3.832	7.24 *
2	1	5.136	9.20 *
0	2	5.520	10.44 **
3	1	6.380	12.07 *
1	2	7.016	13.25 *
4	1	7.588	14.32 *
2	2	8.417	15.90 *
0	3	8.654	16.35

* Damped by radial strips

** Below stop band of bias line filter

All TE and all $TM_{\ell mn}$ (n > 0) will be above band of $-|R_{diode}|$. Outer radius assumed to be 1.00 inch.

The radial conductive mode absorbers are designed after some experiments which were run in double ridged guide in the same frequency range for another project. In these experiments it was desired to damp out the TE_{20} waveguide mode while propagating with minimum insertion loss the TE_{10} mode. The TE_{20} cuts off in the guide used at about 12.5 GHz. The absorbers consisted of longitudinal slots in the center of the broad wall filled with an iron-filled dielectric material Eccosorb MF - 124.* Results are shown in figure 15. Insertion loss of the TE_{20} was typically 4.6 dB far from TE_{20} cutoff whereas the loss of the TE_{10} was about 0.3 dB. The TE_{10} loss was not measured above 12.5 GHz due to mode conversion

* Emerson and Cumming, Inc., Canton, Mass.

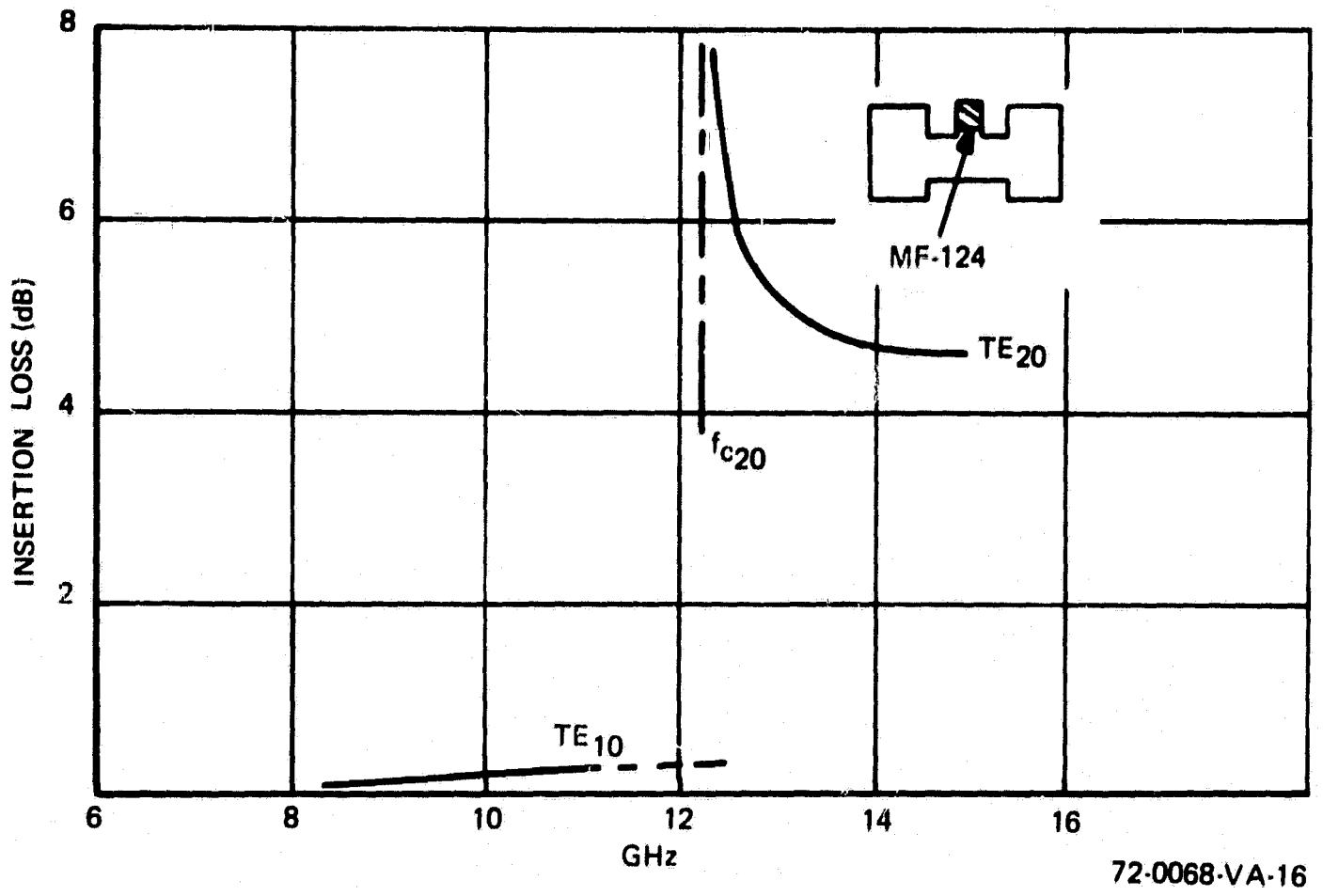

Figure 15. $TM_{\ell mc}$ Mode Suppression

elsewhere in the circuit. Independent measurements indicated that the TE_{10} mode could propagate mode-free in such a guide when proper care was taken in launching. The electric field patterns associated with the TM_{ono} modes are shown in figure 16.

2.4 INTERMODULATION PRODUCTS

Typically in amplifier design, setting a specification on efficiency and linearity requires a compromise due to the fact that high efficiency in electron devices always implies operation in a saturated or nonlinear state. A comparison to traveling wave tubes is instructive. In high-efficiency TWT's, fairly linear operation is achieved about 3 to 6 dB below the saturated output drive depending on the tube type. Linearity can be meaningfully tested by using the two-tone intermodulation product test wherein two sine wave signals separated by a small frequency difference are injected into the device under test, and the relative power levels of the signal outputs and those of the

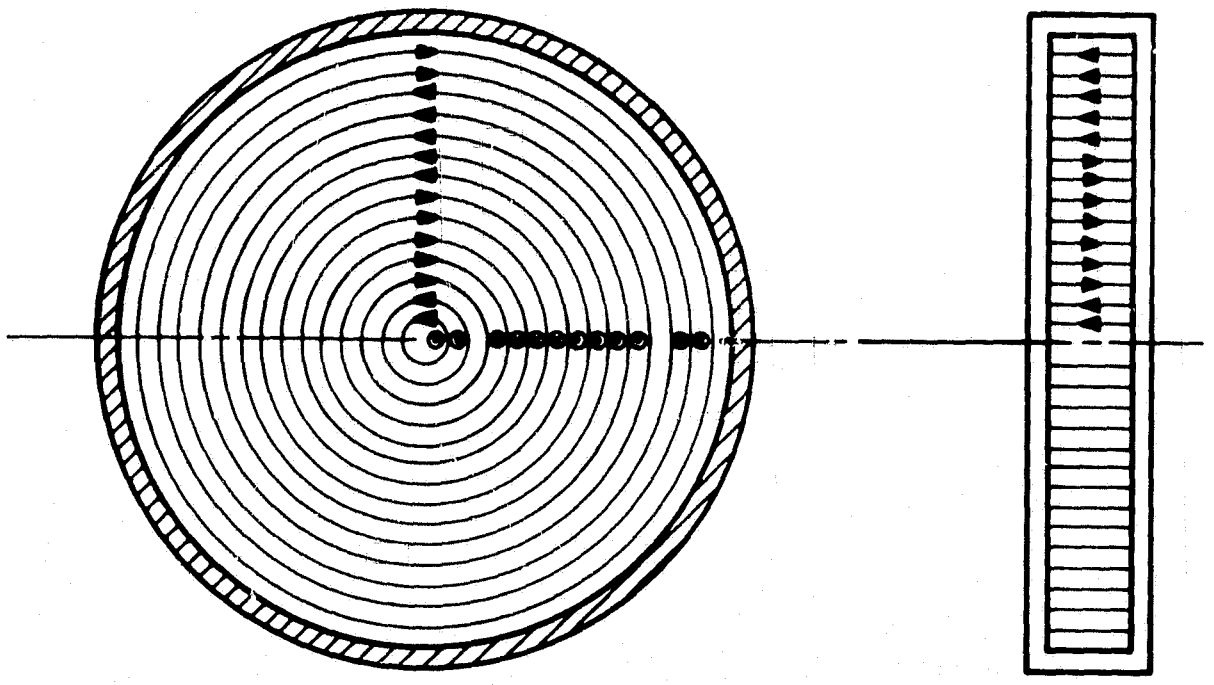

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Figure 16. TM_{ono} Mode Field Patterns

third and fifth order intermodulation products (IMPS) are noted. Classical theory indicated that the nth order IMP's have a log P_{out}/P_{in} slope of n times that of the injected signals. Thus in practical cases of interest, one backs off on the maximum efficiency output a few dB obtaining satisfactorily low IMP's.

Figure 17 shows[3] the expected P_{out}/P_{in} slopes in dB/dB for the fundamental, second harmonic, and third order IMP for the case of the two equal input signals.

The situation for TWT's has been thoroughly covered by M.K. Scherba and J.E. Rowe[3] and in a simple power series model by Foster and Kunz[3] where the power series in question is the output/input voltage transfer function of the amplifier; viz,

$$V_{out} = \sum_{n=1}^{n} A_n V_{in}^{n} \qquad (13)$$

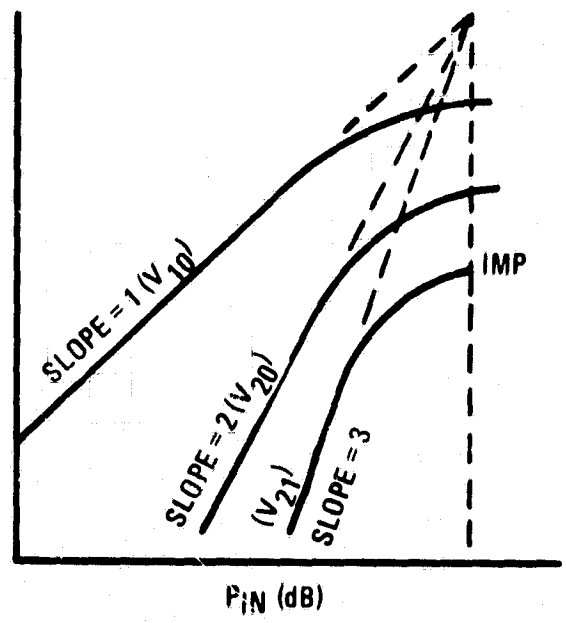

Figure 17. Relative Magnitudes of Various Order IMP's

In most TWT problems taking the series out to n = 3 gives reasonable results and out to 5 very good experimental fits.

Having a V_{out}/V_{in} curve and the equivalent power series coefficients enables one to compute the expected IMP levels as a function of drive signal levels. Expressions for the 3rd and 5th order IMP's, as well as the fundamental tone and the 2nd harmonics are given below, where the V_{in}/V_{out} curve is assumed to be truncated at n = 5.

$$V_{in} = V_1 \cos \omega_1 t + V_2 \cos \omega_2 t \tag{14}$$

Fundamental

$$V_{10} = A_1 V_1 + A_3\left(\frac{3}{4} V_1^{\,3} + \frac{3}{2} V_1 V_2^{\,2}\right) + A_5\left(\frac{5}{8} V_1^{\,5} + \frac{15}{8} V_1 V_2^{\,4} + \frac{15}{4} V_1^{\,3} V_2^{\,2}\right)$$

$$\text{2nd Harmonic } V_{20} = \frac{A_2}{2} V_1^2 + A_4 \left(\frac{3}{2} V_1^2 V_2^2 + \frac{1}{2} V_1^4 \right)$$

$$\text{3rd Order IMP } V_{21} = A_3 \left(\frac{3}{4} V_1^2 V_2 \right) + A_5 \left(\frac{15}{8} V_1^2 V_2^3 + \frac{5}{4} V_1^4 V_2 \right)$$

$$\text{5th Order IMP } V_{32} = A_5 \left(\frac{5}{8} V_1^3 V_2^2 \right)$$

V_{mn} is defined as the voltage corresponding to the frequency $(m\omega_1 - m\omega_2)$. Thus, V_{20} is the second harmonic of the fundamental V_{10}, and V_{21} has the frequency $2\omega_1 - \omega_2$.

The magnitude of the 3rd order IMP's relative to the fundamental will then be given by:

$$\frac{V_{21}}{V_{10}} = \frac{\frac{3}{4} K_3 V^2 + \frac{25}{8} K_5 V^2}{1 + \frac{9}{4} K_3 V^2 + \frac{25}{4} K_5 V^4} \tag{15}$$

where,

$$K_3 = A_3/A_1, \; K_5 = A_5/A_1. \tag{16}$$

If we consider the problem only to third order terms, the third order IMP level is given by

$$\frac{V_{21}}{V_{10}} = \frac{\frac{3}{4} K_3 V^2}{1 + \frac{9}{4} K_3 V^2}. \tag{17}$$

It has been recently proposed to reduce third order IMP's by adapting a linearization scheme used with TWT chains. In this scheme, the second harmonic of the driver tube is fed into the output tube at a phase so prescribed as to minimize or cancel out the second harmonic from the output tube. An example of this effect is shown in figure 18[3]. In this case the second harmonic was about 5 dB down from the fundamental in the power tube input. For a phase of about 160 degrees, the output second harmonic was depressed by about 20 dB; whereas, the fundamental output was increased several dB.

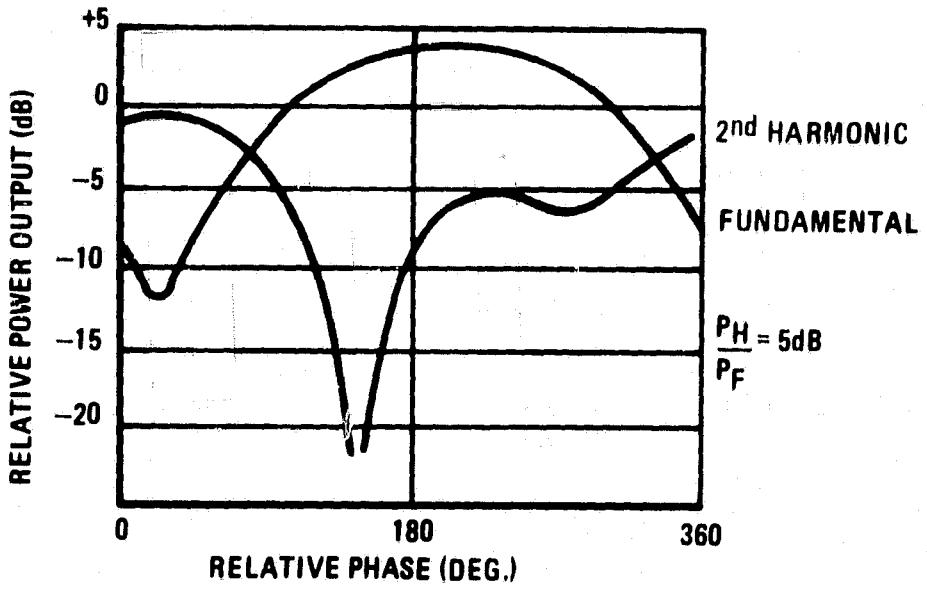

Figure 18. Reduction of 3rd Order IMP's by Proper Phasing of 2nd Harmonic in TWT Chain

The diode amplifier equivalent of this effect differs from the TWT case in two ways. First, the type of nonlinearity is different in that the TWT is an active coupled wave mechanism unlike the avalanche mechanism in an IMPATT diode. This difference is not well documented, but data taken here indicates that at least five terms in the power series must be taken to get a reasonable curve fit. This difference will be discussed below.

More important, in a multistage IMPATT amplifier, the stages are separated by circulators which have useful bandwidths well under an octave, preventing efficient transfer of the driver stage second harmonic to the input of the power stage. Thus, as outlined in the abovementioned contract, the phasing of the second harmonic must be controlled within each stage.

The proposed approach in reducing 3rd order IMP's below those expected from gain compression alone is to use the second harmonic generated within the stage to suppress the third order IMP's. This will be done by reflecting the second harmonic power back to the diode at an appropriate phase by means of adjustable harmonic reflection filter (HRF) built into the diode mount itself.

This situation can be modeled by assuming an input signal consisting of two equal fundamental signals and their respective second harmonics; viz,

$$V_{in} = B_1 \cos \omega_1 t + B_2 \cos \omega_2 t + B_3 \cos (2\omega_1 t + \phi_1) + B_4 \cos (2\omega_2 t + \phi_2) \tag{18}$$

This signal is then impressed on the power series expression of the I - V characteristics. The result for third order IMP's is an additional term arising from the mixing of the second harmonic of one signal and the fundamental of the other. These will have the form:

$$B_1 B_4 \cos (\omega_1 t - 2\omega_2 t - \phi_2)$$

and (19)

$$B_2 B_3 \cos (\omega_2 t - 2\omega_1 t - \phi_1)$$

In order to set the total IMP power to zero, we set the rms IMP current to zero. This results in the following expression, assuming $B_1 = B_2$, $B_3 = B_4$, and $\phi_1 \approx \phi_2$ when $\omega_1 \approx \omega_2$;

$$\cos \phi_1 = \cos \phi_2 = \frac{-\frac{9}{4} \times X^2}{6X} \text{ where } X = A_2^2/A_3. \tag{20}$$

Thus, there is a range of X for which ϕ_2 is real. This can be seen in figure 19, wherein ϕ_2 is plotted vs X. The figure shows a rather broad range of $X = A_2^2/A_3$ for which IMP's can be cancelled.

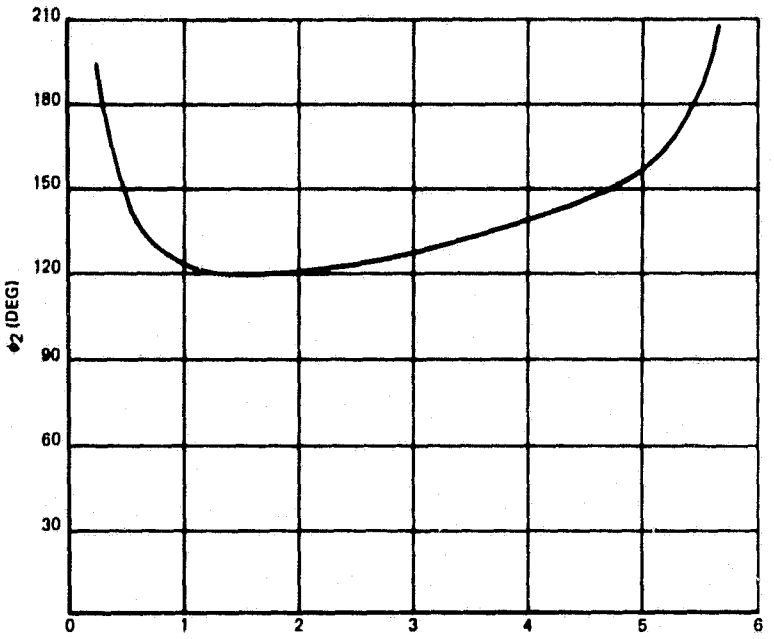

Figure 19. Condition for Cancelling 3rd Order IMP's With 2nd Harmonic Phase (ϕ_2) Adjustment

An order of magnitude of the A's that one could expect for K_u-band IMPATTS can be found from data taken on GaAs and Si diodes tested here at 15 GHz. The measurement problem has been complicated to date by the reactances associated with available diode packages. Diodes tested here were housed in packages which were developed for X-band application and had resonances in that region. At K_u-band these packaged diodes had a strong series inductive component. Typical series equivalent values are given for silicon and GaAs diodes in table 2. Bias current was steady at 150 mA, and operating frequency was 15 GHz.

TABLE 2

TYPICAL SERIES EQUIVALENT VALUES

Silicon

Z_{Diode}	V_{Total}	Inj. Power (mW)
-4.048 + j 53.03	0.589 - j 0.688	8
-4.24 + j 53.06	1.378 - j 1.528	40
-4.24 + j 53.06	1.864 - j 2.162	80
-3.958 + j 53.09	2.637 - j 3.041	160
-3.57 + j 53.12	3.73 - j 4.209	320

GaAs

Z_{Diode}	V_{Total}	Inj. Power (mW)
-5.911 + j 56.37	0.5445 - j 0.6961	8
-5.582 + j 56.4	1.219 - j 1.548	40
-5.456 + j 56.42	1.724 - j 2.184	80
-5.481 + j 60.14	2.249 - j 3.038	160
-4.723 + j 60.22	3.191 - j 4.243	320

V_{total} is the total voltage across the diode and is the sum of the incident and reflected voltages.

Figure 20 shows computed third order IMP levels based on the GaAs diode uncompensated by second harmonic cancellation. The diode was assumed to be in an amplifier configuration with large signal gain = 13 dB. The A coefficients for this case were respectively:

$A_0 = 0.00036$

$A_1 = 0.05694$

$A_2 = 0.00302$

$A_3 = 0.00037$

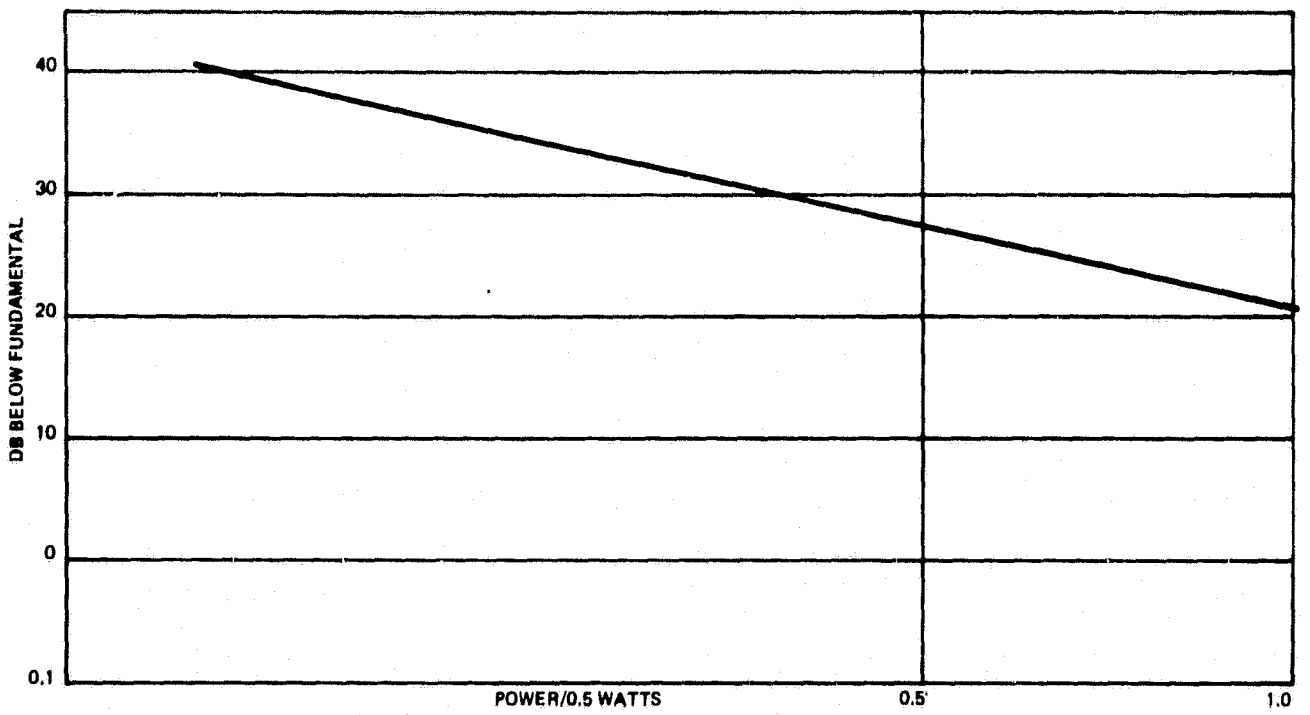

Figure 20. Calculated 3rd Order IMP's (GaAs Diode)

These indicate that the diode was not driven deep into the nonlinear region in the experimental procedure; and the cubic term A_3 is so small that 3rd order IMP's could not be cancelled out by 2nd harmonic reflection because that component, proportional to A_2, would be too large. It is possible, however, to absorb part of the 2nd harmonic power and still achieve cancellation.

Our experimental evidence to date indicates that even in the large signal regime the diodes do not possess as large square and cubic terms in their nonlinear conductance as expected. Typical values of the A's in the nonlinear I - V curve $I = \sum_{i=0}^{n} A_i V^i$ are as given above. If this is generally true of a large sample of diodes, then there is some question as to the 3rd order IMP level one could design to maintain the 4-percent overall efficiency.

Indications of the magnitude of the square and cubic terms in the I - V expansion could be obtained by observing the 2nd and 3rd harmonic amplitudes of diodes run as efficient oscillators. To date evidence is scarce, but several authors[4] state that the harmonic content of IMPATTS operated at the avalanche resonant frequency ($f_a = 2/\tau_a$, where τ_a is the avalanche transit time) is generally low. On the other hand, studies by Gupta and Lomax[5] indicates terminal voltage and current waveforms on a Read model to possess rather high harmonic content, and indeed include some non-integrally related frequencies, and the harmonic content appears to be highly circuit-dependent.

In general, the IMP level will be affected by two mechanisms. The first is the rms voltage-dependent negative conductance, which can be derived from a simple IMPATT diode model in which the predominant nonlinearity arises from a phase slip of the particle current wave with respect to the total voltage across the diode.[4] The 3rd order IMP's are derived from this model by consideration of the instantaneous saturation of the signal voltage in a two-tone test. Computed results[6] are shown in figure 21 which shows 3rd order IMP level versus gain compression in dB. For the simple cubic I - V expansion assumed, it was found that the maximum efficiency occurred when the small signal gain was about equal to twice the gain compression. Thus, we can tabulated in table 3, for our 10-dB amplifier, appropriate combinations of gain compression C, small signal gain (SSG), relative efficiency η/η_{max}, IMP level, and required diode efficiency for an overall 4-percent amplifier efficiency.

It can be seen that with this simple model of diode nonlinearity, the IMP specification combined with the efficiency specification can only be met with laboratory-reported diodes. With commercially available units in either Si or GaAs, the IMP levels will be in the neighborhood of 20 dB, generally consistent with the power series model computed above based on our own measurements of GaAs diodes.

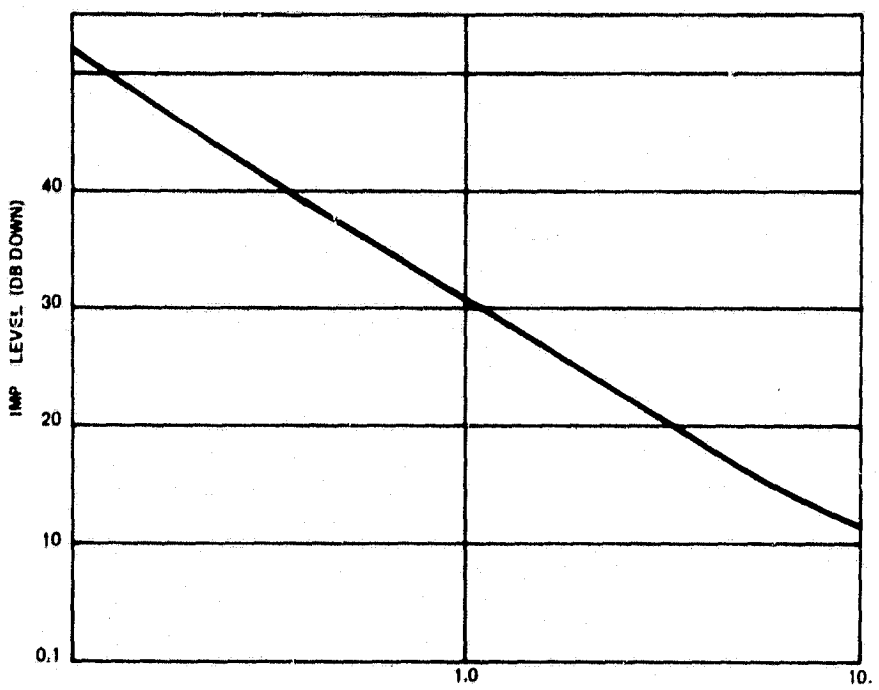

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Figure 21. IMP's vs Gain Compression R

TABLE 3

10-dB AMPLIFIER CHARACTERISTICS

C (dB)	SSG (dB)	Effic/Effic$_{Max}$	IMP Level (dB)	Effic of Diode
1.0	.11	0.27	-31.0	14.8
2.0	12	0.47	-24.5	8.5
3.0	13	0.58	-21.0	6.9
4.0	14	0.65	-18.9	6.2

The second mechanism to affect IMP levels arises from the level of square term in the I - V curve, and is the term which would give rise to second harmonic generation in an oscillator experiment, and is the basis of the herein proposed IMP reduction process by which the fundamental signal at

frequency ω_1 is modulated by the second harmonic of ω_2. Although the physical mechanism for this is not well documented, Brackett[4] has shown strong dependence of diode output on the phase and magnitude of 2nd harmonic injected input for IMPATTS not operating at the avalanche transit time frequency.

Implementation of this harmonic phase injection principle will be done by using a harmonic reflection filter in the plug design. The requirements of such a filter are that it be mechanically adjustable, it have a high VSWR at the 2nd harmonic, and be transparent at the fundamental.

Design of the (HRF) can be done in the diode mount vicinity. Such a filter can consist of two lumped capacitors separated by $\lambda/4$ at the second harmonic frequency. The filter is virtually transparent at the fundamental. Figure 22 shows a computed response of such a filter designed for a coaxial mount. To illustrate the effect of this filter on the bandwidth of a single diode amplifier, the gain over the desired band was computed for a coaxial mount in which this filter was included. Gain variation within ±0.35 dB in 12 dB over the 100-MHz band was computed.

Another type of linearization of the input-output characteristic of the amplifier will be considered next. A typical avalanche diode amplifier usually consists of a linear region and a saturation region which become distinct at typically 3 to 10 dB below the maximum saturated output power. Figure 23 illustrates[7] the input-output characteristic of a single-tuned avalanche amplifier as a function of operating frequency. The amplifier was tuned for a 10 dB small signal gain at 10 GHz. A significant point to notice is that substantial linearization can be accomplished by operating slightly below the frequency of optimum small signal gain. This effect is explained by the fact that the resonant frequency of the amplifier shifts downward with increasing signal power. By intentionally tuning the small

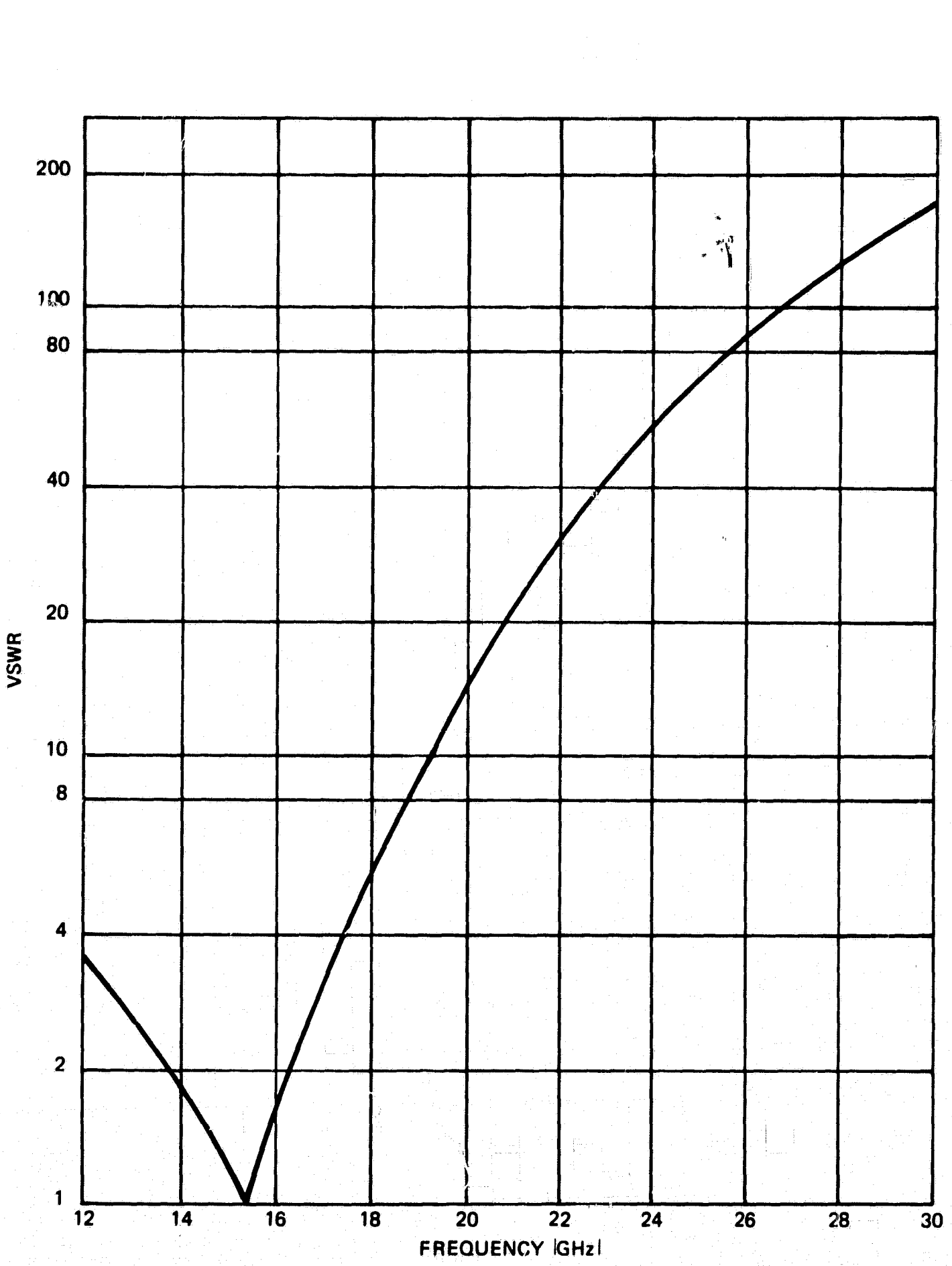

Figure 22. Computed Response of Harmonic Rejection Filter

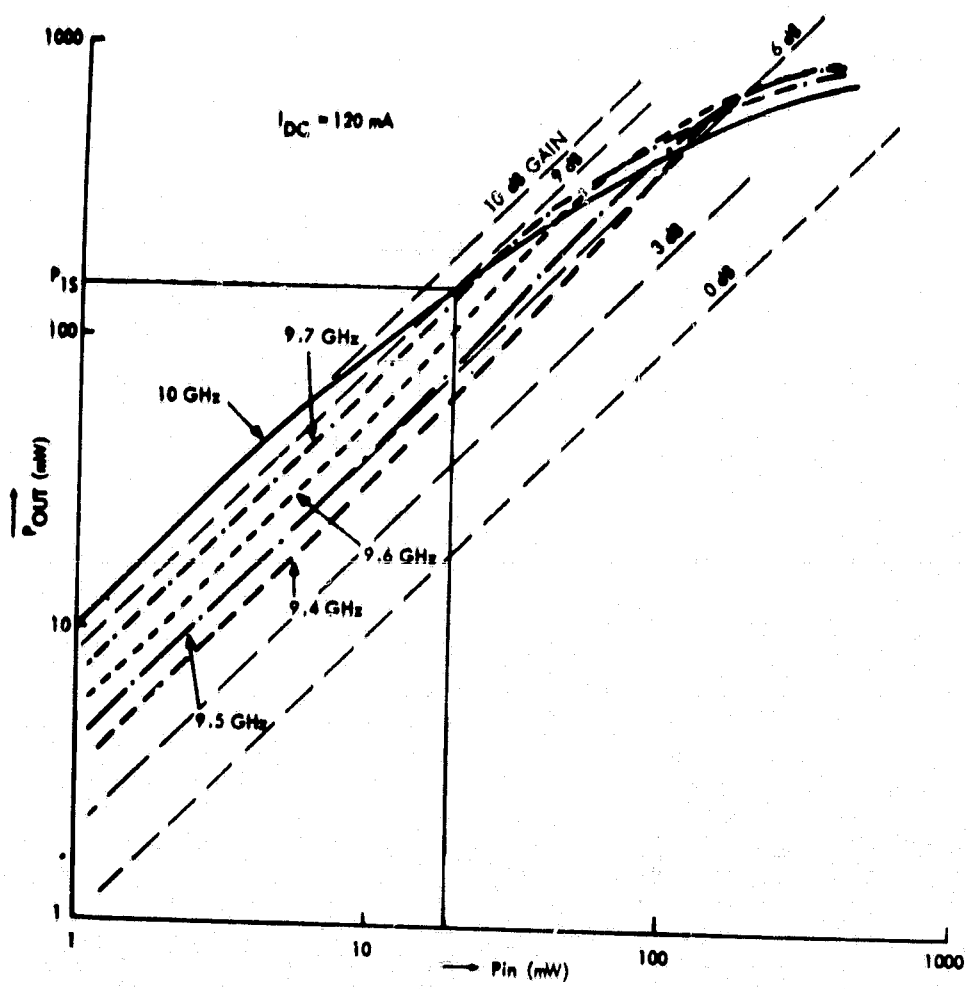

Figure 23. Transfer Power as a Function of Input Power and Frequency

signal resonant point of the amplifier to a frequency slightly above the described operating frequency, the negative conductance reduction will be compensated over the range of signal levels by the opposing effects of the lowering of the resonant frequency and the reduction of $\left|-G_D\right|$ with increasing signal level. In a narrow-band amplifier, this effect can be used to reduce distortion. The transfer phase of the same amplifier is shown in figure 24.[7]

A good test for the linearity of an amplifier is a measure of the third order intermodulation product using two closely spaced input frequencies. In figure 25, the third order intermodulation product D_1 relative to the carrier signal amplitude, is plotted as a function of total carrier power relative to the -1-dB single-carrier compression point. Curves 1 and 2 represent data obtained from an avalanche amplifier at a center frequency of 10 GHz and at 9.5 GHz, respectively. As expected, the curve at 9.5 GHz shows lower distortion due to operation in a more linear range. Curves for two typical TWT amplifiers are also plotted for comparison purposes. It should be noted that the intermodulation products for TWT's and avalanche amplifiers are comparable for equal $\Sigma P_n/P_{ls}$.

2.5 DIODE EVALUATION AND TEST PROCEDURE

The purpose of this part of the program was to evaluate various commercially available IMPATT diodes for use as reflection type amplifiers in a narrow band centered at 15 GHz. Diodes of two manufacturers were tested - Hughes Aircraft Company, Electron Dynamics Division and Raytheon's Special Microwave Devices Operation. The choice of these two vendors was made on the basis of quality, availability, and price. The Hughes diodes were Si diffused junctions; whereas, the Raytheon diodes were GaAs Schottky barrier junctions. Initial tests were performed with both types of diodes

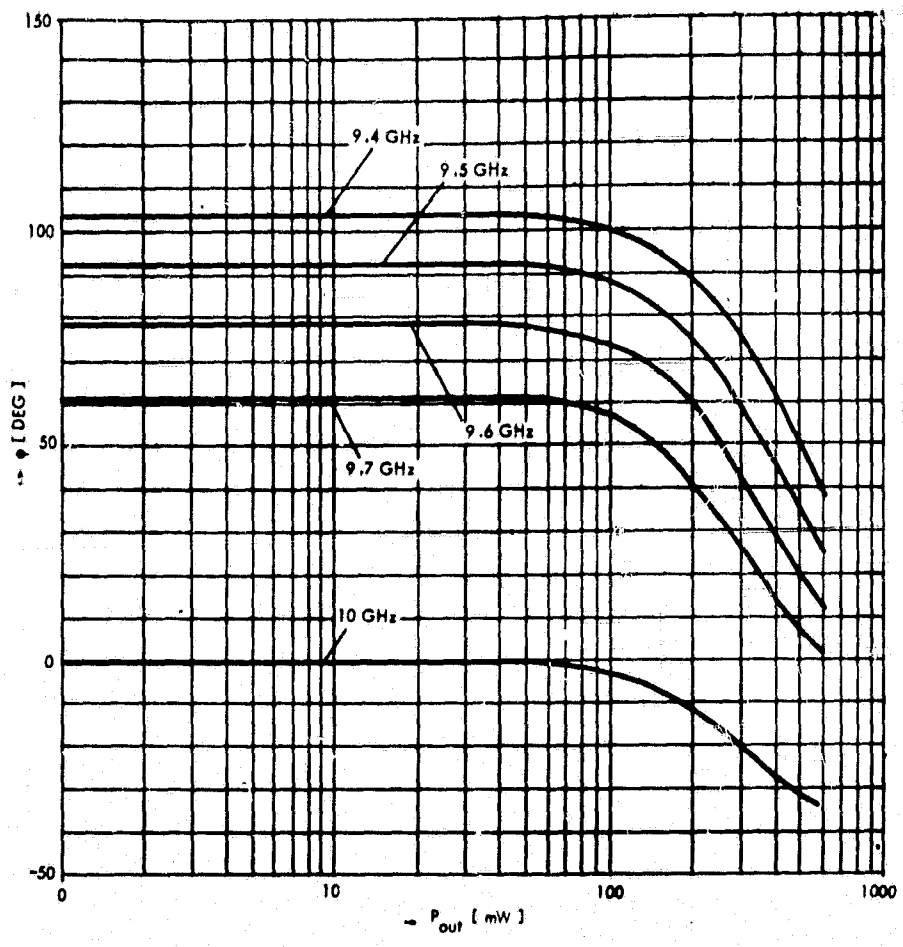

Figure 24. Transfer Phase as a Function of Input Power and Frequency

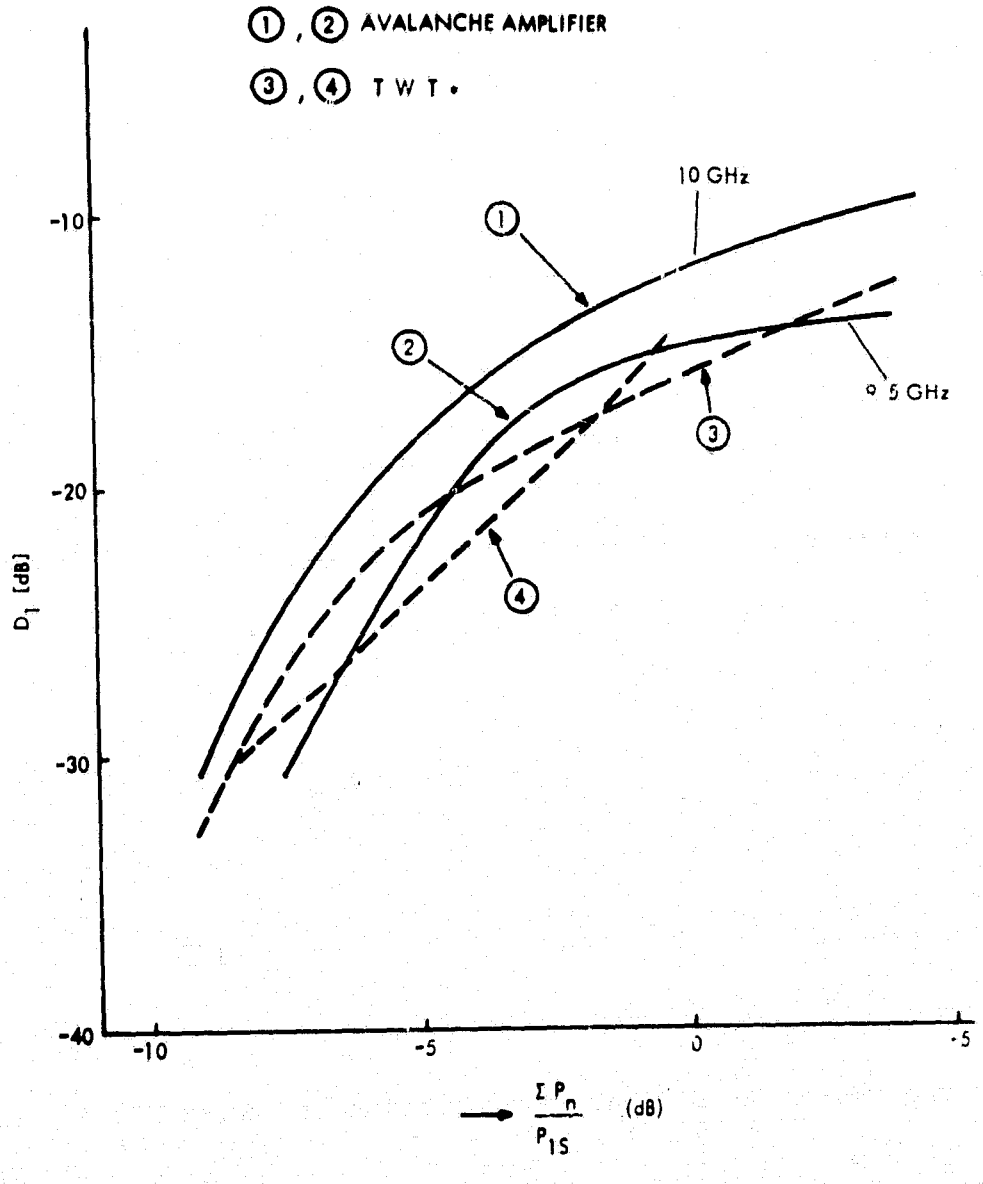

Figure 25. Third Order Intermodulation Product as Function of Input Power Level

mounted in type 16 packages (see figure 12). Figure 26 illustrates the test circuit used. A slotted line technique was chosen because of its relative simplicity and adaptability to high RF power situations. Although a Hewlett-Packard Network Analyzer was available, its use, at present, is limited to low RF power and frequencies of X-band or below. Tests on the analyzer showed substantial inaccuracies above 12 GHz.

2.5.1 Test Procedures

All diodes were tested at 15 GHz, over a range of incident RF powers and bias conditions. Incident RF powers (corrected for line losses) ranged from 8 mW to 320 mW, and bias conditions ranged from unbiased to the point of maximum recommended reverse current.

The diodes under test were mounted in a modified commercially available 7-mm precision short circuit termination as shown in figure 27. The connector was modified by precision boring a 7-mm ID to mate with a similar precision connector at the end of the slotted line. There are several advantages to this form of test mount.

- It allows precise knowledge of the reference plane used for characterization.
- The top contact of the diode package matches very closely the diameter of the inner conductor of the 7-mm connector (3.04 mm), thus reducing the problem of parasitic reactances due to discontinuities at the measurement plane.
- The spring-loaded collet at the mating plane of the precision 7-mm connector allows for positive contact pressure on the diode for biasing purposes.

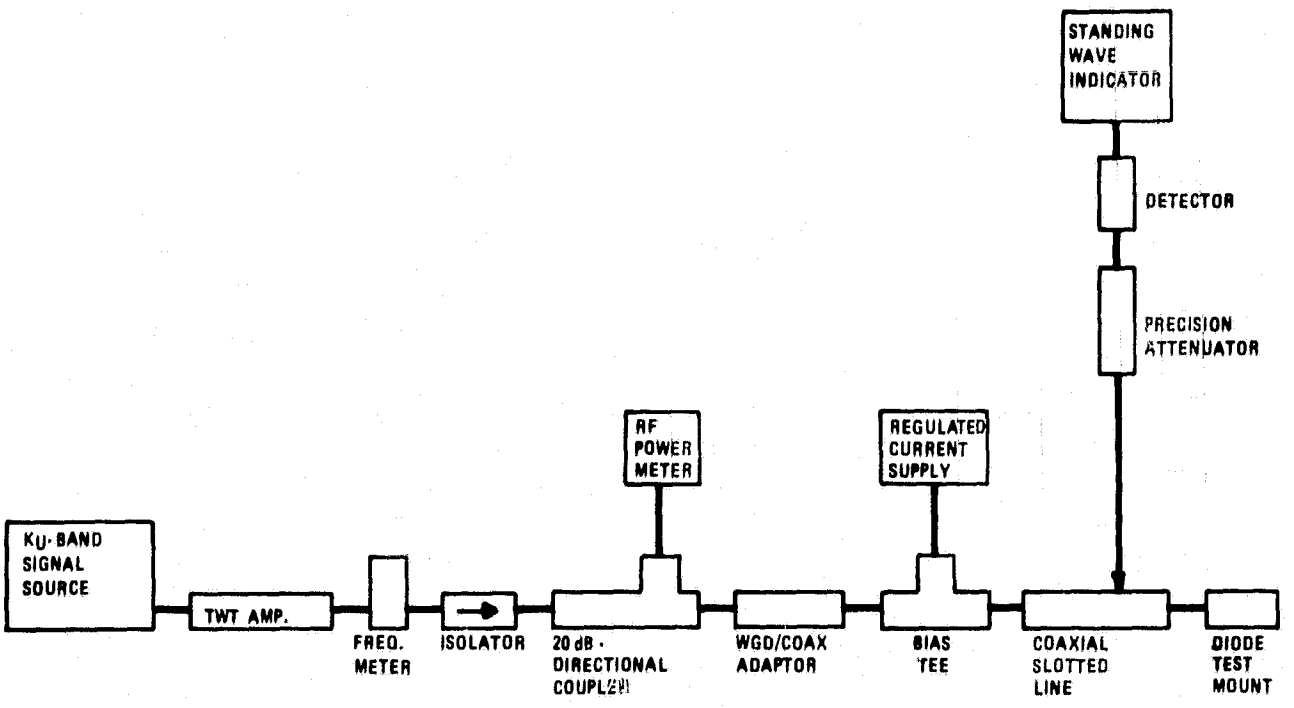

Figure 26. Schematic of Diode Test Circuit

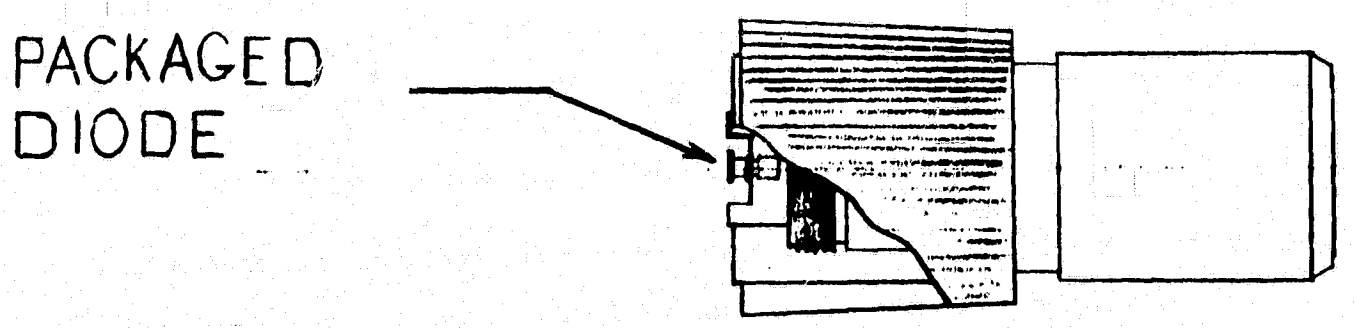

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Figure 27. Diode Test Mount

An Alfred 625B signal generator was used to drive a 10-watt minimum Hughes K_u-band TWT amplifier in order to obtain the power levels required for testing. The power levels required were intentionally substantially lower than the maximum rated power of the amplifier since minimum signal distortion was desired for diode characterization. To ensure that in the testing for 3rd order IMP's, the signal source and drive amplifier must not generate IMP's above a very low level. Figure 28 shows IMP levels in the proposed Hughes TWT driver.

2.5.2 Data Processing and Analysis

The raw data obtained was in the form of null positions and standing wave ratios (in dB) versus incident RF power level and bias. An obvious problem was the determination of the positive to negative crossover point of the diode resistance since the slotted line technique does not discriminate between magnitudes of reflection coefficient greater than unity (return gain) or less than unity (return loss). The solution was to track the change in standing wave ratio with increasing reverse bias current, or $\Delta(SWR)/\Delta I$. The crossover was then determined by the point at which the ratio changed sign. Figure 29 graphically illustrates this technique. Through this technique, it was established that the crossover point occurred in the range 60 to 90 mA for the diodes tested.

Two computer programs were developed to process the raw data. The first program, which was used extensively in the first phase, calculated the actual diode impedance and total complex RF voltage at the diode. A sample printout is shown in figure 30. The second program, which was tested but not used, was developed with the goal of correcting for any parasitics, such as transformers, placed between the slotted line and the diode test mount.

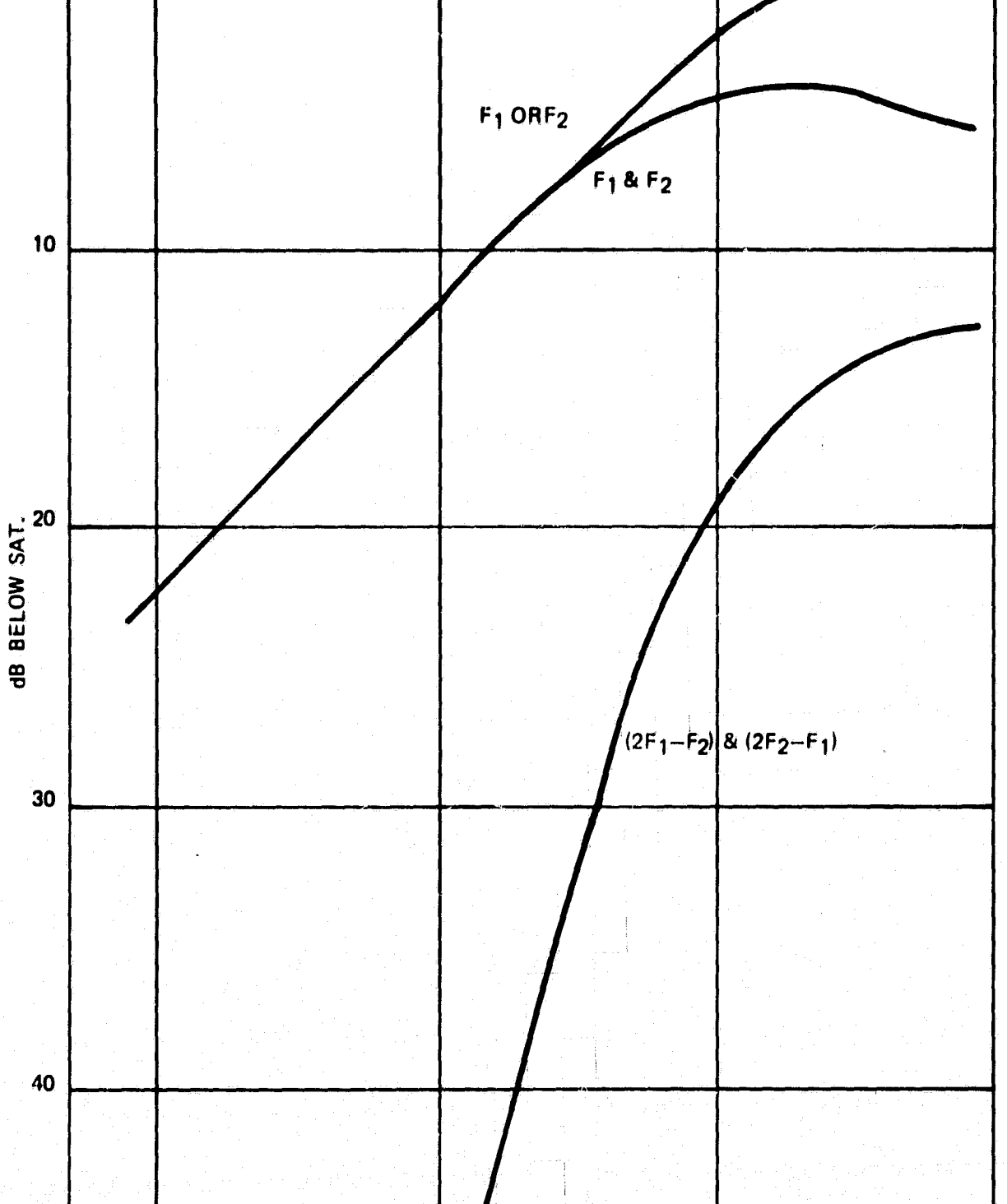

Figure 28. Intermodulation Products in 10-Watt Hughes TWT

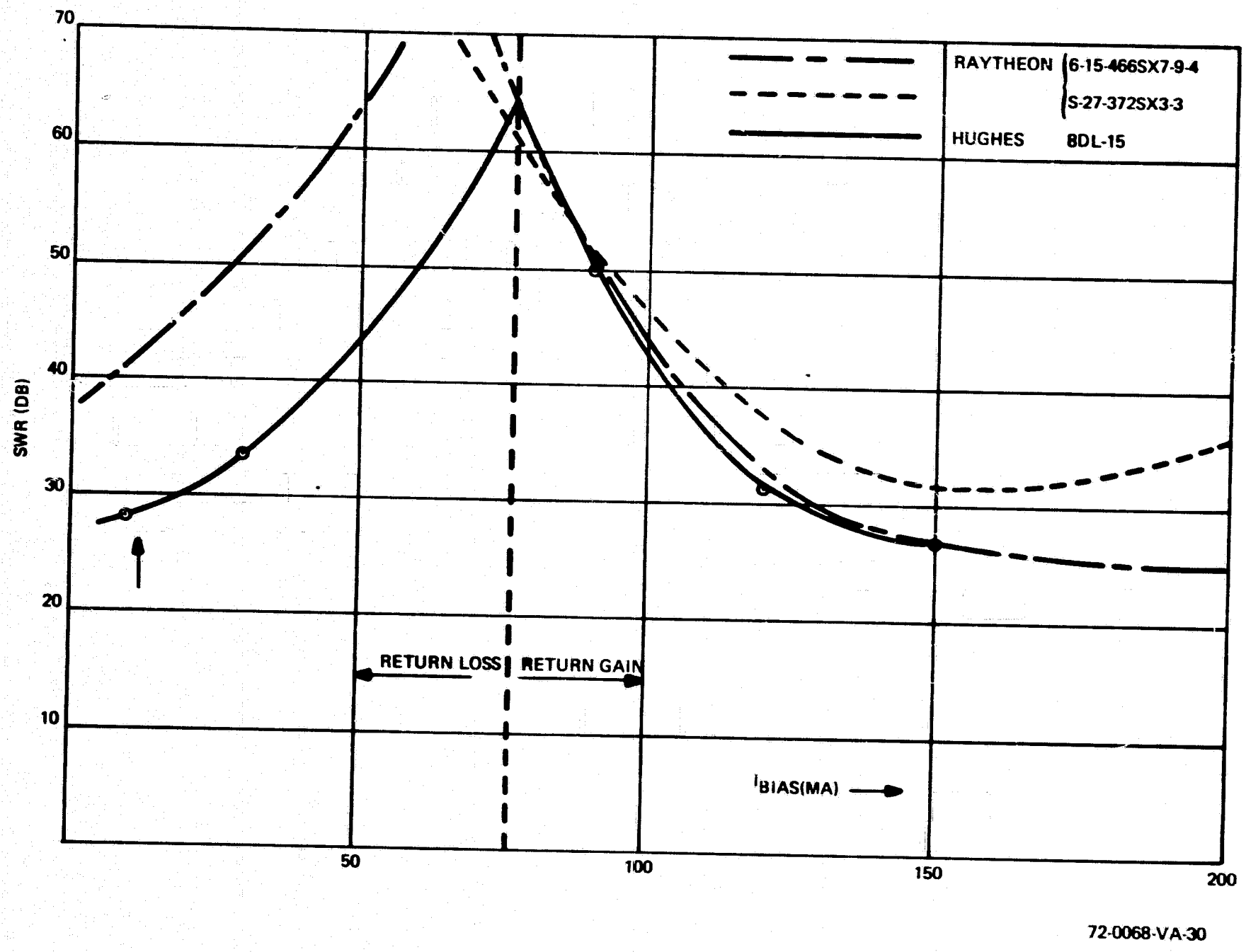

Figure 29. Technique Used to Determine Positive/Negative Resistance Crossover of IMPATT Diode in Slotted Line System

CURRENT(MA)	Z(DIODE) R	X	V(TOTAL) REAL	IMAG
**********FREQ=	1.514E+10	POWER=	8.000E-03WATT**********	
9.000E+01	-4.498E-01	6.791E+01	4.435E-01	-6.078E-01
1.200E+02	-2.127E+00	6.787E+01	4.390E-01	-6.223E-01
1.500E+02	-3.421E+00	6.559E+01	4.552E-01	-6.410E-01
1.800E+02	-2.980E+00	6.561E+01	4.564E-01	-6.369E-01
2.000E+02	-2.189E+00	6.786E+01	4.388E-01	-6.228E-01
**********FREQ=	1.514E+10	POWER=	4.000E-02WATT**********	
9.000E+01	-4.699E-01	7.021E+01	9.487E-01	-1.346E+00
1.200E+02	-2.008E+00	6.787E+01	9.823E-01	-1.389E+00
1.500E+02	-3.230E+00	6.560E+01	1.019E+00	-1.429E+00
1.800E+02	-2.946E+00	6.562E+01	1.021E+00	-1.423E+00
2.000E+02	-2.016E+00	6.566E+01	1.026E+00	-1.404E+00
**********FREQ=	1.514E+10	POWER=	8.000E-02WATT**********	
9.000E+01	-4.699E-01	7.021E+01	1.342E+00	-1.902E+00
1.200E+02	-1.797E+00	6.567E+01	1.453E+00	-1.979E+00
1.500E+02	-3.193E+00	6.560E+01	1.441E+00	-2.020E+00
1.800E+02	-2.846E+00	6.562E+01	1.444E+00	-2.010E+00
2.000E+02	-1.601E+00	6.567E+01	1.454E+00	-1.974E+00
**********FREQ=	1.514E+10	POWER=	1.600E-01WATT**********	
9.000E+01	-4.699E-01	7.021E+01	1.897E+00	-2.690E+00
1.200E+02	-1.547E+00	6.568E+01	2.057E+00	-2.789E+00
1.500E+02	-3.120E+00	6.561E+01	2.039E+00	-2.854E+00
1.800E+02	-2.479E+00	6.564E+01	2.047E+00	-2.827E+00
2.000E+02	-1.444E+00	6.568E+01	2.059E+00	-2.785E+00
**********FREQ=	1.514E+10	POWER=	3.200E-01WATT**********	
9.000E+01	-4.699E-01	7.021E+01	2.683E+00	-3.804E+00
1.200E+02	-1.460E+00	6.568E+01	2.911E+00	-3.939E+00
1.500E+02	-2.912E+00	6.562E+01	2.888E+00	-4.024E+00
1.800E+02	-2.368E+00	6.565E+01	2.896E+00	-3.992E+00
2.000E+02	-1.022E+00	6.569E+01	2.918E+00	-3.914E+00

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Figure 30. Computed Diode Data

Its use is somewhat more complicated than the former program in that it requires measurement of three reference impedances in addition to the actual diode impedance. Using these three references, the program computes a Z-matrix for an arbitrary 2-port which includes the effects of the transformer, for instance. It then inverts the matrix and applies it to the measured data. The output is in the form of measured diode impedance and corrected diode impedance. More detailed diode testing, which is foreseen for any further diode evaluation, will require the use of a transformer to lower the magnitude of the measured SWR's and, consequently, will make use of this computer program.

2.6 THERMAL CHARACTERISTICS

There are three areas of concern in the thermal design of such an amplifier. These are:

a. Thermal resistance from chip junction to the package boundary

b. Thermal resistance from the package to the heat exchanger

c. The heat exchanger itself.

a. Quoted figures for K_u-band high power chips have been in the vicinity of 10°C/watt. A sample calculation is included. It assumes a silicon chip whose diameter $2r_o$ is 10 mils defining a contact area A_{P+} to the copper stud, whose thermal conductivity K is 3.88 watts/cm^2°C with a 10-μm-thick P^+ layer h_p through which the heat passes in a laminar flow path, and a spreading resistance into an essentially infinite copper heat sink. For this case, the spreading resistance R_{T_S} is

$$R_{T_S} = \frac{1}{4Kr_o} = 5.37°C/watt$$

The P^+ region thermal resistance $R_{T_{P+}}$ is

$$R_{T_{P+}} = \frac{h_p}{K_{P+} A_{P+}} = 1.47°C/watt$$

where K_{P^+} is the P^+ region thermal conductivity. The thermal resistance through the silicon-gold-copper interface is 3.3°C/watt. The total thermal resistance is then 10.2°C/watt, or for our case, a total temperature rise from package stud to junction of 100 to 120°C. If in later diode models copper or gold plated type II diamond heat spreaders are used, this will come down about 50°C.

b. Thermal resistance from package to heat exchanger is a fairly complex heat path, limited by the interface drop across the threaded junction between the stud and the top plate. This has been calculated to be about 10°C assuming an average pressure of 10 psi.

c. Heat Exchanger - With a maximum ambient temperature of 50°C it is clear that air cooling is out of the question without extreme volumetric rates of airflow and large bulky heat exchangers. It was therefore decided to go to liquid cooling with the proviso that at a later time cold plate cooling could be incorporated.

The cooling geometry chosen was one turn of 1/4-inch copper tube brazed onto the heat sink side of the cavity assembly. Room temperature water is assumed to flow through at the required flow rate which is estimated as follows, assuming the maximum allowable dissipation of 250 watts.

The heat transfer coefficient necessary to dissipate 250 watts while maintaining a mean temperature difference of 50°F or 27.8°C between the wall temperature and the bulk fluid temperature is about 650 BTU/(hr-ft^2-°F). Using this value for the heat transfer coefficient, the Nusselt number can be calculated. With the appropriate expression for the Nusselt number (which includes the Prandtl number and the Reynolds number), the Reynolds number can be calculated. Since the Reynolds number is the product of the density, velocity, and tube diameter divided by the viscosity, the mean velocity of the fluid can be determined. From the fluid velocity, the mass flow rate can be calculated using the expression $\dot{m} = \rho AV$

where $\dot{m}$ = mass flow rate in lb/sec

ρ = fluid density

V = mean fluid velocity

A = cross sectional area

The mass flow rate necessary for cooling with water is approximately 1 lb/min; whereas, for coolanol 20, the flow rate is approximately 5 lb/min. Thus the flow rate for water will be between 0.25 and 1.0 meters/sec for tubing ID's for 1/4 and 1/8 inch, respectively, with 5 times these figures for coolanol 20.

2.7 OUTPUT CONNECTION

The output circulator will be a modified commercially available 5-port waveguide circulator with two of the ports terminated. The modification is to peak up the response for the narrow band of this application such that the insertion loss per circulation is less than 0.1 dB, and the isolation per circulation is greater than 25 dB. Placing the cavity at the central port of this circulator ensures better than 1.2 VSWR both on input and output, and output insertion loss of 0.2 dB. This corresponds to an efficiency degradation of about 5 percent of the overall efficiency.

2.8 CONSTRUCTION PRINCIPLES

The amplifier is designed in three basic subassemblies; the circulator, the cavity, and the plug.

The circulator, a purchased part, will be a five port E and M Labs model modified to have minimum insertion loss from the cavity to the output.

The cavity includes a gold plated 304 stainless steel cylindrical body part housing holes for adjustment screws, alignment pins and bolts, the output coaxial outer conductor, and bias lead band stop filters. The body part is capped with an OFHC disc-shaped piece which completes the radial line cavity and in which the diode mounts or studs are located. This part also includes the fluid cooling duct in the form of a brazed-on OFHC tube, a technique familiar to high-power microwave tube technology. The 304

stainless steel body and the OFHC cap have virtually identical thermal expansion coefficients which will provide thermal stability to the cavity parameters. High microwave electrical conductivity will be obtained by gold plating the stainless steel.

The high-tolerance items include the plug hole diameter, their angular and radial spacing, and the output coaxial line ID.

The plug design concept chosen consists of a series of metal and dielectric slugs and spacers which combined comprise the bias lead band stop filter and the diode matching circuit. Threaded joints will guarantee good mechanical integrity while allowing flexibility to match a tolerance spread of diode package reactances.

The weight of the first experimental model is estimated at about 6.5 pounds, most of which is the body and heat sink. The circulator is a modified waveguide 5-port model chosen for its low insertion loss and relatively low price. The cavity material is 304 stainless steel for the body and OFHC for the top, chosen for ease of manufacturing and stability. For the delivered models, weight reduction will be achieved in the body and top by going to gold-plated aluminum and in the circulator by going to stripline in the input circulator stage. The aluminum cavity top will have a thermal conductivity about half that of copper, sufficient to provide proper heat transfer to the heat exchanger. Estimated weight is about 1.75 pounds for the body and 0.350 pound for the circulator.

Assembly of the cavity on the E&M circulator will use an aluminum bracket, the details of which will be set upon receipt of the detailed dimension of the circulator. The circulator dimensions have been rough quoted as 4-1/8 x 2-9/16 x 1-5/16 inches, with the waveguide input and output ports on the 2-9/16- x 1-5/16-inch ends and the OSM coax connector leading to the cavity centered approximately on the broadface. A set of engineering drawings is included as figures 31 through 41.

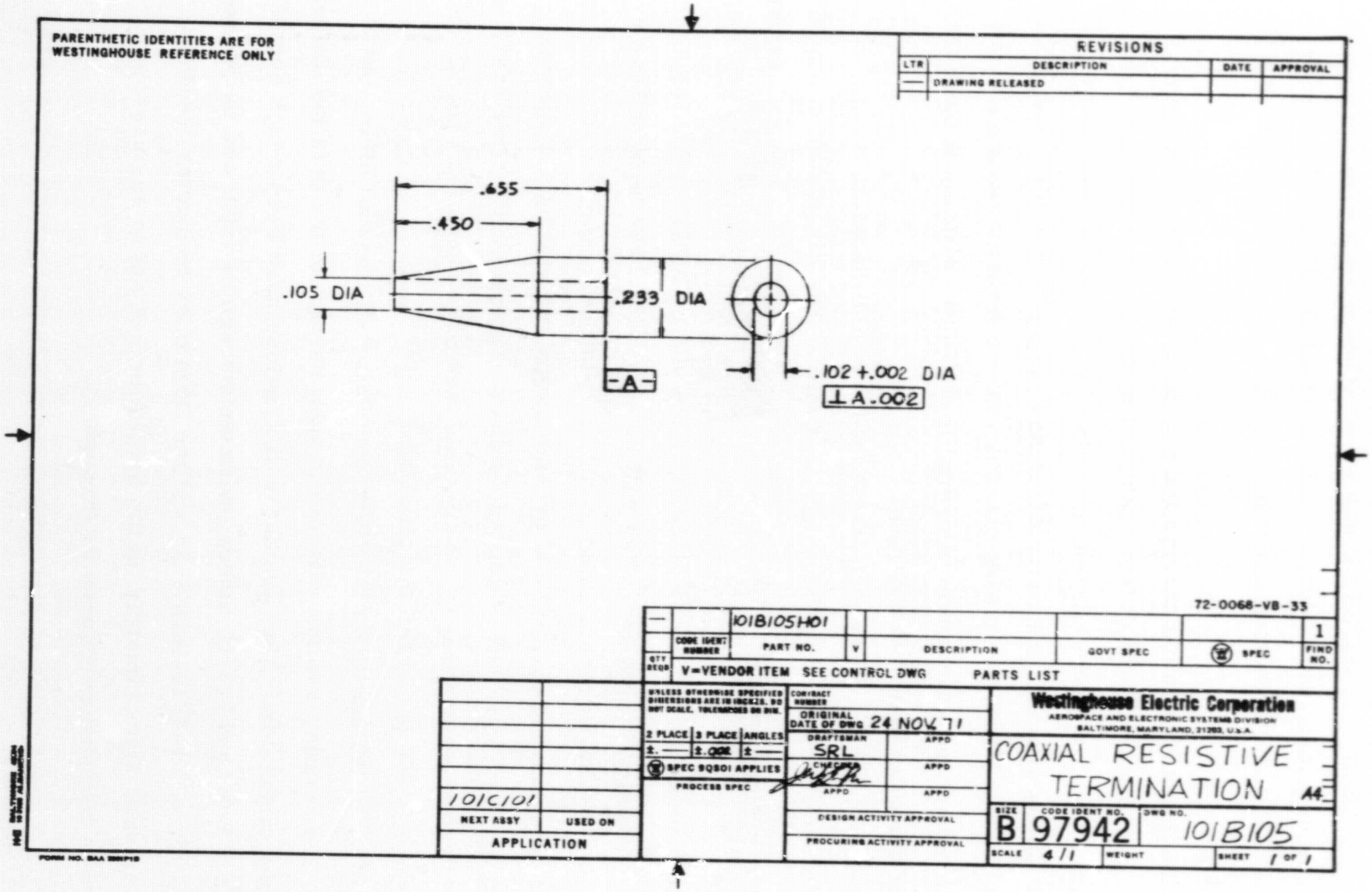


Figure 31. Coaxial Resistive Termination

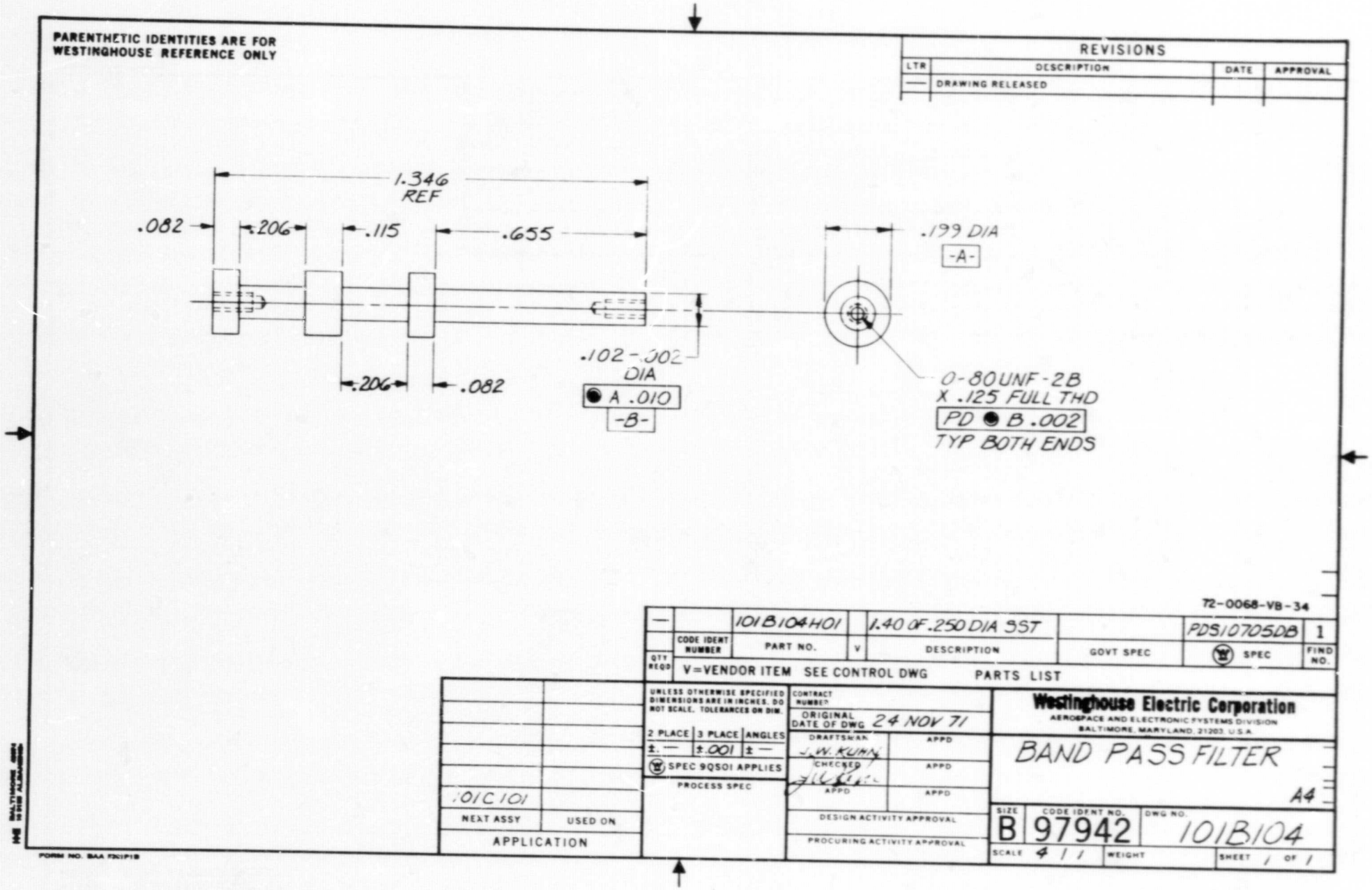


Figure 32. Bandpass Filter

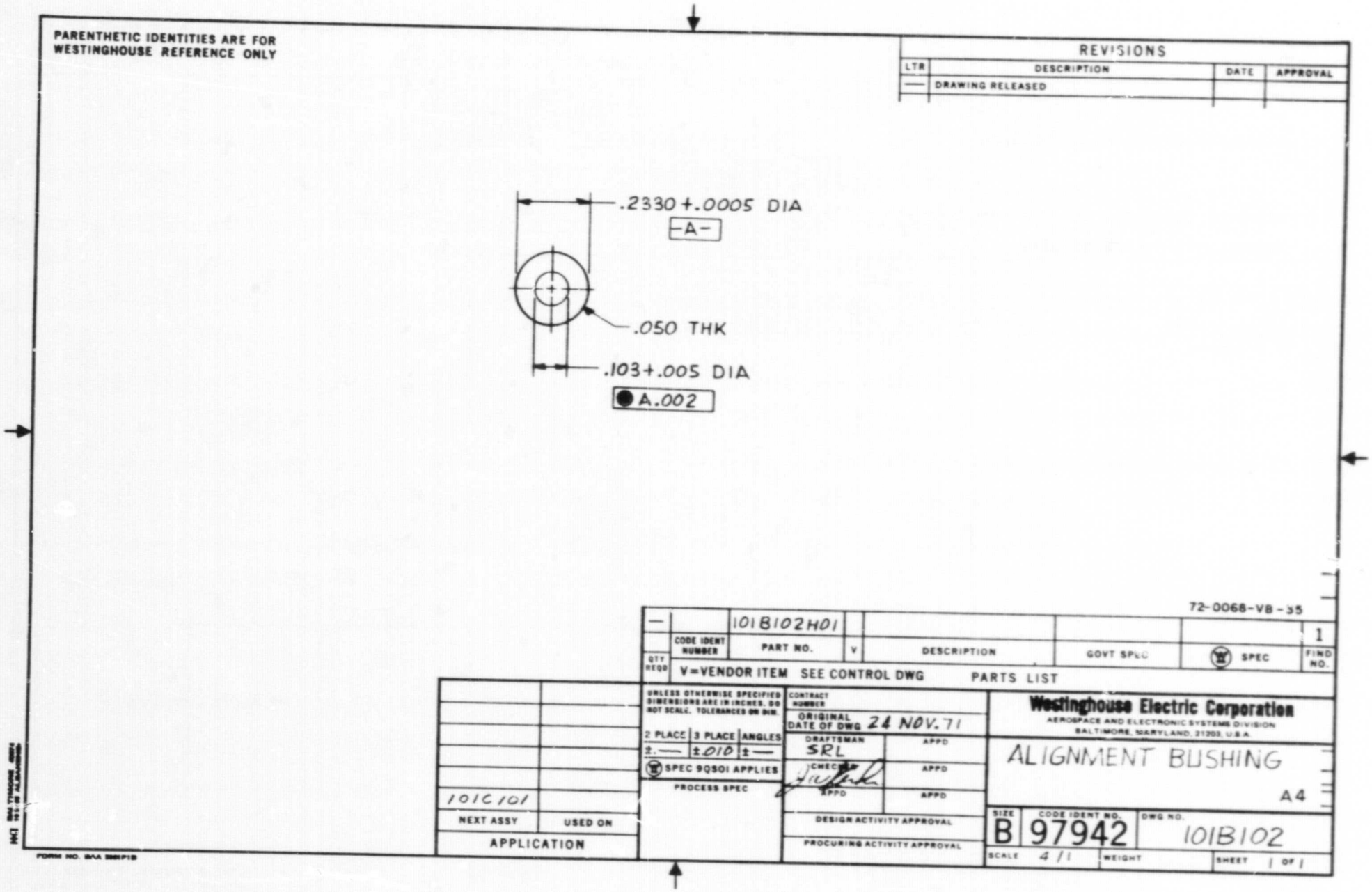


Figure 33. Alignment Bushing

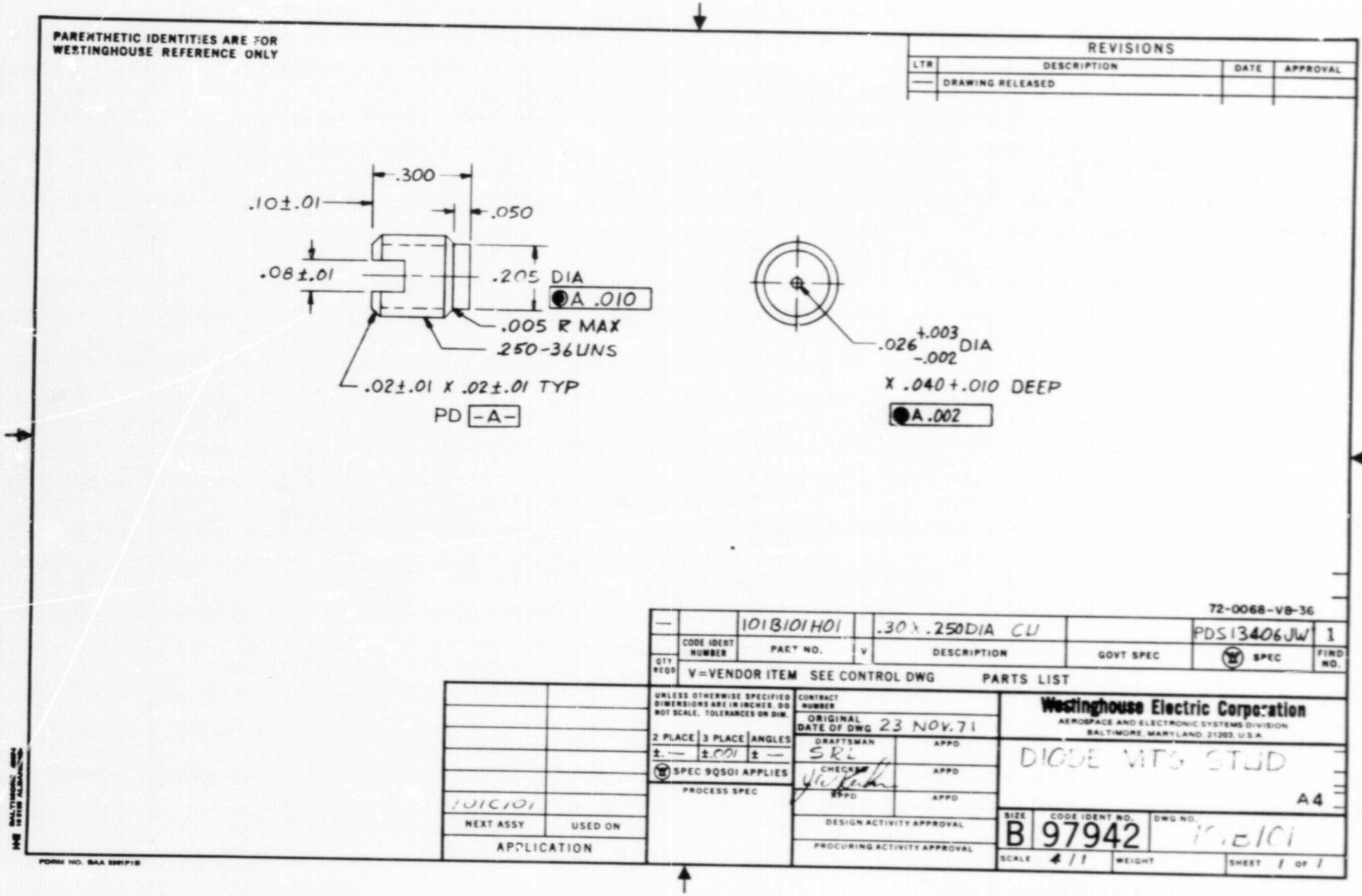


Figure 34. Diode Mounting Stud

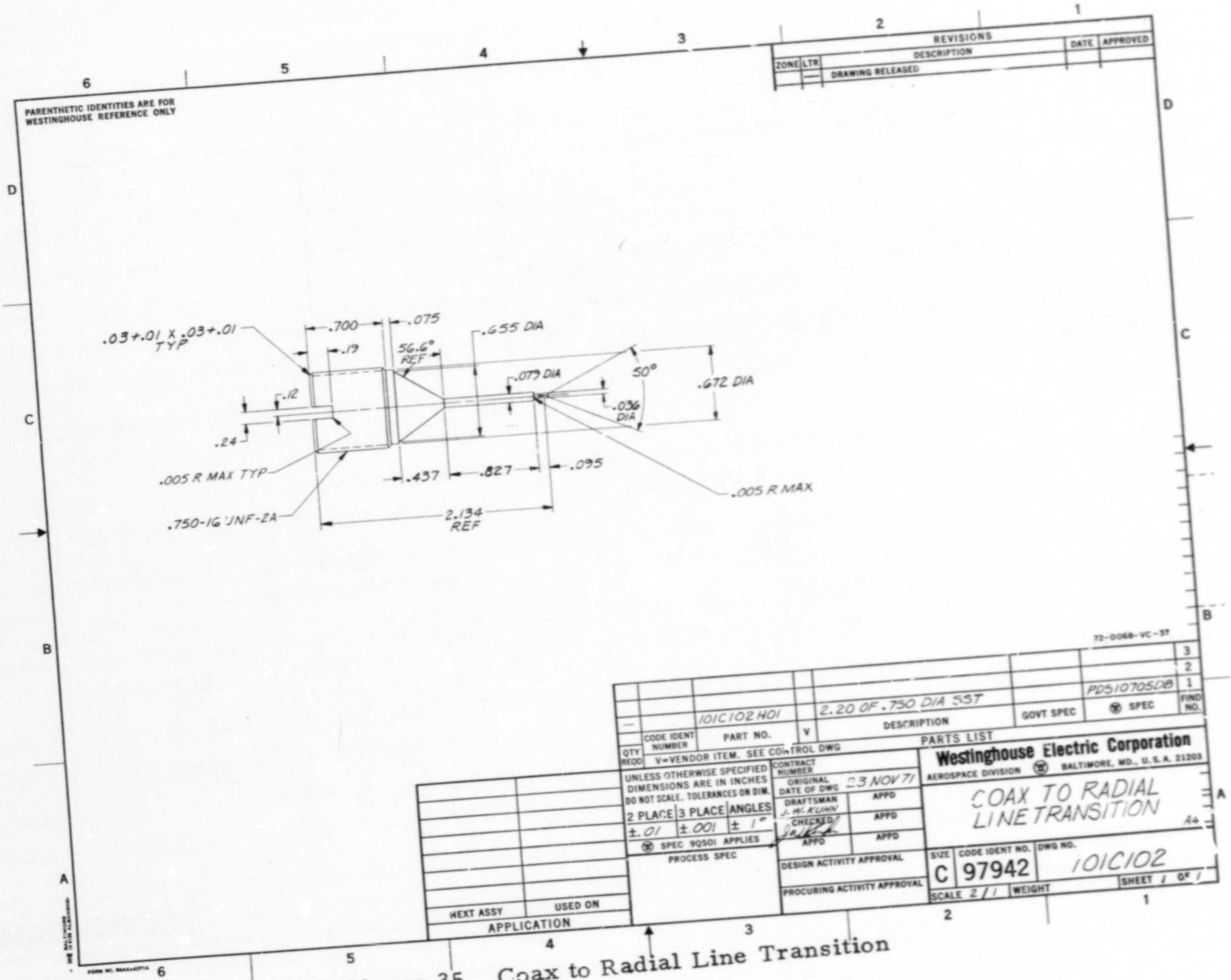


Figure 35. Coax to Radial Line Transition

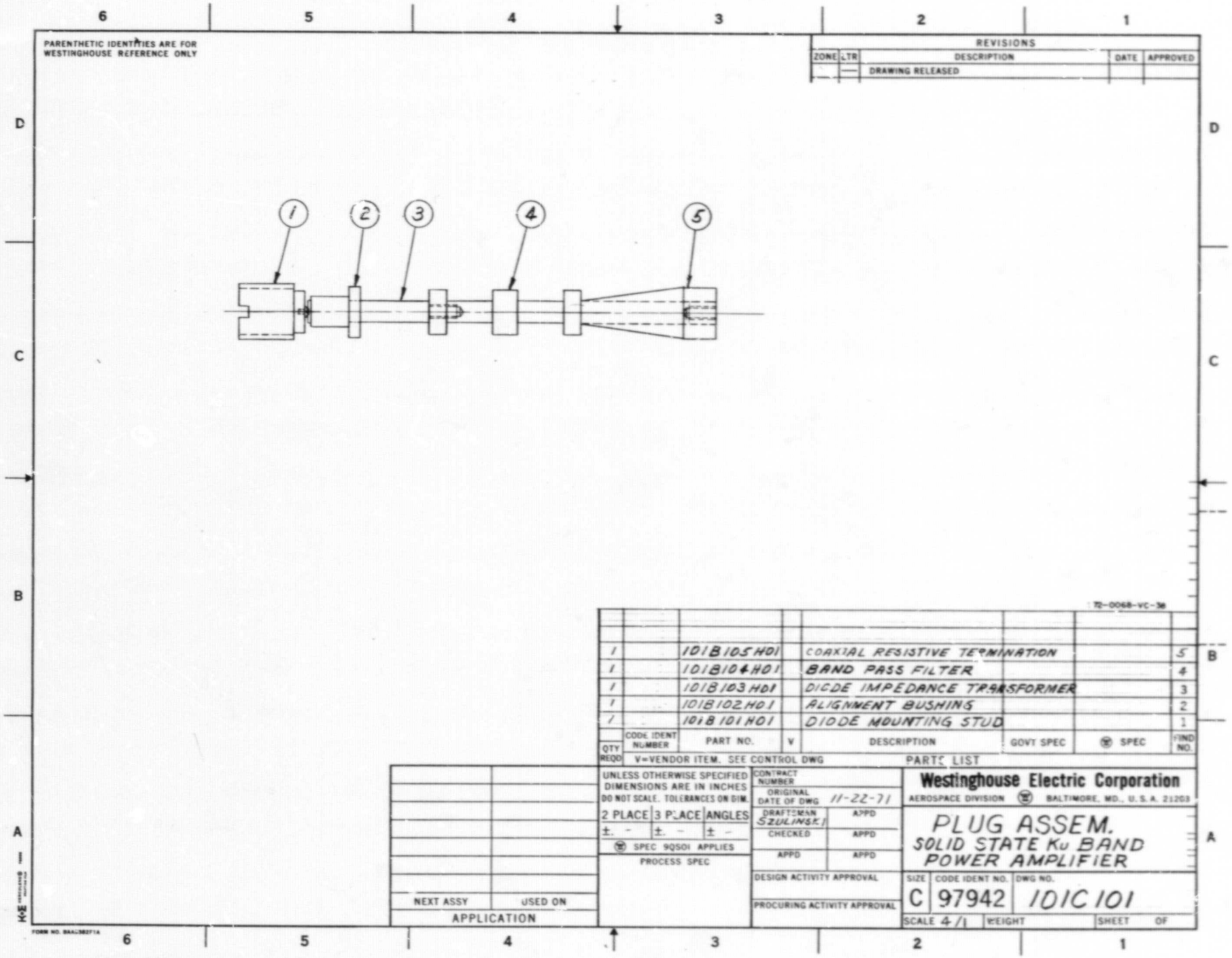


Figure 36. Plug Assembly

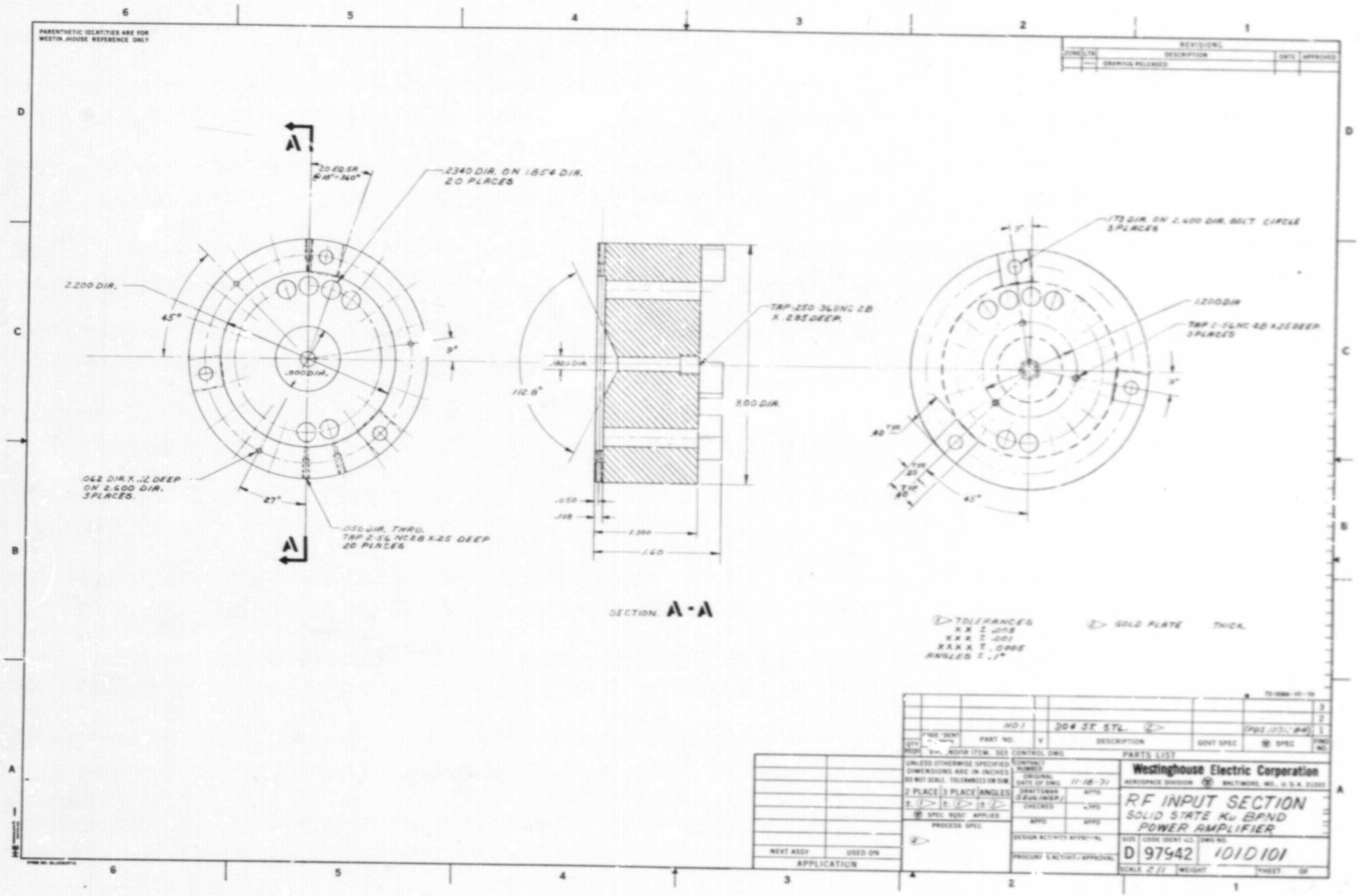


Figure 37. RF Input Section

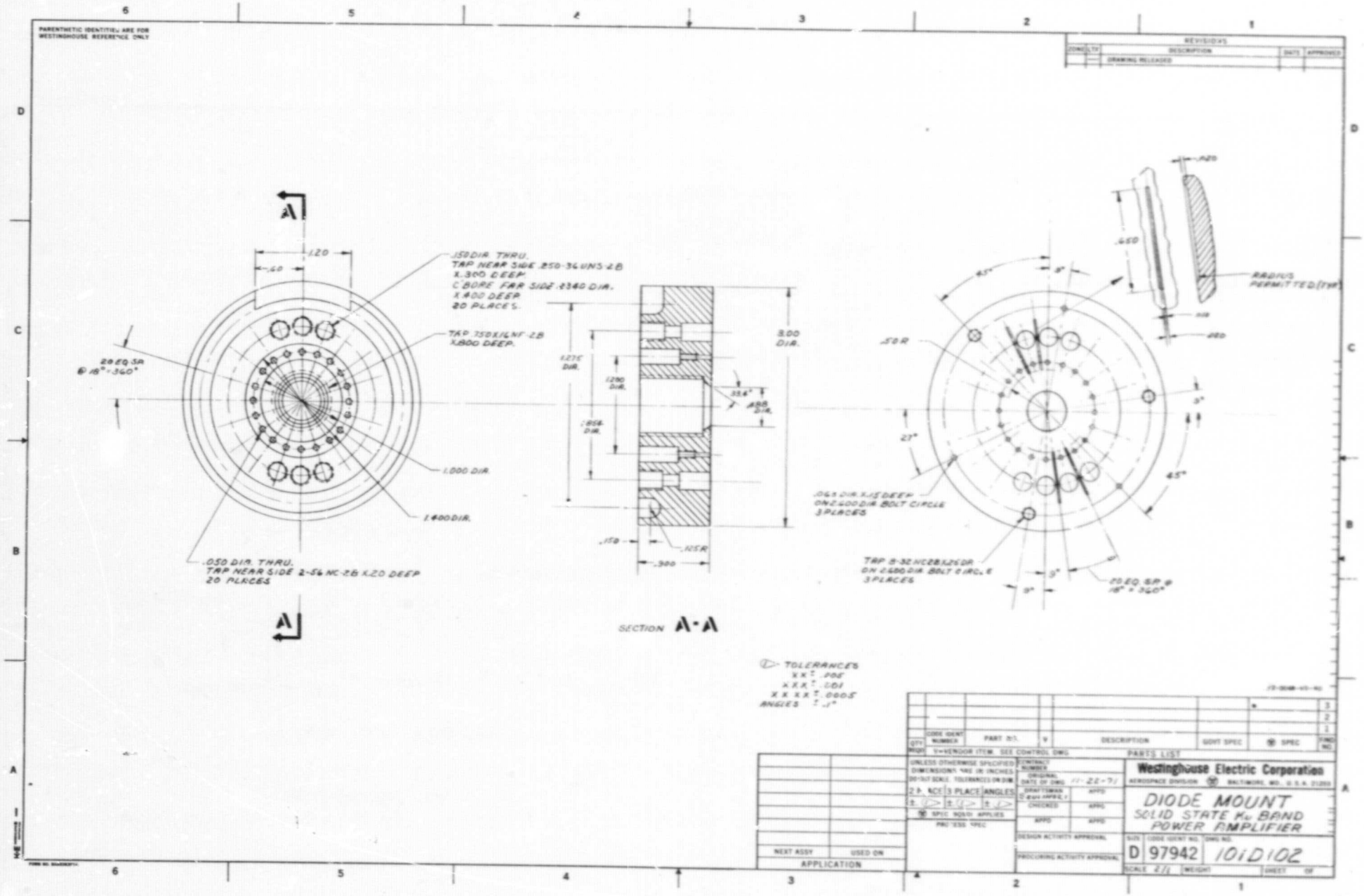


Figure 38. Diode Mount

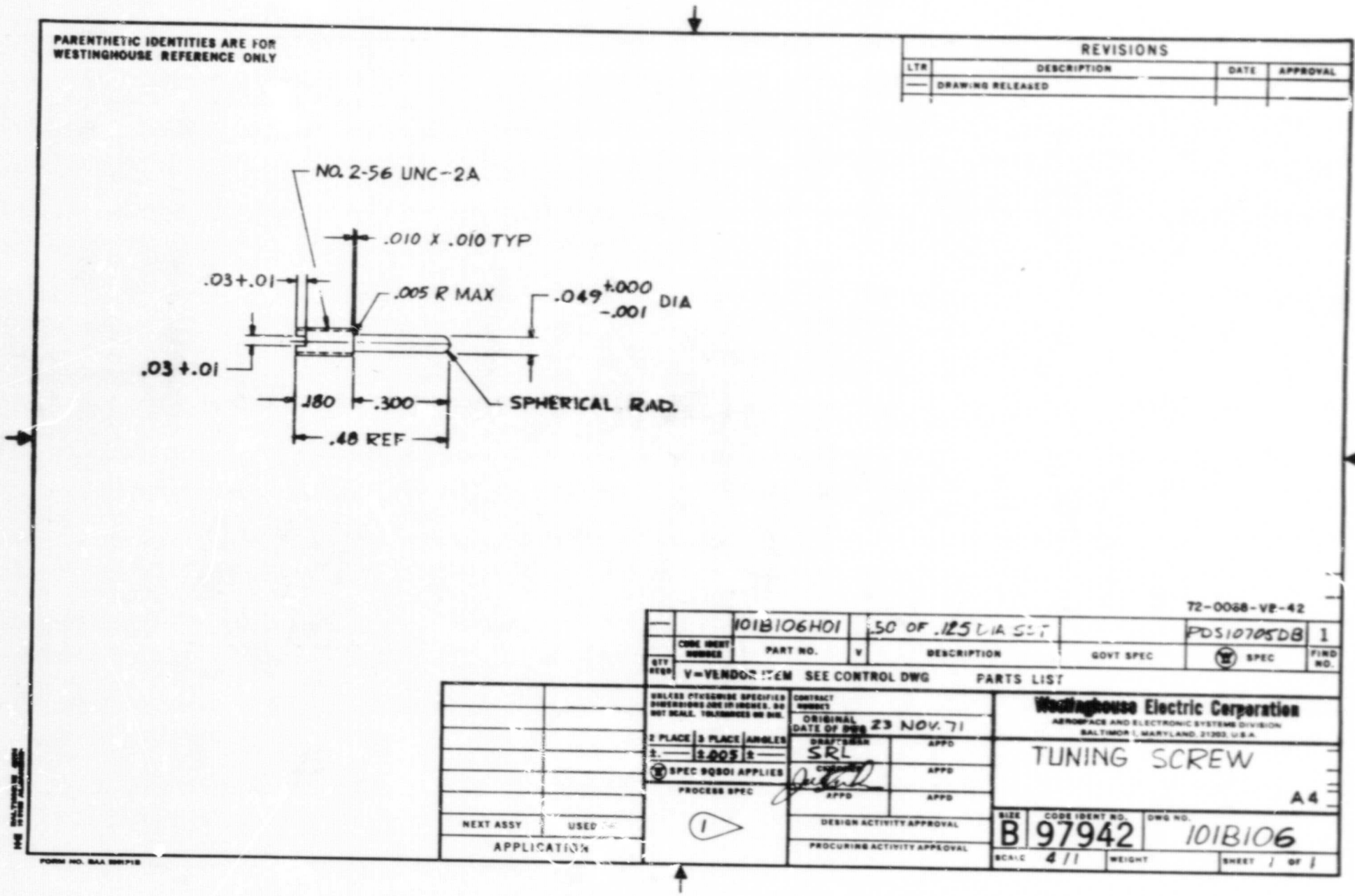
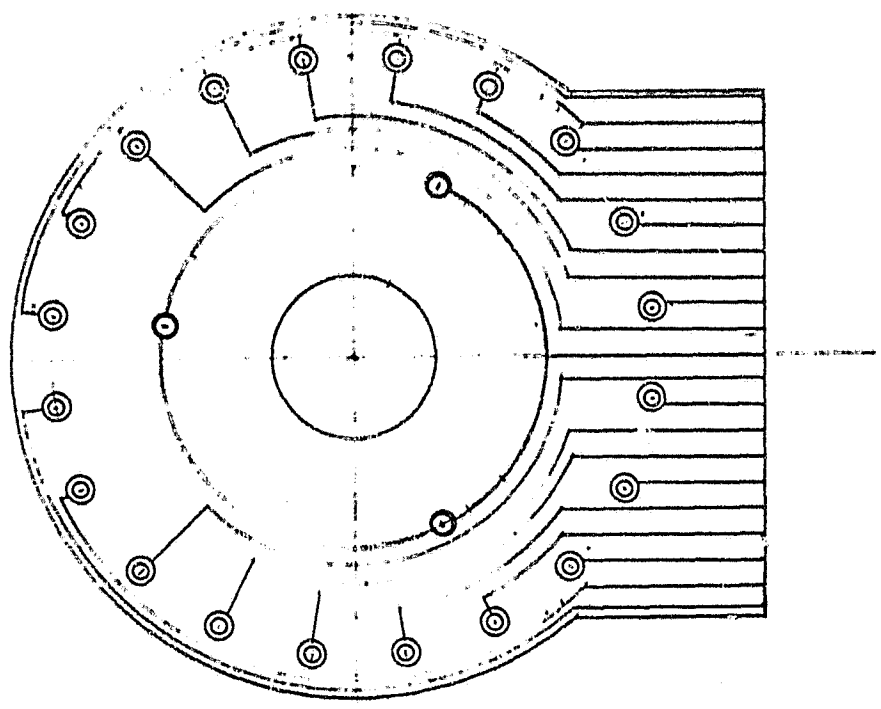


Figure 39. Tuning Screw



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Bias Distribution Printed Circuit Board
Layout Schematic
Figure 3.8.10

Figure 40. Bias Distribution Printed Circuit Board Layout Schematic

2.9 POWER SUPPLY

The power supply chosen will be developed in-house. It has built-in diode open/short turn-off means to identify failed diodes, and individual trim capability for each diode plug. The maximum voltage and current values allow for a variety of diode dc characteristics, with the side condition that the total dc power delivered to the diodes be within the 250-watt limit.

The power supply for this application will be a 60-Vdc, 5-A, current regulated unit to operate from 110 to 120 volts, single phase, 60 Hz and with the following added features.

a. The load will consist of 20 diodes operated in the avalanche mode. The breakdown voltage is about 35 volts.

b. The supply will automatically regulate the total current and can be adjusted to any value between about 0.2 to 5.0 amperes.

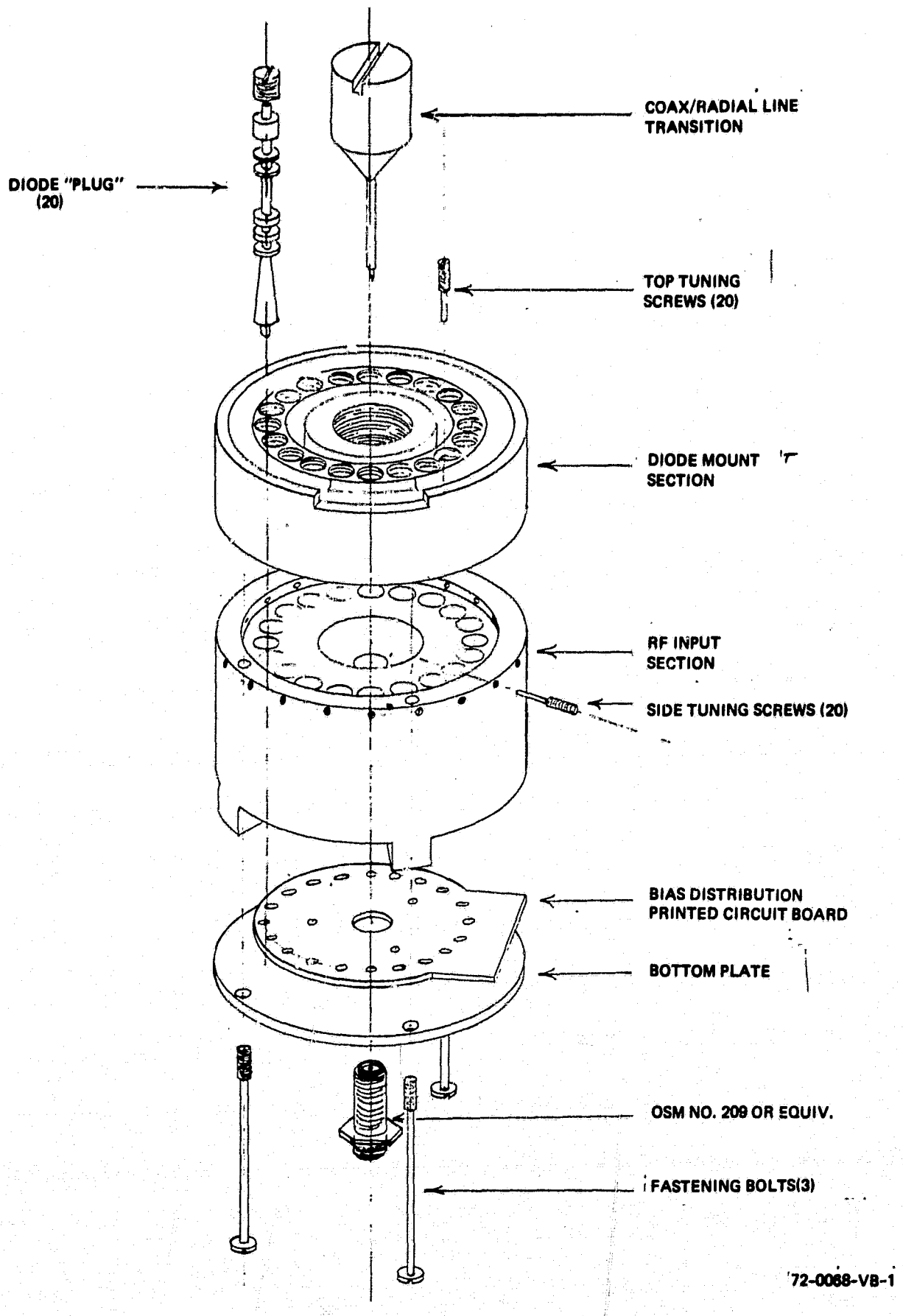

Figure 41. Assembly of Solid-State K_u-Band Power Amplifier

c. Fine current adjustment can be made on each individual diode load. The normal operating current per diode is up to 200 mA.

d. Current regulation against changes in supply line voltage, temperature and load impedance will be no greater than 1 percent.

e. The ripple component will not exceed 1 percent rms of the dc current.

f. The power supply will be turned off rapidly in the event that any one or more of the loads become either opened or shorted. The power will remain off until the reset button is pushed or the input supply turned off.

g. The unit cannot be turned on unless the current adjustment has first been turned to the minimum current position.

h. The current in each IMPATT diode can be individually measured.

i. In the event of a failed IMPATT diode, the monitoring system provides a simple means of identifying the damaged component and determining whether the failure was an open or a short.

Figure 42 shows a schematic diagram of the power supply with the above control features.

The following is a description of the functions of the circuit shown in the figure.

a. Raw dc Supply

Transformer: T1

Rectifier: CR-1

Filter: L^1, C1, and R59

b. Current Regulation and Adjustment

Sensing Resistors: R7 and R8

Comparator-Amplifier: Q4, Q5, and CR-65

c. Series Control Section

Q1, Q2, CR-5, R3 and auxiliary power supply No. 1

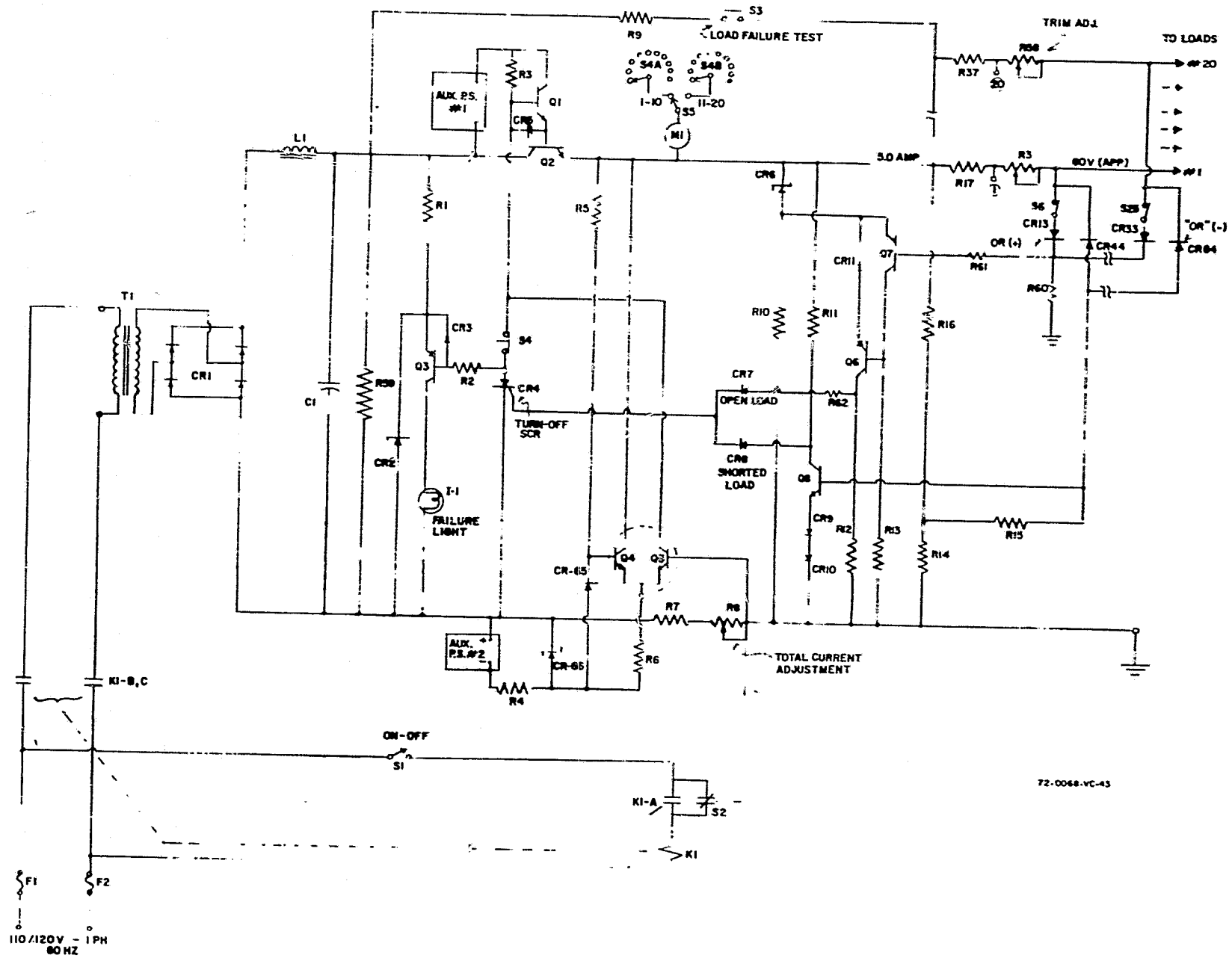

Figure 42. Power Supply Schematic

d. Fault Shutdown

A short or open in any one of the 20 amplifier diodes will shut down the power. When a shutdown signal is received the following components are involved. SCR, CR4 fires, grounding the base of Q1.

Fault Reset: S4

Fault Indication: R1, R2, CR2, CR3, Q3, I-1.

e. Open Load Sensing

A (+) "OR" gate consisting of 20 signal diodes CR13 to CR33 will transmit the high voltage (approximately 50 V) appearing across the open diode to the base of transistor Q7. This will apply a shutdown signal to CR4 using: Q7, Q6, CR6, CR7, R10, R12, and R13.

f. Shorted Load Sensing

A shorted IMPATT diode will transmit low voltage (near zero) to the base of Q8. This is done through the (-) "OR" gate made up of switching diodes CR44 to CR64, R14, R15, and R16. The low voltage is applied to the base of Q8 which then delivers a trigger signal to SCR CR4 through CR8, shutting down the power supply.

g. Short circuit protection is provided by fuses F1 and F2.

h. Fine Current Adjustment

Fine adjustments can be made in each IMPATT diode by means of potentiometers R38 to R58.

i. Current Meters

Individual diode current can be measured by voltmeter M1 which is connected across voltage dropping resistors R17 to R37. Selection of the particular diode is made by the 20 point tap switch S4.

j. Fault Isolation

To determine which particular diode has failed, switch S3 is closed. This passes a small current into the IMPATT diodes, bypassing transistor Q2 which is blocked because of the fault. The current is limited to a safe value by R9.

With S3 closed, the selector switch is rotated, noting the reading of M1 at each position. When the contact of S4 is connected to the defective load diode a change in reading will be noted. If the voltage reading is zero the diode has failed open, and if the current is higher than that for the other positions, the diode has failed short.

k. Reduced Current Starting

Normal on-off control is obtained by switch S1. Master relay K1 is electrically interlocked with the position of the control knob of R8. Interlock contact S2 is closed only when R8 is set for minimum current regulation (maximum resistance).

Thus, if power is turned off it can only be reapplied when the current control knob of R8 is set for minimum current.

l. Graceful Failure

Tests can be run with one or more failed IMPATT diodes by bypassing the fault sensing logic by switches S6.

The power supply will be mounted in a cabinet of dimensions: 19 inches wide by 5-1/2 inches high by 17 inches deep. Weight is approximately 60 pounds. A forced-air self-contained blower will be mounted inside the power supply.

3. PHASE II PROGRAM PLAN

Phase II of this program, which consists of the development, fabrication, testing, and delivery of two solid state K_u-band power amplifiers, will commence upon receipt of approval from the NASA Contract Officer.

The first steps during Phase II will be to further test and characterize commercially available IMPATT diodes, make a decision on the diode package desired and order the required diodes. Replaceable diode plugs containing harmonic reflection filters will be fabricated and tested in order to resolve the principal uncertainty, i.e. the amount of intermodulation product suppression which can be achieved.

Concurrent with the above the brassboard resonator will be developed and the power supply will be fabricated and tested.

Following the above steps a brassboard amplifier will be assembled and tested and modified as deemed necessary. Final resonator development will then proceed followed by assembly and testing of the final amplifiers. The equipment development will culminate in the amplifier acceptance tests to be performed at the Advanced Technology Laboratories of Westinghouse and the delivery of two amplifiers and a power supply.

A milestone schedule of development events is shown in figure 43. Also shown on this schedule are the delivery of final drawings, parts lists, and test procedures (draft and final).

Milestone Schedule of Development Events

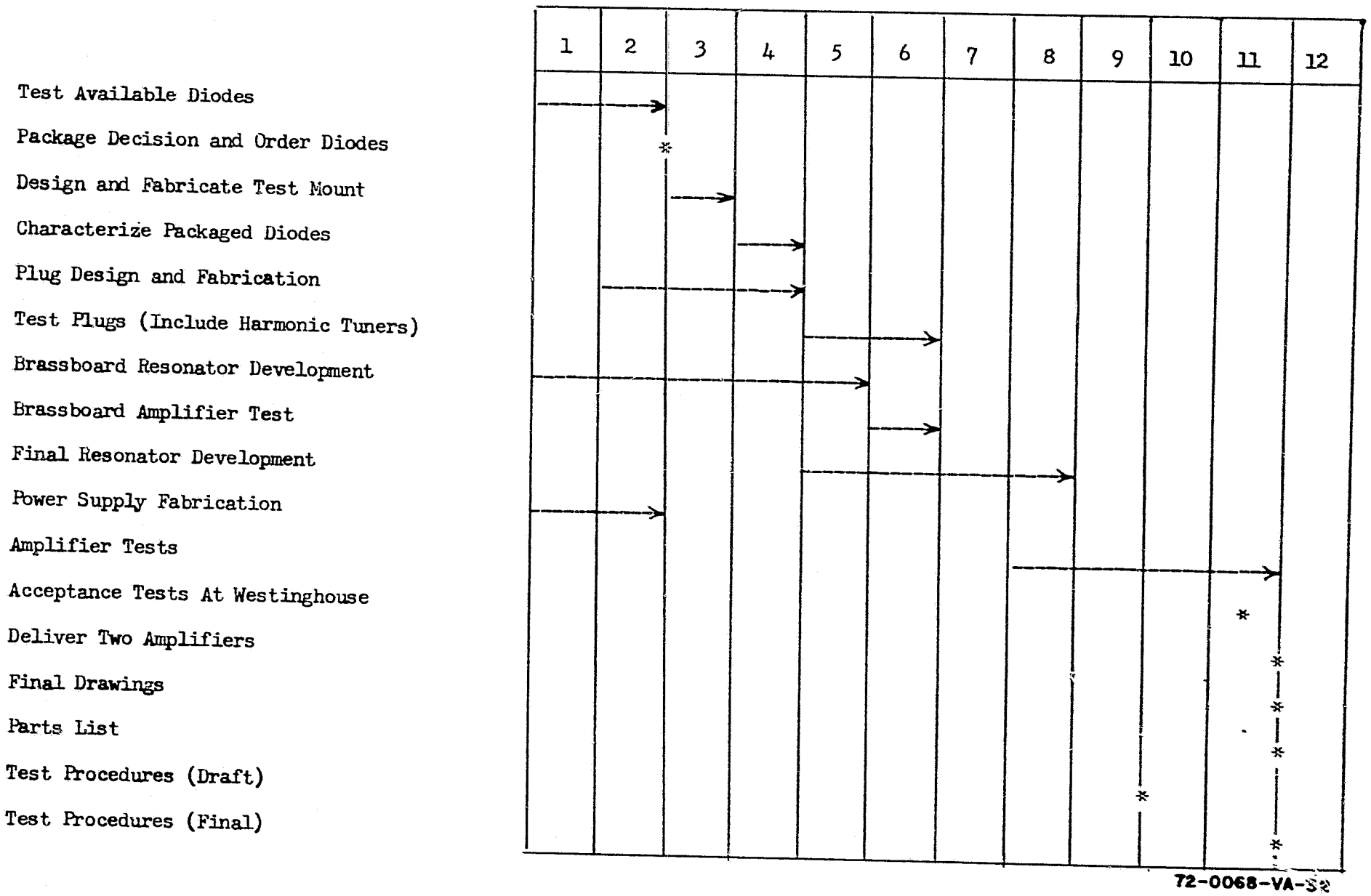

Figure 43. Master Schedule of Development Events

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