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TECHNOLOGY UTILIZATION

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ELECTRONIC CIRCUITS FOR COMMUNICATIONS SYSTEMS

A COMPILATION



NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Foreword

The National Aeronautics and Space Administration and Atomic Energy Commission have established a Technology Utilization Program for the rapid dissemination of information on technological developments which have potential utility outside the aerospace and nuclear communities. By encouraging multiple application of the results of their research and development, NASA and AEC earn for the public an increased return on the investment in aerospace research and development programs.

The compilation of electronic circuits for communications systems has been divided into thirteen basic categories, each representing a unique area of circuit design and application. The circuits and modular subassemblies are only samples of many similar items that are available through the TU program. The enormous volume of information available in this fertile area is indicative of the important role that communications technology has played in the aerospace program.

In general, the compilation items are moderately complex and as such, would appeal to the applications engineer. However, the rationale for the selection criteria was tailored so that the circuits would reflect fundamental design principles and applications, with an additional requirement for simplicity whenever possible.

Additional technical information on individual devices and techniques can be requested by circling the appropriate number on the Reader Service Card included in this compilation.

Unless otherwise stated, NASA and AEC contemplate no patent action on the technology described.

We appreciate comment by readers and welcome hearing about the relevance and utility of the information in this compilation.

> Jeffrey T. Hamilton, Director Technology Utilization Office National Aeronautics and Space Administration

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Contents

SECTION 1. Modulation Techniques	Pa	age
Double-Emitter, Suppressed-Carrier Modulator		
Remodulator Filter		
Ferrite Antenna Modulator		
SECTION 2. Frequency Control		-
Frequency Converter with High Signal-to-Noise Ratio		3
Frequency Multiplier for Remote Operation		4
Varactor Frequency Divider		
Frequency Doubler with Negligible Distortion		5
SECTION 3. FM Design Consideration's Circuit Reduces Distortion of FM Modulator		6
Frequency Offset in Linear FM/CW Transponder		6
Eliminates Clutter		
Optimum FM Preemphasis: A Concept		7
SECTION 4. Filters		
A Self-Tuning Filter		8
in Microwave Applications		9
Tunable Bandpass Filter with Variable Selectivity	• • • •	9
SECTION 5. Phase Detectors		
Continuously Variable, Voltage-Controlled Phase Shifter		
Phase Detector Synthesizes Own Reference Signal Phase Detector Has High Efficiency in Presence of Noise		
SECTION 6. Gain and Frequency Control	••••	
Wide-Range Automatic Gain Control Circuit		12
Simple, Accurate Automatic Frequency Control Circuit		
Gain Control Limiter Circuit	• • • •	14
SECTION 7. RF Oscillators		
Low-Power, Compact, Voltage-Controlled Oscillator Automatic Frequency Control of Voltage-Controlled	• • • •	14
Oscillators		15
A 225 MHz FM Oscillator with Response to 10 MHz		
Voltage-Controlled Oscillator	••••	16
SECTION 8. RF Amplifiers Variable Gain Amplifier		17
Low-Noise, Wide-Bandwidth 1.F. Preamplifier		
Complementary Pair Broadband Transistor Amplifier		
Gain and Phase-Tracking Amplifier		20
SECTION 9. RF Measurement Techniques		
Dynamic Linearity Measurement Technique	••••	20
of RF Power Sources		21

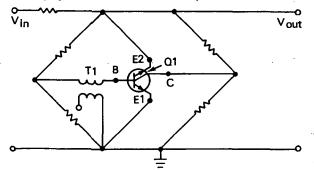
Linear Signal-Noise Summer Accurately Determines Page and Controls S/N Ratio	
SECTION 10. Personal Communications Systems Self-Contained Miniature Electronics Transceiver Provides Voice Communication in Hazardous Environment 22 Personal Communications Assembly	
SECTION 11. Phase-Locked Loop Techniques High Noise Immunity, Wideband Bi-Phase Modulation Scheme	
SECTION 12. Video Circuits for TV Applications Variable Word-Length Encoder Reduces TV Bandwidth Requirements	
SECTION 13. Mixers Added Diodes Increases Output of Balanced Mixer Circuit 29 Compact Microwave Mixer Has High Conversion Efficiency 29 Signal Mixer Provides Outputs with Matched Impedance Characteristics	

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Section 1. Modulation Techniques

DOUBLE-EMITTER, SUPPRESSED-CARRIER MODULATOR

This suppressed carrier modulator develops a signal-to-carrier output ratio of 40 dB or greater with a signal input of 2.5 V peak-to-peak. No tuning potentiometers are required within the



frequency range from 450 to 520 kHz, and all sideband harmonics are less than the carrier output amplitude. A double-emitter, chopper transistor, Q1, achieves the required carrier suppression by reducing the carrier output from a modulator; this reduction takes place in the bridge circuit which balances the effects of the carrier current as it switches the double-emitter transistor from cutoff to saturation. Voltages developed by the circuit are balanced, with respect to the load impedance and ground, by tying the collector of Q1 and the base-transformer combination to separate resistor bridges. The voltage developed across the emitter E1 to the base junction B is equal and opposite to the voltage developed across emitter E2 to the base junction. Therefore, the sum of the emitter voltages is approximately zero with respect to the load impedance. Any stray capacitance between the collector and either emitter, or the base and either emitter, is also nulled in the balanced RC bridge network.

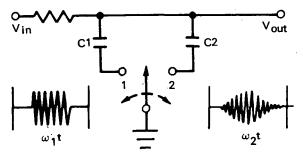
> Source: C.F. Haist and A. Piscopo of IBM Corp. under contract to Marshall Space Flight Center (MFS-12494)

Circle 1 on Reader Service Card

REMODULATOR FILTER

Three simultaneous functions —demodulation, filtering, and modulation — are performed in a single functional remodulator circuit which eliminates spurious signal components at the output. The advantages are extreme simplicity, freedom from mismatch problems, and the ability to use polarized capacitors which tend to be smaller for the larger capacitance values used in other circuits of this type.

The operation of the circuit is as follows: with the switch in position 1, a small positive voltage builds up on C1 during the positive half of the input cycle, $\omega_1 t$, and appears at the output. During the next half cycle with the switch in position 2 and with a switching rate of $\omega_2 t$, C2 acquires a negative charge which also ap-



pears at the output. On succeeding half cycles, charges accumulate on the capacitors and the output rises accordingly. If $\omega_1 t$ and $\omega_2 t$ are synchronous and in-phase, the envelope amplitude of the resulting output signal exponentially reaches the steady state amplitude of the input signal. Upon removal of the input signal,

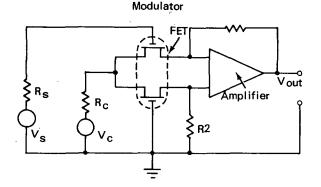
the discharge of the capacitors produces an exponential envelope decay, mirroring the input buildup pattern. From the waveforms shown in the figure, it can be seen that the input signal, when processed through a remodulator, will appear at the output without spurious signal components when ω_1 t is synchronous and in phase with ω_2 t.

Source: H. C. Vivian of Caltech/JPL under contract to NASA Pasadena Office (NPO-10198)

Circle 2 on Reader Service Card

RESISTANCE-CONTROLLED LINEAR PRODUCT MODULATOR

A product modulator with a suppressed carrier (see fig.) consists of a linear amplitude modulator that requires only an operational amplifier and a pair of field-effect transistors



(FET's). No inductors or transformers are required. Amplitude modulation is produced by varying the impedance of the FET's, which, in effect, control the closed-loop gain of the amplifier. The carrier signal V_c is suppressed by utilizing the common-mode rejection capabilities of the amplifier. Therefore, a very close approximation to a true product modulator is obtained when only the sum and difference frequencies of the two input frequencies V_s and V_c appear at the output. Also, by adjusting the amount of common-mode rejection, various degrees of carrier signal rejections are possible. The product modulator may be used in such applications as linear frequency translation, modulation and demodulation techniques such as single sideband AM, double sideband AM, with or without suppressed carrier, quadrature modulation and demodulation, and analog computation techniques.

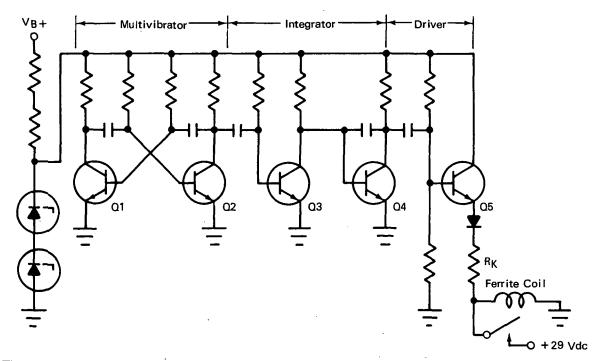
Linear product modulation is equivalent to linear amplitude modulation with a suppressed carrier signal. Since the amount of commonmode rejection is adjustable, amplitude modulation can be obtained with either full-carrier amplitude, reduced carrier, or suppressed carrier. With suppressed carrier, the modulator also functions as an excellent frequency translator in which a range of frequencies is shifted to another frequency band.

> Source: H. Brey and S. Gussow of Sperry Rand Corp. under contract to Marshall Space Flight Center (MFS-14391)

Circle 3 on Reader Service Card

FERRITE ANTENNA MODULATOR

A multiple antenna system located onboard an aircraft eliminates interference zones which reduce the signal strength at the ground receiving station during critical flight periods of takeoff and landing. The interference zones are reduced by inserting a ferrite attenuator into the appropriate antenna waveguide and modulating the ferrite attenuator to change the antenna gain at the receive frequency. This permits ground tracking until the antenna is no longer required, at which time a fixed attenuation quantity is inserted into the waveguide.



The modulator schematic shown in the figure is composed of three sections: (1) a multivibrator, (2) an integrator, and (3) a driver for the ferrite coil. The multivibrator is a free running circuit that establishes the frequency of the modulation wave. Q3 is a switch in the Miller integrator and is controlled by the multivibrator output. The charging and discharging of the capacitor between the base and collector of Q4 determines the final output waveshape. The emitter follower, Q5, drives the ferrite coil. A blocking diode added to the emitter circuit prevents feedback from the 29 Vdc applied to the ferrite coil. R_k , inserted in the emitter of Q5, determines the amount of attenuation required.

Source: S.G. Larson, F.H. Shorkley, J.C. Hooks, and B.T. Williams of Western Electric Company, Inc. under contract to NASA Pasadena Office (NPO-12011)

Circle 4 on Reader Service Card

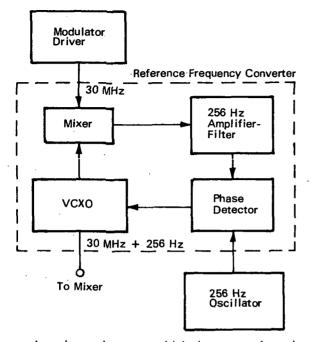
Section 2. Frequency Control

FREQUENCY CONVERTER WITH HIGH SIGNAL-TO-NOISE RATIO

A novel frequency converter with two highly stable reference signals makes use of a very simple phase detector circuit to eliminate the need for the complex and expensive amplification and filter stages required in conventional frequency converters.

The reference frequency converter (see fig.) is basically a conventional phase-lock loop configuration, except that a voltage-controlled crystal oscillator (VCXO) replaces the more conventional voltage-controlled oscillator (VCO). A VCXO is required to select the upper sideband (30 MHz + 256 Hz) and to reject the lower sideband (30 MHz - 256 Hz). For this purpose, the frequency stability of the VCXO must be within $\pm 0.0008\%$.

The 256 Hz output of the mixer is amplified, filtered by an active low-pass filter, and applied



to the phase detector which is a sample-andhold circuit. The sampling signal is a narrow pulse produced by a pulse generator from the 256 Hz reference signal furnished by a stable oscillator. Each pulse turns on an FET in the phase detector. For this condition, the phase detector output voltages assumes the value of the instantaneous input voltage. During the "off" stage, the holding capacitor discharges very slowly, thus maintaining the "holding" level between sampling pulses. If the fixed interval between sampling pulses coincides with the period of the sine wave input to the phase detector, the input wave is sampled at the same level each time, and the output level of the phase detector does not change. If this is not the case, an error voltage appears at the phase detector output. This error voltage is applied to the control input of the VCXO, causing the necessary correction which brings the input of the phase detector into phase coincidence with the 256 Hz sampling pulse train. The signals are now phase-locked, and the output frequency is the sum of the two input reference frequencies.

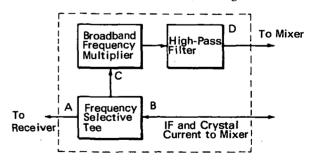
> Source: G.B. Shelton of Sperry Rand Corp. under contract to Marshall Space Flight Center (MFS-14526)

Circle 5 on Reader Service Card

FREQUENCY MULTIPLIER FOR REMOTE OPERATION

An oscillator frequency multiplier can be adapted to harmonic mixer-receiver systems in which the mixer is located remotely from the receiver. The remote oscillator frequency multiplier provides an increase in the sensitivity of remote operated harmonic mixers and an operating capability over a wider frequency range. The mixer is normally connected to the receiver by means of a single coaxial cable, which conducts the local oscillator signal from the receiver to the mixer, and the intermediate frequency and crystal current from the mixer to the receiver.

When the remote oscillator frequency multiplier is used, the local oscillator frequency is multiplied by a factor N, and the sensitivity of the mixer is improved because of the reduction of the harmonic mixing number. Also, the harmonic mixing number is reduced by multiplying and filtering the local oscillator signal prior to introducing this signal to the mixer diode. This process results in reduced mixer conversion loss. The remote oscillator frequency multiplier is connected at "A" and fed through the fre-

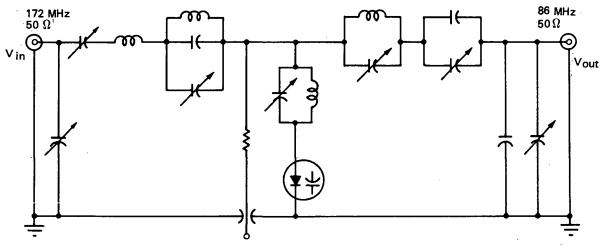


quency selective tee to a broadband frequency multiplier. The frequency selective tee isolates the B port from the local oscillator signal. The output of the broadband frequency multiplier is filtered to remove the fundamental local oscillator signal and undesired harmonics; the multiplied local oscillator signal is available at port D for connection to the local oscillator input port of a three-port mixer.

The intermediate frequency and crystal current port of the three-port mixer is connected to port. B of the remote local oscillator frequency multiplier and these signals are coupled through the frequency selective tee to port A of the remote local oscillator frequency multiplier. The frequency selective tee isolates the 1F signal and crystal current from the broadband frequency multiplier input C.

Source: C.W. Currie and W.H. Graham of Scientific-Atlanta, Inc. under contract to Marshall Space Flight Center (MFS-13291)

No further documentation is available.



VARACTOR FREQUENCY DIVIDER

The varactor frequency divider shown in the schematic is designed to accept an input frequency of 172 MHz and to provide an output frequency of 86 MHz, with input and output impedances of 50 Ω . The varactor has a cutoff frequency of 22 GHz (well above the output frequency) and an output power of 1.5 W. Both the input and output circuits of the divider use an "L" section matching network. This inductance, together with the variable capacitor, the quiescent point capacitance, and the reactance of the tank circuits, forms a low-Q series resonant circuit at 172 MHz in the input and

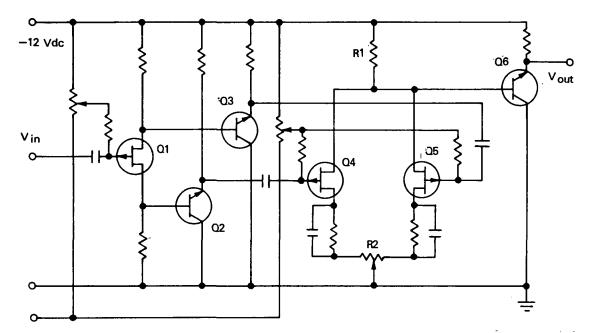
at 86 MHz in the output circuit. The divider has a 3 dB bandwidth of 7 MHz and contains a very small harmonic content in the output. The varactor frequency divider offers a relatively simple method of dividing frequencies with passive elements.

> Source: L.L. Vorel and M.A. Honnell of Auburn University under contract to Marshall Space Flight Center (MFS-14345)

Circle 6 on Reader Service Card

FREQUENCY DOUBLER WITH NEGLIBLE DISTORTION

Frequency multiplication is achieved by a new control circuit that locks a higher frequency to a lower one. The input signal (see fig.) is applied to the first stage Q1, a phase divider with two outputs equal in magnitude but phase shifted π rad (180°). These outputs are applied to the bases of emitter-followers Q2 and Q3 which serve as sine wave shapers for driving the fre-



quency doubling stage Q4 and Q5. If Q4 and Q5 are matched, the fundamental frequency of the input signals will cancel in the common drain resistor R1, and the second harmonics will be added. R2 is used to make fine adjustments for matching Q4 and Q5. Q6 is an emitter-follower output stage that provides a low output impedance. No filter circuits are necessary, and the output waveform is sinusoidal with neglible harmonic distortion within

the frequency range from 10 kHz to 10 MHz. Several of these doublers can be used in cascade if multiplication factors greater than 2 are required.

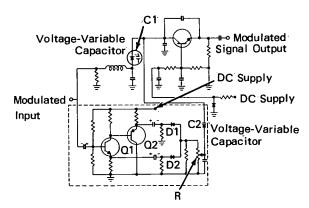
> Source: W.K. Wong of Lockheed Electronics Co. under contract to Manned Spacecraft Center (MSC-13118)

No further documentation is available.

Section 3. FM Design Considerations

CIRCUIT REDUCES DISTORTION OF FM MODULATOR

This correction circuit reduces second harmonic and intermodulation distortion of a voltage-variable capacitor which modulates the oscillator. As shown in the schematic, the modulating input signal is phase-inverted and amplified by Q1 and Q2. The amplified signal is then applied to the full-wave rectifier diodes D1 and D2 which generate the second harmonic without introducing the fundamental frequency component into the correction circuit. The output from the rectifier-squaring network, applied to the potentiometer R, provides a correction sig-



nal to the voltage-variable capacitor C2 across the tuned circuit of the oscillator. The correction signal has the proper polarity to reduce total tank circuit capacitance on both the positive and the negative peak swings of the modulating input signal.

Other applications for this correction circuit might include its use in the master oscillator of

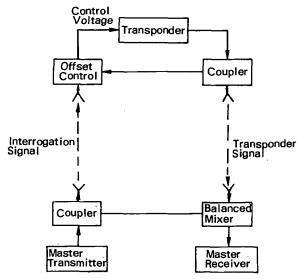
a radio transmitter or in a subcarrier oscillator of a telemetry system.

Source: Radio Corp. of America under contract to Goddard Space Flight Center (GSC-00257)

Circle 7 on Reader Service Card

FREQUENCY OFFSET IN LINEAR FM/CW TRANSPONDER ELIMINATES CLUTTER

Undesirable false echoes or reflections (clutter) of the signal used to interrogate a linear FM/CW transponder located on airborne ve-



hicles are eliminated by a technique which offsets the frequency of the transponder signal with respect to the interrogation signal.

As shown in the illustration, the interrogation signal from the master transmitter is radiated through a coupler to the airborne transponder. The transponder receives this signal

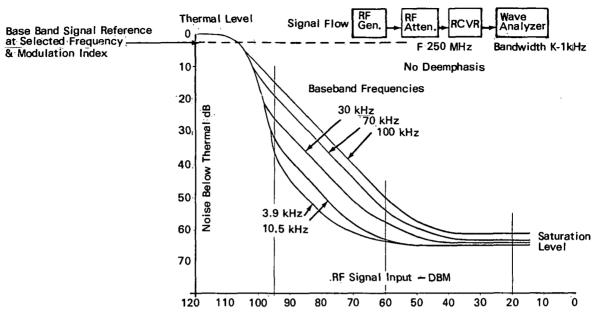
through an offset control which generates a control voltage by comparing the frequency of the interrogation signal to that of the transponder signal. This control voltage changes the frequency of the transponder signal so that it remains constantly offset from the frequency of the interrogation signal. At the master receiver, a portion of the interrogation signal is coupled to a balanced mixer. The transponder signal received by the master receiver is beat against the interrogation signal. The beat signal frequency is proportional to transponder range, provided the system is using an FM/CW altimeter. Without frequency offset, the frequency of the best signal in the master receiver is also a function of transponder time delay. Because of this, signals reflected from false targets whose time delays are equal to that of the desired signals will be indistinguishable from the desired signals. These undesirable signals are eliminated by offsetting the transponder frequency.

> Source: Melpar, Inc. under contract to Marshall Space Flight Center (MFS-00249)

Circle 810n Reader Service Card

OPTIMUM FM PREEMPHASIS: A CONCEPT

The spectral noise characteristics in the baseband of a receiver (without deemphasis) has been measured as a tunction of rf input power. Experimental measurements of output noise vs rf input power for the specific baseband center frequency are shown in the figure. A calibrated rf signal generator and precision rf attenuator are connected to a wave analyzer (tunable volt-



meter). The wave analyzer measures the noise in a small-frequency slot, centered at a specified baseband frequency. The rf generator and fm receiver are set to the operating carrier frequency and the wave analyzer is then tuned to a frequency near the low end of the baseband frequency spectrum. As the rf signal generator output power is varied in discrete increments over the dynamic range of the fm receiver, the wave analyzer measures the noise in the selected baseband frequency slot for each discrete increment of rf input power.

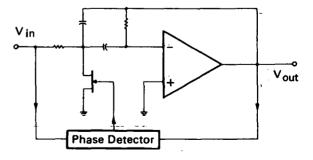
> Source: K.W. Merz of The Boeing Company under contract to Kennedy Space Center (KSC-10151)

Circle⁹ on Reader Service Card

Section 4. Filters

A SELF-TUNING FILTER

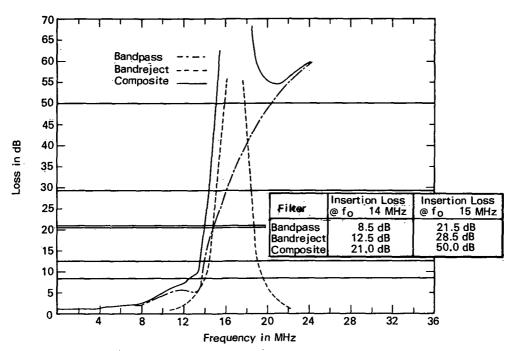
A self-tuning filter covers the range from 2 kHz to 20 kHz, while maintaining constant bandwidth and center frequency gain. The capability of automatically adjusting center frequency to track the signal frequency permits the use of a filter with a bandwidth considerably smaller than the range of input signal frequencies. The resistance-capacitance bandpass filter employed in this design has a center frequency that can be varied by means of a single resistive element. An FET is used in place of an ordinary resistor to control the voltage of the tuning element. The control voltage is derived from a phase detector which compares the phase of



the filter input and output. If phase relationship between input and output is π rad (180°), the filter is tuned to the input frequency, if less than π rad, a correcting voltage is applied to the FET until the phase is π rad, at which time the filter is again in tune. A reference frequency is not required as in ordinary lock-in amplifier filters, and there is no phase change as the signal frequency varies. Source: G.J. Deboo and R.C. Hedlund Ames Research Center (ARC-10264)

Circle 10:on Reader Service Card

COMPOSITE FILTER STEEPENS REJECTION SLOPES IN MICROWAVE APPLICATIONS



A composite filter, consisting of a bandpass filter that shapes the passband and band-reject filters on each edge of the bandpass, steepens the rejection slopes. The use of high, unloaded Q-filters prevents bandpass and band-reject filter interaction that could result in spurious transmissions. The bandpass filter (see fig.) exhibits insertion losses at $f_0 + 14$ MHz and $f_0 + 15$ MHz. The band-reject filter (tuned at $f_0 + 16.75$ MHz) exhibits sharper insertion losses at $f_0 + 14$ MHz and $f_0 + 15$ MHz and $f_0 + 15$ MHz, while the composite filter insertion loss is the algebraic sum of the bandpass and band-reject losses. A typical Butterworth design would require 40 resonant cavities with unloaded Q's of 47,000, unattainable in standard waveguide designs. The composite design contains only 27 cavities with unloaded Q values on the order of 8,000.

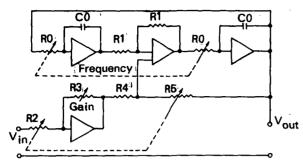
> Source: Dorne and Margolin, Inc. under contract to Goddard Space Flight Center (GSC-00480)

No further documentation is available.

TUNABLE BANDPASS FILTER WITH VARIABLE SELECTIVITY

This stable, RC bandpass filter maintains a continuously noninteracting control of the center

frequency, the center-frequency gain, and the circuit Q. The basic RC network is constructed



from stages that achieve second-order transfer functions using two integrators. The ready availability of integrated circuits makes this method attractive for general purpose tunable filters.

The highly stable RC bandpass filter has separate controls that independently adjust

center frequency, center frequency gain, and Q. The center frequency is controlled by the ganged variable resistors R0 and the selectivity is controlled by R5. The gain at center frequency is proportional to the value of R3 because the ratio R5/R2 is kept constant by ganging R5 and R2; the Q and gain controls are also linear. This technique should be particularly useful in processing low-frequency bioelectronic signals where the center frequency may vary with time.

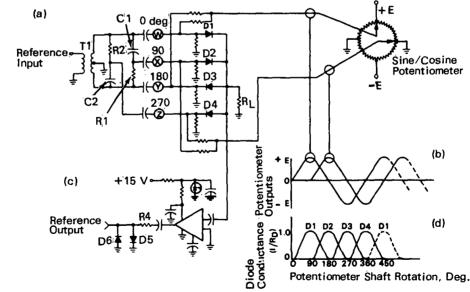
> Source: W.J. Kerwin and C.V. Shaffer Ames Research Center (ARC-10191)

Circle: I I on Reader Service Card

Section 5. Phase Detectors

CONTINUOUSLY VARIABLE, VOLTAGE-CONTROLLED PHASE SHIFTER

This phase shifter circuit adjusts the phase relationship between a locally-generated reference frequency and a received rf signal applied to a phase-coherent detector. The phase shifter checkout equipment. Important features include: (1) continuously variable dc-voltage control through 2π rad (360°); (2) rf circuit volume small enough to combine with a phase detector,



is small enough to be integrated into a receiver subassembly such as a phase detector module, and can be operated either manually or by command from remote control panels of automatic

thereby eliminating the phase shifter subassembly; (3) phase stability within $\pm \pi/18$ rad ($\pm 10^{\circ}$) over the range of 273 to 322 K; and (4) applicability to any reference input frequency from

100 kHz to 10 MHz. The dc voltage applied to diodes D1, D2, D3, and D4, (see fig.) is supplied from the armatures of the sine/cosine potentiometer. As the potentiometer shaft is rotated through 2π rad, the conductance of each diode varies sequentially (see section d of fig.).

Reference signals, applied to the diodes at terminals W, X, Y, and Z, are vectorially summed across the load resistor R_L . As the potentiometer shaft is rotated from 0 to $\pi/2$ rad (0° to 90°), D1 goes from zero to full conduction, and the signal appearing across R_L is that which is applied to terminal W (0 rad). Shaft rotation from $\pi/2$ to π rad (90° to 180°) turns D1 off and D2 on. As this occurs, the effective resistance of D1 increases and that of D2 decreases.

For shaft rotation from $\pi/2$ to π rad the re-

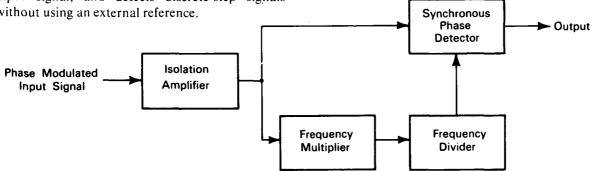
sultant signal across R_L varies in phase from 0 to $\pi/2$ rad. For a shaft rotation from π to $3\pi/2$ rad (180° to 270°), the same action takes place between D2 and D3, and the signal across R_L changes phase from $\pi/2$ to π rad. Between $3\pi/2$ to 2π rad (270° to 360°), the shift is repeated between D3 and D4. From 2π to $\pi/2$ rad (360° to 90°), it occurs between D4 and D1. Since the potentiometer has no stops, the reference signal phase can repeatedly be varied through 2π rad.

> Source: C.E. Johns of Caltech/JPL under contract to NASA Pasadena Office (NPO-11129)

Circle 12 on Reader Service Card

PHASE DETECTOR SYNTHESIZES OWN REFERENCE SIGNAL

A phase detection circuit synthesizes its own phase reference signal from the phase-modulated input signal, and detects discrete-step signals without using an external reference. The output of the frequency multiplier is applied to the frequency divider where, after divi-



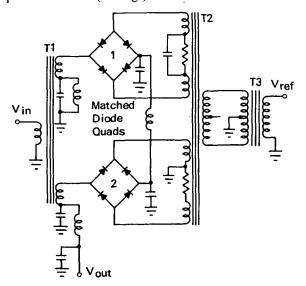
The phase modulated input signal is applied to an isolation amplifier whose output is connected to both the frequency multiplier and the synchronous detector. The frequency multiplier uses the signal from the isolation amplifier as a control timing signal to generate an output at N times the input frequency. The multiplication factor, N, for a particular system is determined from the expression $N = 2\pi/\Delta\phi$, where $\Delta\phi$ is the phase change per step, in radians. A frequency multiplier is used because phase changes in the input signal do not appear in the multiplier output. sion by N, a constant-phase signal is generated as the reference signal in the synchronous detector. The synchronous detector compares the phases of the original signal from the isolation amplifier and synthesized reference signal. The output of the detector is a dc voltage, the polarity of which changes each time the input signal changes phase.

> Source: Fairchild Stratos Corp. under contract to Marshall Space Flight Center (MFS-00247)

Circle 13 on Reader Service Card

PHASE DETECTOR HAS HIGH EFFICIENCY IN PRESENCE OF NOISE

A phase detector circuit operating at 10 MHz is capable of maintaining a balance 40 dB below signal in the presence of 30 dB noise. The phase detector (see fig.) consists of two matched-



diode quads driven in opposite phase by the reference signal. The secondaries of T2, driving the quads, are separated to reduce the interaction. An RC current-limiting circuit inserted between the two parts at rf zero eliminates the effects of stray capacitance to ground. T3 es-

tablishes the ground reference at the midpoint of the primary so that the ends of the primary winding are equally off ground in the opposite rf phase. Thus, capacitance from primary to secondary in T2 will not upset the secondary balance. Each transformer is wound with twisted trifilar wire to ensure that all windings are as similar as possible. Since the quads are turned on out of phase, they rectify opposite half-waves of the signal to give full-wave detection. This action results in signal distortion cancellation which keeps the output balanced at zero in the presence of large, random noise when the signal source has even-harmonic distortion. The two quad outputs are added in series to provide voltage doubling, and since the averaging of random noise is just as efficient with a series arrangement as with a parallel, a 6 dB improvement in dynamic range is attained. The dynamic range (ratio of maximum linear output to unavoidable drift) without adjustment is nearly 80 dB, at a frequency of 10 MHz.

> Source: General Dynamics Corp. under contract to Goddard Space Flight Center (GSC-10753)

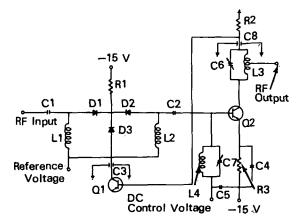
No further documentation is available

Section 6. Gain and Frequency Control

WIDE-RANGE AUTOMATIC GAIN CONTROL CIRCUIT

Radio receivers must use some form of automatic gain control (AGC) to prevent overloading of the final output stage. This AGC circuit (see fig.) is capable of handling input signals of 1 V rms and can maintain a relatively constant output by attenuating the input signal.

The input signal is coupled through Cl to the variable attenuator made up of diode tee-pad network D1, D2, and D3. The attenuator is prebiased in the low-attenuation condition by a reference voltage coupled through rf chokes L1 and L2. The attenuator control elements are R1, C3, and Q1. Output of the attenuator is coupled

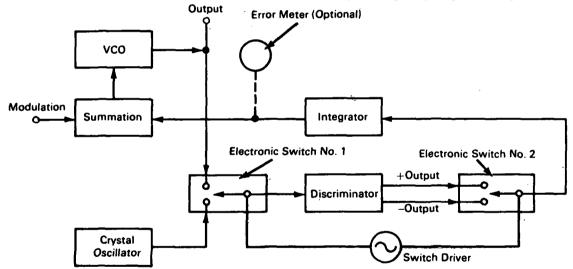


through C2 to reflex amplifier Q2. The amplified rf output is taken from resonant tank circuit L3-C6. The dc control voltage is fed through blocking filter L4-C7 to the dc input of reflex amplifier Q2. The amplified dc output voltage is developed across collector load resistor R2 and fed to attenuator control transistor Q1. Emitter resistor R3, in conjunction with R2, determines the dc gain of Q2, while C8, C4, and C5 act as ac bypass capacitors to maintain the rf gain of Q2 as high as possible. Source: S.H. Black of Sperry Gyroscope Co. under contract to Manned Spacecraft Center (MSC-00166)

Circle:14:on Reader Service Card

SIMPLE, ACCURATE AUTOMATIC FREQUENCY CONTROL CIRCUIT

This simple, automatic frequency control (AFC) circuit designed for use with voltagecontrolled variable-frequency oscillators (VCO's) operates with an accuracy comparable to that of more complex AFC circuits. The output frequency is not affected by the discriminator tuning as long as the controlled variable is within the relatively linear portion of the discriminator curve. Under this condition, the output frequency depends only on the sta-



The outputs of the VCO and the crystal oscillator are alternately switched into the discriminator by electronic switch no. 1 at a rate required for the specific application. The dual-polarity outputs of the discriminator are decommutated by switch no. 2, and the resultant square-wave, error-signal is integrated. The integrated signal is summed with the modulation signal, and the composite is applied to the VCO to reduce the output of the integrator toward zero. Center-frequency tuning of the discriminator is relatively unimportant; the only requirement is that the frequencies of both the VCO and crystal oscillator be within the passband of the discriminator curve.

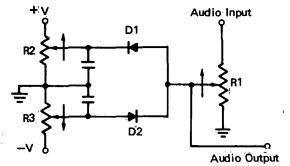
bility of the crystal oscillator. The sensitivity of the circuit is degraded at higher frequencies (as with all discriminators), but this degradation can be minimized by including more loop gain. At still higher frequencies, the circuit can be used at subharmonics of the output frequency either by a heterodyning process or by locking to an unmultiplied frequency sample. Either way, the output frequency is not affected by any discriminator tuning uncertainty.

> Source: F. Byrne Kennedy Space Center (KSC-10393)

Circle 15 on Reader Service Card

GAIN CONTROL LIMITER CIRCUIT

A triple-ganged potentiometer consisting of R1, R2, and R3 (see fig.) limits the audio gain of the circuit shown by controlling the output



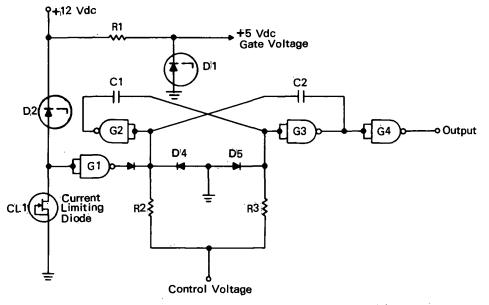
signal. Volume control section R1 controls the signal level in a manner similar to a conventional audio control circuit. Diode D1 limits the peak positive excursion of the signal. When the signal is more positive than the voltages set by R2, D1 conducts and limits the output. The negative peaks are limited by D2 and set by R3. All three resistors are normally ganged together so that the limits are set as the control is adjusted. Variations include using fixed resistors for section R1 and using only limit controls. Important advantages afforded by this circuit include an ability to control the maximum level and to limit any sudden upward changes in the output signal.

Source: G.D. Doland of Lockheed Electronics Co. under contract to Manned Spacecraft Center (MSC-11087)

No further documentation is available.

Section 7. RF Oscillators

LOW-POWER, COMPACT, VOLTAGE-CONTROLLED OSCILLATOR



A low power, compact, voltage-controlled oscillator ($\nabla C\Theta$) has a wide control range, a linear control response, and an output which is compatible with integrated circuitry.

The VCO (see fig.) is designed with an integrated circuit containing NAND gates G1, G2, G3, and G4. The oscillator has a linear response over the frequency range of 1 to 4 MHz for a control voltage of -1 to -6 V, respectively. The highest frequency limit, with a linear response, is approximately 5 MHz. The limiting factor is the propagation delay of the low power logic.

The oscillator section is a bistable multivibrator consisting of G2, G3, D4, D5, R2, R3, C1 and C2. The output is buffered by G4 for fanout purposes to additional circuits. The input network, consisting of G1, D2, D3, and C1, assures that the oscillator will start when power is initially applied, and prevents severe power supply transients from causing the oscillator to "latch up." CL1 is a current-limiting diode used to conserve power.

Voltage regulation for the gates, provided by R1 and zener diode D1, prevents undesirable frequency deviations which would otherwise

occur from ripple on the 5 V power supply. Circuit power consumption is 65 mW at 4 MHz, when the control voltage power is a maximum of 11 mW.

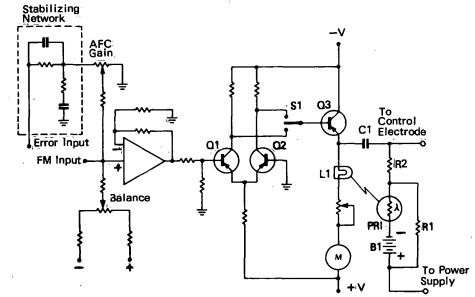
Assuming that a 5 V supply would have sufficient regulation to prevent undesirable frequency deviation, R1 and D1 could be eliminated and D2 changed to a 3 V zener. Subsequent power consumption could be reduced to approximately 25 mW, with no change in the control characteristics.

> Source: J.A. Exley of IBM Corp. under contract to Marshall Space Flight Center (MFS-20136)

Circle 16 on Reader Service Card.

AUTOMATIC FREQUENCY CONTROL OF VOLTAGE-CONTROLLED OSCILLATORS

A unique feature of this frequency-control oscillator circuit (see fig.) is the use of opticalcapacitive coupling for isolation of the klystron control electrode. The electrode voltage is conThe circuit is designed to stabilize the frequency of an S-band reflex klystron. The error input, derived from a discriminator which compares the klystron frequency with a harmonic



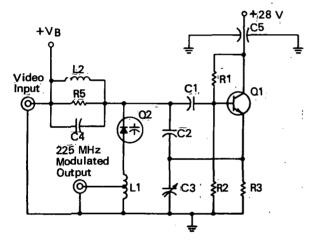
trolled by a voltage-divider photoresistor whose value approximates the potential of the control electrode. This circuit can be used for controlling the frequency of laboratory oscillators and for stabilizing the pump frequencies of parametric amplifiers. of a stable crystal oscillator, is applied to a stabilizing, lead-lag network and then amplified with an operational amplifier. Transistors Q1 and Q2 form an emitter-coupled differential pair for phase inverting the amplified signal without shifting the base operating point of Q3. Q3 drives lamp L1 and coupling capacitor C1. The meter indicates the lamp current and acts as an error indicator. The increase in the current through the lamp decreases the resistance of the photoresistor PR1 and changes the voltage of the control electrode. Because the lamp has a relatively long time constant, the coupling capacitor is used to transfer the high frequency components of the error signal.

Source: R.B. Kolbly of Caltech/JPL under contract to NASA Pasadena Office (NPO-11064)

Circle 17 on Reader Service Card

A 225 MHz FM OSCILLATOR WITH RESPONSE TO 10 MHz

A frequency-modulated transistor oscillator (see fig.) designed for use in wideband television transmitters, is an LC Colpitts tank-circuit configuration which provides sinusoidal output waveforms, even when excited by a nonsinus-



oidal input. The circuit also provides a high rate of phase change at the resonant frequency, which has the effect of producing good frequency stability.

A common-collector configuration for transistor Q1 is used primarily because the collector is internally connected to the case. The combined effects of case capacitance to ground and heat-sink capacitance to ground provide an effective rf ground for the collector.

The varactor Q2 is placed in series with the coil to eliminate the modulation effects that can occur when it is placed in a parallel configuration. At high frequencies, there is sufficient internal inductance and lead inductance to cause the varactor to enter the series-resonant mode. If this condition is allowed to exist, a drastic reduction in Q occurs, producing unpredictable modulation response.

The problem of applying the modulation signal and the bias voltage to the varactor is solved by using a blocking capacitor C1 and a series-trap tuned to a 225 MHz signal. The trap was designed with a low value Q to avoid undue attenuation of the sidebands through the trap and the video amplifier to ground.

The dc biasing network is conventional, with Q1 biased at 40 mA collector current and $V_{\underline{B}}$ at approximately 15 V. This biasing level enables the transistor to operate at a point which produces small-signal, class-A oscillation.

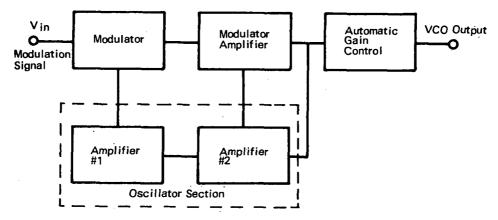
Source: Auburn University under contract to Marshall Space Flight Center (MFS-14977)

Circle 18 on Reader Service Card.

VOLTAGE-CONTROLLED OSCILLATOR

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The voltage-controlled oscillator outlined in the block diagram represents a unique approach to the generation of FM subcarriers and FM modulation. The VCO consists of an RC oscillator, a modulator, and an automatic gain control circuit. The basic oscillator is a phase shifter whose output amplitude is always constant regardless of the amount of phase shift. Two of



these phase shifters (amplifiers) are connected in series and the output of the second phase shifter is inverted and fed back to the input to produce the oscillations. The feedback loop-gain is controlled by an AGC circuit so that the amplifiers operate in their linear regions with a low-distortion sinewave output. The frequency of the oscillator is primarily determined by the value of the RC time constant if the phase shift in the amplifiers is small. The design of the oscillator requires a balanced, high input impedance, differential amplifier with matched transistors that have minimal drift characteristics.

The modulator section generates a current at the oscillator frequency, the magnitude of which is proportional to the modulating signal. The modulator can be considered as an analog multiplier, since its output is the product of an input signal at the oscillator frequency and the magnitude of the modulating signal. The modulator exhibits nonlinear characteristics which serve to negate the opposite nonlinear modulating characteristics of the phase-shift oscillator.

Automatic gain control is accomplished by varying the resistance in the feedback loop of the oscillator second stage. This resistance is varied by changing the gate potential of a field effect transistor. The AGC amplifier compares the output signal amplitude with a reference voltage and supplies a current pulse.

> Source: Spacelabs, Inc. under contract to Manned Spacecraft Center (MSC-11707)

Circle 19 on Reader Service Card.

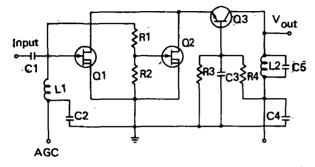
Section 8. RF Amplifiers

VARIABLE GAIN AMPLIFIER

The design of this amplifier combines improved input and output impedances with relatively large signal handling capability and an immunity from the usual adverse effects of automatic gain control (AGC). These advantages are achieved through the use of two FET's, with sources and drains in parallel, plus a resistive divider for the signal, and bias to either of the gate terminals.

The ac signal is coupled into the circuit with C1. L1 provides a high impedance to the ac signal and a low impedance path for the AGC

potential, while C2, C3, and C4 (bypass capacitors) provide low impedance ac-signal paths. R1 and R2 divide the ac signal and the AGC potential applied to the gate of Q1.L2 and C5 form a tuned resonant circuit which is the load impedance at the ac operating frequency. The two FET's, Q1 and Q2, produce a remote cutoff feature that makes the circuit perform in a manner similar to that of a remote-cutoff vacuum tube. At low values of AGC bias, both Q1 and Q2 contribute to the forward transfer admittance. As the bias is increased, Q1 approaches cutoff more rapidly than Q2 since the bias applied to Q2 is also divided by R1 and R2. As Q1 ap-



proaches cutoff, Q2 takes over control of the forward transfer admittance of the circuit. The AGC bias required to cutoff Q2 is larger than that required to cutoff Q1, by a factor determined by R1 and R2. With the proper selection

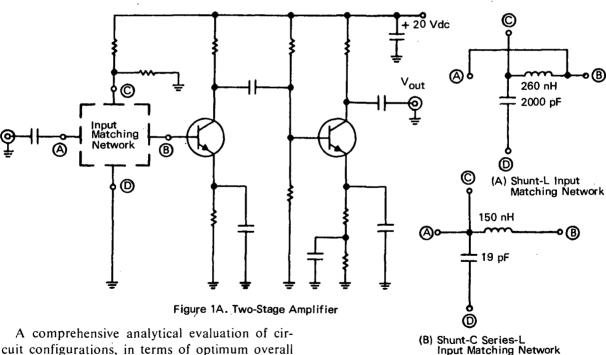
of the ratio of R1 and R2, the FET transfer characteristic can be optimized for a smooth transition.

The grounded-base configuration of Q3 provides a low impedance drain load for Q1 and Q2, further reducing the reverse energy transfer from drain-to-gate of Q1 and Q2, and consequently reducing input impedance variations produced by the AGC.

The elimination of input impedance variations (as a function of AGC voltage) is especially important in rf and i.f. amplifiers where these variations could alter the bandwidth and center frequency of the previous stage.

> Source: G. H. Spaid Goddard Space Flight Center (GSC-10116)

No further documentation is available.



LOW-NOISE, WIDE-BANDWIDTH I.F. PREAMPLIFIER

A comprehensive analytical evaluation of circuit configurations, in terms of optimum overall wideband performance, resulted in the development of a wideband i.f. preamplifier (see fig.) which can be used in most types of communications receivers. Its exceptional performance features include a 20 dB power gain over the

passband of 10 MHz to 100 MHz, with a passband ripple of 1 dB. During the initial design, the major problems which hindered the achieve-

Figure 1B

ment of a high passband with a concurrent low noise figure were found to stem from the difficulty of achieving a source admittance that was optimum with respect to the noise figure over a wide bandwidth.

After a thorough analytical investigation, the basic configuration chosen was a two-stage, common-emitter amplifier with series feedback in the second stage only (see Fig. 1A). The design in Fig. 1B provides a choice between the two input matching networks (A and B) that optimize performance over different portions of the passband. Further computer analysis showed

that the simple shunt-L network meets the noise figure of 1.5 dB at 60 MHz if the passband is from 20 to 120 MHz. The shunt-C, series-L input matching network was found to provide better overall performance from 10 to 110 MHz, but had a marginal noise figure.

> Source: W. S. Jones and G. R. Pierson of **Texas Instruments** under contract to Electronic Research Center (ERC-10321)

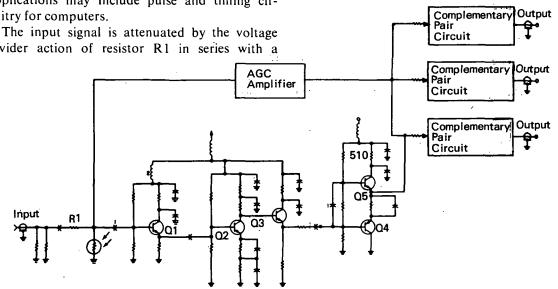
Circle 2010n Reader Service Card.

COMPLEMENTARY PAIR BROADBAND TRANSISTOR AMPLIFIER

A wideband distribution amplifier with a bandwidth of 50 MHz can be used in commercial radio, FM, and television circuits. Additional applications may include pulse and timing circuitry for computers.

divider action of resistor R1 in series with a

Since the basic amplifier is a linear device, an automatic gain control (AGC) system is required; 20 dB of AGC is obtained by varying



thermistor (see fig.). Transistor Q1 acts as an isolation stage, and a voltage amplification of 10 is achieved by the next stage, which includes Q2. The signal is then fed into a high-impedance emitter follower Q3.

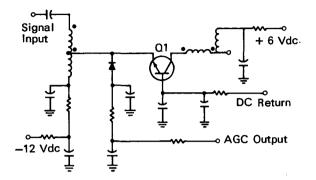
The complementary pair of transistors, Q4 and Q5, functions as a driver for the final output stages. The output impedance of the complementary emitter follower output stages is very low, allowing them to drive low impedance loads with low distortion.

the resistance of the thermistor in the attenuator circuit.

> Source: G. D. Thompson, Jr. and G. F. Lutes, Jr. of Caltech/JPL under contract to NASA Pasadena Office (NPO-10003)

Circle 21 on Reader Service Card.

GAIN AND PHASE-TRACKING AMPLIFIER



A comprehensive analysis of i.f. amplifiers operating at 40.8 MHz was undertaken to provide criteria for selecting the appropriate matched transistors. With the use of matched transistors, the adverse effects in a common-base amplifier stage are minimized. Included in this analysis is a mathematical model of the AGC circuit shown in the figure. The optimum AGC control voltage was dctermined, and mathematical expressions were derived to enable the design engineer to select devices for optimum circuit performance.

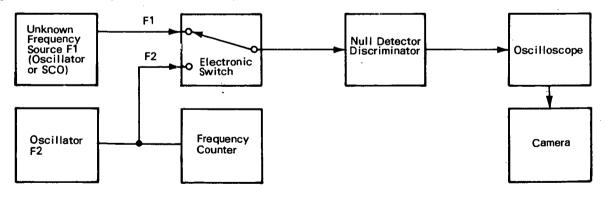
> Source: H. L. Slade of Radio Corp. of America under contract to Manned Spacecraft Center (MSC-12277)

Circle 22 on Reader Service Card.

Section 9. RF Measurement Techniques

DYNAMIC LINEARITY MEASUREMENT TECHNIQUE

This technique measures the dynamic linearity of a frequency modulated (FM) subcarrier oscillator. An FM discriminator operating as a high gain null detector produces an error signal comsquare wave amplitude is directly proportional to the frequency difference of the two oscillators, and its repetition rate is directly proportional to the electronic switch speed. The amplitudes of



posed of two signals (one of known frequency, the other unknown) which are electronically switched to the discriminator input. This analog error signal becomes zero when both input signal frequencies coincide.

When both frequency sources are at the same frequency (F1 = F2), the net output from the discriminator will be zero. When the sources are at different frequencies (F1 \neq F2), a square wave appears at the discriminator output; the

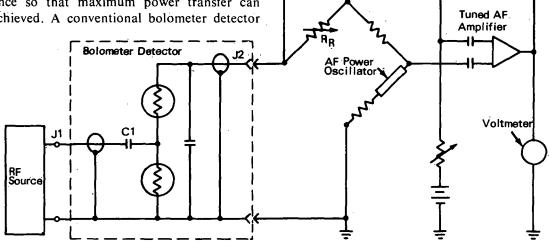
the signal generator outputs are unimportant because of the broad limiting action of the discriminator. The discriminator is fully limiting with an output of 5 mV or greater.

> Source: K. Merz and L. Morrell of The Boeing Co. under contract to Kennedy Space Center (KSC-10186)

Circle¹23 on Reader Service Card.

SIMPLIFIED METHOD FOR MEASURING THE IMPEDANCE OF RF POWER SOURCES

A simple test method using the circuit shown in the figure measures the rf-source output impedance so that maximum power transfer can be achieved. A conventional bolometer detector



and bridge circuit are used to measure the rf power, and a bridge reference resistor is varied to achieve the condition of maximum power transfer.

With no rf power introduced into the bolometer detector, proper amounts of dc and af power cause the bolometer elements to be driven to the resistance which is equal to the value of the bridge reference resistor. With the dc bias maintained constant (to zero the meter), rf power applied to the input J1 changes the resistance of the bolometer element, unbalances the power bridge, and generates a voltage that reduces the af oscillator power by an amount equivalent to the rf power that has been added. The rf source resistance can be derived from the value of R_R .

Source: E. C. Oakley of Caltech/JPL under contract to NASA Pasadena Office (NPO-10734)

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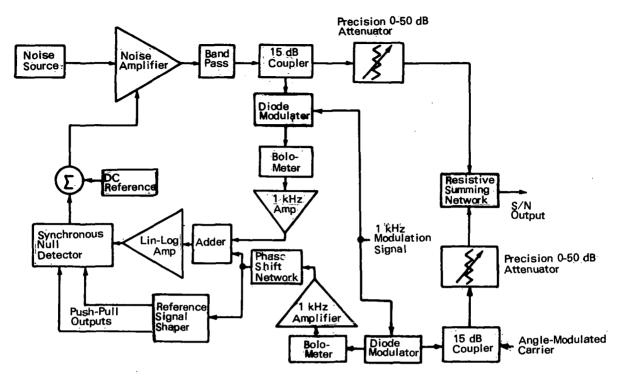
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LINEAR SIGNAL-NOISE SUMMER ACCURATELY DETERMINES AND CONTROLS S/N RATIO

A linear signal-noise summer accurately determines and controls the signal-to-noise power level ratio. This type of circuit should be applicable whenever it is necessary to mix background noise with the desired signal in known ratios and to measure detection as a function of varying S/N ratio. The noise power is referenced to the signal power, so that changes in the signal level are not reflected as changes in S/N ratio but as a change in absolute signal and noise power levels. Noise is generated through a temperature limited diode and then amplified. The effective noise bandwidth of the system is established by a Butterworth filter. The dc reference is a zener, voltage adjustable in level and preset to a desired automatic gain control operating point on the noise amplifier.

The 1 kHz carrier-detected signal, used as a reference signal, is applied to a constant amplitude phase-shifting network. Vectorial comparison of the reference signal and noise signal is made in an adder circuit and then fed to a linear-log amplifier.

The output of the amplifier is applied to the control grid of the synchronous detector. A second signal, taken from the phase shift



network output, is applied through a limiter and square wave shaping circuit to a push-pull amplifier, which in turn is used to drive the deflection plates of the synchronous detector. The synchronous detector difference output is then summed with the dc reference. The noise power is therefore referenced to the carrier such that changes in either of the two levels are not reflected as changes in the S/N ratio.

With the noise power level accurately defined in bandwidth through the noise filter and referenced directly to the angle modulated carrier through the feedback loop, accurate noise levels and signal levels are set through precision $50-\Omega$ attenuators.

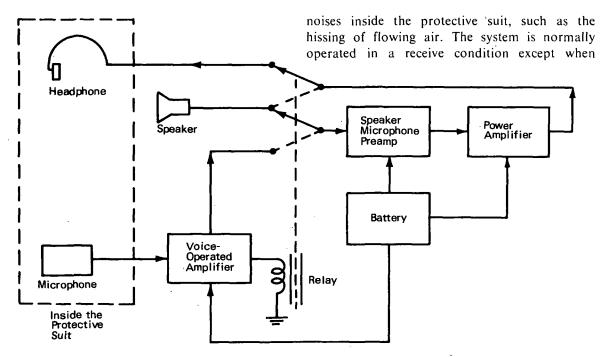
Source: J. L. Sundry of Westinghouse Electric Corp. under contract to Jet Propulsion Laboratory (JPL-SC-00152)

Circle 25 on Reader Service Card.

Section 10. Personal Communications Systems

SELF-CONTAINED MINIATURE ELECTRONICS TRANSCEIVER PROVIDES VOICE COMMUNICATION IN HAZARDOUS ENVIRONMENT

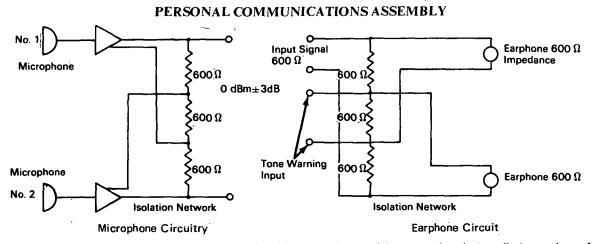
This voice communications system for use in protective suits fulfills the following requirements: (1) The communications equipment does not impede freedom of movement; i.e., attached cabies are eliminated. (2) Operation of the system is automatic; i.e., the voice provides the input energy to activate the system in the proper mode. (3) An acute awareness of the surroundings can be maintained, and sounds which are advance warnings of impending hazards (gas hissing, material cracking, voice warnings and the like) can be heard. (4) The communications system does not introduce an additional hazard; i.e., the rf output power does not activate electromagnetic sensitive devices such as fuses or explosives.



When the operator speaks into the microphone, his voice is transmitted, external to the protective suit, by the combination speaker/receiver. When the operator is not talking, the system is in the receive position so that he can hear noises above a particular audio level in the immediate vicinity. The voice-operated amplifier must be biased to a certain level to prevent activation by the user speaks. In the transmit mode, the unit becomes a miniature audio amplifier with a power output of about 1 W.

> Source: H. E. Cribb Kennedy Space Center (KSC-10164)

Circle 26 on Reader Service Card.



This personal communications system should be useful where work space requires miniaturization and very high levels of noise rejection. The total integrated unit (see fig.) consists of a housing, two-part acoustic tube assembly, microphone amplifier, isolation network, and wiring harness. For redundancy, two microphones operate output level through an isolation network to a balanced load ($600 \pm 60 \Omega$) to provide an output level of 0 dBm \pm 3 dB for an input of 96 dB and 10 dB \pm 3 dB for an input of 116 dB.

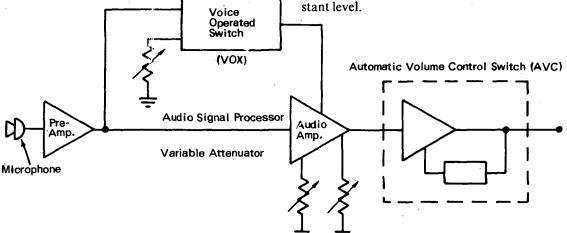
Each earphone assembly includes 6 transducers to obtain a high level audio output of improved quality in the presence of ambient noise. Each assembly, adaptable for use in an earmuff or directly into the ear, consists of the transducers, isolation network, housing, mounting provisions and wiring harness. A tone warning input signal circuit is also provided to alert the operator to incoming intelligence. With two earphones connected to the isolation network (driven at 4 mW sinewave), the output sound pressure level of each earphone, measured at 1 kHz in a 6 cc cavity, is $108 \pm 3 \, \text{dB}$.

Source: N.D. Atlas of North American Rockwell Corp. under contract to Manned Spacecraft Center (MSC-720, 722)

Circle/27 on Reader Service Card

AUDIO SIGNAL PROCESSOR

The signal processing system shown in the diagram provides automatic volume control for an audio amplifier or a voice communication system, without introducing noise surges during AVC gain is nullified, and no noise surge occurs. When the signal resumes, the audio switch returns the amplifier gain to normal, at a rate approximately equal to the decay of the AVC gain, in order to maintain overall gain at a constant level.



pauses in the input, and without losing the initial signal when the input resumes.

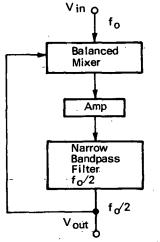
The preamplifier output is fed through a variable-gain amplifier to a conventional automatic volume control (AVC) circuit, and also through an audio switch which detects the presence of a signal and controls the variable-gain amplifier. When the system input halts for more than a moment, the audio switch reduces the gain of the amplifier at approximately the same rate as the AVC circuit gain increases. Thus, the increased False noise triggering is controlled by setting the detection threshold of the switch slightly above the ambient noise level. A short delay is provided in the switch turn-on time to furnish even greater protection against false triggering by high-amplitude, short-duration impulses.

> Source: R. Hymer Manned Spacecraft Center (MSC-12223)

Circle 28 on Reader Service Card

Section 11. Phase-Locked Loop Techniques

HIGH NOISE IMMUNITY, WIDEBAND BI-PHASE DEMODULATION SCHEME



In communication systems where noise is a severe problem, the extremely narrow bandwidth of a phase-locked loop increases the effective signal-to-noise ratio when compared to other types of schemes. A wideband bi-phase demodulator (see fig.) has been proposed as a substitute for the phase-locked loop. The circuit in most instances will yield the same performance as a phase-locked-loop divider as far as signal detection is concerned. The basic regenerator is much less susceptible to noise than a digital divider because of the reduced bandwidth of the divider circuit. Because of the phase. detection process in a bi-phase demodulator, decreasing the clock circuit noise by less than-20 dB below the noise level in the wideband bi-phase circuitry does not appreciably increase the S/N ratio out of the phase detector. Therefore, in many systems now using a phase-lock loop, this simpler regenerative divider is practical. The major advantages of this system are simplicity, low cost, light weight, and low volume, with a circuit performance that rivals a phaselock loop.

> Source: E. J. Mitchell of Radio Corp. of America under contract to Manned Spacecraft Center (MSC-12102)

No further documentation is available.

PHASE-LOCK LOOP PHASE MODULATOR WITH HIGH MODULATION INDEX, LOW DISTORTION

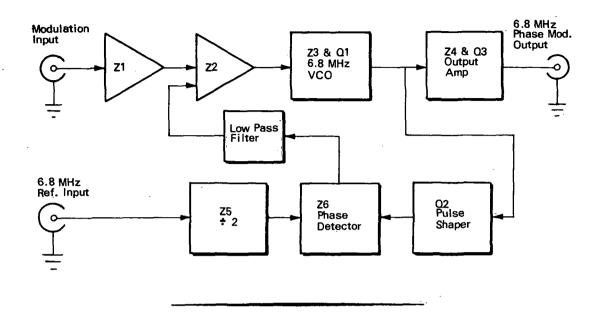
The phase-lock loop phase modulator shown in the schematic generates a 6.8 MHz carrier at modulation indices as high as 2.5 with less than 5% signal distortion. The modulation signal is applied to the noninverting input of amplifier Z1, which provides a dc-coupled modulating signal to Z2 so that the low frequency response of the modulator is unrestricted. As the voltagecontrolled oscillator Z3 is phase-locked to the reference signal at J2, the demodulated signal originating at the phase detector Z6 output cancels any Z3 frequency changes that would be caused by the amplified modulation signal from Z2. This cancellation depends on the loop gain and the phase shift through the loop. As the modulation frequency is increased, the signal increases in phase lead until the first break

point of the closed-loop response is reached.

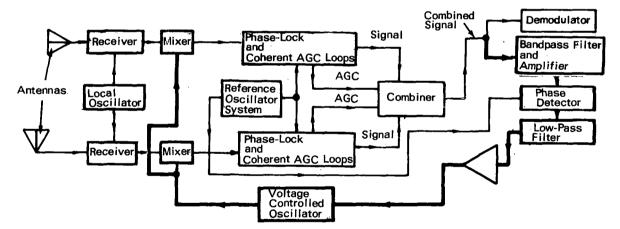
This circuit can have a theoretical phase deviation of π rad (180°) (modulation index of 3.14), but in actual practice is limited primarily by the capability of the phase detector, Z6, to produce a properly damped, full square wave at the reference frequency. The large phase deviations of this circuit are made possible by the use of a digital-type (variable duty cycle) phase detector.

> Source: C. G. Badstiibner of Radio Corp. of America under contract to Manned Spacecraft Center (MSC-12247)

Circle 29 on Reader Service Card.



RF RECEIVING SYSTEM WITH IMPROVED PHASE-LOCK CHARACTERISTICS



An improved receiving system automatically combines the output from two independent receiving channels in a manner that optimizes signal reception. The combined signal output from the two receivers is applied to a primary phase-lock loop, shown by heavier lines in the block diagram. In this loop, the phase of the combined signal is compared with the phase of a reference signal, and an error voltage proportional to the phase difference is developed. This error voltage is used to vary the frequency of a voltage controlled oscillator, which in turn has its output signal heterodyned with the input signal in each of the receiving channels. In this manner, the primary phase-lock loop permits the system to track changes common to both receiving channels so that frequency variations, such as those due to Doppler shifts, are followed. Two secondary gaincontrol loops in the individual receiving channels compensate for differential signal changes in these channels, and thus ensure phase coherence.

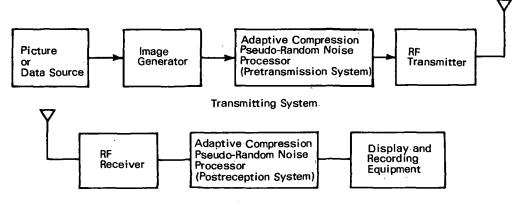
Source: C. R. Laughlin, Jr. and V. J. DiLosa Goddard Space Flight Center (XGS-01222)

Circle 30 on Reader Service Card.

Section 12. Video Circuits for TV Applications

VARIABLE WORD-LENGTH ENCODER REDUCES TV BANDWIDTH REQUIREMENTS

An adaptable, variable resolution (variable word-length) encoding technique increases the transmission efficiency of pulse code modulated television signals by reducing the required bandwhich modulates the transmitter. The PTP obtains analog-to-digital conversion by means of a variable resolution analog-to-digital converter which is capable of converting input





width. The electronic instrumentation includes a pseudo-random noise signal processor which reduces the channel capacity required for signal transmission. Complementary processors are required in both the transmitting and receiving systems.

A pretransmission processor (PTP) is placed between the image generator and the transmitter in the transmission system. A postreception processor (PRP) is placed between the receiver and the display equipment.

The basic function of the PTP is to add an adapted pseudorandom noise to the picture data and encode this combined signal by means of a variable resolution encoder. This process generates a pulse coded picture-pulse-noise signal voltage into a l-through-n bit word. The number of bits per word is selected by a variable compression control generator.

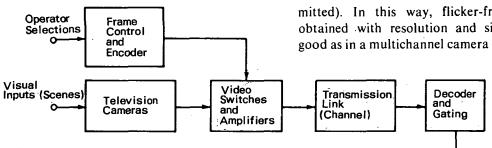
After the signal has been received and decoded, the PRP puts the signal through a variable resolution digital-to-analog converter which decodes it into an analog signal. The adapted pseudorandom noise from the combined analog signal is then removed and processed by a compensator to give an output equivalent to the input signal the PTP was given.

> Source: W. E. Sivertson, Jr. Langley Research Center (LAR-00087)

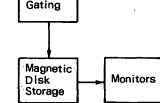
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MULTIPLEX TELEVISION TRANSMISSION SYSTEM

A time-multiplexing system (see fig.) enables several cameras to share a single commercial television transmission channel. In this multiplex system, the output of each camera on a standard transmission link is controlled in any desired sequence, and the sequence is repeated once each second. The number of frames allocated to each camera is decided on the basis of the expected or observed rates of change of the several scenes to be viewed. Each transmitted frame is identified by digitally encoded signals added to the basic camera signal. Automatic equipment at the monitoring end of the link decodes the camera



identification. and routes the successively transmitted frames from the various cameras to the monitors and corresponding magnetic disk recorders. The recorded frames from each camera that is not transmitting are reproduced and channeled to the proper monitor at a rate of 30 frames per second. Thus, every monitor receives 30 frames per second regardless of how often the content of the frame is changed (transmitted). In this way, flicker-free pictures are obtained with resolution and signal-to-noise as good as in a multichannel camera system.



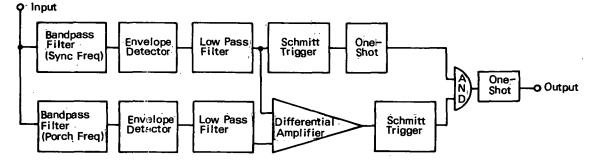
Source: W. R. Reed Manned Spacecraft Center (MSC-11595)



TV SYNCHRONIZATION SYSTEM FEATURES STABILITY AND NOISE IMMUNITY

The synchronization circuit shown in the diagram increases TV video presentation by eliminating ambiguous sync signals. An additional sync level is introduced as a "back porch" on

from statistically separate sources. The noise is r.s.s.'d, and the sum is 3 dB greater than either separately. The peak-to-peak signal is 6 dB greater, so that, for a given signal-to-noise



the sync pulse. In the presence of noise, the sequential signals at sync and porch frequencies provide a sync identification from which a coincidence circuit can generate sync pulses having the required stability and noise immunity.

Basic components in the system include a sync frequency bandpass filter, envelope detector, and low pass filter. A duplicate channel is introduced to sense and translate the porch frequency. Noise at the summing point input to the differential amplifier is derived from two separate equal-bandwidth frequency domains condition, jitter due to noise vs rise-time is 3 dB less than that produced without the differential amplifier. Output coincidence from the syncchannel one-shot and porch-channel Schmitt trigger causes an output from an AND gate which triggers the output one-shot to provide the actual sync pulse to the horizontal sweep.

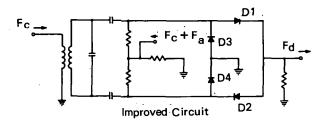
> Source: F. P. Landauer Jet Propulsion Laboratory (JPL-00915)

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Section 13. Mixers

ADDED DIODES INCREASE OUTPUT OF BALANCED MIXER CIRCUIT

This balanced mixer circuit can be used to increase the output signal level of conventional circuits commonly used in radio transmitting and receiving equipment. The addition of two



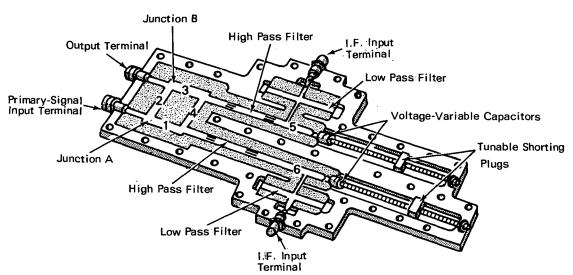
diodes which form a half-wave carrier-switch balanced modulator doubles the output signal level and reduces spurious output and distortion.

The diodes, D3 and D4, are added to a con-

ventional balanced mixer (see fig.) to produce a difference frequency F_d at the output. The inputs F_c and $F'_c + F_a$ represent inputs at the carrier frequency and the carrier plus audio frequencies, respectively. Addition of the center-tap-grounded diodes permits both legs of the circuit to function throughout the ac cycle. This effectively doubles the output frequency while reducing the level of spurious signals at frequencies $F_c + F_a$ and $F_c - F_a$ by 50%. Distortions caused by signals at the third harmonic of F_a are also reduced by 50%.

Source: G. B. Robinson Goddard Space Flight Center (GSC-00354)

No further documentation is available.



COMPACT MICROWAVE MIXER HAS HIGH CONVERSION EFFICIENCY

This compact, lightweight microwave mixer has a relatively high conversion efficiency and power output. A pair of back-to-back voltagevariable capacitors in a stripline network provides the heterodyne action. A primary frequency signal applied to the input terminal passes to branch 1 of the branchline hybrid. The hybrid splits the input signal, providing two signals which are $\pi/2$ rad (90°) out of phase. These out-of-phase signals are applied to the parallel stripline circuits 5 and 6. One of the parallel striplines is a quarter wavelength longer than the other so that the signals are in phase at the ends of the striplines. Intermediate-frequency signals are applied through the low pass filters to the voltage-variable capacitors at the ends of the parallel striplines. As a result of the heterodyne effect produced by the voltage-variable capacitors, the signals are reflected back through the parallel striplines. These signals include the high and low sidebands of the primary input signal. The reflected sidebands are passed by the high pass filters, but are rejected by the low pass filters, thereby reaching the branchline hybrid (1, 2, 3, 4). Differences in electrical paths and phases cause the sidebands to be cancelled at junction A. However, the sidebands are reinforced at

junction B, from which they pass to the output terminal. The tunable shorting plugs may be varied over a selected frequency range to optimize the output level of the voltage-variable capacitors.

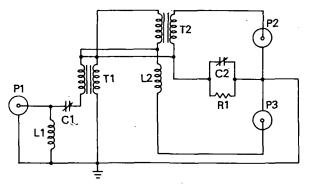
> Source: N. J. Penque and H. A. Rosen of Hughes Aircraft Company under contract to Goddard Space Flight Center (GSC-00197)

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SIGNAL MIXER PROVIDES OUTPUTS WITH MATCHED IMPEDANCE CHARACTERISTICS

The novel circuit shown in the figure enables the routing of a single signal circuit simultaneously into two or more circuits which have similar impedances. Immediate applications include the connection of several radio receivers to the same antenna with no degradation to system performance.

The input signal at port P1 is transformed into two similar outgoing circuits of the same impedance at P2 and P3. The incoming signal feeds into the primaries of transformers T1 and T2, in series with the resonating network L1-C1. A division circuit between the primaries of these transformers feeds directly through L2 to the high side of output port P3. The transformer primaries, having similar characteristics, represent a signal divider which feeds in series with L2 to the output port. The value of L2, serving as a phase correction device, is determined by the input-to-output impedance match. In this case, a 50- Ω input is divided into two 50- Ω output circuits.



The secondaries of T1 and T2 form a circuit divider through an RC network, R1-C1, to the ground side of both P2 and P3. The RC network regulates the voltage delivered by the secondary of T2 to P2, and load-tunes the secondary.

Source: R. C. Kinsel of Avco Corp. under contract to Goddard Space Flight Center (GSC-00063)

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