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ABSTRACT

This paper describes the X-Ray Spectroscopy Experiment to be flown on Aerobee Flight 13.009.

A brief description of the detector system is given followed by a description of the electronic portion.

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ILLUSTRATIONS

I. INTRODUCTION

The sensor portion of the experiment consists of two gas filled sealed multi-anode, multi-layer proportional counters which look out through open doors of the rocket payload after burnout is completed.

An ACS startracker system will orient the detectors to within $\pm$0.1 degree of the selected targets.

Data collected by the detectors will be analyzed in the main electronics, converted into a PCM format, and telemetered to ground stations along with housekeeping information at a 50 K bit rate. Two cameras on board will record aspect information to verify the experiment attitude.

II. DETECTORS

The two detectors will be referred to as Detector "A" (forward) and Detector "B" (aft).

Detector "B", shown in Figure 1, is essentially the same as the detectors flown on flights 13.07 and 13.08 with the exception of the x-ray collimator which has been changed to a 3 degree FWHM circular unit made of Beryllium-Copper tubes.

The "B" detector is a three layer plus anticoincidence sensor in which the detecting gas is 760 torr of xenon plus 76 torr of methane. The detector is a sealed unit employing Butyl O-Rings on the sealing surfaces.

The X-ray entrance is through a 1-mil aluminized Kapton window which uses the mechanical collimator for support.

Detector "A" is a double gas detector in which the first layer of anodes is partitioned from the remaining layers and has a separate gas

(methane). This layer is used as a anticoincidence to guard against low energy electrons, either produced or entering through the collimator.

Partitioning of the layers is effected by an additional Kapton window between the 1st and remaining layers. The gas in the lower portion of the detector will be identical to that of Detector "B".

The "A" collimator is a two part unit with 83 percent of the area having a 1/2 degree FWHM acceptance angle while the remaining 17 percent is blocked off in order to allow a determination of internal detector background during the flight. Detector "A" is shown in Figure 2.

The internal active areas of both detectors are identical in construction and consist of 2 mil diameter wire anodes surrounded by similar ground wires. Each wire is installed with a spring on one end in order to insure a uniform tension.

III. DETECTOR ANTICOINCIDENCE

If an X-ray entering the collimator and passing through the thin window reacts in the gas, it usually deposits all its energy only in one cell. Thus the signature of an X-ray may be singled out as unique from an energetic charged particle which deposits some of its energy in each cell it passes through.

Detector "B" 's three active layers are strapped such that alternating cells are connected together (figure 3).

The alternating cells are treated in the electronics such that if a coincidence event is seen between any two horizontal cells in the same layer the event is not rejected but is marked for possible future analysis. All outside edge cells are strapped together to form

a guard against charged particles around the sensitive detector volume, leaving only the collimator entrance unprotected.

In addition to having this outside anticoincidence we connect each vertical grid (layer) electronically in anticoincidence with every other layer, and thus reject nearly all unwanted particles passing through, or stopping in, the detector.

IV. TELEMETRY FORMAT

The rocket PCM-FM transmitter is continuously modulated with a repeating format consisting of 64 frames of sixteen bit words (Fig. 5). The first word in each frame is a sync word which allows a known starting reference point (Fig. 6).

Words 2 and 34 contain information only on bits 12 through 16. This information is Scaler II and consists of the total acceptable events that have occurred during the readout of the previous word (320 μsec). In the case of word 2 the accumulation time is 640 microseconds, since it has been storing for both words 64 and 1 before being read out.

Words 3 through 32 and 35 through 64 contain spectral data as well as rates (Fig. 7 & 8). The first three bits of these words contain an I.D. (detector and layer identification), 7 bits of pulse amplitude information, mark bit (1 or 0), and 5 bits of Scaler II count rate information. As stated before, the rates being read out in Scaler II are the acceptable events which occurred during the readout of the previous word. A one in bit 11 (mark bit) indicates that the layer being analyzed has a horizontal coincidence.

Word 33 (Fig. 9) contains rate data the first 6 bits of which are upper threshold and vertical coincidence events. Bits 7 through 12 contain commutated low threshold rates. Bits 13 and 14 are used as flags to signal when the A detector anticoincidence rate goes above 1000 and 10,000 events respectively. Bits 15 and 16 are likewise used to flag Detector "B" anti-rates.

This format is repeated continuously at a 50 K bit rate.

V. ELECTRONIC SYSTEM DESCRIPTION

Fig. 10 is a system block diagram of the x-ray experiment. As stated earlier, an x-ray event normally deposits all its energy in one single cell of the detector. The electronic system was designed to detect and analyze just such events.

When an x-ray event or a charged particle stops or passes through the gas volume of the detector, it ionizes the gas. As these ions are accelerated to the closest anode, additional ions are generated by collisions. The collected ions at the anode deposit a charge at the output capacitor. The charge sensitive amplifier (Fig. 11) converts this charge into a shaped voltage pulse proportional to the energy of the incident event and sends it to the input of the Fast Normalizer Amplifier (Fig. 12) of the analog card (Fig. 13). Since analog cards A1, A2, A3, A4, B1, B2, B3 are identical our descriptions will be limited to card A1.

The input signal is amplified by the first stage of the fast normalizer and branched into two paths. In one branch the signal is delayed by approximately 6 μsec. and applied to the second stage of the fast normalizer for additional amplification before reaching the

linear gate (Fig. 14). This delay allows the logic circuitry time to determine by coincidence and anticoincidence whether the linear gate, which is normally closed, should allow the signal to pass. See Figures 15 and 16 for timing waveforms.

The signal in the second branch is also delayed by approximately 2.25 μs and applied to a set of discriminators (Fig. 17). These discriminators yield a .5 μs digitized pulse when their discriminator levels have been exceeded. The amplifier stage between the discriminators (Dual 2A Amp, Fig. 18) provides the necessary gain required for establishing a window for acceptable events. A shunt gate is connected to each discriminator output. A 5 μs pulse is applied at the input of the shunt gate whenever an event occurring in the guard layer exceeds threshold. This pulse will inhibit the upper and lower discriminators whenever a coincidence occurs. The 2.25 μs delay is required so that the .5 μs discriminator pulse is well within the 5 μs inhibit pulse.

The upper and lower level disc. outputs are fed to the Upper Level Logic Card (Fig. 19) "OR" gates and summing amplifiers respectively. One summing amplifier (Figure 20) yields .3 μs output pulse delayed by 2.75 μs when one or more events are in coincidence at the input of the summing network. The other (Fig. 21) yields an output when 2 or more events are in coincidence.

This output is applied to the input of the "OR" gate along with the upper threshold pulses. Either an upper threshold or 2 or more events (vertical coincidence) generate a 3.25 μs inhibit pulse. Thus a .5 μs pulse occurs only if a single low level event occurs and since such an event meets all the necessary requirements, it may be identified

as an x-ray event and stored in the Scaler II register. All other events which have an upper threshold or a vertical coincidence associated with it are rejected events and stored in Scaler I register for rate analysis only.

If the system is not busy, the first Scaler II event received will be allowed to pass a gate and set the System Busy Bistable flip-flops which in turn will close the gate, making the system busy during the pulse height to time conversion. The set pulse (event enable pulse) is also fed to the analog card Event Enable Gate (Fig. 22) and by coincidence determines the layer in which the event occurred. This coincidence pulse triggers a 1 μs pulse generator and feeds it to the ID Logic Card (Fig. 23). The ID logic generates a 3 bit coded ID which identifies the event to a specific layer. This coincidence pulse will also open the linear gate providing it is not inhibited by the Resettable Memory Circuit (Fig. 24). It should be noted that when the lower lever discriminator fired, it also triggered a 12.5 μs pulse delay by 4 μs. This 12.5 μs pulse is applied at the input of the memory inhibit gate, (Fig. 22), preventing the linear gate from opening for the pulse duration. Events which occurred in the same layer and followed another event up to 12.5 μs do not constitute good events and are therefore rejected by preventing the linear gate from opening. All such events are identified in the readout by an ID and no pulse height analysis.

As stated earlier, if all conditions are met, the linear gate will open for 5 μs allowing the analog signal through free of any distortions.

The output of the linear gate is connected in parallel with the other linear gates and is applied to the input of the Nanosecond Sweep

Circuit (Fig. 25) of the Analog to Digital Conv. Card (Fig. 26). The primary function of the ADC card is to convert the linear gate output pulse amplitude into a pulse train containing a number of pulses, proportional to the pulse amplitude. This height to time conversion is accomplished in the Nanosecond Sweep Circuit by charging a condenser and then allowing it to discharge linearly. This linear discharge is converted into a pulse whose width is proportional to the discharge time as shown in Figure 27. This pulse, in turn, gates the Output Gate (Fig. 28) which yields the pulse train. The pulse train is fed to a 127 bit capacity scaler in the Encoder (Fig. 29). The accumulation time is, of course, dependent on the oscillator frequency. 1.6 MHz oscillator frequency was chosen to reduce the dead time to a maximum of $127 \times .625\ \mu s \simeq 79.3\ \mu s$.

The System Busy Bistable shown in Figure 31 assures that subsequent x-ray events will not be processed during conversion time.

As indicated earlier an event will set the System Busy Bistable Flip-Flop. The flip-flop will remain in the set state until a reset pulse is obtained from the Encoder. Since the encoder is free running, it is necessary that no reset is obtained during conversion time. This is accomplished by providing the encoder with an End of Pulse Train Bit. This bit signifies that the pulse processing has been completed and a new event may now be accepted.

It was also stated earlier, that on occasions an event will set the System Busy Bistable but the linear gate did not open because an event has also occurred in the previous 12.5 μs. Since the linear gate did not open, no pulse train could be generated. A more detailed

description of the operation of the ADC card is required to explain this inconsistency. When an x-ray event sets the System Busy Bistable, the output is fed to a 2.5 μs delay generator (Fig. 32). The delayed output is branched into three separate paths. One branch is applied to an inhibit gate (Fig. 33) whose output generates the "end of pulse train bit." In the second branch, the signal is gated with the pulse train. Whenever a pulse train is present at the Output Gate, the gate yields a pulse which is applied at the inhibit gate described above. Therefore, the signal in the first branch is inhibited whenever an event generated a pulse train. In the third branch, the delayed pulse is gated with the free running oscillator. The output of this gate (Fig. 34), synchronized to the oscillator, sets the ADC Bistable (Fig. 35), which initiates the linear discharge of the sweep circuit condenser described earlier. The ADC Bistable high state sets the Output Gate so that a pulse train may be generated. However, before the Output Gate can be set, it has to be enabled by the "shaped" output of the sweep circuit. The trailing edge of the "shaped pulse resets the Output Gate, terminating the pulse train and generates an "end of pulse train" bit.

The 2.5 μs delay, described above, was necessary so that the charging condenser had time to charge fully before initiating the linear discharge.

It should be apparent, that, an "end of pulse train bit" will be generated regardless of input conditions, allowing the Encoder to furnish the reset pulse required to analyze other events.

Mark Bit Logic

Another type of event coincidence not yet dicussed is the Mark Bit or horizontal coincidence (see Figs. 36, 37, 38).

As described earlier, an event which traverses two or more cells in the detector is very likely a charged particle or cosmic ray other than x-ray. Since most particle events that penetrate the detector from the side will be detected in the guard layer and antied out, and since x-ray events are restricted to entering only through the collimated thin window, these horizontal coincidence events are of a special interest such that pulse height analysis is desirable, but flagged as distinct events.

The following is a brief description of the Mark Bit Logic.

As seen in Fig. 3 , the anodes of each layer of the detector are alternately tied together. The lines are connected through transformer windings to a common charge sensitive amplifier whose output is fed to the analog card described previously. The currents induced into the primary windings of the transformer by an event are reflected into the secondary winding and amplified. A coincidence circuit detects a coincidence in the two secondary windings within 5 μs and yields a logic pulse. This logic pulse is gated with a pulse generated by the signal in the primary providing the primary pulse meets the requirements necessary to be identified as an x-ray event, and providing the System Busy Bistable was not busy processing a previous event. The output of the Gate will mark the analyzed event as a horizontal coincidence event for future scrutiny.

Anticoincidence Logic

Some brief references were made earlier in this report on the Anticoincidence or Guard Layer of the detector. We shall now attempt to describe this portion of the system in more detail.

The guard layer, as Fig. 3 indicates, is a sequence of cells which surrounds the detector active area on three sides. As in any other cell of the detector, a signal is obtained from the guard layer whenever an event ionizes the gas within a guard cell. This signal is amplified and fed to a threshold detector. The threshold detector yields a pulse which is applied to a 5 μs pulse generator (Fig. 39). This pulse is then applied to all the Analog Card upper and lower lever Threshold Detector Shut Gates inhibiting their outputs. It is therefore apparent that an event will be totally rejected if a coincidence exists with the guard layer. Since a high rate of guard pulses could, in theory, reject many acceptable events, it was desired to monitor their average rates. This is done by also feeding the threshold detector output to a pair of rate discriminators (Fig. 40). The rate discriminators time constant are so adjusted as to yield an output whenever a rate has been exceeded. The rate fluctuations are monitored in Word 33 of the telemetry format.

Presently, the time constants of the rate discriminators are such that it will flag the telemetry bit when the average rates exceed 1 K events/sec and 10 K events/sec. The Anticoincidence card is shown in Fig. 41.

Eight Channel Commutator

Fig. 42 shows an eight channel commutator. The commutator is recycled every eight data frames and monitors the low level threshold

events of Detectors A & B. The commutator output is fed to a 5 bit register (Scaler I') of the encoder. This register is read out in Word 33 of the telemetry format. To prevent the recycling of the Scaler I' register, an overflow detector will inhibit rates above the count of 31 per frame.

An I.D. is provided in the commutated read-out to indicate the starting sequence. (See Fig. 5)

Housekeeping Monitor Circuits

During sounding rocket flights, the aerodynamic friction raises the payload skin temperature. The experiment, which is somewhat isolated from the skin is monitored by five temperature sensors. The locations of the sensors were chosen so as to obtain the best temperature distribution profile during flight.

Each sensor (Fig. 43) consists of five diodes connected in series, the cathode connected to ground, the anode is connected to a mercury cell whose other terminal is connected to the input of an operational amplifier. The operational amplifier is referenced to ground. As the temperature changes, the conduction of the diode varies. This variation causes a small change from the reference at the input of the operational amplifier. The amplifier gain is adjusted so to give a 0 to 5 volts dc linearly related to a temperature change of -20°C to +60°C.

The amplifier outputs are connected to the housekeeping data commutator whose output modulates the housekeeping transmitter.

The operational amplifier and the reference mercury cell are located in the System Monitor Card (Fig. 43).

A small mercury cell is used as a reference voltage source for monitoring any deviations of the Low Voltage Converter - 3.25 volt output (Fig. 63). The operational amplifier gain is adjusted so as to give a +5 volt swing for a one-volt change at the input. The voltage monitor output is connected to the housekeeping data commutator.

The System Monitor Card includes also a resistive network required to monitor the shutter of the aspect cameras. Whenever a camera shutter opens, a short circuit develops across the flash terminals of the cameras. The flash terminals of each camera are connected to a resistor which has 4.5v applied across it. When the shutter opens, the resistor is shunted to ground and the voltage across the resistor drops to zero. A current limiting resistor in series with the shunted resistor prevents the voltage source from being overloaded. A full time telemetry channel of the housekeeping transmitter monitors each camera status. The camera circuits will be described in more detail later.

Encoder

Figure 30 shows a system block diagram of the Encoder. The Encoder ripple counter is being driven by the 1.6 MHz crystal controlled oscillator (Fig. 44) in the Analog to Digital Conv. card. Outputs from the ripple counter are gated to provide the necessary timing pulses required to shift, set, reset, transfer & clear the data registers and flip-flops. The Encoder contains separate registers for the ADC pulse train, Scaler II, Scaler I & I' and a 17 bit shift register which is continuously shifted at the end of each word bit. The seventeenth bit in the register is required as a time domain buffer which compensates for the propagation

delay of the ripple counter and reflected in the transfer pulses. It will be noted that the transfer from the data registers into the shift register occur during the first half bit of each word, the remaining half bit is required to clear the registers. During the transfer and clear operations, the register inputs are inhibited. In word 1, i.e. the sync word, the word 1 transfer pulse enables the word 1 parallel gate into the shift register which is serially shifted to the output as NRZ code. This code is then converted to the Manchester code as a PCM signal to the transmitter.

In word 33, the word 33 transfer bit will transfer the Scaler I & I' registers and the anti rate flag gates in parallel with the shift register. The word 33 reset pulse will clear the registers.

In words 2-32 and 34-64 the transfer pulse goes directly to the Scaler II parallel gates. However, the transfer pulse must go through the ADC word ready memory before transferring the PHA Scaler, I.D. and Mark Bit. It was described earlier, that an X-ray event must be completely processed before transfer occurs. The "end of pulse train bit" from the ADC card indicates completion of processing an event, and enables the ADC word ready memory gate mentioned above. Once the gate is enabled the transfer pulse will transfer the ID, PHA and Mark Bit gates in parallel to the shift register for readout. The reset pulse is also conditional to the state of the ADC word ready memory gate described above. The reset pulse clears the PHA, ID & Mark Bit registers and also resets the System Busy Bistable Flip-Flop and the ADC Bistable Flip-Flop.

To prevent the system from hanging up due to a missed reset signal, an unconditional set and reset signal is generated at the beginning and end of word 1 & 33, respectively. Because of the unconditional reset, any data stored in the PHA, ID & Mark Bit register is erased. It was stated earlier, that, the only information in word 2 and 34 is the Scaler II rates.

Construction

The Electronic System consists of 20 3.5" x 6" cards interconnected by a harness. The electronic circuits consist mostly of discrete component modules arranged in cordwood fashion (Fig. 58). The module interconnections within the card is accomplished by a multilayer welded matrix and shielded conductors.

Low power DTL integrated circuits and some RTL circuits are being used in this system. The flat packs are arranged on flat sticks interconnected by a multi-layer welded matrix (Fig. 59).

VI. CAMERA CIRCUITS

Mounted on each detector and looking parallel to the collimator sight angle is a Nikon F camera using Tri-X film for photographing star field pictures. These pictures confirm the accuracy and position of the ACS pointing.

There is a separate 12 volt battery pack in the experiment section for powering the camera advance and rewind functions.

The start for the camera circuits consist of supplying a +28 volts through the Haydon timer to the coil of relay K1 (Fig. 60); backup start is applied to relay K4 by the ACS system. The closure of the relay contacts supplies +12 volts from the camera batteries to the contacts

of camera drive relays K2 and K3. A continuous clock pulse from the Encoder is applied to the 9046 input gate which was enabled by the +12 volts zenered to 5 volts. The second gate of the 9046 is used for pulse inversion before being applied to the 9040 binary circuits. The remaining gates (3 and 4) of the 9046 integrated circuit are used to insure that the flip-flops always start in a given position after voltage is applied. The two binaries are used as a divide by three stage which drive the camera relays with a 2.62 second pulse every 7.86 seconds (Fig. 61). Since gates 3 and 4 always start the circuit in the same position, the first pulse out will be a shutter pulse to Camera "B". After 2.62 seconds the Camera "B" shutter closes and immediately rewinds, at the same time Camera "A" shutter opens for 2.62 seconds. When Camera "A" shutter closes it rewinds, 2.62 seconds later Camera "B" is again given a shutter pulse and the sequence repeats continuously until the end of the film roll.

VII. HIGH VOLTAGE

The high voltage used on each detector is supplied by commercial high voltage supplies. Each supply is set away from the preamp section to minimize electromagnetic pickup by the sensitive preamplifiers. The high voltage is delivered to the HV distribution box via a potted raceway. The complete high voltage section is then potted to avoid corona.

Heavy filtering is done in the HV lines to eliminate ripple from the high voltage oscillator in the supplies (Fig. 62).

Power for the high voltage supplies is unregulated +28 volts from the instrumentation batteries. This is turned on by Haydon timers after burn-out.

Both detectors operate at a nominal 2100 volts.

VIII. WIRING

Figure 64 shows the inconnecting wiring harness for cards 1 through 6, connections for cards 7 through 16, plus 18 are shown on Figure 65. Figure 66 shows the interconnections for cards 17, 19, and 20 as well as the rocket interface connector and all housekeeping functions.

IX. TESTING

The main electronics and camera drive circuits are the same as flown on Aerobee flight 13.08. The circuits went through the normal Aerobee 170 qualification testing for vibration and vacuum corona checks as well as successful flight operation. In addition the electronic circuits have been temperature cycled from -10°C to +50°C.

Detector "A" is a new design which incorporates four detecting layers flown on 13.08. Detector B has one new detecting layer and new collimator.

The complete rocket payload will undergo the required vibration levels in the rocket payload minus the parachute section. In addition the experiment section will be corona checked in vacuum at T & E.

X. FLIGHT PROFILE

Figure 69 shows an estimate of altitude in feet versus time in seconds after liftoff based on a net payload weight of 500 pounds.

XI. EXPERIMENT TIMING

The following is a list of nominal times for critical experiment functions. Some times, such as severance, can only be determined after final rocket weight determination.

Time (from liftoff)	Function
T - 0	liftoff
T + 50 sec	booster burn-out
T + 55 sec	high voltage on
T + 105 sec	camera start
T + 110 sec	doors open
T + 315 sec (est.)	doors close (tone 3)
T + 320 sec	doors close (Haydon timer)
T + 322 sec. (est.)	severance (tone 7)
T + 330 sec.	severance (Haydon timer)

XII. WEIGHTS

The following is an estimate of experiment component weights plus total recoverable weight:

Experiment

Item	Weight (lbs.)
Detector "A"	50.0
Detector "B"	48.8
Main electronics (including harness)	28.9
Aspect cameras	6.6
Payload Rack	12.7
Camera batteries & drive circuits	3.0
Rocket skin (with balance weights)	90.0
Total experiment wt.	240.0

Net recoverable payload weight

Item	Weight (lbs)
Instrumentation Section	55.0
Experiment Section	240.0
ACS Section	88.0
Parachute Section	65.0
Est. net payload weight	448.0

Acknowledgments

We wish to thank the following people without whose help this rocket experiment would not exist. The main electronics were originally designed by Code 711 under the direction of C. Cancro (Cancro et al.) and we wish to thank them for what has proven to be an extremely reliable system.

Mr. F. Shaffer is gratefully acknowledged for his fine efforts in the mechanical design and drafting of the detectors and payload system.

References

Cancro, C. A., Crockett, W. R., Garrahan, N. M., McGowan, R. G., X-Ray Experiment Electronics for High Altitude Balloon and Rocket Flights, NASA, GSFC Document No. X-711-68-74, 1968.

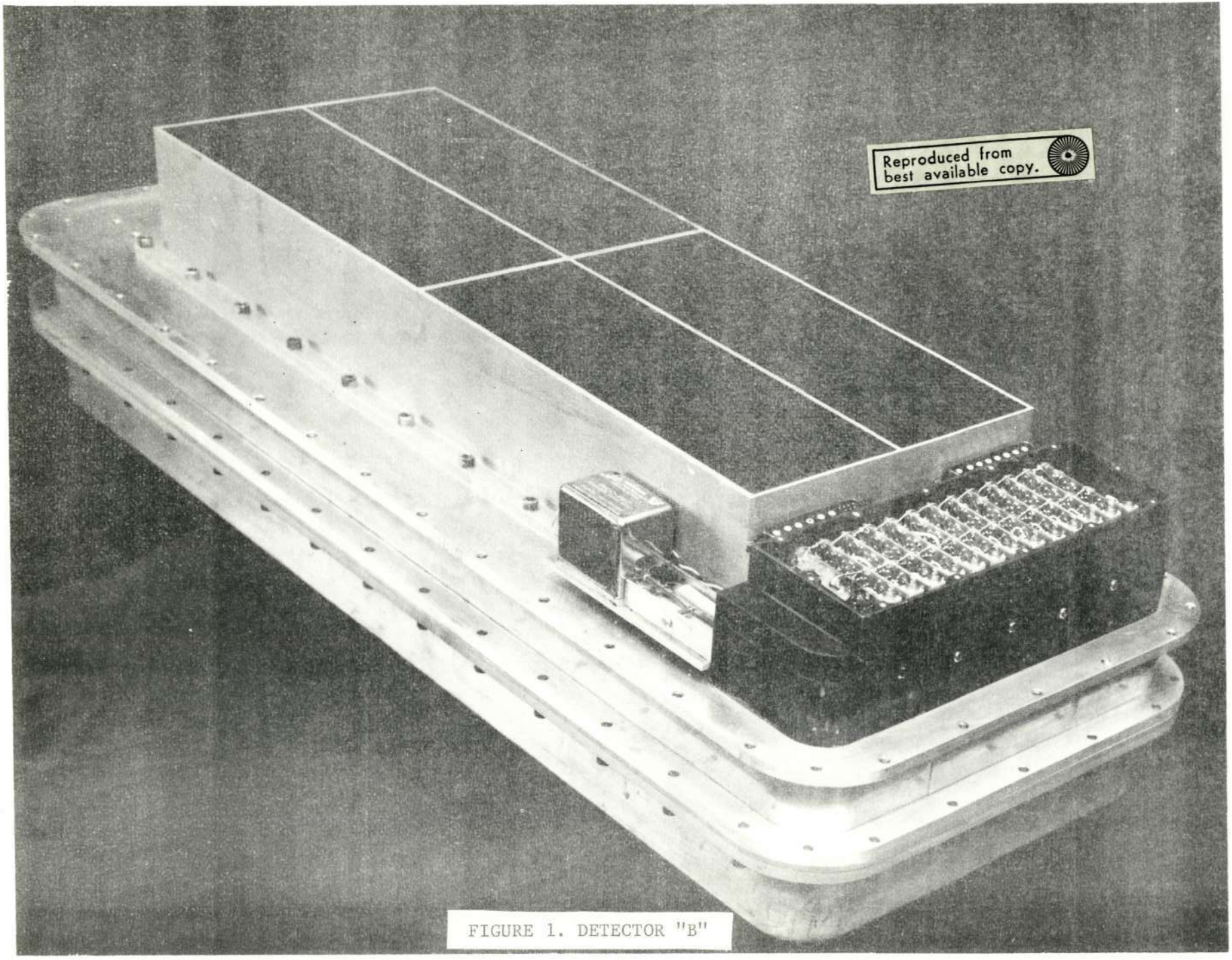


FIGURE 1. DETECTOR "B"

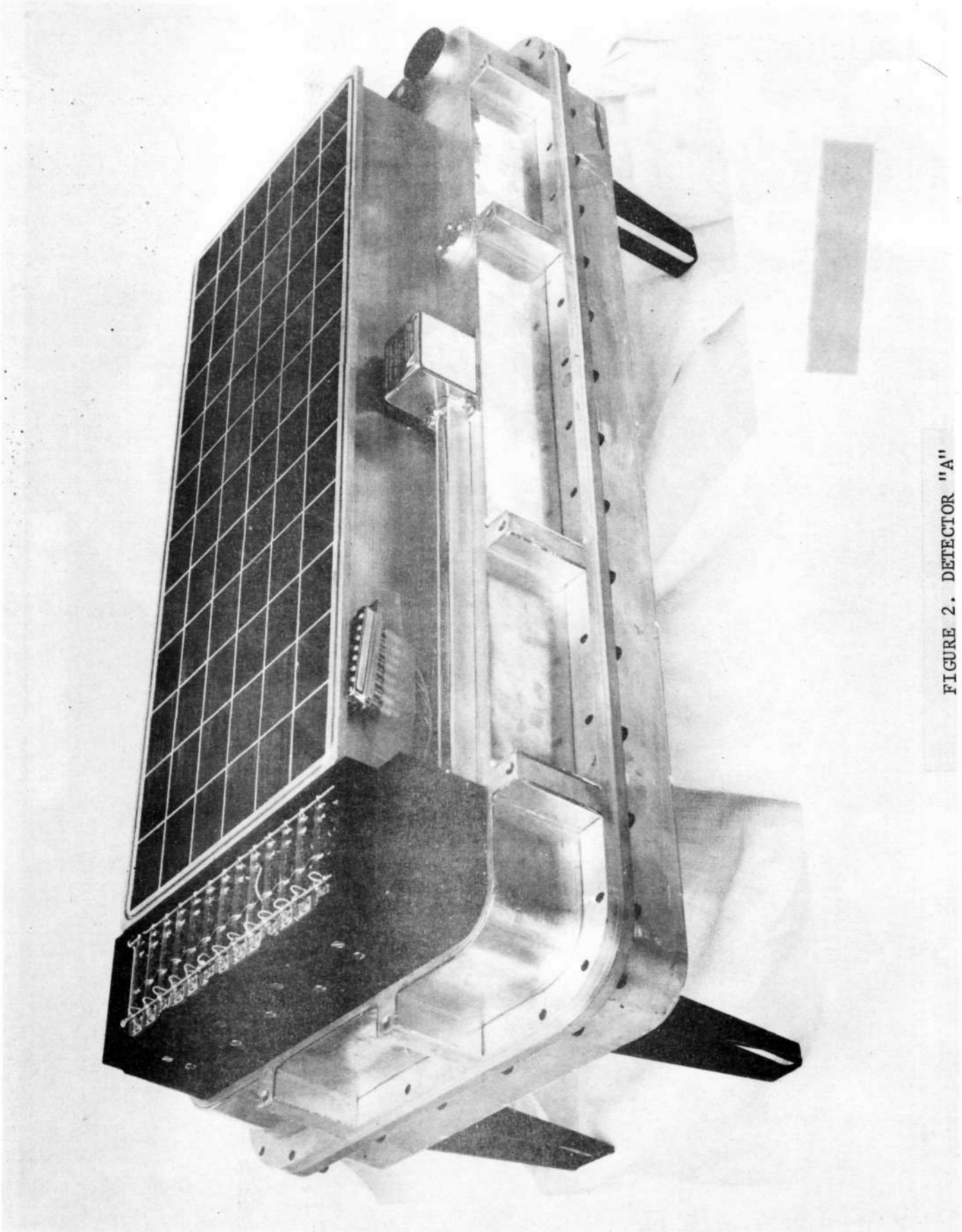
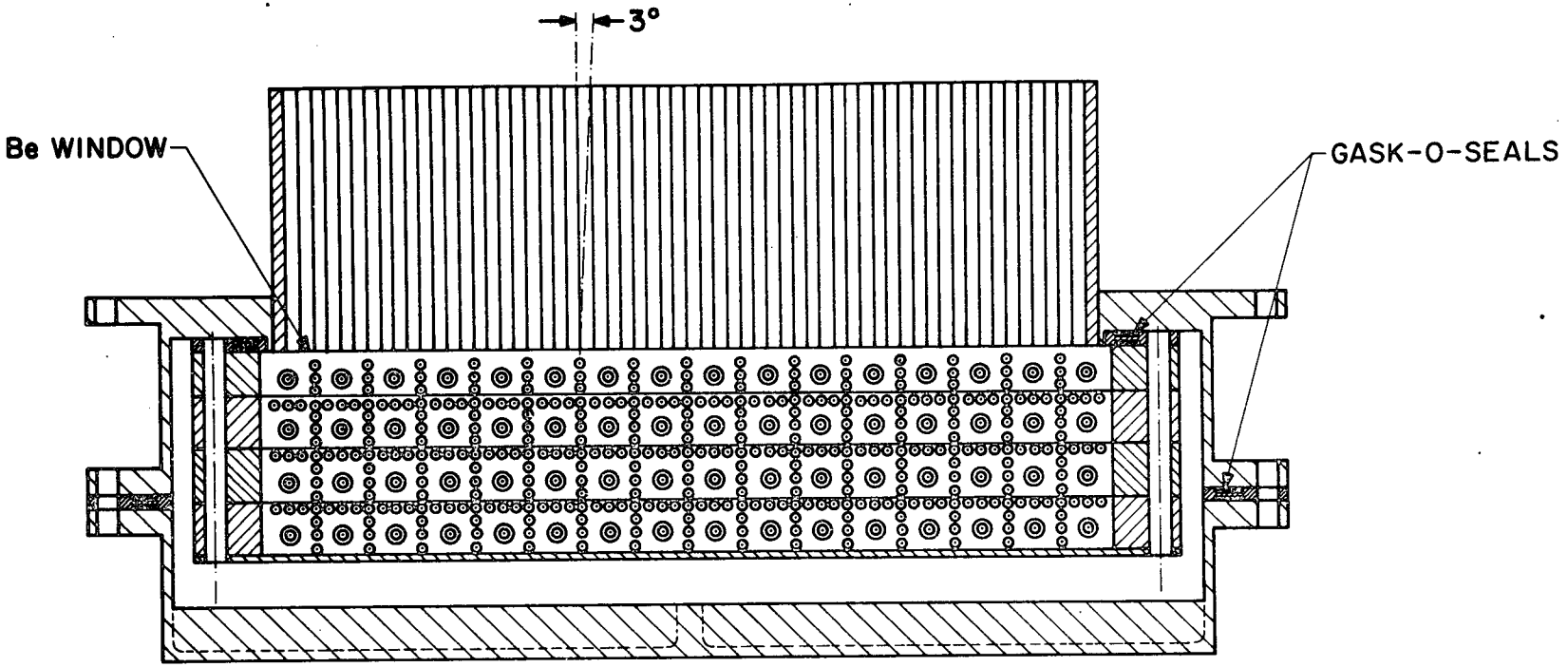
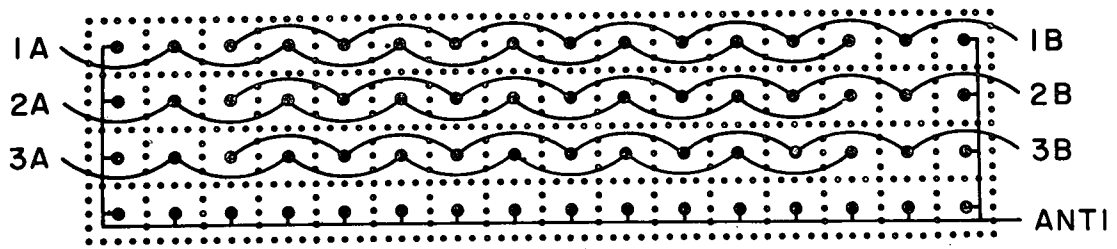


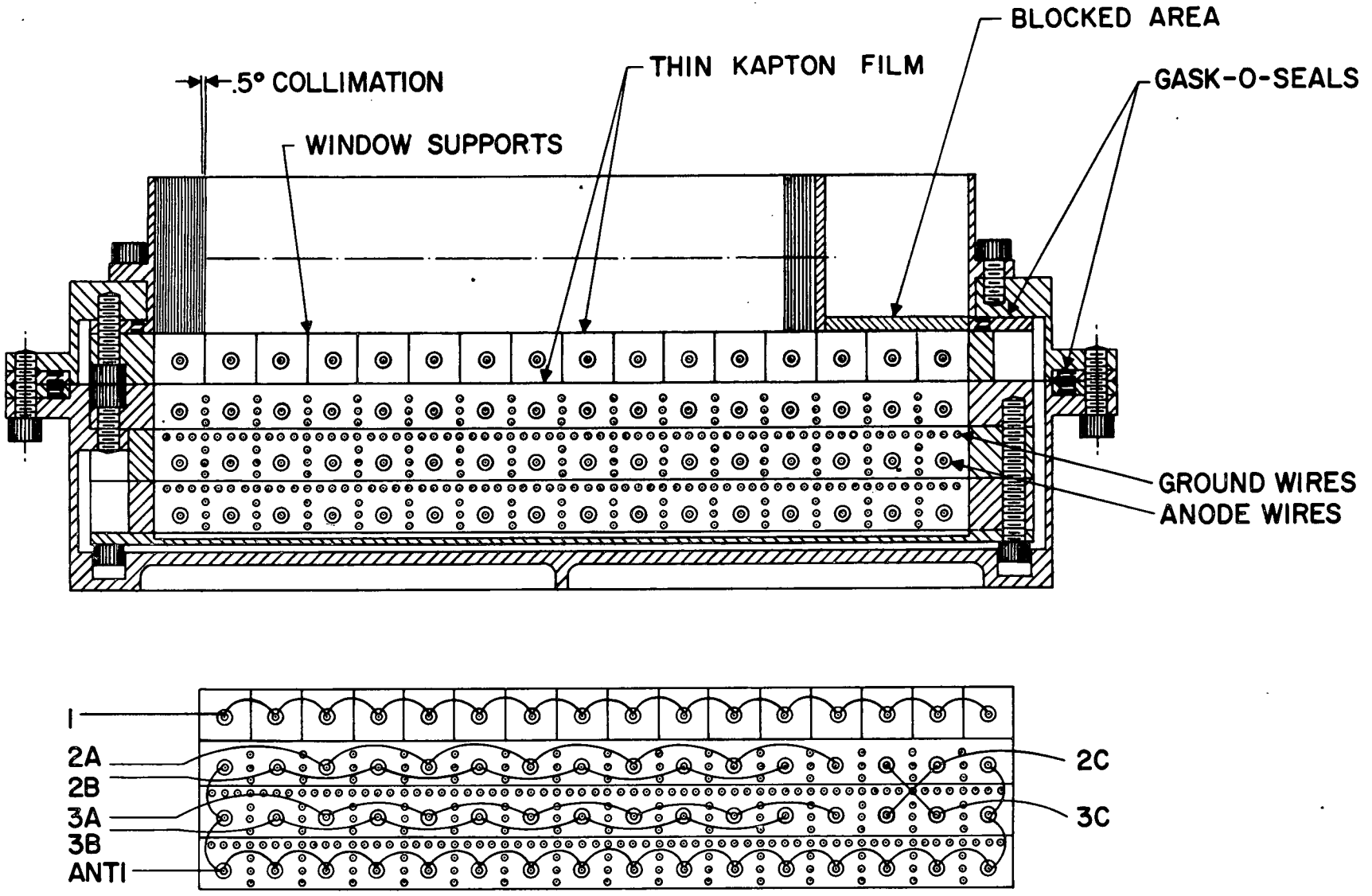
FIGURE 2. DETECTOR "A"





SCHEMATIC DIAGRAM AND

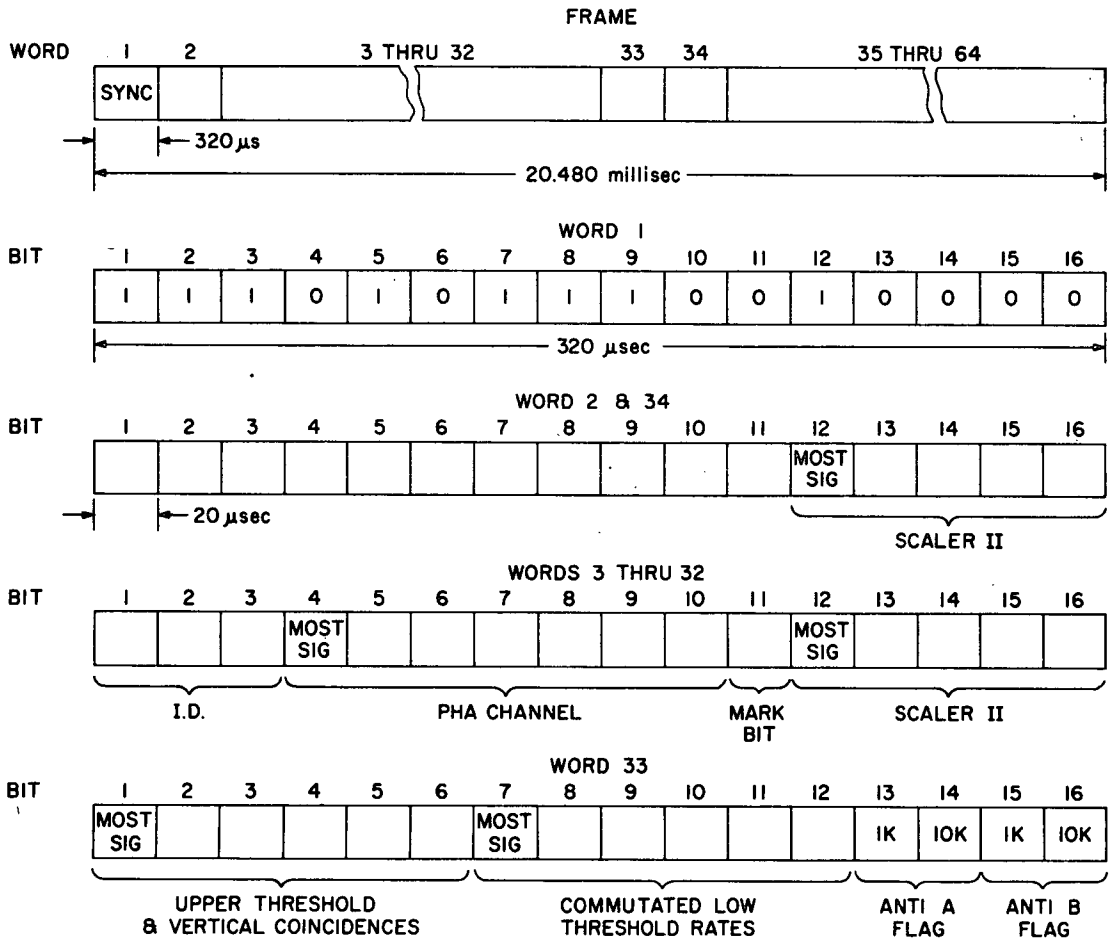
FIGURE 3. SIGNAL HANDLING TECHNIQUE DETECTOR "B"



SCHEMATIC DIAGRAM AND SIGNAL HANDLING TECHNIQUE

DETECTOR "A"

FIGURE 4.



I.D. CODE			
LAYER	BIT 1	2	3
A1	0	0	1
A2	0	1	0
A3	0	1	1
A2/3	1	0	0
B1	1	0	1
B2	1	1	0
B3	0	0	0

8 CHAN COMMUTATOR SEQUENCE						
LAYER	BIT 7	8	9	10	11	12
I.D.	1	0	0	0	0	1
B3						
B2						
B1						
A4						
A3						
A2						
A1						

FIGURE 5. TELEMETRY FORMAT

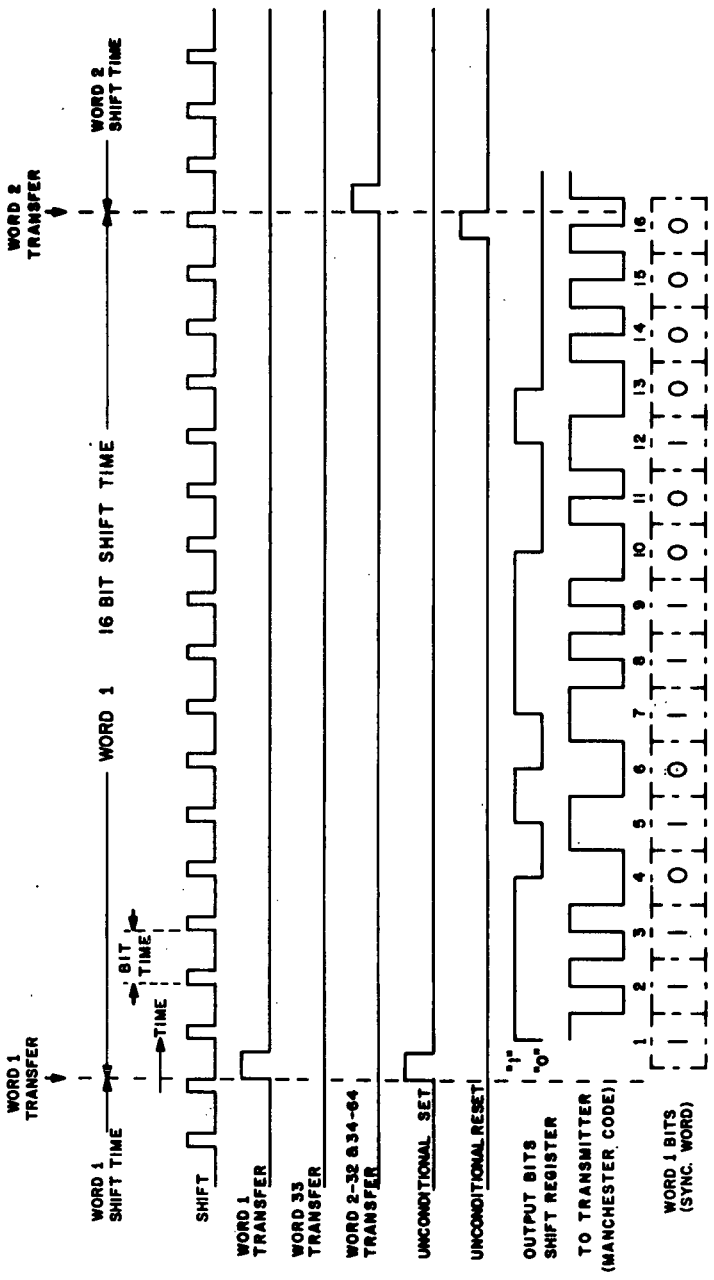


FIGURE 6. ENCODER SYNC WORD TIME WAVEFORM

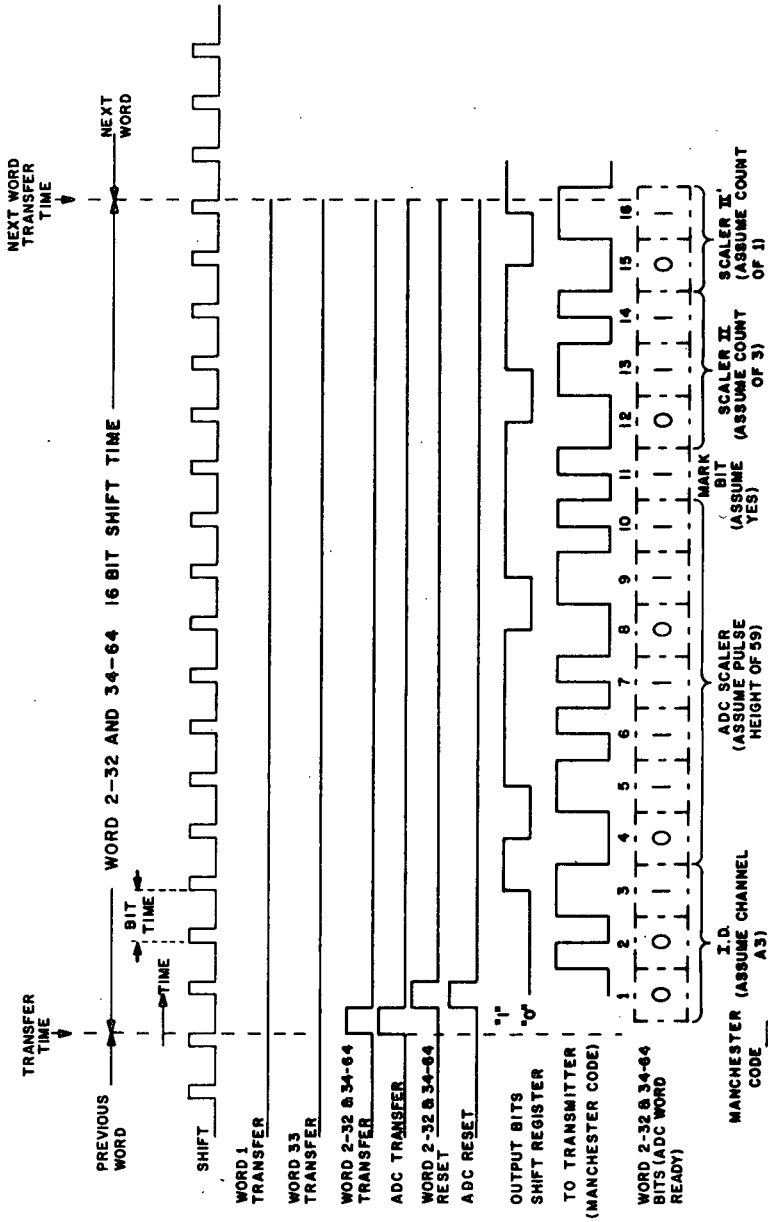


FIGURE 7. ENCODER WORDS 3-32 and 35-64 TIME WAVEFORMS, ADC WORD READY

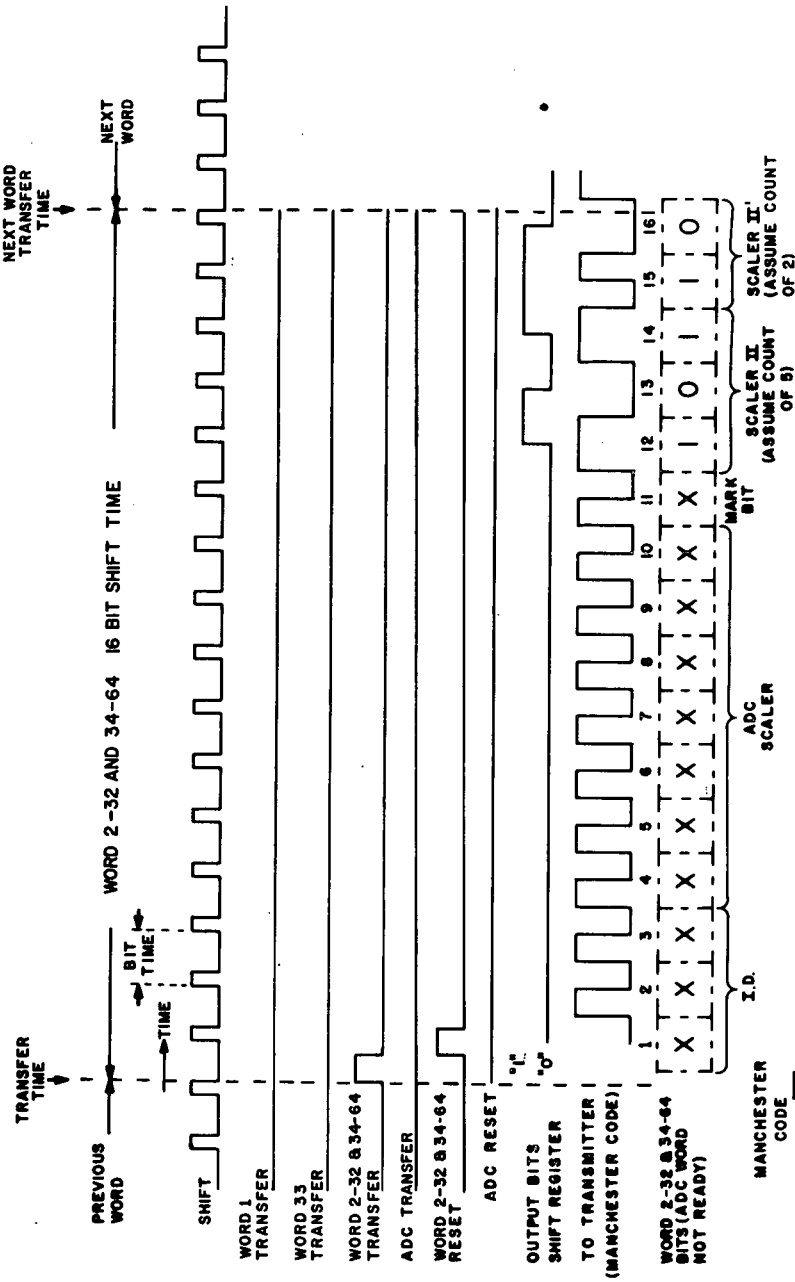


FIGURE 8. ENCODER WORD 3-32 and 35-64 TIME WAVEFORMS, ADC WORD READY

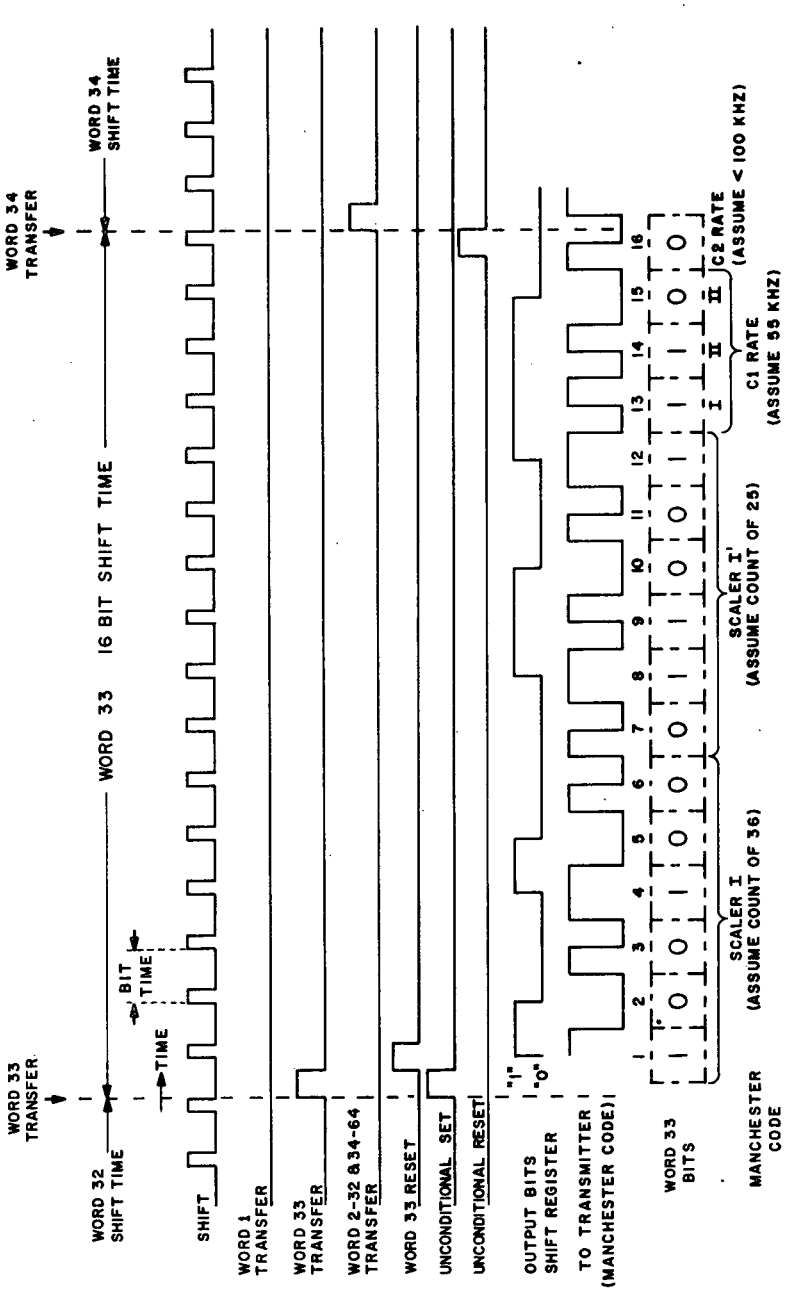


FIGURE 9. ENCODER WORD 33 TIME WAVEFORM

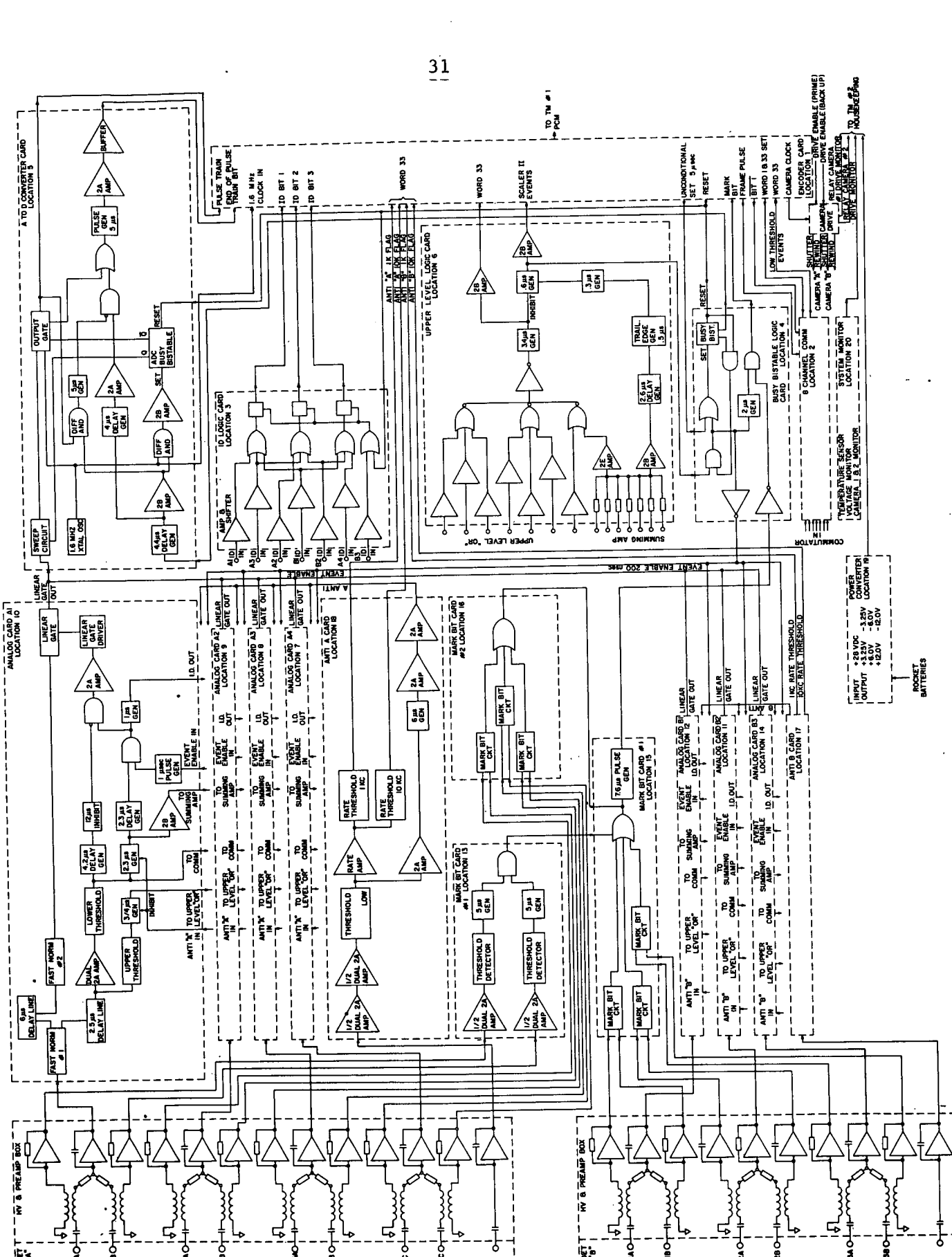


FIGURE 10. SYSTEM BLOCK DIAGRAM

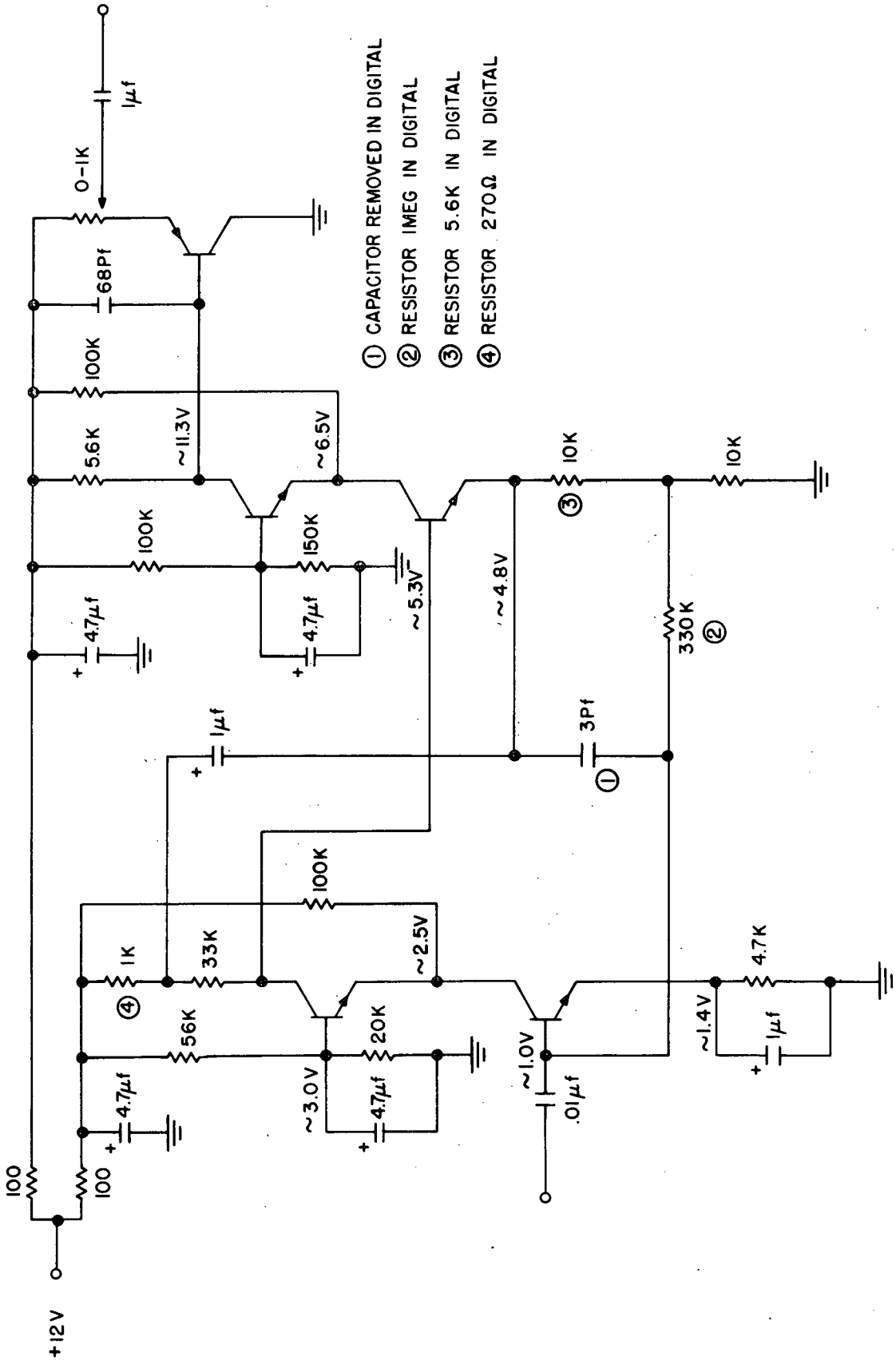


FIGURE 11. CHARGE-SENSITIVE AMPLIFIER

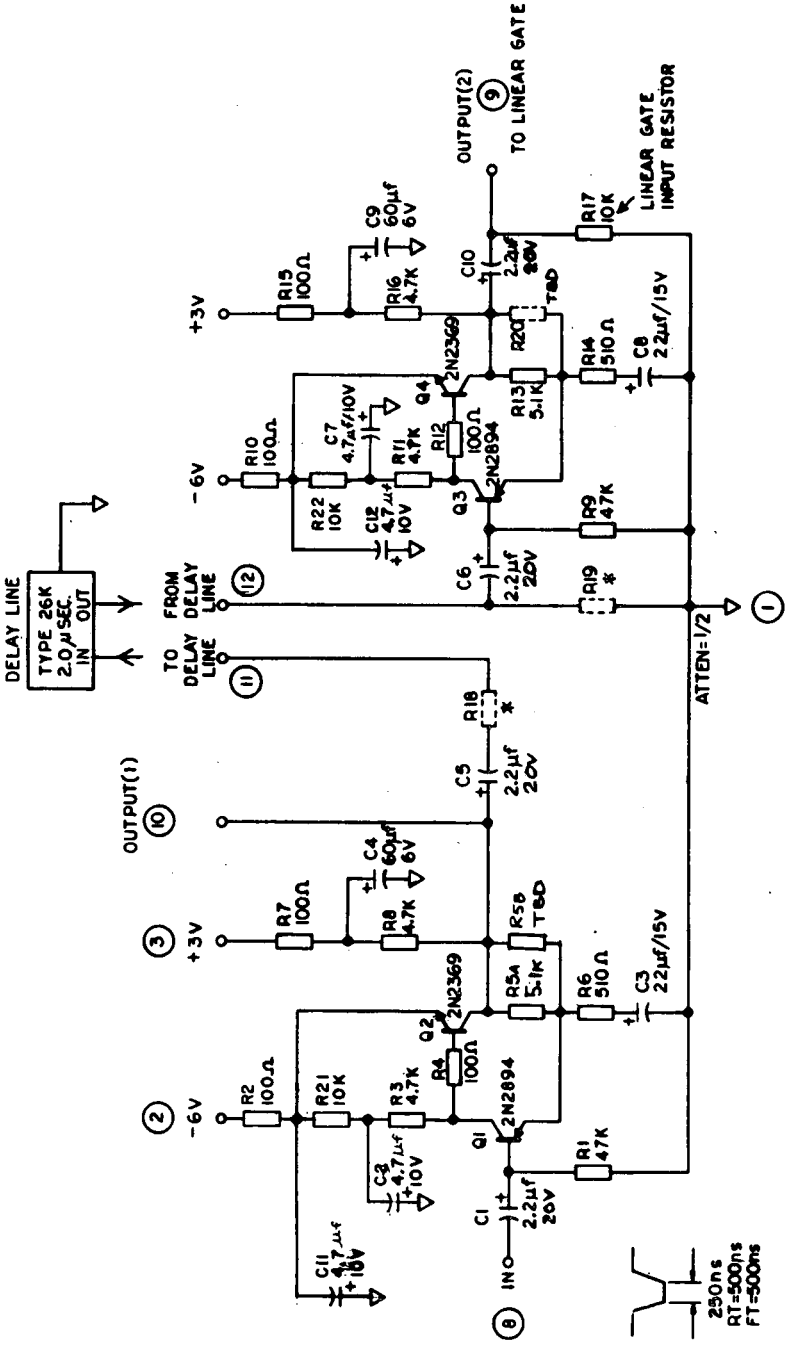


FIGURE 12. FAST NORMALIZER

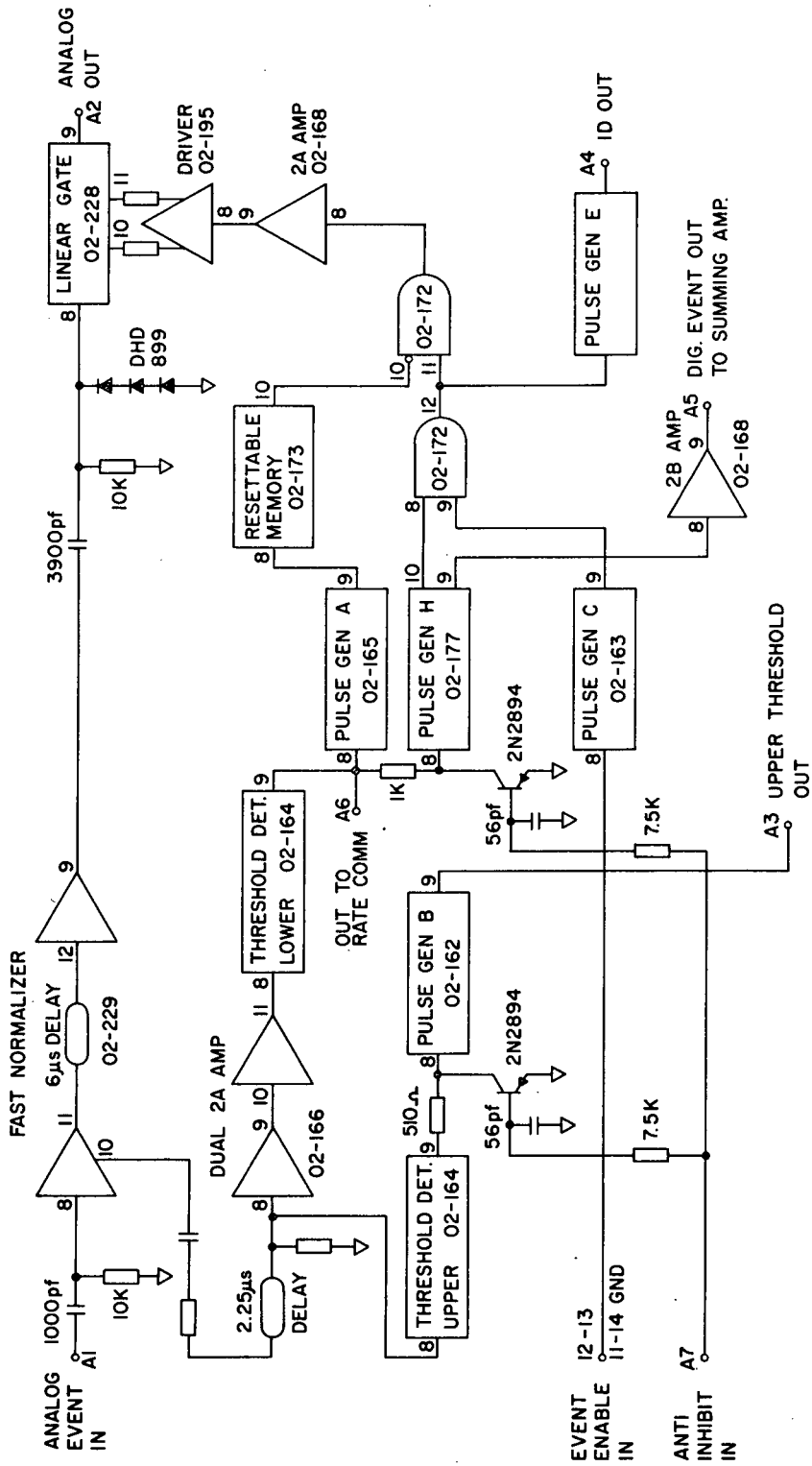


FIGURE 13. ANALOG CARD BLOCK DIAGRAM

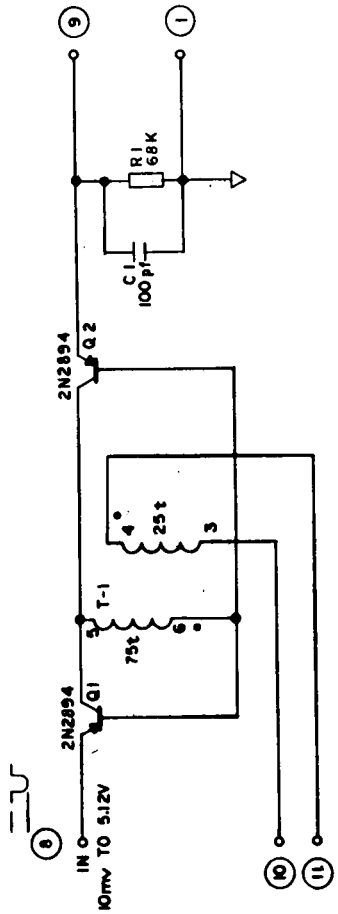


FIGURE 14. LINEAR GATE

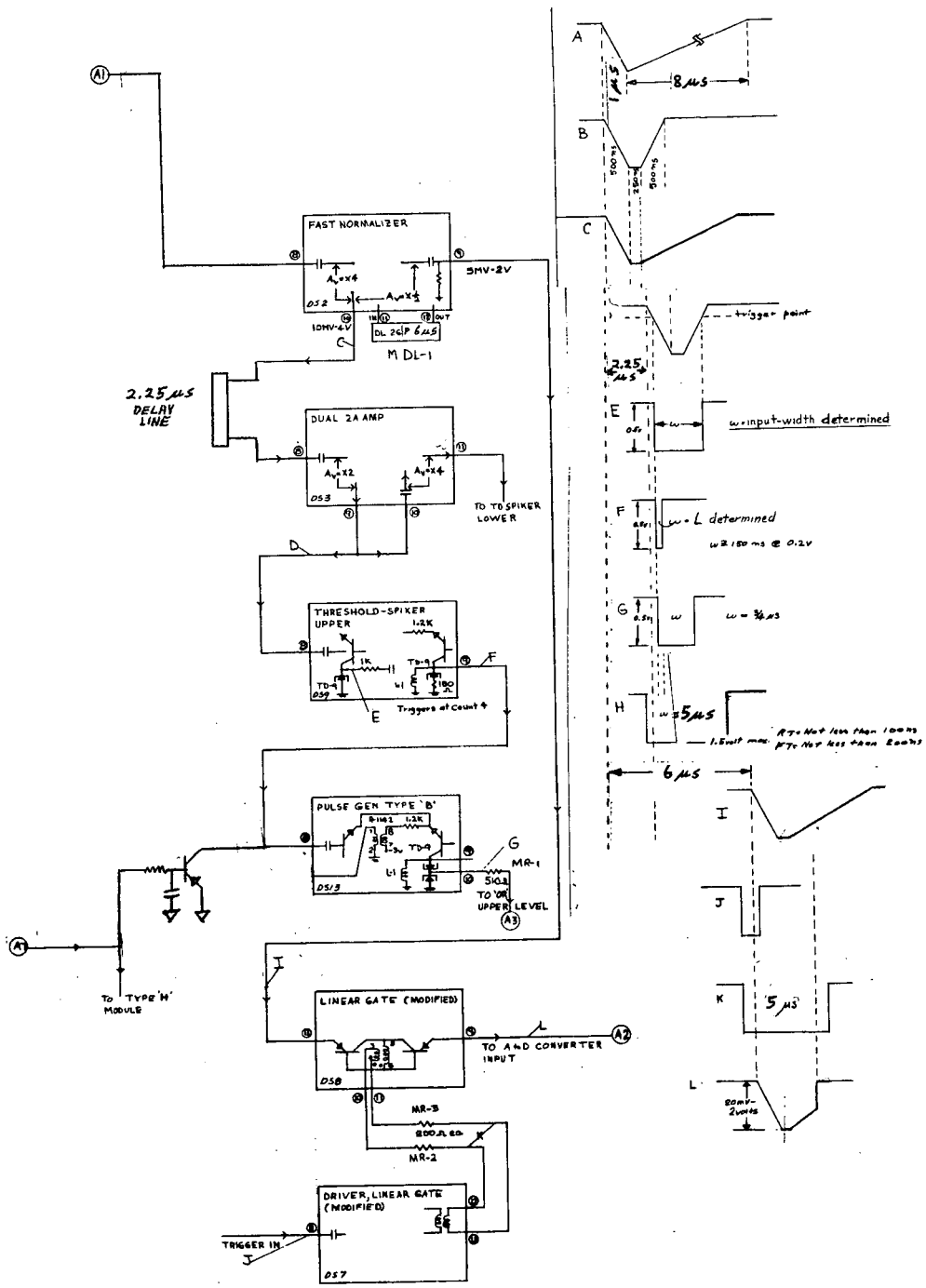


FIGURE 15. ANALOG CARD LINEAR CHAIN TIMING WAVEFORMS

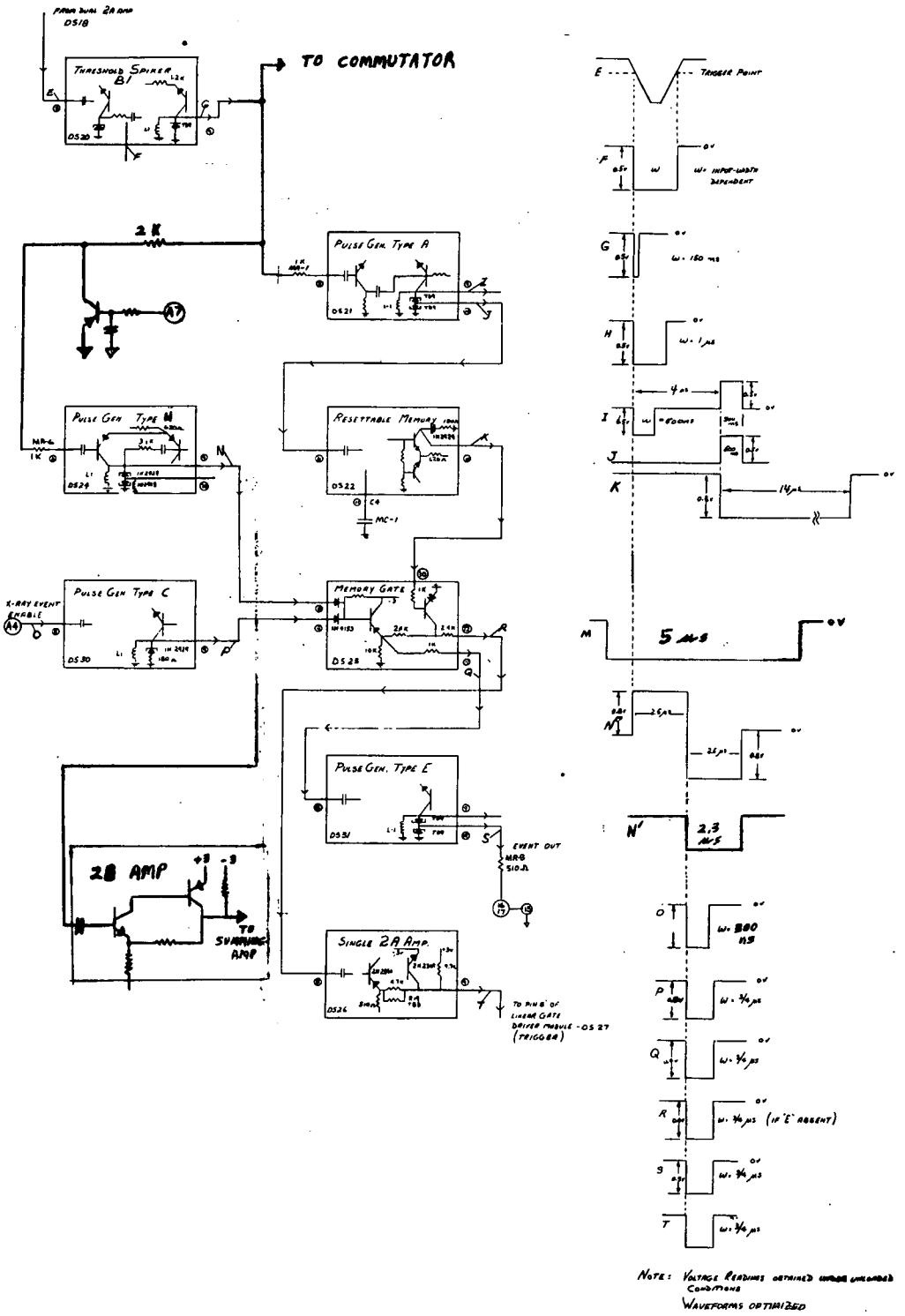


FIGURE 16. ANALOG CARD LOGIC CHAIN TIMING WAVEFORMS

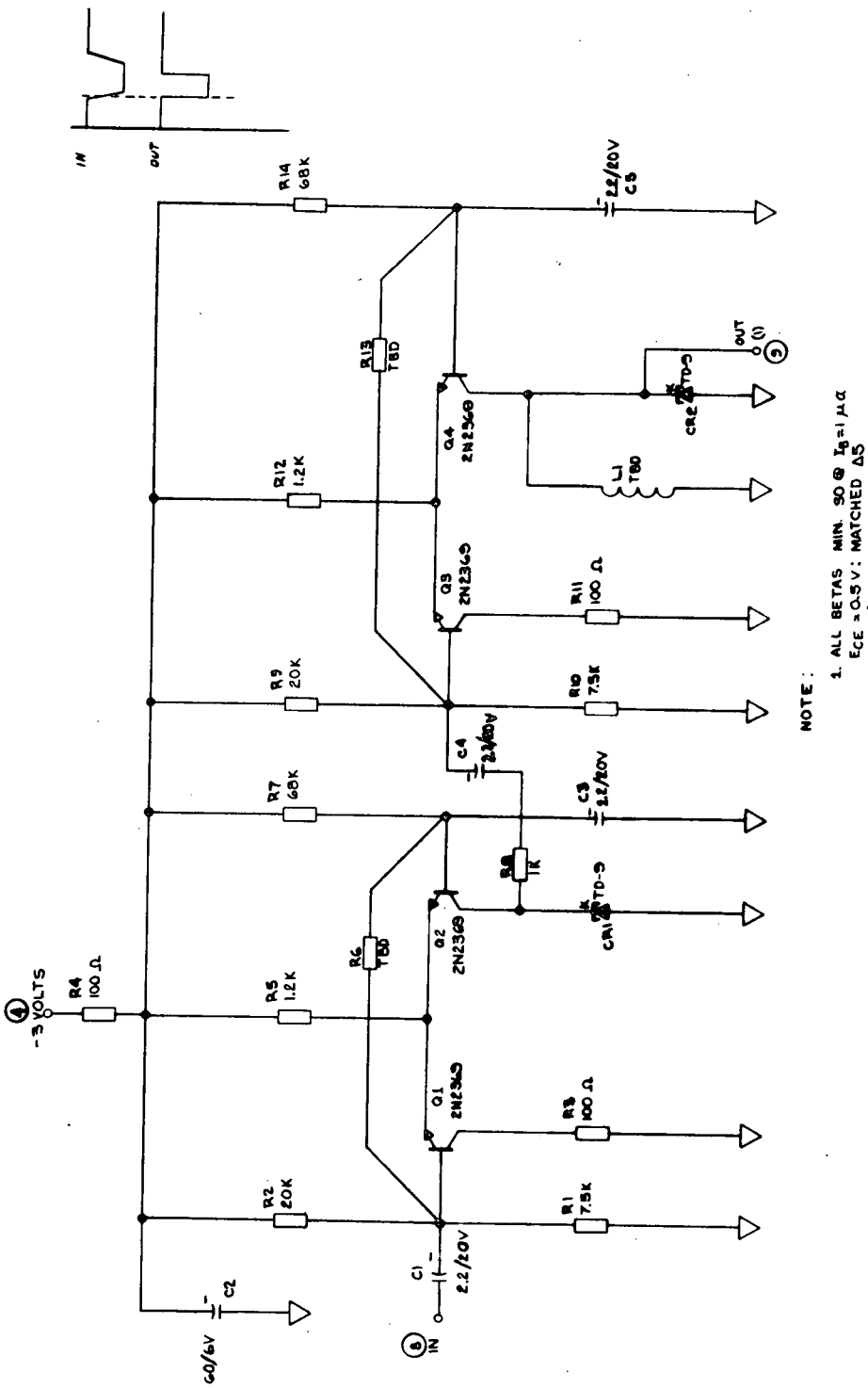


FIGURE 17. THRESHOLD DISCRIMINATOR

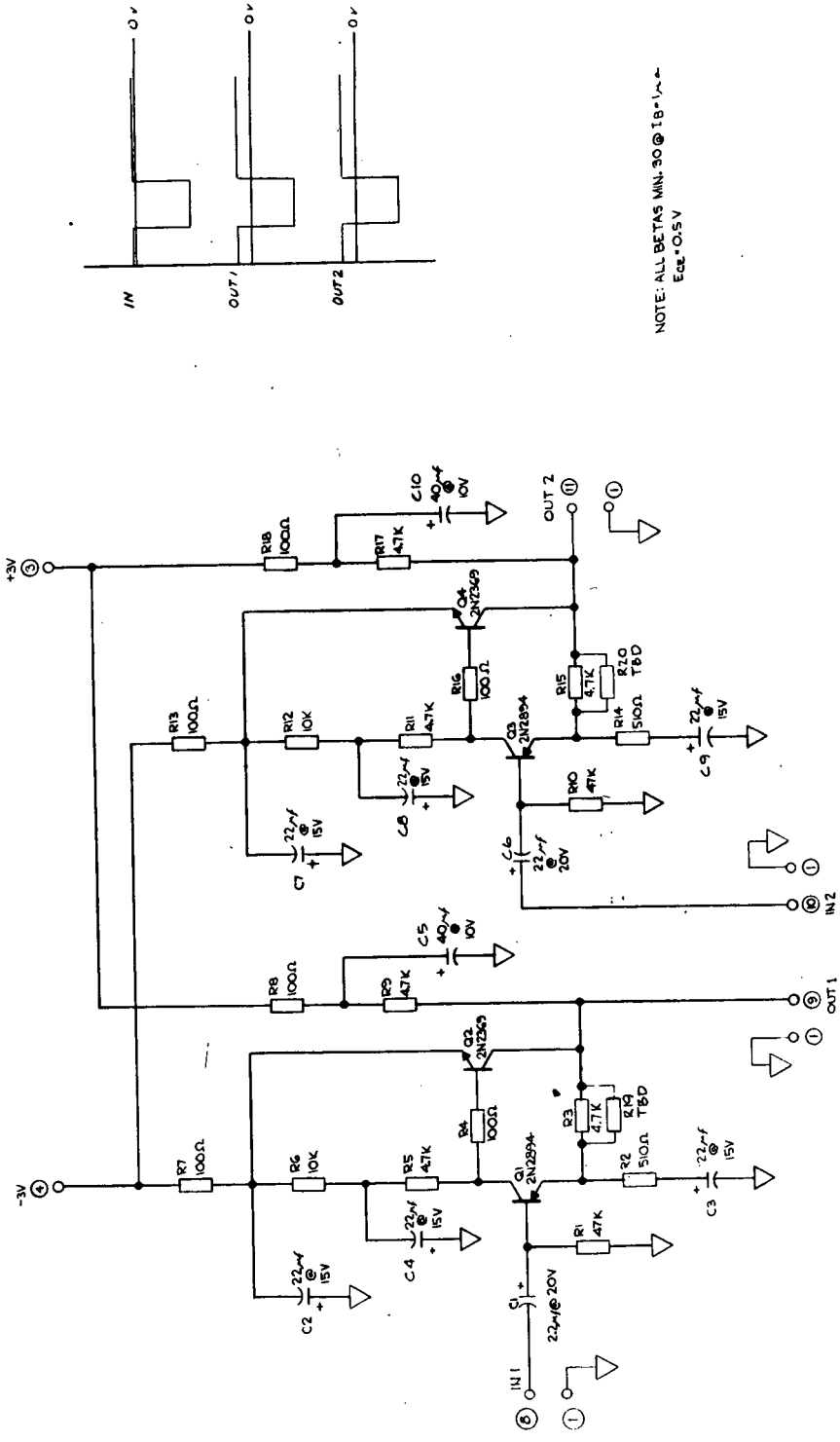


FIGURE 18. DUAL 2A AMPLIFIER

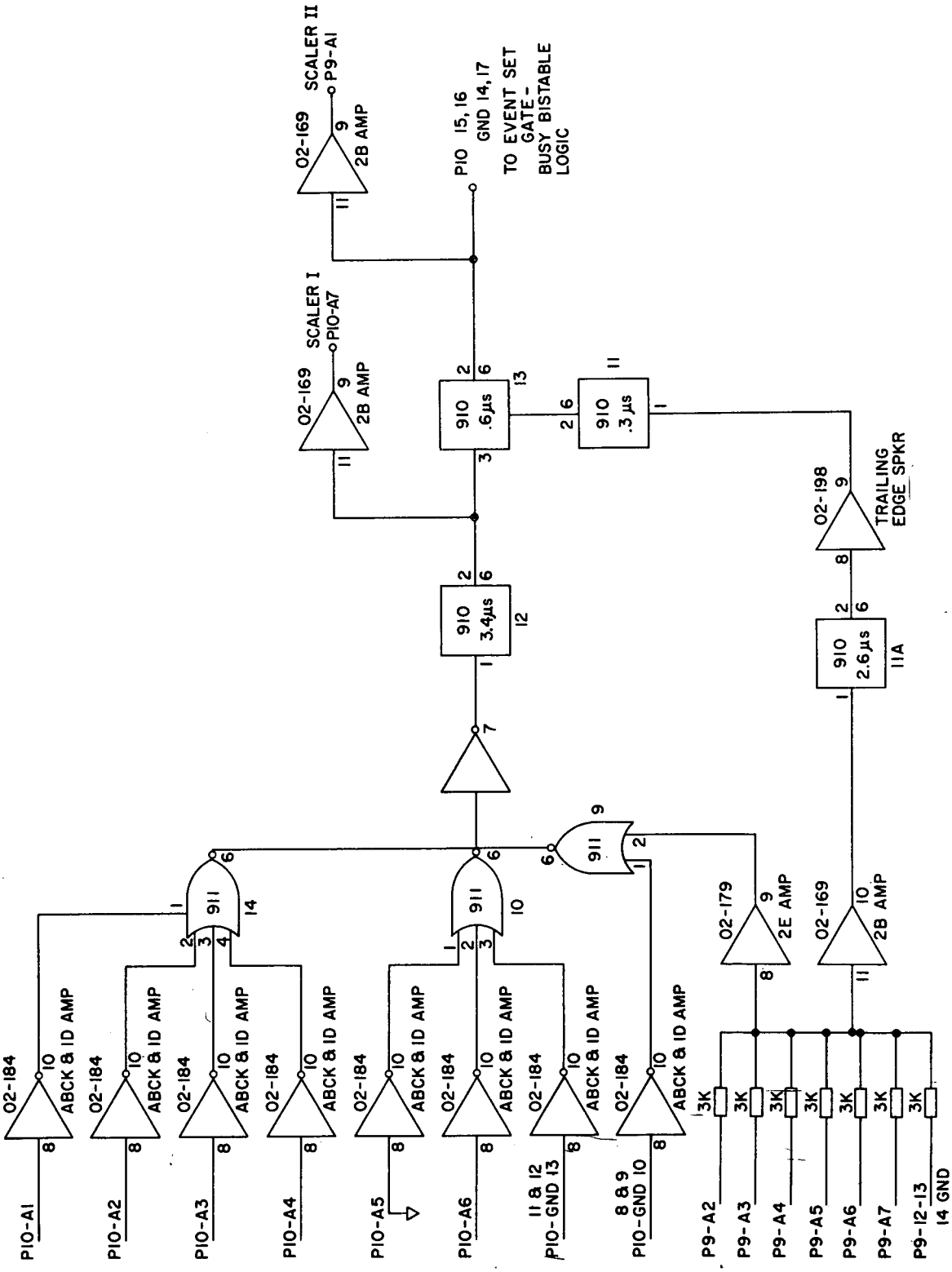


FIGURE 19. UPPER LEVEL LOGIC CARD

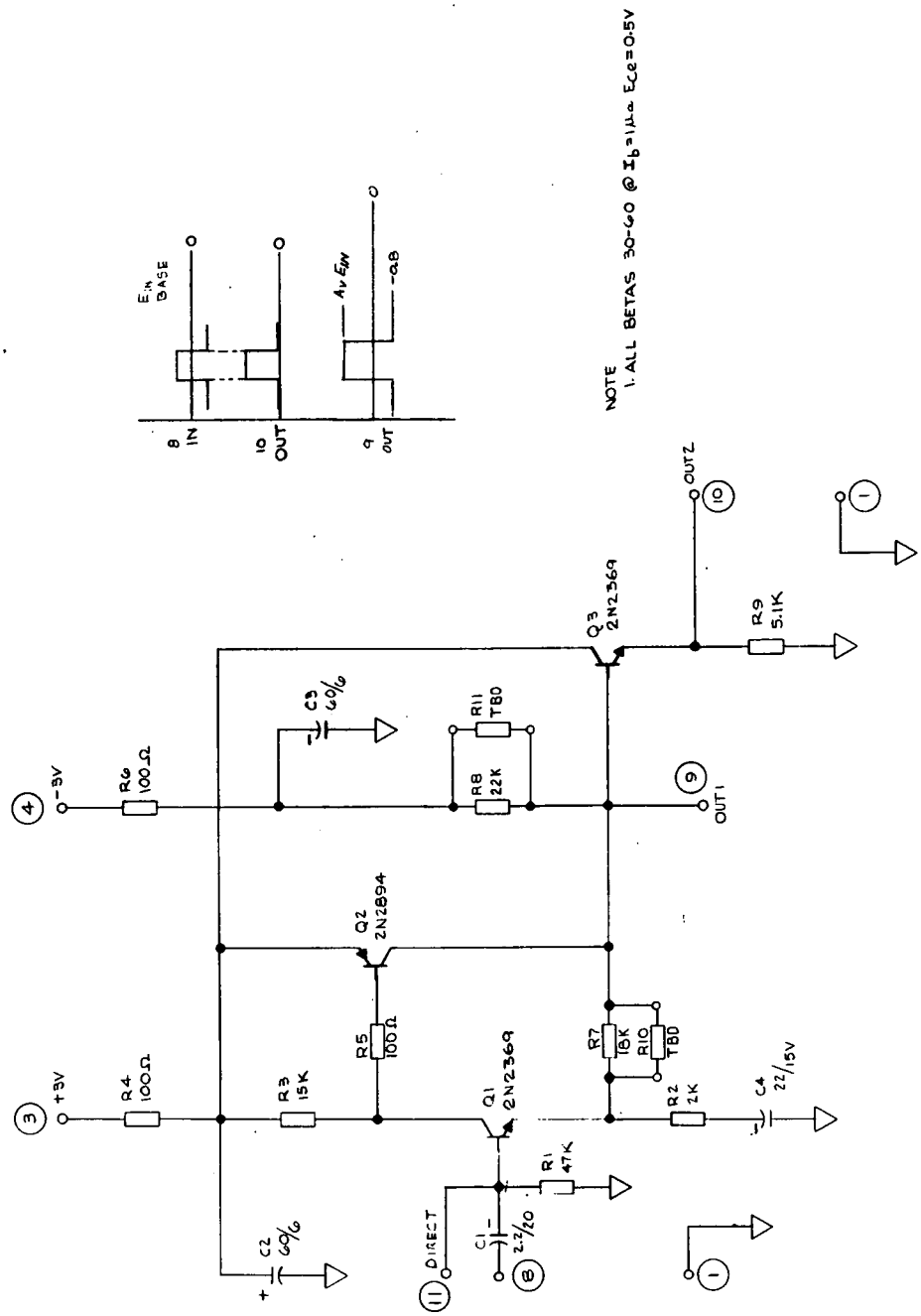


FIGURE 20. 2B AMPLIFIER

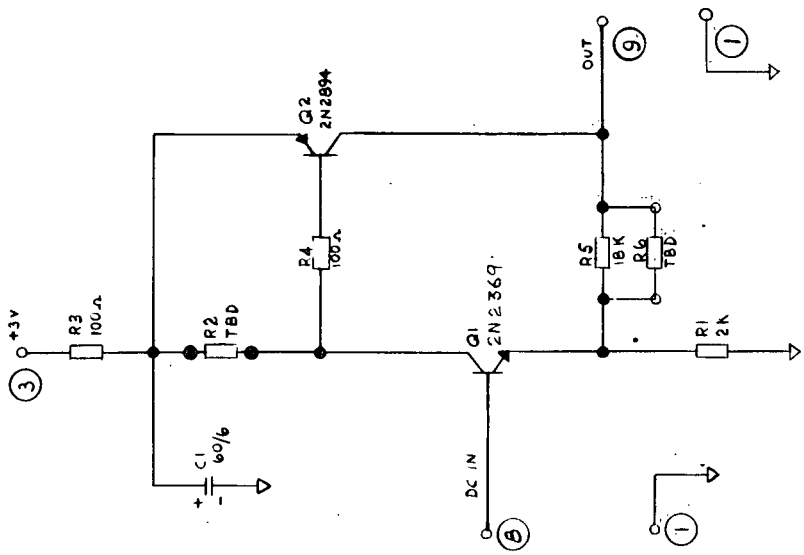


FIGURE 21. 2E AMPLIFIER

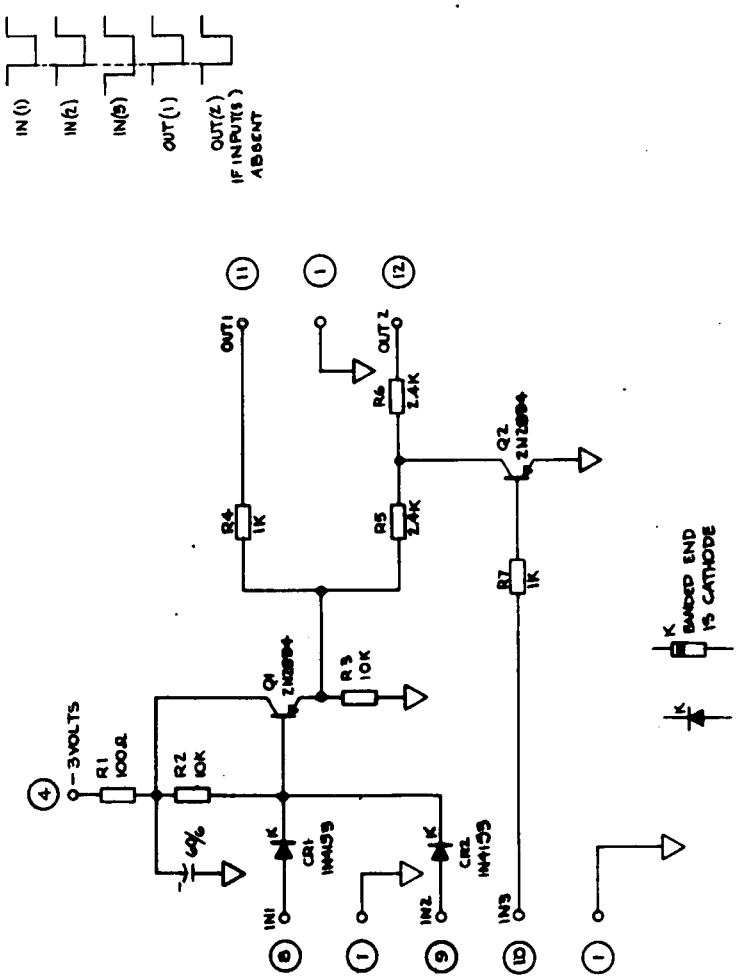


FIGURE 22. EVENT ENABLE GATE

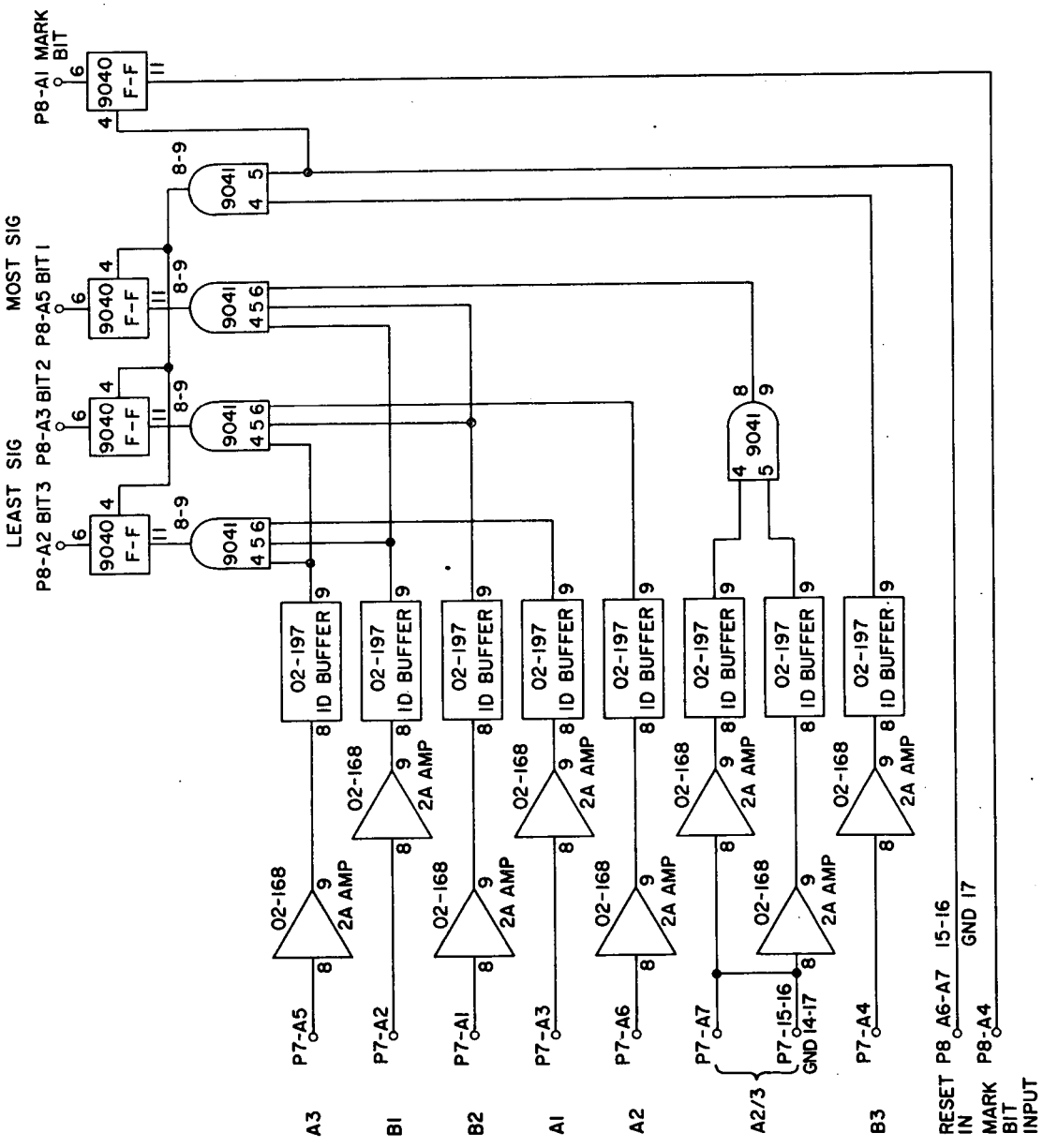


FIGURE 23. I. D. LOGIC CARD

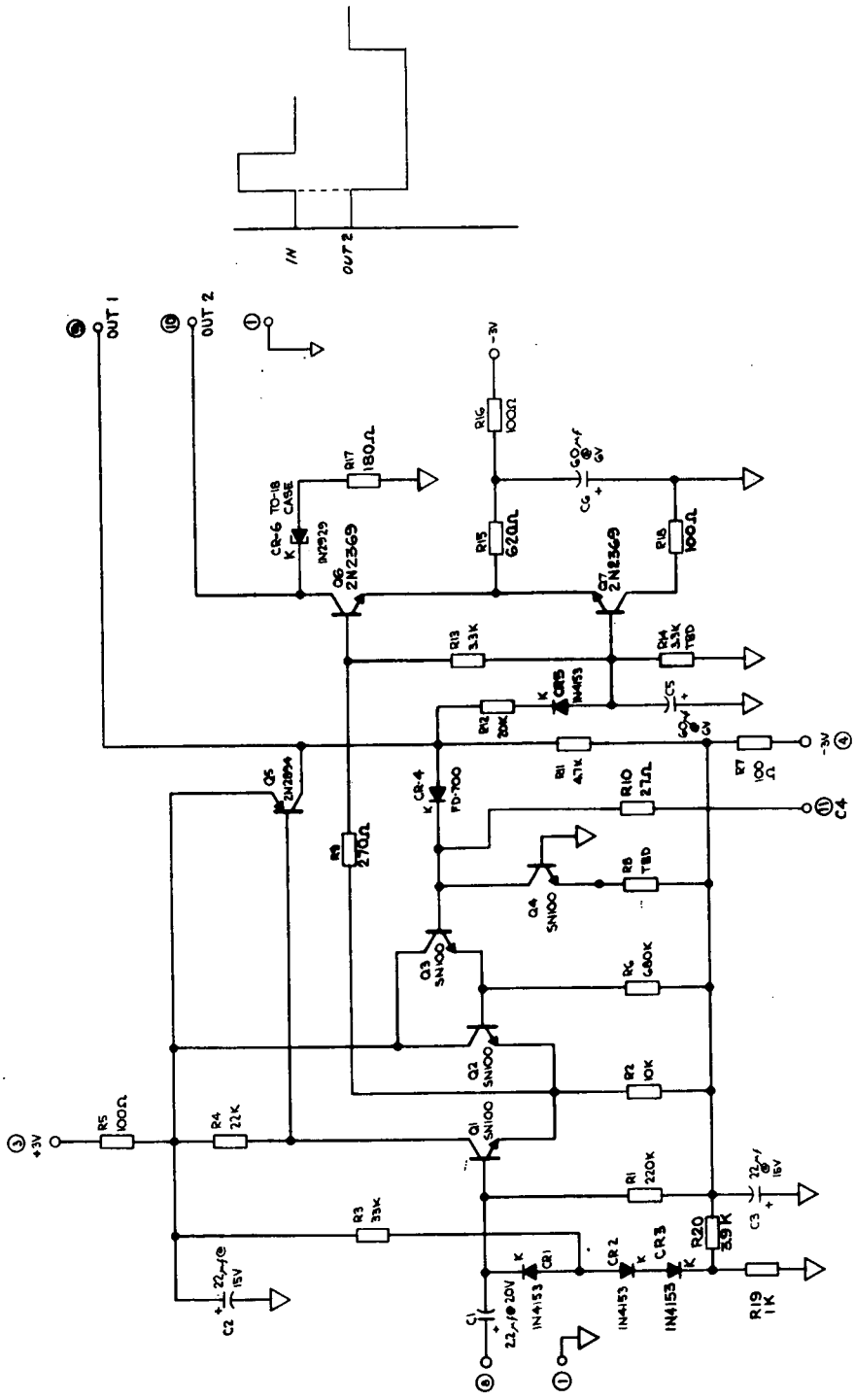


FIGURE 24. RESETTABLE MEMORY

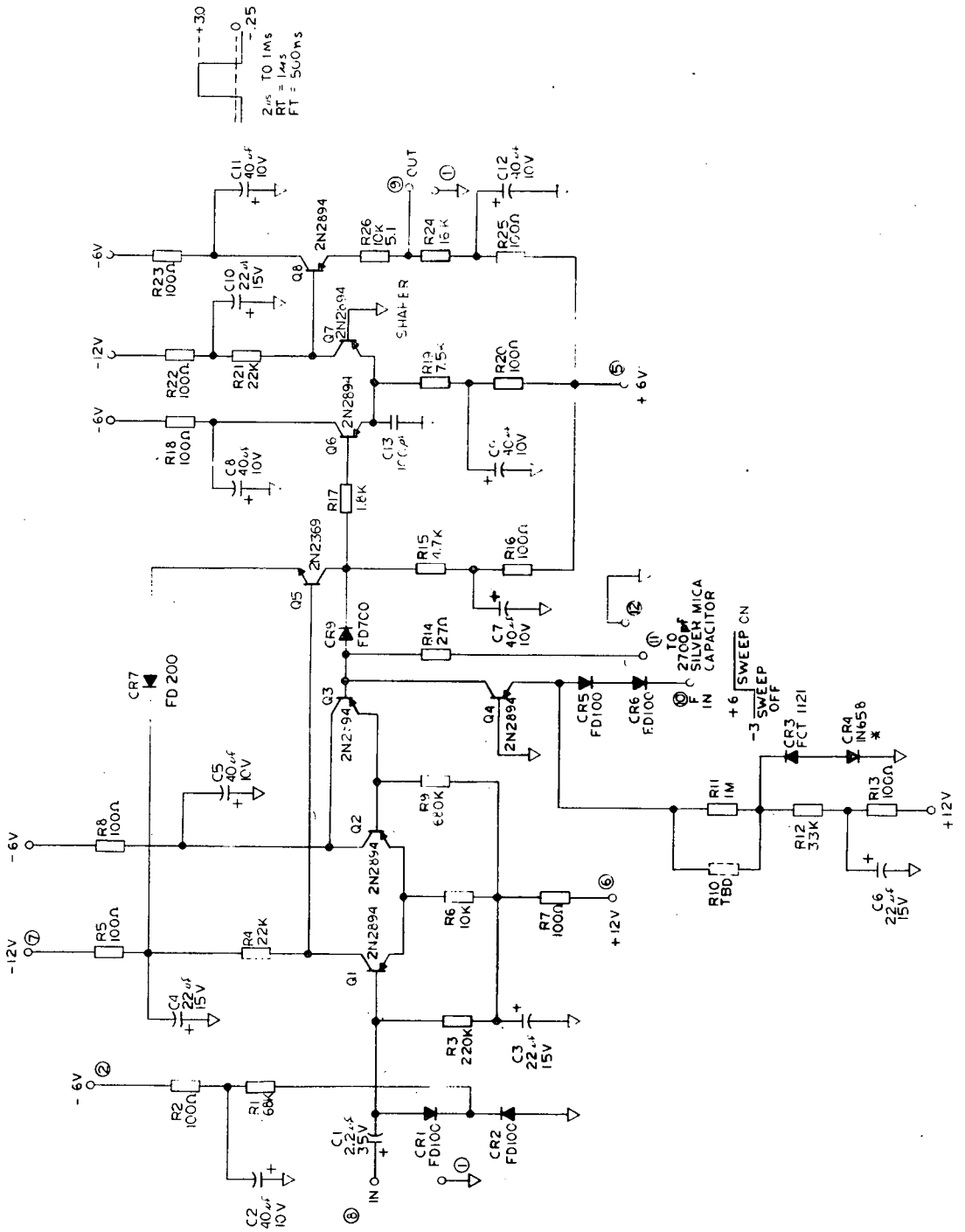


FIGURE 25. NANO-SECOND SWEEP

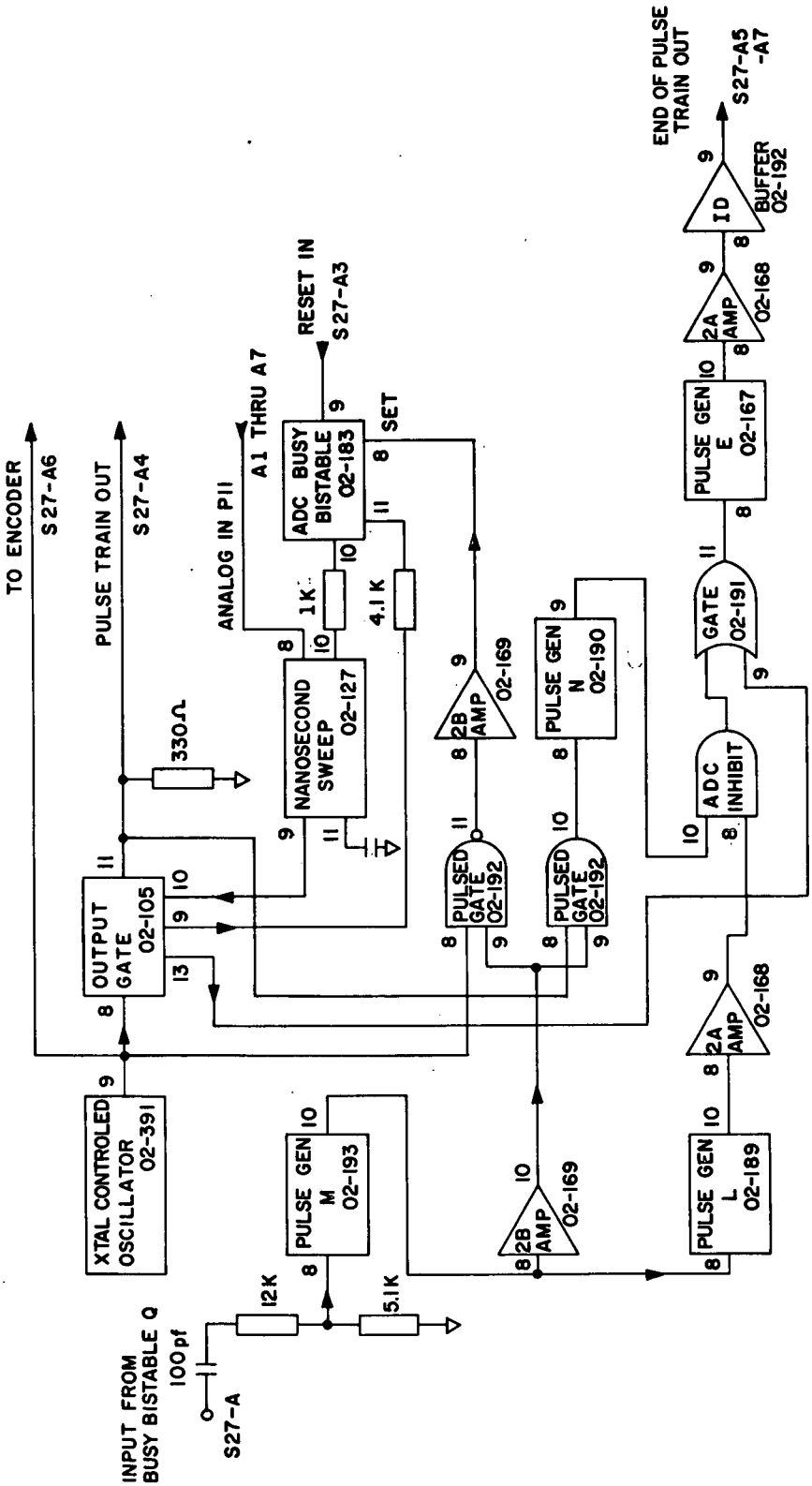


FIGURE 26. ANALOG TO DIGITAL CONVERTER CARD

① FINALLY THE 'ACCEPT' PULSE IS INITIATED AHEAD OF THE RESETTABLE MEMORY—WHICH MAY BLOCK THE LINEAR GATE— AN 'ACCEPT' PULSE MAY OR MAY NOT BE ACCOMPANIED BY A PULSE TRAIN.

② THE 'ACCEPT' PULSE IS ALSO FED TO THE LINEAR CHANNELS 'A' THRU 'K' TO THE EVENT ENABLE INPUT. THE 2.5μs DELAY ALLOWS TIME FOR LOGIC SWITCHING TO UNBLOCK LINEAR GATE. THE +2.5μs WIDTH ENSURES THE CAPTURE OF AT LEAST ONE OSC. 0.625 μs COUNT.

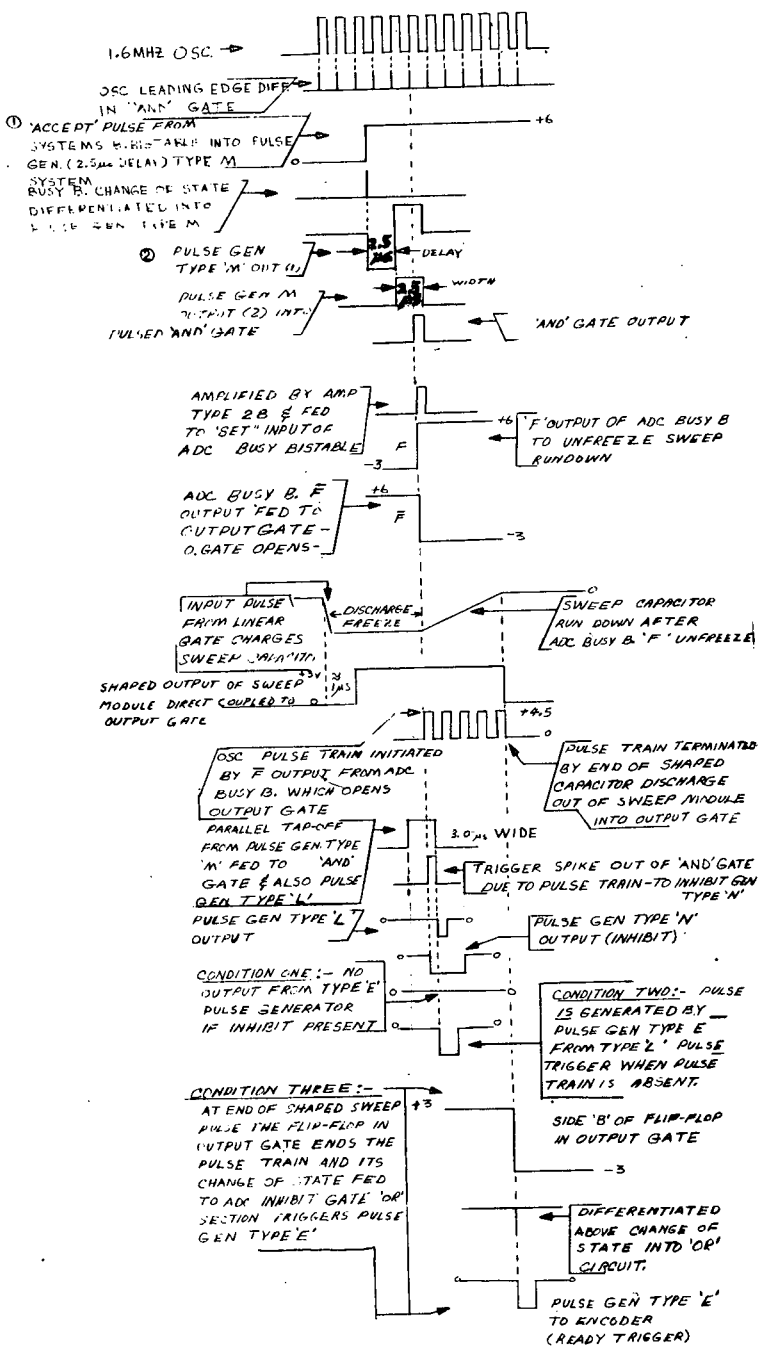


FIGURE 27. ANALOG TO DIGITAL CONVERTER SYSTEM WAVEFORMS

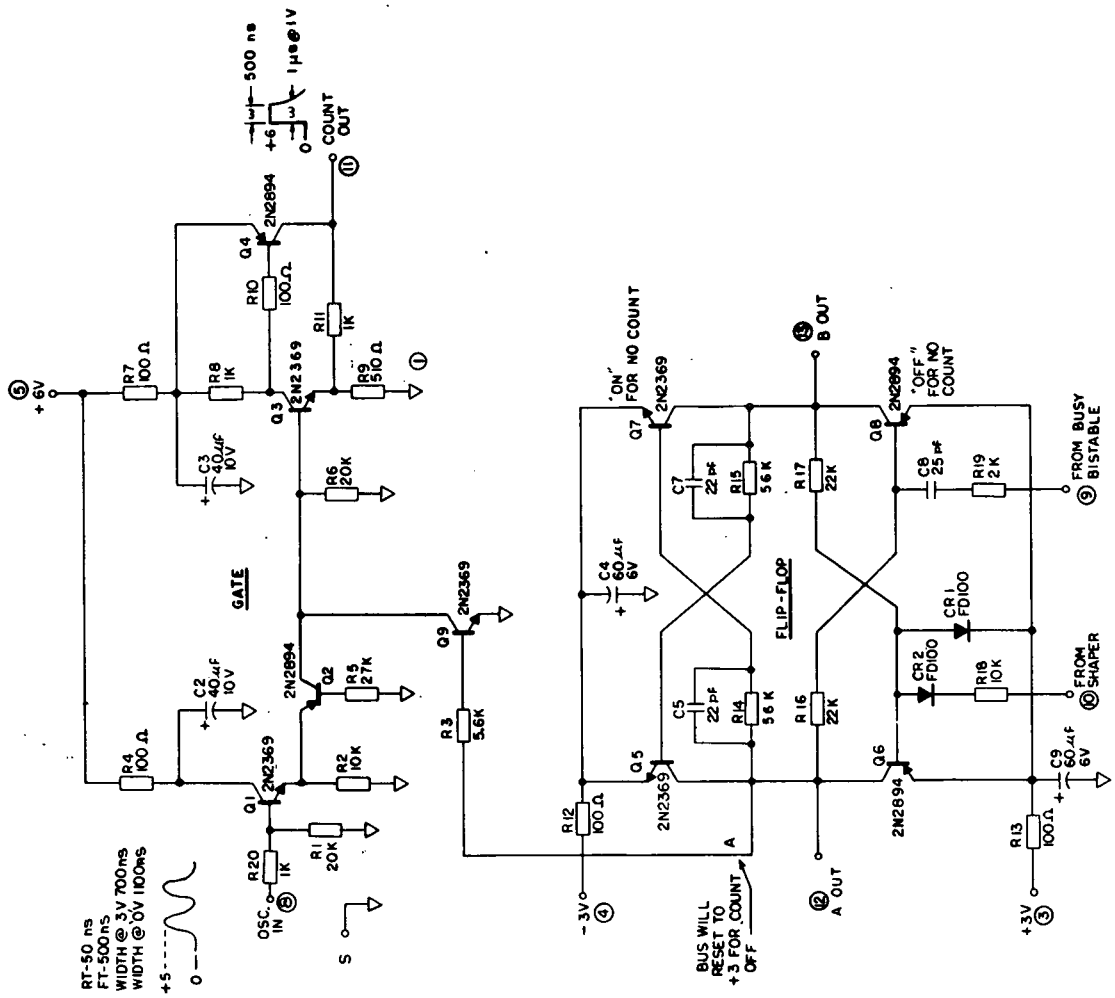


FIGURE 28. OUTPUT GATE

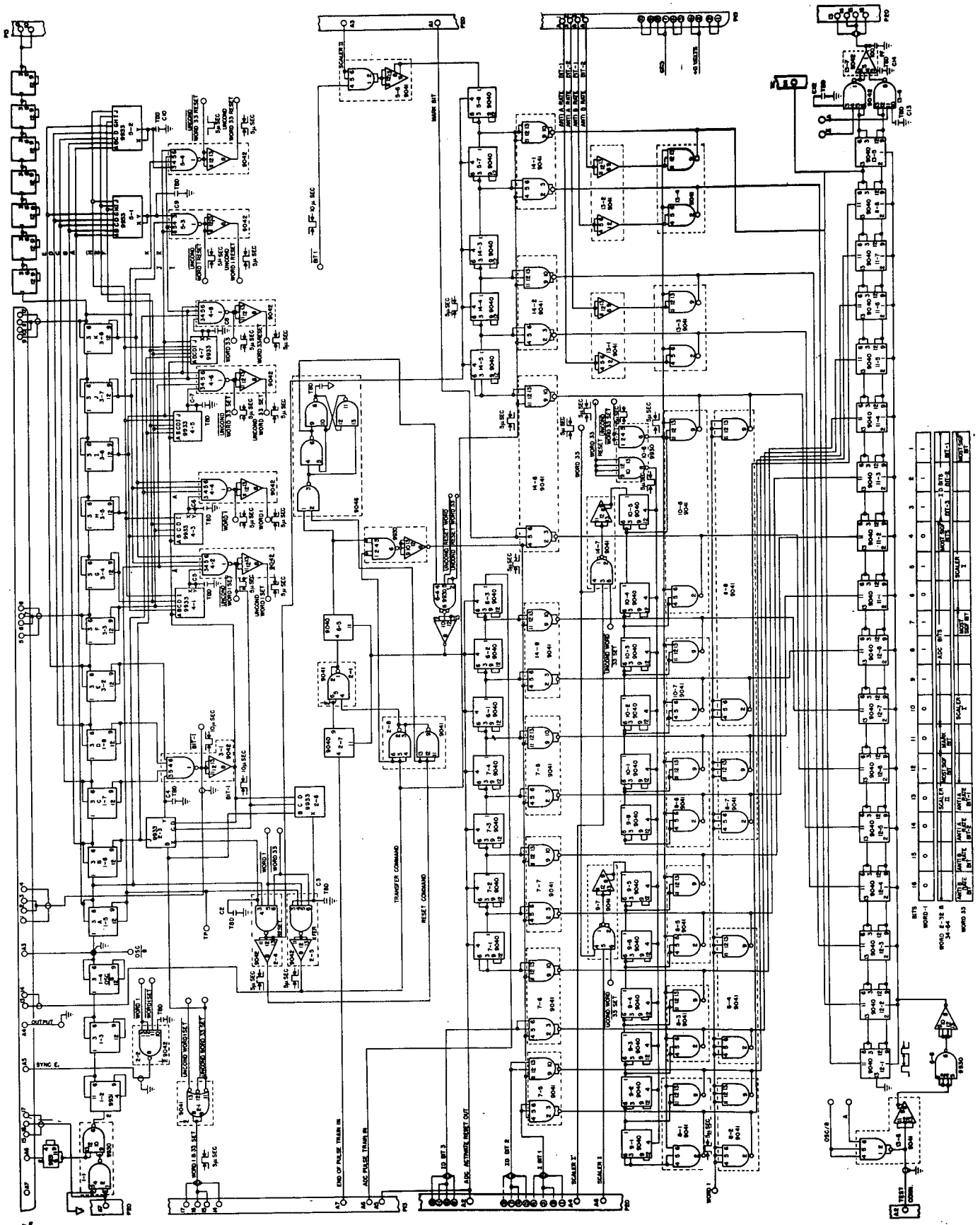


FIGURE 29. ENCODER SCHEMATIC

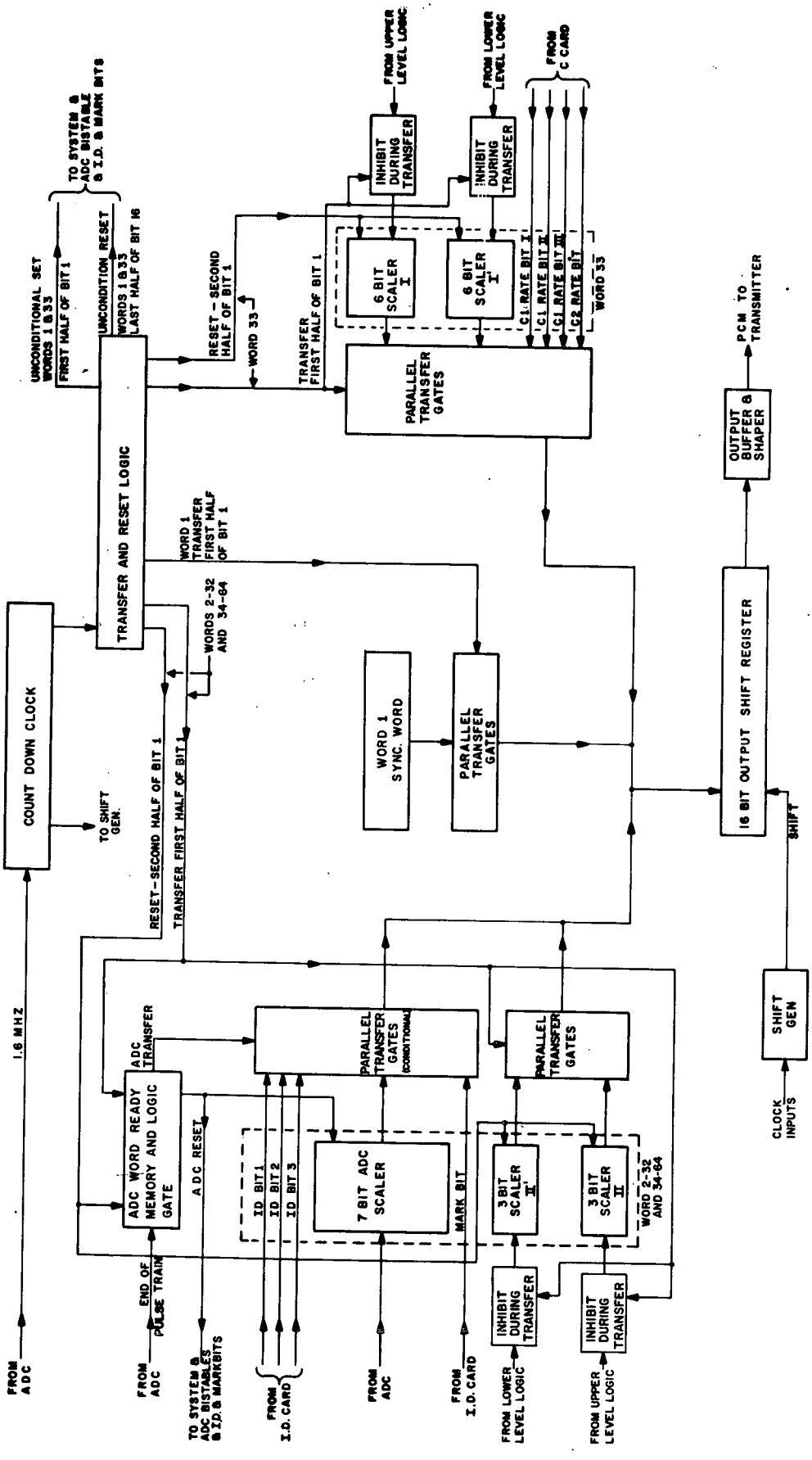


FIGURE 30. ENCODER SYSTEM BLOCK DIAGRAM

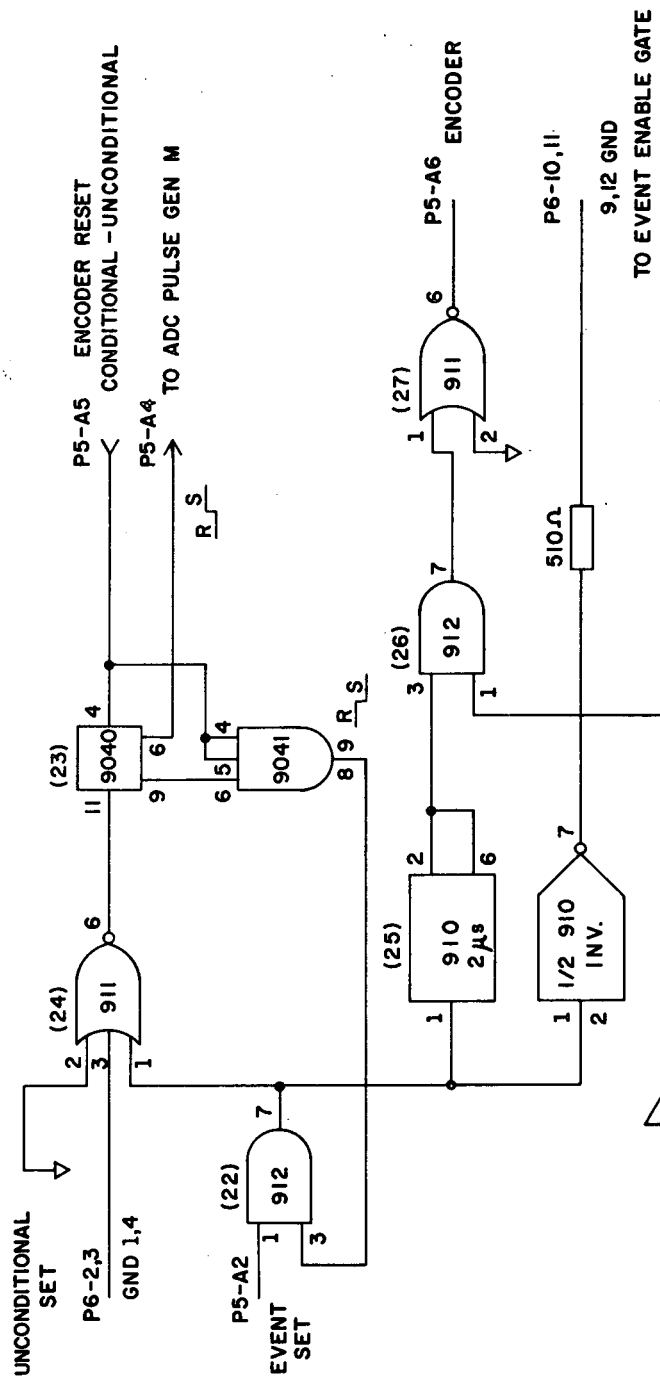


FIGURE 31. BUSY BISTABLE LOGIC CARD

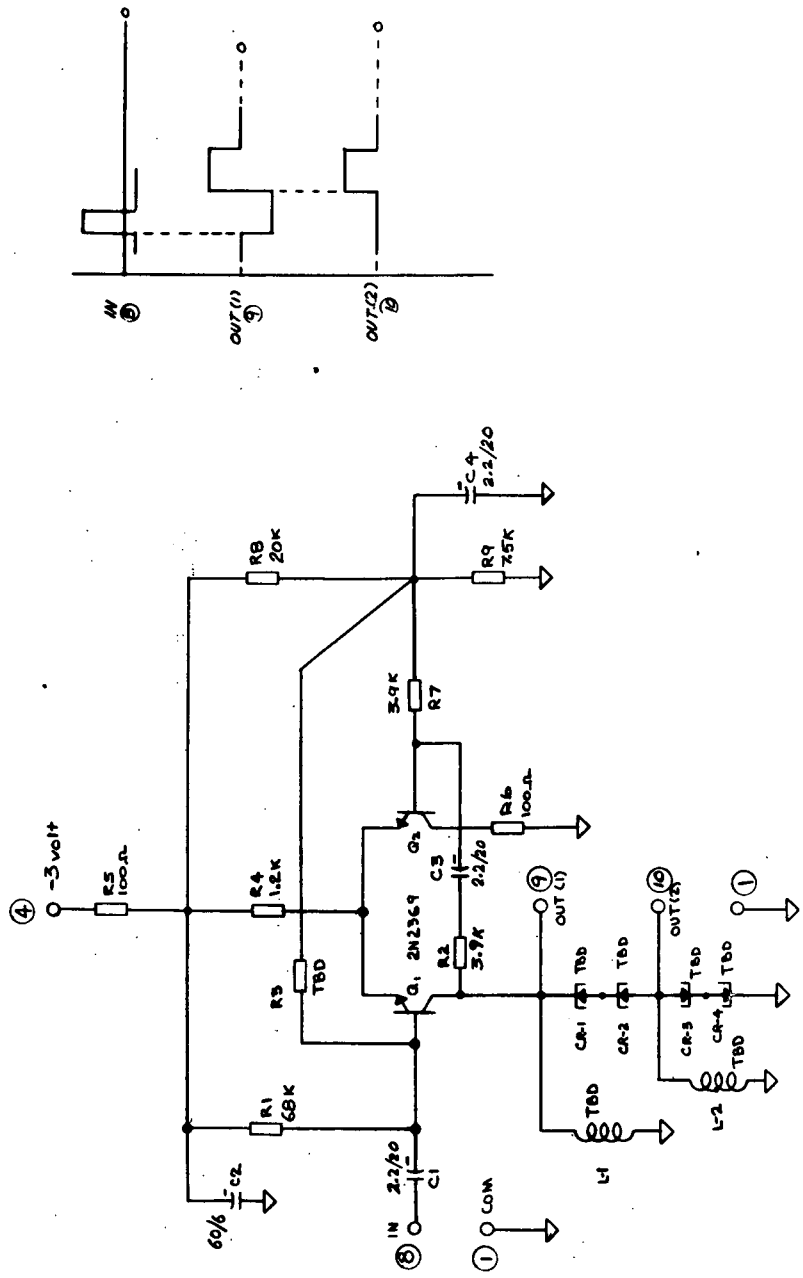


FIGURE 32. TYPE M-PULSE GENERATOR

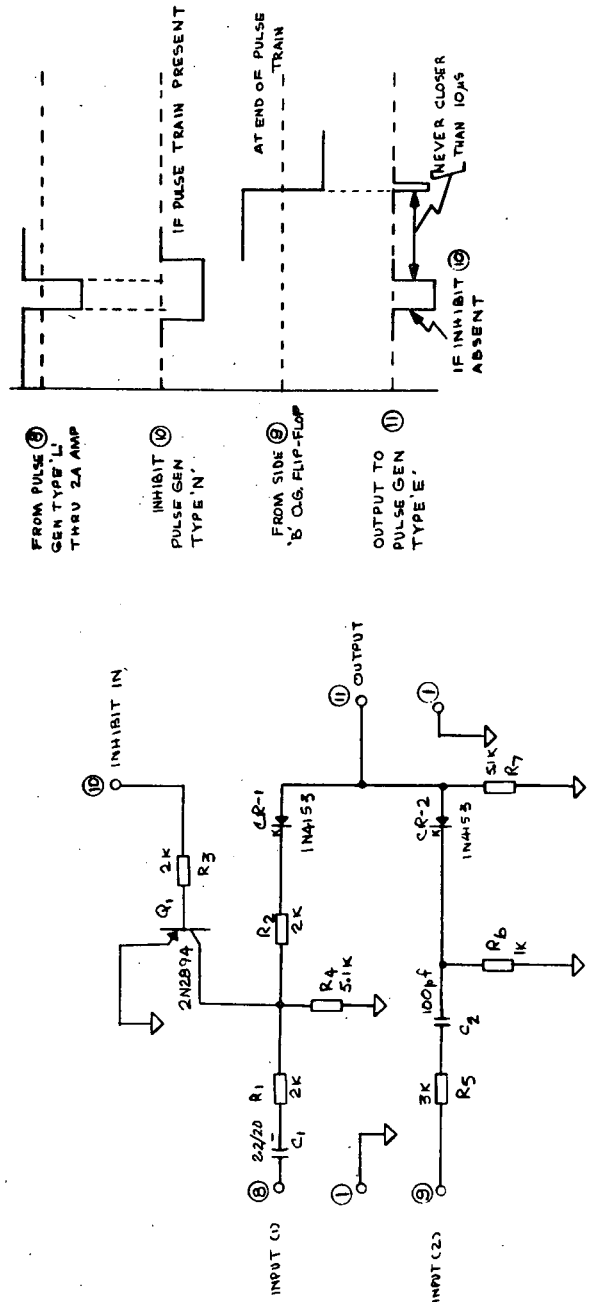
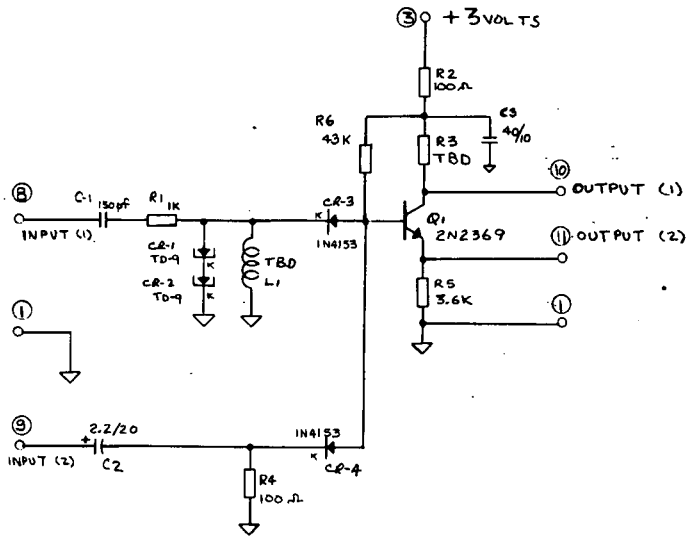


FIGURE 33. ADC INHIBIT GATE



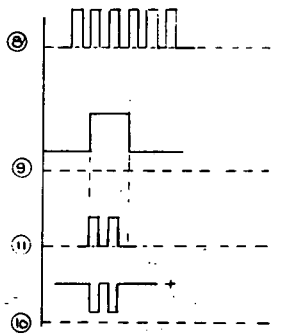


FIGURE 34. PULSED AND GATE

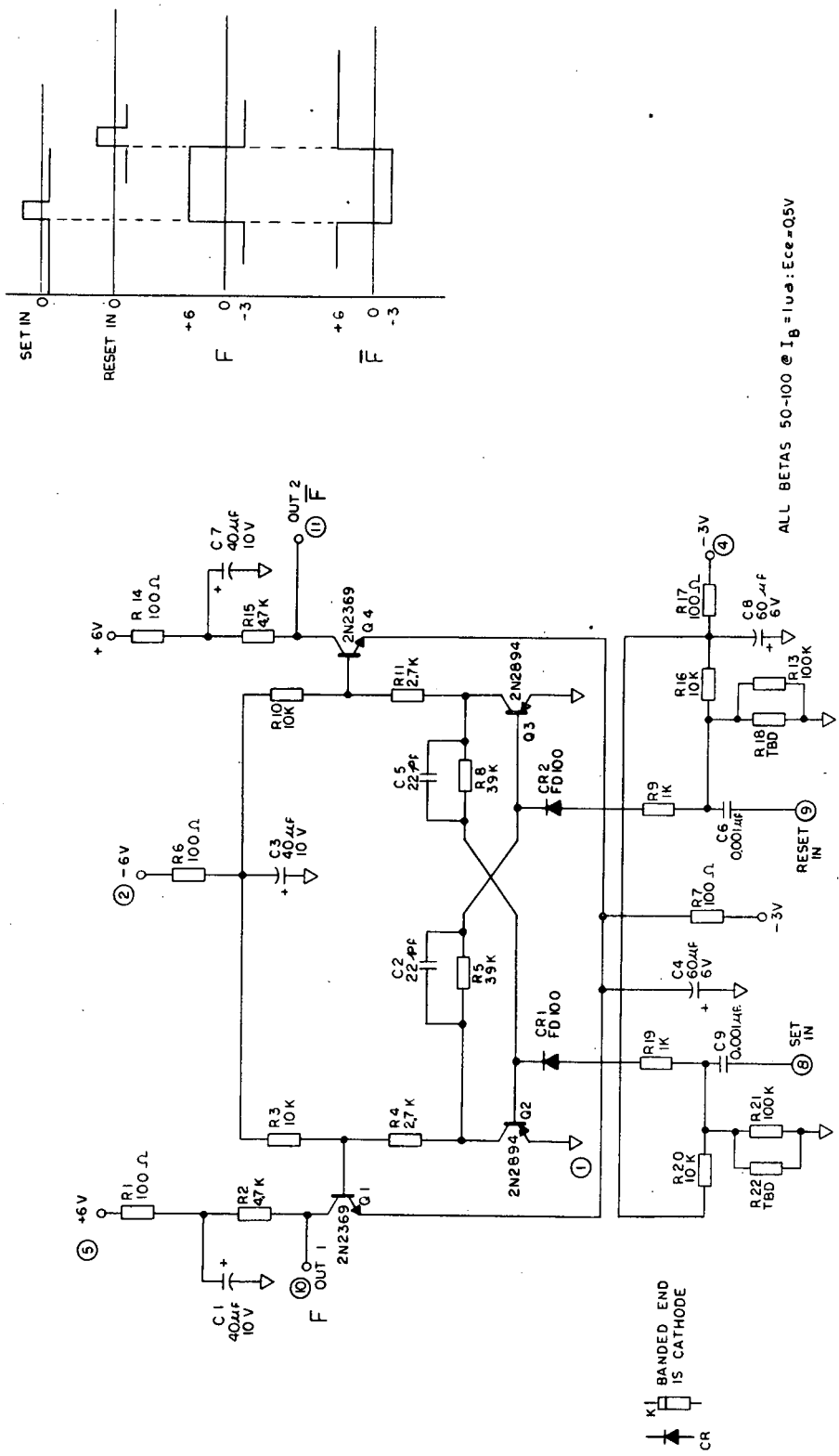


FIGURE 35. ADC BUSY BISTABLE

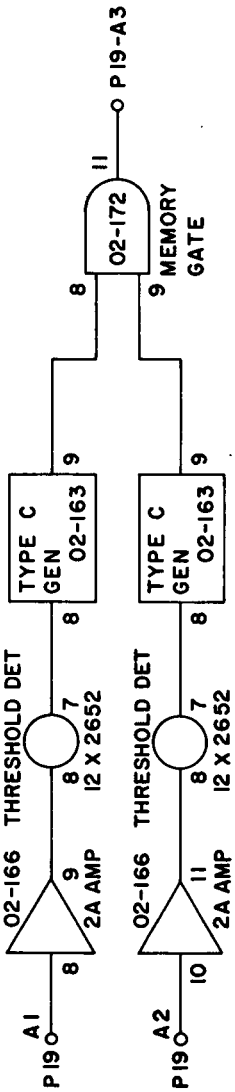


FIGURE 36. MARK BIT LOGIC CARD NO. 1

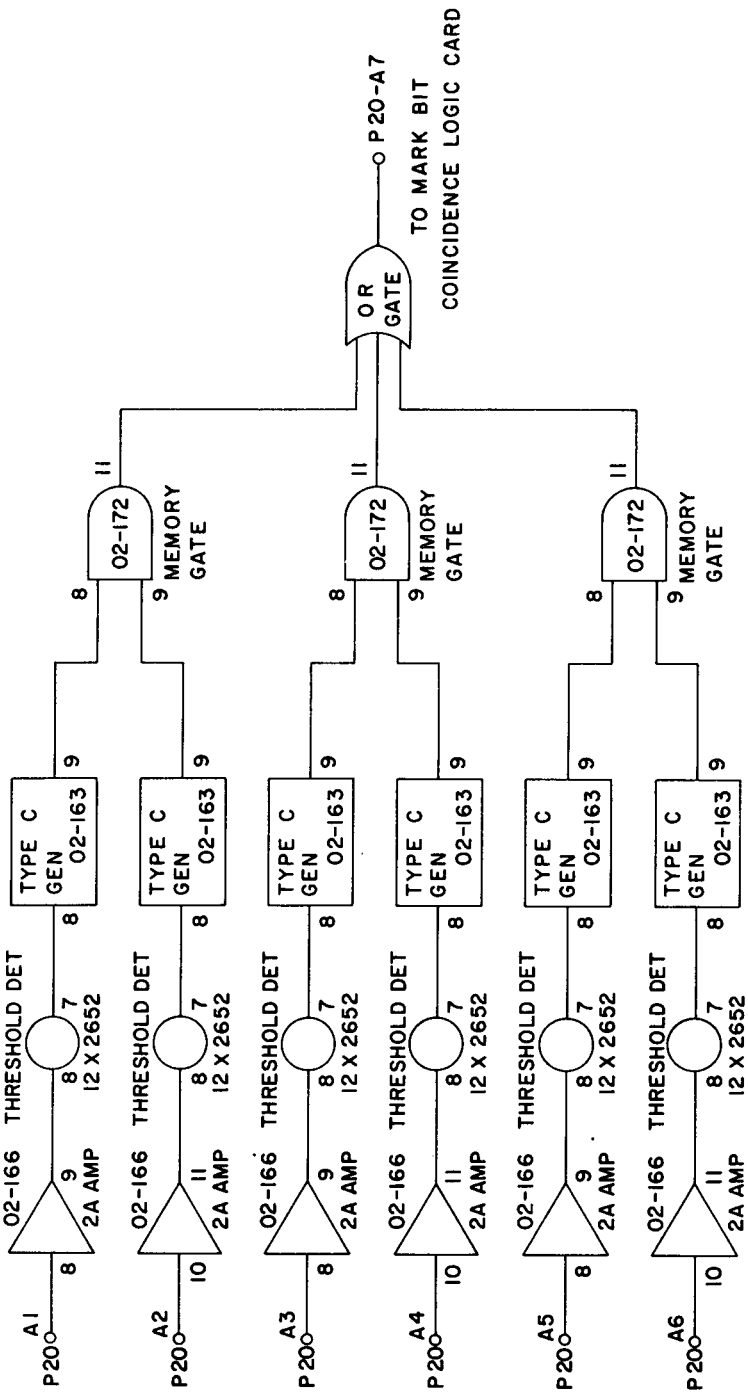


FIGURE 37. MARK BIT LOGIC CARD NO. 2

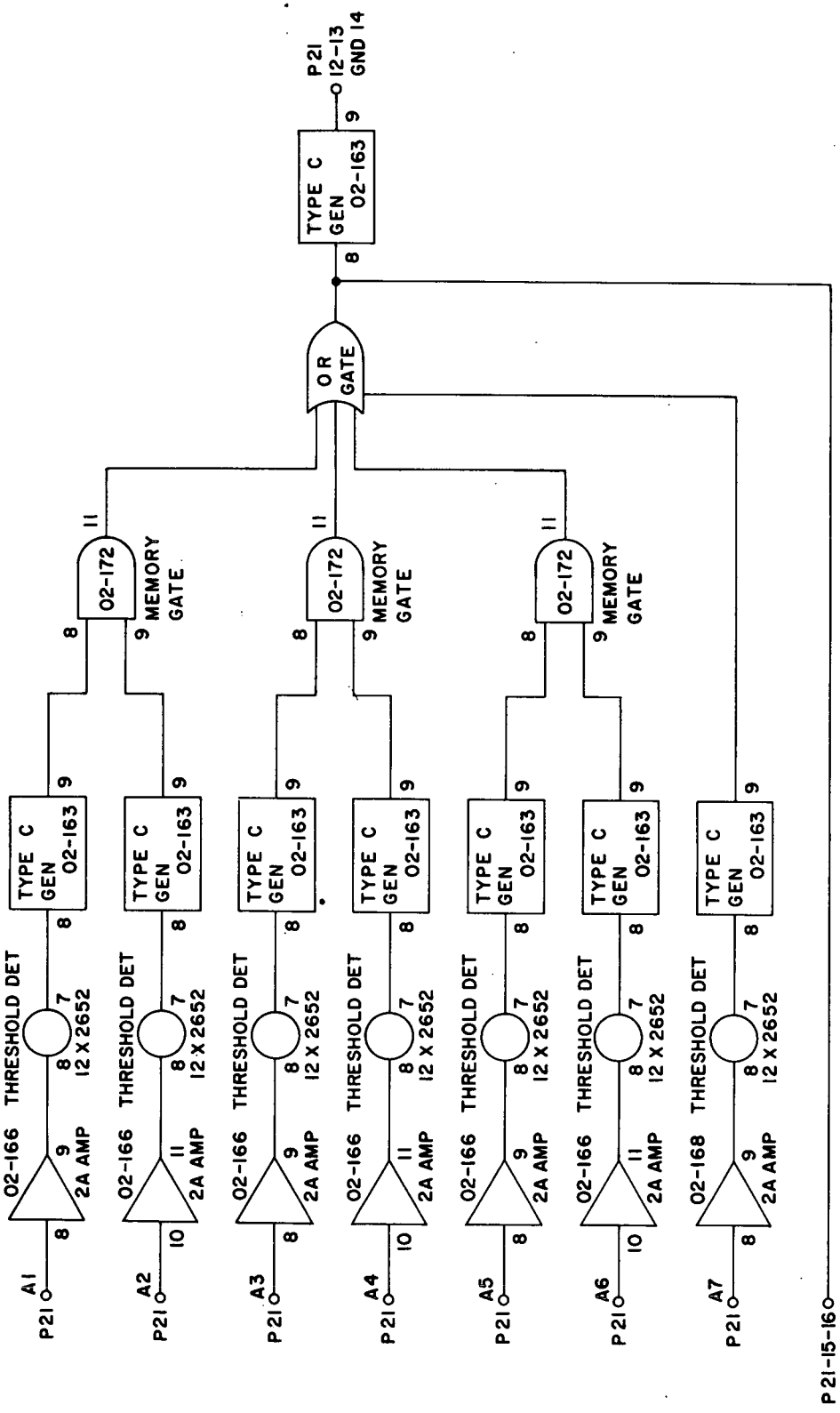


FIGURE 38. MARK BIT LOGIC CARD NO. 3

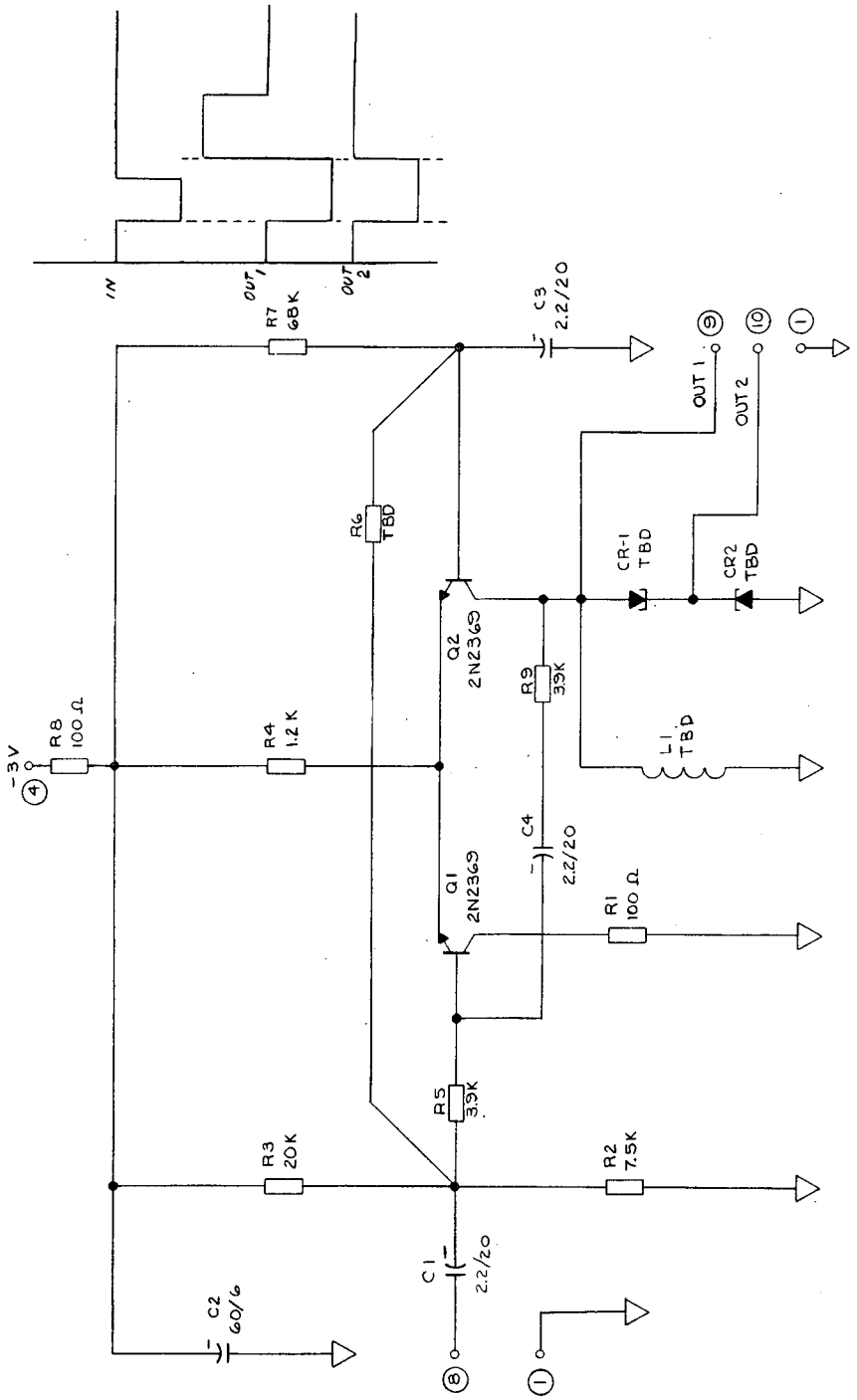


FIGURE 39. TYPE E-PULSE GENERATOR

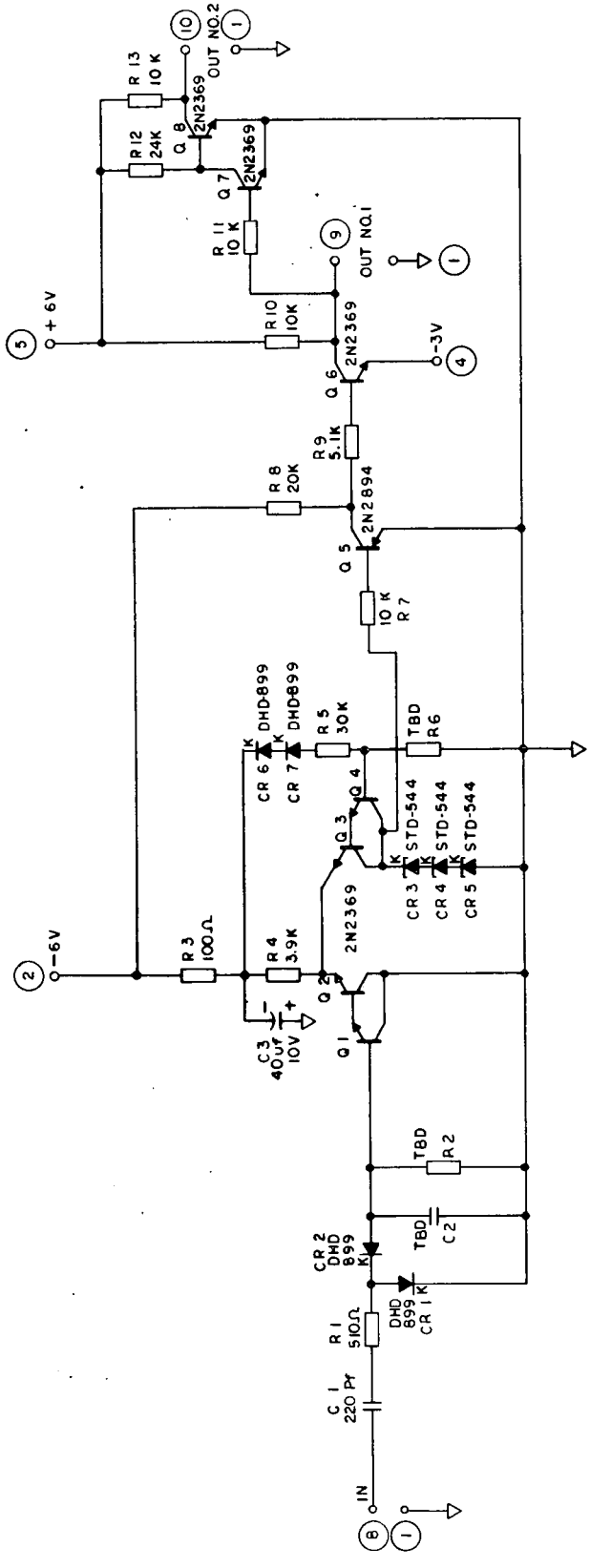


FIGURE 40. RATE DISCRIMINATOR AND OUTPUT CIRCUIT

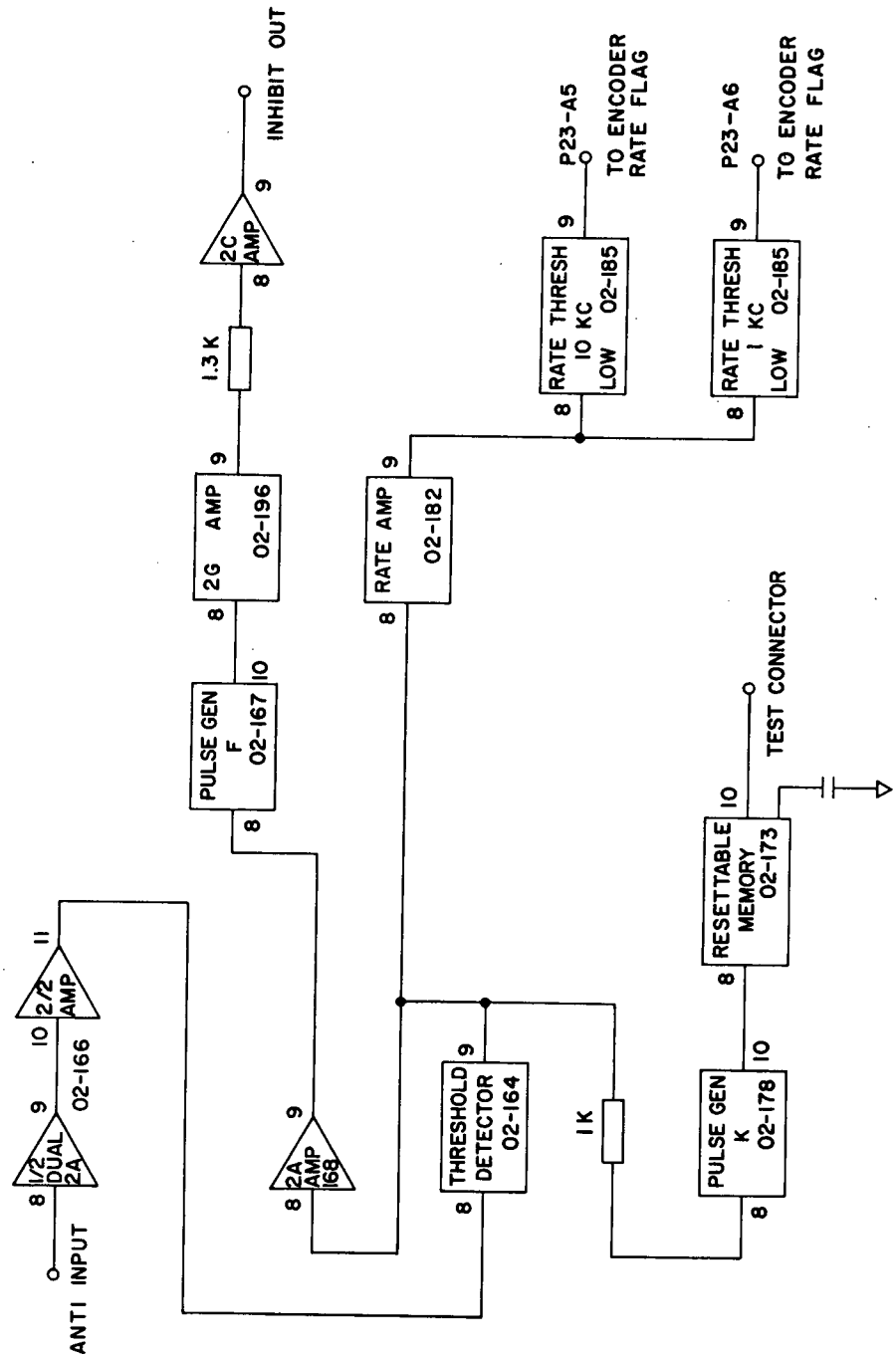


FIGURE 41. ANTICOINCIDENCE LOGIC CARD

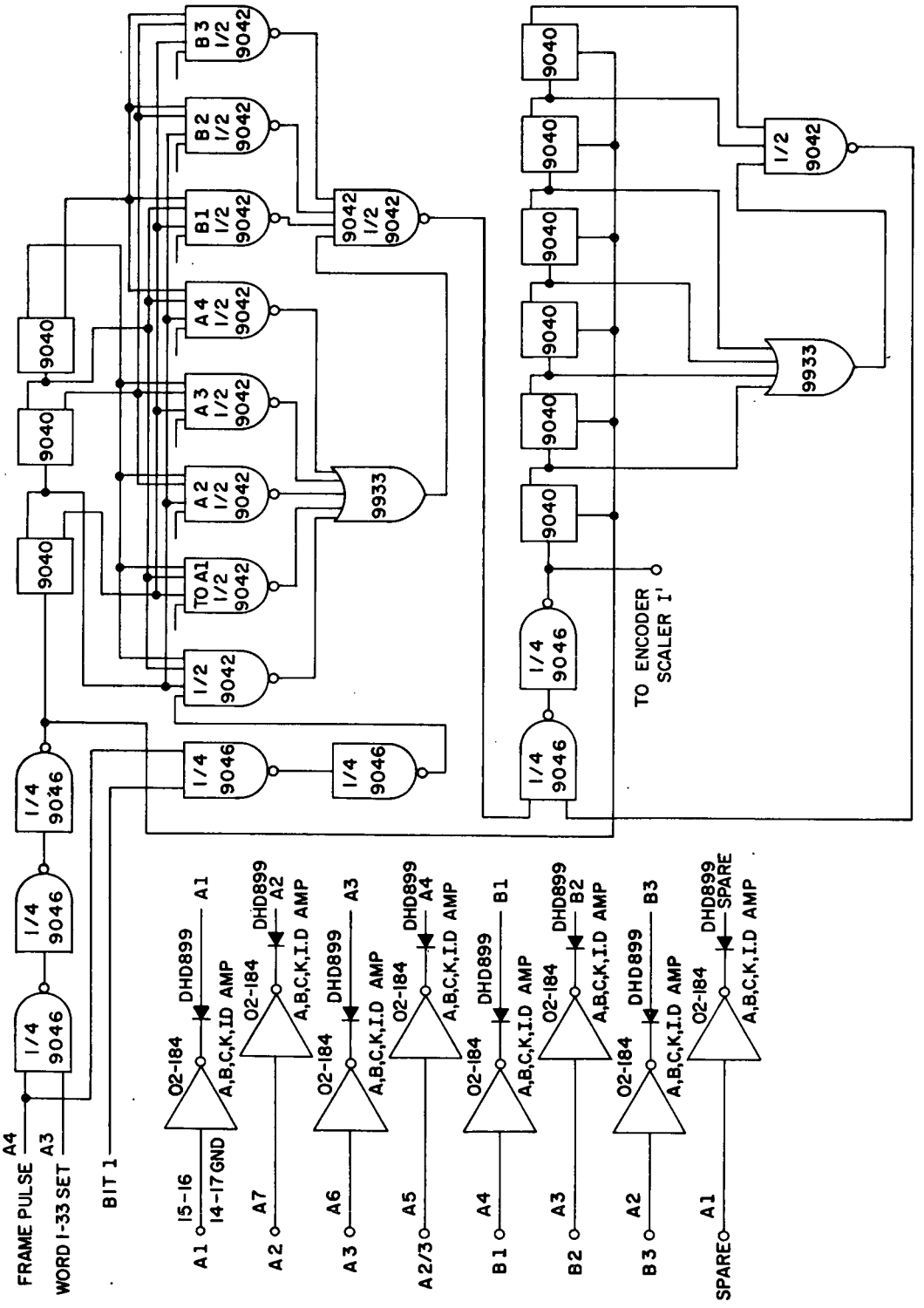


FIGURE 42. EIGHT CHANNEL COMMUTATOR

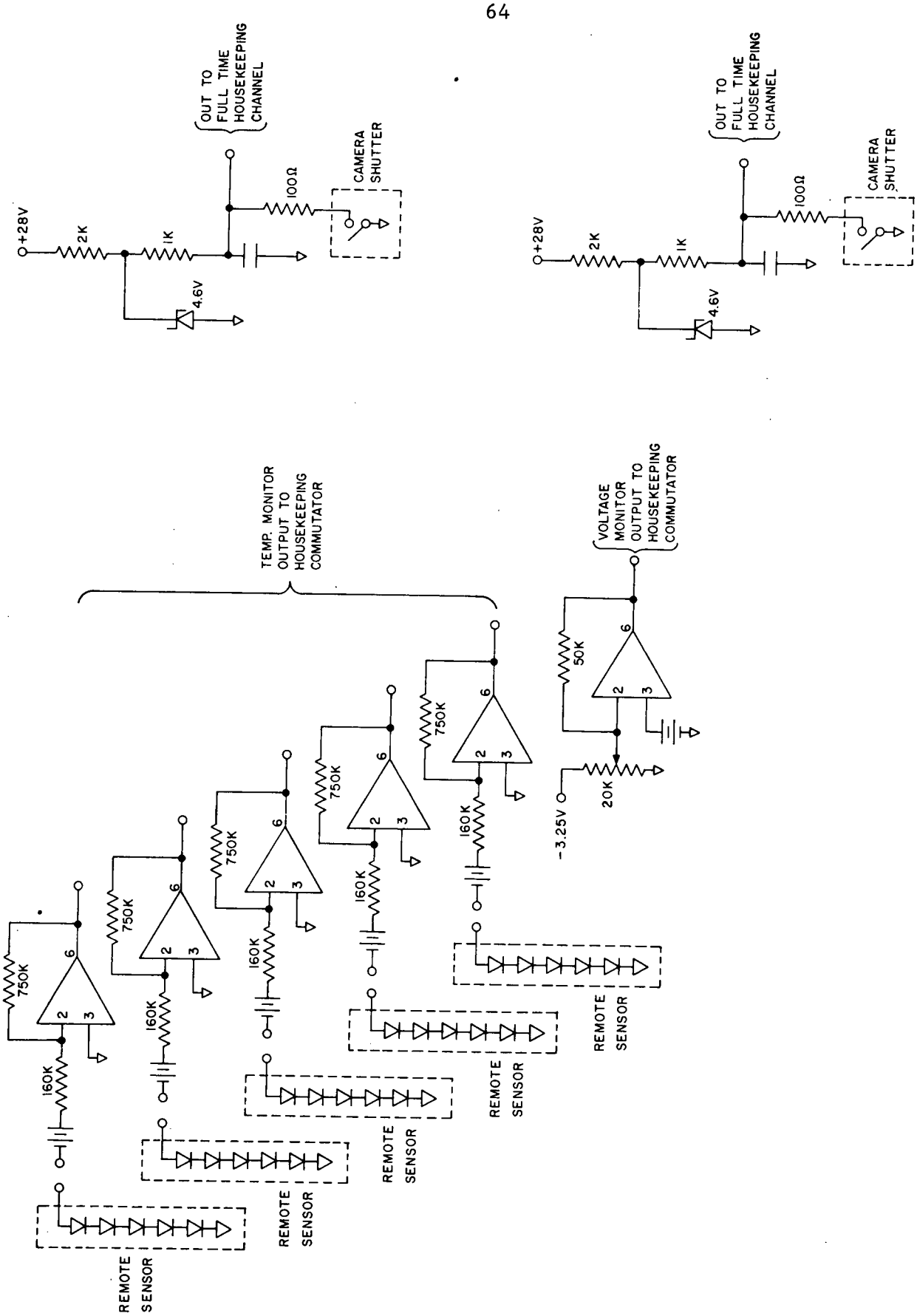
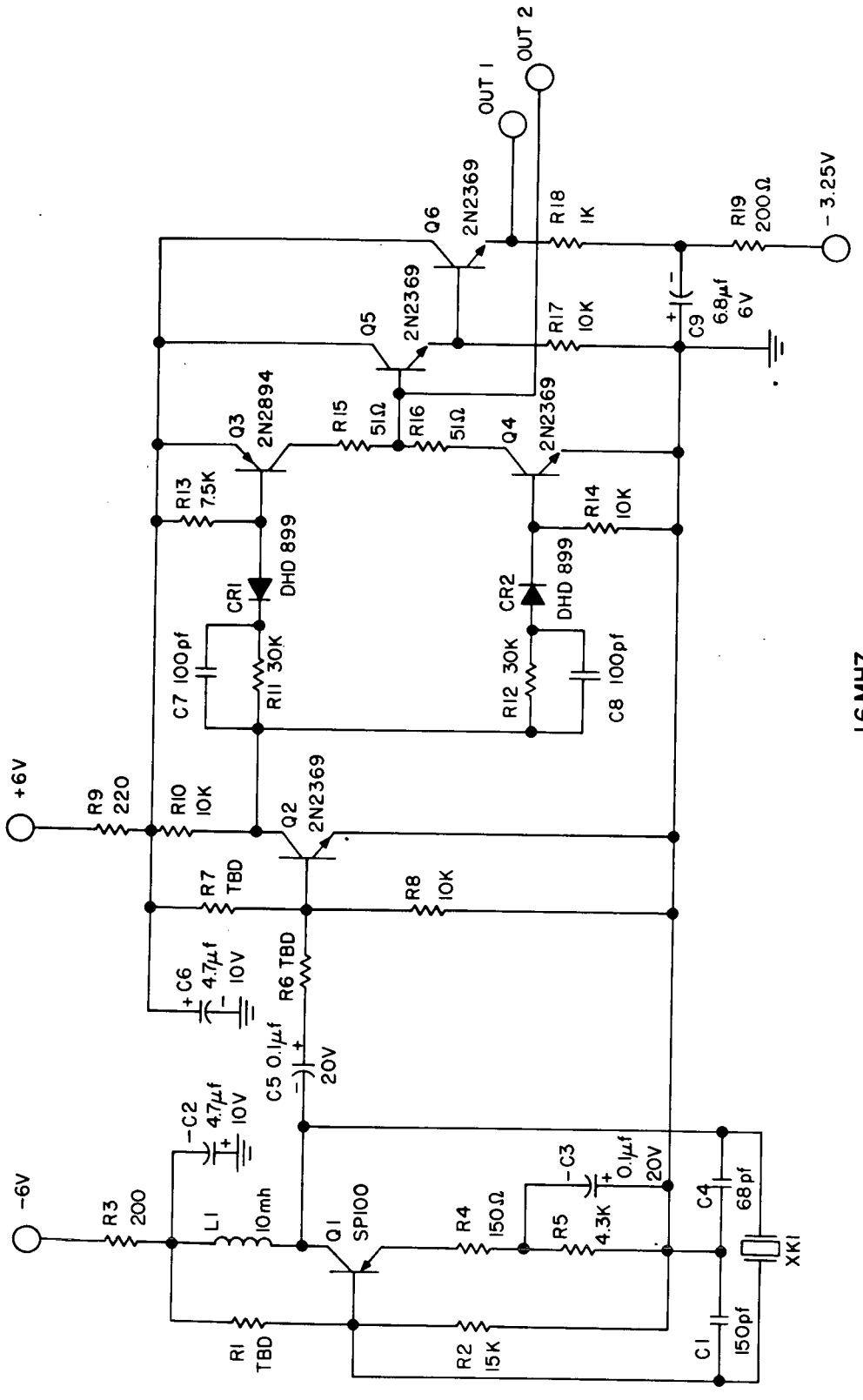


FIGURE 43. SYSTEM MONITOR CARD



1.6 MHZ
OSCILLATOR & SQUARING CIRCUIT

FIGURE 44.

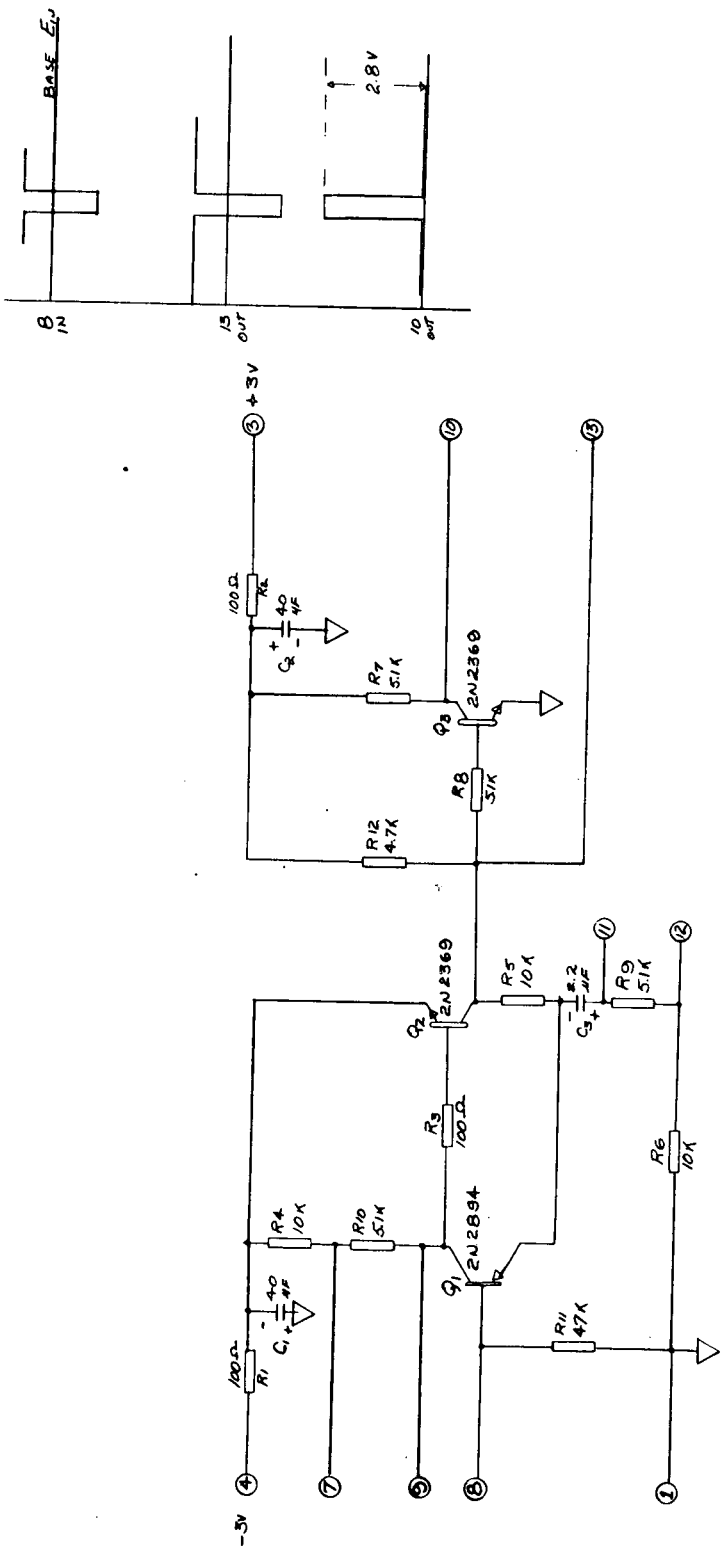


FIGURE 45. A, B, C, K AND I.D. AMPLIFIER

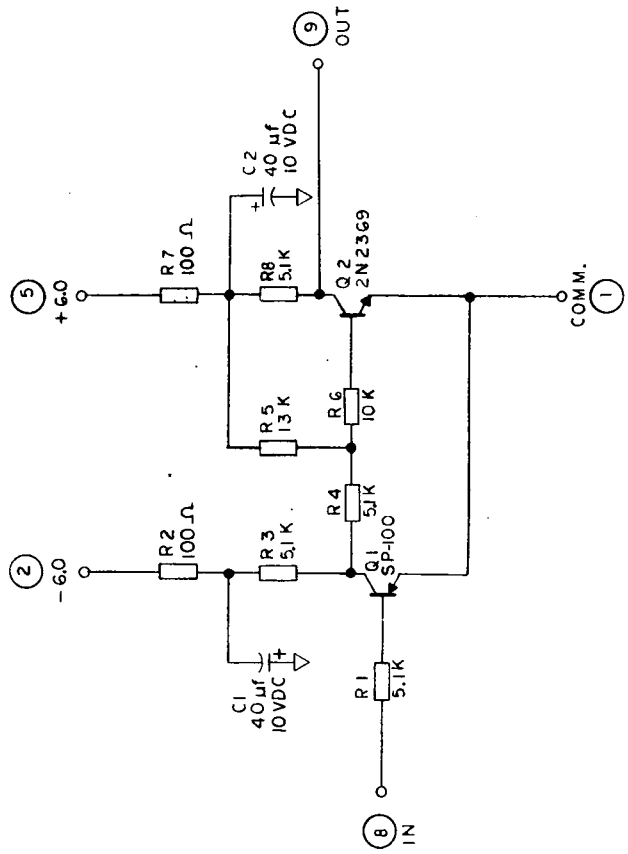


FIGURE 46. I.D. BUFFER

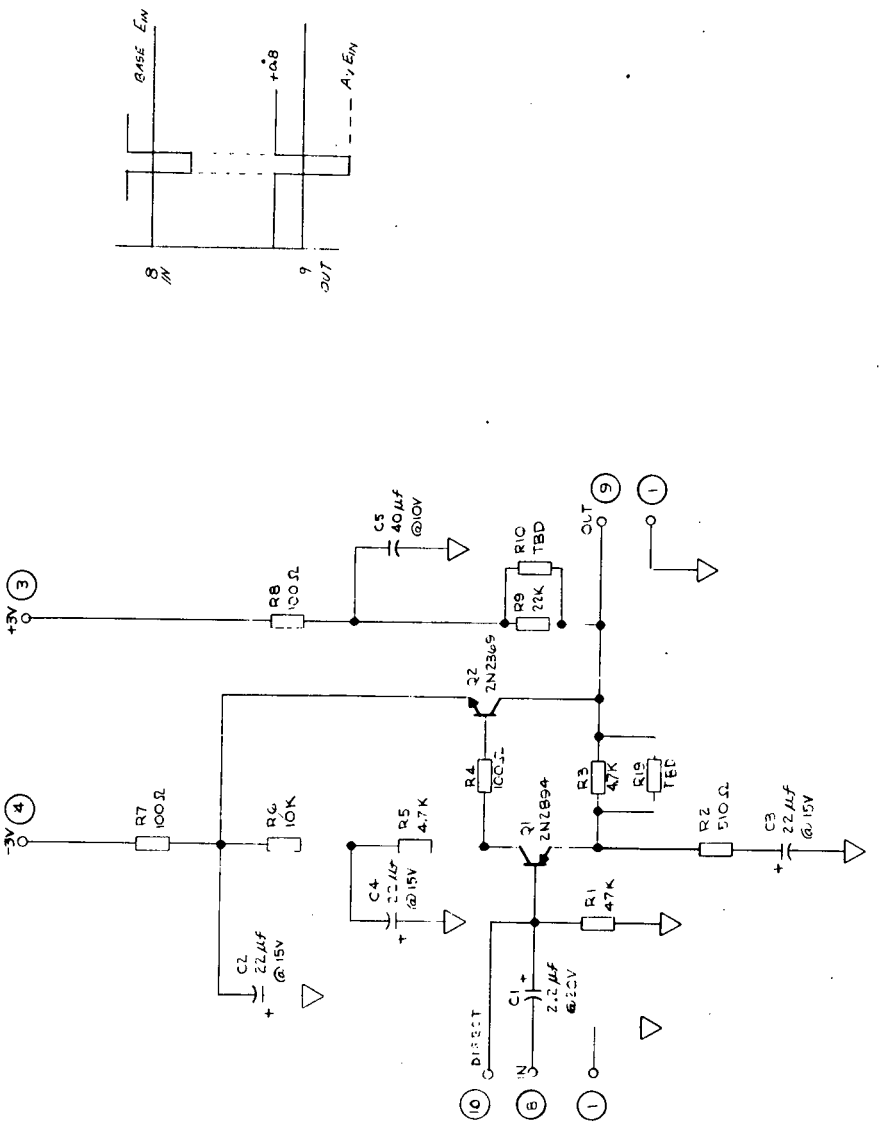


FIGURE 47. SINGLE 2A AMPLIFIER

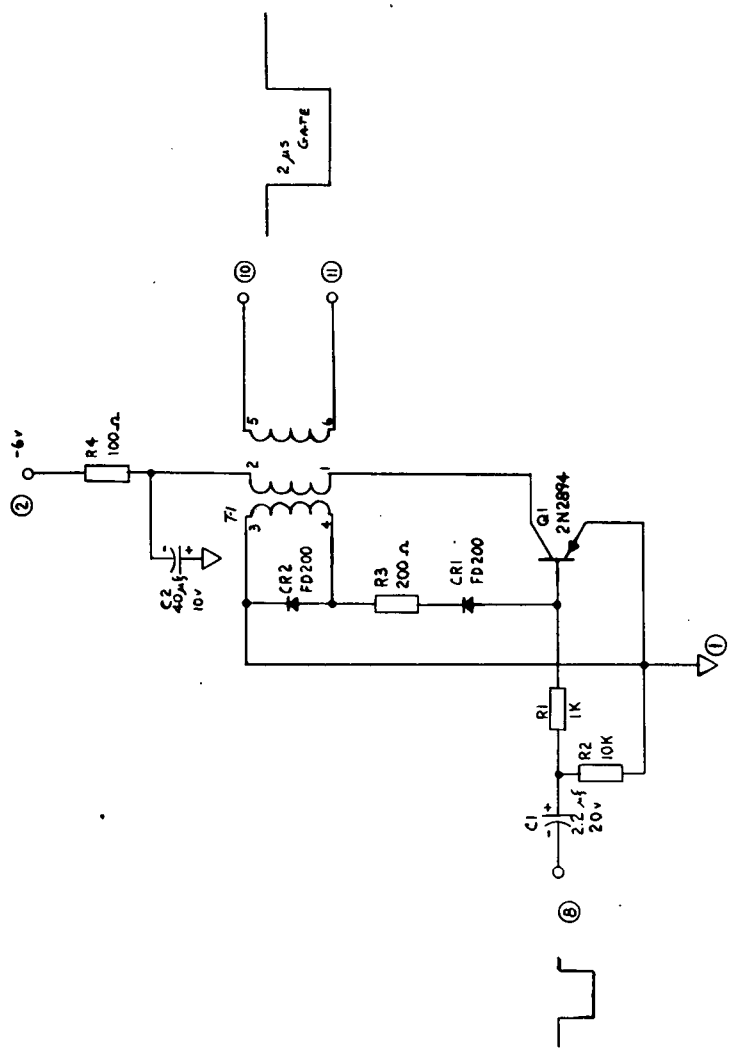


FIGURE 48. LINEAR GATE DRIVER

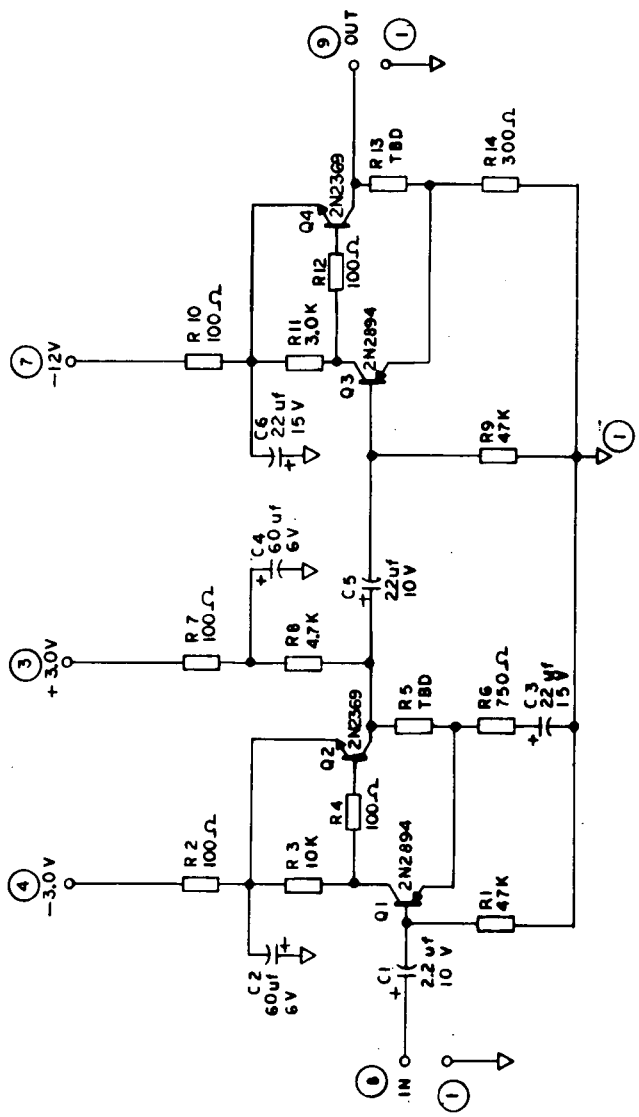


FIGURE 49. RATE AMPLIFIER

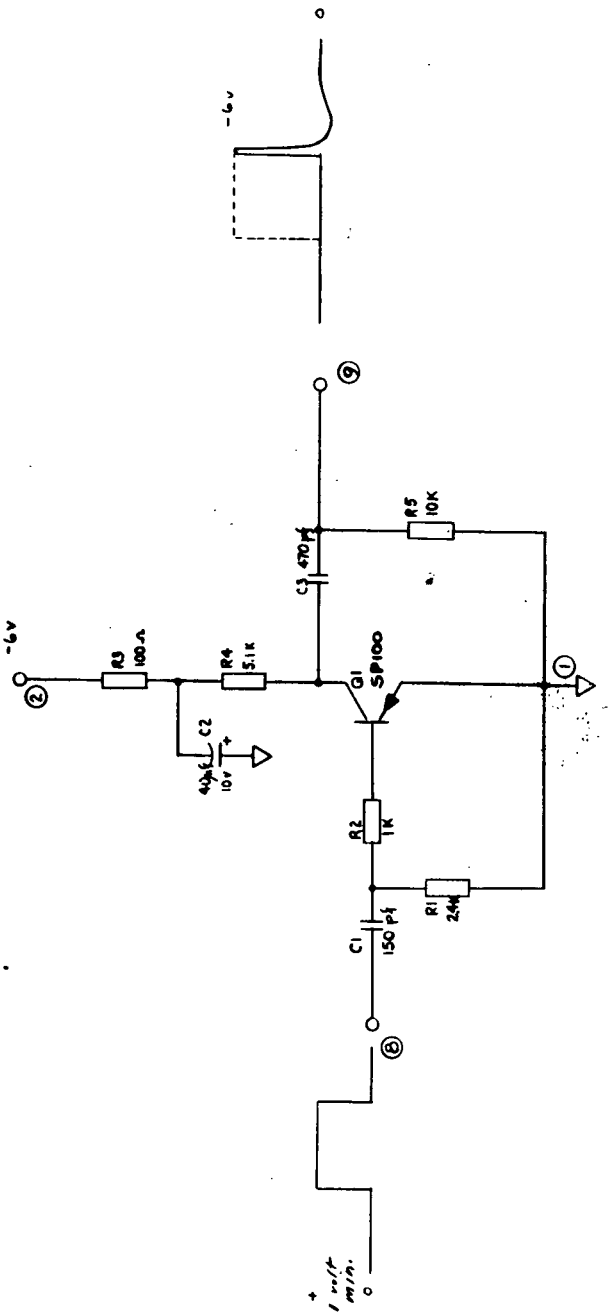


FIGURE 50. TRAILING EDGE SPIKER

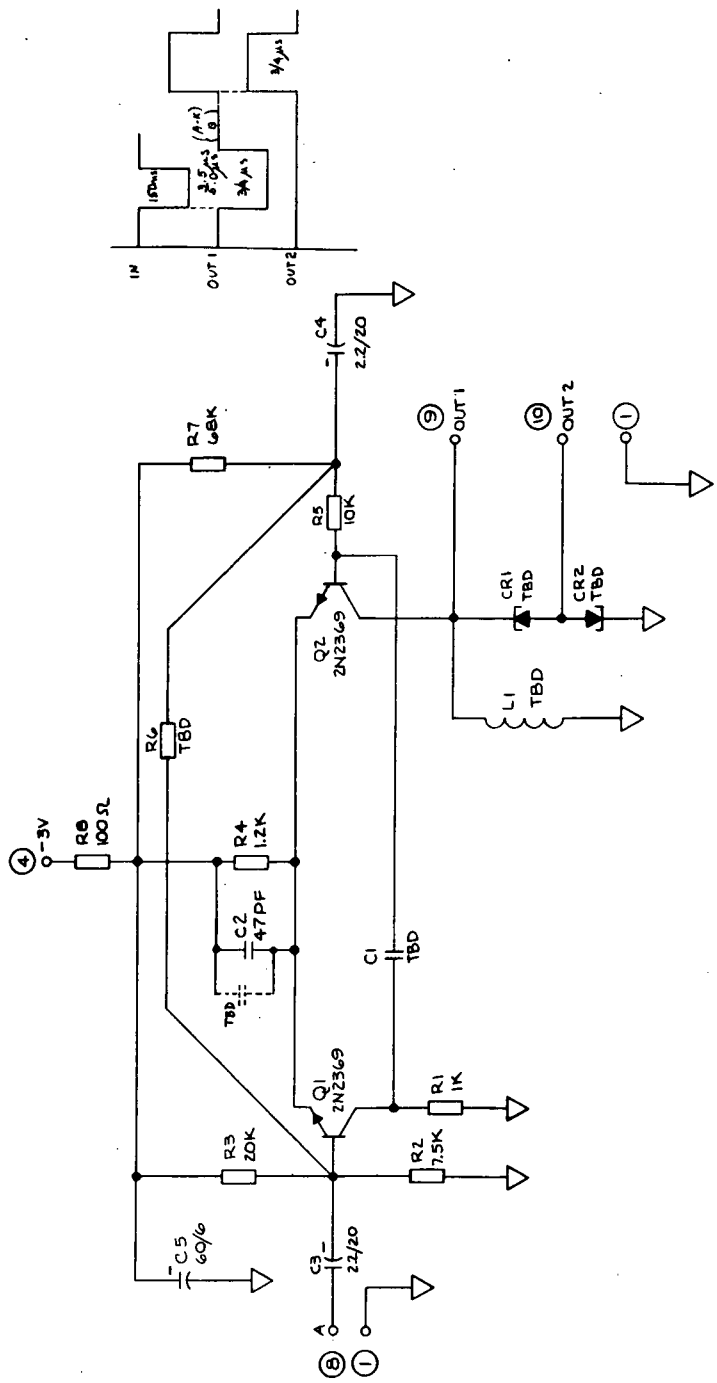


FIGURE 51. TYPE A-PULSE GENERATOR

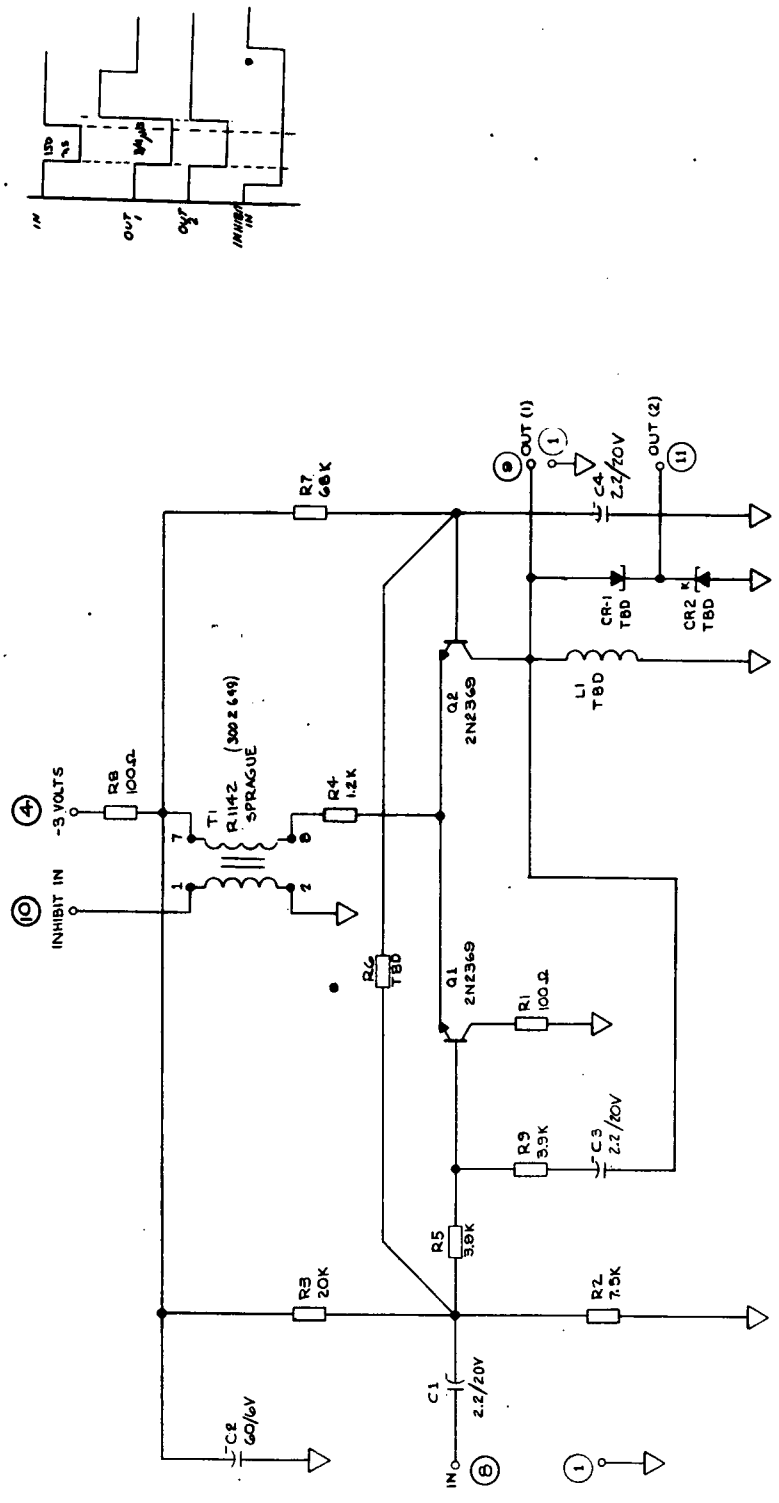


FIGURE 52. TYPE B-PULSE GENERATOR

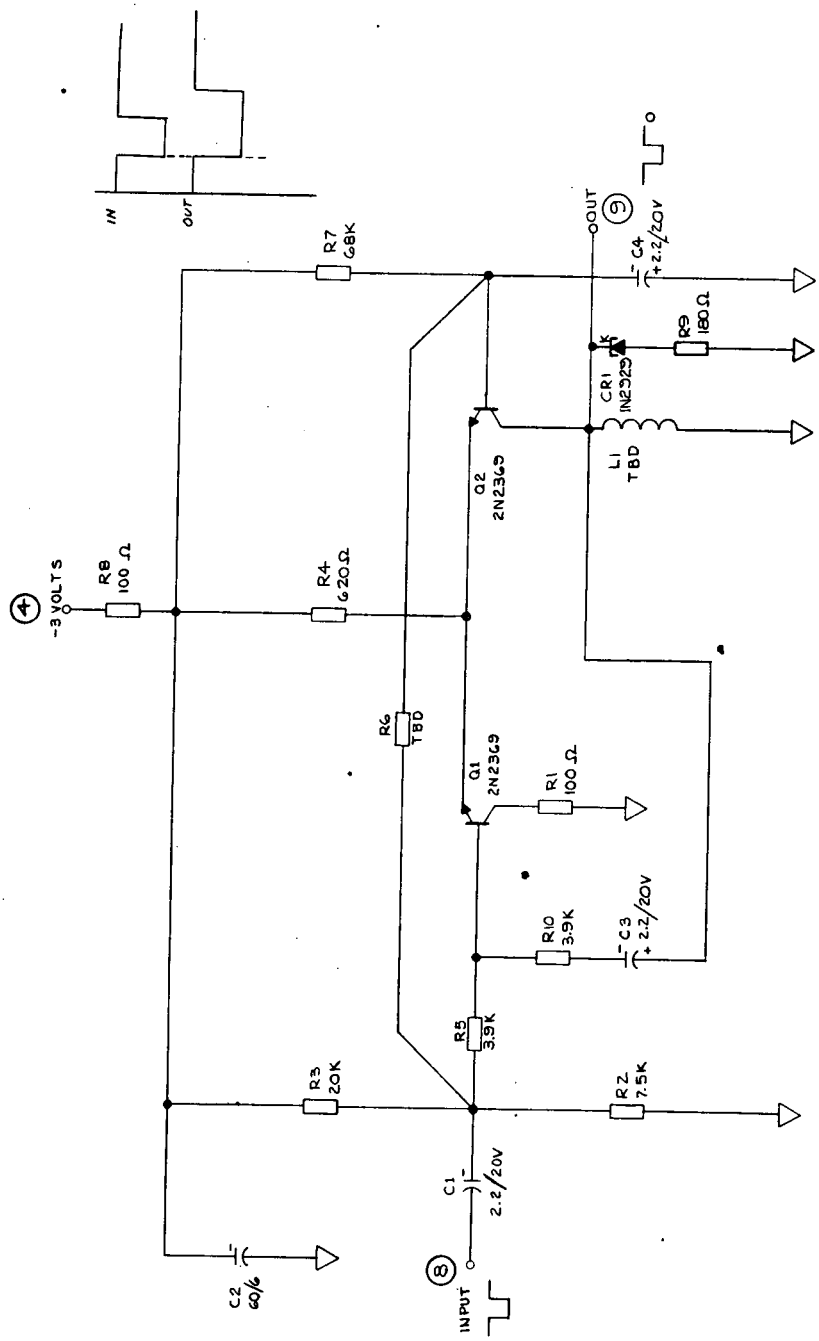


FIGURE 53. TYPE C-PULSE GENERATOR

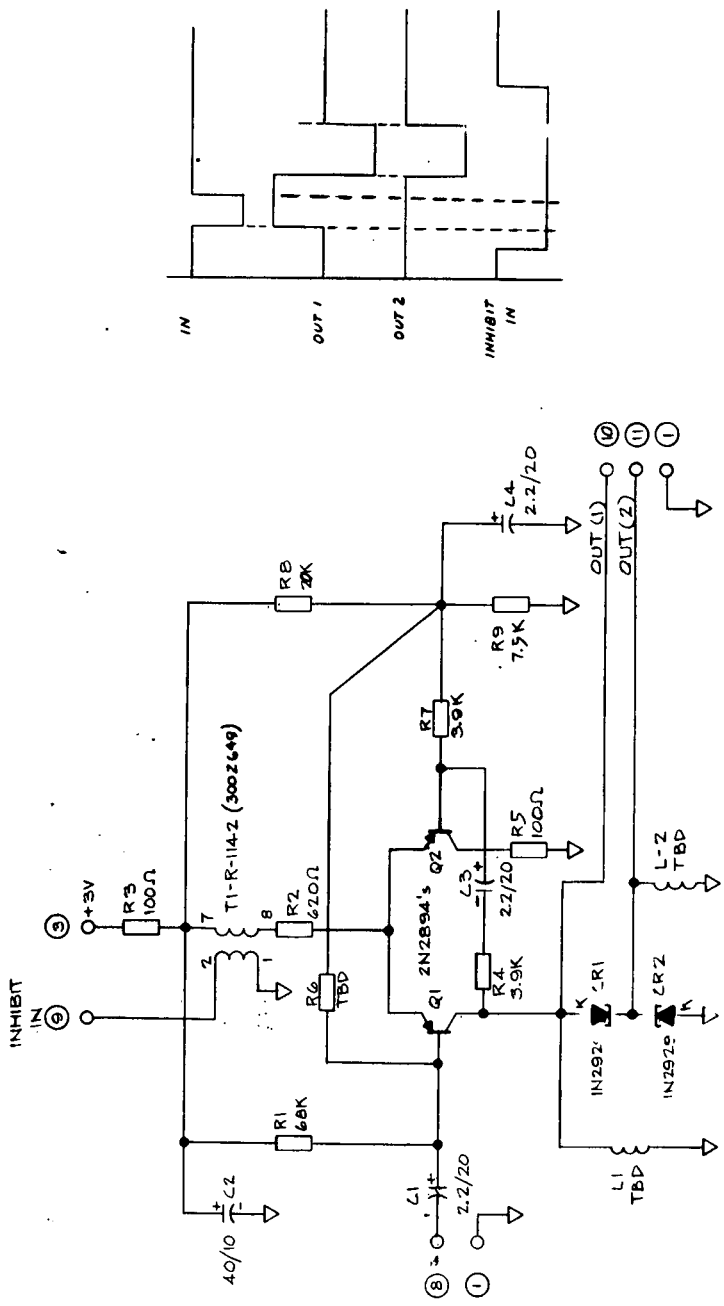


FIGURE 54. TYPE H-PULSE GENERATOR

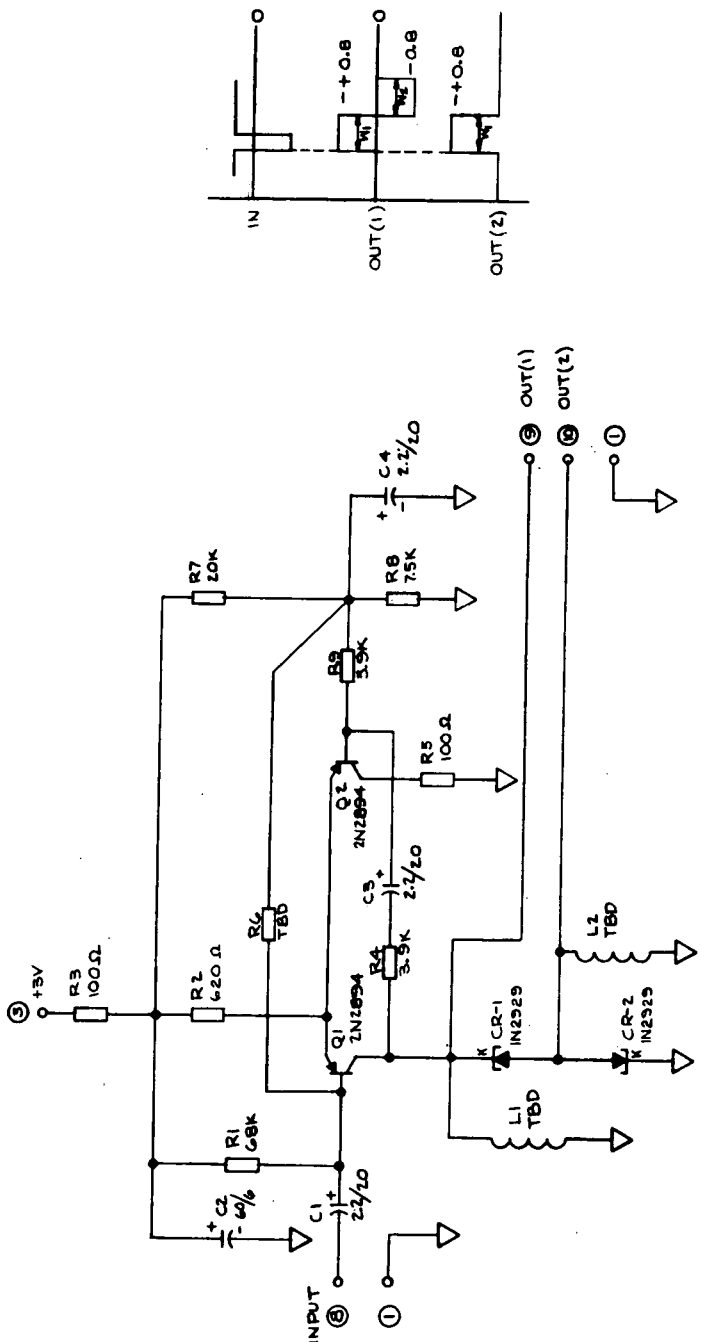


FIGURE 55. TYPE K-PULSE GENERATOR

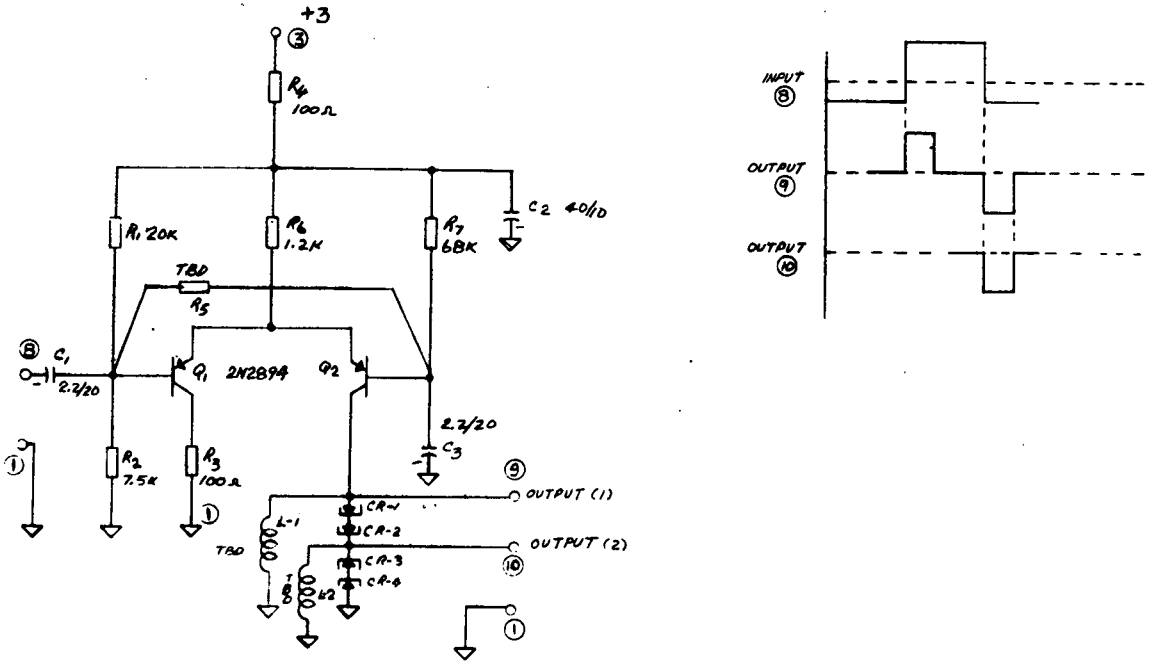
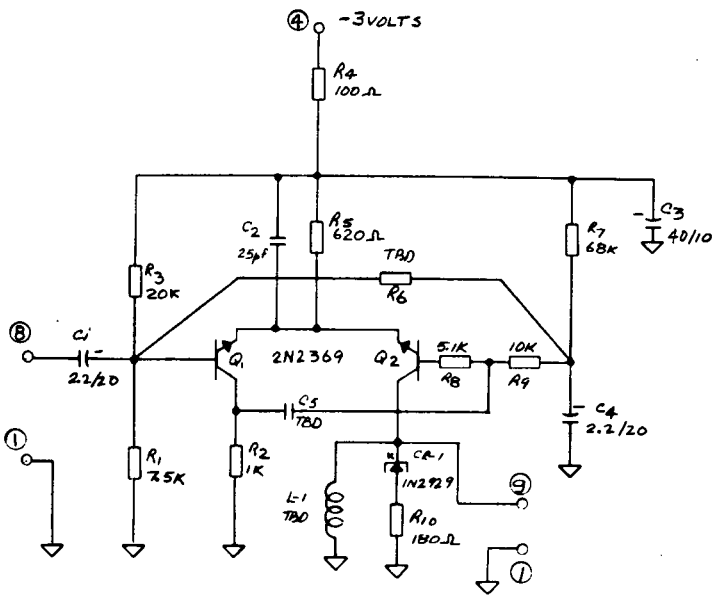


FIGURE 56. TYPE L-PULSE GENERATOR



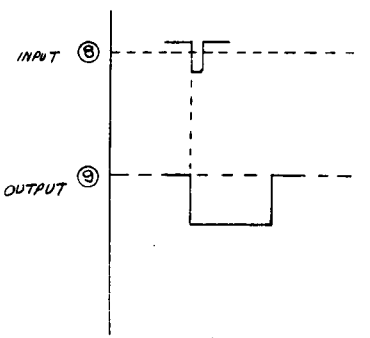


FIGURE 57. TYPE N-PULSE GENERATOR

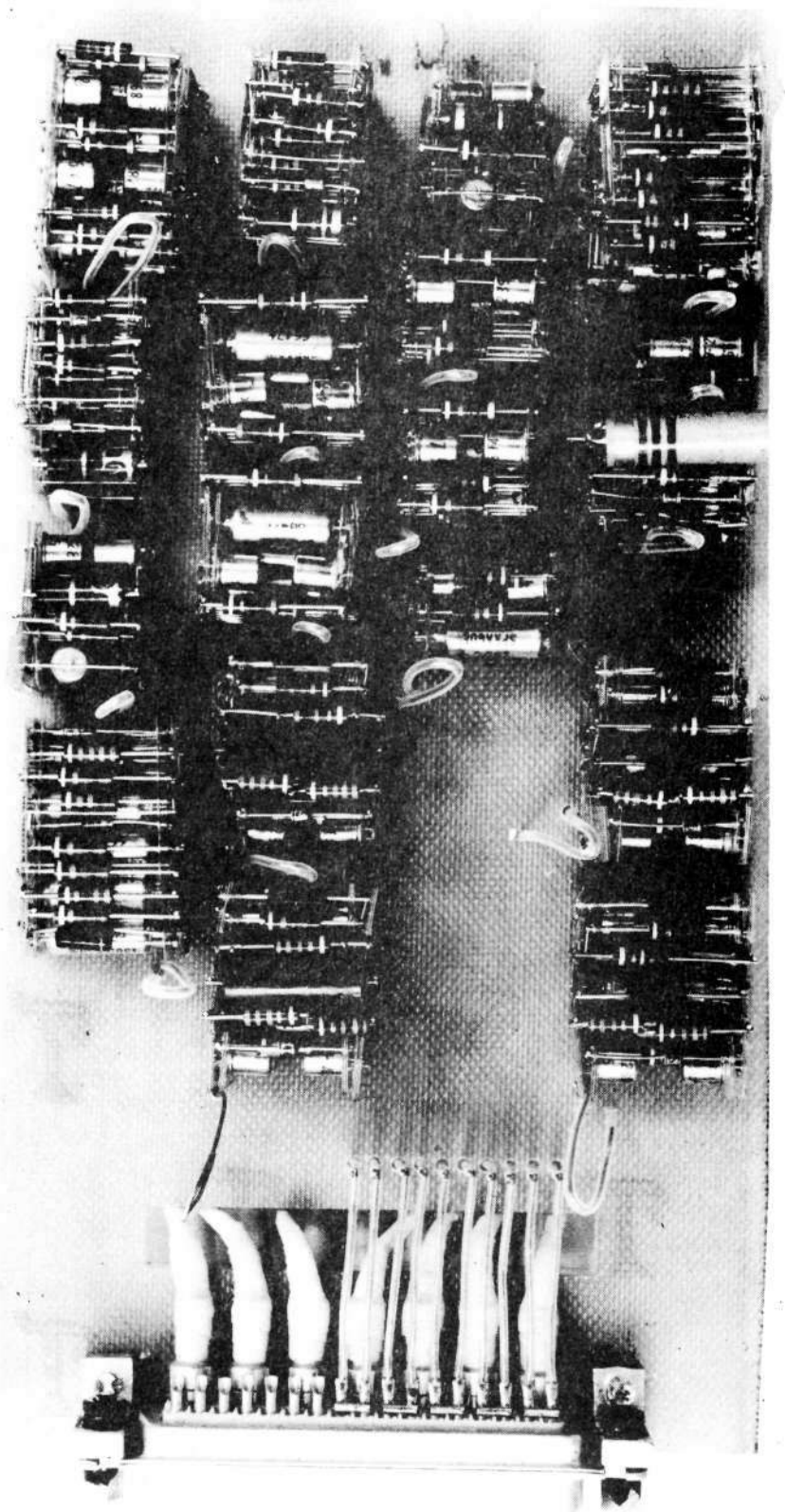


FIGURE 58. TYPICAL CARD BEFORE POTTING

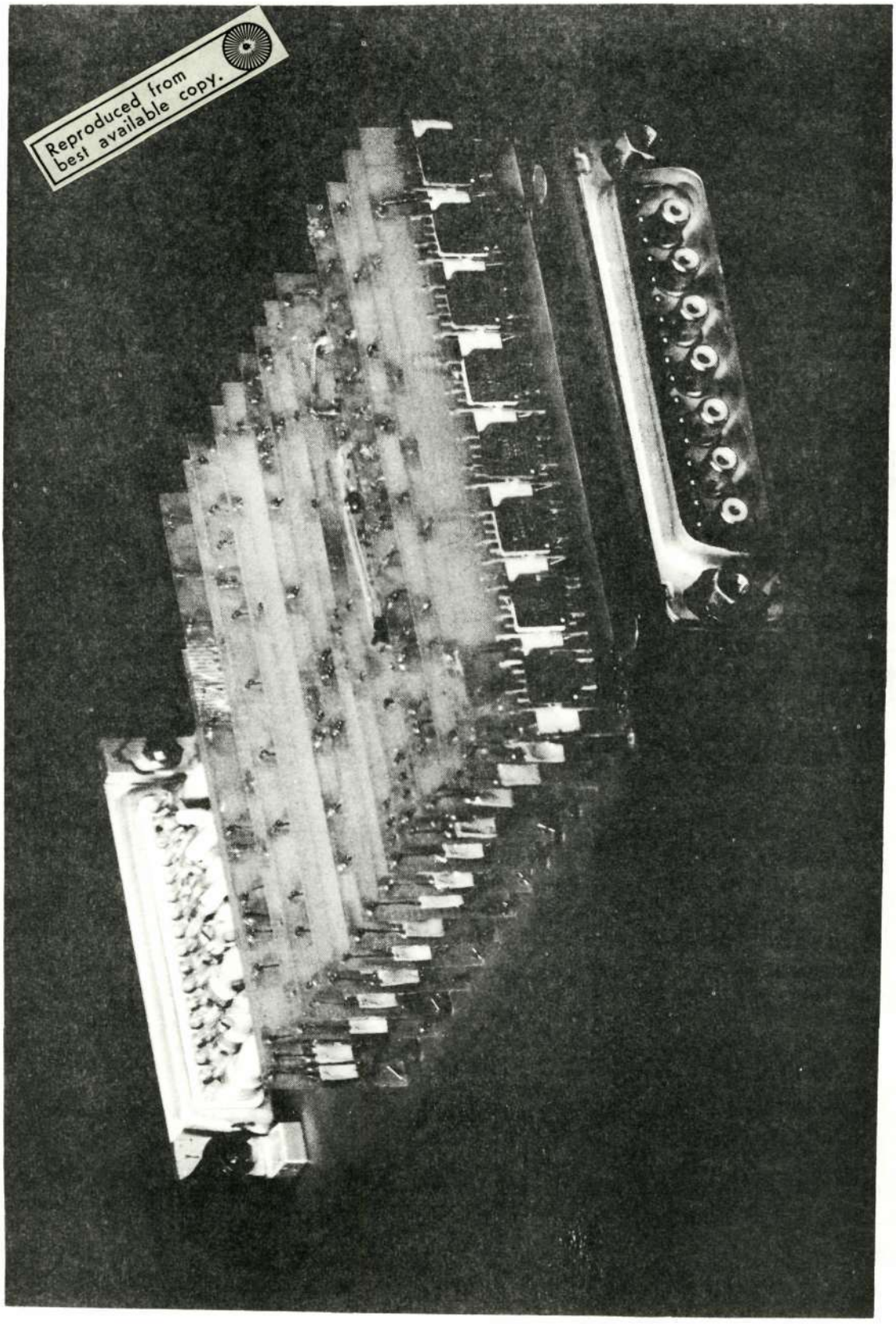


FIGURE 59. ENCODER CARD BEFORE POTTING

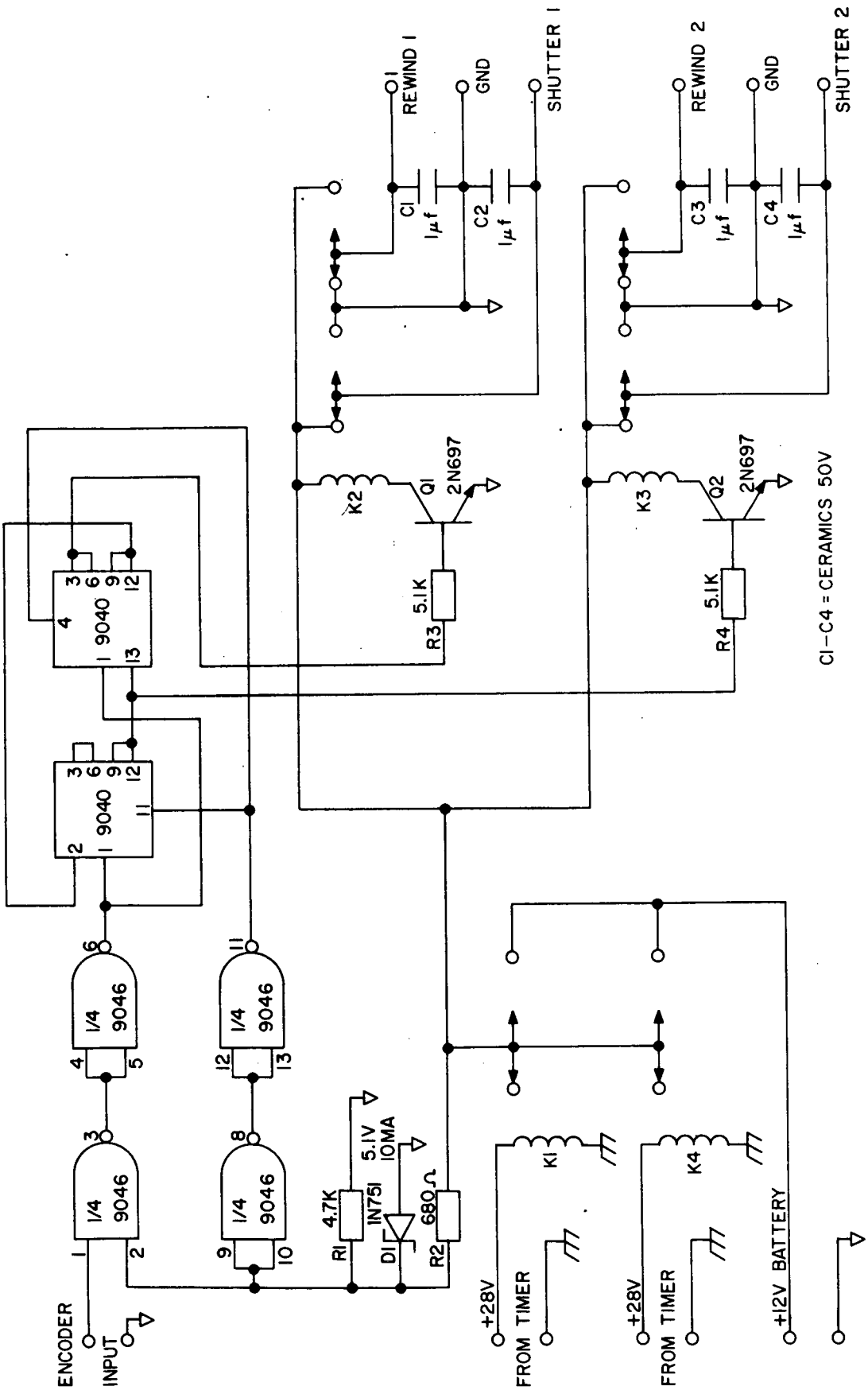


FIGURE 60. CAMERA DRIVE CIRCUIT

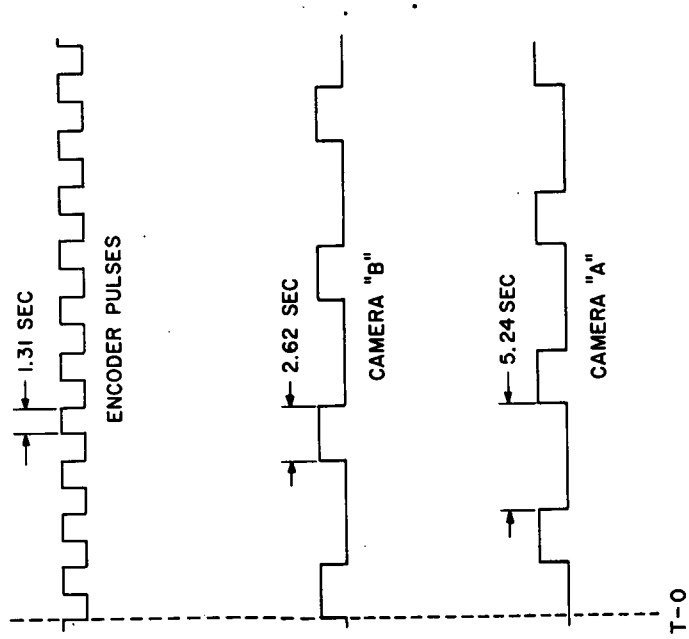


FIGURE 61. CAMERA TIMING

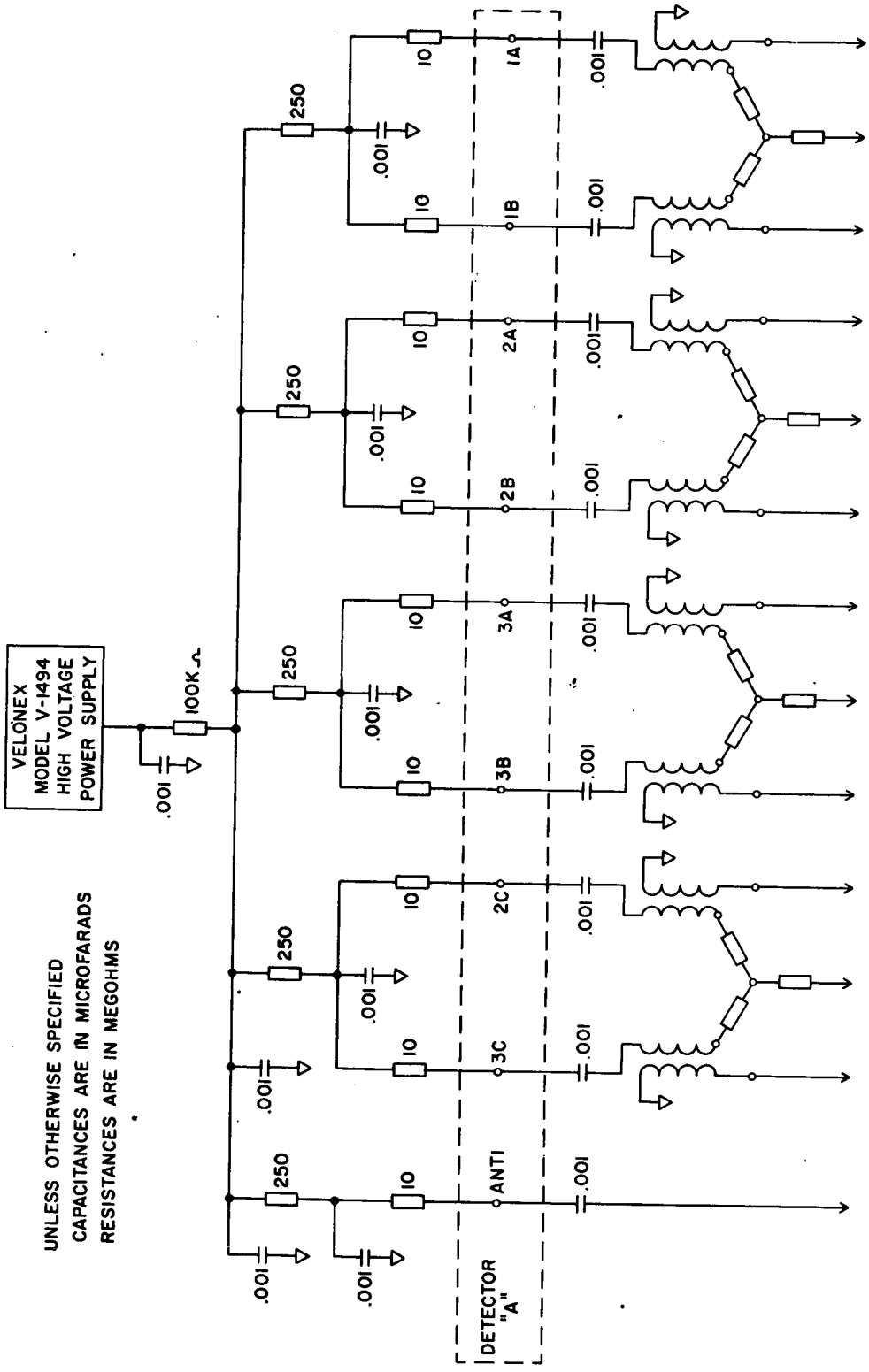


FIGURE 62. HIGH VOLTAGE DISTRIBUTION

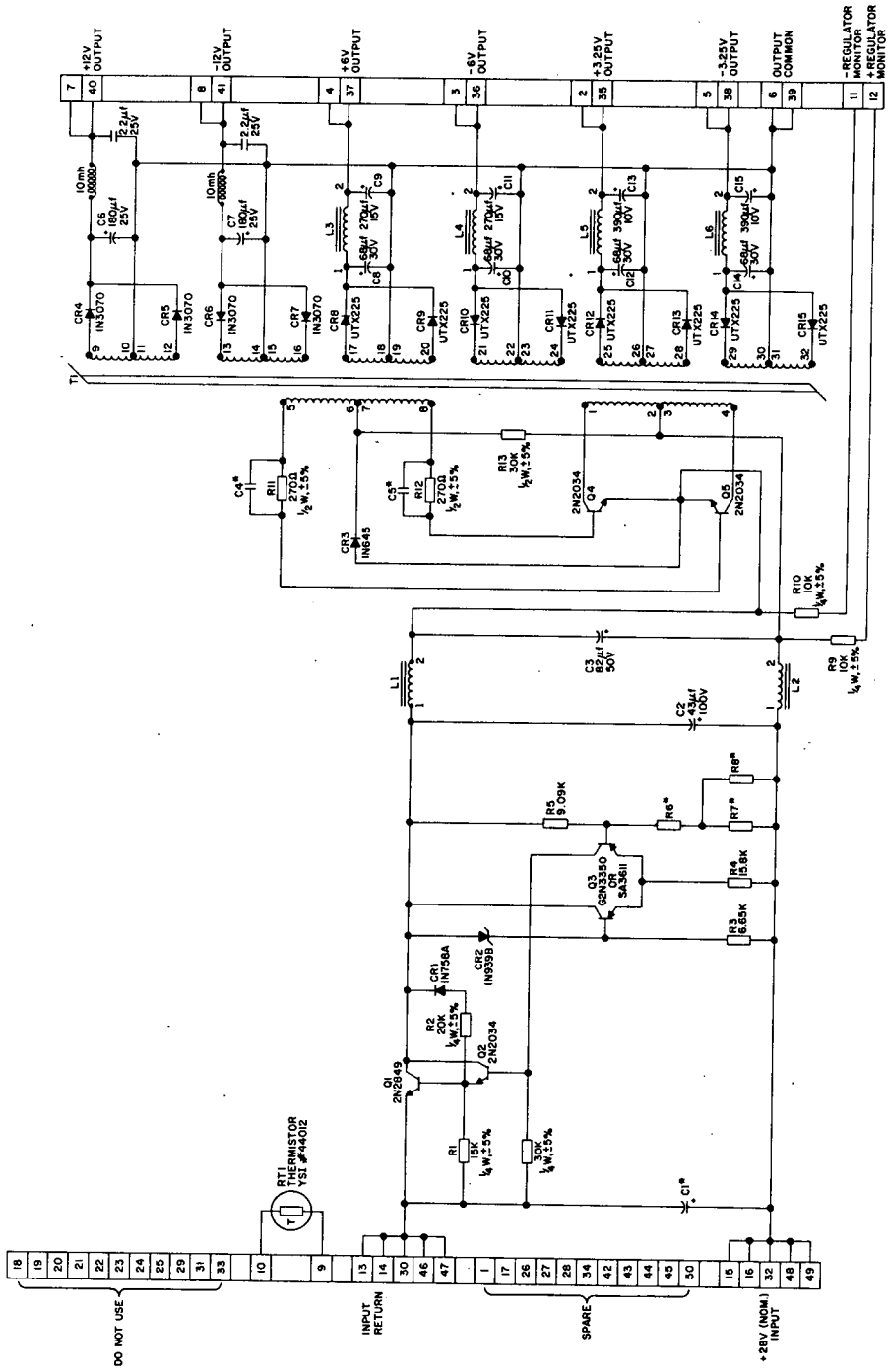


FIGURE 63. LOW VOLTAGE CONVERTER

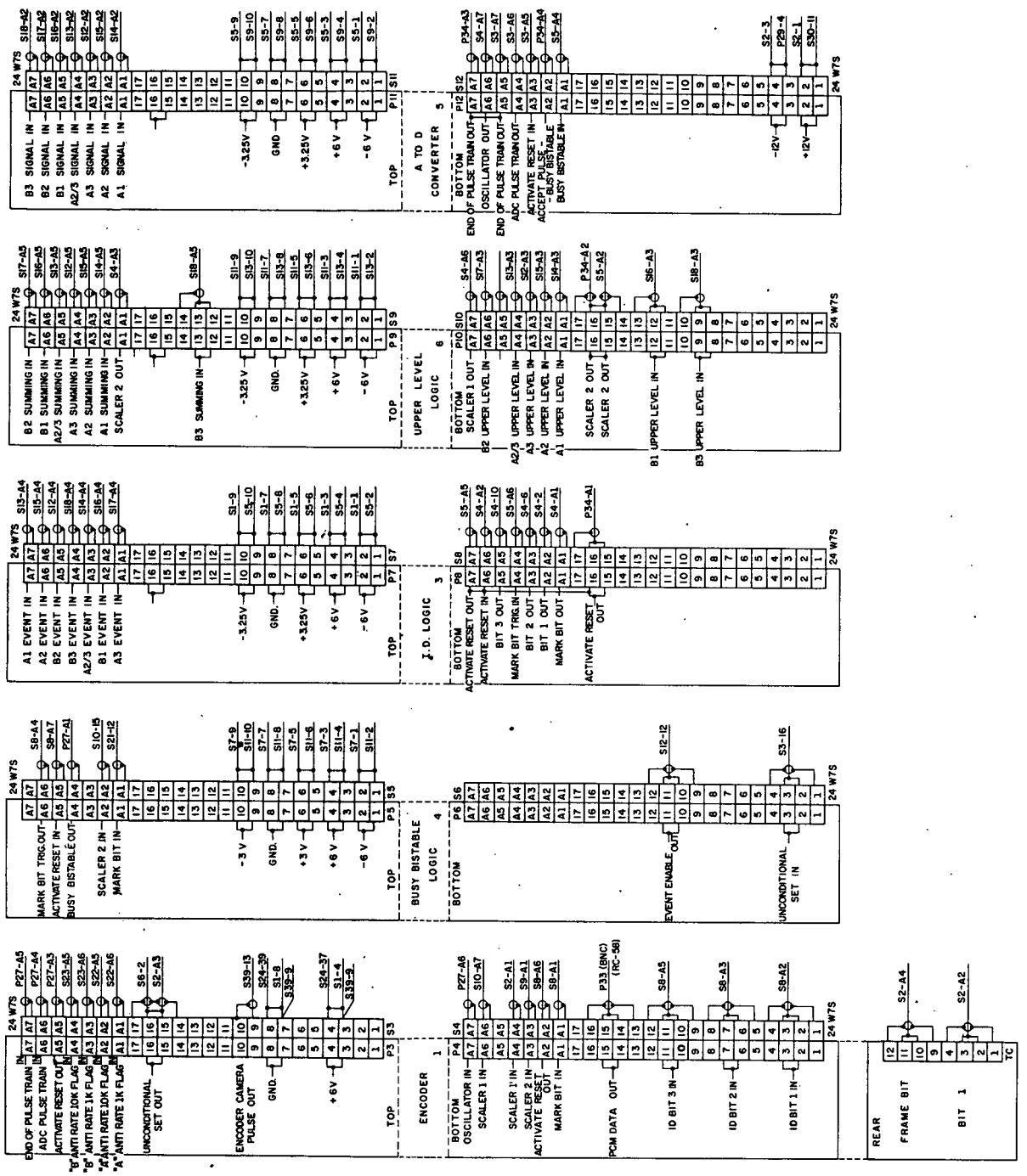


FIGURE 64. WIRING HARNESS - CARDS 1 through 6

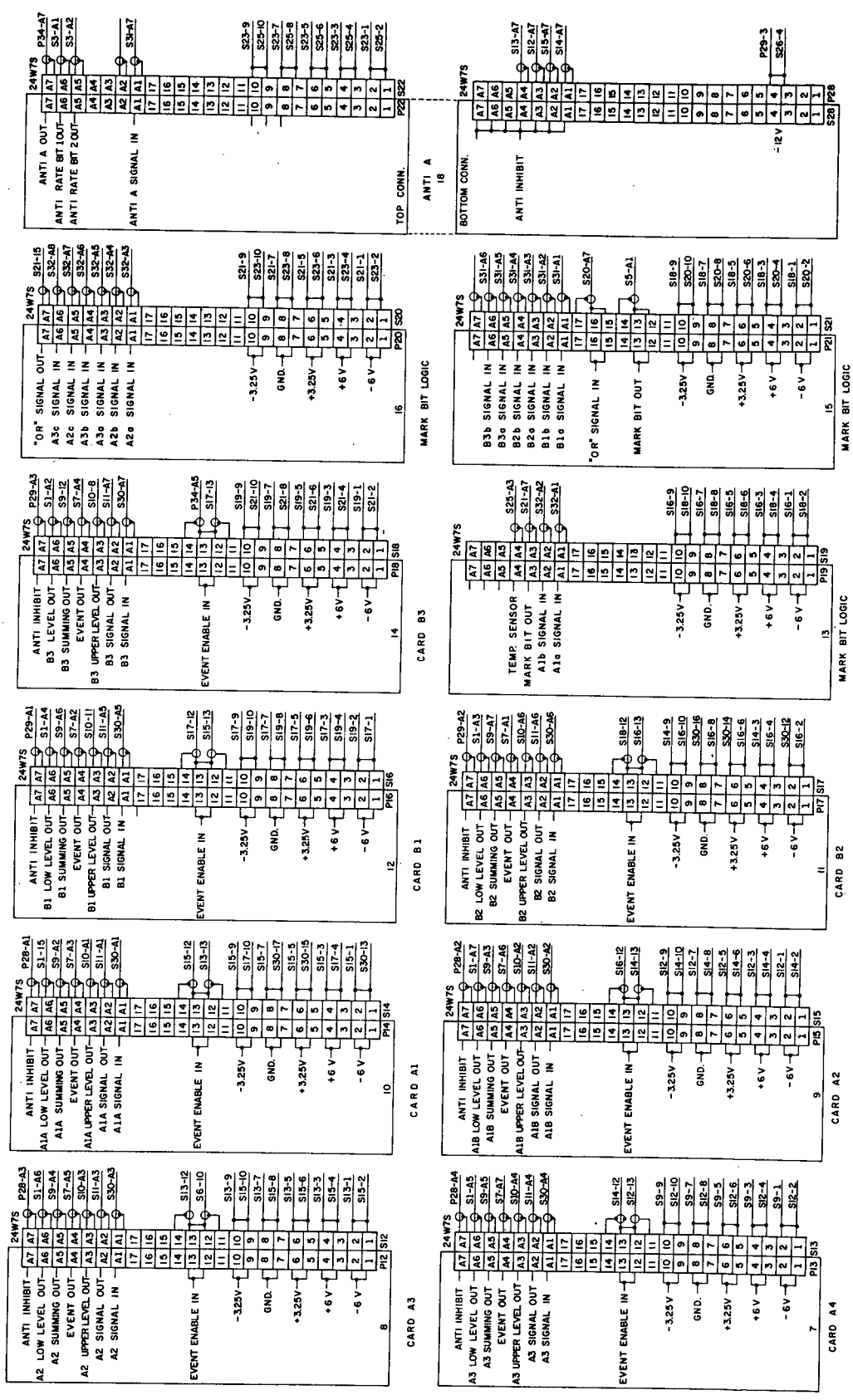


FIGURE 65. WIRING HARNESS - CARDS 7 thru 16, plus 18

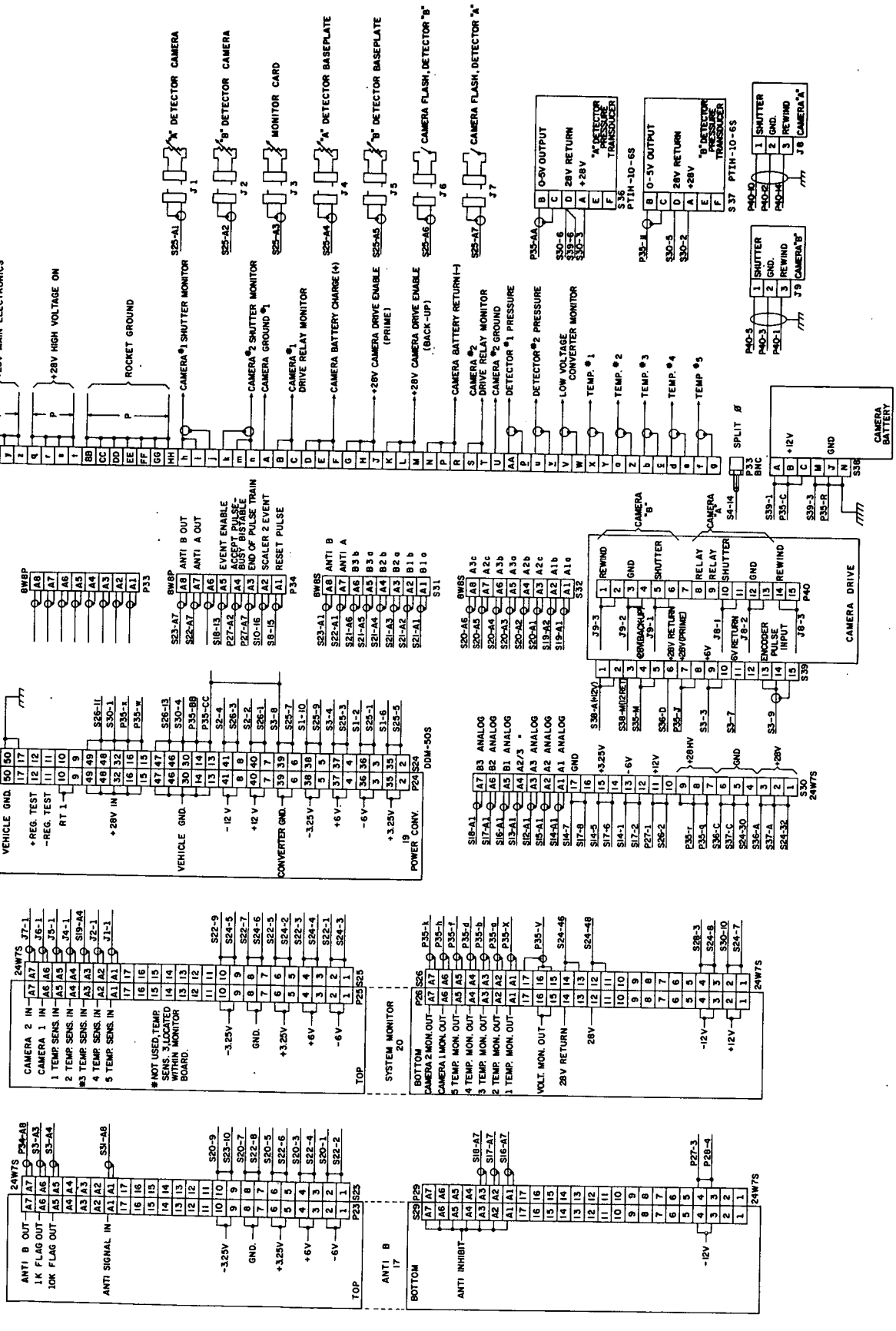
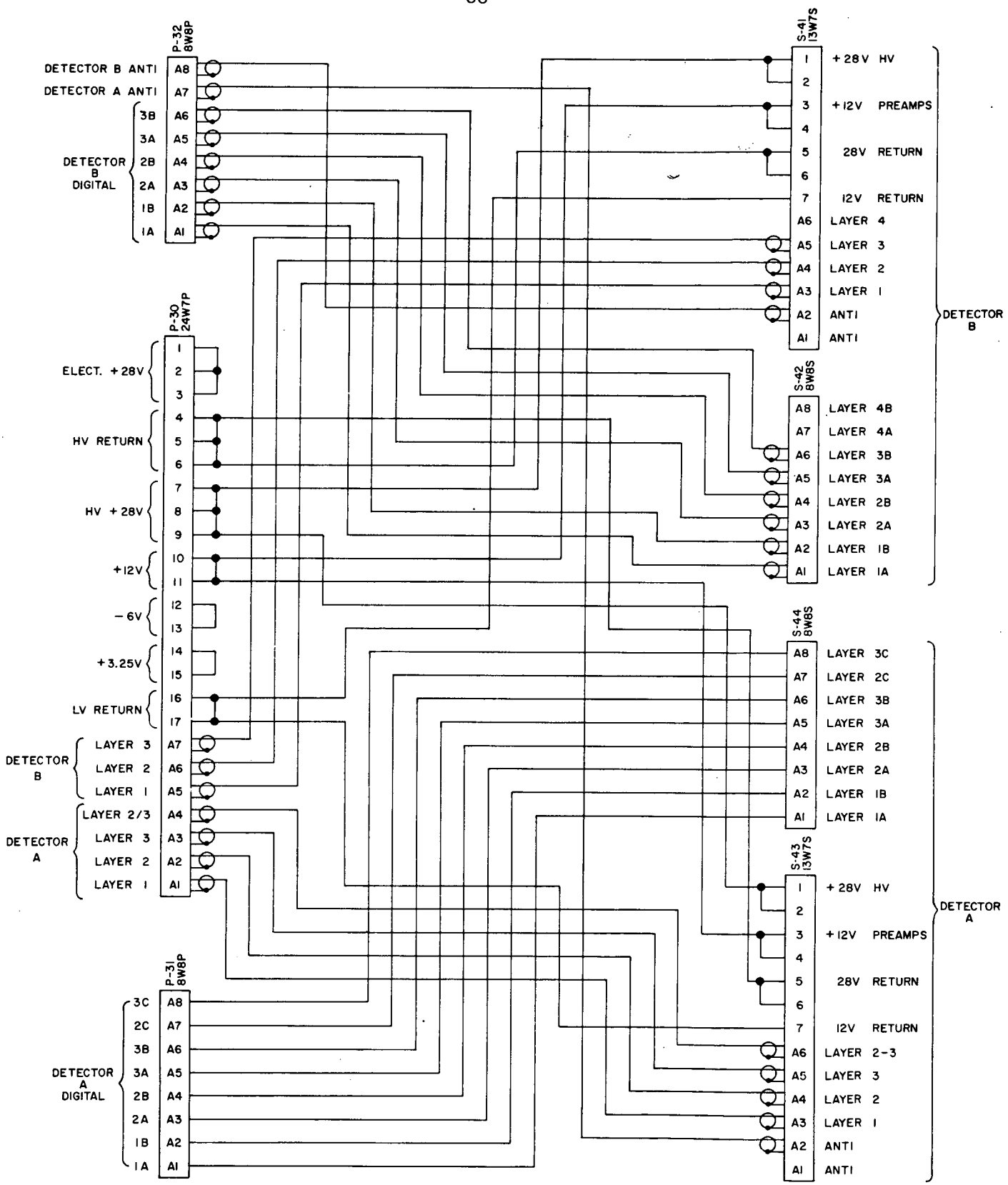
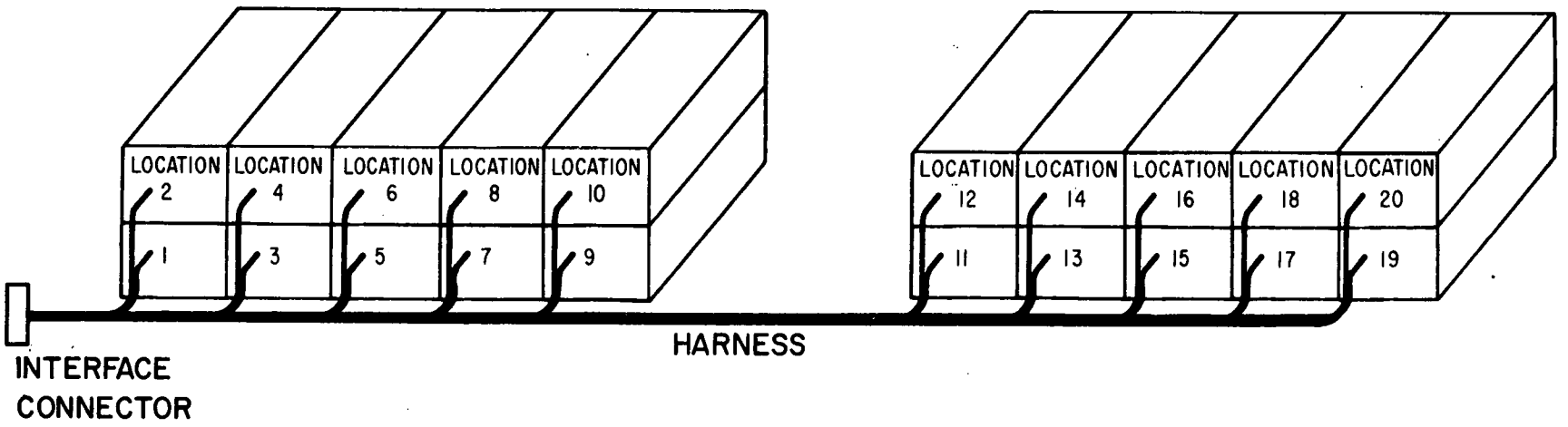


FIGURE 66. WIRING HARNESS - Cards 17, 19,20 & interconnections



INTERFACE CABLE DETECTORS TO ELECTRONICS

FIGURE 67.



MAIN ELECTRONIC CARD LOCATIONS

FIGURE 68.

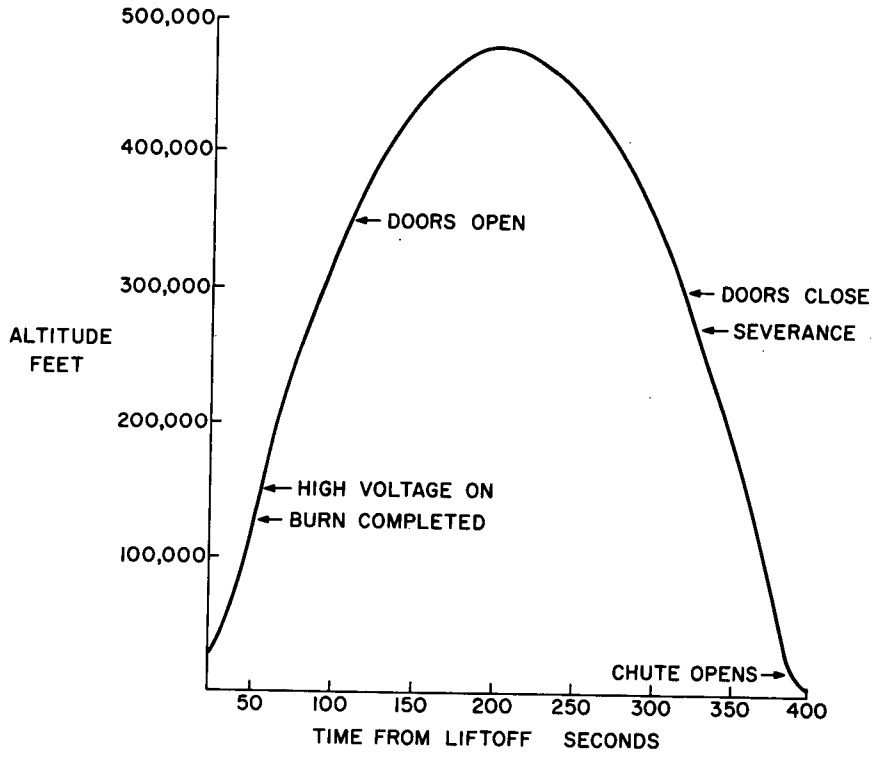


FIGURE 69. ESTIMATED FLIGHT PROFILE