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DEVELOPMENT OF ION IMPLANTED GALLIUM ARSENIDE TRANSISTORS

JANUARY 1972

BY

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PREPARED UNDER CONTRACT NAS 1-10503

BY

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FOR

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

1. Report No. CR-112037	2. Government Accession No.	3. Recipient's Catalog No.	
4. Title and Subtitle Development of Ion Implanted Gallium Arsenide Transistors		5. Report Date January 1972	
		6. Performing Organization Code	
7. Author(s) R. Hunsperger and R. Baron		8. Performing Organization Report No.	
9. Performing Organization Name and Address Hughes Research Laboratories 3011 Malibu Canyon Road Malibu, California 90265		10. Work Unit No.	
		11. Contract or Grant No. NAS 1-10503	
12. Sponsoring Agency Name and Address National Aeronautics and Space Administration Langley Research Center Hampton, Virginia 23365		13. Type of Report and Period Covered Final Technical 22 December through 22	
		14. Sponsoring Agency Code December 1971	
15. Supplementary Notes			
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17. Key Words (Suggested by Author(s)) Ion Implantation GaAs Bipolar Transistors		18. Distribution Statement	
19. Security Classif. (of this report) Unclassified	20. Security Classif. (of this page) Unclassified	21. No. of Pages 84	22. Price*

For sale by the National Technical Information Service, Springfield, Virginia 22151

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FOREWORD

This is the Final Report on Contract NAS 1-10503. The work reported herein was accomplished by Hughes Research Laboratories, 3011 Malibu Canyon Road, Malibu, California 90265. This report covers the period of 22 December 1970 through 22 December 1971. Ten previous monthly technical letter reports concerning Development of Ion Implanted GaAs Transistors are dated 15 February 1971 through 15 November 1971. The NASA-Langley program monitor for this contract was Dr. J. Robertson. The principal investigators on this contract were R. Hunsperger and R. Baron. Technical assistance was provided by D.M. Jamba, J.K. Neeland, D. Loper, R.G. Wilson, and E. Wolf. O.J. Marsh, Assistant Manager of the Chemical Physics Department, provided technical supervision for the project.

ABSTRACT

The goal of this program was to develop techniques for creating bipolar microwave transistors in GaAs by ion-implantation doping and to investigate the characteristics of these devices. Early in the contract period we measured the electrical properties of doped layers produced by the implantation of the light ions Be, Mg, and S, which are suitable for forming the relatively deep base-collector junction at conveniently low ion energies. We also determined the electrical characteristics of ion implanted diodes of both the mesa and planar type. This work led to the fabrication of n-p-n planar transistor structures by implantation of Mg to form the base regions and Si to form the emitters. These devices were found to have reasonably good base-collector and emitter-base junctions but the current gain β was immeasurably small. The low β was attributable to radiative recombination in the base region, which was excessively wide.

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S E C T I O N I

INTRODUCTION AND SUMMARY

The goal of this program was to develop techniques for creating bipolar microwave transistors in GaAs by ion implantation doping and to investigate the operating characteristics of these devices.

There are basically three important problems involved in the fabrication of ion implanted bipolar microwave transistors in GaAs. First, one must be able to create the step-like carrier concentration profile with a very thin base layer (shown in Fig. 1) that is required for theoretically optimum design.¹ Second, the required concentrations (N_E , N_B , N_C) of electrically active dopant atoms must be obtained, and finally, ion implantation-caused lattice damage must be removed by suitable annealing procedures to produce high mobility, trap-free material. Substantial progress has been made toward the solution of all three of these problems during the year's work on this contract.

Since no dopant had been adequately tested experimentally that could be used to fabricate the required several tenths micron deep base-collector junctions at conveniently low ion energies, work performed during the early months of the contract period was directed toward testing light dopants with relatively large penetration depths.* Hall measurements were made of the electrical properties of p-type layers produced by implantation of either Be or Mg and also those of n-type layers created by S implantation.

* Some of the results of this work were published in the paper "Mg and Be Ion Implanted GaAs," by R.G. Hunsperger, R.G. Wilson, and D.M. Jamba, Journal of Applied Physics, 43, 1318 (1972) included as Appendix B of this report.

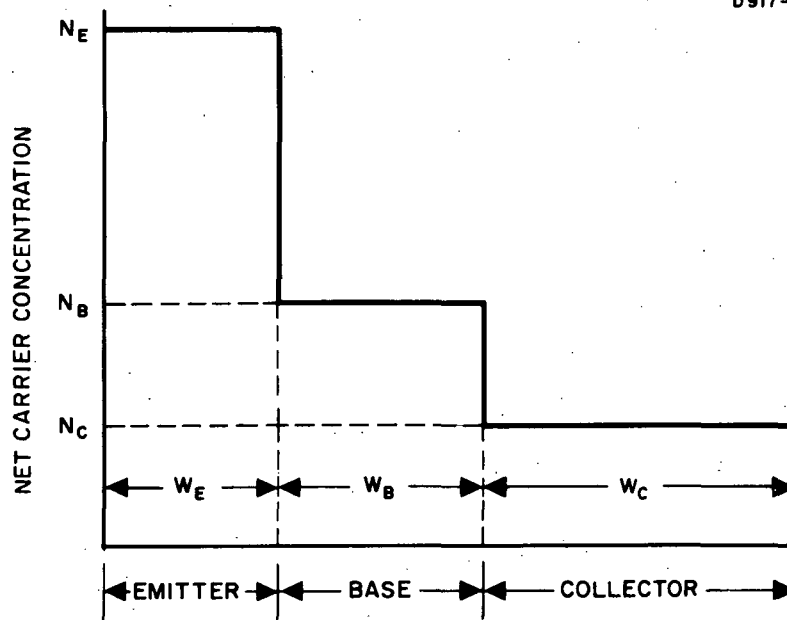


Fig. 1. Optimum Impurity Profile for a High Frequency Transistor (as Determined by Fujinuma, et al.¹)

The carrier concentration profiles and resulting junction depths in Be or Mg implanted samples were investigated. A number of different measurement techniques were utilized, including angle sectioning and etch staining, scanning electron microscope measurements, argon ion beam sputtering for layer removal, and capacitance-voltage measurements. All four techniques were successful in part, but adequate determination of the concentration profiles for the dopants of interest over a broad range of implantation and anneal conditions could not be completed during the contract period. In general, the results obtained thus far have shown the depth of penetration of Mg, Be, or S ions to be greater than or equal to the depth predicted by the Lindhard-Scharff-Schiott theory, and in some cases to be dependent on the anneal temperature. Much work is needed to understand (and ultimately control) the concentration profiles of implanted ions in GaAs.

One of the major objectives leading to transistor fabrication is to determine the electrical properties of junction diodes produced in GaAs by ion implantation. Thus, as part of the work under this contract, we examined the dc voltage-current characteristics of both planar and mesa diodes formed by Cd ion implantation. The planar diodes were superior to the mesa devices in terms of leakage current, which led us to design and fabricate a rudimentary ion implanted transistor structure using planar technology.

The transistor structures were fabricated by implanting n-type substrates with 45 keV Mg ions to form the base regions and subsequently implanting them with 20 keV Si ions to form the emitters. After the devices were suitably annealed and electrical contacts were provided, they were found to have good emitter-base and base-collector junctions, with breakdown voltages of 15 and 25 V, respectively. However, the devices had no measurable gain; β was ≈ 0 , apparently, because the base width far exceeded the calculated value of 500 Å. Observation of the devices under test with an infrared image converter showed strong luminescence in the base region.

During the course of the work, technological problems were encountered, such as making good low resistance ohmic contacts to thin ion implanted n-type layers and forming protective thin film coatings that would withstand annealing cycles and other processing steps. Techniques were found to solve, or at least greatly mitigate, these problems.

Fabrication of these rudimentary devices has served to point out technological problems, such as oxide lifting during annealing and the difficulty of making low resistance ohmic contacts to thin, ion implanted, n-type layers. It has also demonstrated the need for implanted ion concentration profile data, which are presently unavailable. However, the fact that n-p-n transistor structures have been made,

despite these yet unsolved problems, gives strong support to the idea that ion implanted bipolar GaAs transistors are indeed feasible. In addition, the work has established the following important facts.

- It is possible to fabricate an n-p-n structure in GaAs by "double" implantation of both n- and p-type dopant atoms, followed by annealing.
- During annealing, sufficient radiation damage can be removed to produce "back-to-back" diodes with relatively low reverse leakage current.
- The observation of strong luminescence when the emitter-base junction was forward biased indicated that minority carrier lifetime in the base region was at least as long as the lifetime for radiative recombination. Since this radiative lifetime puts a fundamental upper limit on diffusion length in GaAs, one can conclude that minority carrier lifetime (or diffusion length) in a properly annealed ion implanted transistor is not limited by residual radiation damage.

S E C T I O N I I

DOPANT STUDIES

Work done prior to the beginning of this contract (on the related contract NAS-12-124) demonstrated that shallow p-type layers of relatively high carrier concentration and mobility, suitable for emitter junction fabrication, could be formed in GaAs by Zn or Cd ion implantation. It was also known that similar n-type layers could be formed by implantation of Te,² Se,³ Si,⁴ and Sn.⁵ However, no dopant had been adequately tested experimentally that could be used to fabricate the required several tenths micron deep base-collector junctions at conveniently low ion energies (say, below 100 keV). Thus, work performed during the early months of this contract period was directed toward testing light dopants with relatively large penetration depths, particularly the p-type dopants Mg and Be and the n-type dopant S.

A. SULFUR IMPLANTATION

Since much information about S implanted GaAs was already available,^{4,6} we performed only one additional experiment to determine if outdiffusion of sulfur was significant during implantation at room temperature. (We had observed outdiffusion of sulfur implanted at 400°C without an oxide coating and in samples implanted at room temperature but heated to 400°C during deposition of an oxide coating.)

Samples were prepared by implantation of 100 keV sulfur ions into p-type substrates at room temperature. Prior to implantation, the samples were coated with a 700 Å thick layer of sputtered SiO₂ to limit possible outdiffusion of the

sulfur and also to minimize ion channeling. Following implantation these samples were annealed at 800°C, and Hall measurements of the electrical properties were made using the van der Pauw technique.⁷ The carrier concentrations and mobilities for these samples, shown in Table I, are about the same as have been observed previously for identically implanted samples without the SiO₂ coating.⁶ Thus, outdiffusion of the dopant sulfur does not appear to be a problem at room temperature. The conclusion we reach is that it is not necessary to implant sulfur through an oxide at room temperature to prevent outdiffusion, but that a protective oxide layer should be deposited (at room temperature) before the sample is annealed.

The junction depths in these samples were measured by the angle section and stain technique after they had been annealed for 15 min at 800°C. The depth in samples implanted with 5×10^{14} ions/cm² was 0.24 μ m while it was equal to 0.3 μ m in samples implanted with 1.1×10^{15} ions/cm². Thus, as expected, sulfur implantation does yield deeper junctions than cadmium (of the same or lesser energy); much of the greater depth appears to be caused by diffusion of the implanted sulfur ions during implantation and/or annealing. (The Lindhard-Scharff-Schiøtt⁸ predicted penetration depth for 100 keV S⁺ in GaAs is only ≈ 700 Å.) The carrier concentration, mobilities, and junction depths shown in Table I indicate that it is reasonable to use such implantations to form the base regions of p-n-p transistors.

B. MAGNESIUM IMPLANTATION

Magnesium implanted layers were investigated because we anticipated that such doping would be very useful in forming the base regions of n-p-n transistors, since Mg

penetrates relatively deeply because of its small mass; the profile should be easily controllable because the critical angle for channeling is very small.

A hot cathode, electron-bombardment ion source was used to produce the Mg ions, as described in Appendix A.

The GaAs substrates used in these experiments were $\langle 111 \rangle$ oriented wafers ($\pm 3^\circ$), with the B-face chemically polished prior to implantation. The wafers were intentionally misaligned 8° with the ion beam during implantation to minimize ion channeling. Implantation was performed with the substrates at room temperature, and the samples were subsequently coated with a 2000 Å thick sputtered layer of SiO_2 prior to annealing at higher temperatures in a flowing N_2 atmosphere to prevent outdiffusion of the dopant and dissociation of the GaAs.

The carrier concentration per cm^2 N_S and the effective mobility μ in the p-type layers produced by ion implantation and annealing were measured using the van der Pauw-Hall technique.⁷ The substrates used were n-type, with $n = 1 \times 10^{16} / \text{cm}^3$, so that the p-n junction between the implanted layer and the substrate would provide electrical isolation during measurement.

TABLE I

Carrier Concentration and Mobilities for GaAs Samples
Implanted with 100 keV Sulfur Ions

Samples (100 keV S^+ → GaAs)	Carrier Concentration N_S , cm^{-2}	Mobility μ_m , $\text{cm}^2/\text{V sec}$	Sheet Resistivity, ρ_s $\Omega/\square$	Junction Depth, μm
Dose = 5×10^{14} ions/ cm^2 implanted through 700 Å SiO_2 ; sample annealed for 15 min at 800°C .	6.6×10^{12}	1720	550	0.24
Dose = 1.1×10^{15} ions/ cm^2 implanted through 700 Å SiO_2 ; sample annealed for 15 min at 800°C .	5.9×10^{12}	1960	538	0.30

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One group of samples was prepared by implanting 45 keV Mg^+ ions in doses ranging from $5 \times 10^{13}/\text{cm}^2$ to $1 \times 10^{15}/\text{cm}^2$. They were then annealed at temperatures in the range 100° to 900°C . No p-type layer was observed in samples annealed at $\leq 500^\circ\text{C}$, but they did form in samples annealed at $\geq 600^\circ\text{C}$. The results of Hall measurements made on those samples are shown in Figs. 2 through 4. Note that for samples with ion dose $\leq 1 \times 10^{14}/\text{cm}^2$, 100% electrical activity was observed after annealing at 800°C . The surface carrier concentration (after 800°C anneal) saturated in the range of 1 to $2 \times 10^{14}/\text{cm}^2$ for samples with ion dose $> 10^{14}/\text{cm}^2$, while annealing at 850° and 900°C , produced a decrease in carrier concentration in these samples from that obtained after 800°C anneal. This decrease may be due to outdiffusion of the Mg or possibly may result from self-compensation. The maximum carrier concentration/ cm^2 that was observed corresponds roughly to a peak concentration in the implanted layer of $2 \times 10^{19}/\text{cm}^3$, which has been reported also by Kressel and Hawrylo⁹ to be the maximum concentration they observed in epitaxially grown (950°C) layers. The peak concentration/ cm^3 in the implanted layer is not known exactly, because the concentration versus depth profile was not determined. The thickness of the p-type layer in samples annealed at 800 to 900°C was approximately $0.4 \mu\text{m}$, as determined by thin layer stripping (using 2 keV Ar ion sputtering) coupled with Hall measurements. The layer thickness predicted by the Lindhard-Scharff-Schiøtt⁸ (LSS) range-energy theory is $\sim 0.12 \mu\text{m}$. Thus it is apparent that some ion channeling or diffusion did occur, and it cannot be assumed that the implanted and annealed layer has the gaussian shape predicted by the LSS theory.

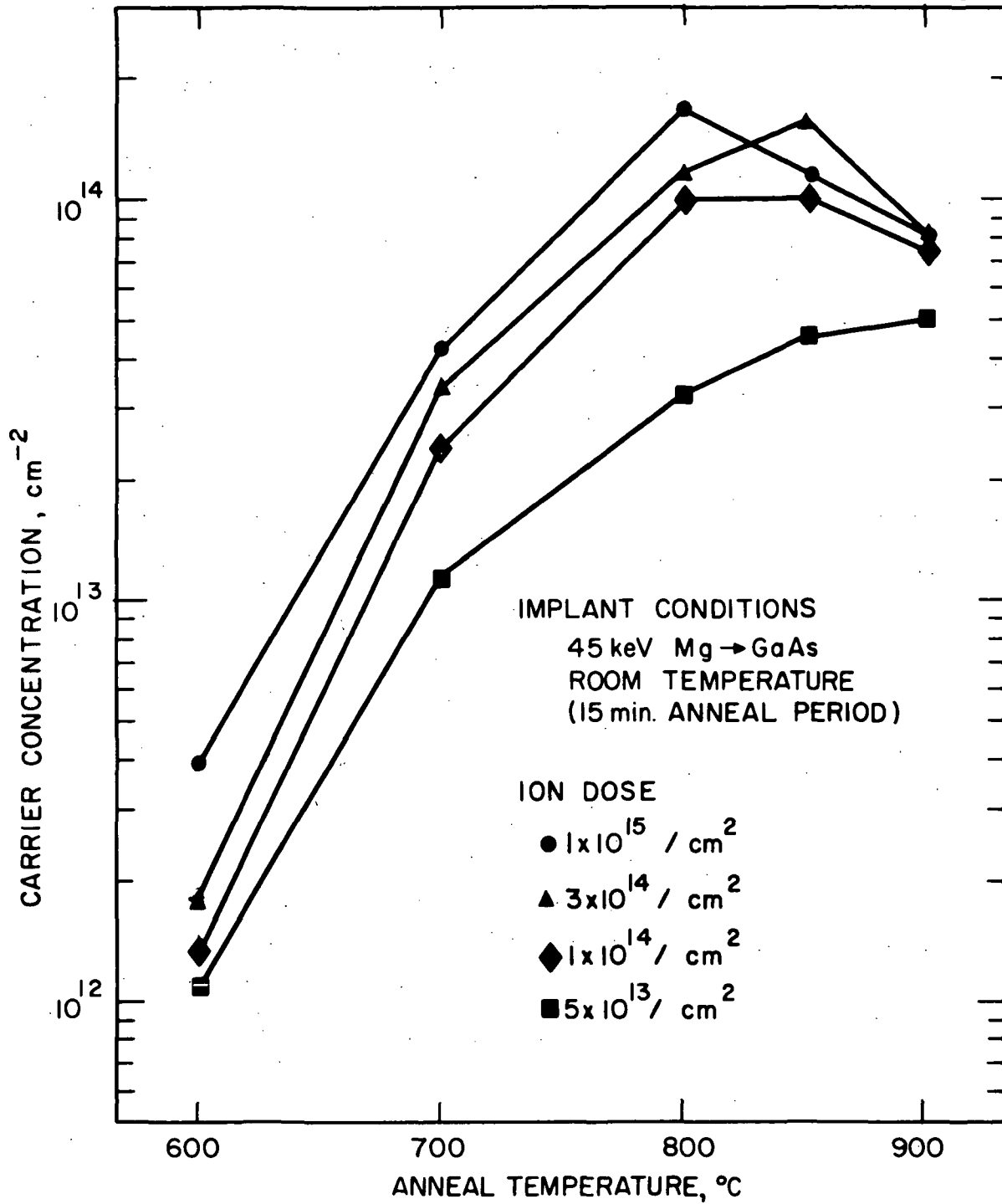


Fig. 2. Surface Carrier Concentration in Mg Implanted Layers in GaAs.

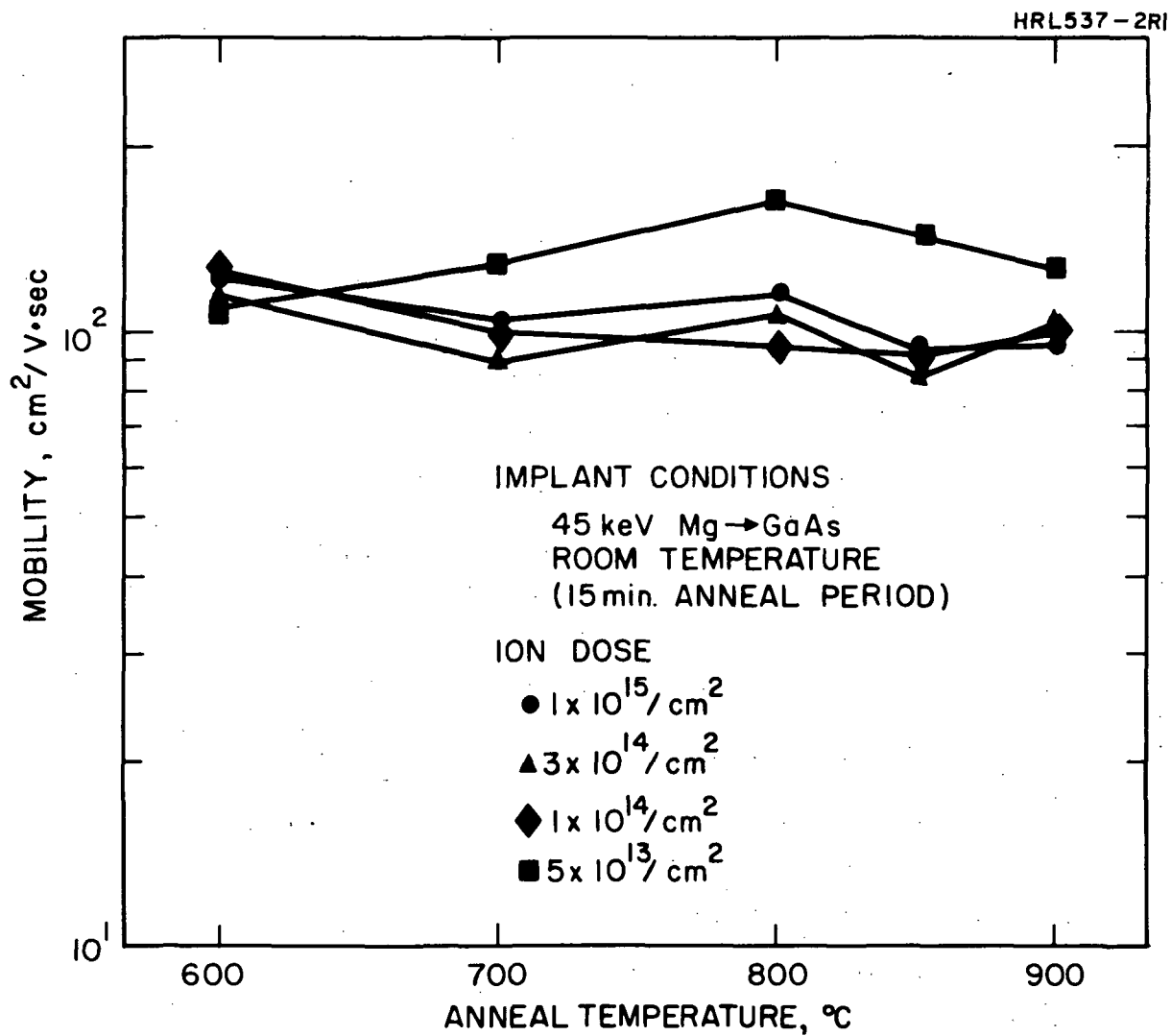


Fig. 3. Mobility in Mg Implanted Layers in GaAs.

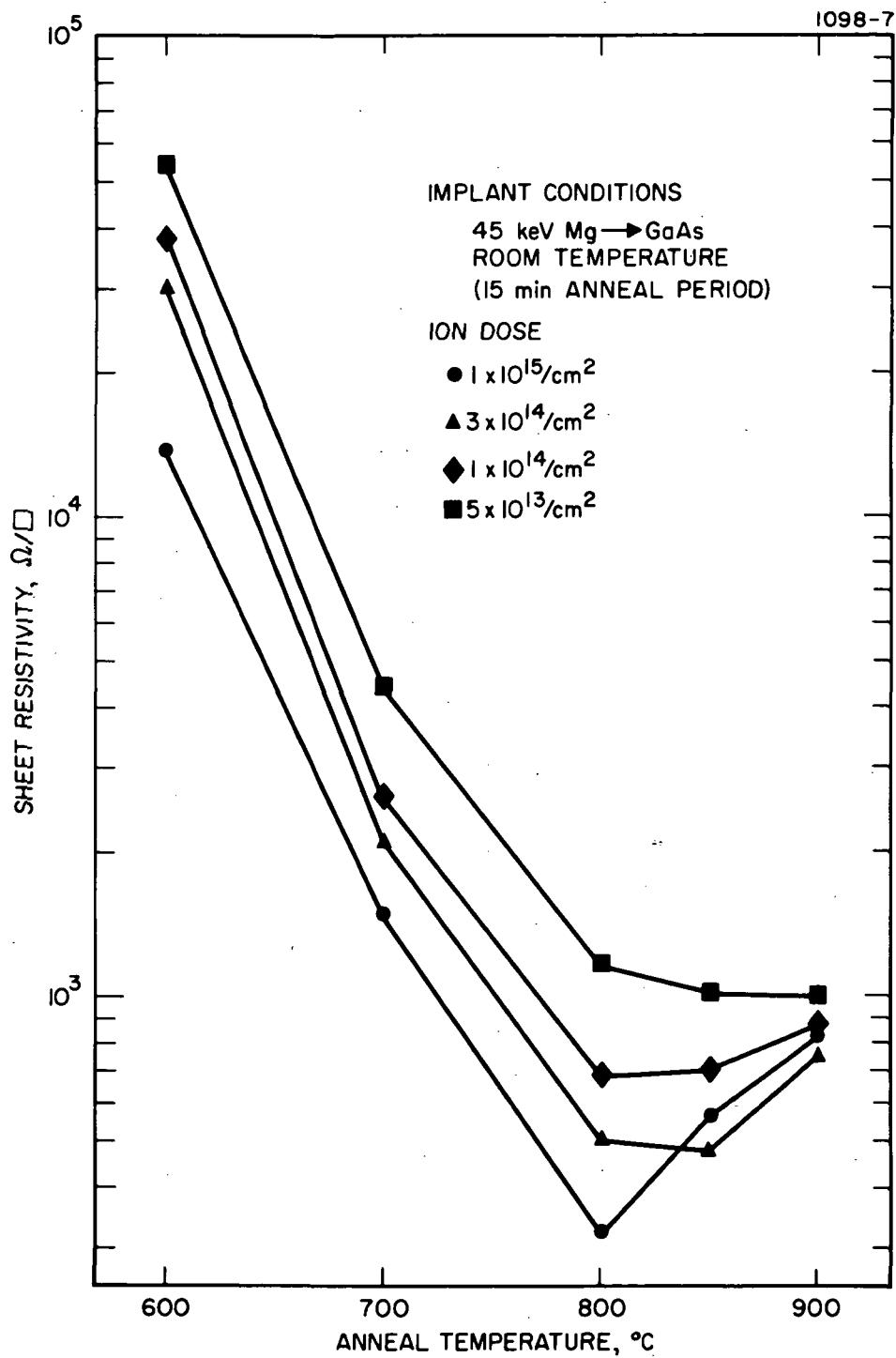


Fig. 4. Sheet Resistivity of Mg Implanted Layers in GaAs.

The fact that carrier mobility was $\sim 100 \text{ cm}^2/\text{V sec}$ even in samples annealed at only 600°C (see Fig. 3) suggests that lattice disorder produced by Mg implantation anneals at a lower temperature than that produced by the same dose of Cd or Zn ions. Cd or Zn implanted layers must be annealed at $\geq 800^\circ\text{C}$ before mobility recovers to values $\sim 100 \text{ cm}^2/\text{V sec}$ that are comparable to mobilities observed in bulk GaAs single crystals of equivalent doping concentrations.

From the data of Fig. 4, it can be seen that the sheet resistivity of these Mg implanted samples decreased with increasing anneal temperature in the range 600 to 800°C but remained relatively constant for further increase in temperature above 800°C , or in some cases even increased as a result of decreased carrier concentration.

C. BERYLLIUM IMPLANTATION

The electrical properties of p-type layers produced by room temperature implantation of 40 keV Be ions were also investigated. The substrate material and the implantation and anneal conditions were the same as those used for Mg implantation, as described in the preceding section. The required Be ions were generated by placing BeCl_2 in the axial probe of the electron-bombardment source. (Refer to Appendix A for a detailed discussion of the Be ion generation method.)

The surface carrier concentrations of p-type layers produced by room temperature implantation of 40 keV beryllium ions are shown in Fig. 5. As in the case of Mg, no p-type layer was observed until the samples were annealed. The anneal temperature required to produce a p-n junction depended on the ion dose and varied from 400°C for a sample implanted

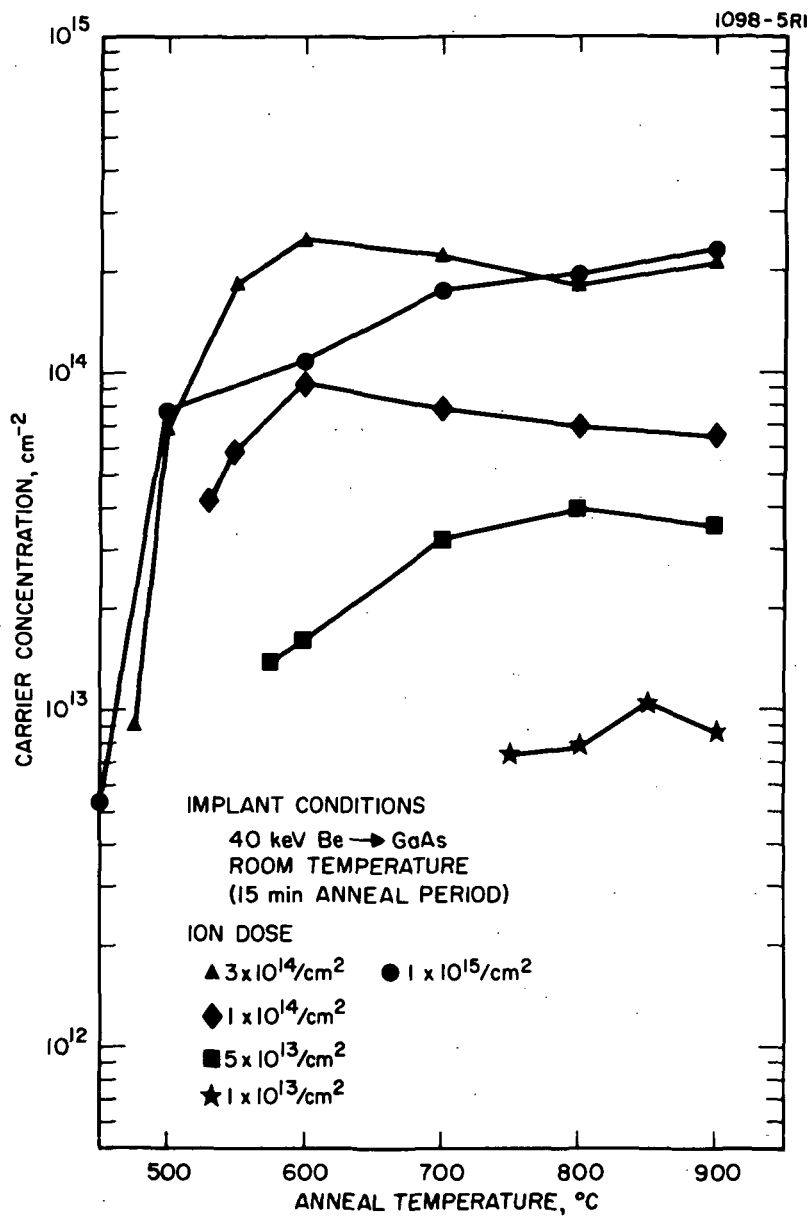


Fig. 5. Surface Carrier Concentration
in Be Implanted Layers in GaAs.

with 1×10^{15} ions/cm² to 750°C for one with ion dose = 1×10^{13} /cm². After annealing a sample with ion dose = 1×10^{15} /cm² at 400°C for 15 min, a p-type layer was observable because of the rectifying current-voltage characteristic of the junction formed at the interface with the n-type substrate. However, the resistivity of the layer was so high ($\rho_s = 1.1 \times 10^6 \Omega/\square$) that no Hall measurement of carrier concentration or mobility could be made. Annealing at temperatures of 450°C and higher produced lower resistivity p-type layers for which Hall measurements could be made. The data are plotted in Fig. 5, along with data for samples implanted with lower ion dose. The maximum carrier concentration reached was only about 20% of the total of 1×10^{15} ions/cm² that were implanted, as compared to the >80% electrical activity observed in the case of samples implanted with 3×10^{14} Be⁺/cm². Also, it is interesting to note that carrier concentration increased more slowly with anneal temperatures for the samples implanted with 1×10^{15} Be⁺/cm² than for those implanted with 3×10^{14} /cm², even though mobility recovered to values ~ 100 cm²/V sec after annealing at temperatures as low as 450°C. A possible explanation is that Be atoms, remaining in interstitial sites or in defect complexes after saturation of substitutional Be is reached at a given temperature, may act as compensating centers. The fact that mobility was greater than 100 cm²/V sec as shown in Fig. 6, then implies that many of the implanted atoms form electrically neutral centers, because ionized impurity scattering would cause a significantly lower mobility if all of the implanted atoms were charged. An alternate explanation is that we were observing the effects of differences in the implanted ion concentration profile with depth in samples implanted with different ion doses. A concentration of 2×10^{14} /cm² electrically active atoms distributed over a shallow depth would cause a lower measured average mobility

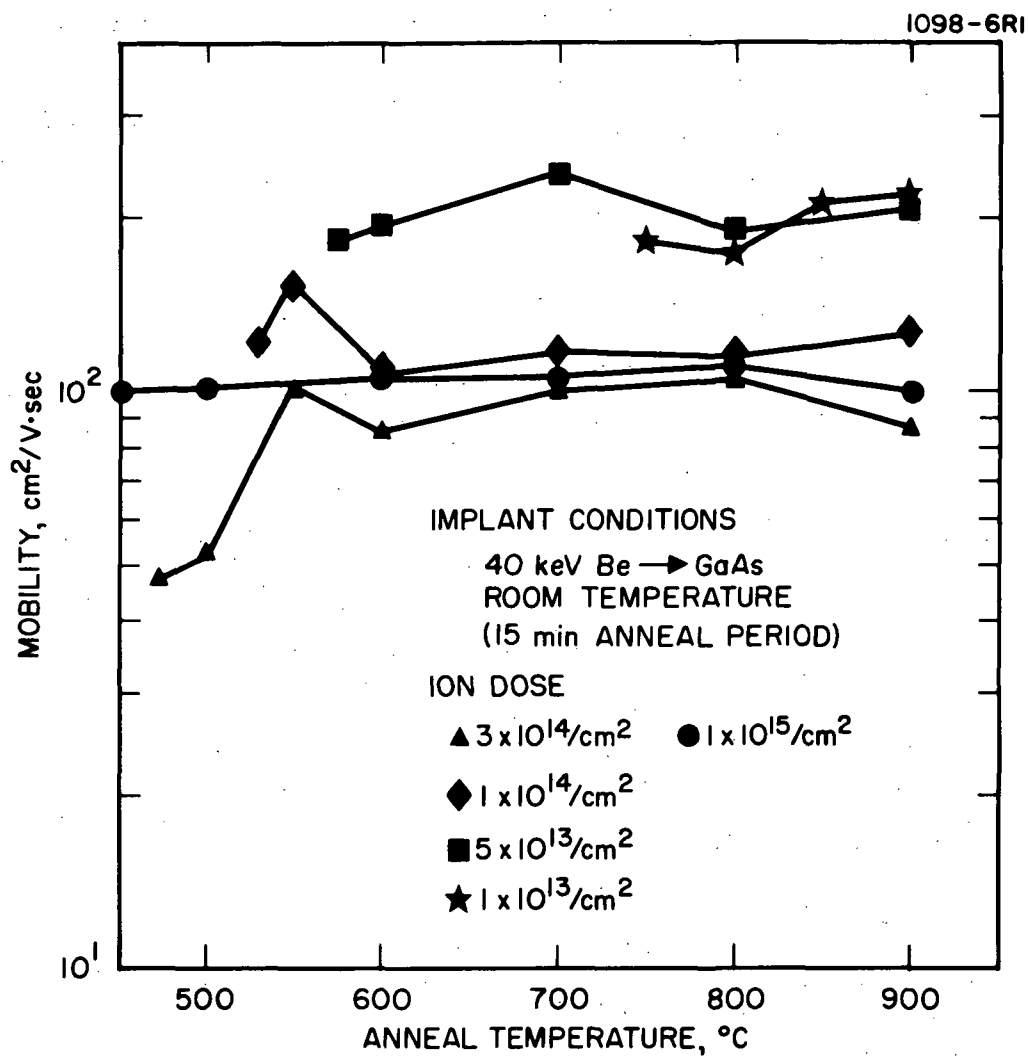


Fig. 6. Mobility in Be Implanted Layers in GaAs.

than would be caused by the same concentration per cm^2 spread over greater depth, because the contribution from regions of lower concentration per cm^3 would be greater in the latter case. Measurement of the implanted ion concentration profile is necessary to establish which explanation is correct.

In the case of samples implanted with $\geq 1 \times 10^{14}$ ions/ cm^2 , maximum electrical activity (>80% of the implanted ions electrically active) was observed after annealing at only 600°C . This temperature is considerably lower than 800°C , which has been found to be the temperature required to produce maximum electrical activity in Mg implanted layers and also in Cd, Zn, Si, or S implanted layers.^{4,6,10} The anneal behavior of carrier mobility indicates that recovery of the lattice from implantation-caused damage occurs at a relatively low temperature, since μ rises to a reasonable value for bulk p-type material (in the range 100 to 200 $\text{cm}^2/\text{V sec}$) after annealing at as low as 550°C , and then the curves of μ versus temperature are relatively flat for higher temperatures. It is interesting to note that samples implanted with ion dose $\geq 1 \times 10^{14}/\text{cm}^2$ reach 80% electrical activity after annealing at 600°C , while samples implanted with smaller doses require annealing at higher temperatures before the same percentage of the implanted ions are electrically active. Thus it appears that a certain amount of lattice disorder is conducive to movement of the ions to lattice sites in which they are electrically active, presumably substitutional positions.

The variation of sheet resistivity as a function of ion dose and anneal temperature is shown in Fig. 7. The minimum ρ_s observed was approximately 300 $\Omega/\square$, as in the case of Mg implanted samples, but the anneal temperature required to reach that value was only 550°C compared to 800°C for Mg.

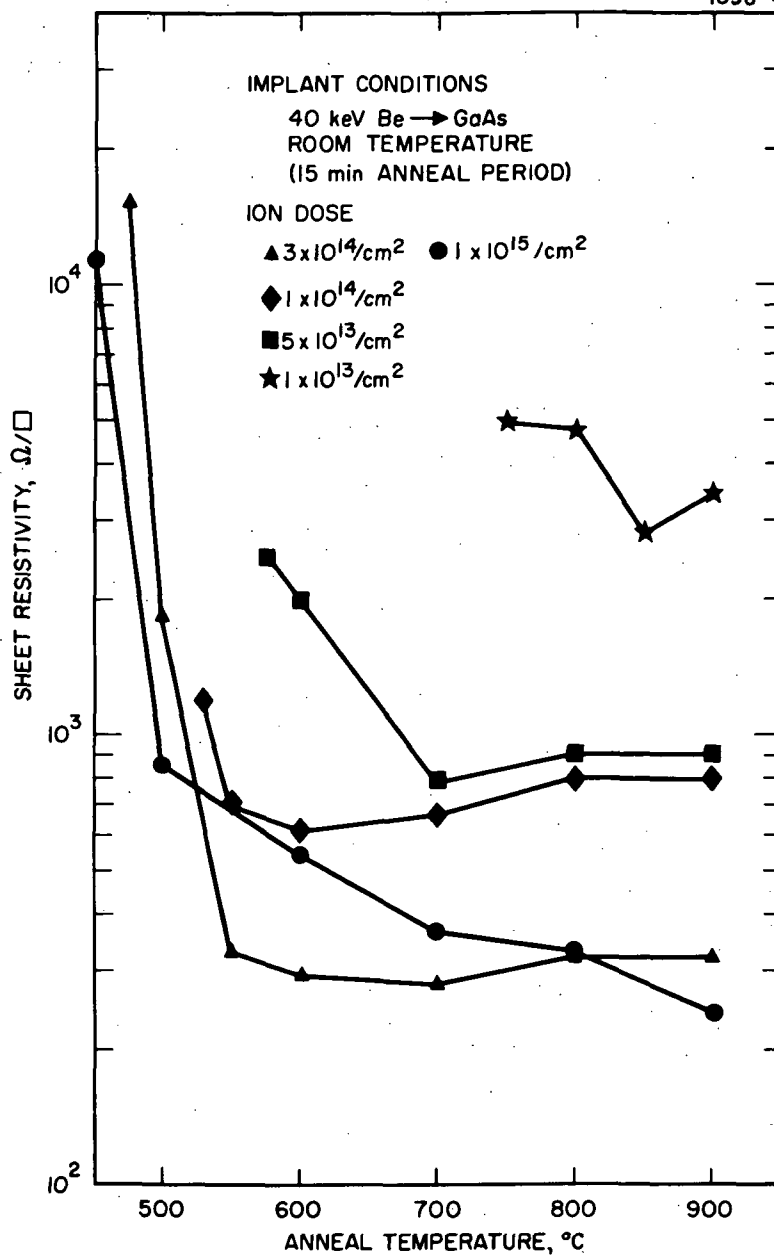


Fig. 7. Sheet Resistivity of Be Implanted Layers in GaAs.

D. ACTIVATION ENERGY OF BERYLLIUM

The activation energy E_A of the Be acceptor level in GaAs has not been previously determined. A series of experiments was designed to measure E_A as a function of Be doping concentration. Four samples were multiply implanted to produce deep, uniformly doped layers of 10^{16} , 10^{17} , 10^{18} , and 10^{19} atoms/cm³, respectively. The calculated dopant profile and implant schedule are shown in Fig. 8 for the 10^{17} /cm³ sample, which was the only one actually measured under this contract. The sample geometry is also shown in Fig. 8. The sample was designed for Van der Pauw-Hall measurements, with the heavily implanted contact pads in the corners allowing the use of pressure contacts. The masked areas were formed by the fingers used to hold the sample during implant and improved the geometry of the device for Van der Pauw measurements.

Because of the low doses and concentrations (as low as 10^{12} /cm² and 10^{16} /cm³) used, a substrate of very lightly doped (10^{14} /cm³) n-type GaAs was chosen. Unfortunately, after the samples were implanted, it was determined that this substrate material converts to p-type on being annealed above 650°C. Because of this, the samples were only annealed to 550°C for 15 min, which is not enough to fully anneal the implanted layers.

After anneal, the Hall effect and resistivity were measured versus temperature from 333 to 36°K. The upper temperature limit was set by the equipment, and the lower temperature limit was determined by when good contact to the sample could no longer be maintained. The Van der Pauw technique was used, and the measurements were performed on an automated Hall measurement system. This system is described in Appendix C.

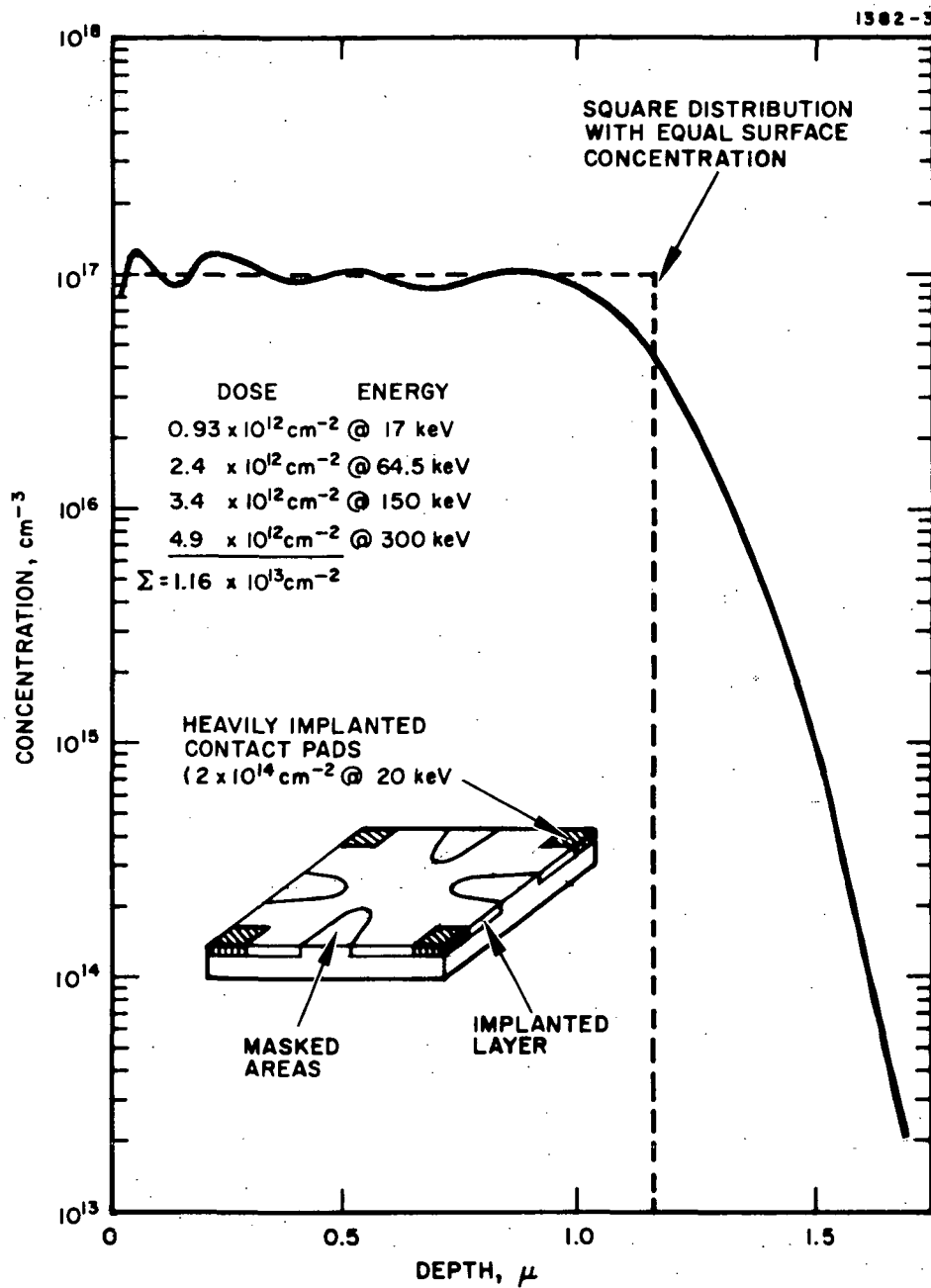


Fig. 8. Calculated Profile for Be Implanted into GaAs. Also shown are the Implant Schedule, the Uniformly Doped Distribution with Equal Surface Concentration, and the Sample Geometry.

The resulting carrier concentration p and Hall mobility μ_H are plotted versus temperature in Figs. 9 and 10. The values of p were calculated using an assumed layer depth of 1.16 μm . This is the depth of a uniformly doped layer with a concentration of $10^{17}/\text{cm}^3$ and a surface concentration of $1.16 \times 10^{13}/\text{cm}^2$, the calculated parameters for this implant (see Fig. 8). The measured values of p were fitted to

$$p = \frac{-\left(N_D + \frac{N_V e^{-E_A/kT}}{g}\right) + \sqrt{\left(N_D + \frac{N_V e^{-E_A/kT}}{g}\right)^2 + 4(N_A - N_D) \frac{N_V e^{-E_A/kT}}{g}}}{2}$$

the expected behavior for a singly ionized, nondegenerate, compensated acceptor level. The acceptor density N_A , donor density N_D , and E_A were adjusted for a least squares fit. The degeneracy of the level g was assumed to be 4, as expected for an acceptor in GaAs (a fit, assuming $g = 2$ gave significantly poorer results). The effective density of states in the valence band N_V was calculated from $N_V = 7 \times 10^{18} (T/300)^{3/2} \text{ cm}^{-3}$. The resulting values of the parameters are $E_A = 0.017_3 \text{ eV}$, $N_A = 7.3_0 \times 10^{16}/\text{cm}^3$, $N_D = 2.2_2 \times 10^{16}/\text{cm}^3$, and $\int N_A dx = 8.47 \times 10^{12}/\text{cm}^2$. The solid curve in Fig. 9 is the calculated fit, and the points are the measured values. The value determined for E_A is very reasonable, falling between $E_A = 0.012 \text{ eV}$ for Mg and $E_A = 0.019 \text{ eV}$ for C.

The values of μ_H versus temperature in Fig. 10 are also very reasonable, with the measured values having the expected $T^{-3/2}$ dependence for lattice scattering at higher temperatures. The peak mobility of $1500 \text{ cm}^2/\text{V-sec}$ at 59°K is in reasonable agreement with values for Zn doped GaAs reported by Ermanis and Wolfstirn¹¹ at somewhat higher doping levels ($[\mu_H]_{\text{peak}} = 700 \text{ cm}^2/\text{V-sec}$ at $T = 90^\circ\text{K}$ for the lowest concentration reported, $N_A = 1.275 \times 10^{17}/\text{cm}^3$).

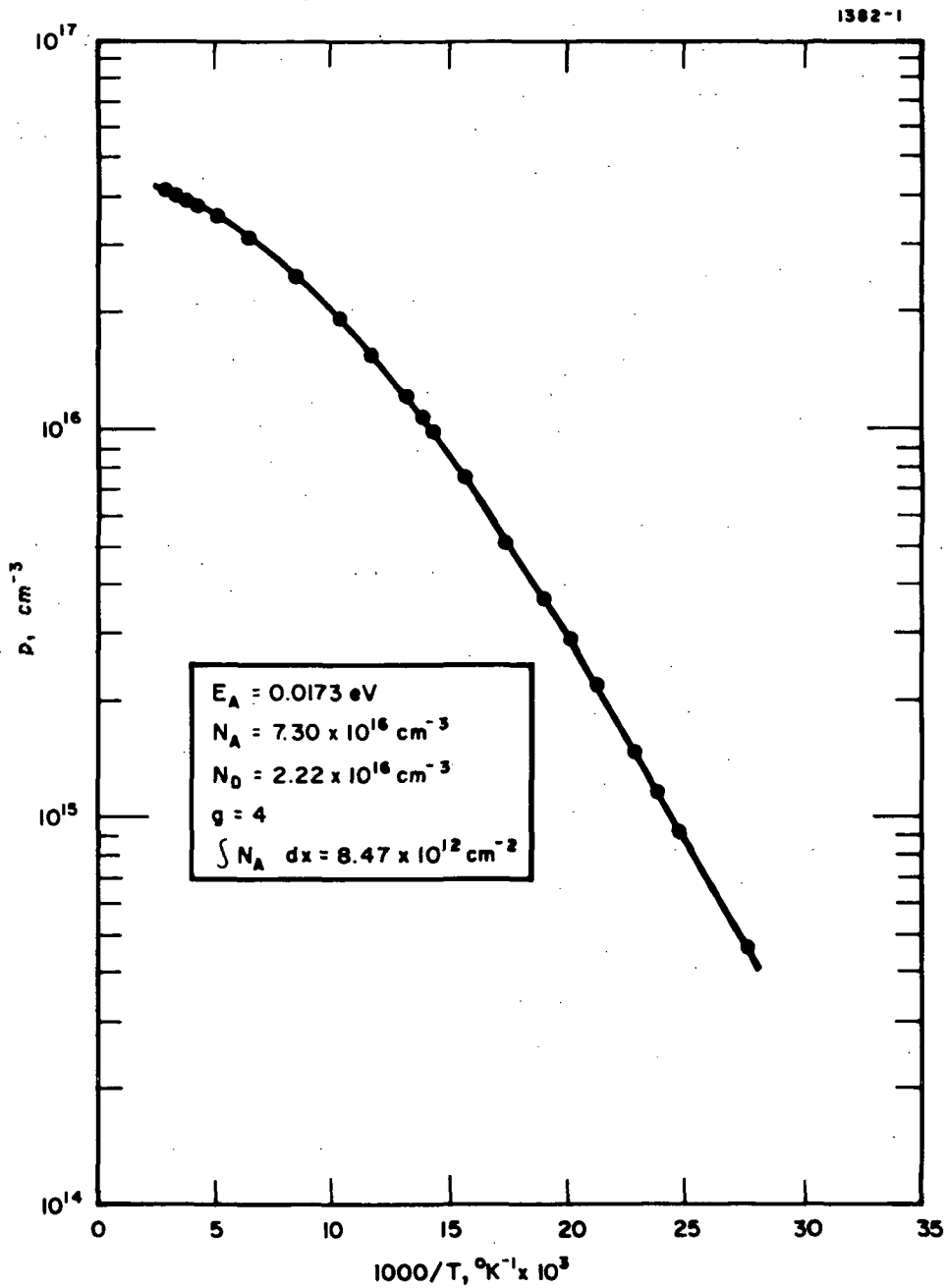


Fig. 9. Hole Concentration Versus Temperature Assuming a Uniformly Doped Layer with Depth = 1.16μ . The Curve is a Least Squares Fit to the Measured Points as Described in the Text.

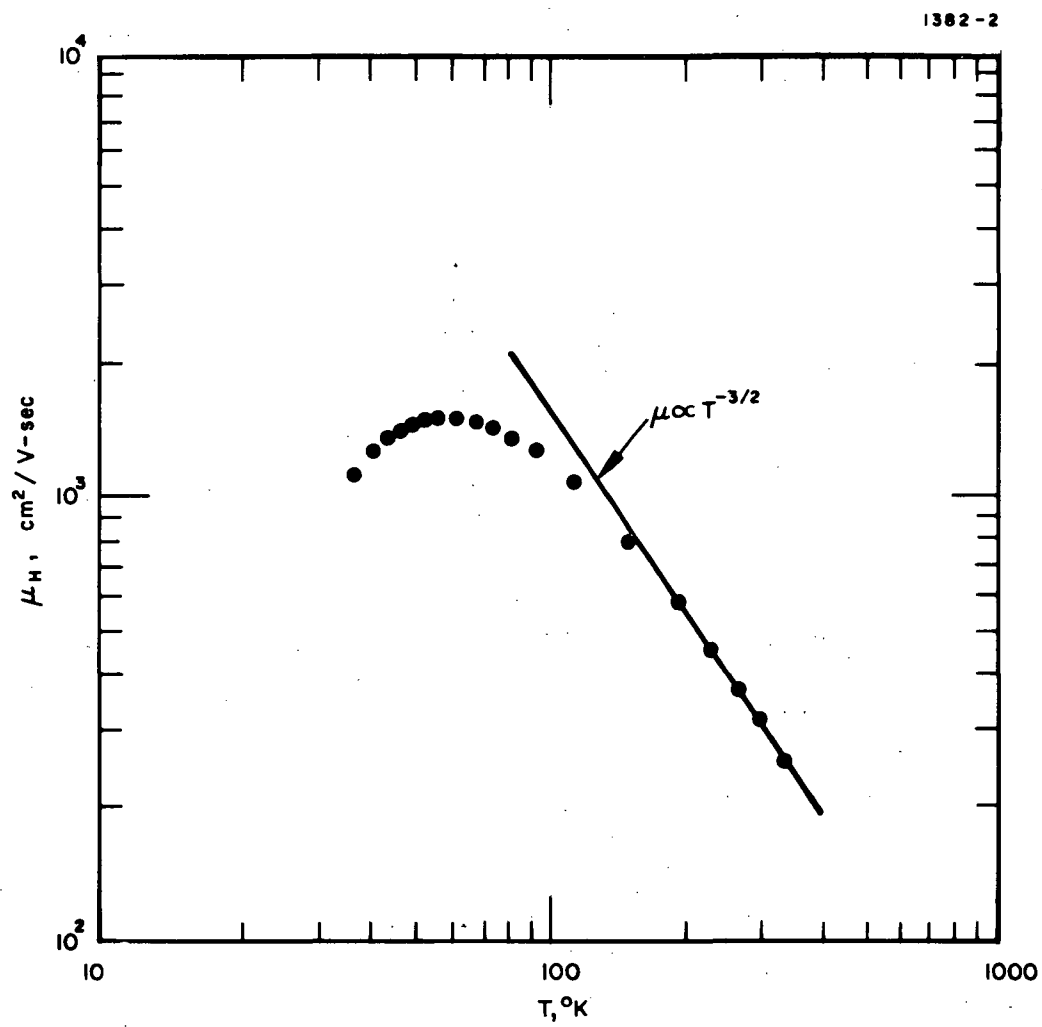


Fig. 10. Hall Mobility Versus Temperature.

In agreement with the data presented in Fig. 6, the mobility seems to be fully annealed at 550°C, whereas the carrier concentration has not. Part of this lack of anneal is caused by compensating donors. These are apparently defect centers which anneal at higher temperatures. The remainder of this lack of anneal could be caused by Be atoms not yet on substitutional sites. However, to definitely establish this, further work would need to be done. This would consist of measurements versus anneal temperature to establish the fully annealed values, thereby eliminating uncertainty in the implanted dose, and measurements on successively stripped samples to establish the profile and eliminate uncertainty in the depth of the layer. Of course, the measurements should be extended to the other samples in this series.

In conclusion, Be is a dopant with a low activation energy that anneals at reasonably low temperatures and has a very light mass, allowing deep layers to be implanted at relatively low energies. At this point, it seems to be a very good candidate for implanting base regions for n-p-n transistors, although further work is needed to establish this firmly.

S E C T I O N I I I

PROFILE STUDIES

One of the most difficult problems in fabricating an ion implanted bipolar transistor is obtaining the required control over dopant concentration profiles with depth. Very little is known about such profiles in GaAs, and the techniques of measurement are not nearly so well developed as in the case of silicon. For those reasons, much of the work under this contract was directed toward developing reliable methods of measuring the concentration profiles of implanted atoms and the resulting carrier concentrations in GaAs. We have applied a number of different methods to this problem, including angle sectioning and etch staining, scanning electron microscope measurements, argon ion beam sputtering for layer removal, and capacitance-voltage measurements for determining concentration profiles. All four techniques have been successful in part, but much work remains to be done in this area before reliable and adequate data are obtained for the dopants of interest. The results of measurements made during this contract period and a discussion of the difficulties encountered are given in the following subsections.

A. ANGLE SECTION AND STAIN METHOD

Angle section and etch staining is a standard technique used for determining junction depths, based on the difference in etch patterns produced by a given etchant in regions of different carriers or concentrations. Finding an etchant that will reliably delineate the junction in GaAs is a difficult

problem. The only etchant that we have found to be at all effective is a mixture of six parts H_2O and one part HNO_3 . This etchant was used to delineate the junction in samples prepared by implanting a dose of $3 \times 10^{14}/\text{cm}^2$ 40 keV Be ions into an n-type substrate with $n = 1 \times 10^{16}/\text{cm}^3$. A beveled angle of 1.5° was lapped onto the edge of each sample with $0.05 \mu\text{m}$ Al_2O_3 polishing compound, and the samples were etched with the HNO_3 solution. The implanted p-type layer was stained dark by this method, and the junction was thus revealed for observation by optical microscopy. The results are shown in Table II. The change in junction depth in the temperature range 475 to 550°C is believed to result either from shift of the $N_D = N_A$ level as more of the implanted ions became electrically active and/or compensating centers are annealed away, or from enhanced diffusion because of high vacancy concentrations in the damaged layer. The calculated change in junction depth that could be expected to occur from normal Fickian diffusion at 600°C is only $\sim 10^{-4} \mu\text{m}$, using a diffusion coefficient of $D = 1 \times 10^{-20} \text{ cm}^2/\text{sec}$ obtained by extrapolating the data of Poltoratski and Stuchechnikov.¹² The junction depth predicted by the LSS theory⁸ is $\sim 0.3 \mu\text{m}$, which supports the first of the two proposed possible explanations of junction motion during annealing.

TABLE II
Junction Depth in 40 keV Be^+ Implanted Samples

Anneal Temperature, $^\circ\text{C}$	Depth, μm
475	0.15
500	0.27
550	0.30
600	0.30

T338

While angle section and staining was applied successfully to Be implanted p-type layers and S implanted n-type layers (as discussed in Section II-A), the method did not work for the case of Mg implanted samples. In all cases we were unable to locate the junction in Mg implanted samples, because the p-type layer did not stain regardless of what etchant was used.

B. SCANNING ELECTRON MICROSCOPE METHOD

Scanning electron microscope (SEM) measurements were also used in an attempt to locate the junction in Mg implanted samples. Electrical contacts were added to the samples after they were beveled, so that bias voltage could be applied. The diodes had reasonably good V-I characteristics with relatively low leakage current when reverse biased. Nevertheless, no junction region could be observed with the SEM operated in either the emissive mode or the conductive mode. Some of the diodes were annealed for 1 hour at 500°C after beveling to remove any lapping damage that possibly had been introduced. Such damage could conceivably produce deep-level compensating centers that would destroy the p-n junction at the beveled surface. However, no junction was observed either by etch staining or by evaluation of the SEM measurements in the annealed samples.

C. ION BEAM SPUTTERING METHOD

The only technique that was successfully used to locate the junction in Mg implanted samples was that of layer removal by Ar ion sputtering. One sample was implanted with a dose of $1 \times 10^{15}/\text{cm}^2$, 45 keV Mg ions with the substrate at

room temperature and was subsequently annealed for 15 min at 900°C. A 2 keV Ar beam was used to sputter off layers of the Mg implanted sample, and Hall measurements were made to determine at what point the p-type layer had been completely removed. This technique showed the p-type layer to be approximately 0.4 μm thick, much greater than the $\approx 0.1 \mu\text{m}$ thickness that would be expected from the LSS theory. It is unlikely that this large junction depth resulted from ion channeling because the critical angle for channeling of Mg ions in GaAs is very small, and the samples were not intentionally aligned. A more probable explanation is diffusion during annealing. This premise is supported by the observation that diodes formed by Mg ion implantation of n-type substrates followed by annealing at 600°C exhibit strong, broad area light sensitivity when reverse biased. Diodes made by similar ion implantation, but annealed at 700°C or higher, have essentially no light sensitivity. Since visible photons penetrate GaAs only to a depth of $\approx 0.1 \mu\text{m}$, an increase in junction depth because of Mg diffusion would be expected to diminish light sensitivity. To establish whether junction depth was a function of anneal temperature, the combination of layer removal (by 2 keV Ar ion sputtering) with Hall measurements of electrical activity was used to roughly "bracket" the junction depth in a set of four samples implanted with an ion dose $\approx 1 \times 10^{15}/\text{cm}^2$ and annealed at 600, 700, 850, and 900°C, respectively. Since the purpose of this experiment was to establish whether junction depth was a function of anneal temperature rather than to determine the exact depth in each case, relatively thick layers were removed in each sputtering step, yielding the coarse data shown in Table III. These data clearly indicate that junction depth is a fairly strong function of anneal temperature. Two explanations are possible: Mg diffusion during annealing, or change of the $N_A = N_D$ level because of a larger percentage of ions electrically active after annealing at higher temperature.

TABLE III

P-Type Layer Thickness in Mg Implanted GaAs

Anneal Temperature, °C	Approximate Thickness of the p-Type Layer t , Å
600	$t < 2500$
700	$t \approx 2500$
850	$2500 \leq t \leq 3500$
900	$3500 \leq t \leq 4500$

T339

D. CAPACITANCE-VOLTAGE METHOD

More detailed information about the carrier concentration profile in ion implanted layers can be obtained by making capacitance versus reverse bias voltage measurements on Schottky barrier diodes formed on the layer. This technique was applied to a set of samples prepared by implanting 40 keV Be ions into $\langle 111 \rangle$ p-type substrates ($p \approx 2 \times 10^{16}/\text{cm}^3$), coating them with SiO_2 , and annealing them for 15 min at 800°C . Following annealing, the oxide was removed in HF and surface barrier dots were formed on the samples by metallic evaporation. At first we attempted to form gold surface barrier diodes on some of the samples. However, satisfactory surface barrier was not formed on any sample. Leakage current was so great that capacitance measurements were impossible, and in fact it was difficult to tell whether there was even a rectifying barrier contact. Subsequently, aluminum surface barrier dots were evaporated on the remaining samples, and these formed relatively low leakage diodes.

The capacitance-voltage technique then was used to determine the carrier concentration profile with depth in three of these samples implanted with different doses of Be^+ . Details of the sample descriptions are given in Fig. 11, along with the concentration data. The profile for the most lightly doped sample closely follows the distribution predicted by the LSS theory, but those measureable for the more heavily doped samples extend over such a small range of depth that it is difficult to ascribe a shape to the curves. (The limits to the depth range of the measurements are caused by reverse bias breakdown at the deep end of the curve and increasing forward bias conductivity at the shallow end.)

In summary, the results obtained during the contract period have shown the depth of penetration of Mg, Be, or S ions to be greater than or equal to the depth predicted by the LSS theory and in some cases to be dependent on the anneal temperature. The total picture of ion penetration in GaAs is very complicated, and much additional work is needed to understand (and ultimately control) the concentration profiles of the desired dopants.

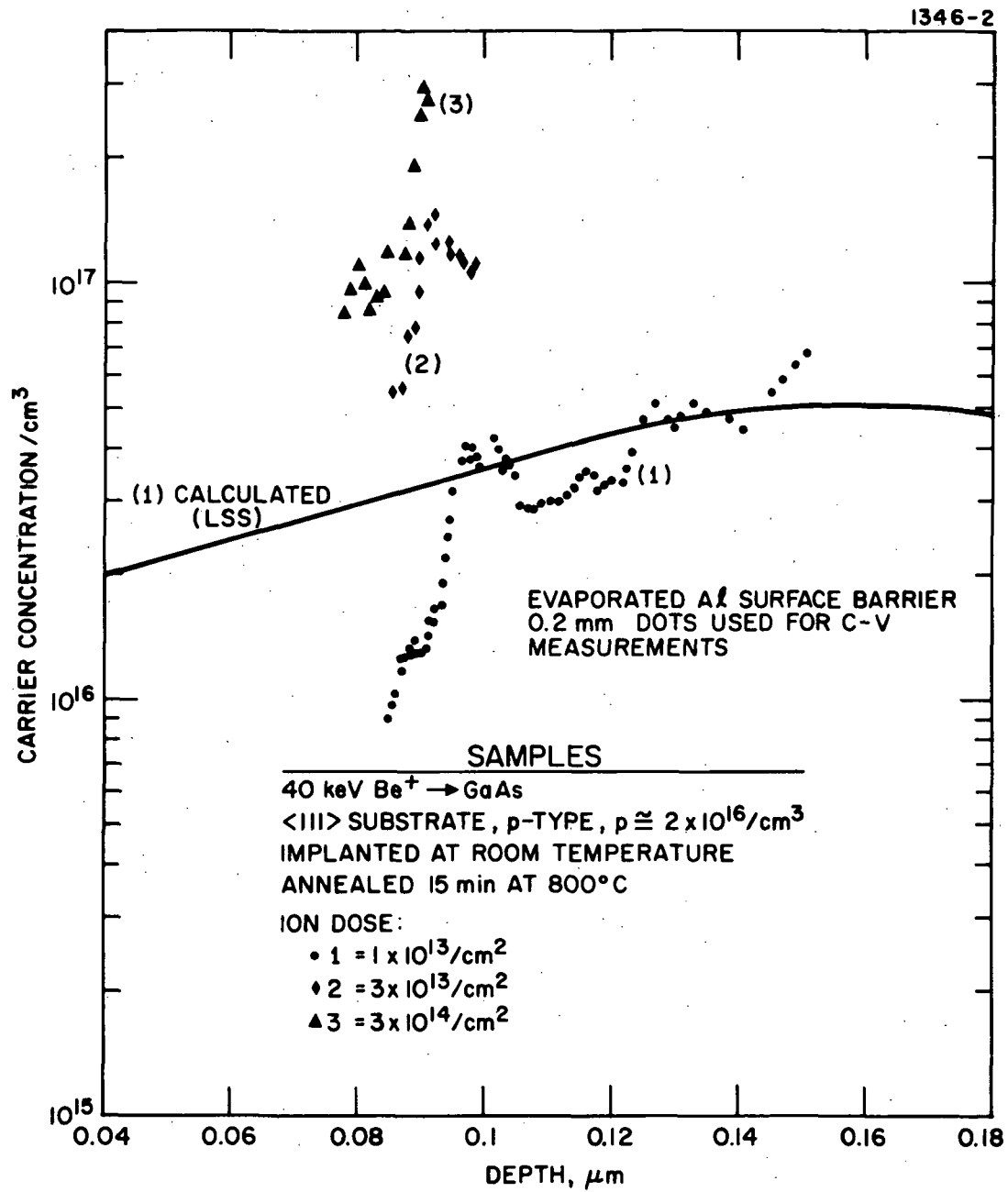


Fig. 11. Carrier Concentration Profiles in Be⁺ Implanted GaAs.

S E C T I O N I V

DEVICES

One of the major objectives leading to transistor fabrication is to determine the electrical properties of junction diodes produced in GaAs by ion implantation. Thus, as part of the work under this contract, we examined the dc voltage-current characteristics of both planar and mesa diodes formed by ion implantation.

A. DIODES

In one case planar diodes were formed by implanting n-type GaAs substrates with 60 keV Cd ions (at room temperature) using a sputtered SiO_2 layer as an implantation mask. Holes were opened in the oxide layer by photoresist masking and selective etching at the points where ion penetration was desired. Subsequent to implantation, the samples were coated with a sputtered SiO_2 layer to prevent dissociation and were annealed for 15 min at 800°C. Mesa diodes of the same size were also formed, by similarly implanting and annealing identical substrates over their entire surface area, and then photoresist masking and etching to produce raised mesa diodes. Ohmic contacts were made to the n-type substrates by forming a microalloyed Sn-Ni layer by vapor deposition and heat treatment for 5 min at 450°C. Contact to the p-type implanted layers was made using indium. The diode area was fairly large (1.5 x 1.5 mm), corresponding to the base region of a relatively large rectangular transistor configuration that has been chosen for initial experimentation. Reverse leakage current in these potential base-collector diodes was

observed to be very small, $\sim 10^{-8}$ A/mm². However, one problem noted was that many of the diodes appeared to be "shorted" after large area In contacts were applied to the implanted p-type layer, while they had relatively good diode characteristics when contact was made using just a gold probe. The effect seemed to be associated with small pin holes in the p-type layer that resulted from lifting of the protective oxide film during annealing or etching. Such oxide lifting was found to be a major problem in transistor fabrication, and thus much work was done during the contract period to improve our oxide coating techniques. The results of this work are detailed in Section V of this report. At this point, it suffices to say that oxide lifting results, to a large extent, from inadequate surface cleaning prior to deposition. The use of more elaborate cleaning procedures than mere solvent washing greatly mitigates the problem, as proven by the following example.

A new set of Cd implanted diodes was prepared for which the fabrication and contacting techniques were the same as those used for the diodes described in the preceding paragraph, except that the new samples were ultrasonically cleaned in hot methyl alcohol before being sputter coated with SiO₂ to provide surface protection during annealing. This procedure greatly reduced the problem of oxide lifting and resultant pin hole production that was responsible for shorting many diodes of the earlier set, which was only rinsed in hot methyl alcohol but not ultrasonically cleaned. However, the ultrasonic cleaning can cause fracture of the brittle GaAs wafer and thus is somewhat hazardous. (Therefore, we continued to investigate possible improvements in cleaning procedures such as sputter removal of a few angstroms of material from the surface immediately before SiO₂ coating, as described in Section V.) The voltage-current characteristics of the new diodes are shown in Figs. 12 and 13; the following observations can be made from the data.

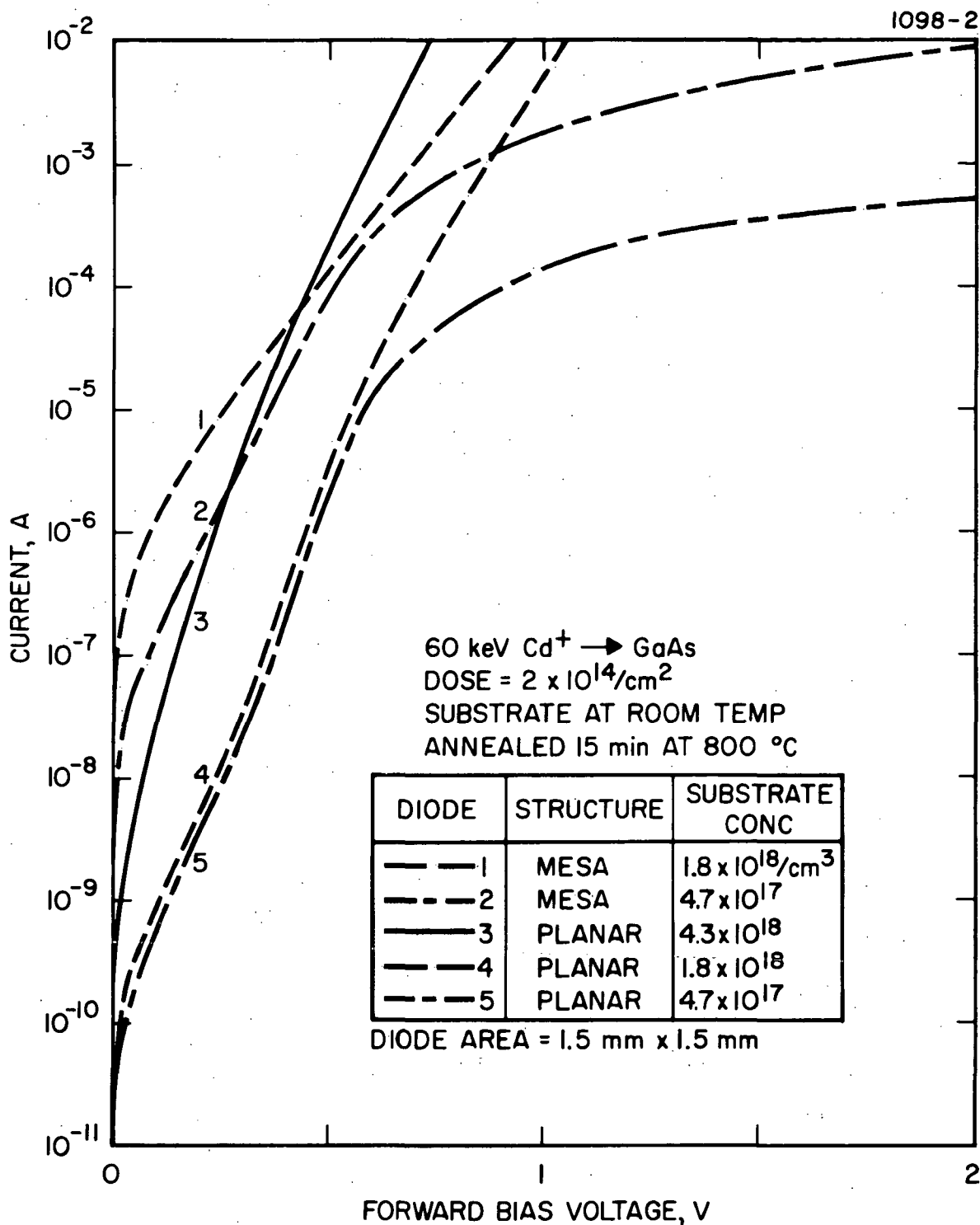


Fig. 12. Forward Bias V-I Characteristics of Cd Implanted Diodes.

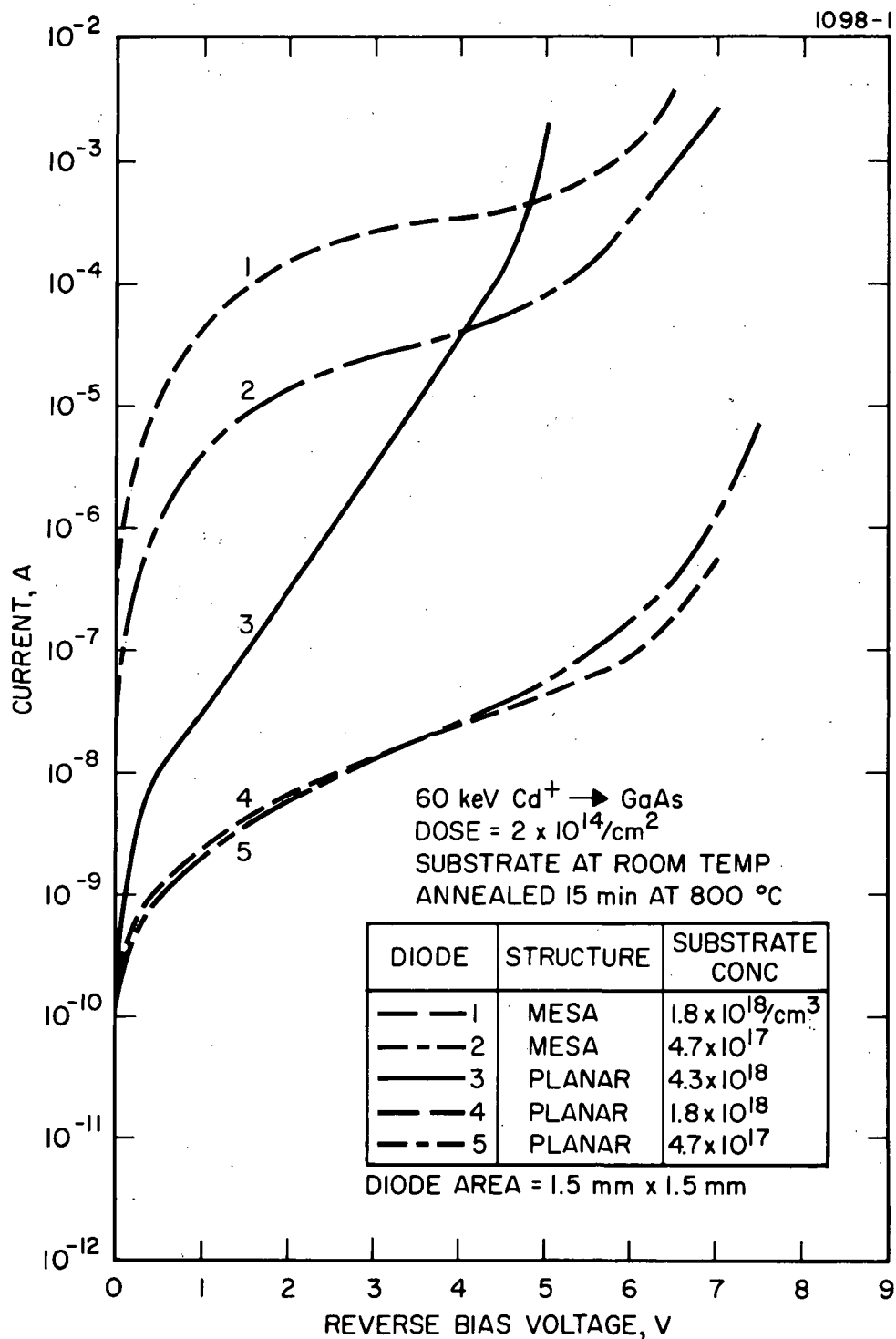


Fig. 13. Reverse Bias V-I Characteristics of Cd Implanted Diodes.

- The forward characteristics of the diodes essentially follow the familiar relation

$$J = J_s \exp \left(\frac{qV}{nKT} \right) ,$$

where n has a value between 1 and 2 corresponding to a combination of both recombination current and diffusion current as one would expect in a GaAs diode. Projection of the exponential portions of the curves to the zero voltage axis gives values of the saturation current density J_s which are greater for mesa diodes than for planar diodes, all other variables being equal. The larger values of J_s for mesa diodes may result from surface leakage current generated at the exposed junction perimeter, although the planar diodes were not coated with a passivating oxide layer and hence also had an exposed junction.

- The effect of series resistance was apparent in the case of diodes 2 and 5, both with substrate concentration = $4.7 \times 10^{17}/\text{cm}^3$. The indicated series resistances are $\approx 130 \, \Omega$ for diode 2 and $\approx 2700 \, \Omega$ for diode 5. Calculations show that the series resistance introduced by the bulk substrate material should be $\approx 6 \times 10^{-3} \, \Omega$ for these diodes and the "spreading" resistance for current flow from the In dot contact through the p-type implanted layer should be $\approx 130 \, \Omega$ at most. Capacitance-voltage measurements indicate that there is no I-layer present. Thus the unusually high series resistance most likely is caused by a high contact resistance in the alloyed (Ni-Sn) contact to the n-type substrate. It is more difficult to contact lightly doped n-type GaAs than it is heavily doped material. We have found that the Sn-Ni alloy technique produces a reliable ohmic (nonrectifying) contact to substrates with impurity concentrations as low as $2 \times 10^{14}/\text{cm}^3$. However, excessive contact resistance may result.

- Reverse leakage current is greater in mesa diodes than it is in planar diodes formed in the same substrate material; this is consistent with the observation that J_S is larger. For all diodes tested, the slope of the reverse current-voltage characteristic is greater than that which would be expected if diffusion current and generation current were the only components flowing. The additional current may be due to tunneling, particularly in the case of diode 3 formed in the most heavily doped substrate and having as a result a very narrow junction depletion layer.
- The reverse bias breakdown voltage was in the range of 5 to 8 V for all diodes. This is approximately what is theoretically predicted for avalanche breakdown in abrupt junctions formed in relatively heavily doped substrates such as these. (In terms of p- and n-type impurity concentrations, these diodes represent emitter-base junctions rather than base-collector junctions. Practical base-collector junctions will require substrate impurity concentration $\sim 10^{16}/\text{cm}^3$.)

Since the planar diodes had somewhat better electrical characteristics than mesa devices, and since planar technology can be more easily applied to the more complex structure of a transistor, we decided to fabricate some preliminary transistor structures using planar technology.

B. TRANSISTORS

Transistor structures were fabricated by implanting n-type substrates with 45 keV Mg ions to form the base regions and subsequently implanting them with 20 keV Si ions to form the emitters. SiO_2 films (≈ 2000 Å thick) sputter deposited at room temperature, were used as implantation masks. Holes were opened in the areas where ion penetration

was desired by using photoresist masking and HF etching techniques. The SiO_2 films used as masks to form first the bases and then the emitters held up well throughout the various processing steps; good adhesion was observed, possibly because we used a light sputtering with Ar ions to clean the surface of the wafers before deposition of the SiO_2 . (There was no break in vacuum between the sputter cleaning and deposition steps.) Two wafers were processed, each containing nine transistor structures with the rectangular geometry shown in Fig. 14. The calculated dopant concentration profiles with depth, based on LSS theory, are shown in Fig. 15. However, from past experience we expected that both the emitter and base junctions would be deeper because of ion channeling and/or diffusion. When the two wafers were put through the critical high temperature annealing process that is required to cause the implanted ions to become electrically active, problems associated with processing technology became evident. However, the initial results were encouraging, in that five n-p-n structures were created. One wafer, with the calculated concentration profile shown in Fig. 15(b), was annealed for 15 min at 800°C . During annealing the protective SiO_2 layer lifted at many localized spots, resulting in dissociation at these points. Because of this, the second wafer, with the concentration profile shown in Fig. 15(a), was annealed at only 700°C for 20 min. The lower annealing temperature did reduce oxide lifting, but after masking and etching to open up the base and emitter contact holes, the SiO_2 layers on both wafers were in such poor condition that it was impossible to evaporate metallic contacts without shorting out the devices. (See Fig. 16). Nevertheless, it was possible to measure some of the device characteristics using pressure probes, which formed rectifying surface barrier contacts. All of the devices on the wafer annealed at 800°C appeared

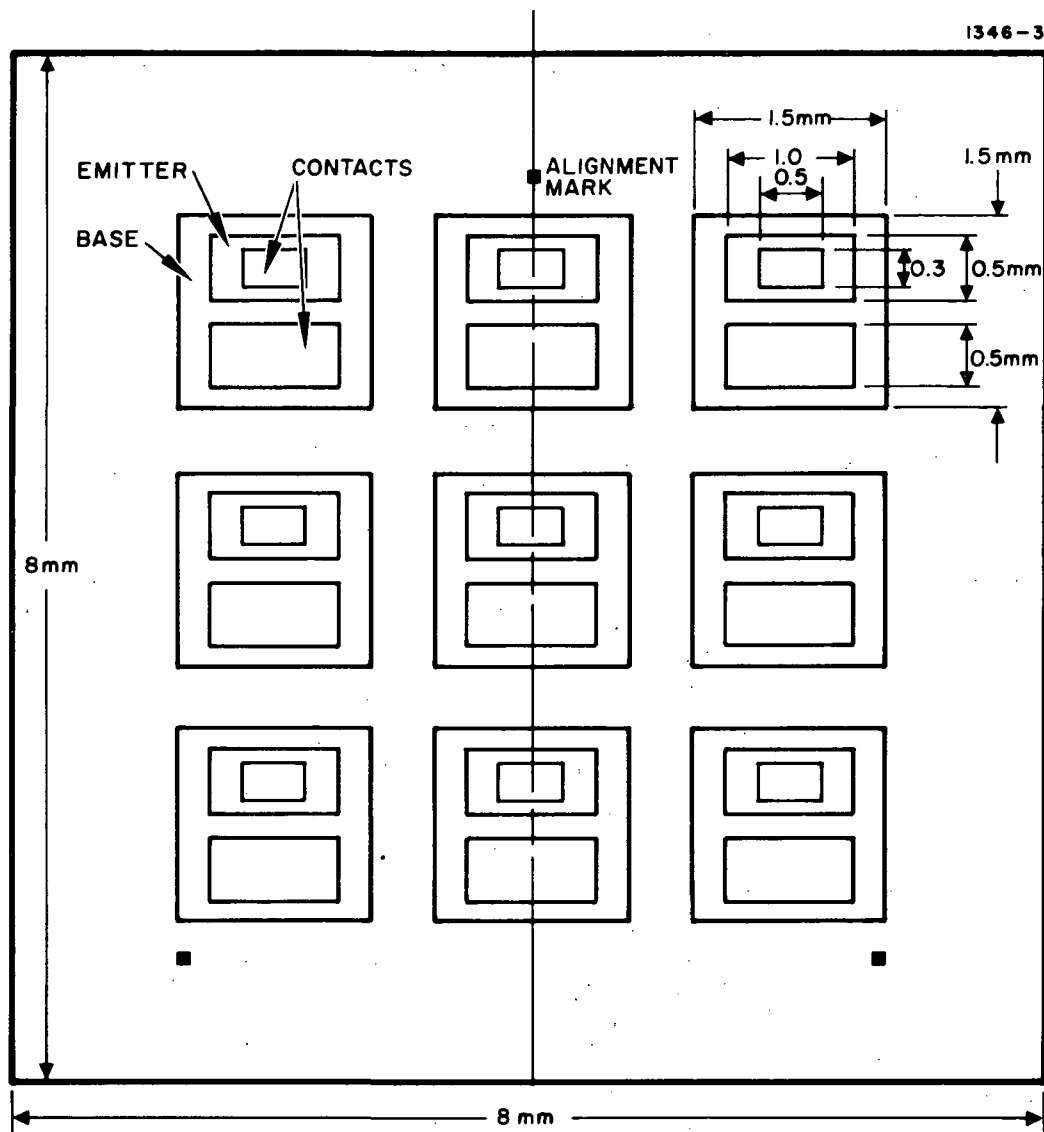


Fig. 14. Geometry of Ion Implanted Planar Transistor Structures.

CALCULATED IMPLANTED ION CONCENTRATION, cm^{-3}

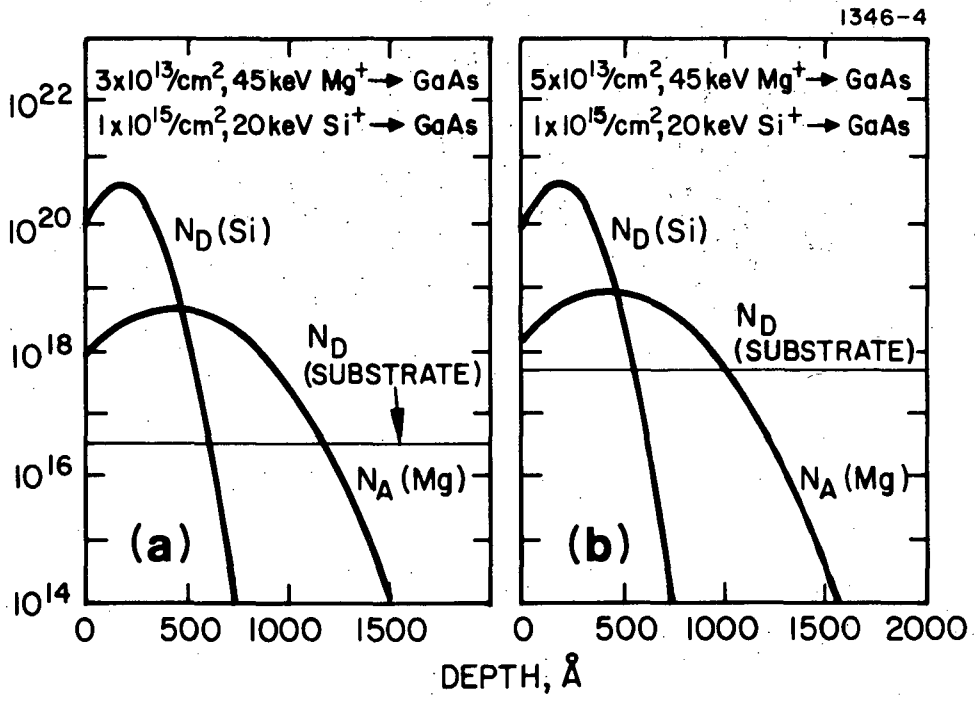
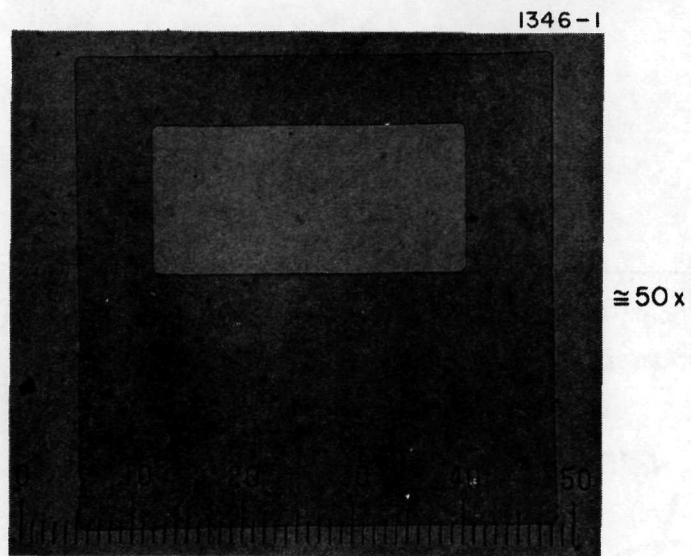
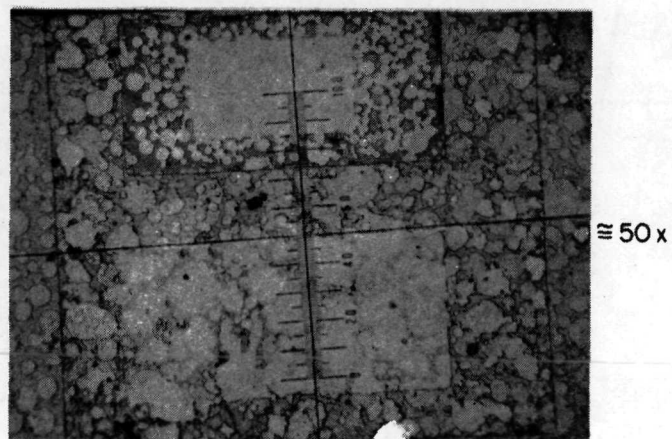


Fig. 15. Calculated Ion Concentration Profiles in Ion Implanted Transistors.



(a) BEFORE ANNEALING



(b) AFTER ANNEALING, PHOTO RESIST MASKING,
AND ETCHING TO OPEN EMITTER AND BASE
CONTACT HOLES.

Fig. 16. Bubbling of SiO_2 Coating
Resulting from Processing.

to have an emitter-to-collector short; no p-n junction behavior was observed. However, on the wafer annealed at 700°C, five of the nine devices had good emitter-base and base-collector junctions. The others appeared shorted. Measurement of the forward bias characteristics of the junctions was prevented by the surface barrier contacts. However, the reverse bias characteristics of the junctions could be measured, since the surface barriers were forward biased for conditions of reverse bias on the p-n junctions. The reverse breakdown voltage for the base-collector junctions was ≈ 25 V for all of the nonshorted devices, while emitter-base reverse breakdown voltage was ≈ 15 V. For both emitter-base and base-collector junctions, considerable generation current was observed when the devices were illuminated by a microscope light while under reverse bias. While the devices had what appeared to be good junctions, we were unable to observe any transistor action when the device characteristics were displayed in the common emitter mode on a curve tracer, with the base current stepped as high as 1 mA. In other words, they had immeasurably small β .

To permit further study of the electrical characteristics of these transistor structures, ohmic contacts were formed on the emitter and base regions of one of the transistor structures by the following process. First, a new 2000 Å thick layer of sputtered SiO_2 was deposited over the entire wafer to fill in the holes that developed in the old oxide cover during annealing. Next, a layer of photoresist was put on the wafer. It was exposed, developed, and etched to open contact holes at the emitter and base regions. Then a layer of silver was evaporated over the photoresist, filling in the contact holes as well. During this step, a metal mask was used to limit the silver deposition to the area surrounding only one device, thus leaving four remaining n-p-n structures

for possible future experimentation with different contacting methods. Finally, the photoresist was dissolved away with acetone, carrying the silver layer with it except in the contact regions where the silver adhered well to the GaAs. The evaporated silver resulted in nonrectifying contacts to the base and emitter regions, permitting measurement of the junction characteristics. Both the emitter-base and base-collector junctions were found to behave normally, except that reverse leakage current was considerably increased by the addition of the silver contacts. This increase in leakage current over that observed when contact was made merely with tungsten probes was possibly caused by minute shorts at the points in the base and emitter contact regions where oxide lifting during annealing had allowed localized dissociation of the GaAs. When the device characteristics were displayed in the common emitter mode on a curve tracer, with the base current stepped as high as 100 mA, no transistor action was observed. As before contacting, β was $\approx$ zero. The device was viewed with an infrared image converter while the biases were being swept by the curve tracer. Light emission was observed when base current was stepped above 10 mA and the intensity appeared to increase relatively uniformly with increasing base current. The intensity of light emission was, however, independent of collector voltage (and current). All of the carriers injected at the emitter-base junction appeared to be recombining in the base region before reaching the collector. The most likely explanation is that the base width far exceeded the calculated $0.05 \mu\text{m}$ that would have resulted if the concentrations of electrically active dopant atoms corresponded to those shown in Fig. 15.

The problem of producing the desired dopant concentration profiles in GaAs is extremely complicated, because there are few experimental data available for the dopants of

interest, and there is no quantitative theoretical model for ion penetration in a crystalline semiconductor that is adequate to predict the profile that will result from a given set of implantation conditions. In addition, junction depth measurements (described in Section III) have indicated that the carrier concentration profile that results from a given implant, in some cases, depends on the anneal temperature used. Considering these problems, we were not surprised to find $\beta \approx 0$ for devices fabricated based on profiles calculated using the LSS theory, which strictly applies only to amorphous materials and which neglects the effects of diffusion and unionized dopant atoms. Nevertheless, the devices that were made did establish the following important facts.

- It is possible to fabricate an n-p-n structure in GaAs by double implantation of both n- and p-type dopant atoms, followed by annealing.
- During annealing, sufficient radiation damage can be removed to produce back-to-back diodes with relatively low reverse leakage current.
- The observation of strong luminescence when the emitter-base junction was forward biased indicated that minority carrier lifetime in the base region was at least as long as the lifetime for radiative recombination. Since this radiative lifetime puts a fundamental upper limit on diffusion length in GaAs, one can conclude that minority carrier lifetime (or diffusion length) in a properly annealed ion implanted transistor is not limited by residual radiation damage.

In addition to establishing the above encouraging facts, fabrication of the transistor structures also served to point out a number of technological problems related to forming the required oxide coating and electrical contacts. These problems are discussed in the following section.

S E C T I O N V

TECHNOLOGY

A. CONTACTS

One of the problems encountered in making any GaAs device is that of forming adequate ohmic contacts. Contact can be made to p-type material (with carrier concentration $>10^{16}/\text{cm}^3$) fairly easily by using indium in the form of either an evaporated or soldered contact. In the case of n-type GaAs, particularly for a thin ion implanted layer, other techniques must be used. One method that can be used is to evaporate a layer of tin, followed by a layer of nickel to prevent the tin from "balling up," and then annealing at 450°C for about 5 min. This technique results in ohmic contacts even on material of low carrier concentration ($<10^{16}/\text{cm}^3$), but we found that contact resistance was fairly high ($>1000\ \Omega$) in some cases. In addition, this method is not 100% effective on ion implanted n-type layers, because the alloyed contact penetrates $\sim 0.1\ \mu\text{m}$ and can thus short through a thin layer.

A method that was used successfully to contact implanted n-type layers is to form contact pads of evaporated silver at room temperature. Even without annealing, the resulting contacts had lower resistance than the Sn-Ni alloy contacts, and there was no problem of excessive penetration through the implanted layer. We have used evaporated silver (in work on related contracts) to produce ohmic contacts on n-type GaAs with a carrier concentration of $n \approx 10^{14}/\text{cm}^3$. According to Mike Malbon,¹³ who suggested the Ag contacts, the contact resistance can be reduced by annealing at 400 or 500°C . Difficulties with the silver contacts are that they are soft

and easily abraded, and that they tarnish in air within a few days unless they are gold coated.

B. SURFACE COATING TECHNIQUES

Because of the reported difficulties associated with oxide lifting during annealing, we initiated a concentrated effort to analyze and solve the problem by developing improved oxide coating techniques for GaAs.

To protect GaAs crystals during high temperature processing (up to 900°C) we have employed thin layers of silicon dioxide deposited by means of Ar ion beam sputter-evaporation, using fused silica as a source material. The main objectives have been to establish a workable process and to optimize film thickness, so that thermal erosion during annealing is eliminated or reduced to a degree acceptable for transistor fabrication.

Silicon dioxide deposition is very sensitive to surface cleanliness. Particles left on the surface prior to oxide deposition lead to formation of pin holes or bubbles in the oxide during annealing which allow thermal erosion at those points. Figure 17 is a dark field photograph of an oxide after 800°C annealing. The surface is badly eroded and typical of the results obtained if the substrate is not sufficiently cleaned or if the oxide is not thick enough.

The best results have been achieved with the following cleaning procedure: 10 min in hot trichloroethylene, 10 min in hot acetone, and 10 min in hot isopropyl alcohol, followed by a 5 min rinse in running deionized water. (Swabbing is used when necessary.) Just prior to oxide deposition in the evaporator, the GaAs surface is ion bombarded in pure argon at 5 keV energy and $10 \mu\text{A}/\text{cm}^2$ beam density for 5 minutes which removes ~ 50 to $100 \text{ \AA}$ of material.

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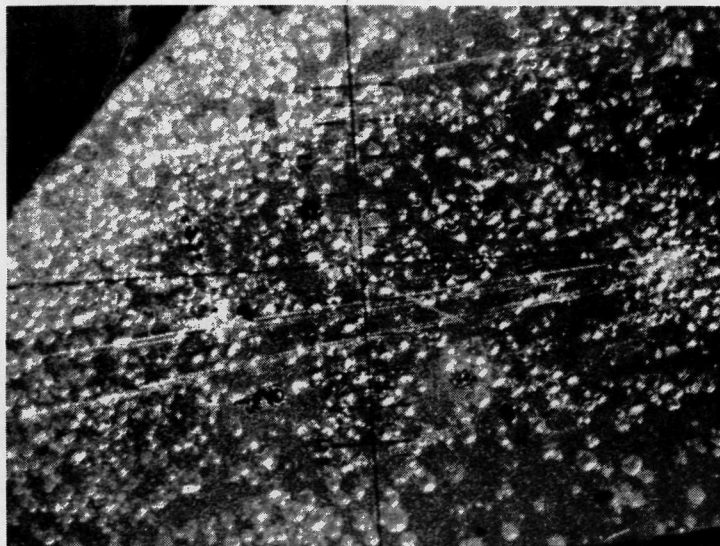


Fig. 17. Dark Field Photograph of an Eroded Surface after 800°C Anneal (55x).

Figure 18 is a high power (11,000 x) scanning electron micrograph of a typical evaporated oxide layer prior to annealing. Note that no defects are observable. (The two white spots are dirt specks, intentionally included to demonstrate that the microscope was properly focused.) Figure 19 shows the results obtained after an 800°C anneal of a sample cleaned with the described procedure. Oxide lifting is greatly reduced by the improved cleaning procedure, but some defects remain. (See Fig. 17 for comparison with Fig. 19.)

In summary, ion beam evaporated layers of silicon dioxide in the thickness range from 2000 to 4000 Å have sufficiently protected GaAs surfaces during high temperature processing to allow electrical measurements to characterize implanted dopant layers. However, even with the best cleaning procedure we have found, the oxide integrity is not such that it could be used reliably for small device fabrication at this time. Future work should be done to eliminate pin holes and to investigate the observed defects which form on (or in) the oxide. Also, other methods of deposition are possible, including the use of other materials, such as aluminum oxide or silicon nitride. The use of these materials as protective films should be further investigated.

M 8368



Fig. 18. Scanning Electron Micrograph of a 3000 Å Silicon Dioxide Layer Before Annealing (11,000 x).

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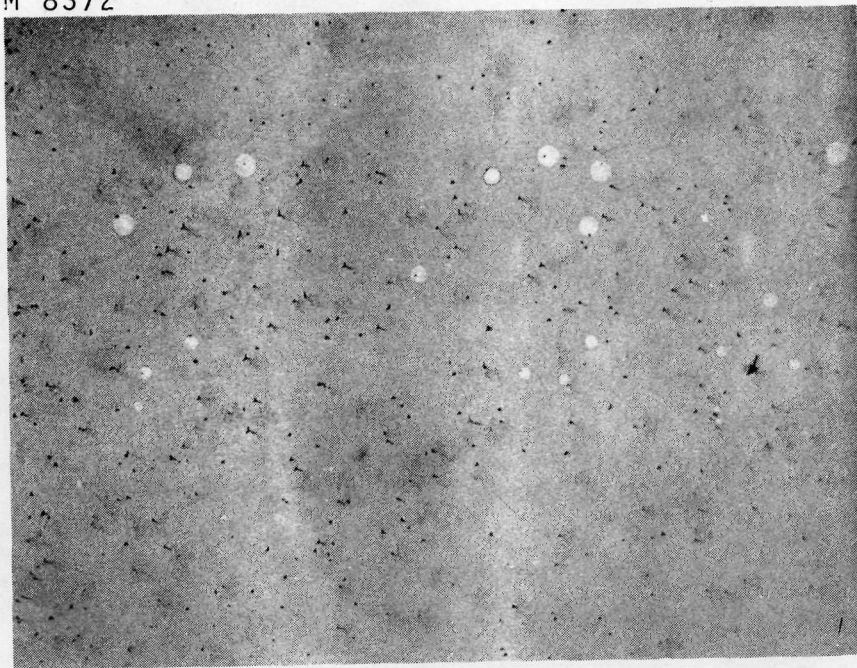


Fig. 19. Light Field Photograph of Surface Defects after 800°C Anneal of Sample Cleaned Following the Improved Procedure. (50 x).

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A P P E N D I X A
Mg AND Be IMPLANTATION TECHNIQUES

Mg AND Be IMPLANTATION TECHNIQUES

The Mg or Be implantation doping of the GaAs samples was performed in a 150 kV implantation system using hot-cathode electron-bombardment ion source to produce the Mg and Be ions.

The Mg ions were generated by placing metallic Mg in an axial probe inserted into the source from the back flange to a location on the axis where the beam current could be controlled at the desired level; a current at the target of a few μA was sufficient for the work reported. The ion source and system were shown to be capable of delivering about 50 μA of Mg to the target. Two techniques were tried to produce a Be ion beam. Using Be metal in the probe, as was done for Mg, produced only about 10^{-8} A of Be^+ because of the temperature limitation within the source and the lower vapor pressure characteristics of Be. The use of BeCl_2 in the probe produced about 0.2 μA of Be^+ , which was sufficient for the reported work.

For both Mg and Be, a plasma was generated in the ion source, and the ions were extracted from the plasma at about 2 kV and introduced through a focusing lens into a 150 kV constant gradient accelerator that was partially shorted for the lower energies used here. An electron suppression geometry was used that produces ion current independent of bias voltage above 45 V of suppression voltage; 90 V was applied for the implantations.

Mass spectra obtained for the ion beams used showed good separation among the Mg isotopes (see Fig. A-1). Be has a single stable isotope of mass 9, that is easily mass separated. A mass separation definition slit placed just before the beam raster scanner allowed $^{24}\text{Mg}^+$ and $^9\text{Be}^+$ to be separated from

other components of the beams, even when the beam was swept over a 2 x 2 in. area. Mass separation was performed by passing the total ion beam through a circular electromagnet with 6 in. diameter pole faces. The resolving power of the total system was about 150.

Uniform ion current density and hence dose were produced over the GaAs sample area by electrostatic deflection of the ion beam with orthogonal triangular wave form potentials of different frequencies applied between two pairs of plates. The ion dose was controlled by integrating the suppressed current to a target area larger than the sample and smaller than the area covered by the rastered ion beam. The integrator was preset to the total charge corresponding to the desired ion dose over the controlled area, and the rastered ion beam was maintained centered on the target area during implantation.

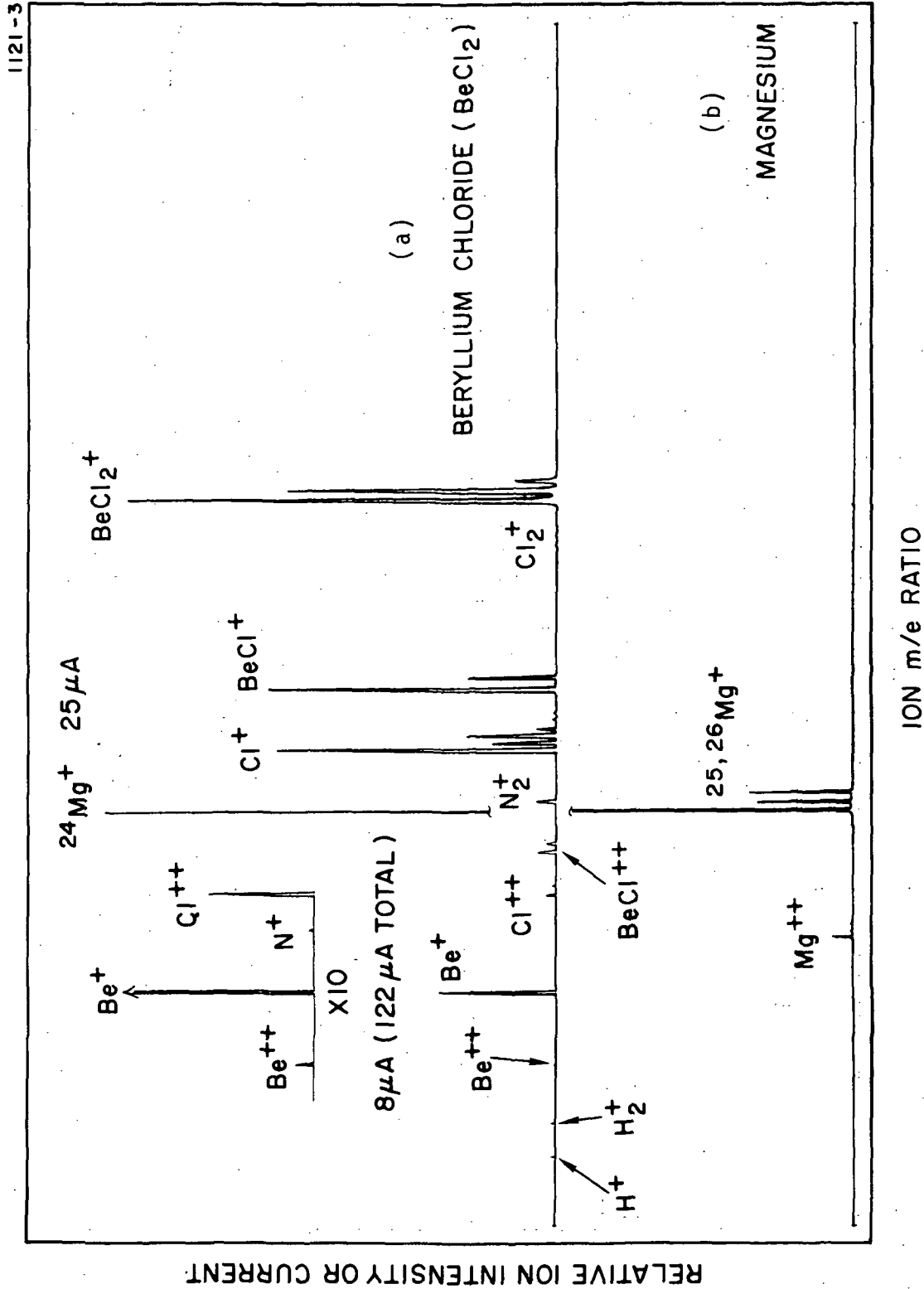


Fig. A-1. Mass Spectra of Ion Beams. (a) Used for Be Implantation. (b) Used for Mg Implantation.

A P P E N D I X B

Mg AND Be ION IMPLANTED GaAs

Mg and Be Ion Implanted GaAs*

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P-type layers have been produced in GaAs by implantation of either Mg or Be ions, with the substrate at room temperature, followed by annealing at higher temperatures. The ion source in both cases was a hot-cathode, electron-bombardment type. The Mg ions were generated by placing metallic Mg in an axial probe inserted into the source, while the Be ions were produced by placing BeCl_2 in the probe. N-type $\langle 111 \rangle$ substrates were implanted with 45 keV Mg or 40 keV Be ions, and were subsequently annealed for 15 minutes at temperatures up to 900°C . The dependence of surface carrier concentration, and mobility on ion dose and on post-implantation anneal temperatures was determined using the van der Pauw-Hall technique.

*This work was supported in part by NASA, Langley Research Center, Hampton, Virginia.

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Beryllium and magnesium are known to be p-type dopants in GaAs.^{1,2} However, to our knowledge, they have not been used previously as dopants by means of the ion implantation method. Because Mg and Be are light ions compared to the commonly used p-type dopants for GaAs such as Zn and Cd, they penetrate more deeply into the lattice for a given ion energy and hence are particularly useful in applications where a relatively thick doped layer is required. This paper describes the methods of generating the desired Be and Mg ions and the electrical properties of the p-type layers produced by implanting them in GaAs substrates.

A hot-cathode, electron-bombardment ion source was used to produce the Mg and Be ions. The Mg ions were generated by placing metallic Mg in an axial probe inserted into the source from the back flange to a location on the axis where the ion beam current could be controlled at the desired level; a current at the GaAs target of a few μA was sufficient for the work reported here, although the ion source and system were shown to be capable of delivering about 50 μA of Mg to the target. Two techniques were tried to produce a Be ion beam. Using Be metal in the probe as was done for Mg produced only about 10^{-8} A of Be^+ because of the temperature limitation within the source and the lower vapor pressure characteristics of Be. The use of BeCl_2 in the probe produced about 8 μA of Be^+ which was sufficient for the reported work.

*This work was supported by NASA Langley Research Center, Hampton, VA.

Mass separation of either $^{24}\text{Mg}^+$ or $^9\text{Be}^+$ from other components of the beams was performed by passing the total ion beam in each case through a 6" dia. electromagnet and a definition slit placed just before the electrostatic raster scanner which was used to scan the beam over a 2 x 2 inch area. Mass spectra obtained for the ion beams showed good separation among the Mg isotopes (see Fig. 1), and the single stable Be isotope of mass 9 was also easily mass separated.

The GaAs substrates used in these experiments were $\langle 111 \rangle$ oriented wafers ($\pm 3^\circ$), with the B face chemically polished prior to implantation. The wafers were intentionally misaligned 8° with the ion beam during implantation to minimize ion channeling. Implantation was performed with the substrates at room temperature and the samples were subsequently coated with a 2000 Å thick sputtered layer of SiO_2 prior to annealing at higher temperatures in a flowing N_2 atmosphere. This oxide coating has been found effective in preventing dissociation of the GaAs, as well as reducing outdiffusion of the implanted ions during annealing.

The carrier concentration per cm^2 , N_S , and the effective mobility, μ , in the p-type layers produced by ion-implantation and annealing were measured using the van der Pauw-Hall technique.³ The substrates used were n-type, with $n = 1 \times 10^{16}/\text{cm}^3$, so that the p-n junction between the implanted layer and the substrate would provide electrical isolation during measurement.

One group of samples was prepared by implanting 45 KeV Mg^+ ions, in doses ranging from $5 \times 10^{13}/\text{cm}^2$ to $1 \times 10^{15}/\text{cm}^2$. They were then annealed at temperatures in the range 100 - 900°C. No p-type layer was observed in samples annealed at $\leq 500^\circ\text{C}$, but they did form in samples annealed at $\geq 600^\circ\text{C}$. The results of Hall measurements made

on those samples are shown in Fig. 2. Note that for samples with ion dose $\leq 1 \times 10^{14}/\text{cm}^2$, 100% electrical activity was observed after annealing at 800°C . The surface carrier concentration (after 800°C anneal) saturated in the range of $1 - 2 \times 10^{14}/\text{cm}^2$ for samples with ion dose $> 10^{14}/\text{cm}^2$, while annealing at 850°C and 900°C produced a decrease in carrier concentration in these samples from that obtained after 800°C anneal. This decrease may be due to outdiffusion of the Mg, or possibly may result from self-compensation. The maximum carrier concentration/ cm^2 that was observed corresponds roughly to a peak concentration in the implanted layer of $2 \times 10^{19}/\text{cm}^3$, which has been reported also by Kressel and Hawrylo⁴ to be the maximum concentration they observed in epitaxially grown (950°C) layers. The peak concentration/ cm^3 in the implanted layer is not known exactly because the concentration versus depth profile was not determined. The thickness of the p-type layer in samples annealed at $800 - 900^\circ\text{C}$ was approximately 0.4 micron, as determined by thin layer "stripping" (using 2 kV Ar ion sputtering) coupled with Hall measurements. The layer thickness predicted by the Lindhard-Scharff-Schiøtt⁵ (L.S.S.) range-energy theory is ~ 0.12 micron. Thus it is apparent that some ion channeling or diffusion did occur, and it cannot be assumed that the implanted and annealed layer has the Gaussian shape predicted by the L.S.S. theory.

The fact that carrier mobility was $\sim 100 \text{ cm}^2/\text{Vsec}$ even in samples annealed at only 600°C suggests that lattice disorder produced by Mg implantation anneals at a lower temperature than that produced by the same dose of Cd or Zn ions. Cd or Zn implanted layers must be annealed at $\geq 800^\circ\text{C}$ before mobility recovers to values $\sim 100 \text{ cm}^2/\text{Vsec}$ that are comparable to mobilities observed in bulk GaAs single crystals of equivalent doping concentrations.

The electrical properties of p-type layers produced by room temperature implantation of 40 keV beryllium ions are shown in Fig. 3. As in the case of Mg, no p-type layer was observed until the samples were annealed. The anneal temperature required to produce a p-n junction depended on the ion dose, and varied from 475°C for a sample implanted with 3×10^{14} ions/cm² to 750°C for one with ion dose = 1×10^{13} /cm². In the case of samples implanted with $\geq 1 \times 10^{14}$ ions/cm² maximum electrical activity (>80% of the implanted ions electrically active) was observed after annealing at only 600°C. This temperature is considerably lower than 800°C, which has been found to be the temperature required to produce maximum electrical activity in Mg implanted layers and also in Cd, Zn, Si or S implanted layers.^{6, 7, 8} The anneal behavior of carrier mobility indicates that recovery of the lattice from implantation-caused damage occurs at a relatively low temperature, since μ rises to a reasonable value for bulk p-type material (in the range 100 - 200 cm²/Vsec) after annealing at as low as 550°C, and then the curves of μ vs. temperature are relatively flat for higher temperatures. It is interesting to note that samples implanted with ion dose $\geq 1 \times 10^{14}$ /cm² reach 80% electrical activity after annealing at 600°C while samples implanted with smaller doses require annealing at higher temperatures before the same percentage of the implanted ions are electrically active. Thus it appears that a certain amount of lattice disorder is conducive to movement of the ions to lattice sites in which they are electrically active, presumably substitutional positions.

Angle-section and staining techniques applied to samples implanted with 3×10^{14} Be⁺/cm² showed that the p-n junction depth varied from 0.15 micron in samples annealed at 475°C to 0.3 micron in samples annealed at 550 or 600°C, and remained at about 0.3 micron in samples annealed above 600°C. The change in junction depth in the temperature range 475 -

550°C is believed to result either from shift of the $N_D = N_A$ level as more of the implanted ions became electrically active, or from enhanced diffusion because of high vacancy concentrations in the damaged layer. The calculated change in junction depth that could be expected to occur from normal Fickian diffusion at 600°C is only $\sim 10^{-4}$ micron, using a diffusion coefficient of $D = 1 \times 10^{-20} \text{ cm}^2/\text{sec}$ obtained by extrapolating the data of Poltoratskii and Stuchenbnikov.⁹ The junction depth predicted by the LSS theory⁵ is ~ 0.3 micron, which supports the first of the two proposed possible explanations of junction motion during annealing.

The results presented in this paper have shown that Be and Mg can be used as ion-implanted dopants in GaAs, producing p-type layers with reasonably large hole concentrations and mobilities in the range 100 - 200 cm^2/Vsec .

Acknowledgement

The authors would like to thank O. J. Marsh for suggesting that Mg and Be might be useful as ion implanted dopants in GaAs and for helpful discussions of the work. They are also indebted to D. Loper for angle-section and staining and to H. Garvin for ion beam sputtering used in layer thickness determination.

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Figure Captions

1. Mass Spectra of Ion Beams
 - a. used for Be implantation
 - b. used for Mg implantation
2. Electrical properties of Mg implanted layers in GaAs
3. Electrical properties of Be implanted layers in GaAs

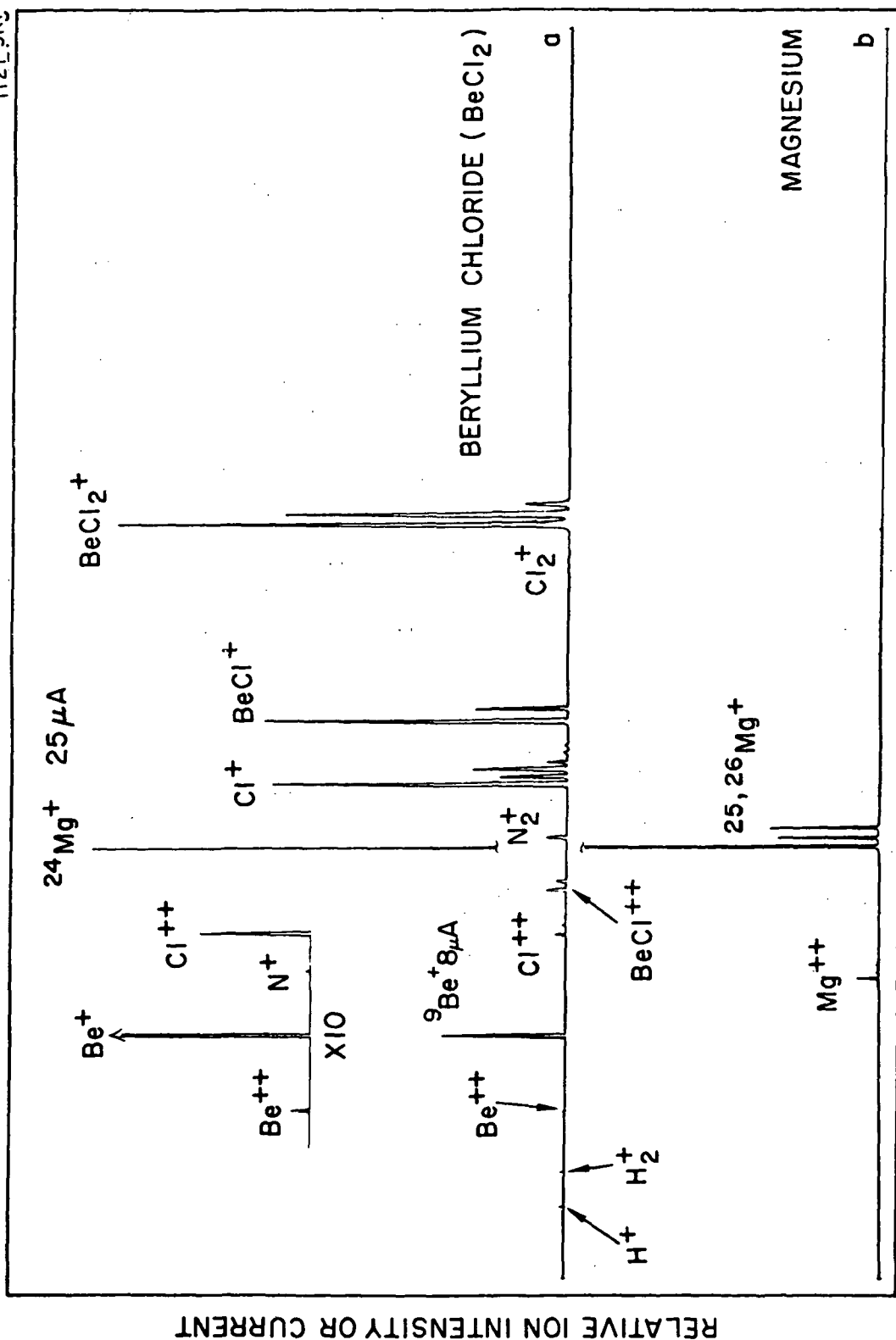
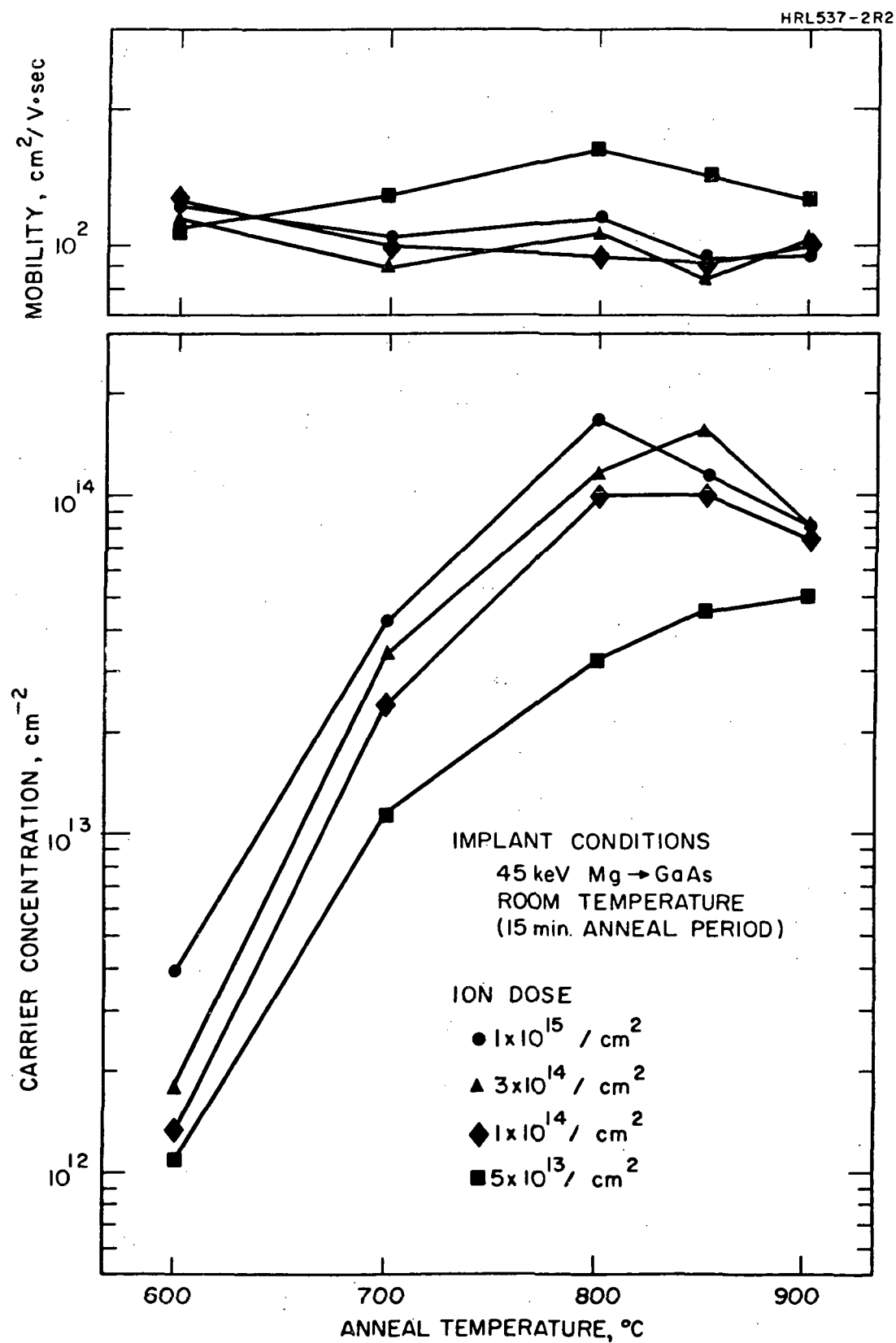


Fig. 1
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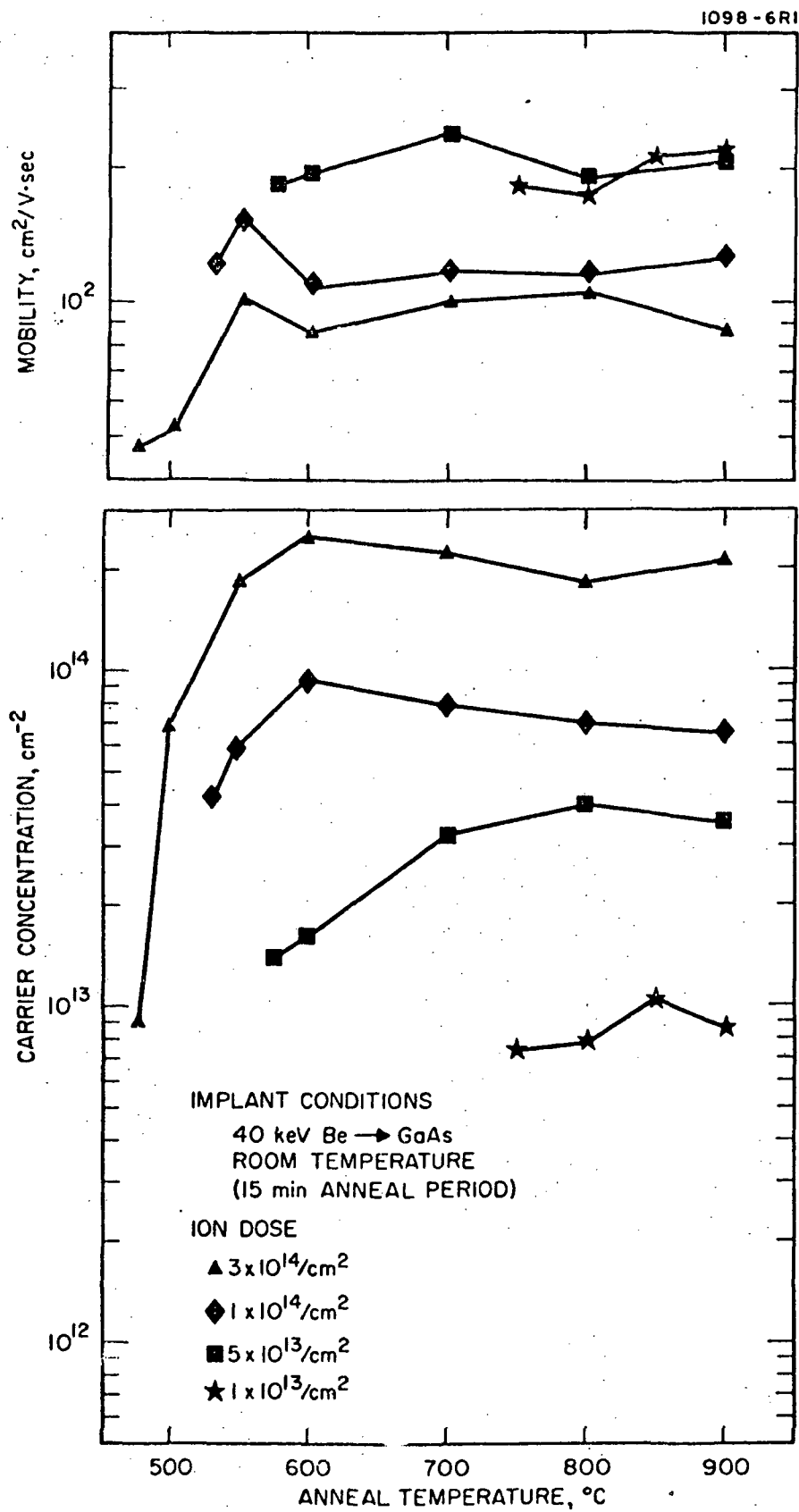


Fig. 3
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 Wilson
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A P P E N D I X C
HALL MEASUREMENT SYSTEM

HALL MEASUREMENT SYSTEM

A computer controlled data acquisition system is available to automatically make Hall effect measurements versus temperature. The system is currently capable of controlling the sample temperature from 4.2 to 323°K. It can accommodate any configuration of the sample from 8-lead bar to Van der Pauw and control the current applied from 2×10^{-9} A to 10^{-2} A. The system is set up to provide both a list and a plot of the calculated results (density of free carriers, surface concentration, mobility, etc.) in real-time and to communicate the data to a large time-share computer for nonlinear curve fitting to determine the energy of the impurity level, the density of donors, and the density of acceptors.

A. DESCRIPTION OF SYSTEM

A block diagram of the system is shown in Fig. C-1. The system is built around a Lockheed MAC-16 computer with 8 k words of memory. Bulk storage is provided by a cartridge magnetic tape unit with 4 tape drives (200 k words capacity) and a fast (8.3 msec average access time) disk of 200 k words capacity. Communication with the experimenter is provided by a teletype, a high speed printer, and a plotter. The digital to analog converters (D/A) which drive the plotter are also capable of driving an oscilloscope display. A real-time clock provides both time of day and interval timing functions. The time of day portion runs on an independent power supply with battery backup. This allows the computer, which has power failure detection and auto-restart capability, to determine the length of a power failure and thus whether to abort or continue a run. This capability is essential for unattended operation.

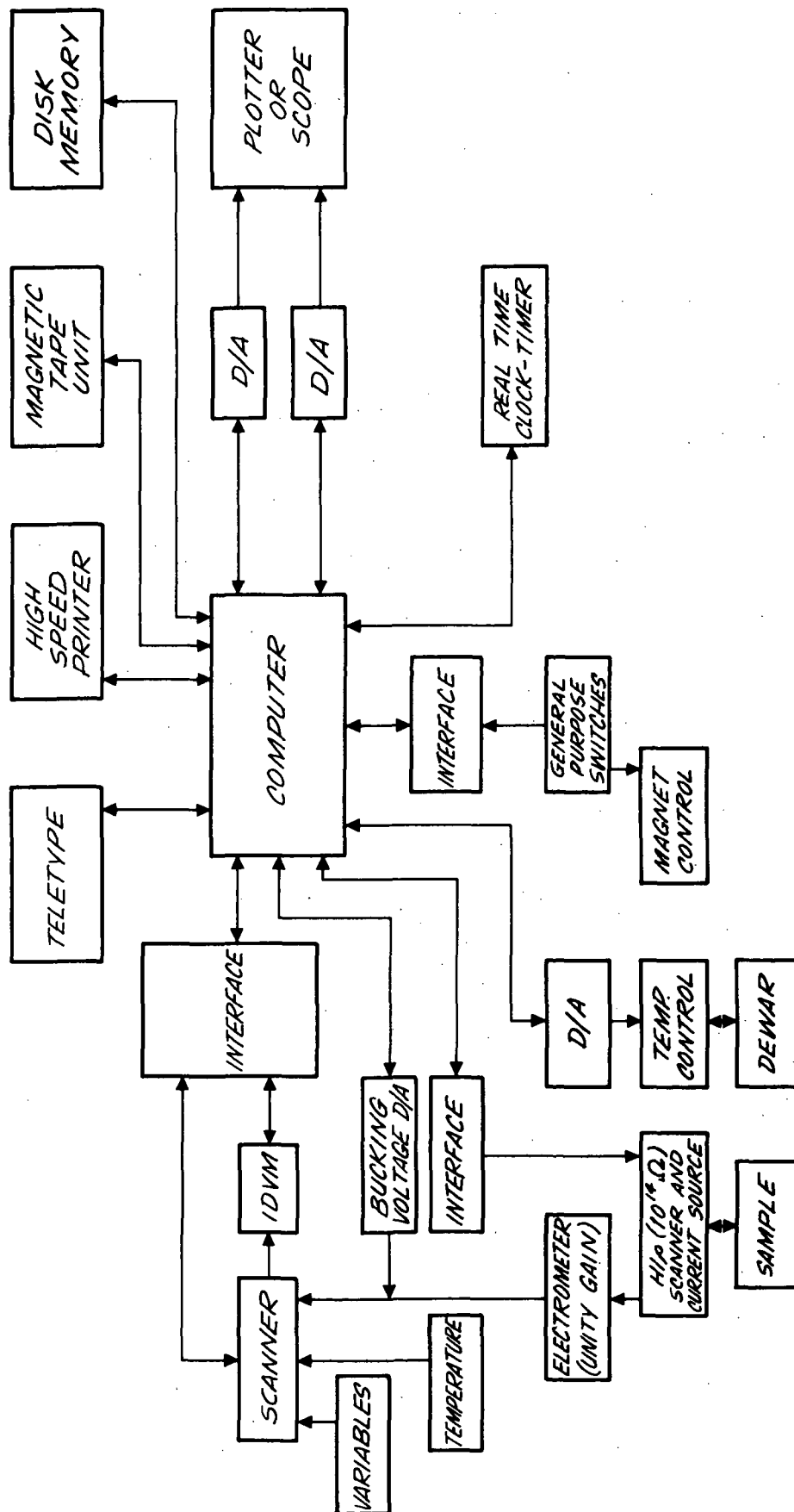


Fig. C-1. Digital Data Acquisition System Block Diagram.

Analog to digital conversion is provided by an integrating digital voltmeter (IDVM) with 1 μ V resolution out of 1 V and a 1 sec integration time for high noise rejection. A low level guarded scanner with <1 μ V offset precedes the IDVM. The voltage signal from the Hall sample is buffered by a differential electrometer amplifier of unity gain. This amplifier has 10^{14} Ω input impedance, 10 μ V and 1 fA p-p noise level (0.01 - 1 Hz), >145 dB common mode rejection, and a dynamic range of ± 20 V. The amplifier is guarded and provides individual driven guards for both inputs to minimize the effects of cable capacitance. A constant current source can be programmed from 2×10^{-9} A to 10^{-2} A in a 1, 2, 5 sequence with an accuracy of 0.1% and a compliance of 20 V. This circuit can also be used to measure sample current with an external constant voltage source (such as a D/A) applied to the sample. A special switching matrix which maintains $>10^{14}$ Ω insulation resistance and <1 μ V offset voltages, allows switching the current (or voltage) source onto any two of eight sample leads and also allows switching the input to the differential electrometer to any two of eight sample leads. A separate voltage source may be switched onto one of the sample leads to allow biasing the back of a sample. Provision is also made for the "zapping" of contacts. The versatility of the switching matrix allows Hall measurements to be made on any desired Hall pattern, from 4-lead Van der Pauw to 8-lead bar.

The computer controls 16 relays, two of which are dedicated to controlling the magnet, i.e., turning it on and off and reversing it. The maximum magnetic field available is 13 kg. Computer control of the magnitude of the magnetic field is planned for future expansion of the system.

The dewar is of the flowing gas type. At present, the sample temperature can be regulated from 4.2°K to 323°K by means of the computer providing a set point voltage (via a D/A) to the dewar temperature controller. The computer can sense when the sample temperature has stabilized and can measure the actual sample temperature by means of a platinum resistance thermometer.

B. SYSTEM SENSITIVITY

The sensitivity of the system is characterized by the equation for the Hall voltage V_H ,

$$V_H = \frac{BI}{N_s e} \times 10^{-8}, \quad (C-1)$$

where B is the magnetic field (g), I is the current (A), e is the electronic charge, and N_s is the surface concentration (cm^{-2}). Thus the maximum value of N_s that can be measured is given by

$$(N_s)_{\max} = \frac{B_{\max} I_{\max}}{e(V_H)_{\min}} \times 10^{-8}. \quad (C-2)$$

If $I_{\max}$ is determined by the current source ($I_{\max} = 10^{-2}$ A), $(V_H)_{\min}$ is determined for a signal-to-noise (S/N) ratio of $10[(V_H)_{\min} = 10^{-4}$ V], and $B_{\max}$ is the maximum available field (13 kg), then $(N_s)_{\max} \approx 8 \times 10^{16} \text{ cm}^{-2}$.

For small mobilities, the resistance of the sample rises until $I_{\max}$ is limited by the maximum voltage that can be applied to the sample $(V_s)_{\max}$. Typically the ratio of contact and contact arm resistances to the sample resistance is such that $(V_s)_{\max}$ is no more than about 5 V. This value is often

consistent with the limitation imposed by avoiding breakdown of the isolation junction. If the sample configuration is about 1 cm (as in the van der Pauw method), the sample resistance is numerically equal to the sheet resistivity, given by

$$R_s = (N_s e\mu)^{-1} \quad (C-3)$$

Substituting $I_{\max} = (V_s)_{\max}/R_s$ and eq. (C-3) in eq. (C-2), $(N_s)_{\max}$ cancels out and we are left with a minimum value for μ :

$$\begin{aligned} \mu_{\min} &= (V_H)_{\min} (B_{\max} (V_s)_{\max})^{-1} \times 10^{+8} \quad (C-4) \\ &\approx 0.15 \text{ cm}^2/\text{V-sec} \end{aligned}$$

for the above values. As R_s increases, the current noise Δi_n of the amplifier dominates, and $(V_H)_{\min}$ in (C-4) must be replaced by $10 \Delta i_n R_s$, where the factor 10 is the assumed S/N ratio. This yields

$$\begin{aligned} (N_s)_{\min} &\approx 10 \Delta i_n [B_{\max} (V_s)_{\max} e\mu^2]^{-1} \times 10^{+8} \\ &\approx 3.8 \times 10^{11}/\mu^2 \text{ cm}^{-2} \quad (C-5) \end{aligned}$$

As R_s increases further, it approaches the input impedance R_{in} of the amplifier, setting an upper limit on R_s of about $0.03 R_{in} \approx 3 \times 10^{12} \Omega$. This sets a further bound on N_s given by

$$\begin{aligned} (N_s)_{\min} &\approx (0.03 R_{in} e\mu)^{-1} \\ &\approx 2.1 \times 10^6/\mu \text{ cm}^{-2} \quad (C-6) \end{aligned}$$

Note that high contact or contact arm resistances could greatly increase the source impedance presented to the amplifier, which is what actually should be used for R_s in (C-5) and (C-6), and thus degrade the performance of the system considerably.

For large values of μ , the maximum field is limited by the condition that $(\mu B \times 10^{-8}) \ll 1$, in order that the low field Hall mobility be observed. Assuming that $\mu B_{\max} \times 10^{-8} = 0.1$ satisfies the condition, $(N_s)_{\max}$ becomes

$$\begin{aligned} (N_s)_{\max} &\approx \frac{0.1 I_{\max}}{\mu e (V_H)_{\min}} \\ &\approx \frac{6.7 \times 10^{19}}{\mu} \text{ cm}^{-2} \end{aligned} \quad (C-7)$$

These results are summarized in Fig. C-2, where the acceptable range of N_s and μ is indicated (the limitation implied by eq. (C-6) is too small to show).

An important limiting factor is the value of $(V_H)_{\min}$, which is determined by the noise of the electrometer buffer amplifiers. A decrease in $(V_H)_{\min}$ would proportionately move each of the boundary lines to increase the acceptable range of N_s and μ . The trade-off is that a decrease in amplifier noise is usually accompanied by a decrease in input impedance. This restricts the maximum value of R_s . For example, a state-of-the-art improvement in the amplifier might yield a noise level of 0.4 μ V and 4 pA p-p (0.01 to 1 Hz) with an input impedance of $10^9 \Omega$. This would improve performance to the dashed line in Fig. C-2, but note that the trade-off is a poor one for high values of R_s . A further improvement in input noise level and $(V_H)_{\min}$ can be achieved by converting to an ac excitation for the constant

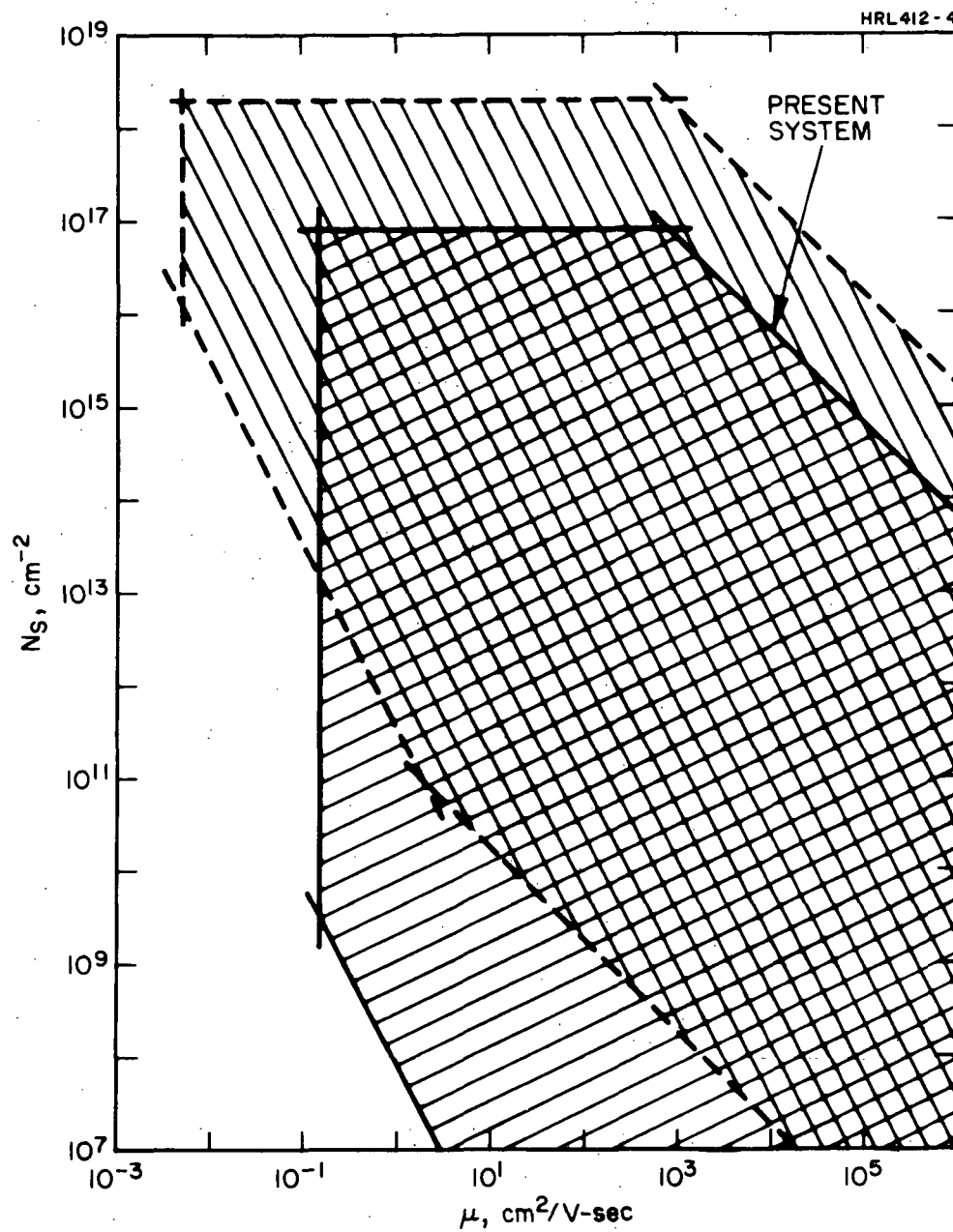


Fig. C-2. Relative Performance of Hall Measurement Systems.

current source and providing a lockin detector. However, it is difficult to maintain a high input impedance in an ac system because of the effects of input capacitance. Note that the present system has been optimized for high source impedances, and is useful over a very large range of parameters. It is only when pushing for extremely low mobilities or for higher doping densities than are normally encountered in ion implantation research that improvements to the system would be necessary.