NASA TECHNICAL MEMORANDUM

NASA TM X-68066

NASA TM X-68066

ASDTIC DUTY-CYCLE CONTROL FOR POWER CONVERTERS

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TECHNICAL PAPER proposed for presentation at the 3rd Annual Power Processing and Electronics Specialists Conference sponsored by the Institute of Electrical and Electronics Engineers Atlantic City, New Jersey, May 22-23, 1972

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E-6940

ABSTRACT

The application of analog signal to discrete interval converter (ASDTIC), a hybrid micromodule, two loop control subsystem, to a switching, step-down dc to dc converter is described in this paper. The power circuitry, interface and ASDTIC subsystems used in this switching regulator were developed to exhibit the improved regulation, transient performance, regulator stability and freedom from the effects of variations in parts characteristics due to environmental changes and aging. ASDTIC can be used with other types of power circuits that use duty-cycle control techniques by simple changes in the interface subsystem[1]. The circuitry and performance characteristics of a +10V dc switching converter as well as that of the ASDTIC micromodule are described. Realization of the ASDTIC hybrid micromodule has been accomplished with a hermetically sealed, beam-lead, bonded/deposited nichrome thin film resistors, discrete capacitors and integrated circuits on dilithic, glazed alumina substrates using 22 feed through terminals in an integrated package.

INTRODUCTION

The function of power converters in aerosapce systems is to transfer and transform electric power from the output terminals of generators to other forms as required by specific loads. Efficiency, size, weight, reliability, ripple, regulation, electromagnetic compatibility and stability all are important parameters in aerospace power converter systems. Important factors affecting the satisfactory achievement of these parameters are often poorly defined in the information given to engineers responsible for designing power converter systems. A recent study indicated that (2):

1. Power converter design requirements are, most often, established as input-output steady state characteristics by systems engineers.

2. Input-output specifications usually are restricted to voltage, current, and resistive load requirements.

3. Actual power sources involve time-varying and irregular current and voltage supplies; noise and transient irregularities are peculiar to the source type.

4. Actual specific loads are active electronic devices with time-varying and irregular current sinks; arcing and transient irregularities are peculiar to the load type.

5. Power converting tasks usually involve nonlinear problems of time-varying systems that are extremely complex to analyze.

From the result of this study, it became clear that optimum methods to transfer and transform electric power were very much dependent upon available devices, generating sources, and load parameters. These are constraints difficult to identify for future aerospace missions. The study did show that some commonality does exist in many power converters, particularly in the control and interface subsystems (2,3).

ASDTIC SUBSYSTEM DESCRIPTION

A power converter transfer device diagram is shown in Fig. 1. This switching power converter consists of three subsystems; power circuit, interface and ASDTIC subsystems. All switching power conditioning equipment diagrams can be redrawn into this generalized block diagram format. The un-

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[1]This paper is based on research and development directed by Dr. F. C. Schwarz at the National Aeronautics and Space Administration, Lewis Research Center, Cleveland, Ohio, Electronics Research Center, Cambridge, Massachusetts, and at TRW, Inc., TRW Systems Group, Redondo Beach, California under Contract NAS12-2017 (1).

regulated input power passes through an energy storage network or input filter to attenuate the switching current drawn by the switching power stage. The power controlled by the power switching stage is processed through an optional power transformer and output rectifier to the output filter energy network. The control subsystem collects information from the power subsystem in the form of analog signals and produces a sequence of control signals at discrete time intervals. The control signals cause rectangular voltage (duty-cycle) pulses to be generated in the power network for voltage transformation.

The ASDTIC control subsystem senses output voltage by means of a direct current (dc) loop and the energy storage in the output filter network by means of the alternating current (ac) loop. These two signals are summed, compared with a reference and integrated. The resultant signal activates a threshold detector which effects duty-cycle control of the power switch, via the pulse generator and power drive circuits in the interface subsystem.

In order to be widely applicable as a control subsystem for power processors, it was established that the ASDTIC hybrid micromodule should possess the following characteristics (4):

1. It shall generate a pulse train to effect the pulse generator whose ratio of time on to time on plus time off or duty-cycle is varied in accordance with input variations, load energy stored and load voltage as compared to a fixed reference voltage.

2. It shall have a duty-cycle control mode which will provide stable operation independent of input line and output load characteristics.

3. It shall be insensitive to component variations and provide a stable and temperature-compensated reference voltage

4. It shall provide a high gain dc control loop to provide tight regulation for low frequency input or output variations.

5. It shall provide a moderate gain (less than the above dc gain) ac control loop to provide stable operation at zero gain crossover beyond the output filter time constants.

6. It shall provide a duty-cycle modulated signal suitable for use with interface subsystems for various types of switching power converters.

Figure 2(a) shows the basic circuit diagram for a step-down converter with series switching transistor Q, commutating diode CR, output filter network LC1, pulse generator ($K_T = T_{on}$), ASDTIC control and reference. Voltages for seven nodes are identified in this diagram. Figure 2(b) shows five of these waveforms for a fixed output load: input line voltage E_{in}, inductor winding voltage E_L, integrator output voltage E_I, threshold detector voltage E_{TD} and pulse generator voltage E_{pG}.

At time T_o the integrator output voltage reaches the reference voltage level of the threshold detector, the threshold detector produces a pulse which activates the pulse generator circuit. In this example the pulse generator is assumed to produce an output for a fixed period ($K_T = T_{on}$).

During the off-time of the power switch Q, the inductor voltage is clamped to the output voltabe and the integrator voltage is forced up until the integrator reaches the threshold detector reference level. At which time, the power switch is commanded on again.

To show the effect that line variations have on the step-down power converter, assume that at some time T_1, the input line voltage is step-increased to a higher value. A higher voltage instantly appears at E_L to raise the energy stored in L. This forces the integrator output to go faster and to a lower value. After the power switch is turned off the integrator takes a longer time to reach the threshold detector reference level E_{TDR} delaying the turn on-time of power switch Q.

It can be observed from this simple example that immediate response is obtained for changes in the input line condition through the ac loop sensing the output inductor stored energy. The dc feedback loop for this case does not have to produce an error signal with a filter delay. The dc loop produces similar circuit response for variations in load voltage.

Preliminary mathematical stability analysis shows that with the proper selection of the dc and ac loop gain resistors R1 and R2, the ac loop can be made to crossover beyond the output filter time constants LC1. This makes the converter less sensitive to changes in output loading characteristics like increased output capacitances in the load equipment, or changes in the output load resistance.

ASDTIC AND STEPDOWN CONVERTER CIRCUITS DESCRIPTION

The ASDTIC subsystem schematic diagram is shown in Fig. 3. The subsystem consists of four circuits (see dashed sections in fig. 3): series regulator, dc summing amplifier, integrating amplifier and threshold detector. Figure 4 shows a complete schematic diagram for a +10V dc to dc step-down, switching converter. This converter consists of thirteen circuits (see dashed sections in fig. 4): booster, voltage divider, reference, gain, compensating, control, load, pulse generator, power switch, power drive, energy storage, noise suppression, output filter and overload protection.

Series Regulator

The series regulator consists of a voltage regulator integrated circuit (AR4, Type LM 100 F, fig. 3) and supporting circuit components (C3, C4, R19, R20, R21 and R22) which can provide up to 12 mA at +20V dc ±2 percent. Resistor R21 provides short circuit protection. The capacitor C4 provides output filtering. The resistors R19 and R22 provide a voltage feedback signal for comparison with an internal reference. The general character-

istics for the ASDTIC series regulator are given in table I.

Dc Summing Amplifier

The summing amplifier transfer device consists of a differential input operational amplifier (AR1, Type RM 4101-Q, fig. 3) which is unconditionally stable and has a unity gain crossover frequency of approximately 500 kHz. The amplifier is located on the alumina substrate with the exceptions of the voltage sensing gain resistors (R23 and R24, fig. 4) and a stabilizing compensation capacitor C7. The general characteristics for the ASDTIC dc summing amplifier are given in table I. The emitter follower output stage (Q1, fig. 3) provides low output impedance when in its linear range while providing current limiting by cutting off when the output current limits are reached.

Integrator

The integrator amplifier transfer device consists of a field effect transistor source follower and a differential input operational, amplifier (AR2, Type RA 909A and Q2A, B, Type KY 3956)

Electronic integrators, usually RC integrators, are widely used. The volt-seconds of a sample of a function are converted to a corresponding time interval in the application under consideration. This process is, however, largely dependent on the invariance of component characteristics due to variations in environmental conditions, including ambient temperature and aging of components. One objective of this program was to devise an integrator with the distinction of maintaining its accuracy of expected operation notwithstanding variations in its components characteristics, and variations of applied voltage waveforms and supply voltages within practical limits.

A circuit philosphy was developed that will vary the time base of its cyclic operation concurrent with the effects on the processing of signals that are due to variations of the characteristics of components included in this network. The read out of information from this network occurs against the same time varying time base. The former referred to effects of variations of components characteristics are in this way undone and the read out information is obtained as if the components had maintained their characteristics in an invariant form. It is this novel functional mechanism that distinguishes this approach from other networks of this kind which operate against preprogrammed time bases and are therefore, unable to cope with variations in the characteristics of their components. It is emphasized that this network philosophy utilizes the time variant characteristic of the same component to undo the effect of its own variation in characteristics rather than to call for compensation of these effects by other components.

The source follower has specially selected base resistors R5 and R6 so that the source follower has a drift error referred to the input of less than 3 mV. The general characteristics for the ASDTIC integrator are given in table I. The amplifier is located on the alumina substrate with the exception of the energy stored sensing gain resistors (R26 and R27, fig. 4) and the integrating capacitor (C8, fig. 4). The integrating capacitor is a computer grade, high quality mica capacitor with a TC less than 30 ppm/^{o}C with high insulation resistance.

Threshold Detector

The threshold detector transfer device consists of a differential input operational amplifier (AR3, Type RA 238, fig. 3), clamping diodes (CR3 and CR4, Type LP 100), and a three transistor digital driver (Q3, Q4 and Q5, Types MMT 3906 and 2369, respectively). The output swing of the operational amplifier is limited between 2 and 4 V dc by diode clamping an internal point in the operational amplifier. Limiting prevents the amplifier from saturating and exhibiting large storage times common in operational amplifiers (5). If the amplifier were allowed to limit in the negative direction, the emitter base reverse voltage rating would be exceeded in the level shift transistor Q3. The "low" output level is from the saturated drive transistor Q4. The "high" output level is the unconditioned input voltage at the generator impedance. The general characteristics for the ASDTIC threshold detector are given in table I.

The inverter transistor Q5 provides an output which is in phase with the input; provision is made in the hybrid module for use of either output, depending on the interface subsystem requirements. The threshold detector is located on the alumina substrate with the exception of an external load resistor (R29, fig. 4) and a jumper connecting pin 38 to pin 39. The selected operational amplifier used in the threshold detector is a compromise--not so fast as to require high power consumption (typically 100 mW), retains a moderate slew rate response (typically 2 V/μsec) and can be internally clamped with small power sacrifice to achieve a digital type output (diode clamp pin 13).

ASDTIC STEP-DOWN CONVERTER APPLICATIONS

The ASDTIC micromodule and the two loop control method have been applied to step-down converters (6,7). Figure 4 shows the complete schematic diagram for a +10 V dc to dc step-down converter used for a Brayton cycle signal conditioner power supply. The five waveforms explained in Fig. 2 are identified as nodes in this figure.

Essentially these waveforms describe a sampling process since the integrator is producing a frequency modulated pulse train by the action of the sensing voltage compared to the reference voltage. The action of the pulse generator with resistor-capacitor (R32, C9, fig. 4) timing is such as to produce a nearly constant volt-seconds on time-pulse (8).

From the input amplifier in the ASDTIC to the output threshold detector, a pulse amplitude modulated wave is converted into a constant volt-seconds duty-cycle modulated wave. Offset voltage

in the integrated circuit operational amplifiers is held to a minimum by careful component selection and testing. The effect of input offset voltage is to change the dc level shift but does not otherwise effect the operation of the ASDTIC hybrid micromodule. The effect of reducing load on the converter is to cause the inductor (L2, fig. 4) current to go to zero during an operating cycle; this would open the ac loop and cause unstable operation. A capacitor (C7, fig. 4) between the converter output and the integrator input maintains the ac loop during zero MMF inductance conditions damping the network for stable operation. The positive slope of the integrator output resistor-capacitor (R27 and C8, fig. 4) charging curve is such that the maximum duty-cycle at the pulse generator corresponds to the threshold detector's duty-cycle. A pulse at the power drive circuit corresponds to saturation of the converter power switch; the absence of a pulse corresponds to the converter transistor being in the blocking state. Operation of the output filter (CR13, L2 and C12, C13 and C14, fig. 4) has been explained in existing literature (9). Input filters, although not extensively used in the ten volt application, are generally required to meet EMC specifications; these filters are discussed entensively in existing literature (10).

Figure 5 shows a photograph of three independent step-down converters used for the Brayton cycle signal conditioner supplies. The three converters are rated at: +10V dc at 2A dc, -10V dc at 0.7A dc and +5V dc at 2A dc. The general characteristics for the +10V dc Brayton cycle signal conditioner supply are shown in table II. Nine Brayton signal conditioner power supplies using ASDTIC were built and are being used. A recent performance analysis showed an exhibited mean-time-between-failures of 6653 hours per failure and the units are still being tested (11).

Figure 6 shows an oscilloscope picture of the output transient response (bottom trace) due to positive and negative step changes in the input voltage (top trace) from 18V dc to 32V dc for a 20 W resistive load. The output voltage, during this transient, remains fixed at 10,000 V dc. The output ripple varies from 24 m Vpp to 52 m Vpp well within the 100 m Vpp required.

The general specifications shown in tables I and II are by no means firmly fixed or necessary conditions. For many applications less stringent specifications may be required and in these applications different versions of ASDTIC may be used. Future power converter specifications are bound to effect these present specifications. However, tables I and II give some data from which discussions to explain ASDTIC technology can be opened. Inquires concerning ASDTIC technology may be directed to:

Spacecraft Technology Division
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NASA-Lewis Research Center
21000 Brookpark Road
Cleveland, Ohio 44135

MICROELECTRONIC ASDTIC MODULE

The ASDTIC subsystem was identified as a candidate for hybrid microminiaturization. This subsystem has been realized as a hybrid micromodule consisting of bonded/deposited resistors, capacitors, and integrated circuits on alumina substrates (12). The interface subsystem which includes the pulse generator is still in the development phase being studied for future hybrid micromodule activity.

The ASDTIC hybrid micromodule consists of four integrated circuit packages, five transistors, four diodes, five capacitors and twenty-three nichrome, thin films resistors. The thin film elements are fabricated on two 6.35 cm by 3.81 cm glazed alumina substrates onto which the discrete components are bonded (13). The entire package dissipates approximately 500 mW of power most of which is developed in the threshold detector and output circuits. A photograph of the uncovered hybrid micromodule is shown in Fig. 7 where the four integrated circuit packages can be seen mounted on the alumina substrates and surrounded by the supporting thin film and discrete components.

The glazed alumina substrates are processed using standard integrated circuit processing techniques which are described in existing literature (12, 13, 14). The thin film resistors are adjusted to a precise value after fabrication to provide resistors with tighter tolerances and facilitate compensation for other components in the completed circuit. Adjustments in resistor values are made by physical cutting, evaporation or laser methods. Electrical tests of the substrate resistors are performed before and after silicon dioxide deposition and after thermal stabilization. Chip capacitors and resistors are attached to the substrate utilizing DuPont 5504A silver epoxy. Packaged components such as transistors, diodes and integrated circuits (integrated circuits are mounted on thin mylar film to minimize scratching and thermal cycle fatigue) are attached to the substrate by bonding with Dow Corning 3140 RTV silicone compound. This material is also used to bond the substrates to the package header.

CONCLUDING REMARKS

The application of analog signal to discrete time interval converter (ASDTIC), a hybrid micromodule, two loop control subsystem, to a switching, step-down dc to dc converter is described in this paper. The purpose of the ASDTIC control development program is to make available a general purpose control component with superior regulator stability, regulation, freedom from the effects of variations in parts characteristics due to environmental changes and aging, and transient response. The ASDTIC control component will enable standardization of future power conversion control subsystems.

The basic control subsystem has been fabricated as a hybrid micromodule for duty-cycle modulation which is intended to perform virtually all electronic control functions that are required in a

broad class of power converters. Several ASDTIC micromodules have been successfully processed, evaluated and installed in government agency equipment thus far. The ASDTIC development is still in process. The objectives of the current LeRC Contract NAS3-14394 are to verify and demonstrate the applicability of ASDTIC to three different types of power converters; to construct demonstrator models for education and training of personnel and to acquire knowledge in the area of power converter design that will be applicable to devise better power processors.

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TABLE I. - GENERAL ASDTIC SPECIFICATIONS

	Min.	Max.	Units
Series Regulators			
Output impedance (dc to 100 kHz)		2.0	
Output voltage	19.6	20.4	Vdc
Output current		12.0	mAdc
Phase margin		0.77	rad
Line rejection	45		dB
DC Summing Amplifier			
Input voltage	6.0	8.0	Vdc
Input offset voltage	-5	+5	mVdc
Linearity		50	µVdc
Tracking (-55° to 125° C)	-0.5	+0.5	mVdc
Input impedance	5		MΩ
Integrator Amplifier			
Open loop gain (dc)	19.8		dB
Slew rate	1.0		V/µsec
Input drift	-1.5		mVdc
Input impedance	1		MΩ
Threshold Detector			
Input current	-4	+4	µAdc
Rise time		0.3	µsec
Fall time		0.1	µsec
Delay time		1.0	µsec
Ouput current sink		10.0	mAdc

TABLE II. - PLUS TEN VOLT CONVERTER

GENERAL SPECIFICATIONS

	Min.	Max.	Units
Voltage variation[1]	9.966	10.039	Vdc
Worse case ripple	28	55	mVpp
Worse case voltage spikes	58	74	mVpp
Short circuit current	5.35	5.80	Adc
Efficiency	73.1	81.6	percent

[1]The parameter ranges for voltage variation measurements were: temperature, -54 to +85° C; load, 10 W to 20 W; input voltage range, 18V dc to 32V dc.

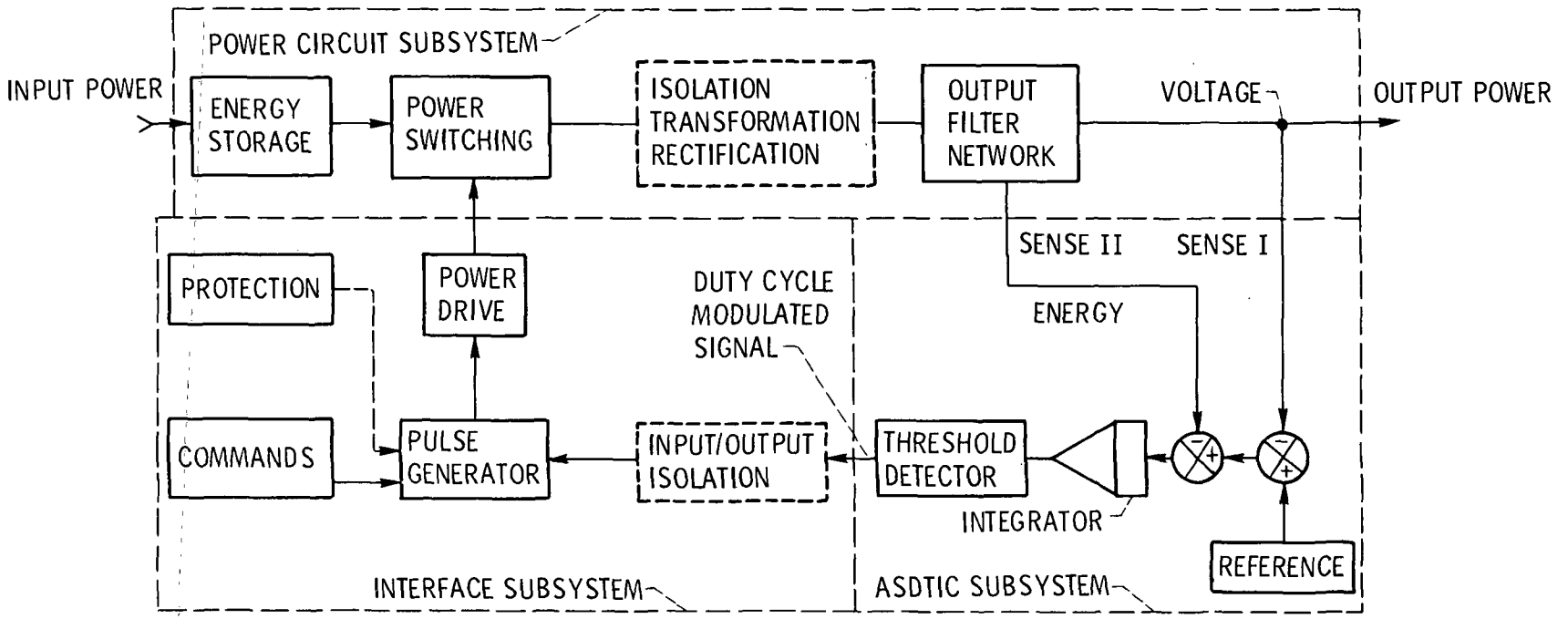
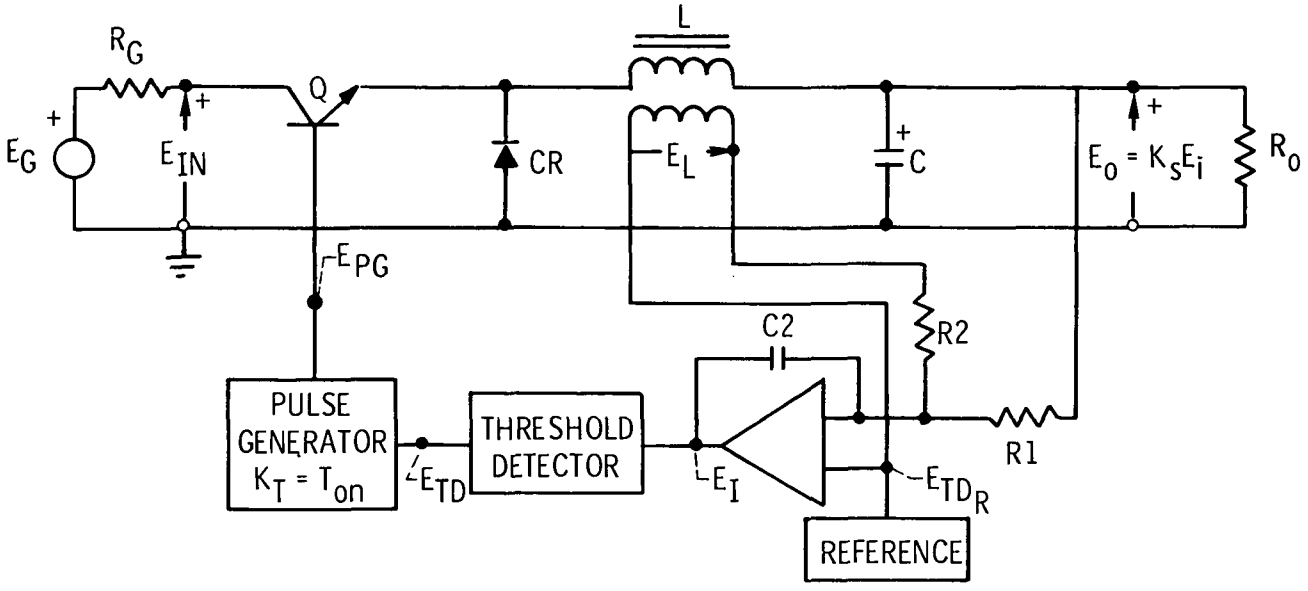
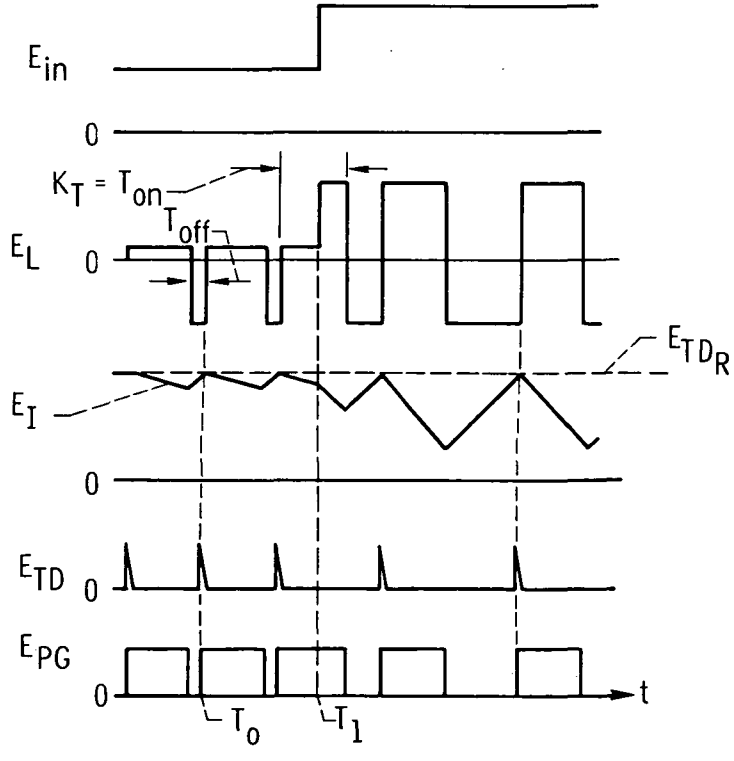


Figure 1. - Power converter transfer device diagram using ASDTIC control.



(a) BASIC CIRCUIT DIAGRAM.



TIME, μSEC

(b) WAVEFORMS.

Figure 2. - Step-down power converter application of ASDTIC.

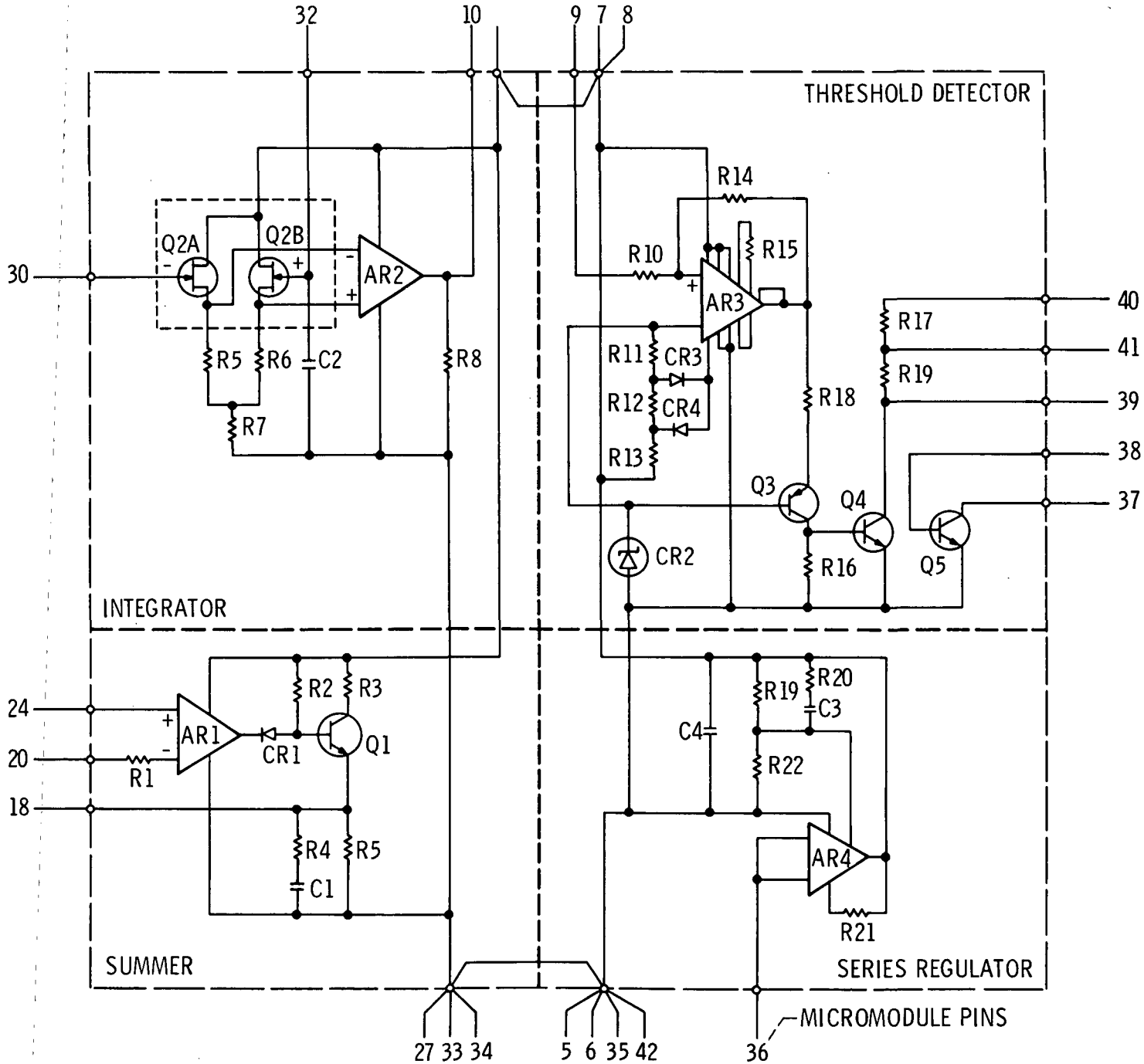


Figure 3. - ASDTIC schematic diagram.

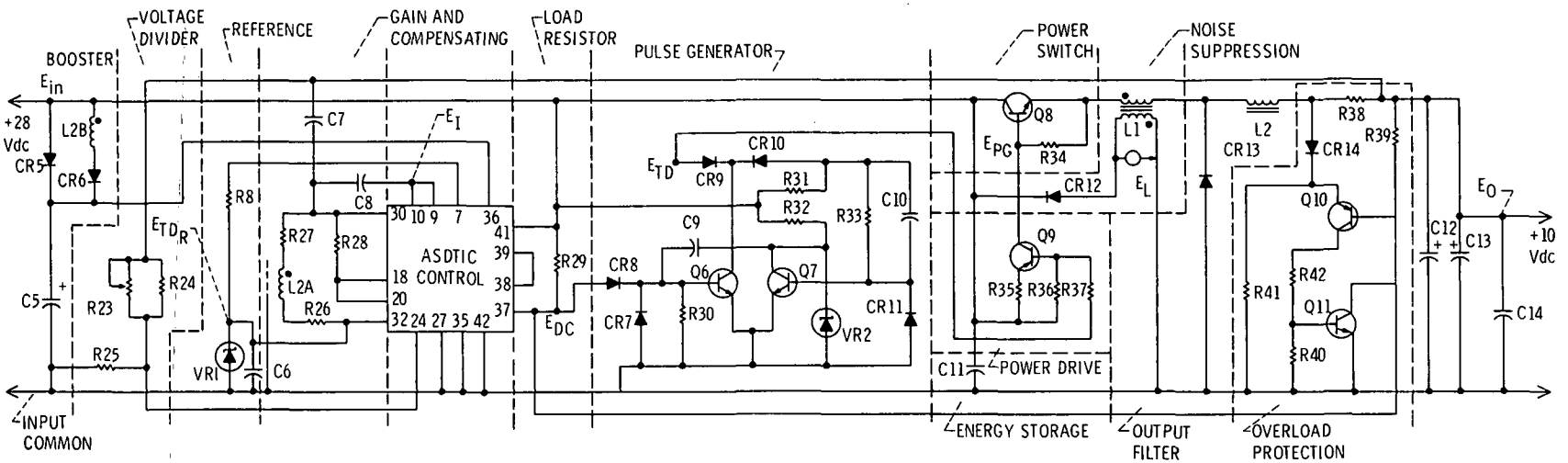


Figure 4. - Plus ten volt schematic diagram-ASDTIC application.

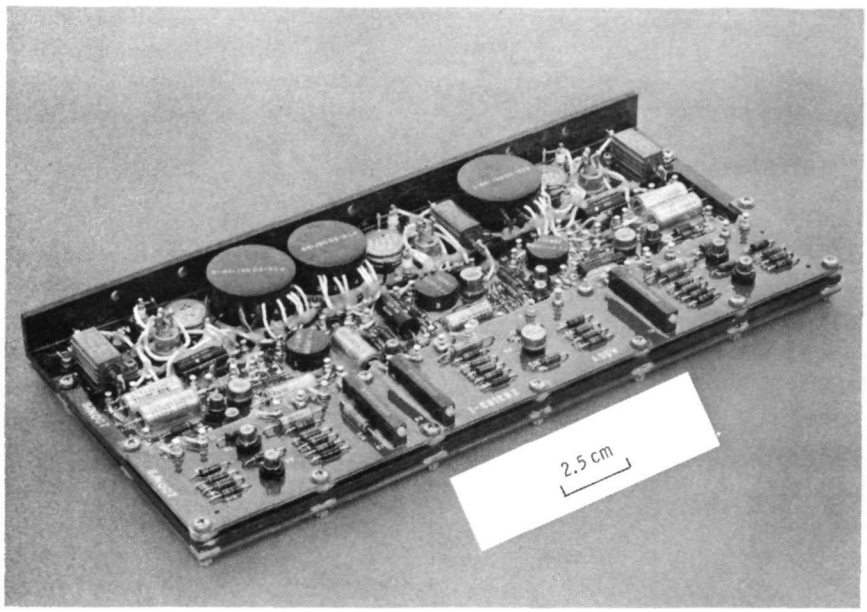


Figure 5. - Brayton cycle step-down converters.

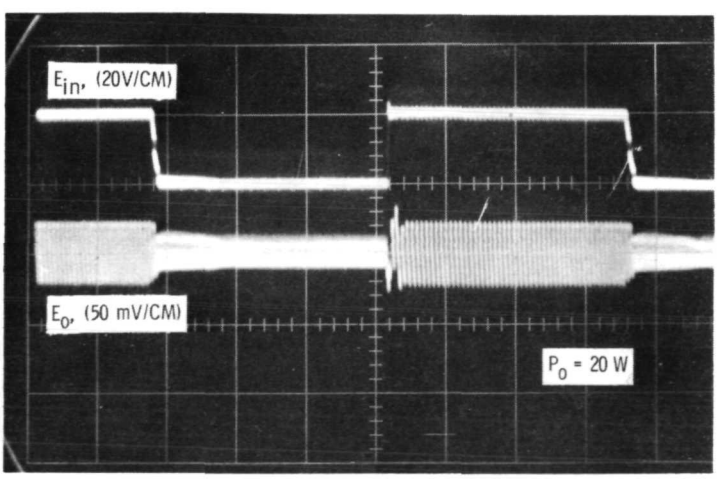


Figure 6. - Plus ten volt converter transient response.

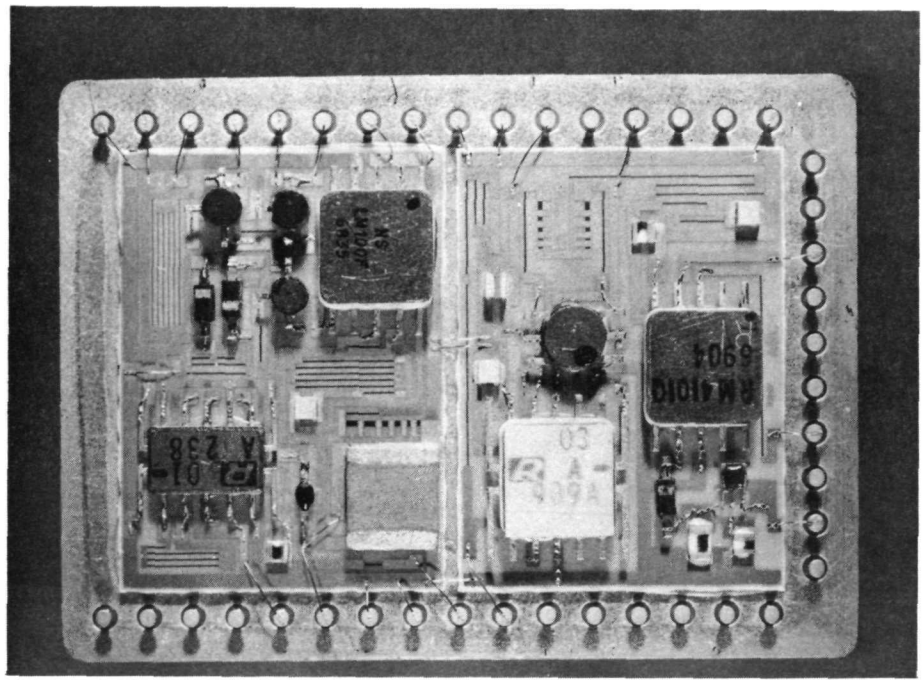


Figure 7. - ASDTIC hybrid micromodule (uncovered).