NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

SOFT X-RAY ASTRONOMY
PROPORTIONAL COUNTER ELECTRONICS

Prepared by

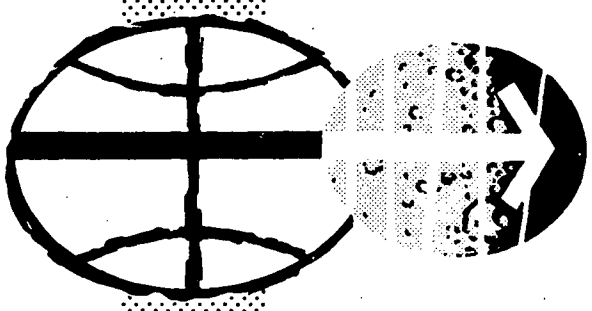
Lockheed Electronics Company, Inc.
Houston Aerospace Systems Division
Houston, Texas

Under Contract NAS 9-12200

For

PLANETARY AND EARTH SCIENCES DIVISION

National Aeronautics and Space Administration
Manned Spacecraft Center
Houston, Texas



MANNED SPACECRAFT CENTER
HOUSTON, TEXAS

December 1971

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SOFT X-RAY ASTRONOMY
PROPORTIONAL COUNTER ELECTRONICS

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HOUSTON AEROSPACE SYSTEMS DIVISION
HOUSTON, TEXAS 77058

SUMMARY

The X-ray Multiwire Proportional Counter is a flight type scientific instrument designed to measure cosmic X-ray fluxes at sounding rocket altitudes in the energy range of 0.1 to 10 KeV. Four instruments will be launched in a Black Brandt IV rocket employing different combinations of detector windows and gas.

The Multiwire Proportional Counter detector is constructed with two layers of twelve 1"x1"x18" cells. A columnator is mounted on the face of one layer whose cells are wired together alternately to form two main detector sections. The Electronics and Gas Regulation systems are mounted on the face of the second layer whose cells are wired together to form one Anticoincidence Detector section.

X-ray events occurring in any of the twelve main detector cells are converted into voltage pulses and measured with a 32-Channel Pulse Height Analyzer.

Normally X-rays will have short ionization paths in only one of the main Detector Cells at a time and won't enter the Anticoincidence Detector cells. To distinguish between X-rays and charged particles, the instrument includes a Coincidence Discriminator (to detect events taking place in two adjacent cells simultaneously), an Anticoincidence Discriminator (to detect an event taking place in an Anti-coincidence Cell), and a Pulse Rise Time Discriminator. The Pulse Rise Time is equal to the Charge Collection Time which is inversely proportional to the ionization path length.

The instrument includes an Automatic Gain Control (AGC) system designed to maintain constant system gain during the data collection under conditions of varying gas pressure and gas impurities. The AGC system employs feedback control of the detectors high voltage.

A Nikon camera, with an automatic picture-taking control system, is to be flown with the four gas proportional counters to correlate the rocket's pointing direction with the astronomical source of the X-rays.

ACKNOWLEDGEMENTS

Acknowledgement is made of the contributions of the following persons for their efforts on behalf of this project:

Dr. Donald Robbins for his scientific and technical direction.

Dr. John Mack for his contributions to the detector-electronics interface.

Dr. Michael Lampton for his technical advice.

Bob Trittipo, Jerry Winkler, Daya Patel, Bill Holtman, and Mike Withey for the design, fabrication, and testing of the X-ray electronics.

Their efforts are sincerely appreciated.

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1. INTRODUCTION

The instrument described in this report was designed for a rocket borne experiment in the field of X-ray astronomy. The objective of the experiment was to measure and study the sources and diffuse background of extra-solar X-rays in the energy range from 0.1 – 10 KeV. Measurements of stellar X-rays in this range can only be made above the atmosphere at altitudes greater than about 120,000 ft. This experiment was designed for the Black Grandt VC rocket. The basic design of detector and electronics was taken from suggestions made by the University of California under NASA contract NAS 9-11024. Major redesign of all electronic components was done by the Lockheed Electronics Co., Inc., under NASA contract NAS 9-5191. Scientific investigators from NASA-MSC and the University of Houston provided technical direction for the project.

The electronic systems were completed in August 1971. Because of reductions in the NASA budget, the planned flight for the summer of 1972, from White Sands, New Mexico, was cancelled. A proposal was made to Kitt Peak National Laboratory through the University of Houston for a rocket ride. However, this request was unfruitful. Other sources of assistence in acquiring a rocket ride are being investigated. In addition, a proposal has been made to NASA-MSC to fly an X-ray astronomy experiment using technology developed for this project on the Post Apollo International Rendezvous and Docking Mission.

2. SYSTEM

The wiring Schematic, Soft X-Ray Equipment (with wiring interconnections) is shown in Figure 2-1.

The detector is wired into three sections: an Anticoincidence Section and two Main Sections. An event in the detector is converted into a pulse, the height of which is proportional to the energy of the X-Ray event. A Pulse Height Analyzer converts the pulse heights into five bits of digital data. Three additional bits of data (bringing the total to eight bits per pulse) are generated by discriminators. These three additional bits are generated by the discriminators under the following circumstances:

- A charge collection time (Pulse Rise-Time Discriminator).
- The simultaneous occurrence of an event in both main sections (Coincidence Descriminator).
- The simultaneous occurrence of events in the Anticoincidence Section as well as in either of the two Main Sections (Anticoincidence Discriminator).

The tail pulses from the change-sensitive preamplifiers are amplified (without shaping) by the "fast" amplifiers, to provide large tail pulses for the Rise Time Discriminator. The large tail pulses are then shaped and summed in the Main Post Amplifier.

The Pulse-Height Analyzer (PHA) consists of a linear gate, a pulse stretcher, and a successive approximation Analog-to-Digital Converter. The PHA control opens the linear gate when a pulse occurs, initiates the Analog-to-Digital conversion,

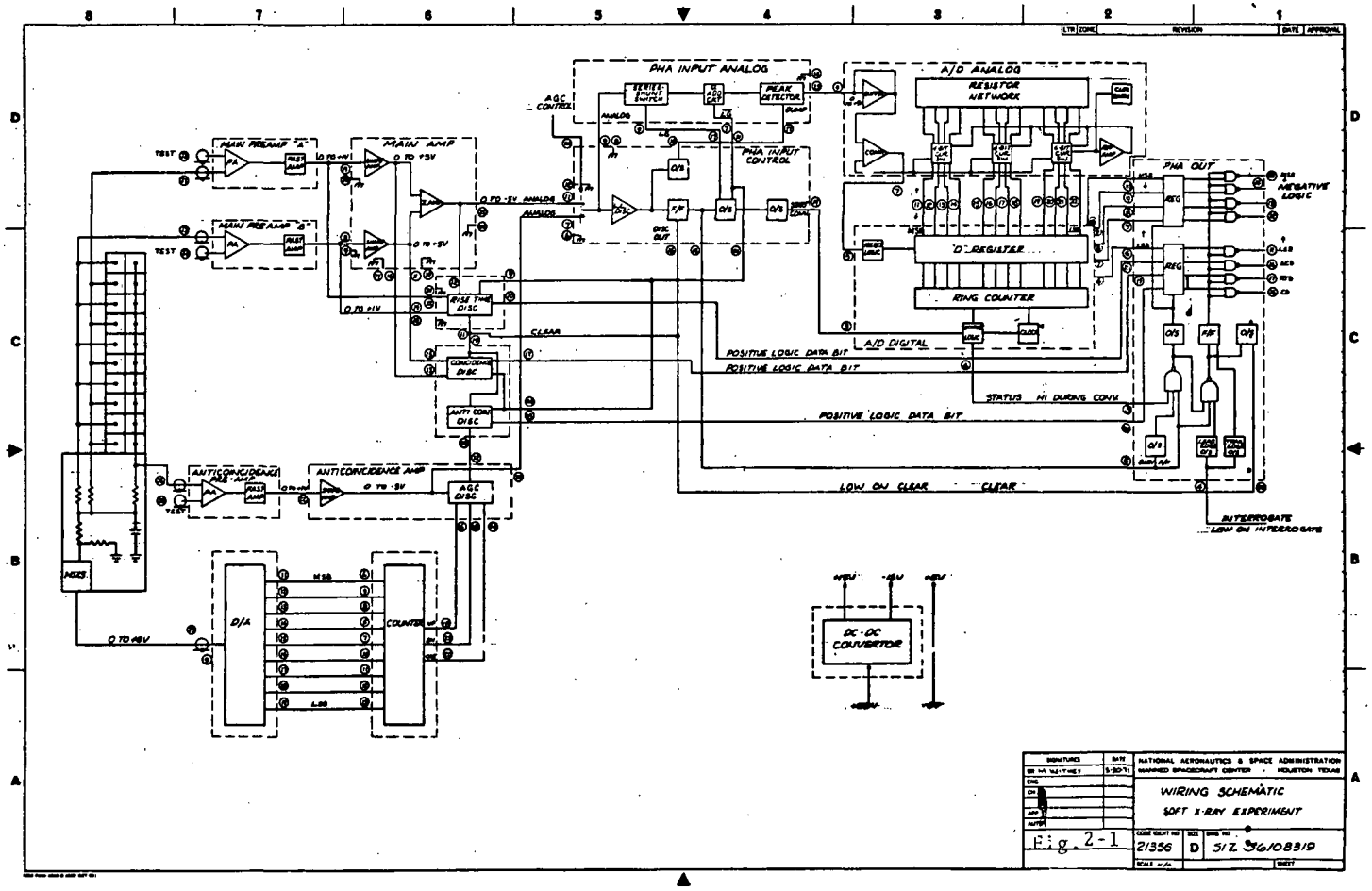


Fig. 2-1

Figure 2-1. — Wiring Schematic, Soft X-Ray Experiment

and generates a dump command (to discharge the pulse stretcher when conversion is complete). It also pulse-gates the discriminators, guaranteeing that any generated discriminator bits correspond only with the pulse being analyzed by the PHA. The PHA control also sends a busy signal to the telemetry interface when a pulse is received. The busy signal is removed when the PHA control receives a CLEAR pulse from the telemetry interface.

The five bits of pulse height data (from the A-to-D Converter) and the three discriminator bits are transferred to the Telemetry Interface Storage Register when a conversion is completed. The data is made available to the telemetry when the DTL output gates are enabled. This transfers the data from the storage register to the gate outputs. The DTL gates are enabled only when the following conditions occur simultaneously: an interrogate pulse is received, the "busy" signal is present, and the A-to-D Converter is not converting.

An Automatic Gain Control System is incorporated to maintain constant overall system gain during those periods when the gas gain of the proportional counter changes. These changes may occur due to deterioration of the gas, pressures change, or for other reasons. This system is based on a paper by Mike Lampton ("Feedback Control of Proportional Counter Gain", Review of Sci. Inst., January 1971). The system utilizes a Kev Iron-55 calibration source located in the Anticoincidence Detector Section. A discriminator outputs UP pulses to an up-down counter if pulse heights are below the discriminator level and DOWN pulses to the counter if the pulses are above the descriminator level. The up-down counter's output programs a Digital-to-Analog Converter which controls a programmable,

high voltage power supply. Changes in the High Voltage Detector bias compensate for changes in pressure and impurity in the detector and thus enable it to maintain constant gas gain and the pulse heights.

SYSTEM GAIN PARAMETERS

When the energy of an X-Ray event reaches 10 KeV, the electronics system of the proportional counter produces a 5 volt semigaussian pulse at the amplifier input to the Pulse Height Analyzer.

The charge deposited on a detector anode wire when an X-Ray event occurs is:

$$Q = \frac{E\ G_{DET} e}{W}$$

where E = X-Ray energy, eV

G_{DET} = detector gas gain, electrons per electron

e = electron charge, coulombs per electron

W = gas work function, eV per electron

The voltage from the amplifier is:

$$V_{PA} = \frac{AQ}{C_f} = \frac{E\ G_{DET} e}{C_f\ W}$$

where Q_f = preamplifier feedback capacitor, farads

A = amplifier gain, volts/volt

Block diagrams with the main channel gain parameters, are shown in Figure 2-2.

Automatic Gain Control System Parameters

The automatic gain control system operates with a P-10 proportional Counter Detector. It is capable of "locking-on" in flight. It reaches equilibrium within one second. It can maintain the detector's gas gain at 10,000 over the pressure range of 1.1 to 2.1 atmospheres. It does this with less than 1 percent deteriorization in the pulse height resolution as compared with the fixed voltage-pressure of Fe^{55} histograms.

The important system parameters are:

- The detector pressure vs voltage vs gas gain.
- The strength of the Fe^{55} calibration source.
- The preamplifier-amplifier gain.
- The mean discriminator level.
- The number of bits in the up-down counter and Digital-to-Analog Converter.
- The high voltage supply range.

The preamplifier and amplifier gains in the AGC channel are identical to those in the main channels. The mean level discriminator is set at 3 volts for the 6 Kev Fe^{55} source which sets the pulse level for the maximum energy 10 Kev X-rays at 5 volts.

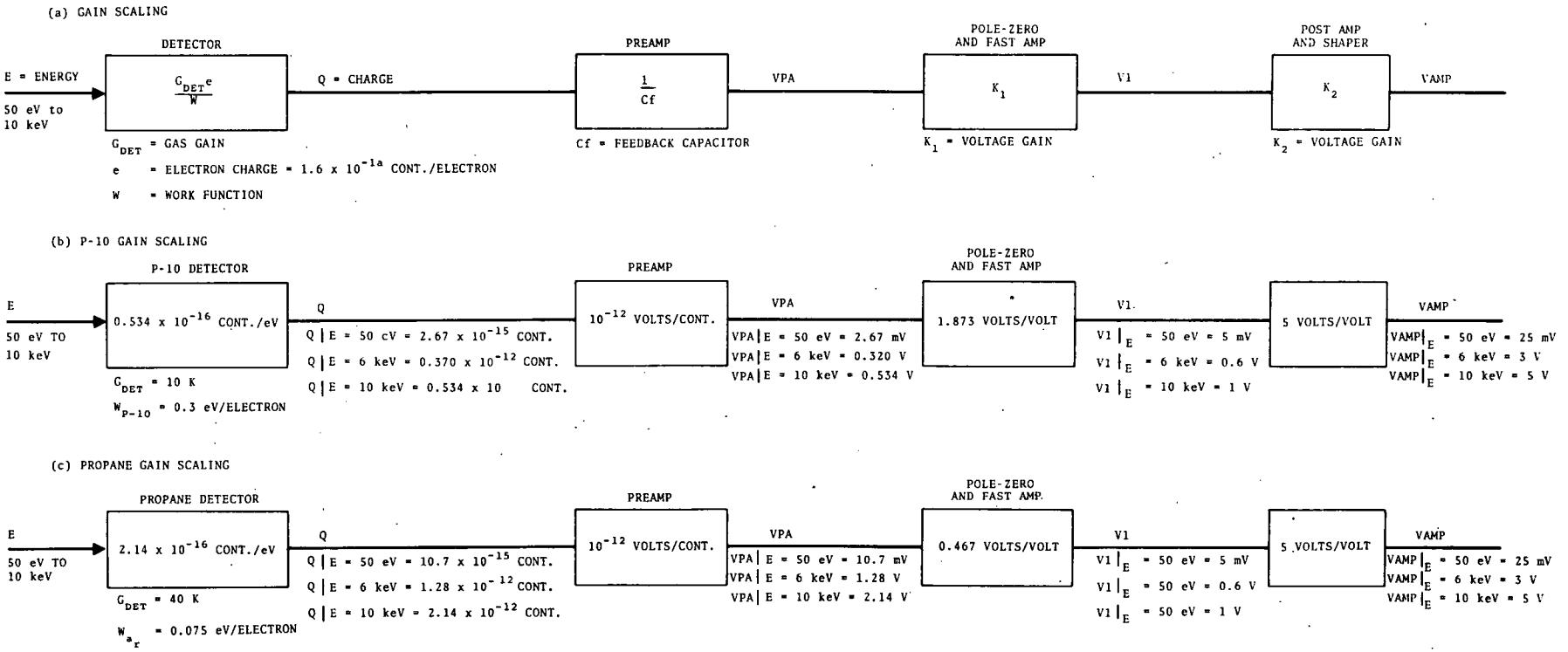


Figure 2-2 Main Channel Gain Scaling

The count rate from the Fe^{55} source is limited to 1000 counts per second to avoid main channel contamination. Nine bits in the Digital-to-Analog Converter and Up-Down Counter result in the required response and resolution (see Lampton's paper in Appendix A for the resolution and response equations). The high voltage supply has a range of 1500 to 2600 volts. From the gas gain vs voltage vs pressure curves, shown in Figure 2-3, it is seen that 1850 volts are required to maintain the gas gain at 10,000 when the pressure is 1.1 atmospheres. 2,000 volts are required to maintain the gas gain at 10,000 when the pressure is 2.1 atmospheres.

With a propane gas proportional counter detector, the Automatic Gain Control System must maintain the gas gain at 40,000 in flight at a pressure of 0.2 atmospheres and allow a pulse from an Am^{241} source to be seen on the ground at 1.2 atmospheres. From the gas gain vs voltage vs pressure curves for propane, shown in Figure 2-4, it is seen that 1630 volts are required to maintain the gas gain at 40,000. At 2.2 atmospheres the propane gas gain is only 50 which will not produce a large enough pulse from the Fe^{55} source to operate the AGC. For ground checkout an Am^{241} source will be installed in the rocket door and should produce enough charge in the counter per event to operate the AGC at a gas gain as low as 10. During the flight the Am^{241} source will be removed when the rocket door is opened and the AGC will operate with the Fe^{55} source.

High Voltage Bias and Filter Network

The high voltage bias and filter networks and the preamplifier's feedback network were designed to allow a high gas gain slew rate during the initial AGC "lock-on" and yet still provide enough filtering to prevent high voltage changes to appear

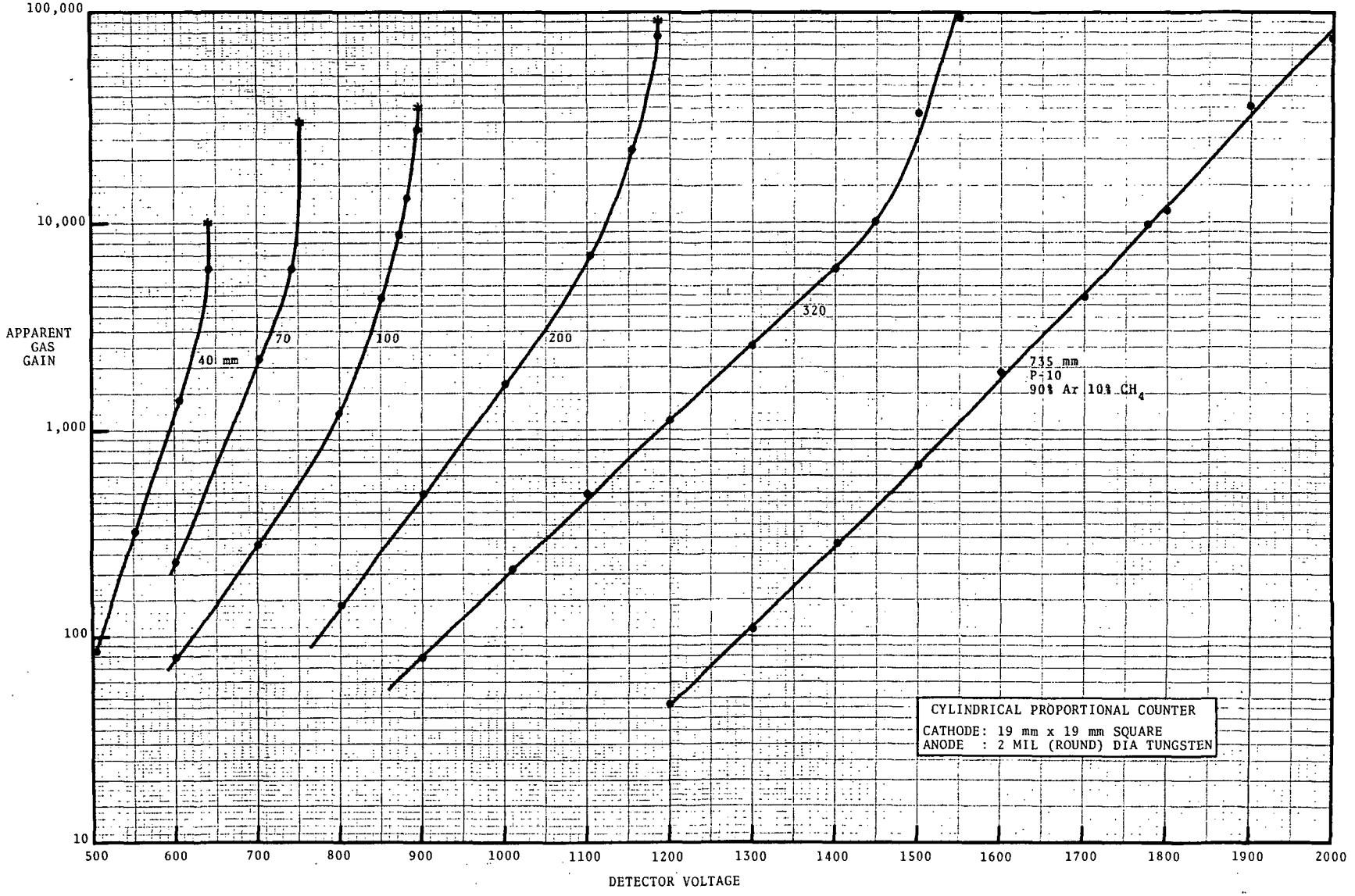


Figure 2-3. – P-10 counter pressure versus voltage versus gas gain curves.

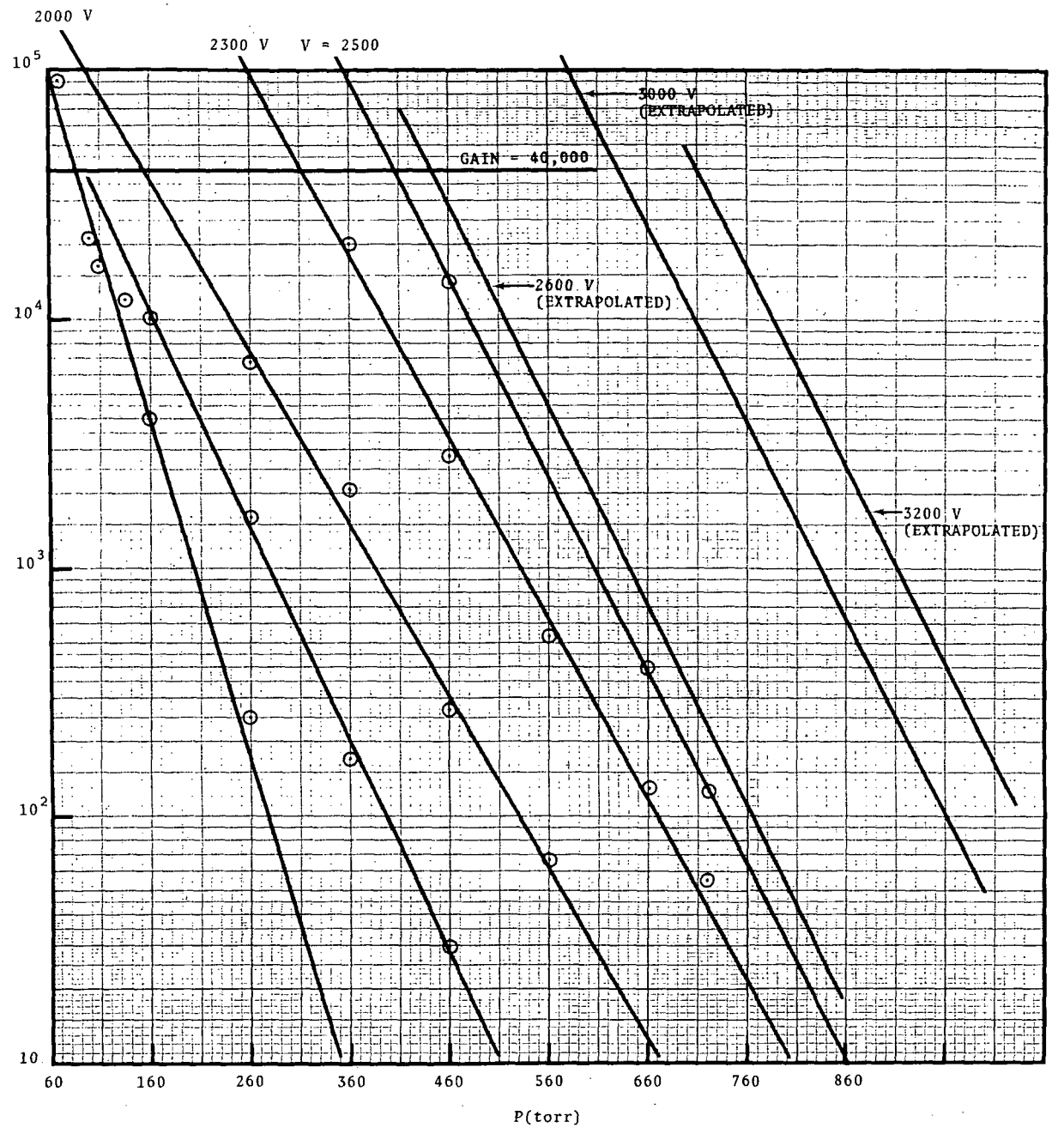


Figure 2-4. – Propane Counter Pressure Versus Voltage Versus Gas Gain Curves.

as noise at the preamplifier's output.

The Automatic Gain Control System is shown in Figure 2-5, detailing the bias and filter networks. 40MΩ resistor (R) loads the Velonix high voltage power supply at 50 percent of full load, allowing a minimum of 1,000 volts per second slew rate. A one second time constant filtering is provided by 10MΩ resistors (R1A, R1B and R1C) and 0.01 microfarad capacitors (C1A, C1B and C1C). High frequency isolation between the high voltage supply and the three detector sections is provided by 10MΩ resistors R2A, R2B and R2C. Coupling the pulse charge from the detector into the preamplifier are 1,000 picofarad capacitors C2A, C2B and C2C.

The preamplifier's tail pulse time constant is 10^{-5} seconds determined by the 1.0 picofarad capacitor C_f and the 10MΩ feedback resistor R_f. Feedback resistor R_f can't be reduced below 10MΩ because of the increase in thermal noise generated by the preamplifier as discussed in section 3.2. However, the feedback time constant is much smaller than the main filter time constant so that step voltage changes in the high voltage supply, produced by the Auto-Gain Control, do not significantly affect the preamplifiers output. The voltage change in the preamplifier produced by a high voltage change may be expressed as:

$$\frac{\Delta VPA}{\Delta HV} = \frac{C_2}{C_f} \times \frac{\tau_f}{\tau_1} = \frac{1000pf}{1pf} \times 10^{-5} = 20 \text{ millvolts}$$

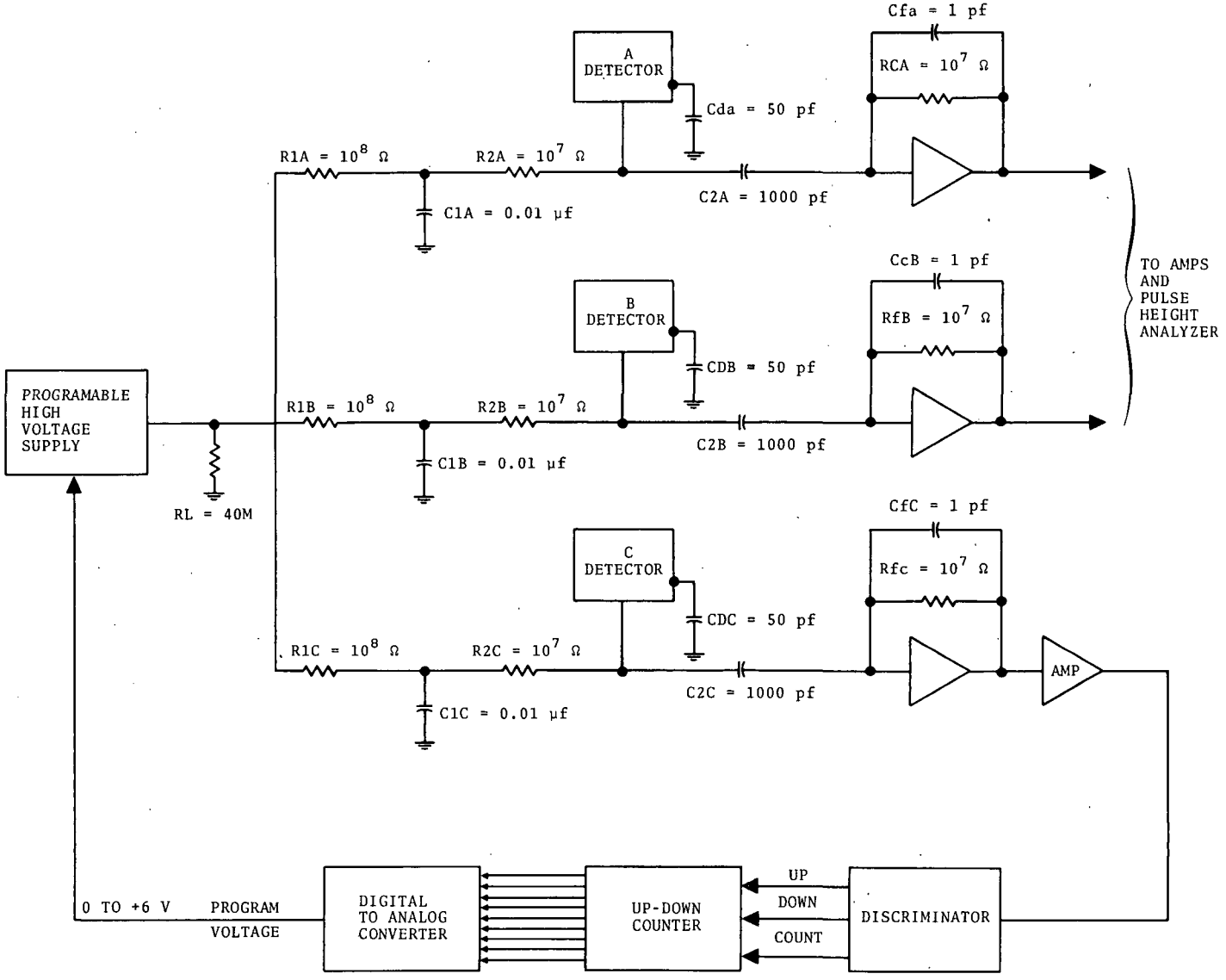


Figure 2-5. — AGC System Detailing Bias and Filter Networks

$\frac{Y_f}{Y_1}$ = ratio of feedback to main filter time control

$\frac{C_2}{C_f}$ = ratio of coupling to feedback capacitors

The 20 millivolts is negligible because of its low frequency which makes it appear as a base line shift easily removed by AC coupling.

3. ELECTRONIC PACKAGING

The proportional counter electronics are hermetically packaged in a sealed aluminum housing as shown in the isometric exploded assembly drawing of Figure 3-1. A detailed drawing of the electronics housing is shown in Figure 3-2. Figures 3-3 through 3-6 depict the details of the electronic housing's top cover, bottom cover, PC card guides, and gasket.

The major portion of the electronics are mounted on 11 3.2 in. by 2.8 in. printed circuit boards. Each circuit board plugs into a 22-pin Winchester connector mounted in the base of the housing.

Each of the three preamplifiers and the DC-to-DC Converter are packaged in individual aluminum housings and are located within the main electronics housing. Details of the preamplifier housing and cover are shown in Figures 3-7 and 3-8 respectively. Details of the DC-to DC converter housing and cover are shown in Figures 3-9 and 3-10 respectively.

Power enters the housing via a 9-pin cannon connector mating and data exists via a 15-pin connector, 9-pin and 15-pin test connectros are provided with pin-for-pin jumpers to the power and data connector. The incoming power and power grounds are filtered by Erie filtercons. The three detector inputs, the three preamplifier test imputs, and the control signal to the high voltage supply are routed through the housing by means of miniature Sealectro Convex coaxial connectors. These coaxial connectors have disconnects on either side of the housing to permit easy preamplifier removal.

The camera is mounted with the camera control electronics as shown in the isometric explode assembly drawing, Figure 3-11.

Figures 3-12 through 3-15 depict the details of the Camera Control Housing and Cover, Digital Display Projector Housing, and the camera clamp.

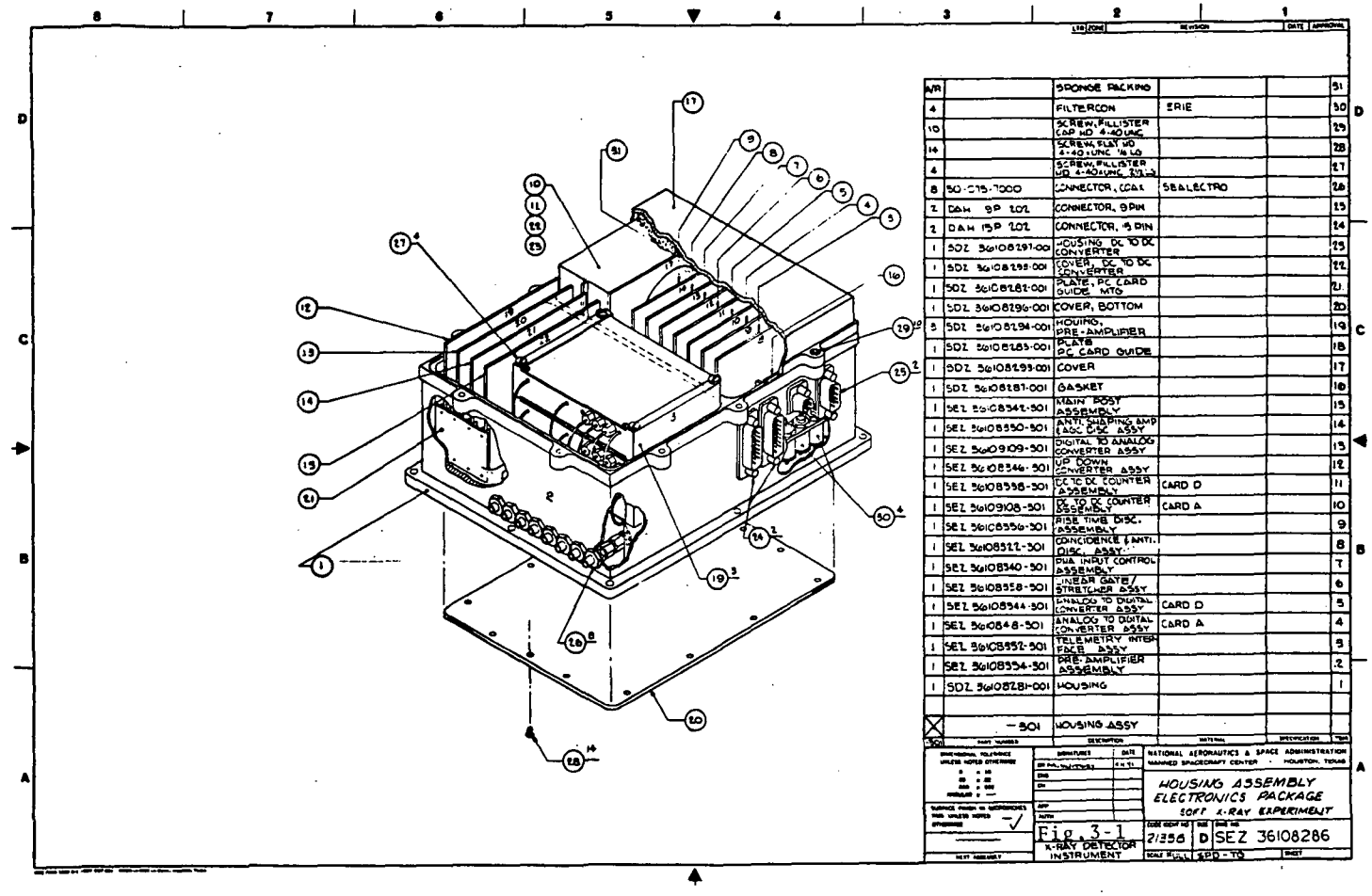


Figure 3-1. — Housing Assembly, Electronics Package

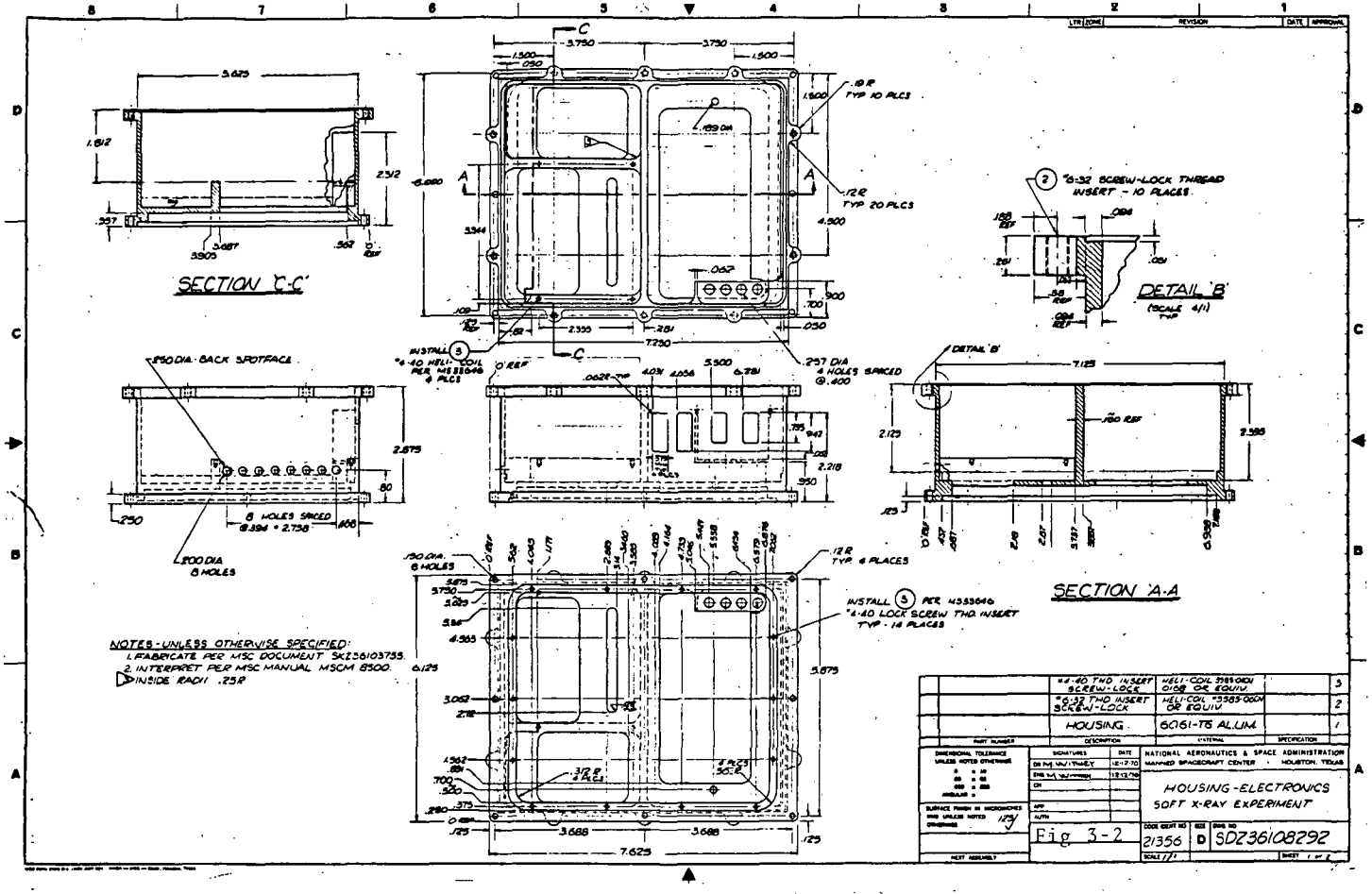


Fig 3-2

Figure 3-2. — Housing, Electronics

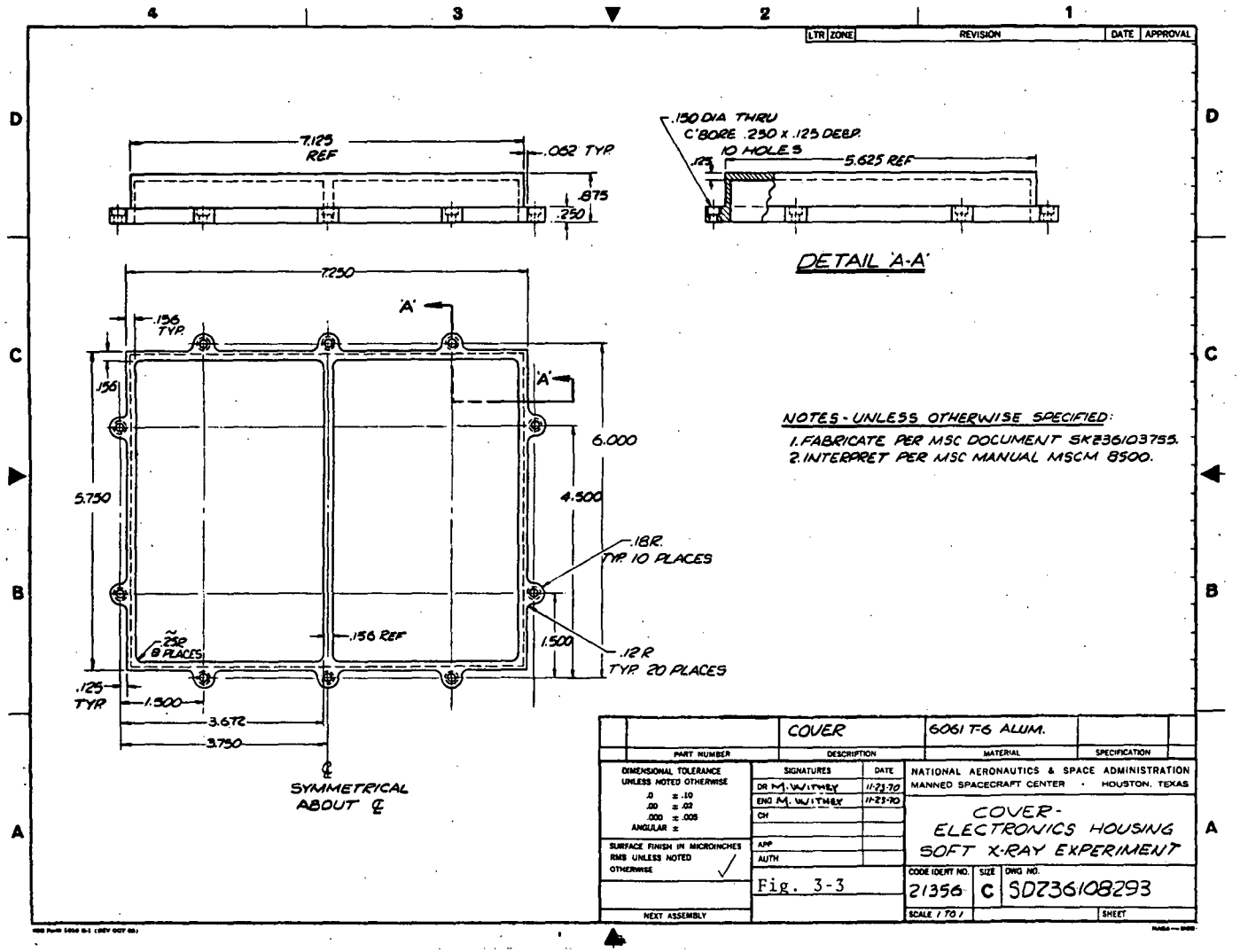


Fig. 3-3

Figure 3-3. — Cover, Electronics Housing

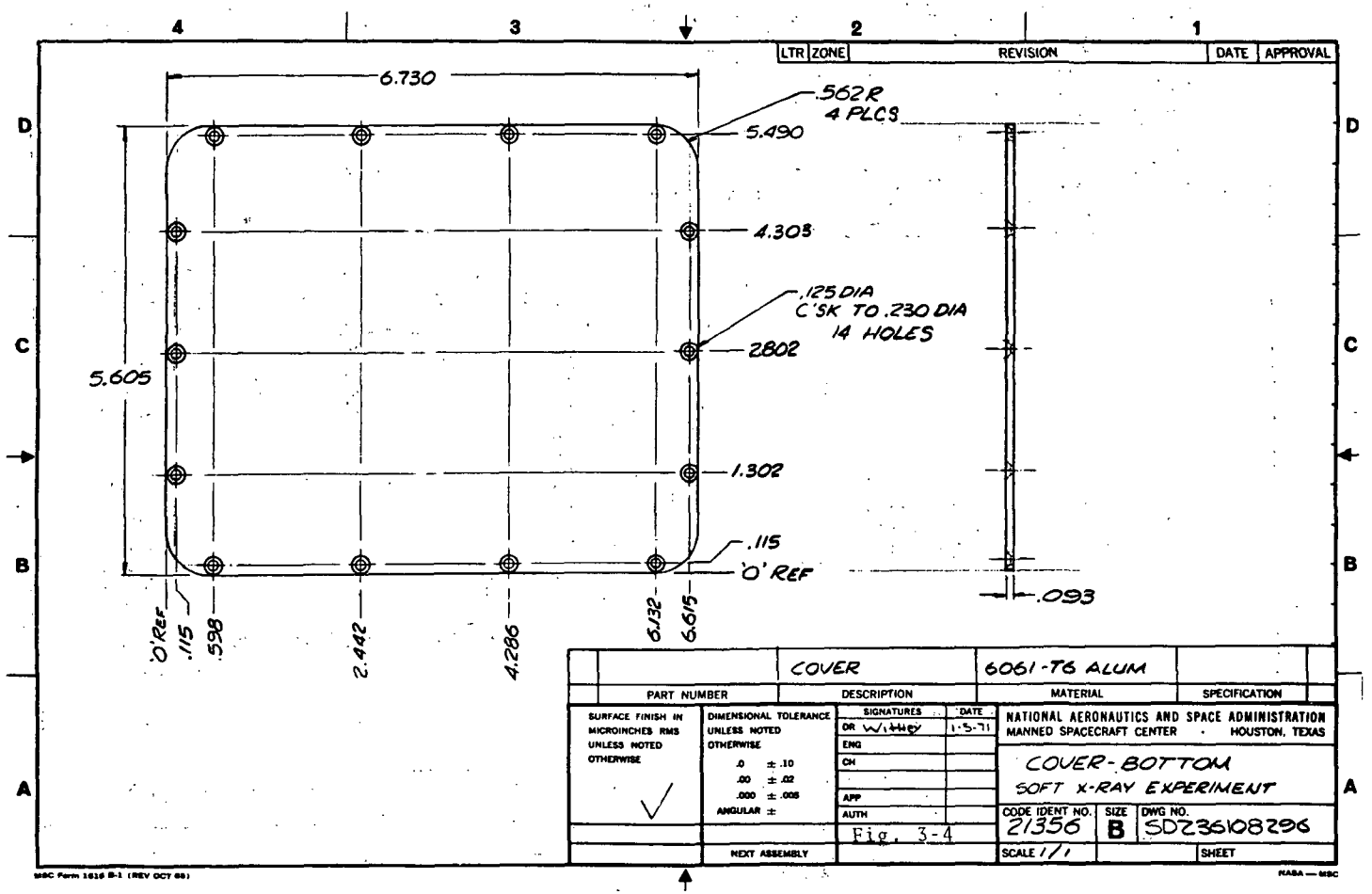


Fig. 3-4

Figure 3-4. — Cover-Bottom

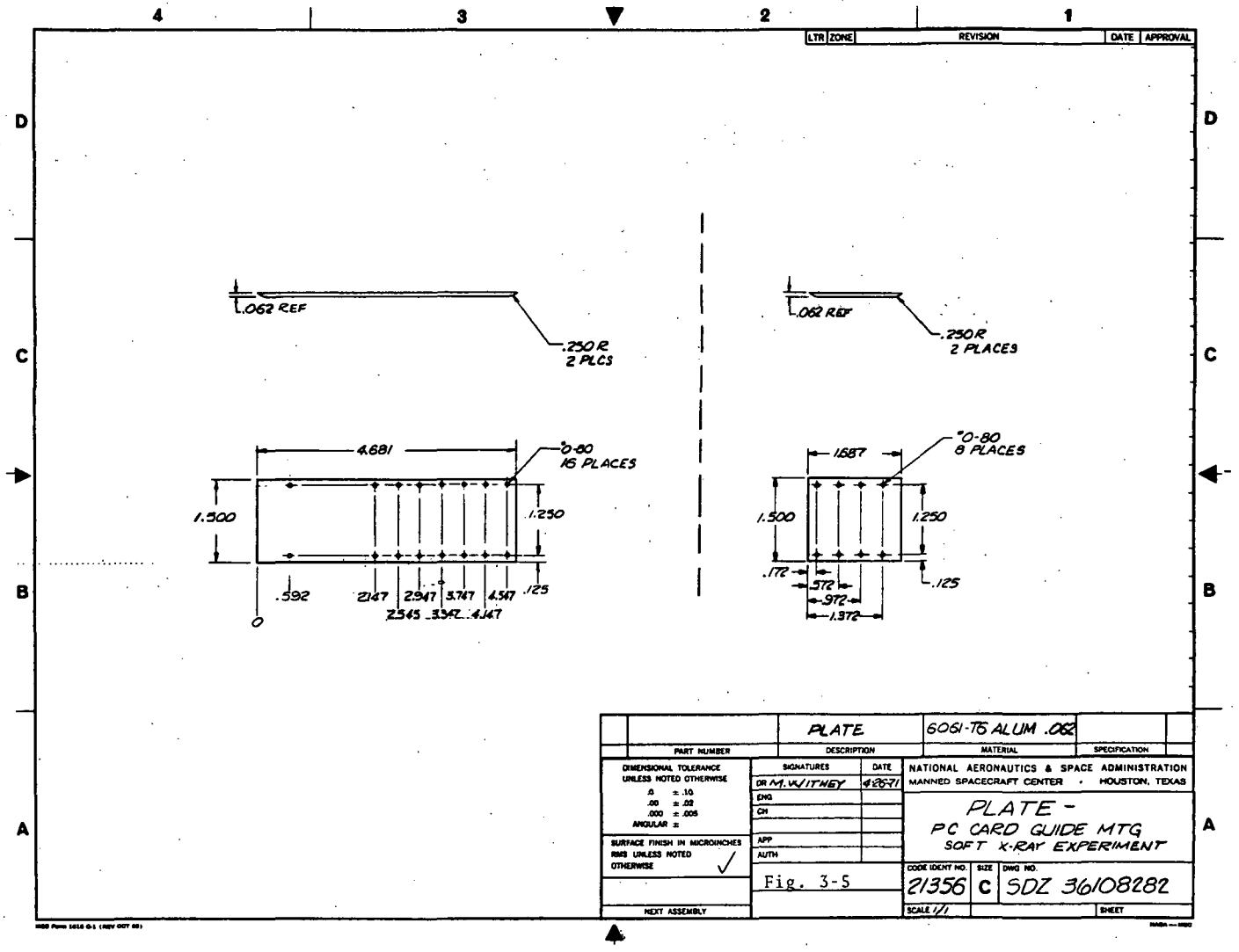


Fig. 3-5

Figure 3-5. — Plate-PC Card Guide Mounting

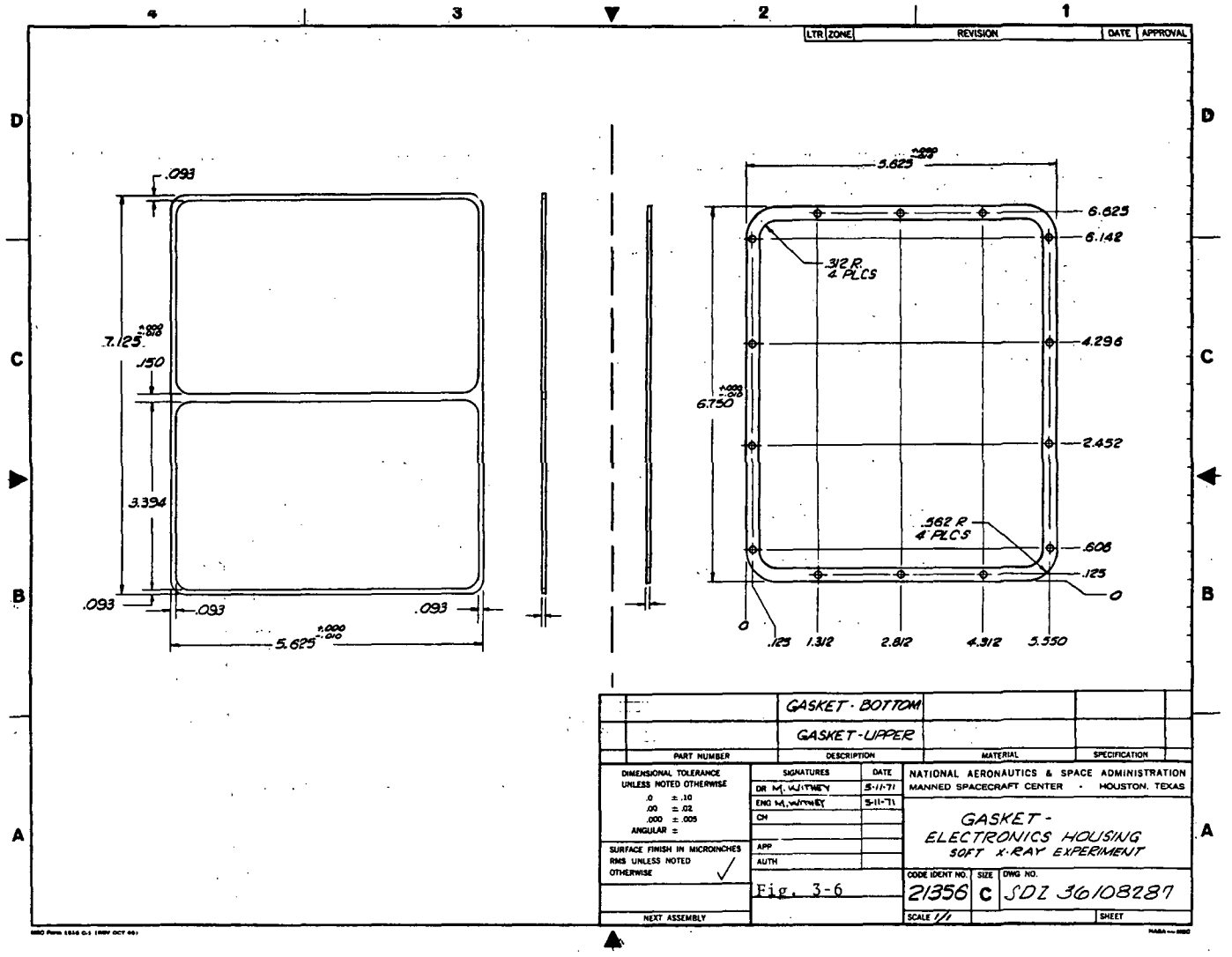


Figure 3-6. — Gasket-Electronic Housing

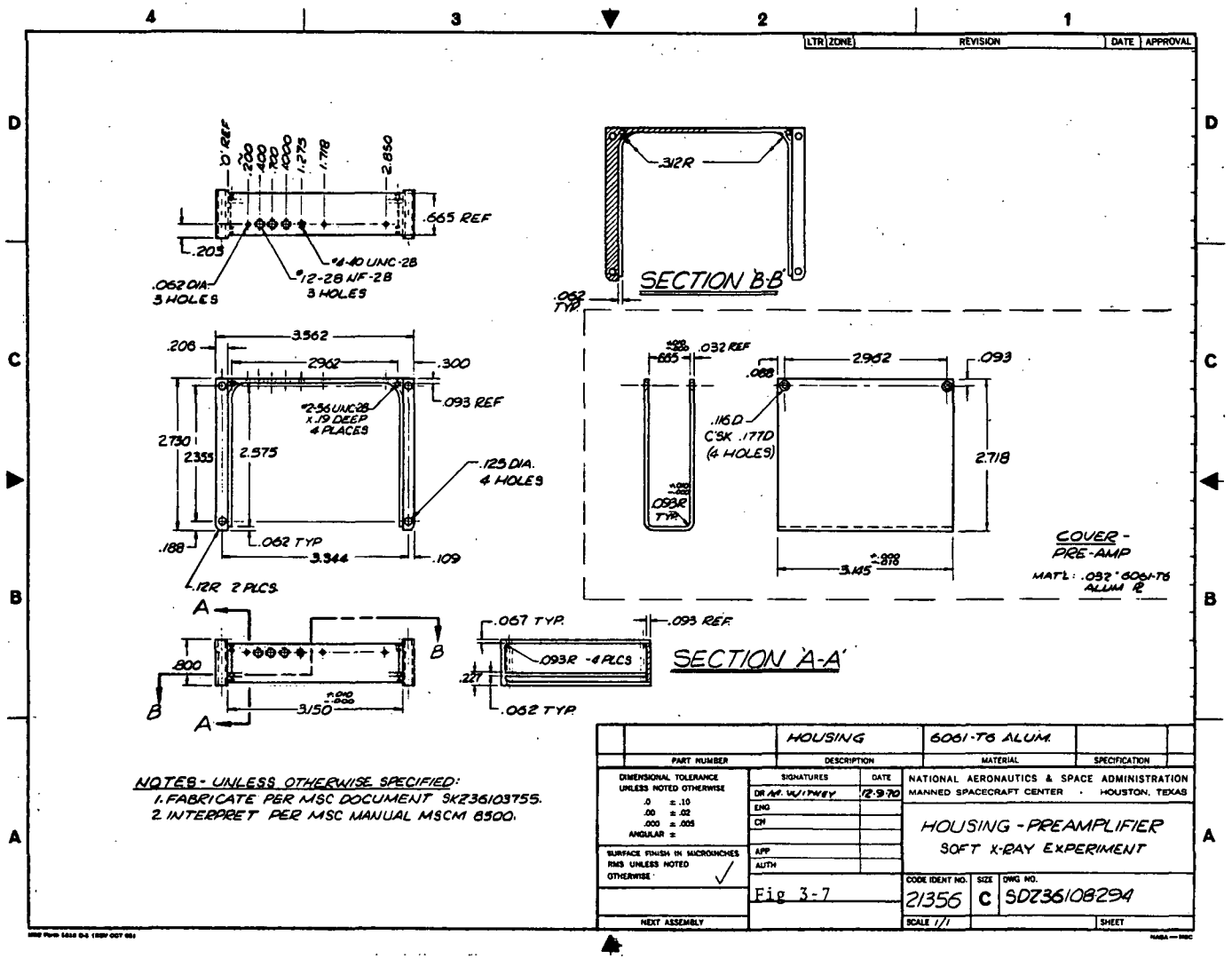


Figure 3-7. — Housing - Preamplifier

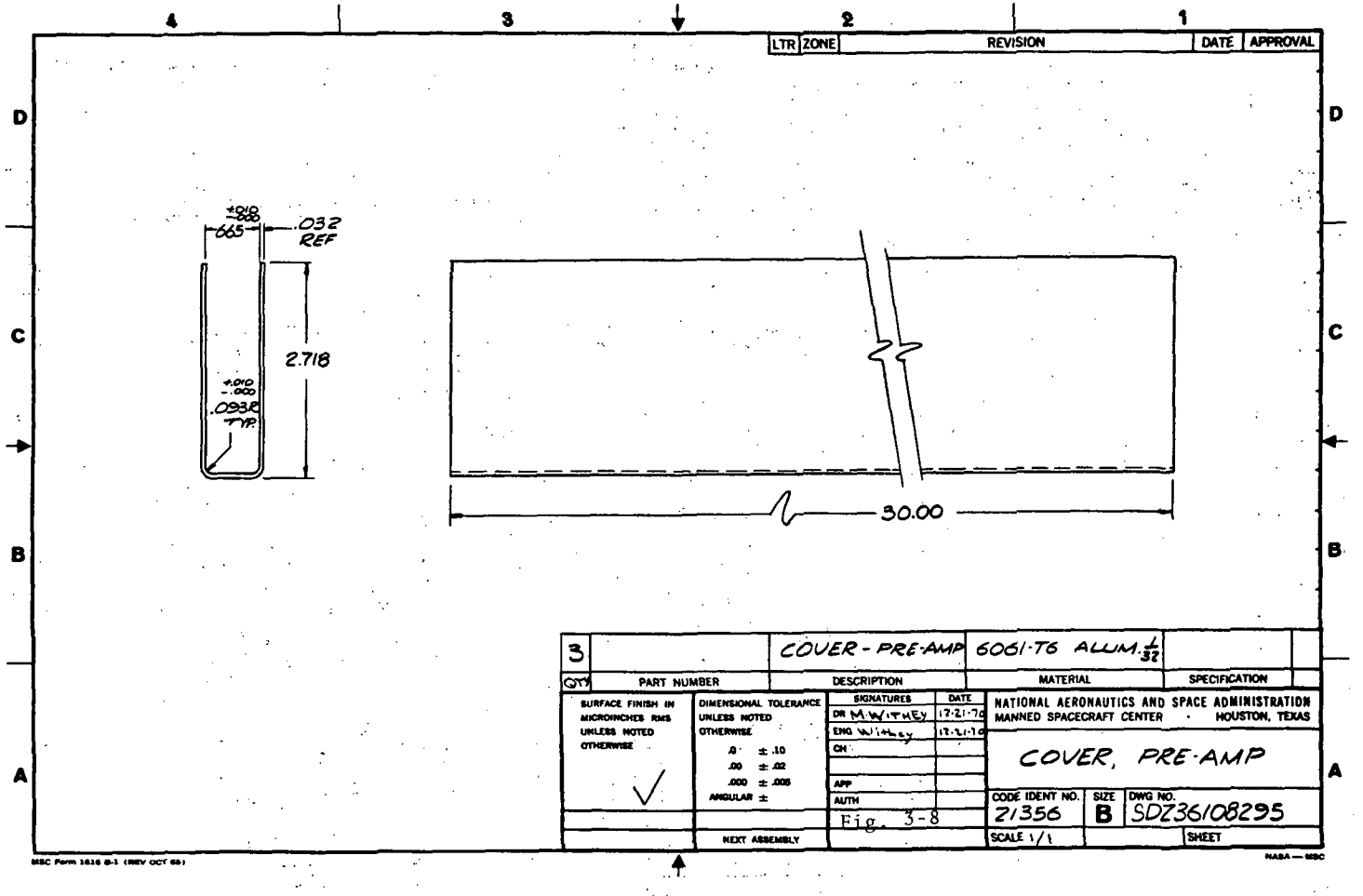


Fig. 3-8

Figure 3-8. — Cover; Pre-Amp

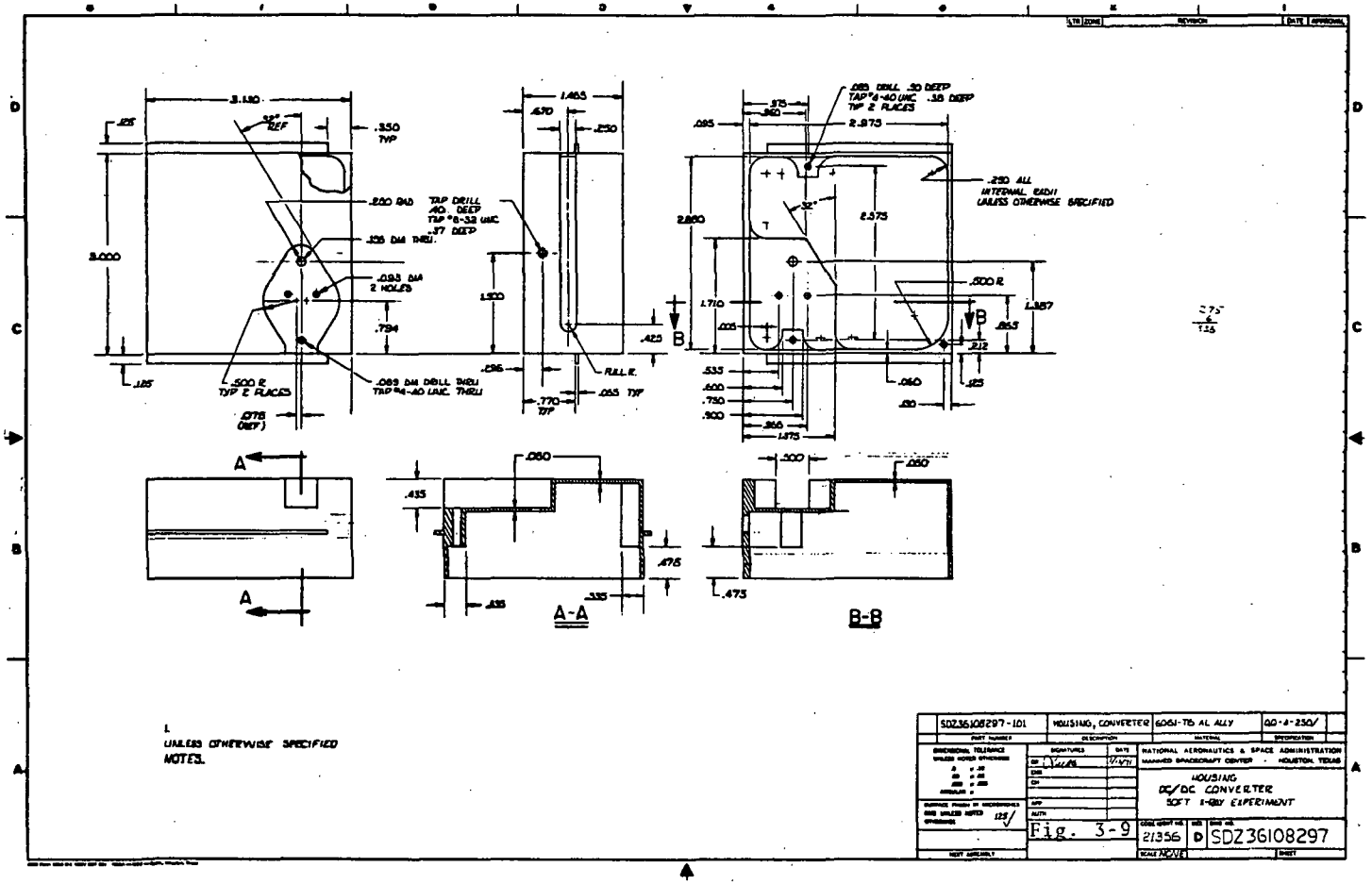


Figure 3-9. — Housing, DC/DC Converter

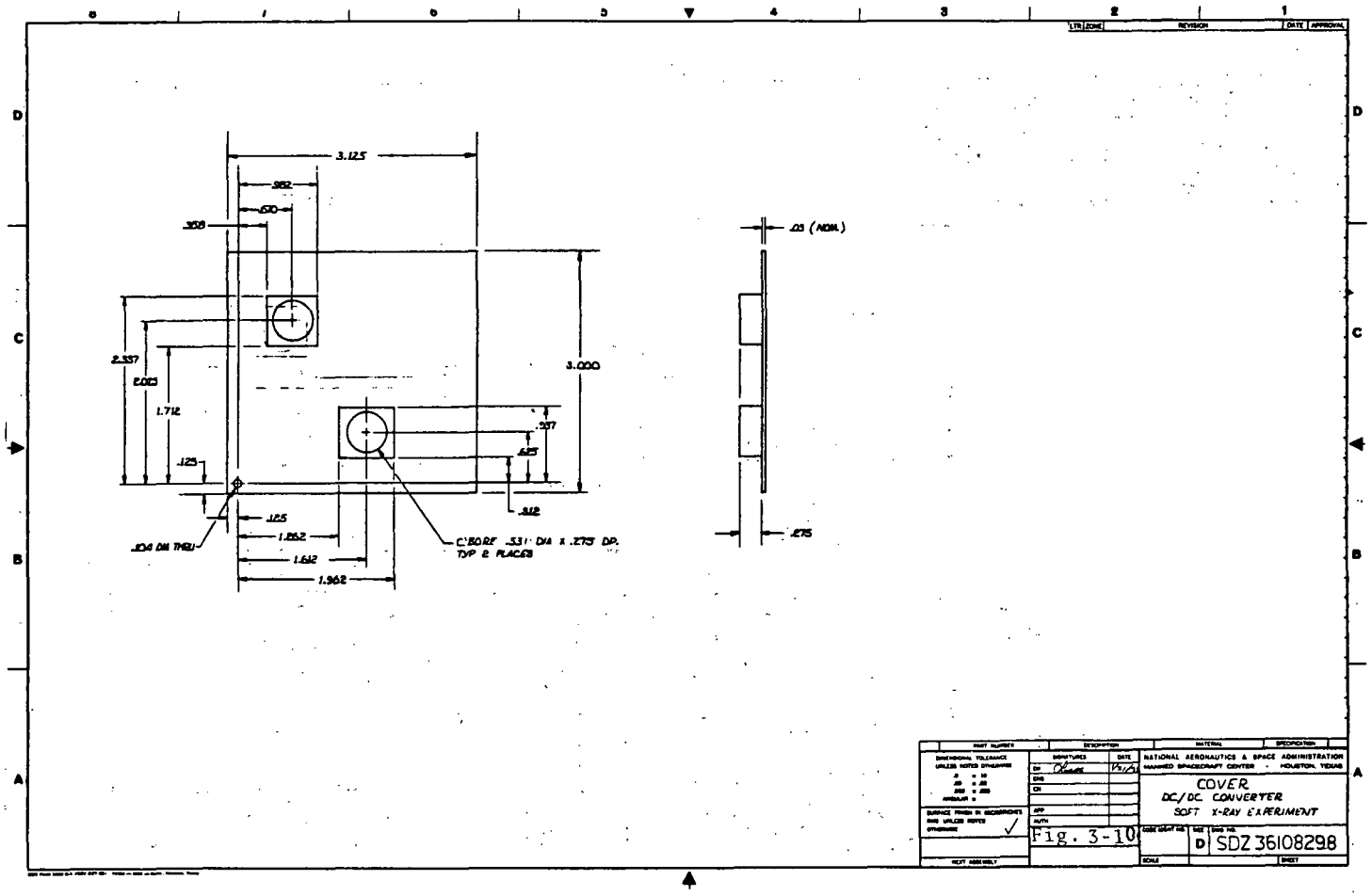


Figure 3-10. — Cover, DC/DC Converter

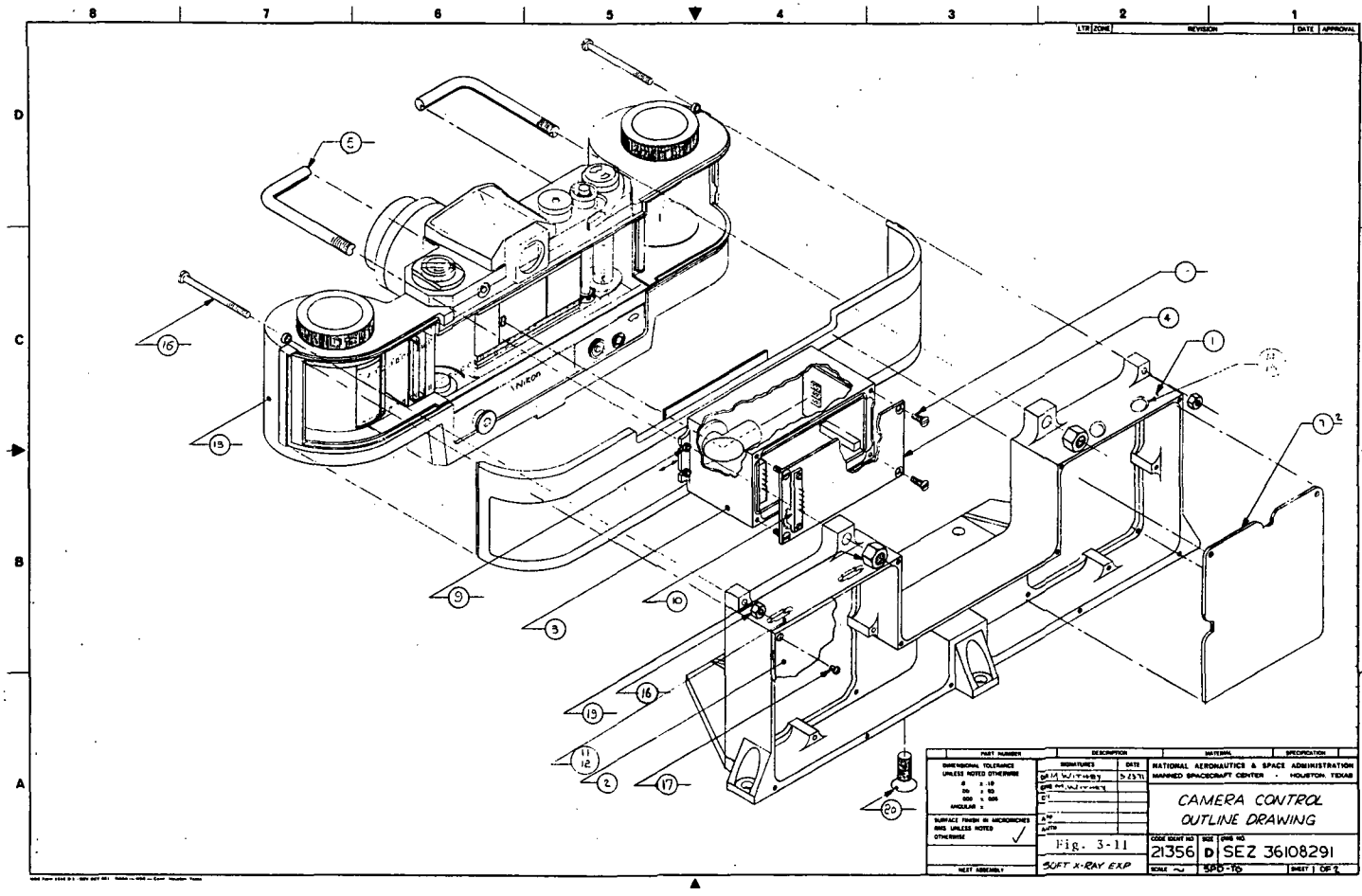
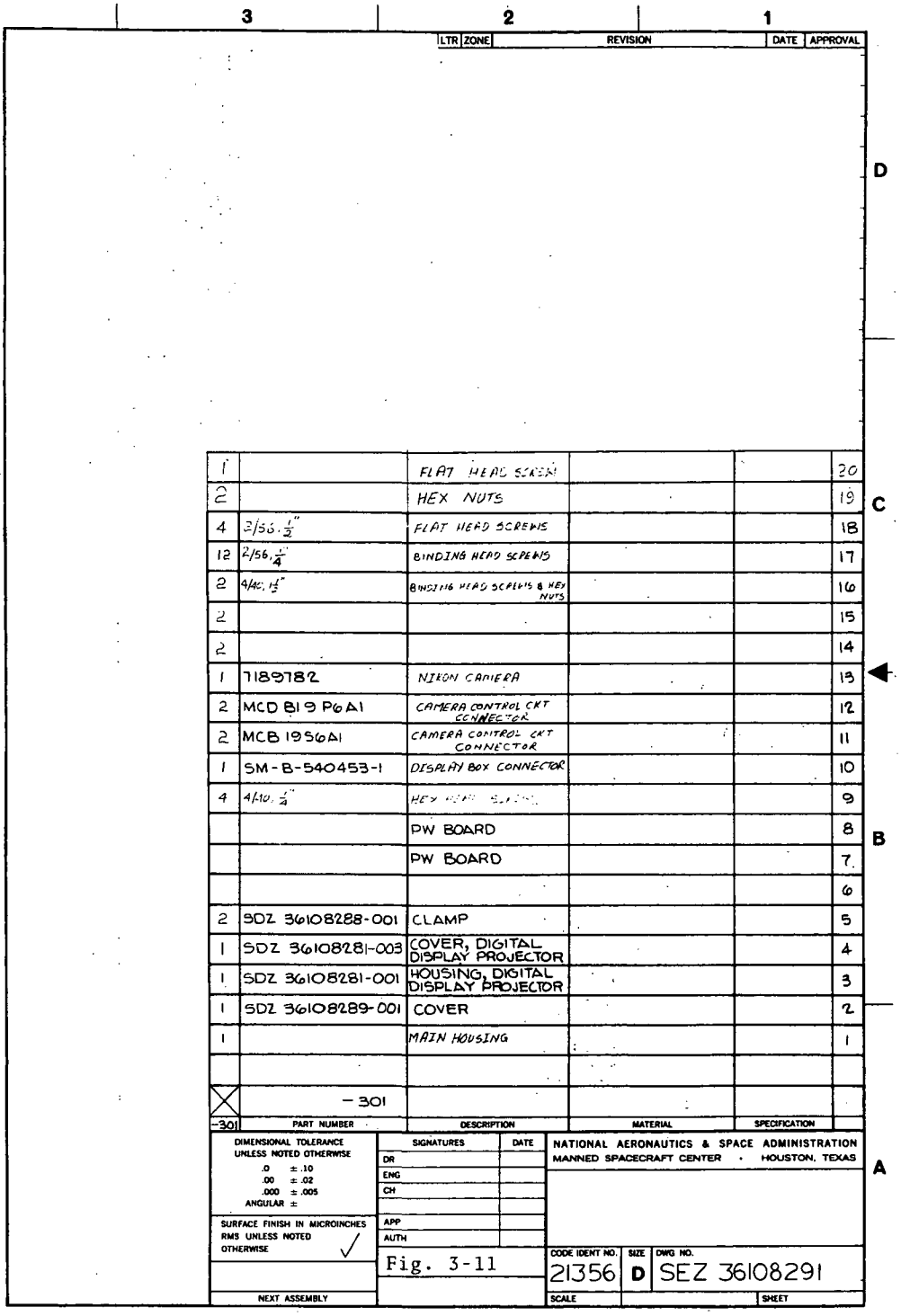


Figure 3-11. – Camera Control Outline Drawing



	3	2	1		
		LTR ZONE REVISION		DATE	APPROVAL
1		FLAT HEAD SCREW			20
2		HEX NUTS			19
4	2/56, 1/2"	FLAT HEAD SCREWS			18
12	2/56, 1/4"	BINDING HEAD SCREWS			17
2	4/40, 1/2"	BINDING HEAD SCREWS & HEX NUTS			16
2					15
2					14
1	7189782	NIKON CAMERA			13
2	MCD 819 P6A1	CAMERA CONTROL CKT CONNECTOR			12
2	MCB 19S6A1	CAMERA CONTROL CKT CONNECTOR			11
1	SM-B-540453-1	DISPLAY BOX CONNECTOR			10
4	4/40, 1/4"	HEX [illegible]			9
		PW BOARD			8
		PW BOARD			7
					6
2	SDZ 36108288-001	CLAMP			5
1	SDZ 36108281-003	COVER, DIGITAL DISPLAY PROJECTOR			4
1	SDZ 36108281-001	HOUSING, DIGITAL DISPLAY PROJECTOR			3
1	SDZ 36108289-001	COVER			2
1		MAIN HOUSING			1
X	-301				
-301	PART NUMBER	DESCRIPTION	MATERIAL	SPECIFICATION	

D C B A

DIMENSIONAL TOLERANCE UNLESS NOTED OTHERWISE
.0 ± .10
.00 ± .02
.000 ± .005
ANGULAR ±

SURFACE FINISH IN MICROINCHES RMS UNLESS NOTED OTHERWISE ✓

NEXT ASSEMBLY

SIGNATURES	DATE
DR	
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Fig. 3-11

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21356	D	SEZ 36108291

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Figure 3-11 (Concluded) Camera Control Outline Drawing

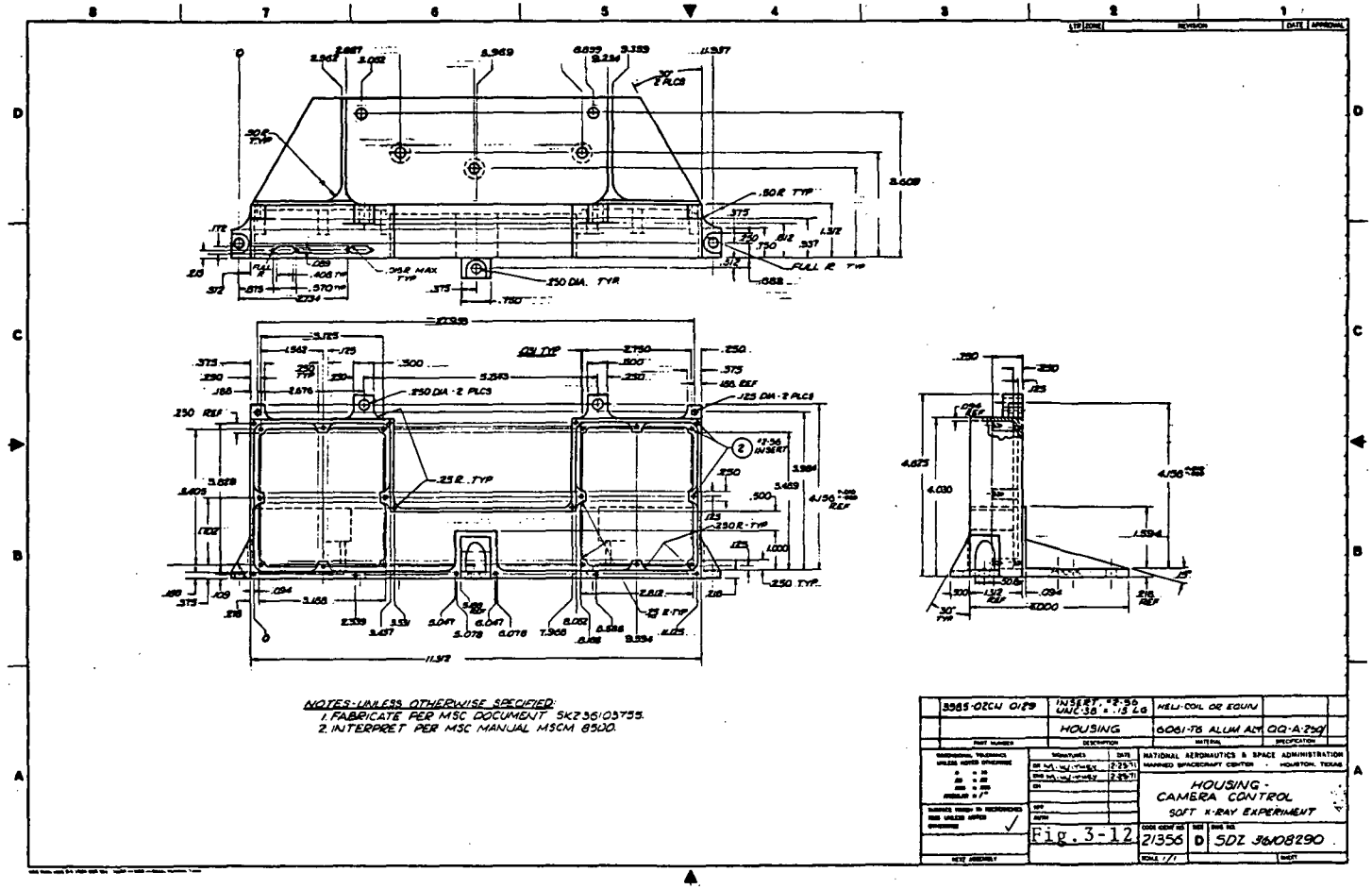


Figure 3-12. — Housing-Camera Control

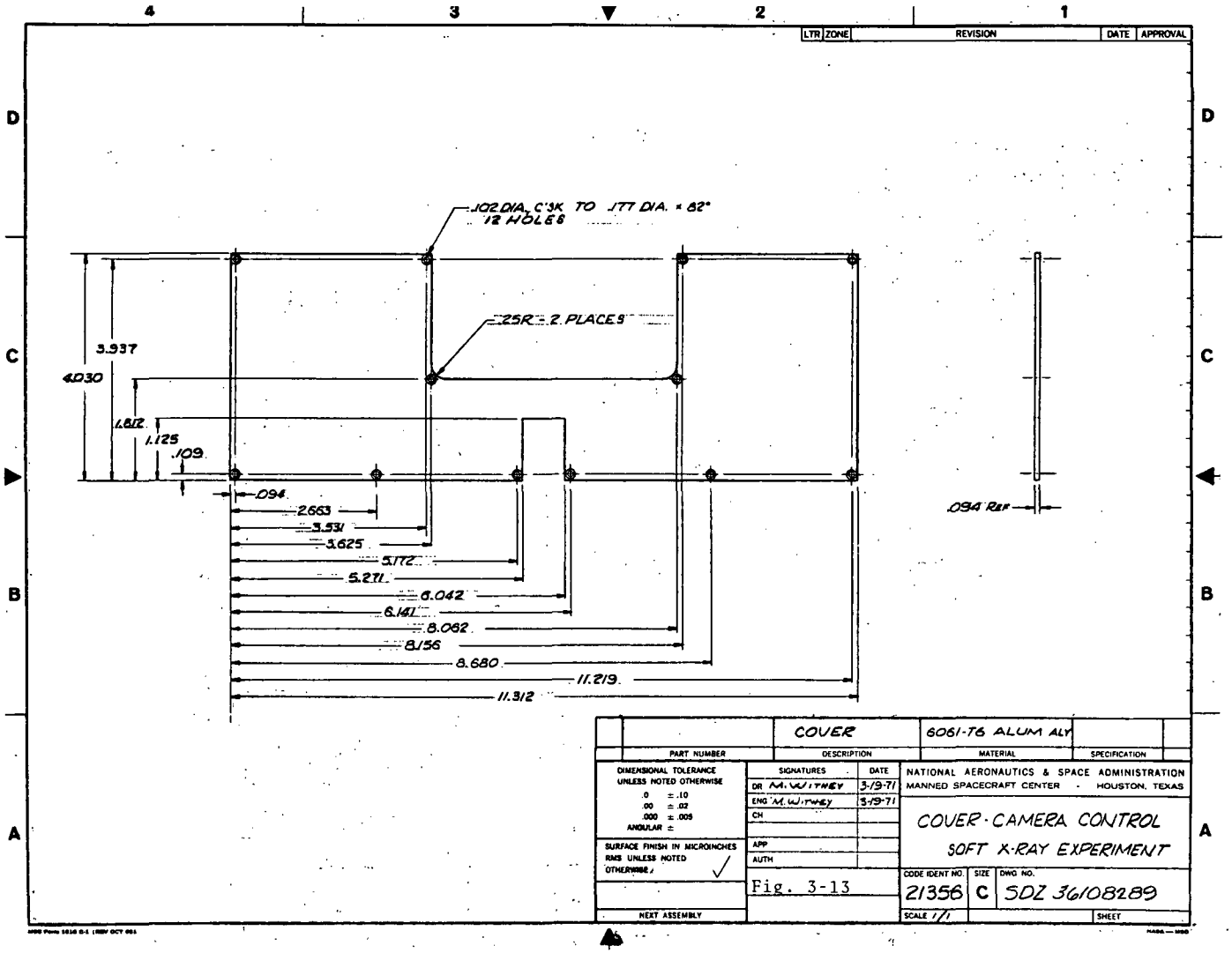


Figure 3-13. — Cover-Camera Control

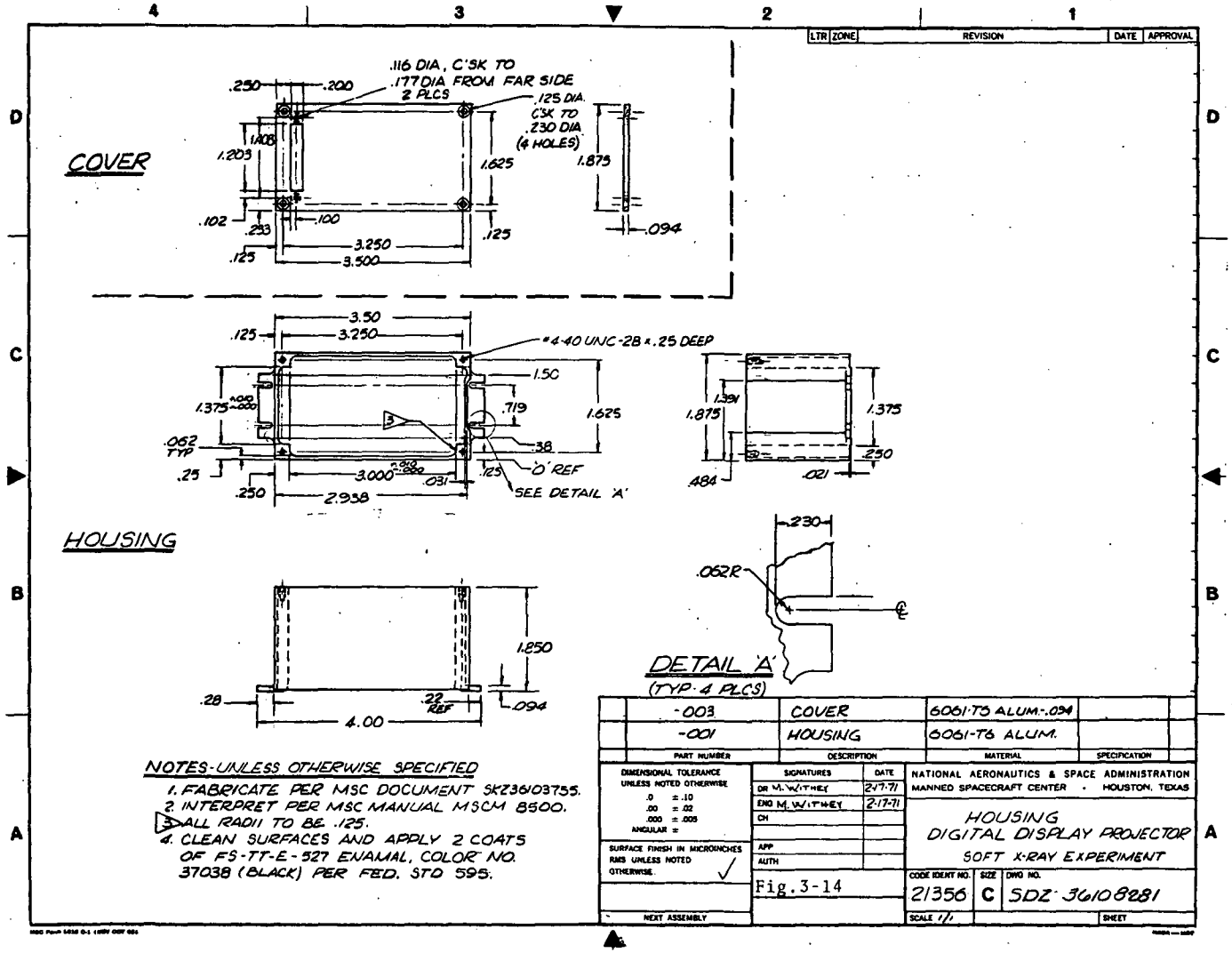


Figure 3-14. — Housing-Digital Display Projector

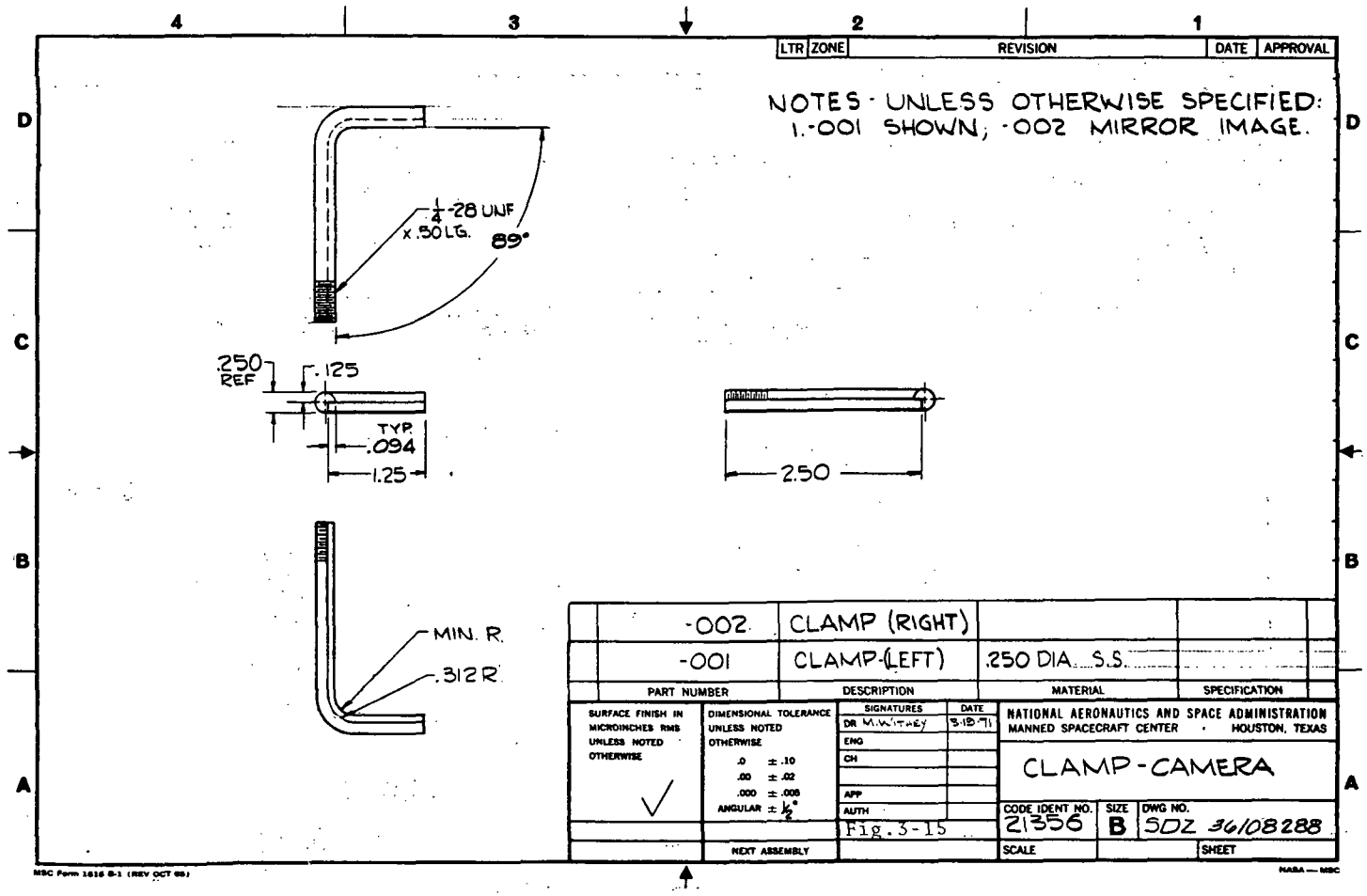


Figure 3-15. — Clamp-Camera

4. PREAMPLIFIERS

There are three preamplifier modules in each electronic housing. Each preamplifier module includes a low noise, high speed, charge sensitive, preamplifier and a high slew rate, post amplifier. The charge sensitive preamplifier's rise time is less than 30 nanoseconds and its noise is less than 7 Kev (referred to silicon). The schematic diagram, the board assembly, and the printed circuit layout are shown in Figures 4-1 through 4-3 respectively. The post amplifier has a slew rate of 1000 volts per microsecond which preserves the 30 nanoseconds pulse rise time at its output.

The signal coming from the preamplifier can be expressed as:

$$e_{PA}(t) = \frac{Q}{C_f} e^{-t/T} \qquad (1)$$

where Q = signal charge at the preamplifiers input

C_f = C17 = 1pf = preamplifier's feedback capacitor

$\tau_f = R_f C_f$ = R21 C17 = $(10^7\ \Omega)(1\text{pf}) = 10^{-5}$ seconds

= preamplifier signal decay time constant and R_f is a high valued resistor connected across C_f.

In the complex frequency domain equation (1) becomes

$$E_{PA}(S) = \frac{Q}{C_1} \frac{1}{\tau_f S + 1} \qquad (2)$$

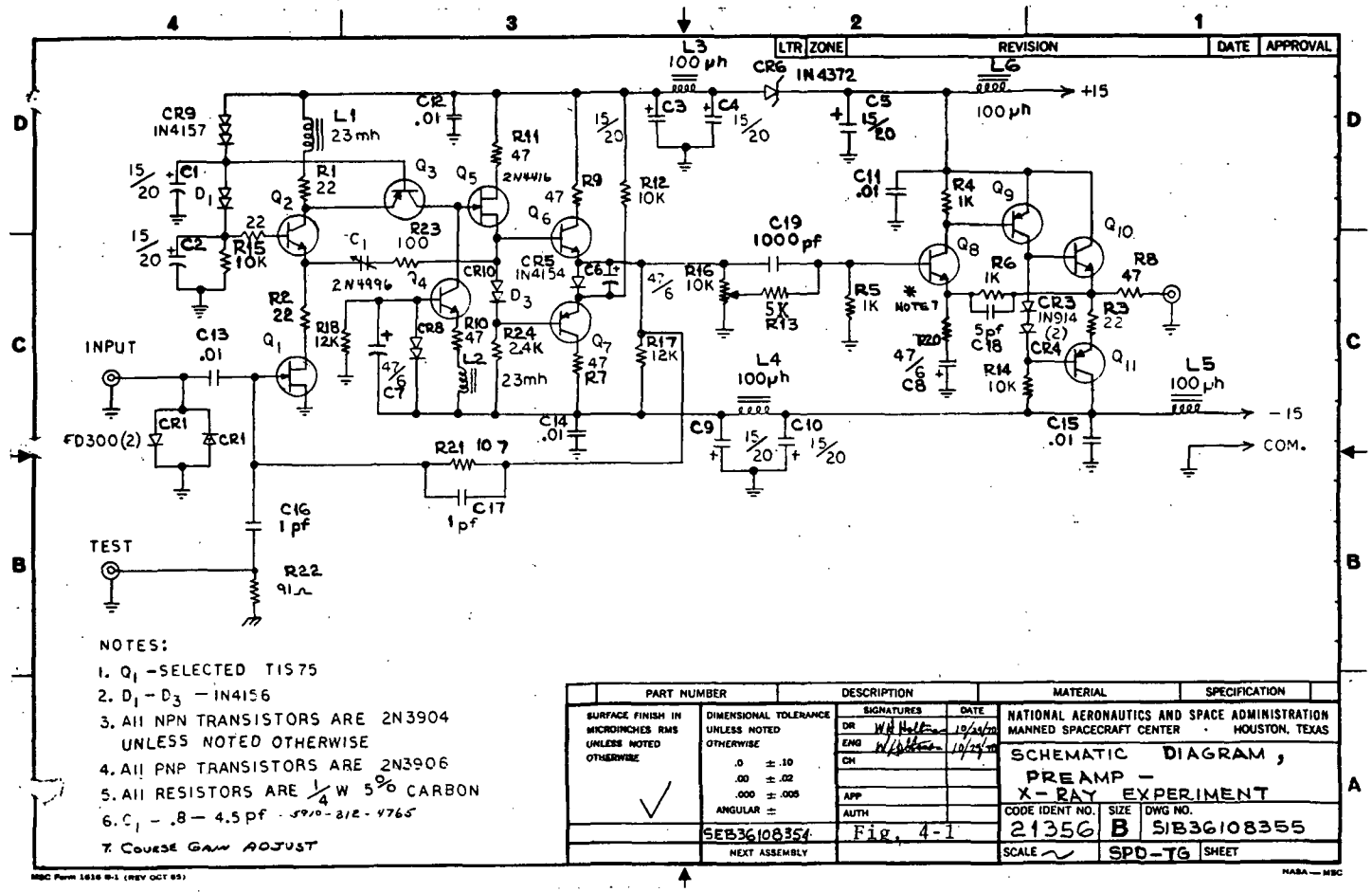


Figure 4-1 Schematic Diagram, Preamp

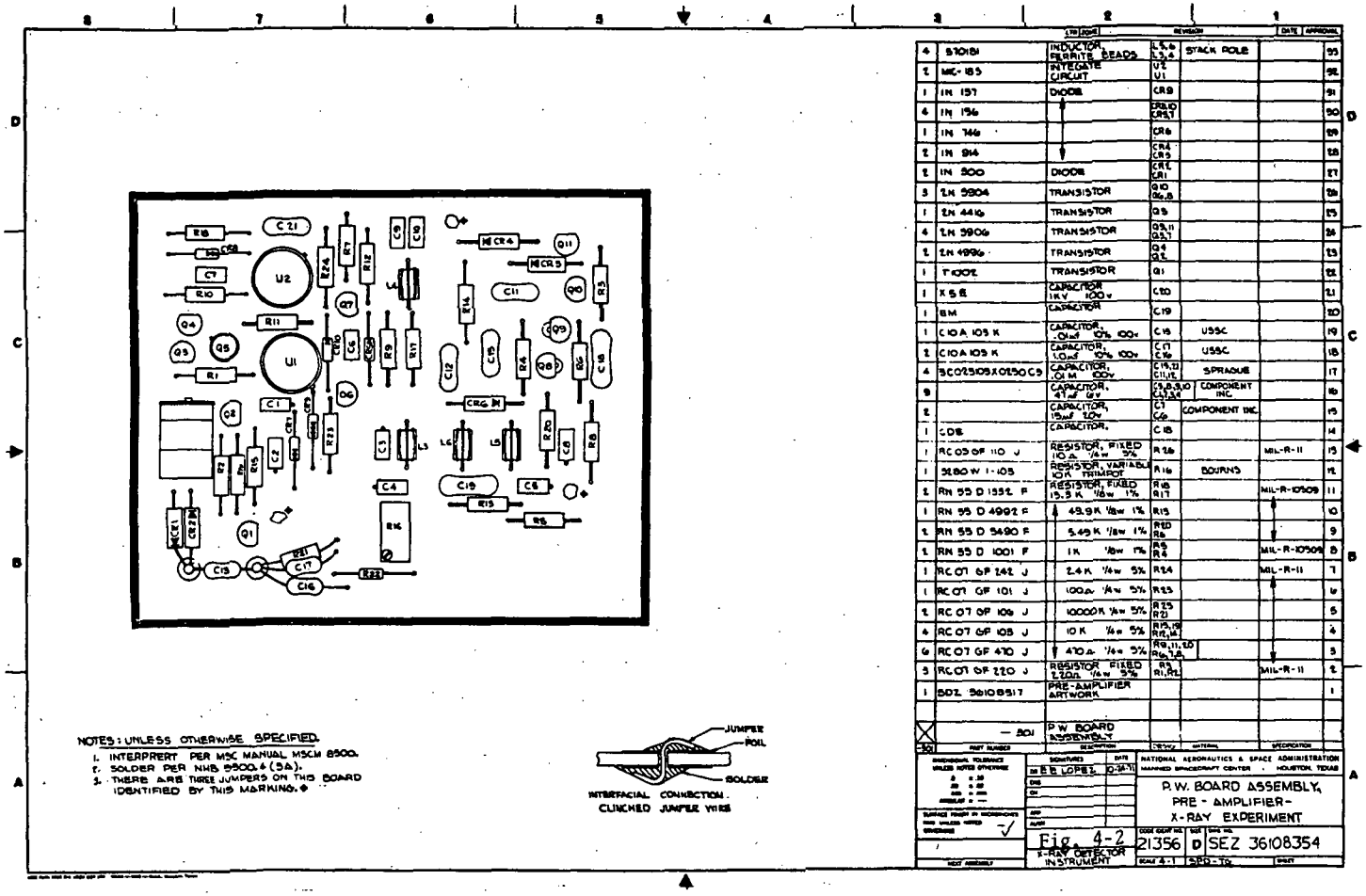


Figure 4-2 PW Board Assembly, Preamplifier

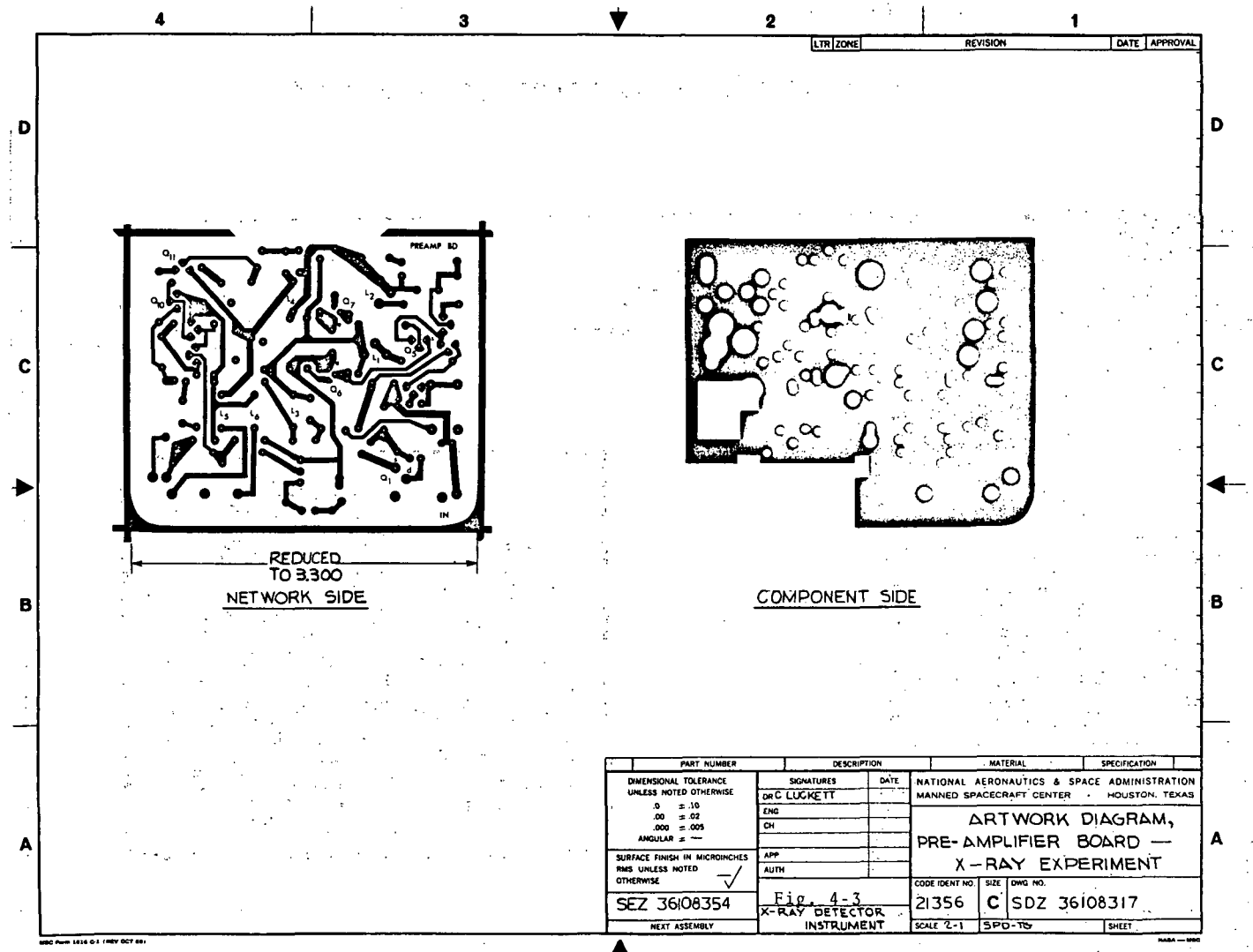


Figure 4-3 Artwork Diagram, Preamplifier Board

It is desirable to reduce the preamplifier signal decay time constant from 10^{-5} seconds to 10^{-6} seconds before it enters the high slew rate amplifier. This is accomplished with a pole-zero concellation network whose transfer function in the complex frequency domain is:

$$Z(S) = \frac{K_1(\tau_z S + 1)}{\tau_p S + 1} \qquad (3)$$

where $K_1 = \frac{R_5}{R_5 + R_{13} + KR_{16}} = \frac{1K\Omega}{1K\Omega + 5K\Omega + 5K\Omega}$

$= 0.091$ = DC gain of the pole zero network, K is the R_{16} potentiometer setting

$\tau_z = (R_{13} + KR_{16})C_{19} = 10^{-5}$ seconds

= time constant of the "zero"

$\tau_p = R_5 C_{19}$ = time constant of the pole

The signal into the amplifier can be expressed by combining equations (2) and (3)

$$E'_{PA} = E_A Z = \frac{Q}{C_f} \frac{1}{(\tau_f S + 1)} \frac{K.(\tau_z S + 1)}{(\tau_p S + 1)}$$

The time constant of the "zero" can be exactly matched to the preamplifiers decay time constant by adjusting potentiometer R_{16} so that the input to the amplifier is

$$E'_{PA} = \frac{Q}{C_f} \frac{K_1}{\tau_p S + 1}$$

The AC gain of the pole-zero network is approximately 0.4 producing a 0.2 volt pulse out of the pole-zero network when the event energy is 10 KeV.

The transfer function of the high slew rate amplifier may be expressed in the complex frequency domain as

$$\frac{e_A}{e'_{PA}} = \frac{K_A S}{(\tau_{1A} S + 1)(\tau_{2A} S + 1)}$$

where $K_A = R_G C_8$

$\tau_{1A} = R_6 C_{18} = 5 \times 10^{-9}$ sec .

$\tau_{2A} = R_{20} C_8 - 5 \times 10^{-3}$ sec to 10×10^{-3} sec .

The pulse gain of the fast amplifier at the leading edge pulse frequency of 30 mHz is approximately

$$\left.\frac{e_A}{e'_{PA}}\right|_{30mHz} \approx \frac{1}{R_{20} C_{18} S} = \frac{1}{(1.2 \times 10^3\ \Omega)(5_{pf})(30\ mHz)} = 5$$

Thus the pulse out of the amplifier is a tail pulse having a rise time of 30 nanoseconds, a fall time of 1 microsecond and an amplitude of 1 volt for a 10 KeV event.

The components of the preamplifier's noise are listed in Table 4-1. The charge sensitive preamplifier has three main stages: (1) a FET (Q_1) for high input impedance, (2) a common base stage (Q_3) for voltage gain, and (3) a complementary follower pair (Q_6 and Q_2) for isolation. Q_2 sets the

Table 4-1 Preamplifier Noise

CAUSE	FORMULA, Coulomb^2	PARAMETER VALUE	NOISE VALUES WITH τ = 1 μsec, gm = 10^{-2} mho								
			FET + PROTECTION = 30pf			PLUS 50 pf det = 80 pf			PLUS 20 pf det = 100 pf		
			Coulomb^2 x 10^{-34}	RMS Electrons	FWHM Kev(S_i)	Coulomb^2 x 10^{-34}	RMS Electrons	FWHM Kev(S_i)	Coulomb^2 x 10^{-34}	RMS Electrons	FWHM Kev(S_i)
VOLTAGE NOISE:											
FET Noise Resistance	$3.7kTRC^2/\tau$	R = Vds(on) = 70Ω	9.50	192	1.63	67.2	513	4.35	105.5	642	5.43
FET Load Resistor	$3.7kTC^2/gm^2RC\tau$	R_i = 2000Ω	0.68	52	0.44	4.8	137	1.16	7.5	171	1.45
Common Bad Shot Noise	$1.85qI_{b2}C^2/qm2_\tau$	I_{b2} =10μa	0.27	32	0.28	1.9	86	0.73	3.0	108	.91
Follower Shot Noise	$1.85qI_{b3}C^2/qm2\tau$	I_{b3} = 10μa	0.27	32	0.28	1.9	86	0.73	3.0	108	.91
			Total Voltage			Total Voltage			Total Voltage		
			10.72	205	1.73	75.8	544	4.61	119.0	1029	8.71
CURRENT NOISE:											
FET Gate Leakage	$1.85qI_g\tau$	I_g = 2na	5.9	152	1.29	5.9	152	1.29	5.9	152	5.9
Feedback Resistor	$3.7kT\tau/R_f$	R_f = 10M	15	242	2.05	15	242	2.05	15	242	2.05
HV Bias Resistor	$3.7kT\tau R_b$	R_b = 100M	1.5	77	0.65	1.5	77	0.65	1.5	77	0.65
Protection Diodes	$3.7qI_o\tau$	I_o = 1MA	5.9	152	1.29	5.9	152	1.29	5.9	152	1.29
			Total Current			Total Current			Total Current		
			28.3	623	5.28	28.3	623	5.28	28.3	623	5.28

Constants

q = electron charge = 1.6×10^{-19} $\frac{\text{Coulombs}}{\text{electron}}$

k = boltzmans constant = 1.38042×10^{-23} $\frac{\text{watt sec}}{{}^\circ k}$

T = °k = 300°K (nominal)

$$\text{RMS Electrons} = \frac{\sqrt{\text{coulombs}^2}}{q}$$

$$\text{FWHM Kev}(S_i) = \text{RMS Electrons} \times \frac{3.6\text{ev}}{\text{electron}} \times \frac{2.35\ \text{FWHM}}{\text{RMS}} = 8.46\ \frac{\text{ev FWHM}}{\text{electronRMS}} \times \frac{\text{RMS}}{\text{Electrons}}$$

current bias for FET, $Q_1$1. Q_4 provides a current sink load for Q_3 . FET Q_5 is a source follower providing a high impedance load for the common base stage.

The amplifier section has two common collector stages (Q_8 and Q_9) for gain and a complementary follower pair (Q_{10} and Q_{11}) . R_{19}, C_{19}, R_{18}, C_{18} form the negative feedback impedance network which determines the amplifiers gain.

Diodes CR1 and CR2 provide 3000 V short circuit protection at the preamplifiers input. Capacitor C_1 and resistor R_{23} form a positive feedback speed-up network. T_1 and T_2 are peaking coils.

Capacitors C_{13} and C_{16} respectively, AC couple the detector and test inputs into the preamp. Resistor R_8 provides output short circuit protection. CR_6 is a 3V zener diode which level shifts the +15V supply voltage to +12 volts. Inductors L_3, L_4, L_5 and L_6 , capacitors C_1, C_2, C_3, C_4, C_5, C_6, C_7, C_9, C_{10}, C_{11}, C_{12}, C_{14}, C_{15} and C_{18} , are filter elements. Diodes CR5, CR6, CR7, CR8 and CR9; Resistors R_1, R_2, R_3, R_4, R_7, R_9, R_{10}, R_{11}, R_{12}, R_{13}, R_{14}, R_{15}, R_{17}, R_{18}, and R_{19} are bias elements.

5.0 MAIN AMPLIFIER

The main amplifier includes two Ortec-type active filter amplifiers which shape the tail pulses from the two main preamplifiers into semigaussian pulses having a one microsecond time constant. The semigaussian pulses are then summed.

The main amplifier schematic is shown in Figure 5-1. The board assembly is shown in Figure 5-2. The printed circuit layout is shown in Figure 5-3.

The active filter section is shown in Figure 5-4.

For K=2, the transfer function becomes

$$\frac{e_{out}}{e_{in}} = \frac{\frac{K}{R^2C^2}}{S^2 + \frac{2S}{RC} + \frac{K}{R^2C^2}} = \frac{\frac{2}{R^2C^2}}{S^2 + \frac{2S}{RC} + \frac{2}{S^2C^2}}$$

$$= \frac{\frac{2}{R^2C^2}}{\left(S + \frac{1+j}{RC}\right)\left(S + \frac{1-j}{RC}\right)}$$

For a given resolving time (RC), the time response of the filter network depends only on K. In this case, the complex roots cause an underdamped effect which reduces the resolving time and results in a more symmetrical pulse shape.

A one microsecond time constant was chosen as a compromise between a larger signal to noise ratio and pulse pile up.

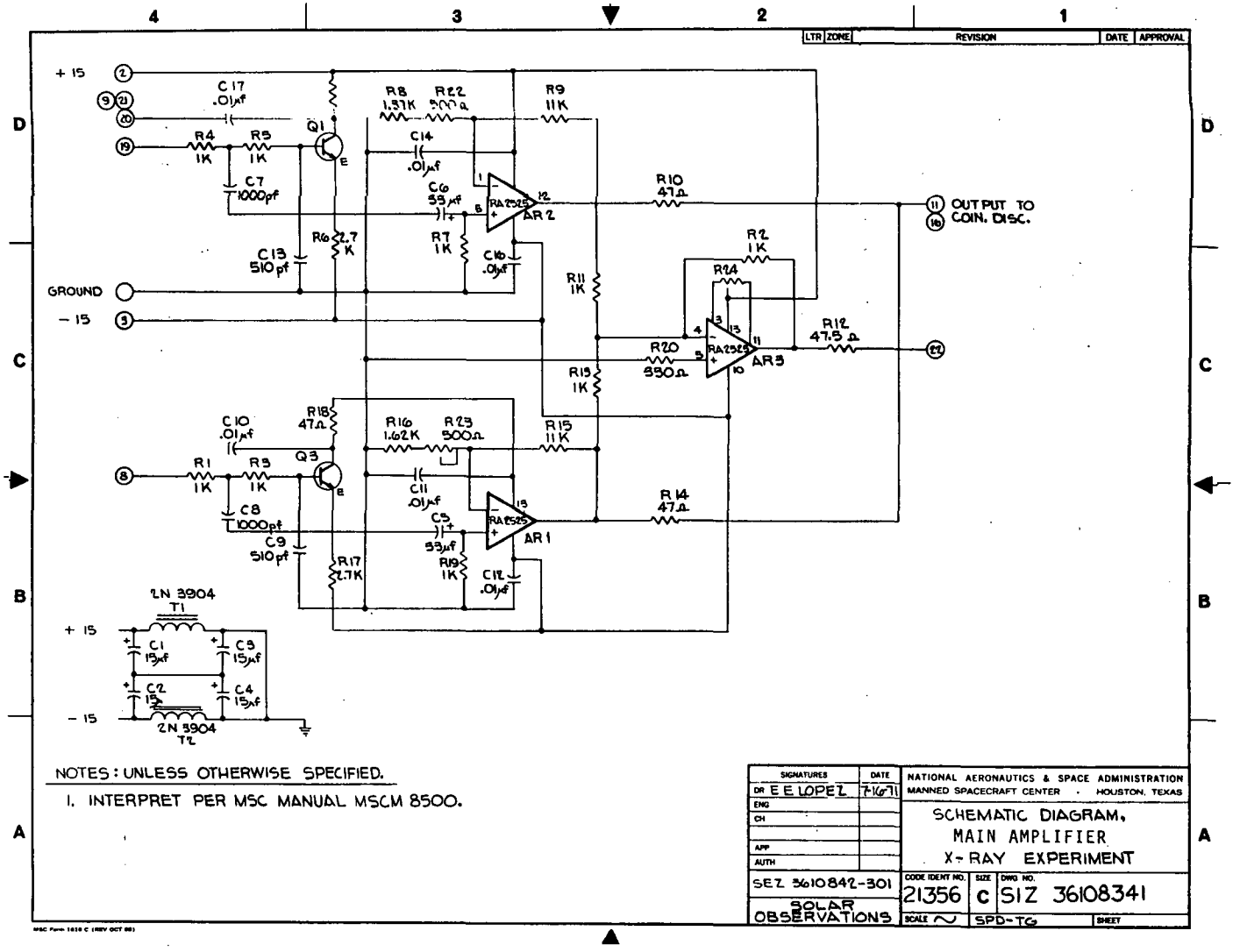


Figure 5-1. — Schematic Diagram, Main Amplifier

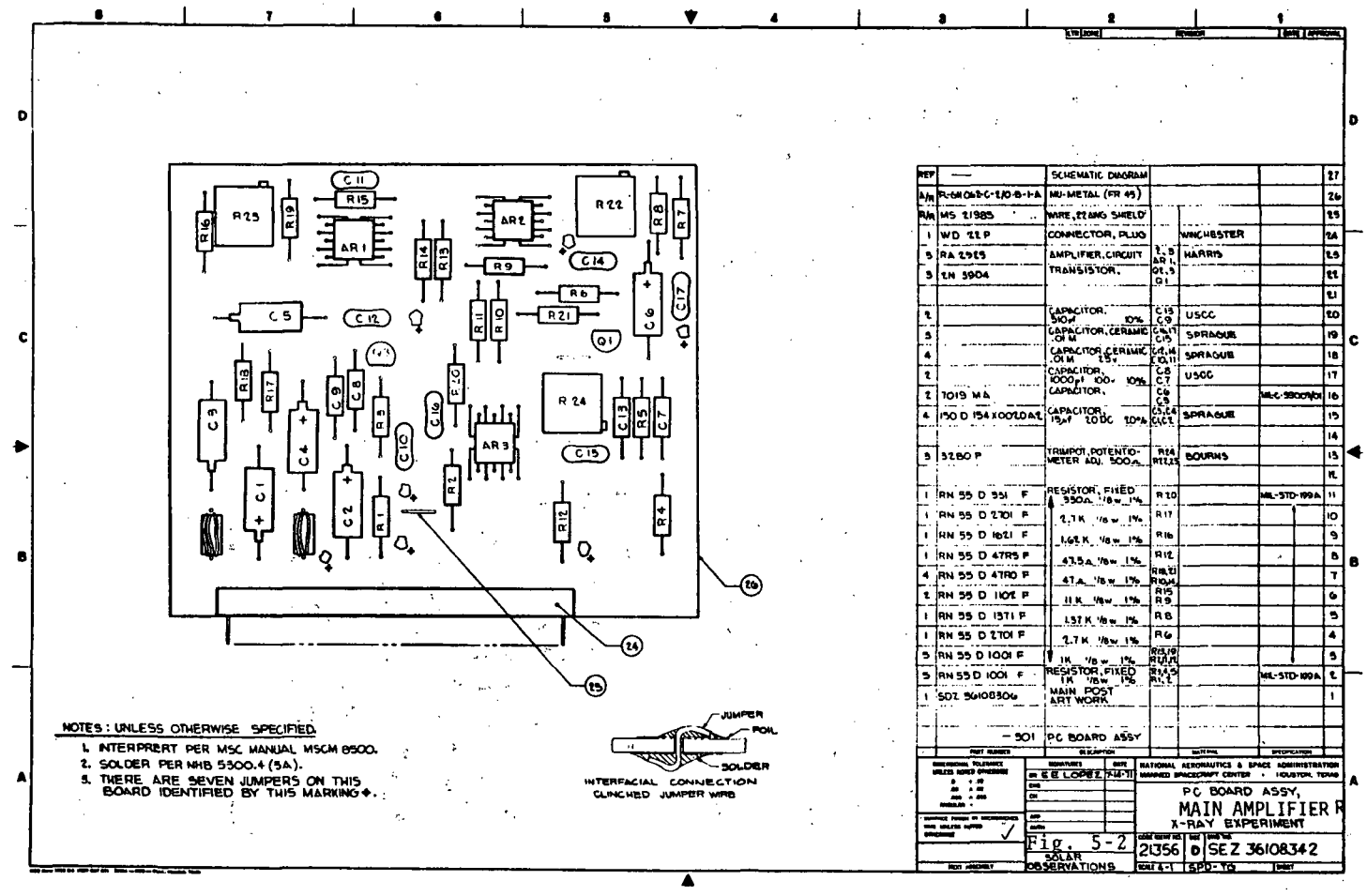


Figure 5-2. — PC Board Assembly, Main Amplifier

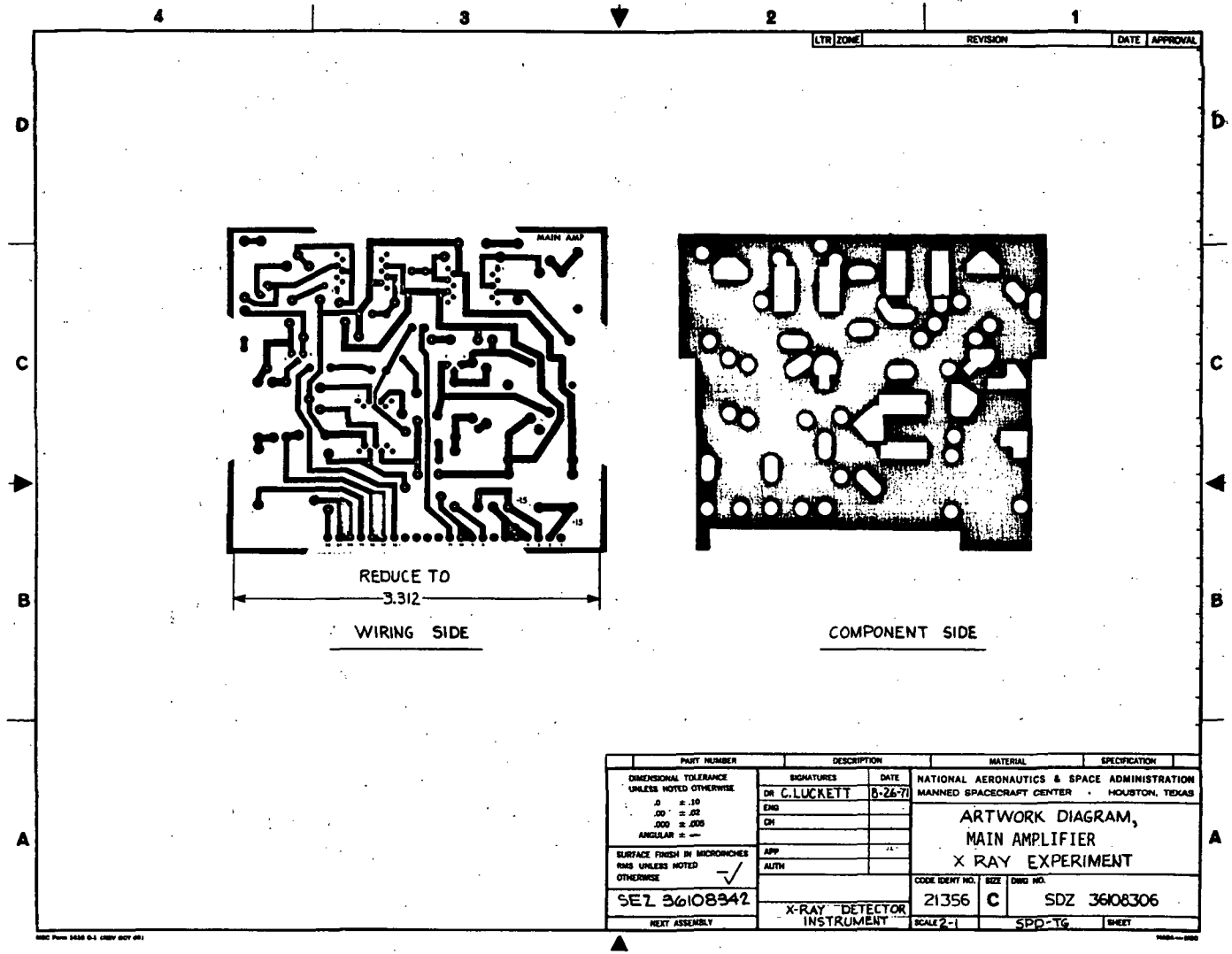


Figure 5-3. — Artwork Diagram, Main Amplifier

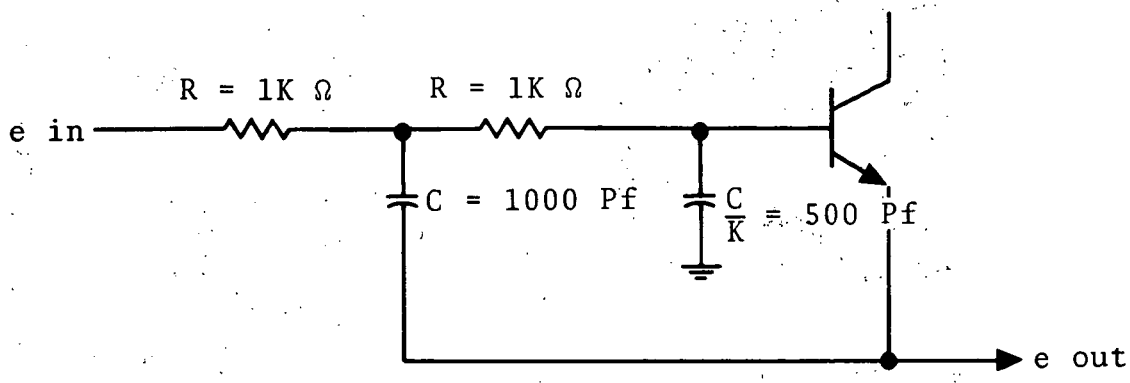


Figure 5-4. Main Amplifier Filter Section.

6. LINEAR GATE – PULSE STRETCHER

The Linear Gate-Pulse Stretcher is a high-speed, low-distortion, switch and peak detector. The circuit adds less than five millivolts of error to a one microsecond pulse 25 millivolts high. It accepts the first pulse in an interrogate interval and stretches its peak value for 40 microseconds to allow an Analog-to-Digital conversion.

The schematic diagram board assembly, and printed circuit layout are shown in Figures 6-1, 6-2, and 6-3 respectively.

The input pulses from the main amplifier are AC coupled through capacitor C2, delayed for 100 nanoseconds by delay line L1 to allow time for the gate to open, and inverted by amplifier A1.

The gate consists of Field Effect Transistors (FET) Q_1 and Q_2, which have no effect on the pulses when the gate is open but short them to ground when the gate is closed. The use of two FET's instead of one increases the pulse attenuation when the gate is off from 95 percent to 99 percent. The gate's speed is 50 microseconds. The gate's driver circuit consists of transistors Q_3 and Q_4, resistors R18, R22, R23, R33 and R34, and capacitor C14.

The accuracy of high-speed, low-pulse-level, linear gates is limited by the electron charge coupled across the FET's gate-to-source junction, which adds to the pulse height. To compensate for this, a charge cancellation circuit is employed consisting of capacitor C5 and resistor R_3 driven by the inverse of the linear gate command pulse.

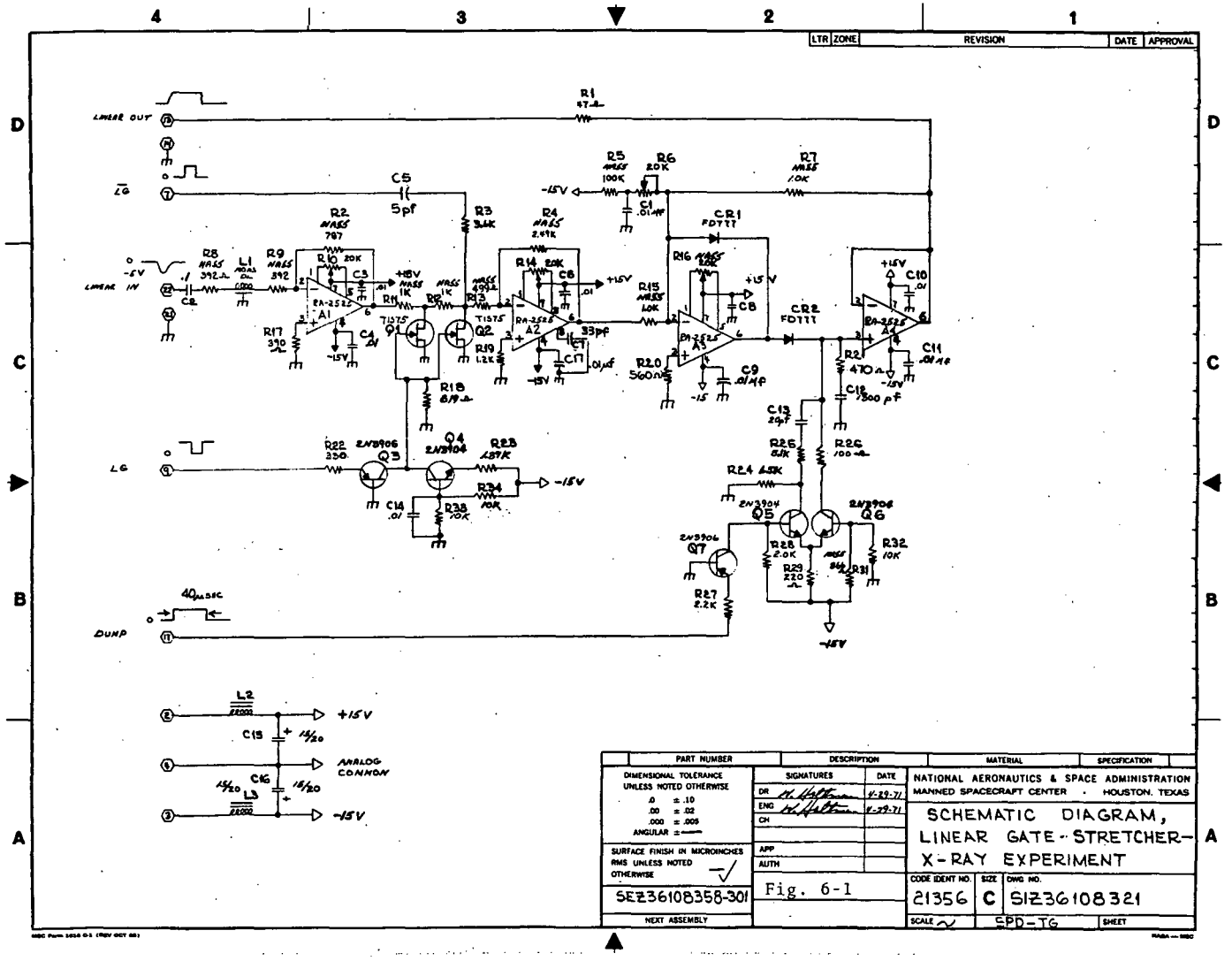


Figure 6-1. — Schematic Diagram, Linear Gate-Stretcher

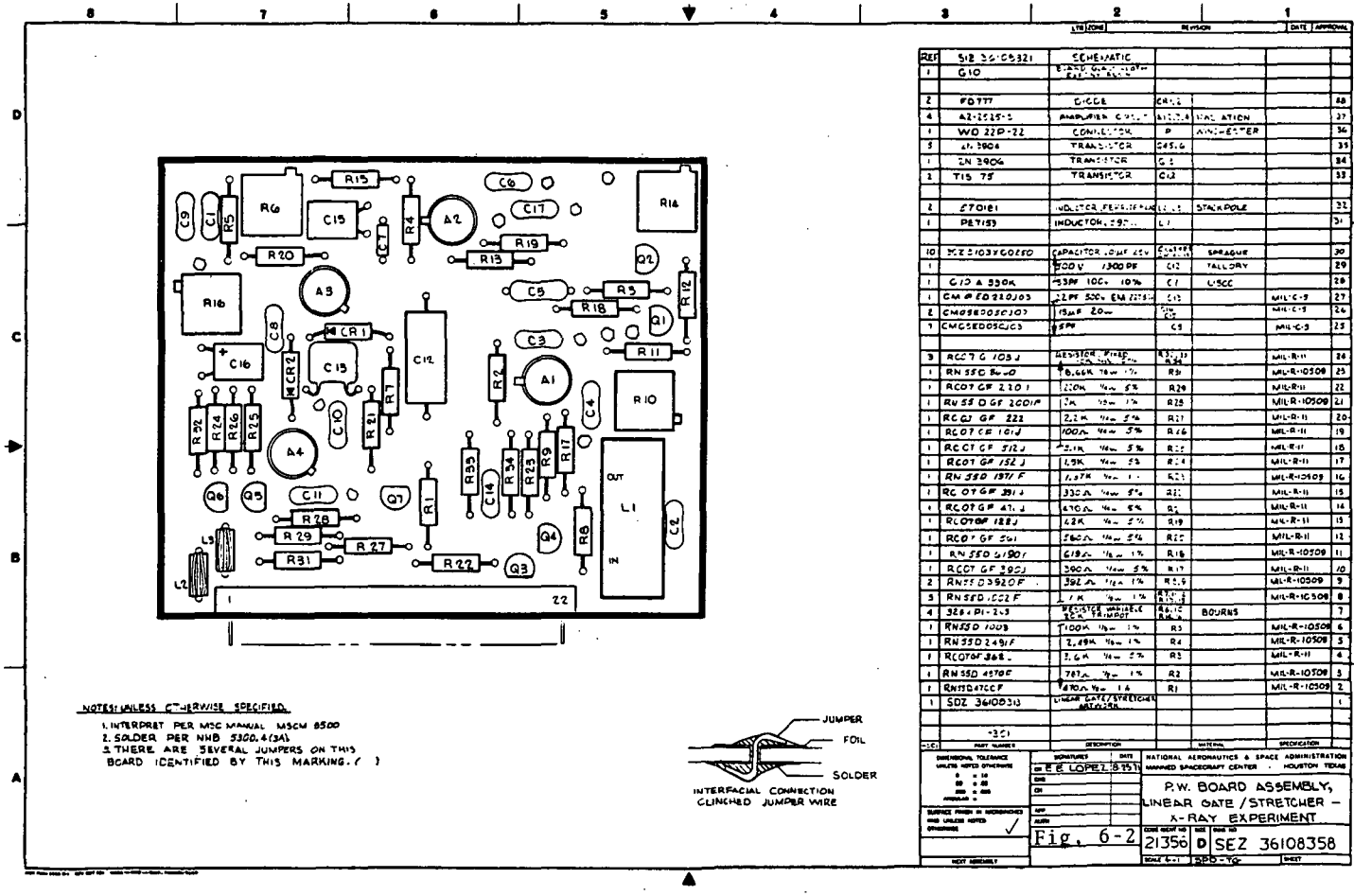


Figure 6-2 — Board Assembly, Linear Gate-Stretcher

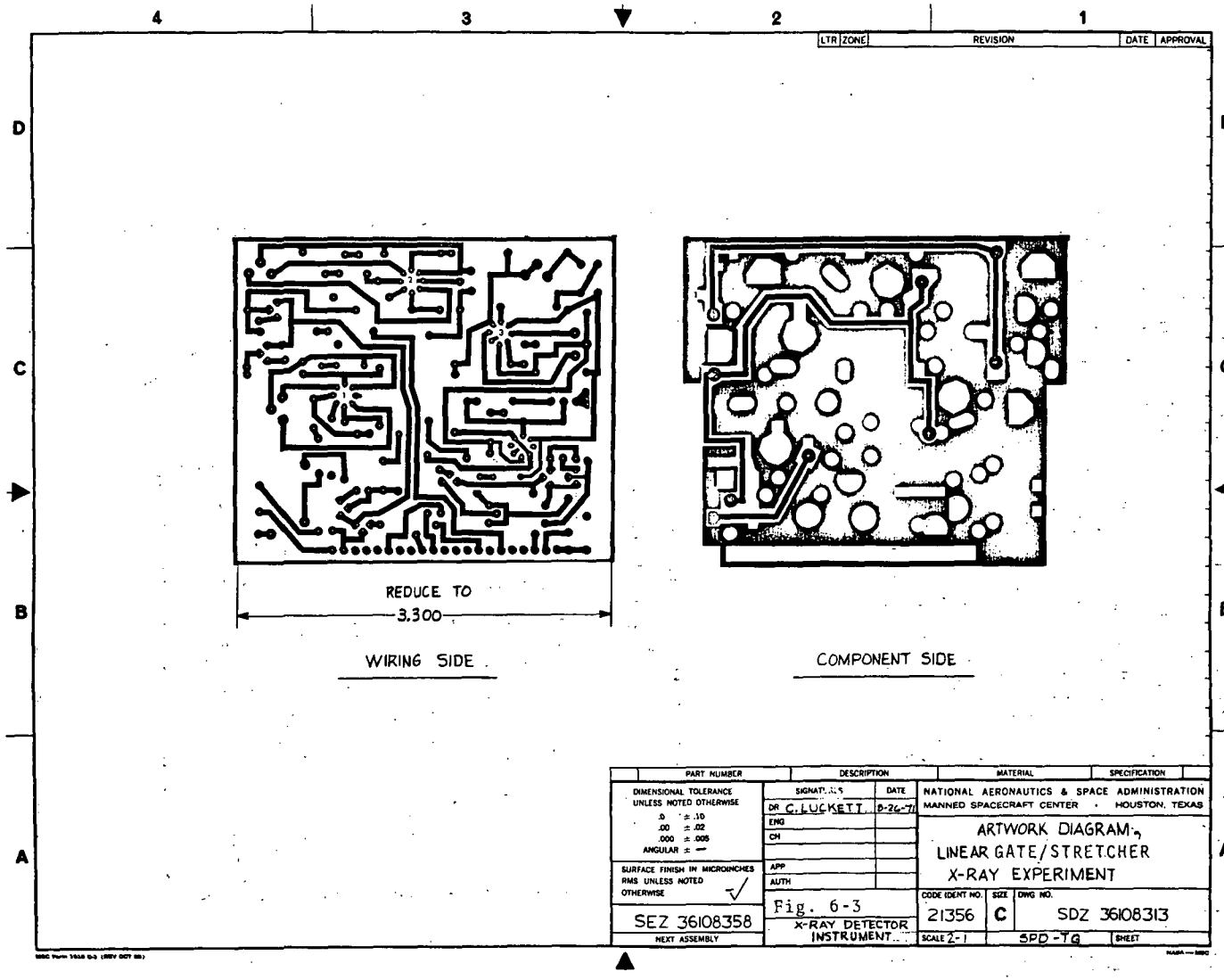


Figure 6-3. — Artwork Diagram, Linear Gate-Stretcher

The main elements of the peak detector are rectifier diode CR2 and holding capacitor C12. These elements are included in the closed loop of the unity gain operational amplifier A3, compensating for the voltage drop across diode CR2. Amplifier 44 is a buffer reducing pulse "droop" during the A-to-D conversion. Diode CR1 reduces the charge coupled across diode CR2 by clamping the output of amplifier A3 to zero volts instead of allowing it to swing to a minus fifteen volts when the pulse slope becomes negative.

A constant-current dump circuit, consisting of transistors Q_5, Q_6 and Q_7, and resistors R24, R26, R27, R28, R29, R31, and R32, discharge the holding capacitor after the conversion is complete. A charge cancellation circuit, consisting of capacitor C13 and resistor R25, is included.

7. PULSE HEIGHT ANLAYZER CONTROL

The Pulse Height Analyzer (PHA) Control circuits accepts semigaussian pulses from both the main and AGC amplifiers. It then generates the linear gate, the charge cancellation, the dump commands for the linear gate-stretcher circuit, the START CONVERSION command for the Analog-to-Digital Converter, the "busy" signal for the telemetry interface circuits, and the OK-TO-DISCRIMINATE command to the rise-time and coincidence discriminators.

It also includes a single-pole, double-throw switch which routes the pulses from the Anticoincidence Amplifier to the Pulse Height Analyzer upon receipt of an AGC control command.

The schematic diagram, board assembly, printed circuit layout, and the timing diagram are shown in Figures 7-1, 7-2, 7-3, and 7-4 respectively.

The low level discriminator (AR1) is set at 25 mv (50 ev). All signals below this level are considered noise. When a pulse is received above 25 mv it sets the busy flip-flop (Z_1), triggers the DUMP command one-shot (Z_4), and generates an OK-TO-DISCRIMINATE command to the rise-time and coincidence discriminators. The busy flip-flop (Z_1) generates the BUSY command to the telemetry interface and triggers the linear gate one-shot, (Z_2). The linear gate one-shot (Z_1) generates the linear gate commands (LG and $\overline{\text{LG}}$) and triggers the start convert one-shot (Z_3). FET's Q3 and Q4 form a single-pole, double-throw switch which routes the AGC amplifier pulses to the Pulse Height Analyzer when an AGC CONTROL command is logic "1", and similarly routes the main amplifier pulses when the command logic is "0".

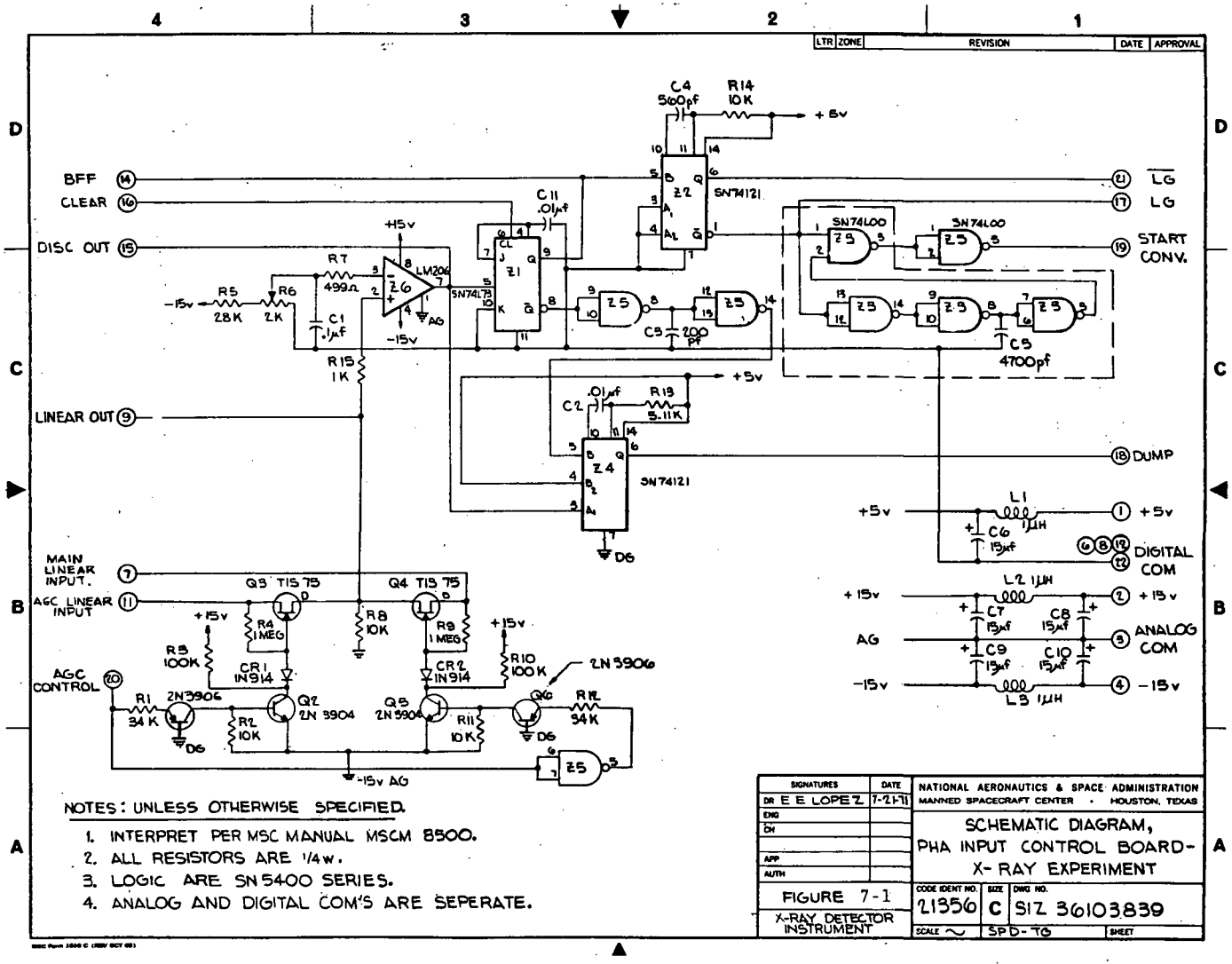


Figure 7-1 Schematic Diagram, PHA Input Control Board

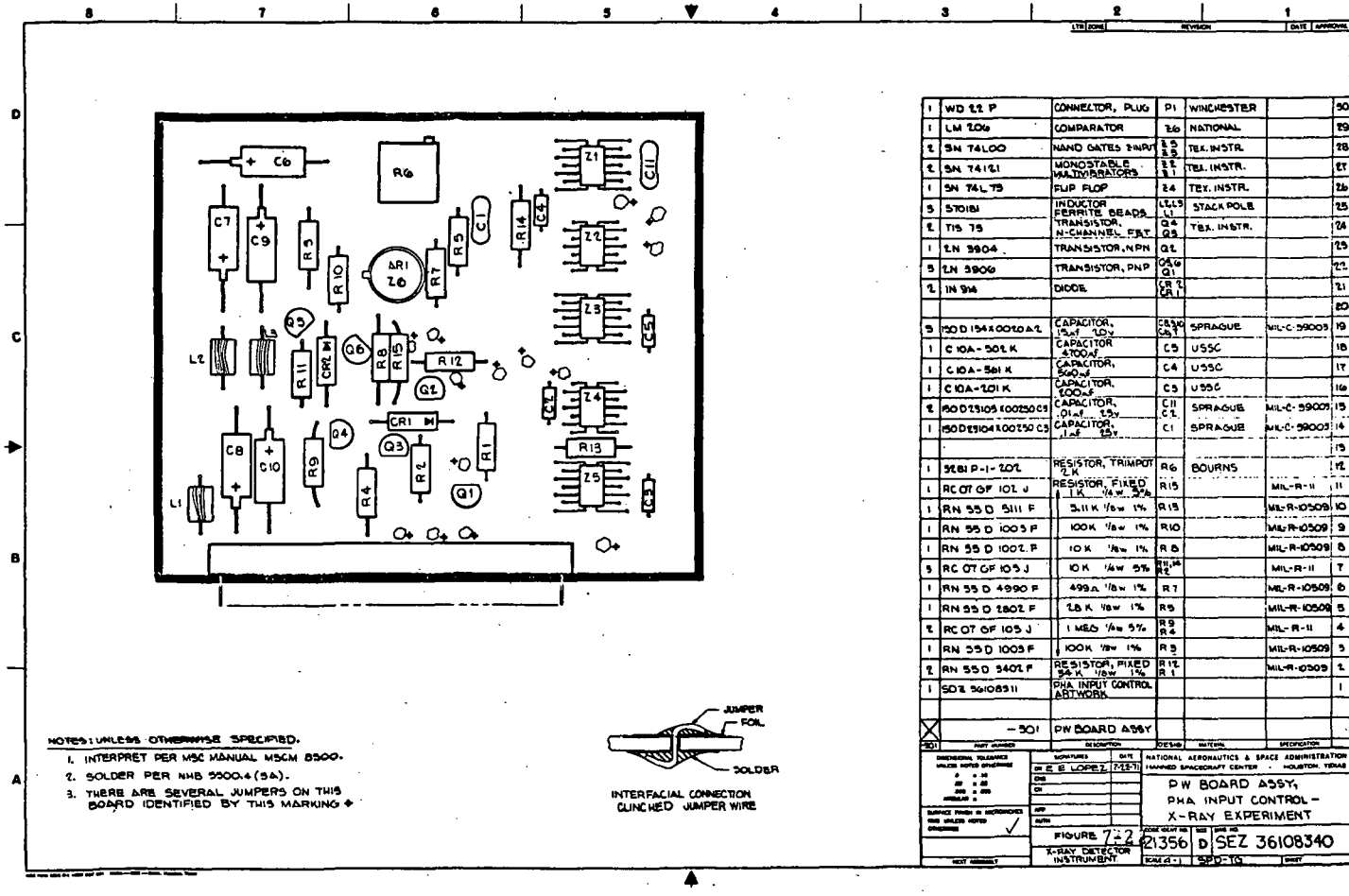


Figure 7-2 PW Board Assembly, PHA Input Control

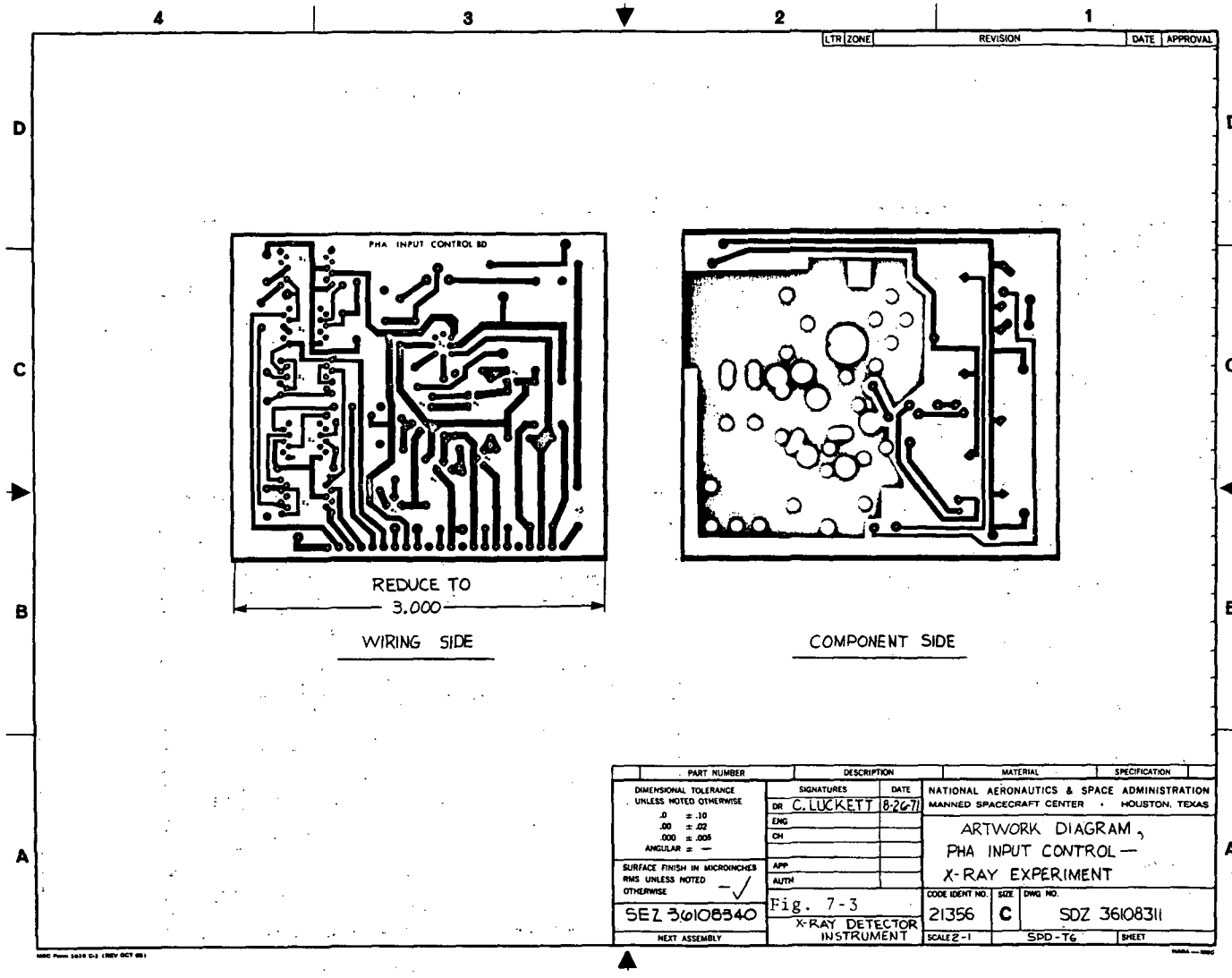


Figure 7-3 Artwork Diagram, PHA Input Control

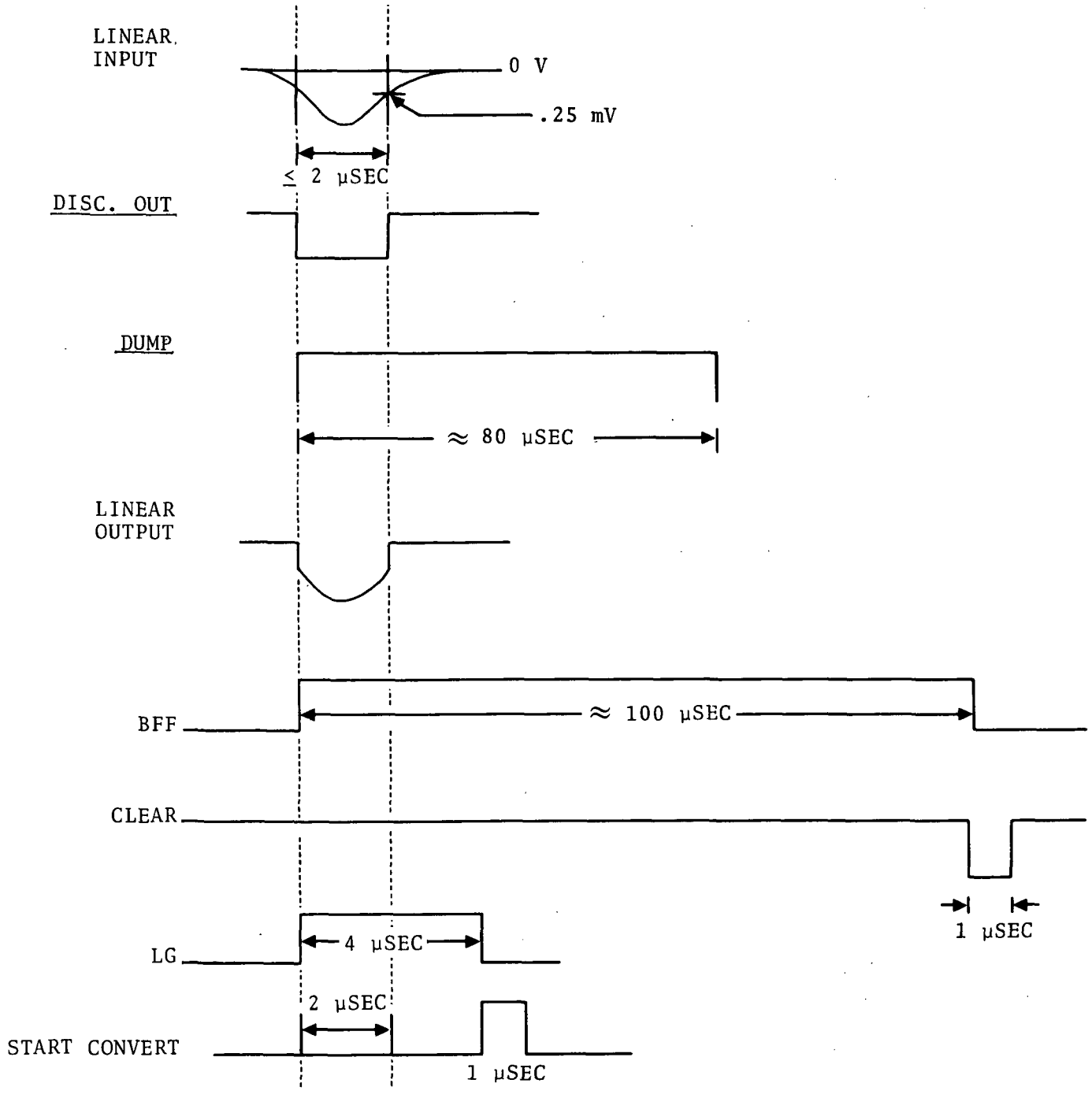


Figure 7-4. — PHA Input Control Timing.

8. ANALOG-TO-DIGITAL CONVERTER

The Analog-to-Digital (A-to-D) Converter forms the heart of the Pulse Height Analyzer. The A-to-D Converter is a 12-bit, successive approximation type employing three Analog Devices (AD550 monolithic quad current switches) and an AD850 precision resistor network. Although only five bits are transmitted, an accuracy equivalent to at least that of a 10-bit converter is required to achieve the one percent differential channel linearity specification. The five-bit conversion time is less than 40 microseconds.

The schematic diagram, board assembly, and printed circuit layout for the Analog portion of the A-to-D converter are shown in Figures 8-1, 8-2, and 8-3 respectively. The schematic diagram, board assembly, and printed circuit layout for the Digital portion of the A-to-D Converter are shown in Figures 8-4, 8-5, and 8-6 respectively. A simplified block diagram of the A-to-D Converter is shown in Figure 8-7.

Digital inputs from the "D" register are converted into weighted currents by the switches and summed by the resistor network. The reference amplifier (AR_1) makes the current in the switch reference transistor equal I_{ref} (see Figure 8-7) by controlling the Base-to-Emitter voltage of all the transistor switches. This weighted current is subtracted from a current proportional to the input analog voltage. The polarity of the resulting error current is fed back to the "D" register to either leave or reset the bit being compared. The converter starts each conversion upon receipt of a positive Start Convert pulse. During conversion the status output is low or "busy".

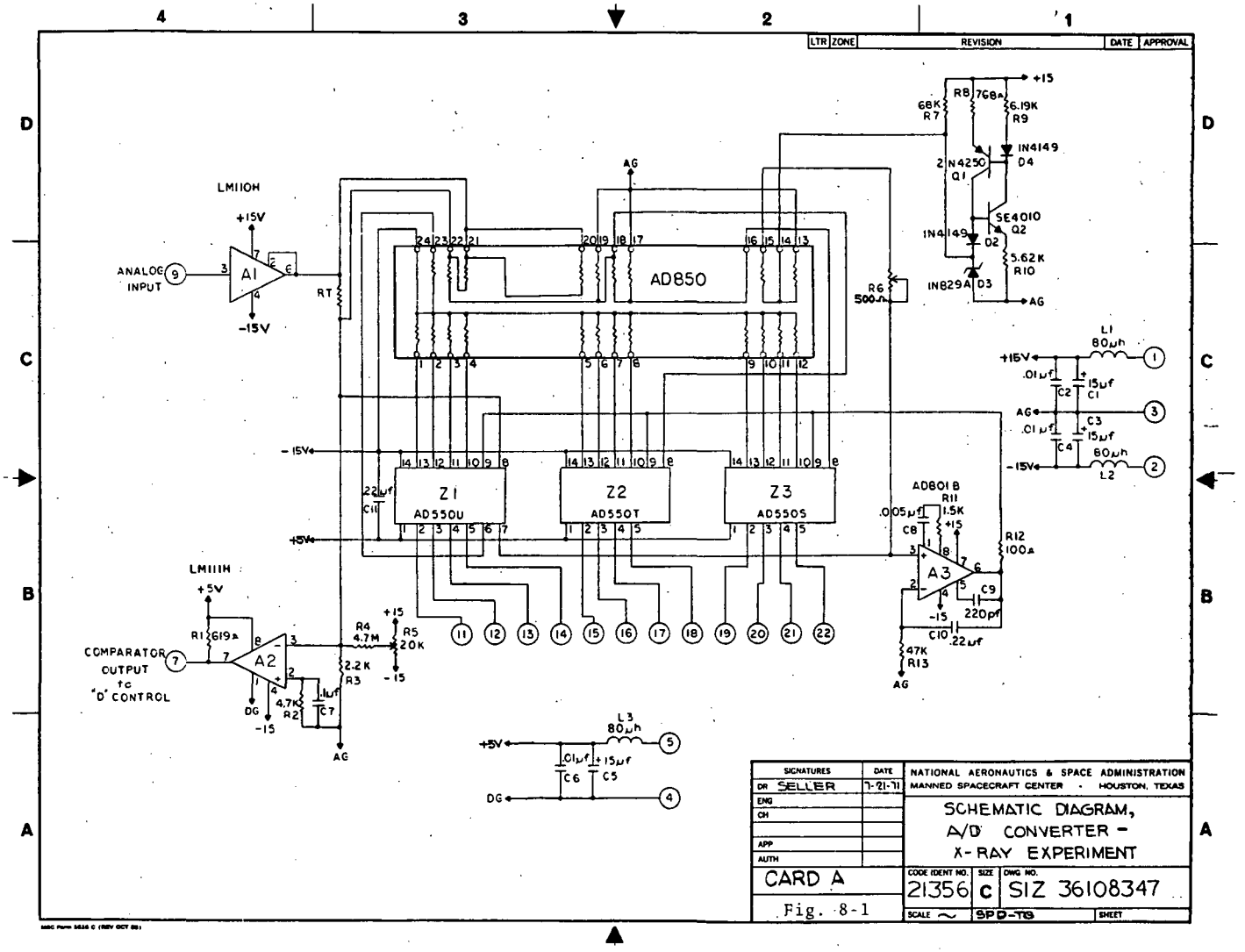


Figure 8-1 Schematic Diagram, A/D Converter

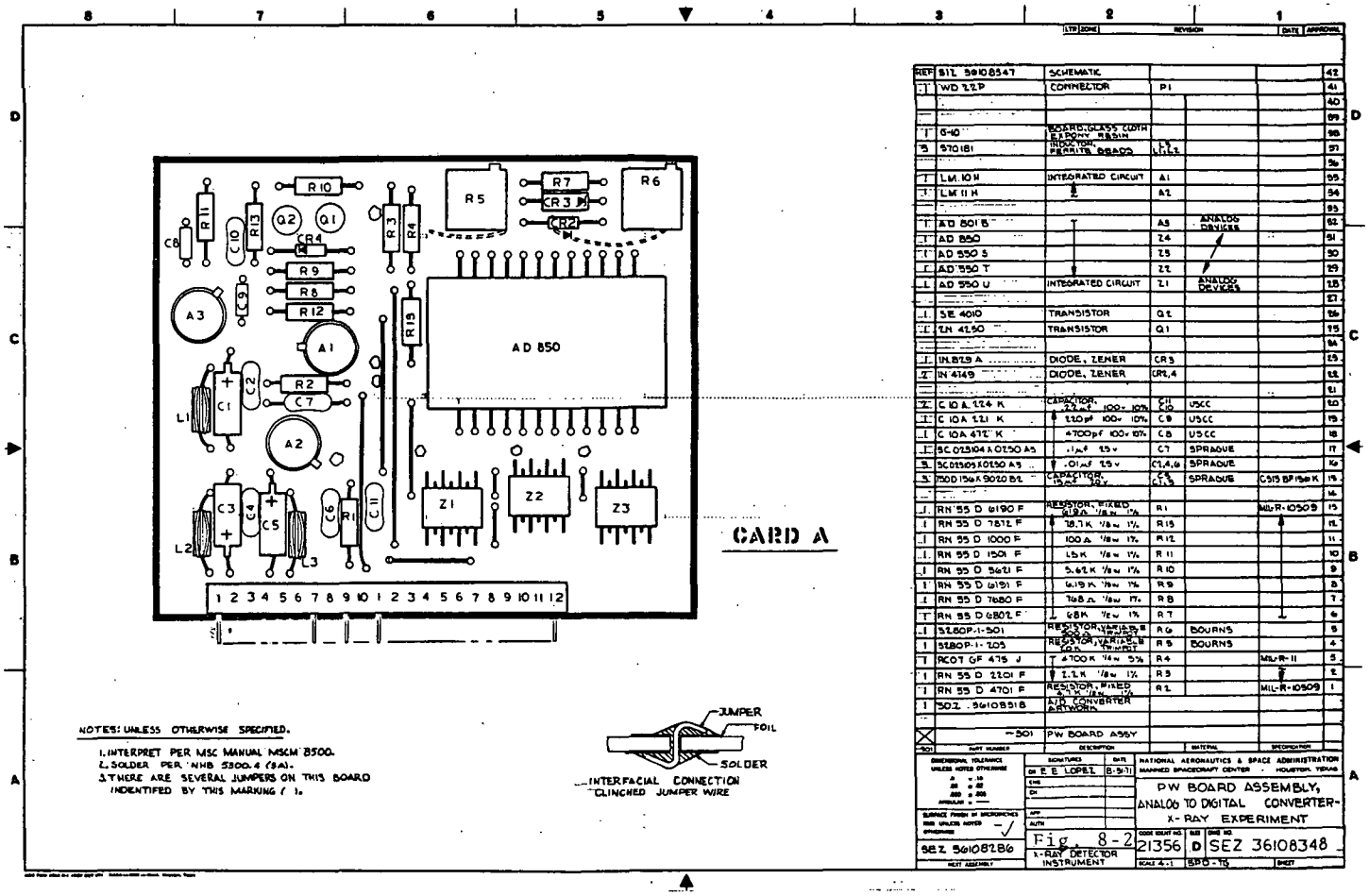


Figure 8-2 PW Board Assembly, A/D Converter

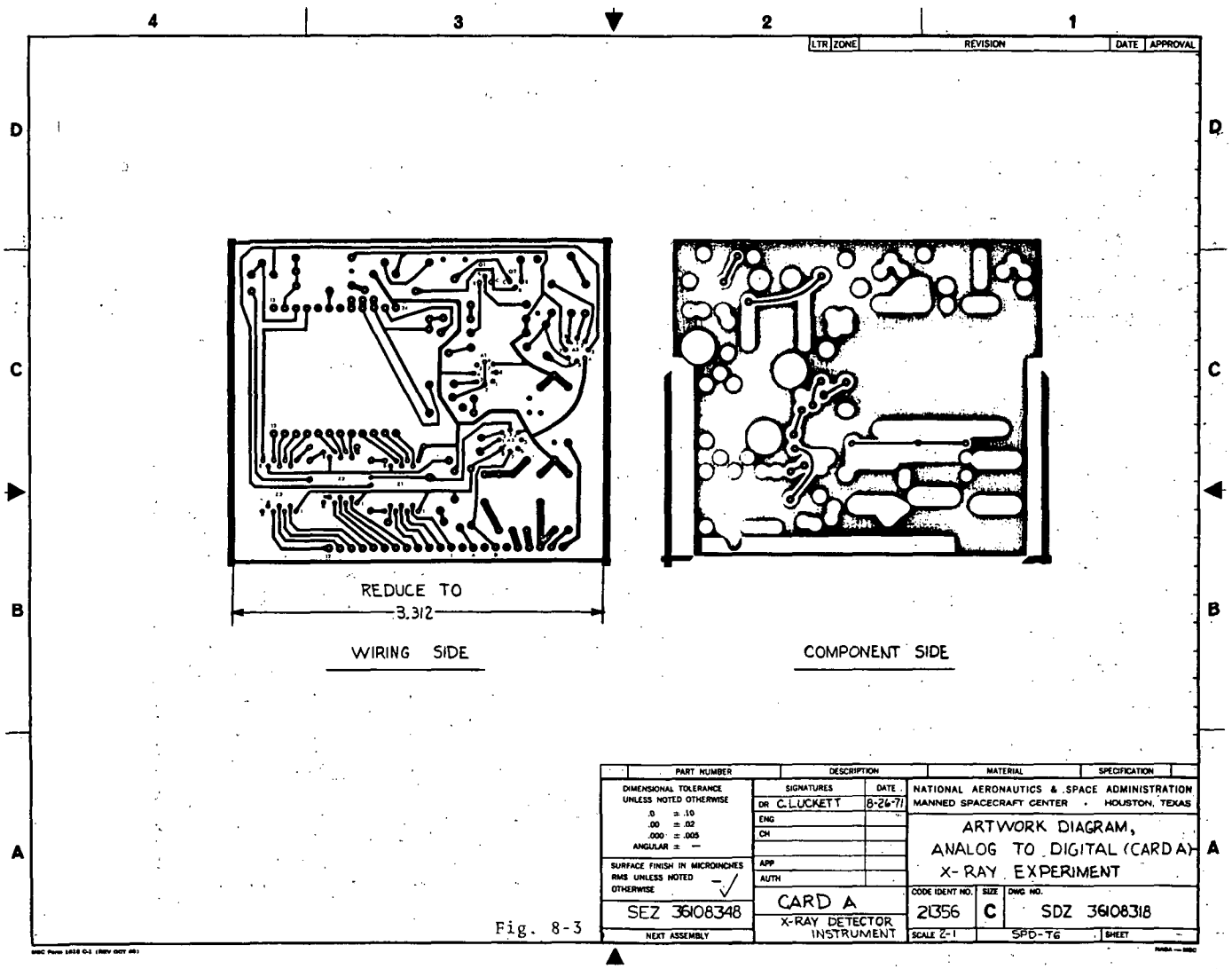


Fig. 8-3

Figure 8-3 Artwork Diagram, A/D Converter (Card A)

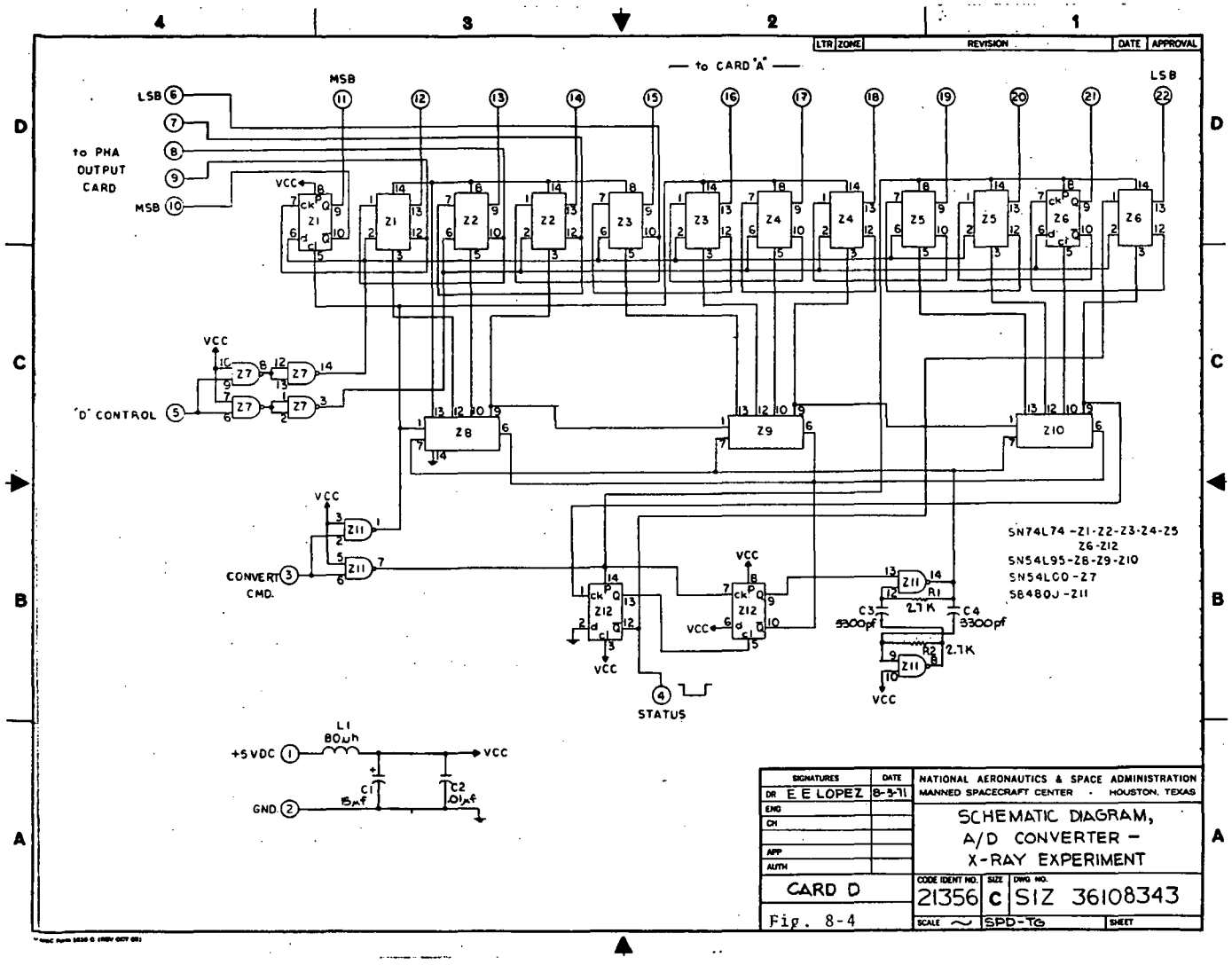


Figure 8-4 Schematic Diagram, A/D Converter

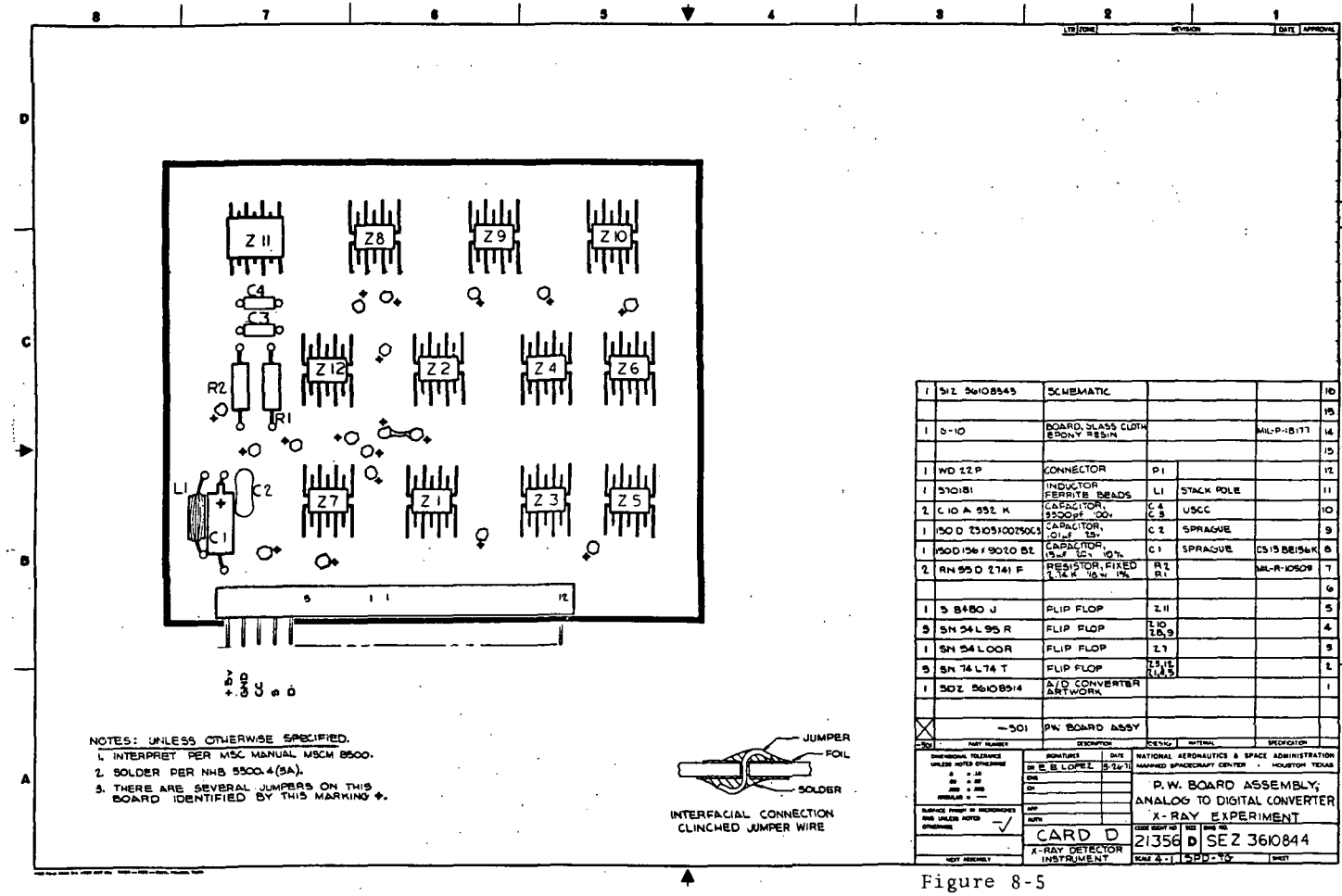


Figure 8-5

Figure 8-5 PW Board Assembly, A/D Converter

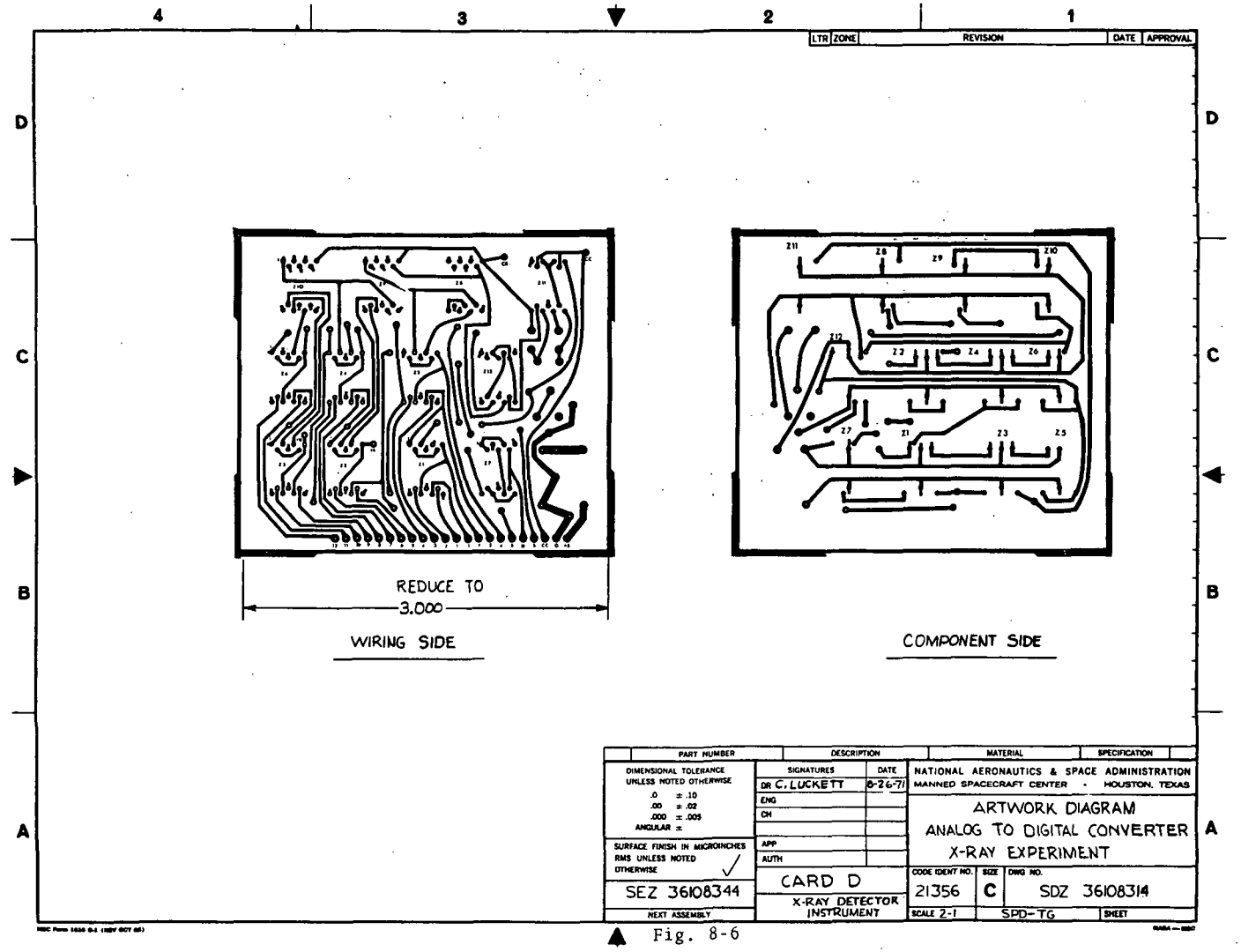


Fig. 8-6

Figure 8-6 Artwork Diagram, A/D Converter (Card D)

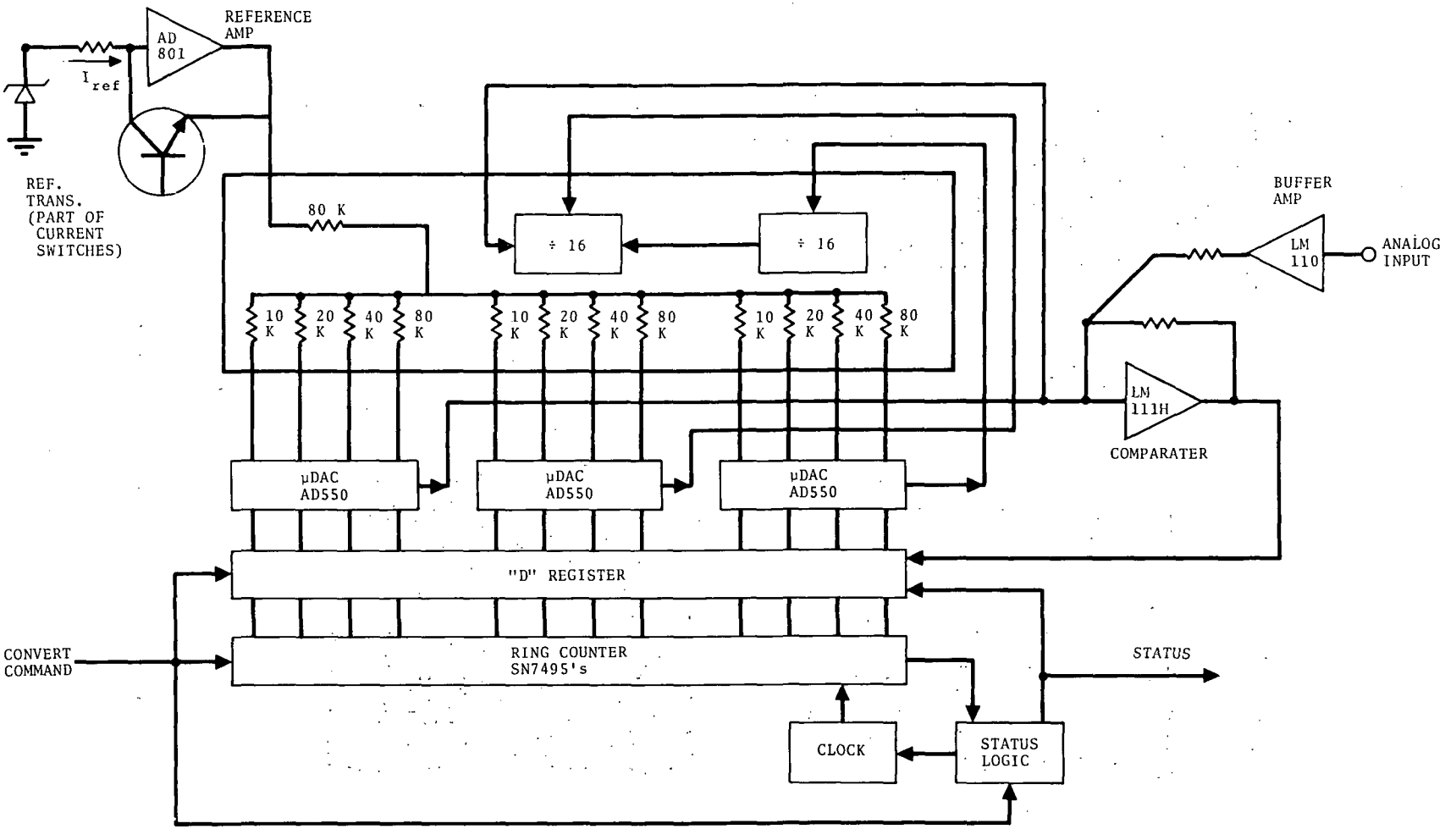


Figure 8-7. – Analog-to-Digital Converter, Block Diagram.

9. TELEMETRY INTERFACE

The telemetry interface accepts five bits of pulse height data from the A-to-D Converter and three bits of discriminator data from the coincidence, anticoincidence and rise-time discriminators. The data is transferred to the telemetry upon receipt of an interrogate pulse from the telemetry.

The telemetry interface uses a status signal from the A-to-D Converter and a busy signal from the PHA control circuit to insure that data will be available for transfer only if an X-ray event has occurred within the previous interrogate interval and if the A-to-D Converter is not converting.

DTL output gates are provided to allow wire-or multiplexing into the telemetry's PCM encoder. The schematic diagram, board assembly, printed circuit layout, and timing diagram are shown in Figures 9-1, 9-2, 9-3, and 9-4 respectively.

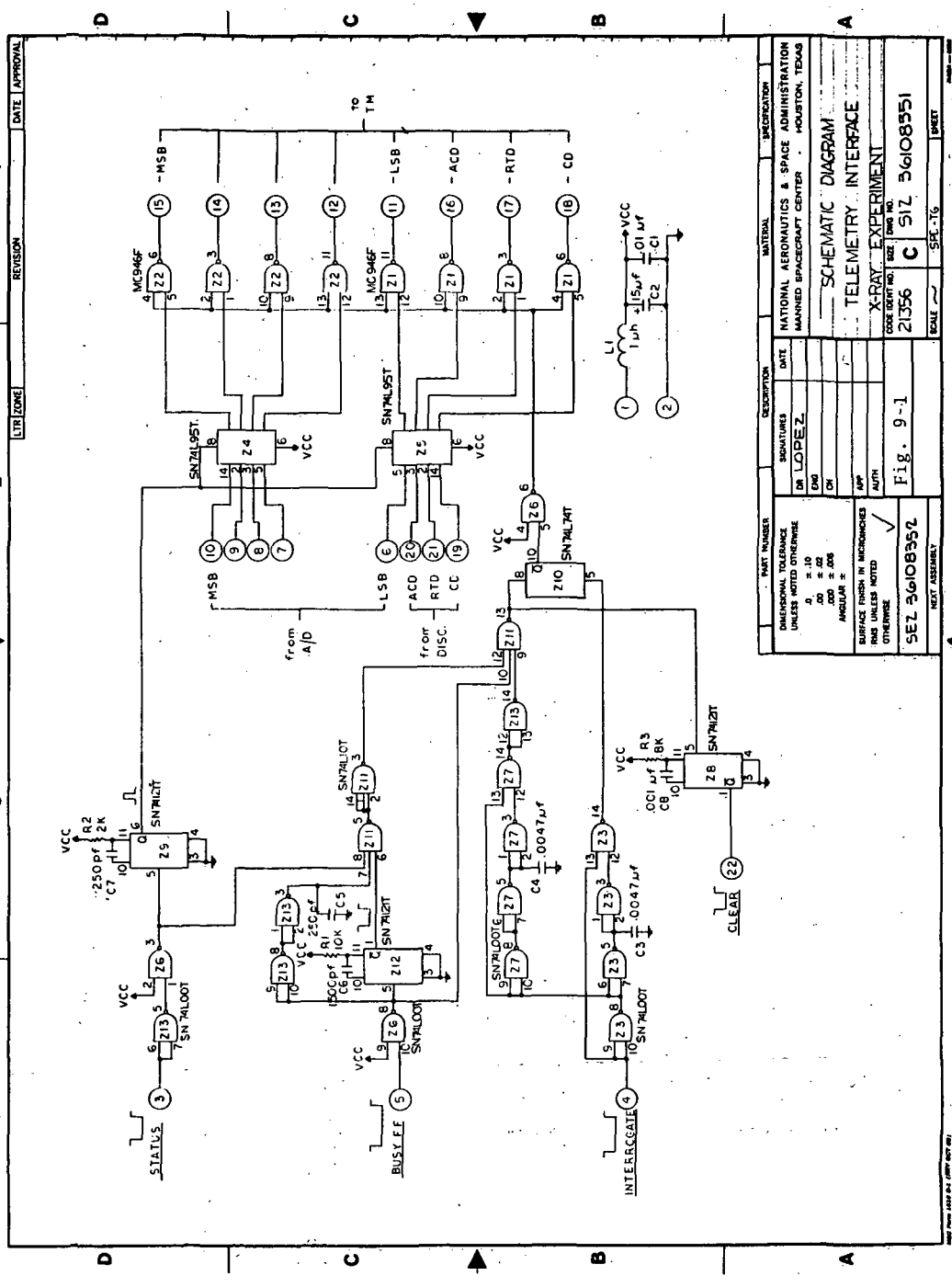


Figure 9-1. — Schematic Diagram, Telemetry Interface

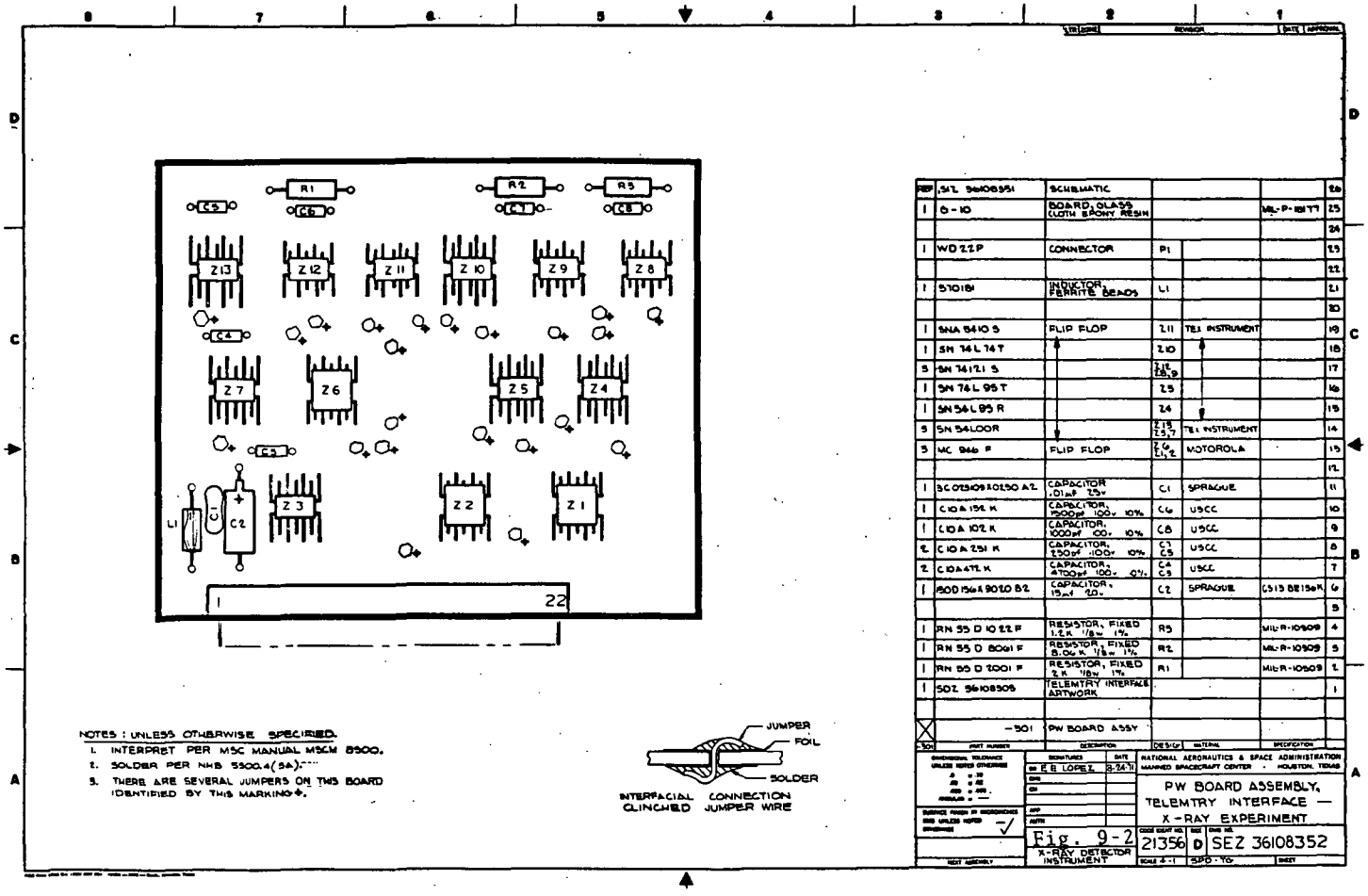


Figure 9-2. — PW Board Assembly, Telemetry Interface

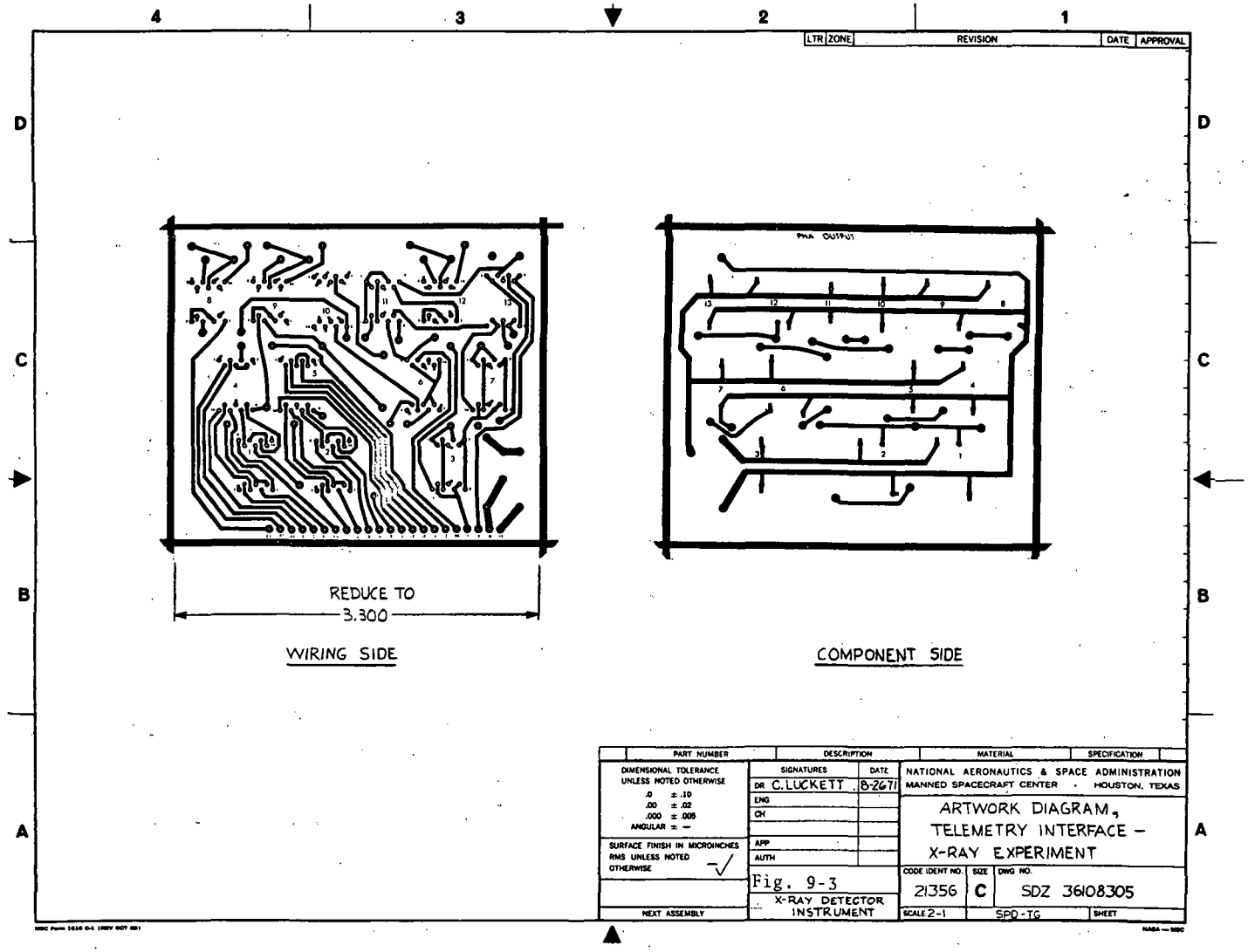


Figure 9-3. — Artwork Diagram, Telemetry Interface

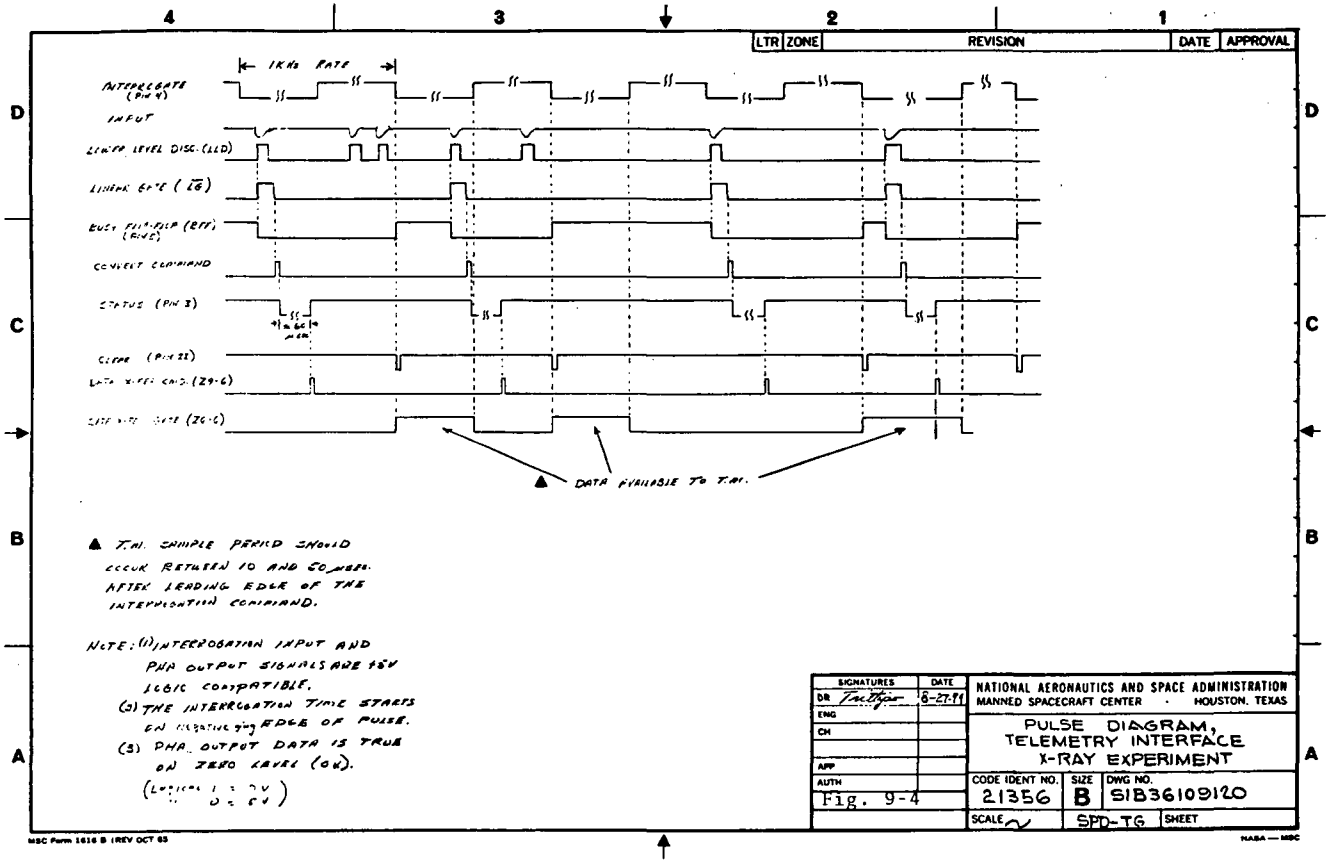


Figure 9-4. – Pulse Diagram, Telemetry Interface

10. ANTICOINCIDENCE AMPLIFIER AND AUTO-GAIN-CONTROL (AGC) DISCRIMINATOR

The Anticoincidence Amplifier shapes the tail pulses from the Anticoincidence Preamplifier. It is an Ortec-Type active filter amplifier identical to those in the main amplifier section. For a discussion of this amplifier refer to Section 5.

The AGC discriminator determines whether a pulse from the Anticoincidence Amplifier is larger or smaller than a preset level of three volts. On a scale which equates five volts to an X-ray event energy of 10 Kev, a three volt level corresponds to the 6 Kev energy of the Iron-55 calibration source.

The discriminator sends a COUNT command to the up-down counter whenever an X-ray is detected in the Anticoincidence Detector. Coincidentally it sets the UP command to a logic "1" and the DOWN command to a logic "0" if the pulse is less than three volts. The reverse occurs if the pulse is greater than three volts. Pulses below 25 millivolts, which correspond to 50 eV of energy are rejected as noise.

The schematic diagram, board assembly, printed circuit layout, and timing diagram are shown in Figures 10-1, 10-2, 10-3, and 10-4 respectively.

Comparator X1 is the mean pulse level discriminator. Comparator X2 is the noise level discriminator. A one shot (Z_1) produces the one microsecond count pulses and a flip flop (Z_2) stores the UP and DOWN commands.

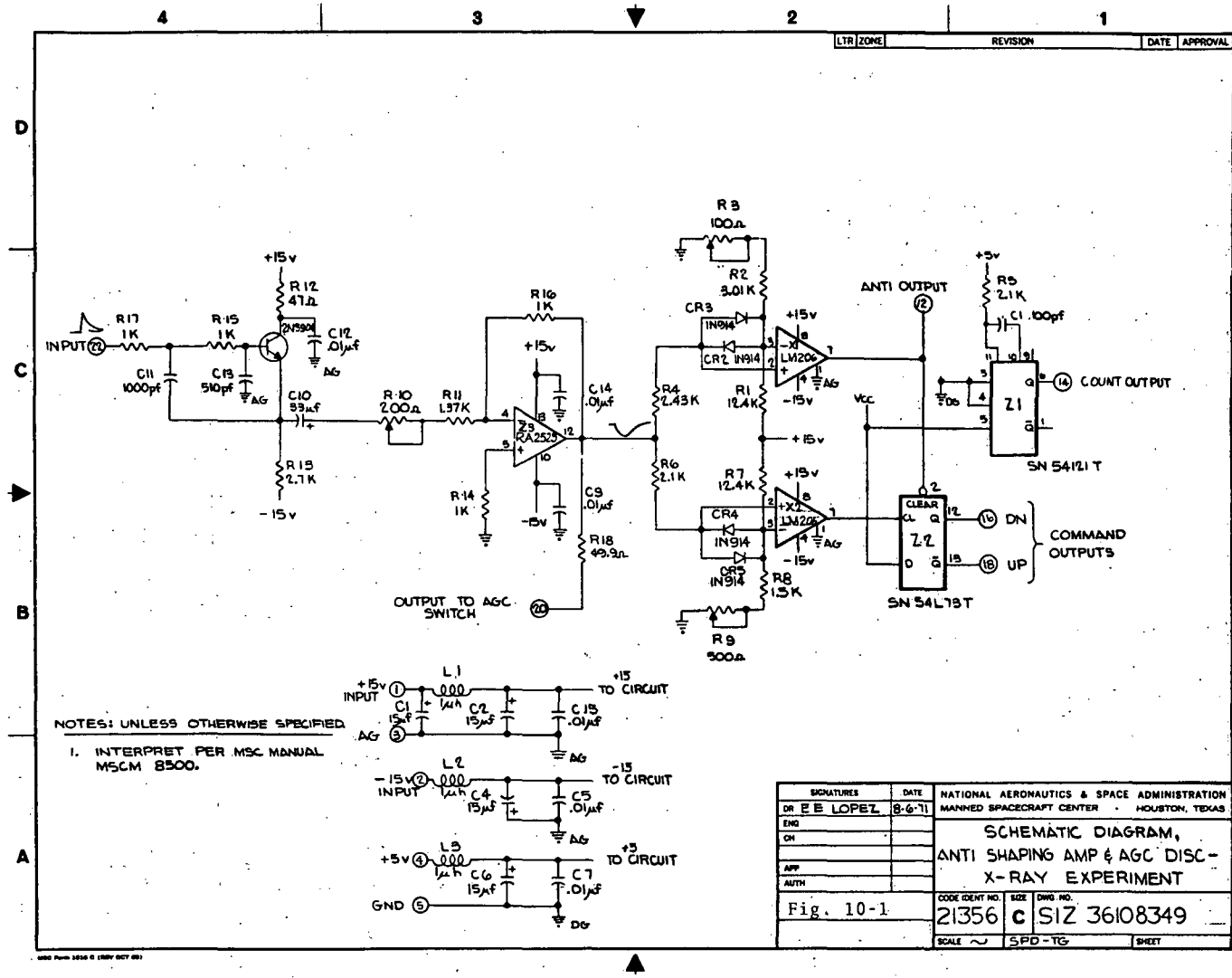


Figure 10-1.— Schematic Diagram, Antishaping Amplifier and AGC Discriminator

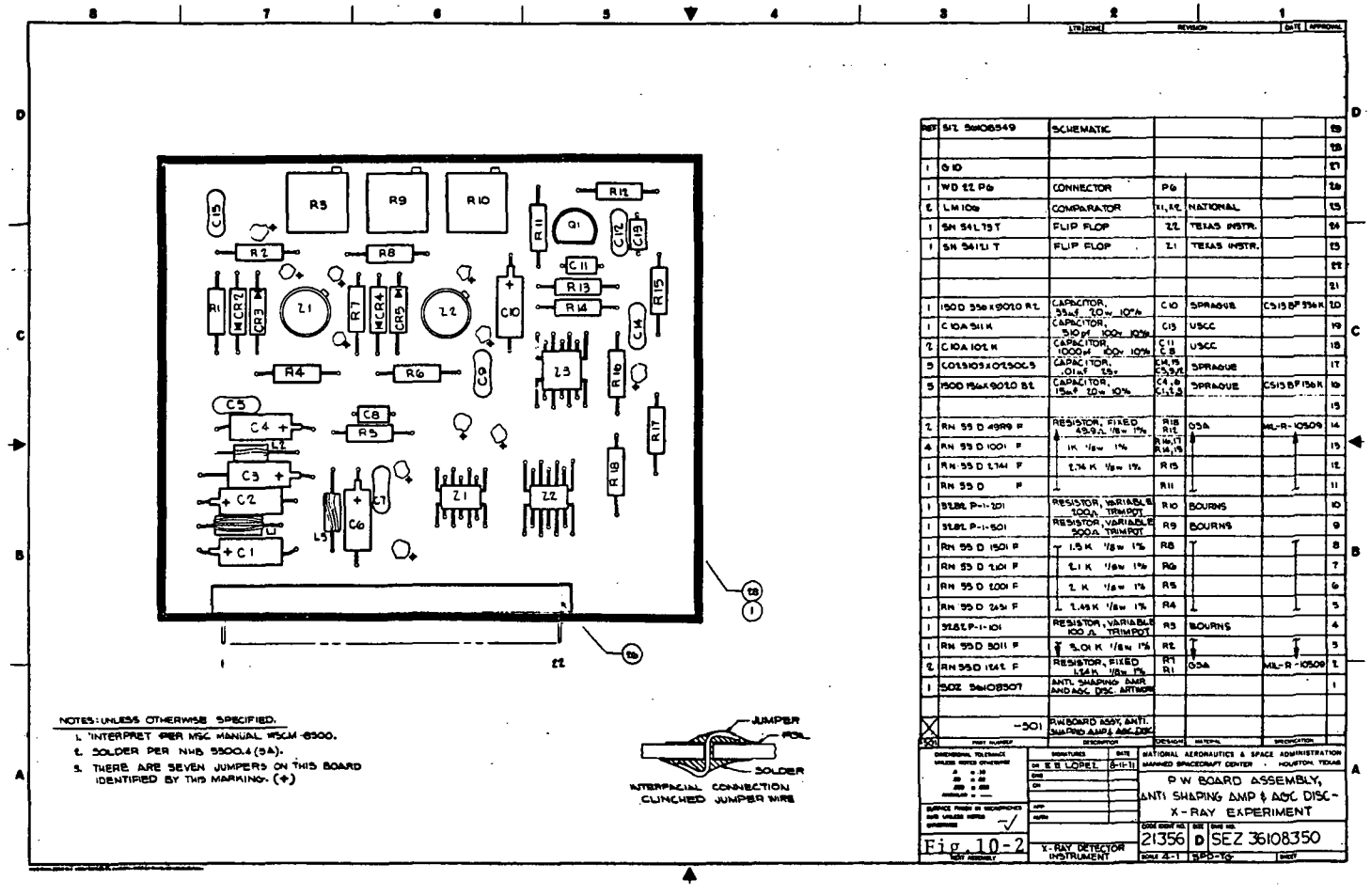


Figure 10-2. — PW Board Assembly, Antishaping Amplifier and AGC Discriminator

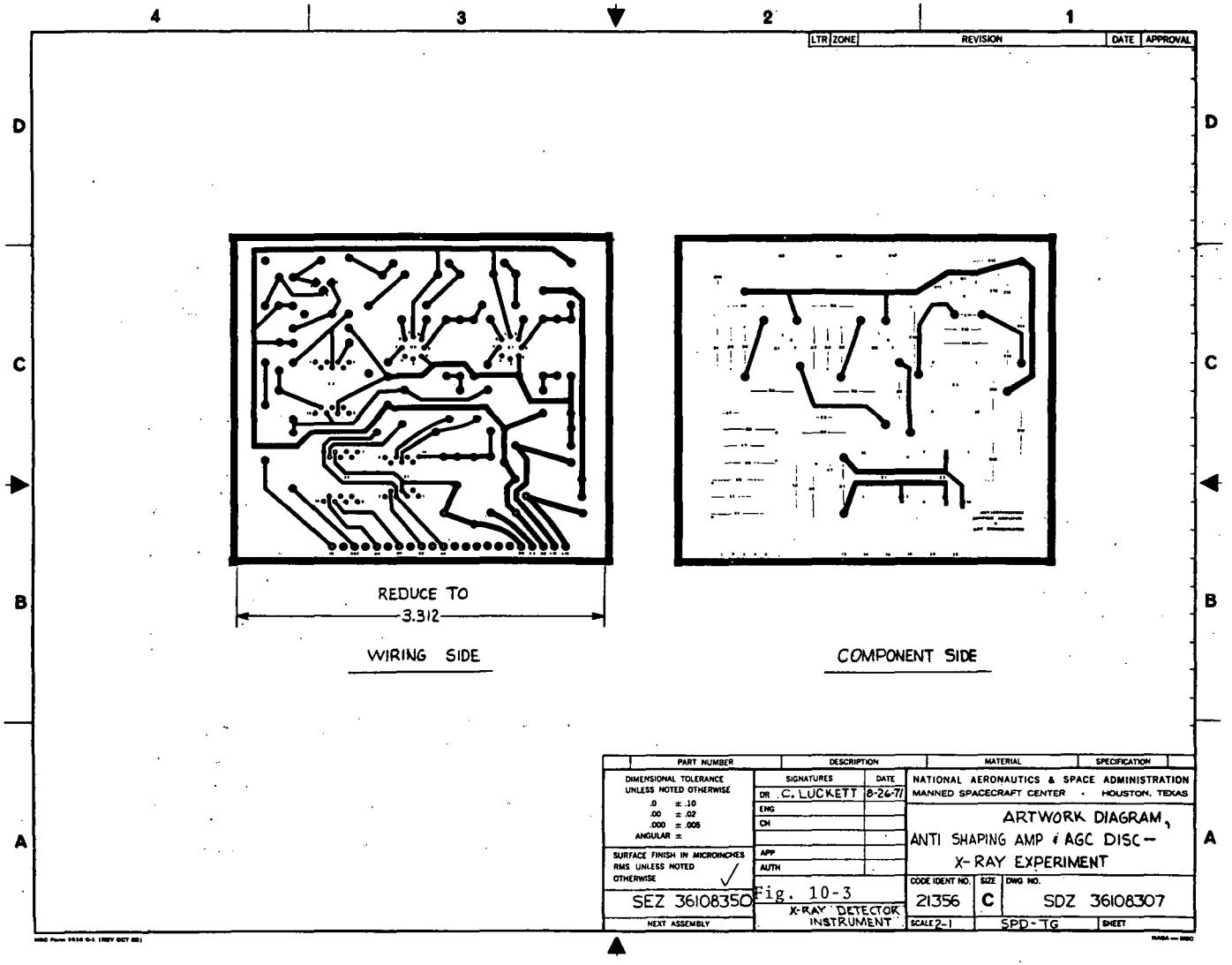


Figure 10-3. – Artwork Diagram, Antishaping Amplifier and AGC Discriminator

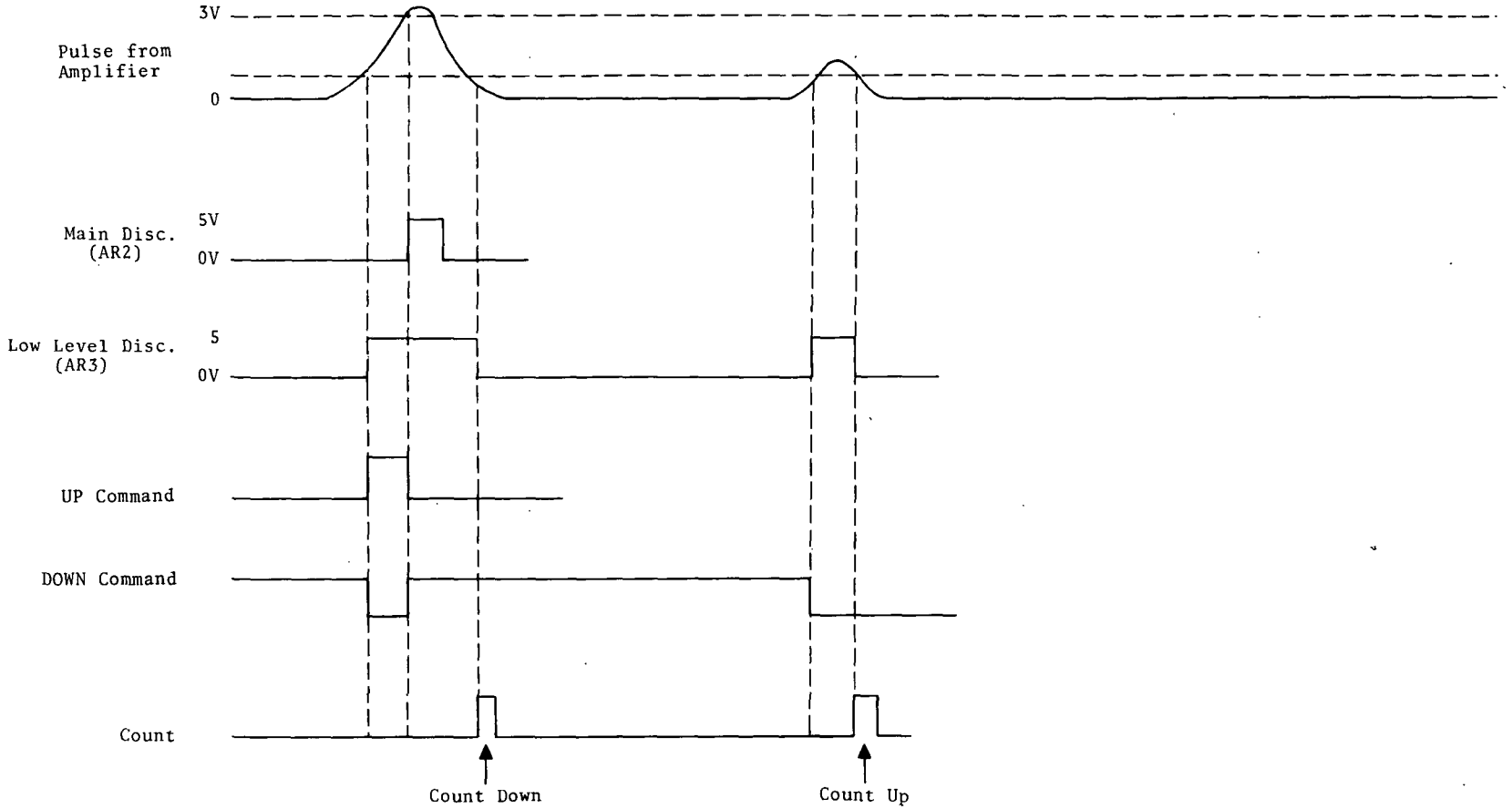


Figure 10-4. Timing Diagram, AGC Amplifier Discriminator

11. AUTO GAIN CONTROL (AGC) UP-DOWN COUNTER

The AGC Up-Down Counter stores a digital number corresponding to the program voltage required to program the high voltage supply to a level that produces three volt pulses from the Anticoincidence Amplifiers when a 6 Kev X-ray is detected.

The 12-bit Up-Down Counter is implemented with three TTL MSI 4-bit synchonous Up-Down Counters connected in series. The counter will count up one bit when the UP command is high and a clock pulse is received. It will count down one bit when the DOWN command is high and a clock pulse is received. The UP and DOWN commands are inverted functions insuring that only one of the two is high at any given time. Logic is provided to inhibit the DOWN counts when the counter is loaded with zeros and UP count when the counter is loaded with ones.

The schematic diagram, board assembly, and printed circuit layout are shown in Figures 11-1, 11-2, and 11-3 respectively.

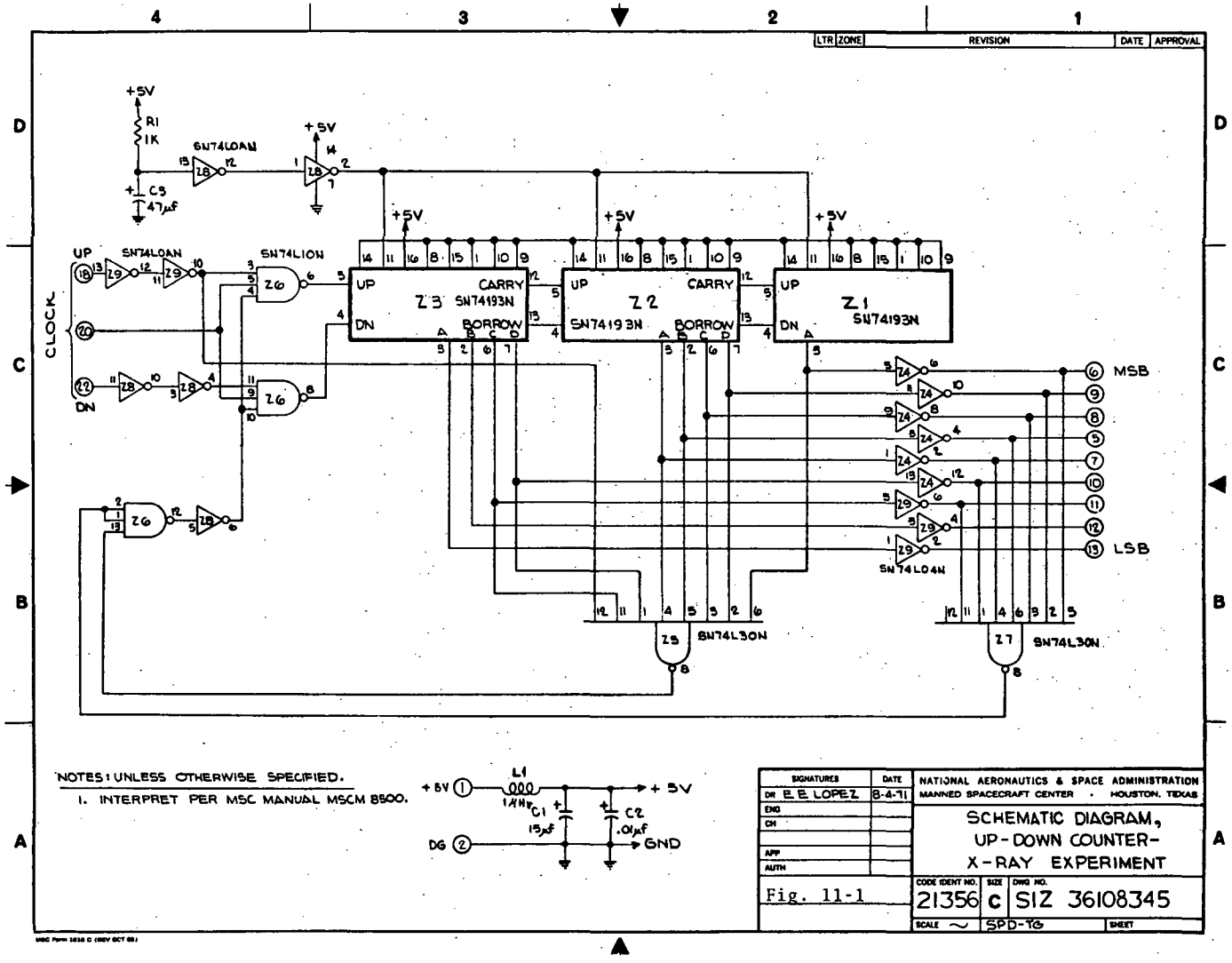


Figure 11-1 — Schematic Diagram, Up-Down Counter

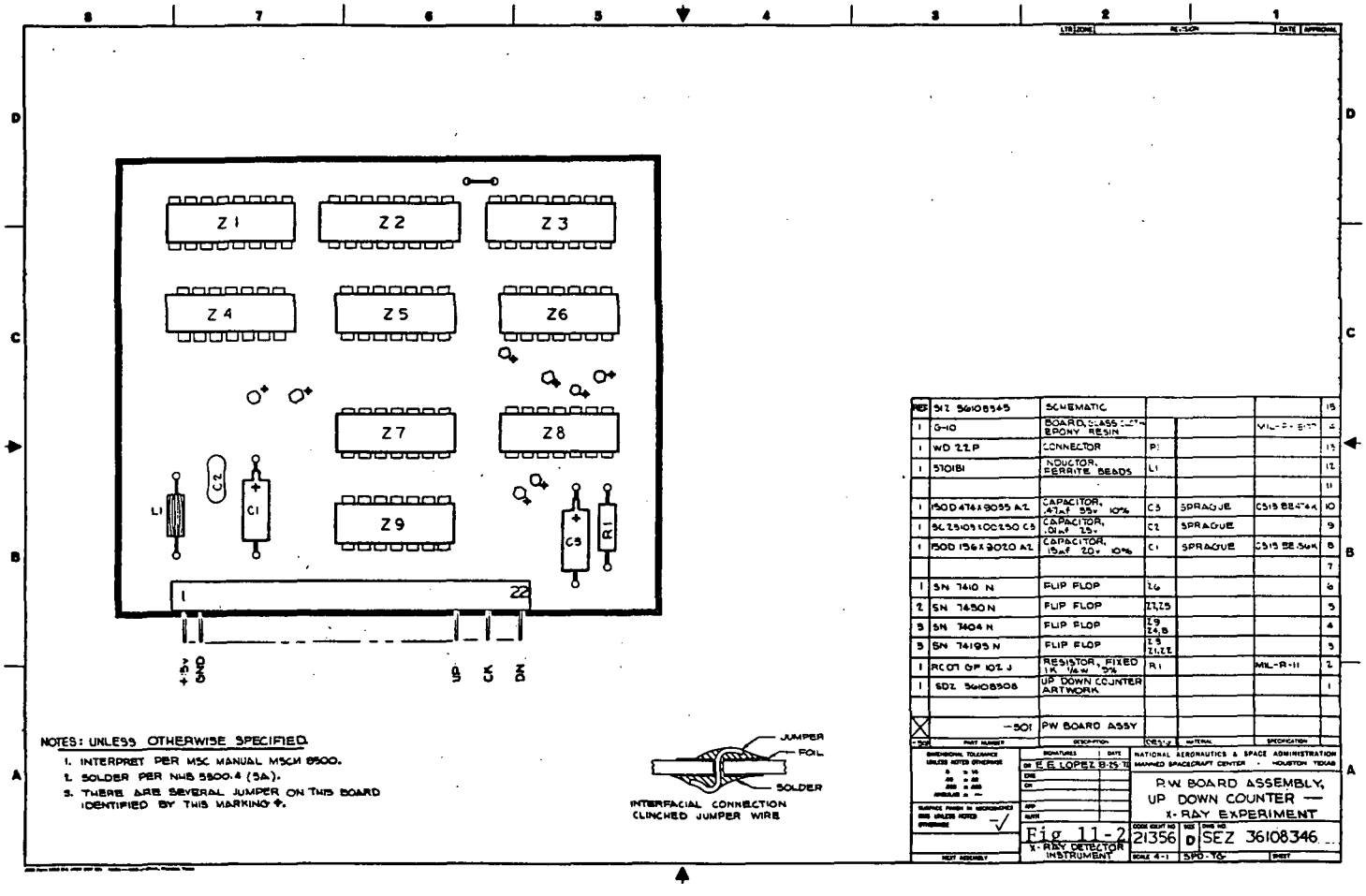


Figure 11-2. — P.W. Board Assembly, Up Down Counter

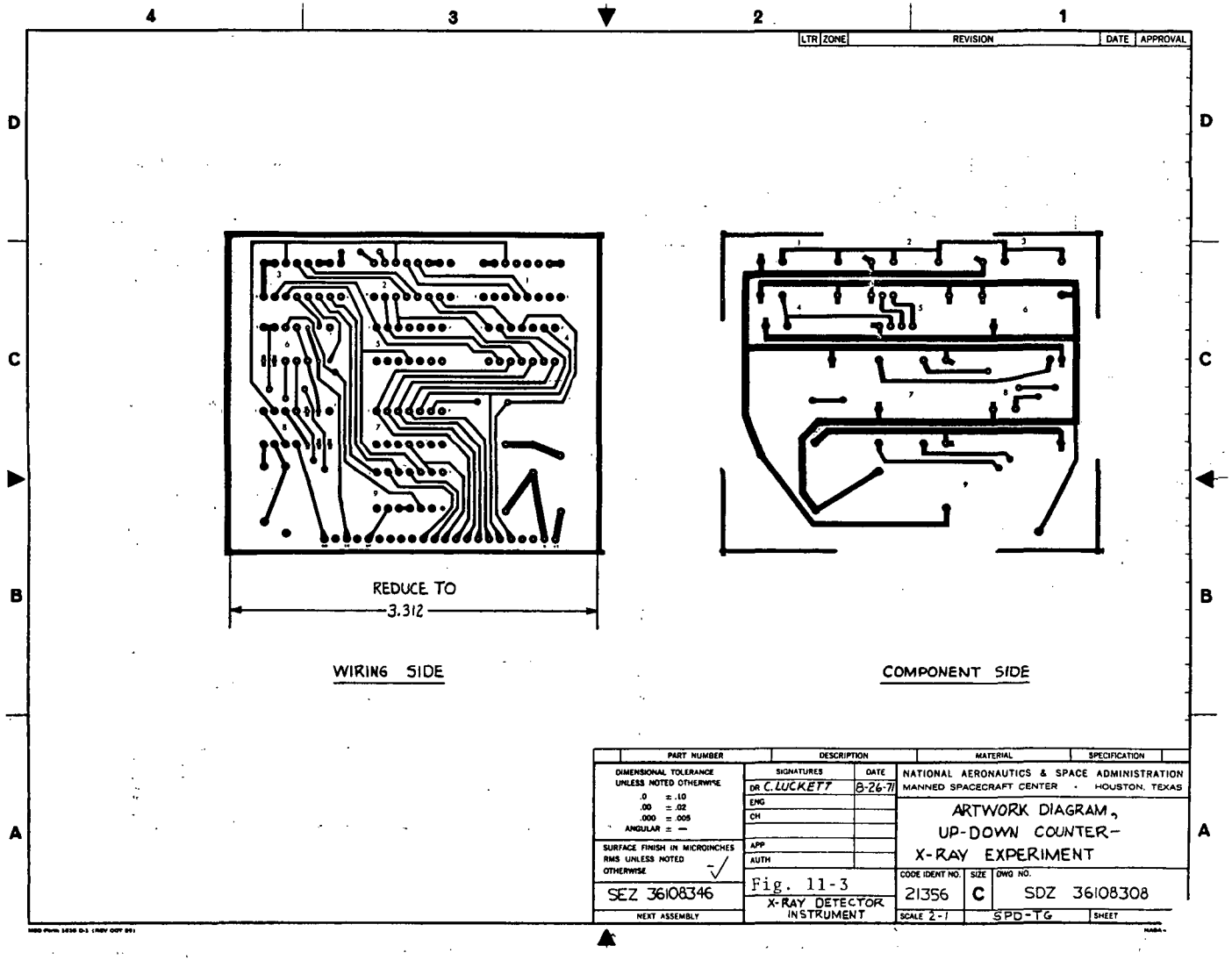


Figure 11-3. — Artwork Diagram, Up-Down Counter

12. DIGITAL-TO-ANALOG CONVERTER

The Digital-to-Analog Converter programs the high voltage supply with a zero-to-six volt analog voltage proportional to the twelve-bit digital number stored in the AGC Up-Down Counter.

The schematic diagram, board assembly, and printed circuit layout are shown in Figures 12-1, 12-2 and 12-3 respectively.

The twelve-bit D-A Converter employs three Analog Devices (AD 550 monolithic quad current switches) and an AD 850 resistor network. Digital inputs to the current switches are converted into successive approximation-type weighted currents by the current switches. The individual currents are summed by the resistor network and converted by an operational amplifier (AR_2) into an analog voltage proportional to the digital input. The switch currents are precisely controlled by reference amplifier AR1, which forces the switch reference transistor's collector current to equal a reference current of 0.125 milliamperes generated by Zener diode CR1, resistors R20, R21, and potentiometer R7. A block diagram of the Digital-to-Analog Converter is shown in Figure 12-4.

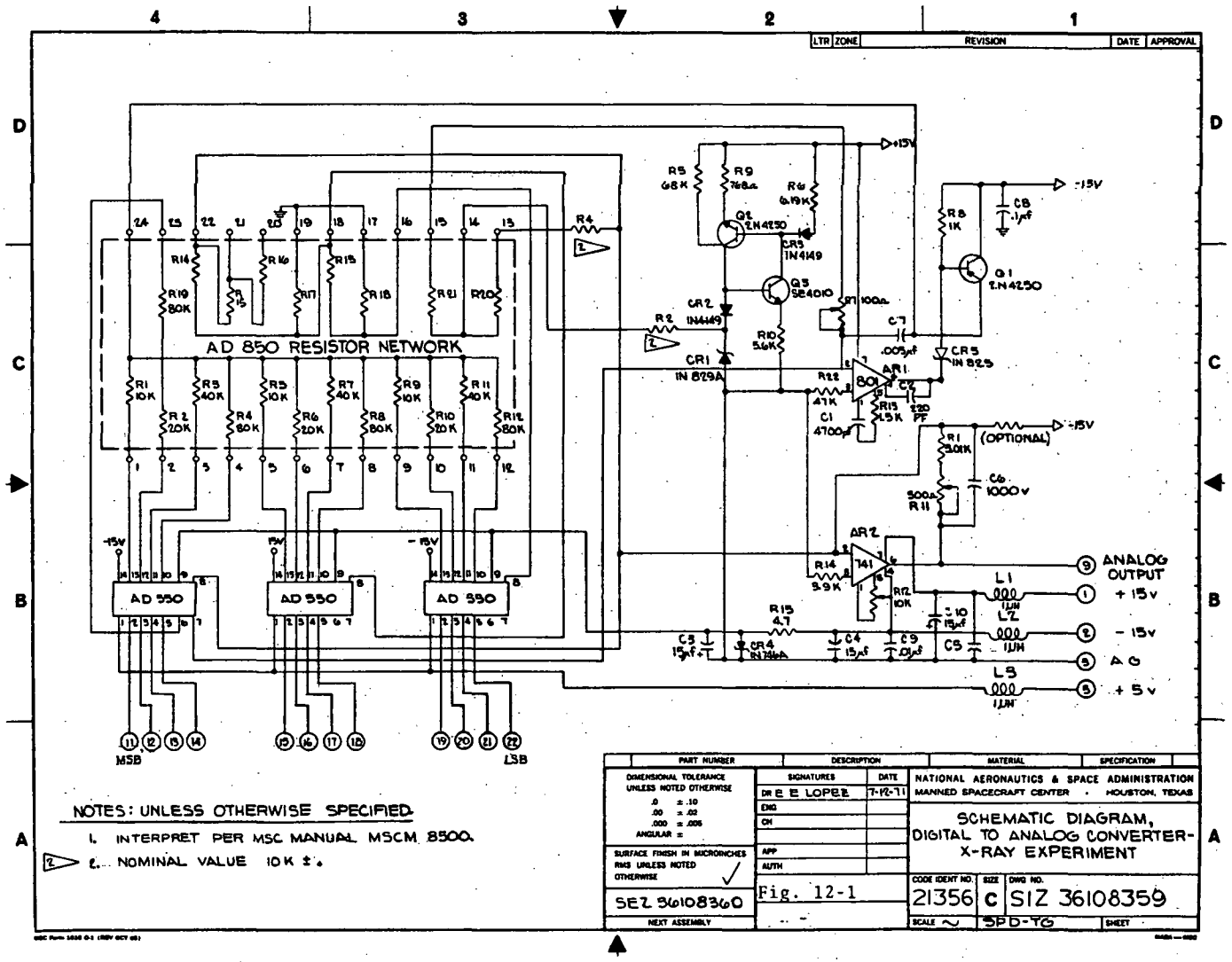


Figure 12-1. — Schematic Diagram, D-A Converter

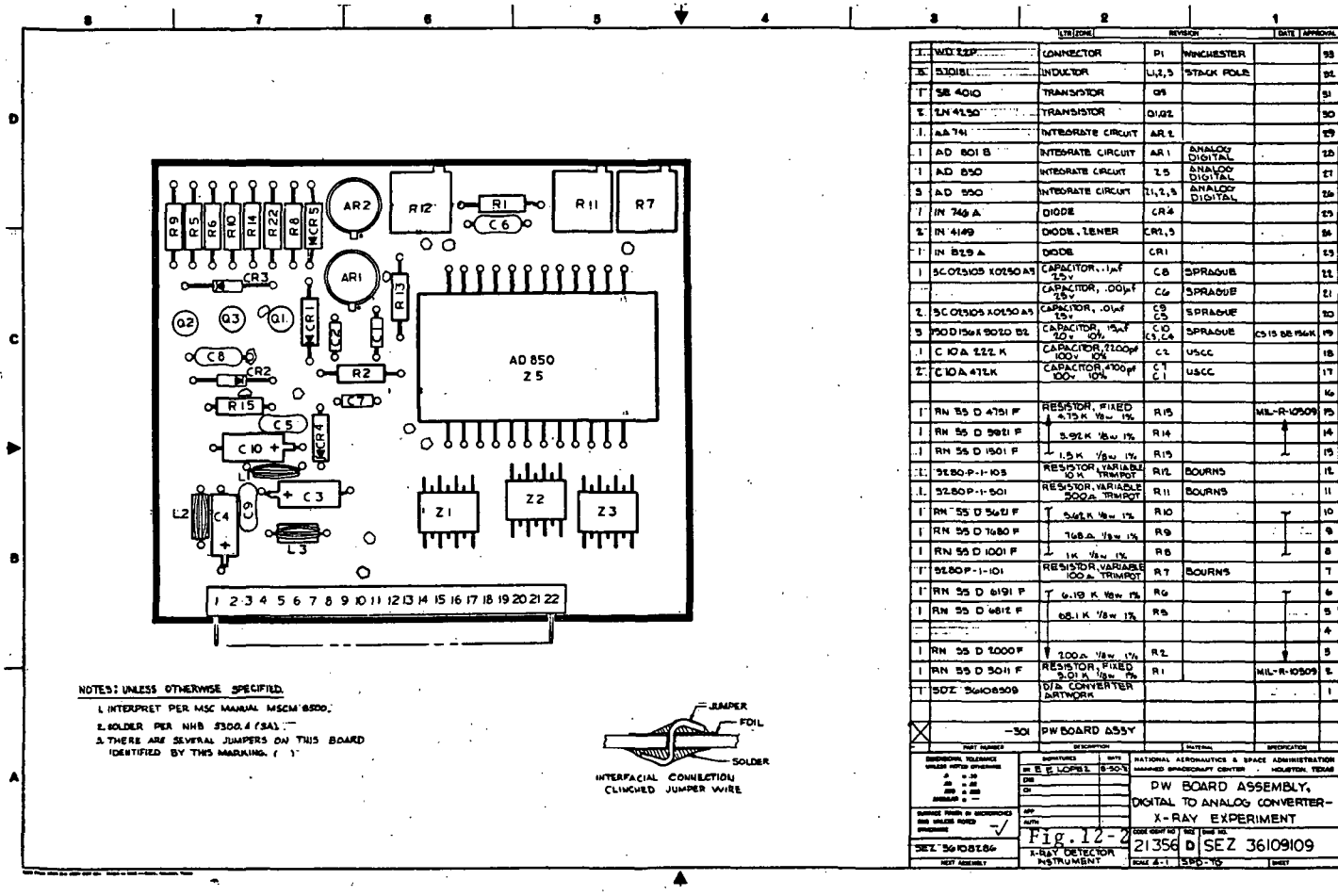


Fig. 12-2

Figure 12-2. — P.W. Board Assembly, D-A Converter

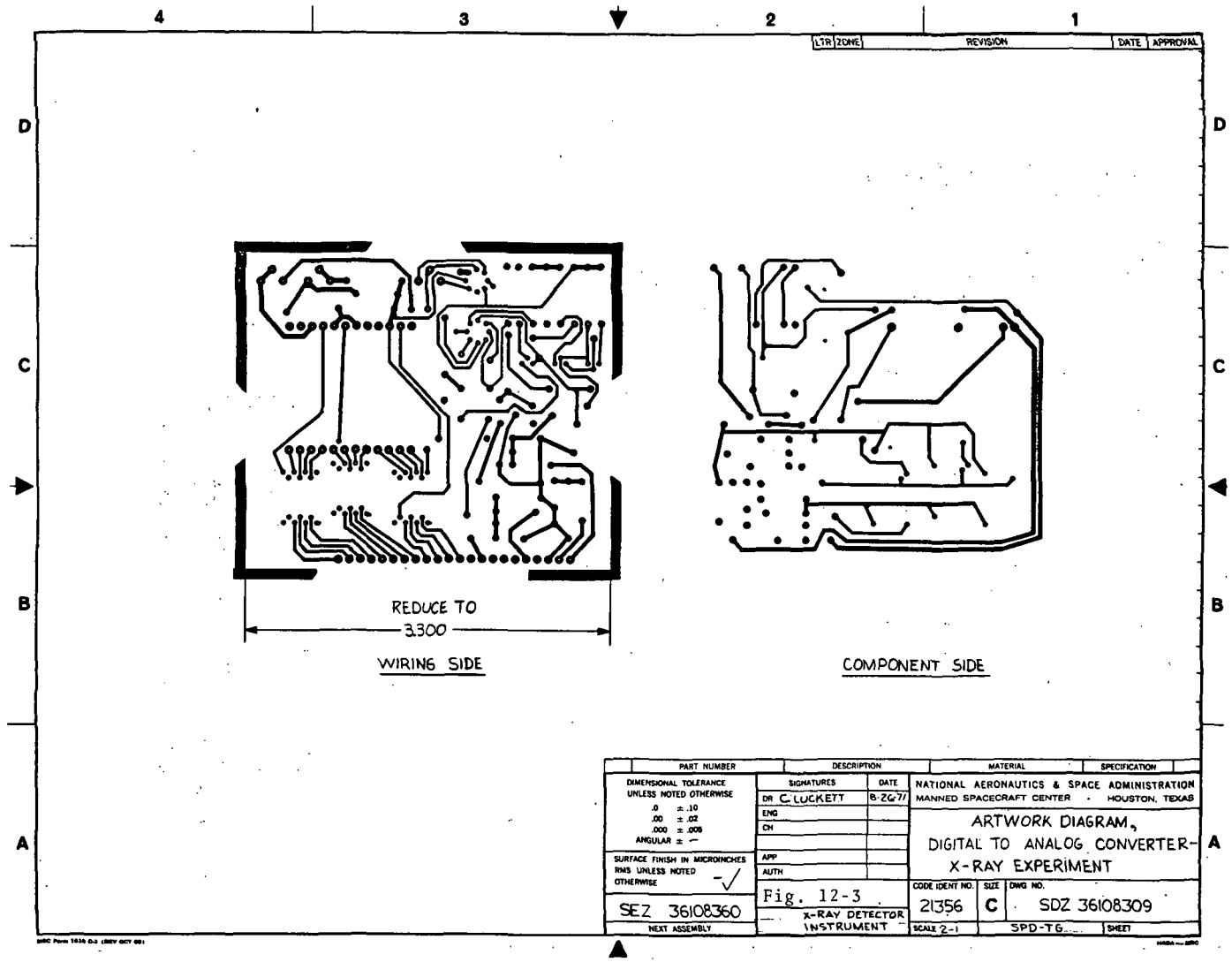


Figure 12-3. – Artwork Diagram, D-A Converter

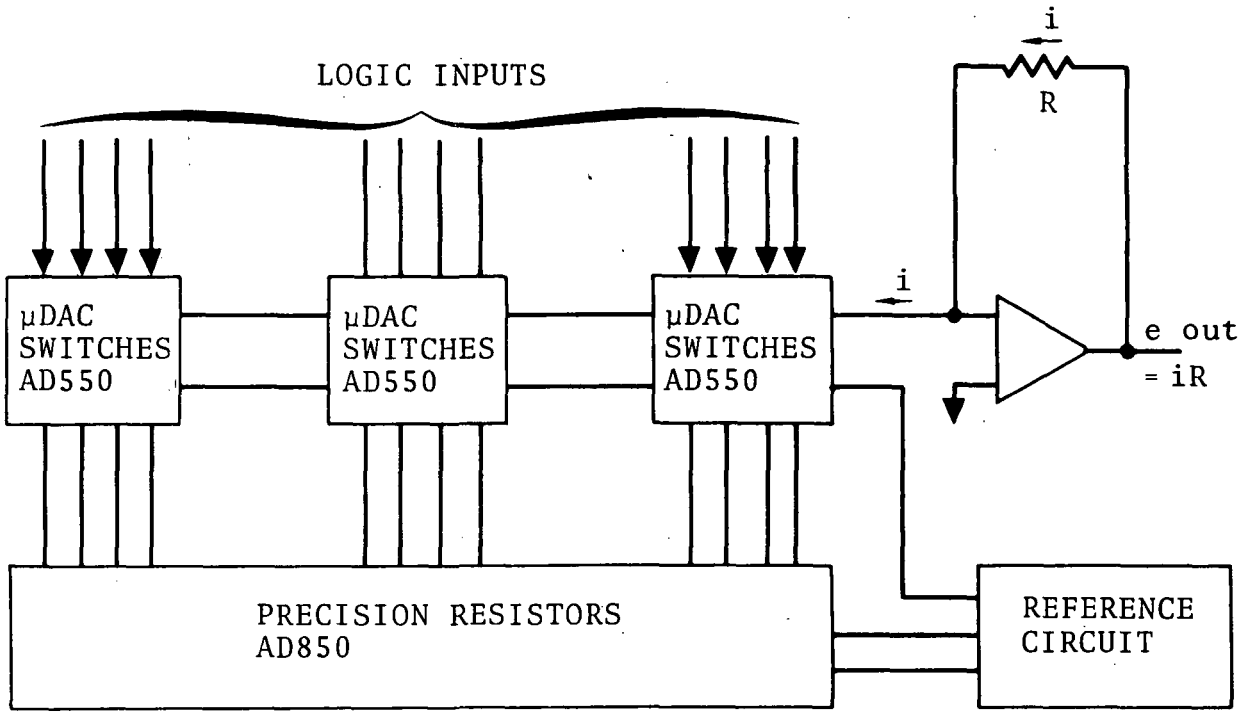


Figure 12-4. Block Diagram, Digital-to-Analog Converter

13. RISE-TIME DISCRIMINATOR

Generally X-rays will ionize a shorter path in a gas proportional counter and thus have a shorter charge collection time than will charge particles.

The Rise-Time Discriminator will distinquish between nuclear events whose charge collection time is less than 75 percent of, or greater than 125 percent of, a present time as low as 40 manoseconds. The operable range of pulse heights is 150 millivolts to 5 volts which corresponds to an energy range of 300 eV to 10Kev and all but the first of the 32 pulse height analyzer channels.

The schematic diagram, board assembly, printed circuit layout, and timing diagram are shown in Figures 13-1, 13-2, and 13-3 13-4 respectively.

First, the pulses from the preamplifiers are summed and filtered with a 30 nanosecond time constant Twin-T notch filter which reduces the noise but doesn't effect the pulse rise-time. The filter includes an operational amplifier whose active elements are transistors Q_1, Q_2, Q_3, Q_4 and Q_5. The feedback impedance network consists of resistors R5 and R6 and capacitors C3 and C4. The input impedance network consists of resistors R1 and R2 and Capacitor C1. If the differentiating time constant of input network is set equal to the integrating time constant of the bridged-T network and R1-R2-R_a and R5 = R6 = R_b then the transfer function of the filter in the complex frequency domain becomes:

$$Z(S) = \frac{Ca\ (RaCa\ S + 1)}{(R_bC_b)^2\left(S^2 + R_bC_bS + 1\right)}$$

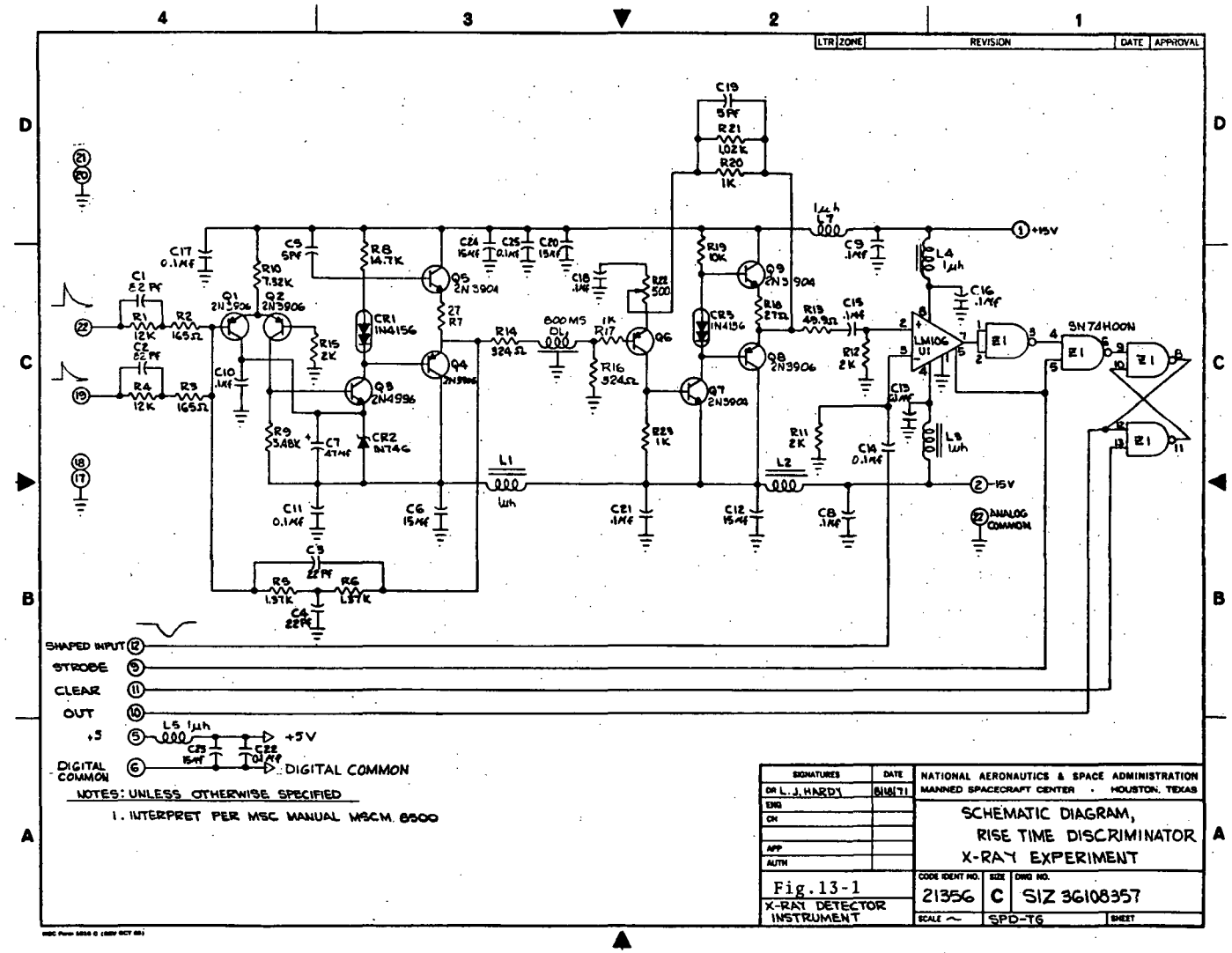


Figure 13-1. — Schematic Diagram, Rise-Time Discriminator

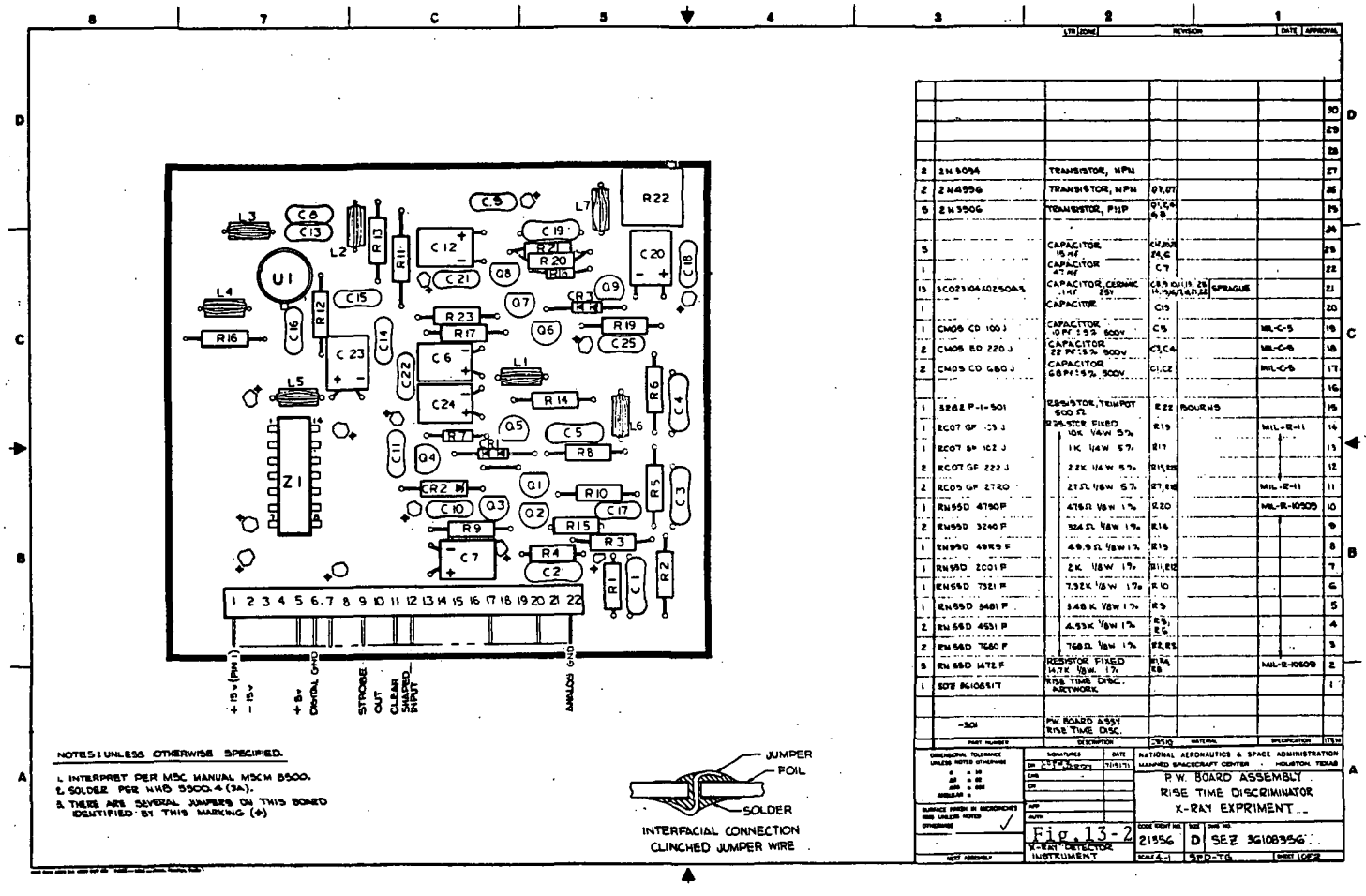


Figure 13-2. – P.W. Board Assembly, Rise-Time Discriminator

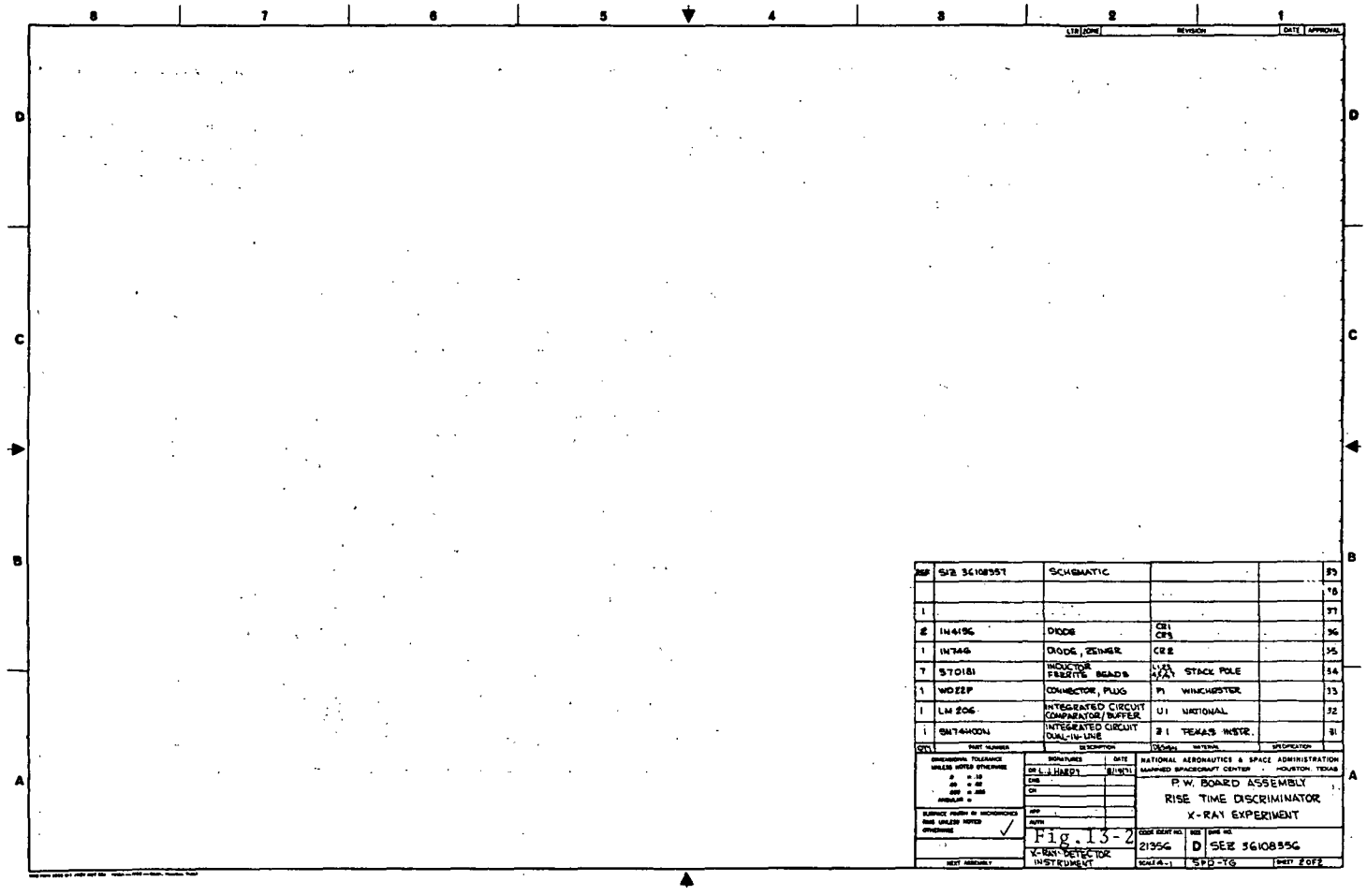


Figure 13-2. — (Concluded) P.W. Board Assembly, Rise-Time Discriminator

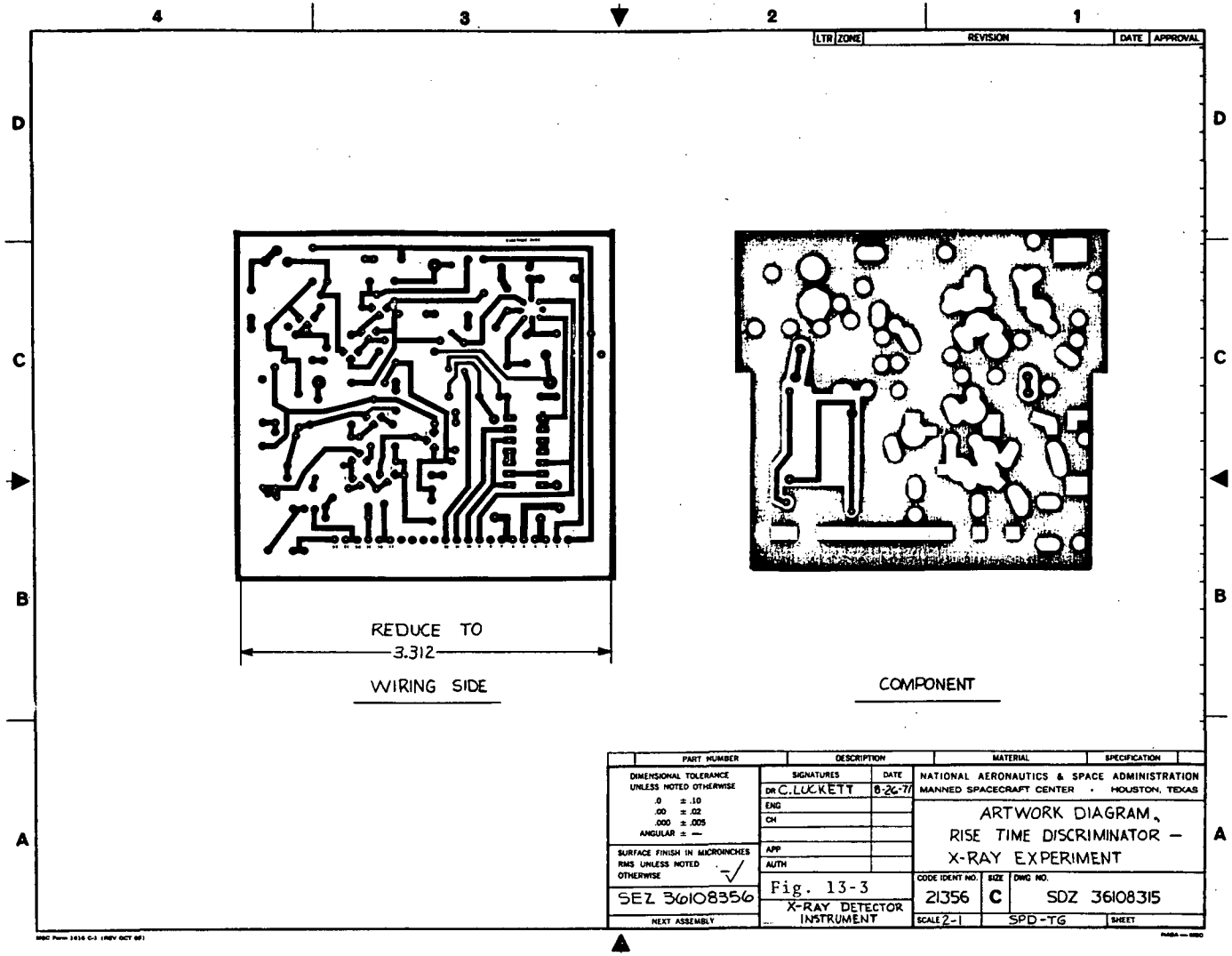


Figure 13-3. — Artwork Diagram, Rise-Time Discriminator

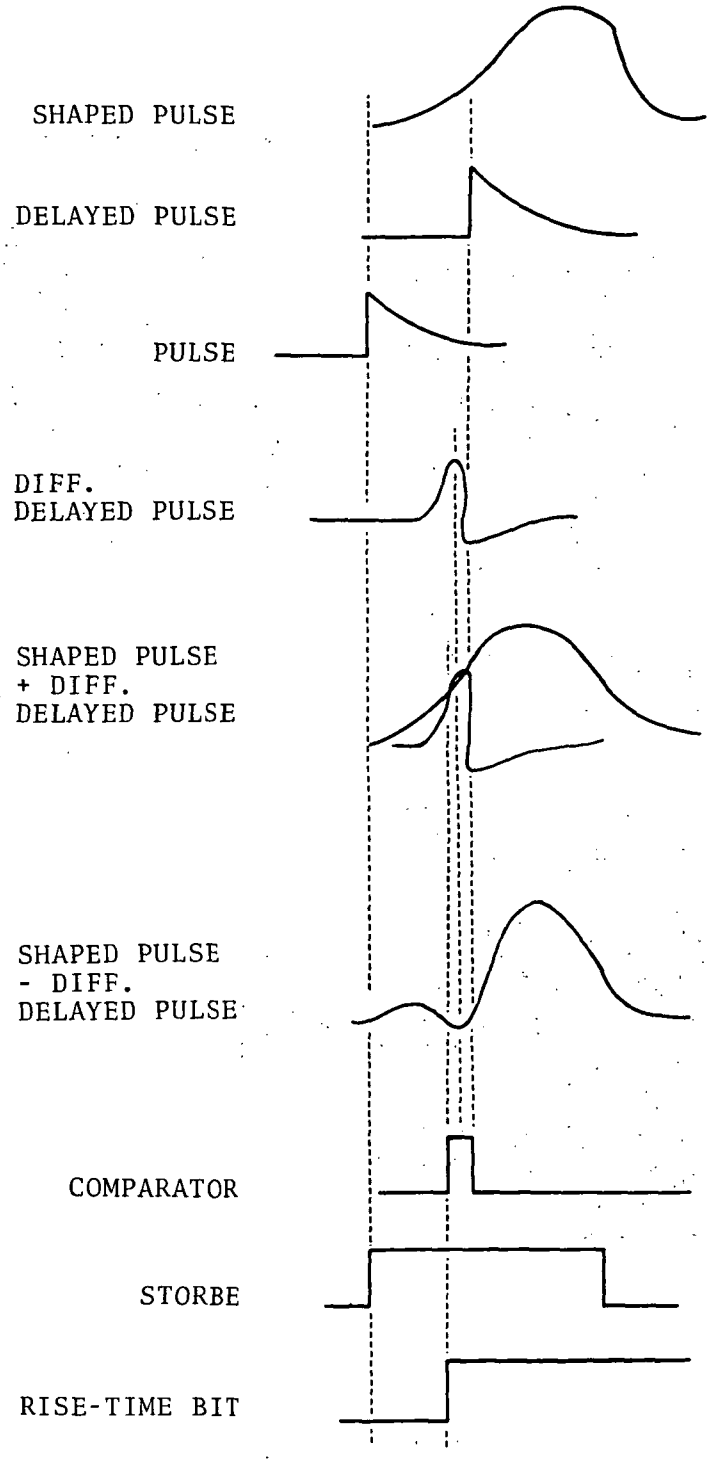


Figure 13-4. — Rise-Time Discriminator Timing Diagram.

After filtering, the rise time discrimination is performed by comparing the pulse height of a differentiated pulse with a shaped pulse whose pulse height is proportional to the pulse height of the undifferentiated pulse. This works because the rise time is proportional to the pulse slope. Before comparision the differentiated pulse is delayed 800 nanoseconds with respect to the shaped pulse so that the peak of the differentiated pulse occurs when the shaped pulse is at 50 percent of its peak value. The differentiator includes a non-inverting operational amplifier whose active elements are transistors Q6, Q7, Q8 and Q9, and a feedback network whose elements are capacitors C18 and C19 and resistors R20, R21 and R22. At the frequencies of interest (30 to 200 nanoseconds) the transfer function of the differentiation network becomes:

$$Z(S) = \frac{(R20 \,||\, R21)\ C18\ S}{R22} = 10^7\ S$$

The output latch is strobed to insure that the pulse height discriminator bit corresponds to the pulse being pulse height analyzed.

14. COINCIDENCE AND ANTICOINCIDENCE DISCRIMINATORS

If a pulse occurs in the A and B channels simultaneously, the comparators (AR1 and AR2) produce simultaneous pulses setting an output flip-flop and sending a positive coincidence data bit to the telemetry. If a pulse occurs in the anti-coincidence channel, an output flip-flop will be set sending a positive anticoincidence data bit to the telemetry.

The comparators' outputs are gated with the linear gate command insuring that discriminator bits correspond to a unique pulse analyzed by the Pulse Height Analyzer. The output flip-flop is reset with a CLEAR command from the telemetry interface.

The coincidence discriminator will send a logic "1" bit to the telemetry if ionization occurs simultaneously in two adjacent Main Detector Cells. The Anticoincidence Discriminators send a logic "1" bit to the telemetry if ionization occurs simultaneously in a Main Detector Cell and an Anticoincidence Detector Cell.

The schematic diagram, board assembly, printed circuit layout, and timing diagram are shown in Figures 14-1, 14-2, 14-3 and 14-4 respectively.

A1 and A2 in Figure 14-1 are comparators which produce positive logic pulses whenever the shaped pulses from the main "A" and main "B" detector sections go above a 25 milli-volts noise discrimination level set by potentiometer R4. If the two pulses occur simultaneously with the strobe pulse ($\overline{LG}$), the coincidence latch (Z2) will be set. If the

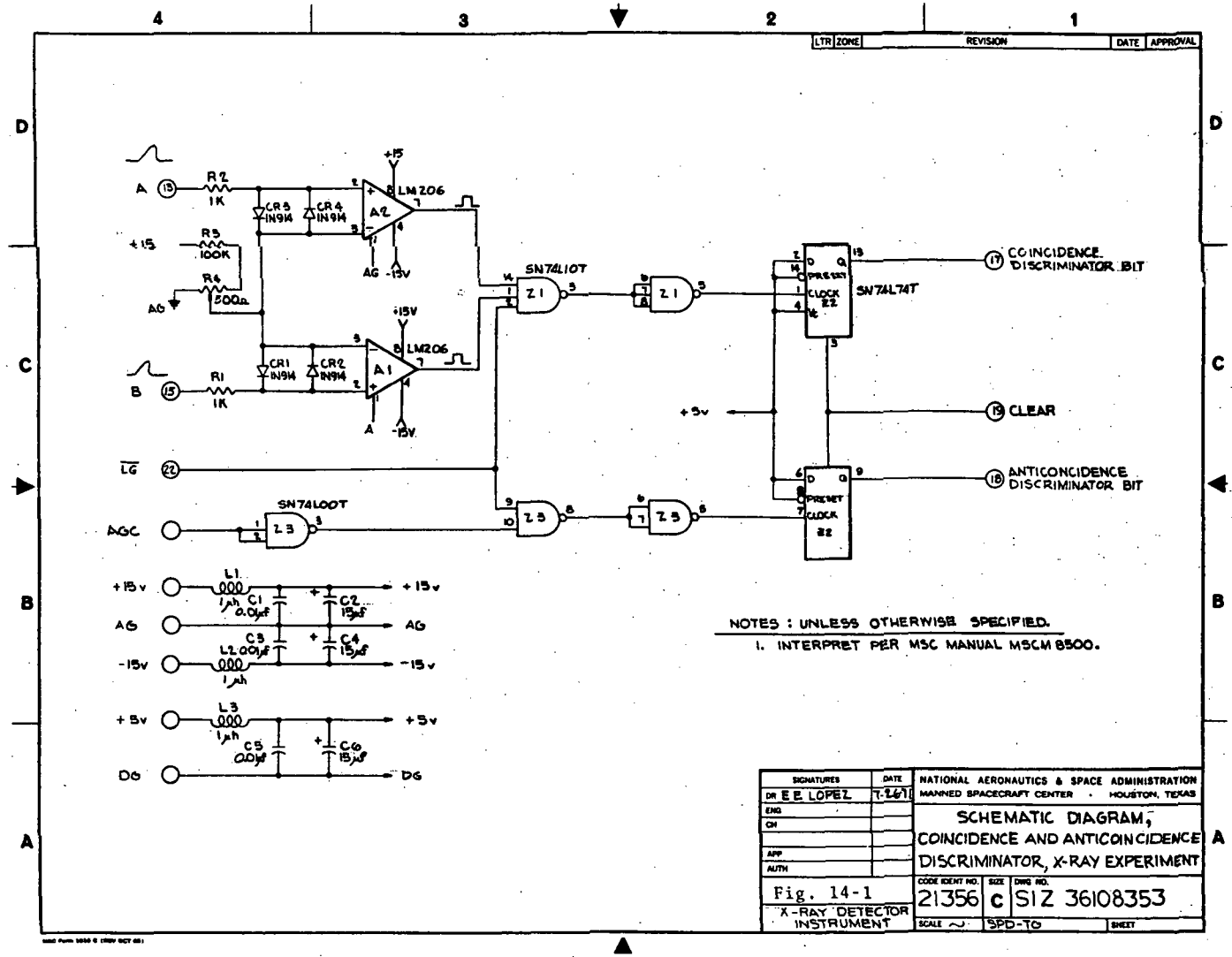


Figure 14-1. – Schematic Diagram, Coincidence and Anticoincidence Discriminator

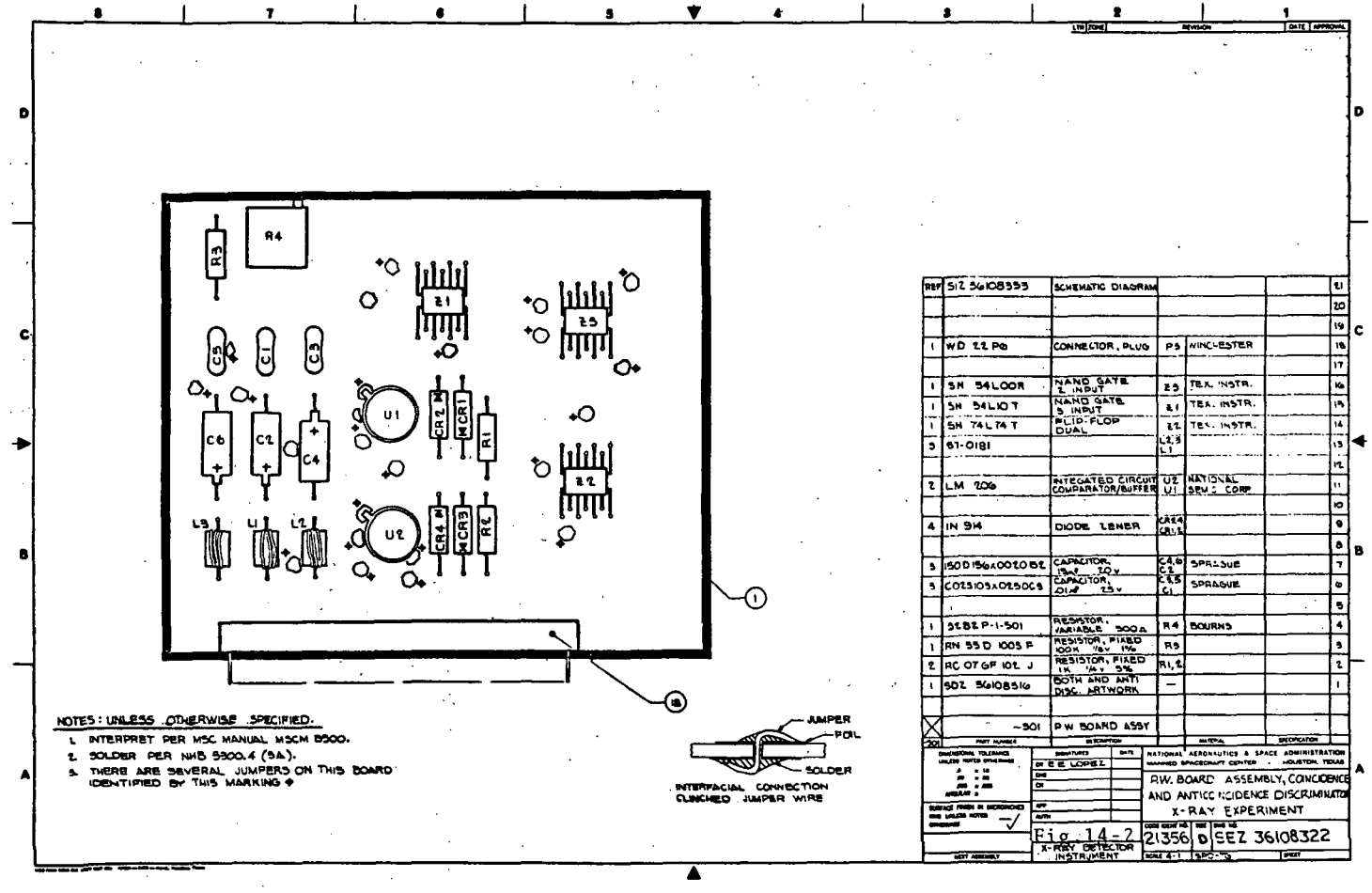


Figure 14-2. — P.W. Board Assembly, Coincidence and Anticoincidence Discriminator

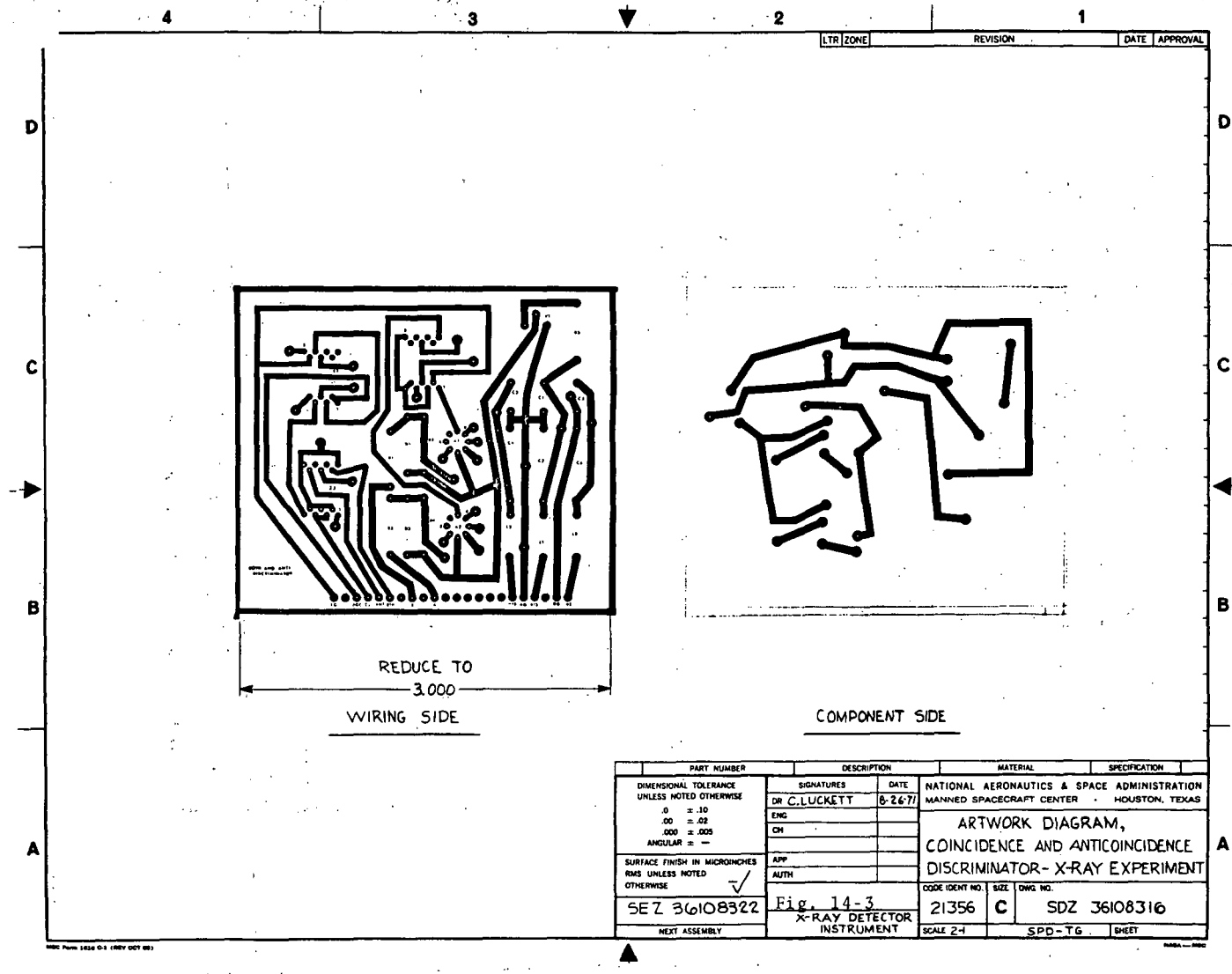


Figure 14-3. — Artwork Diagram, Coincidence and Anticoincidence Discriminator

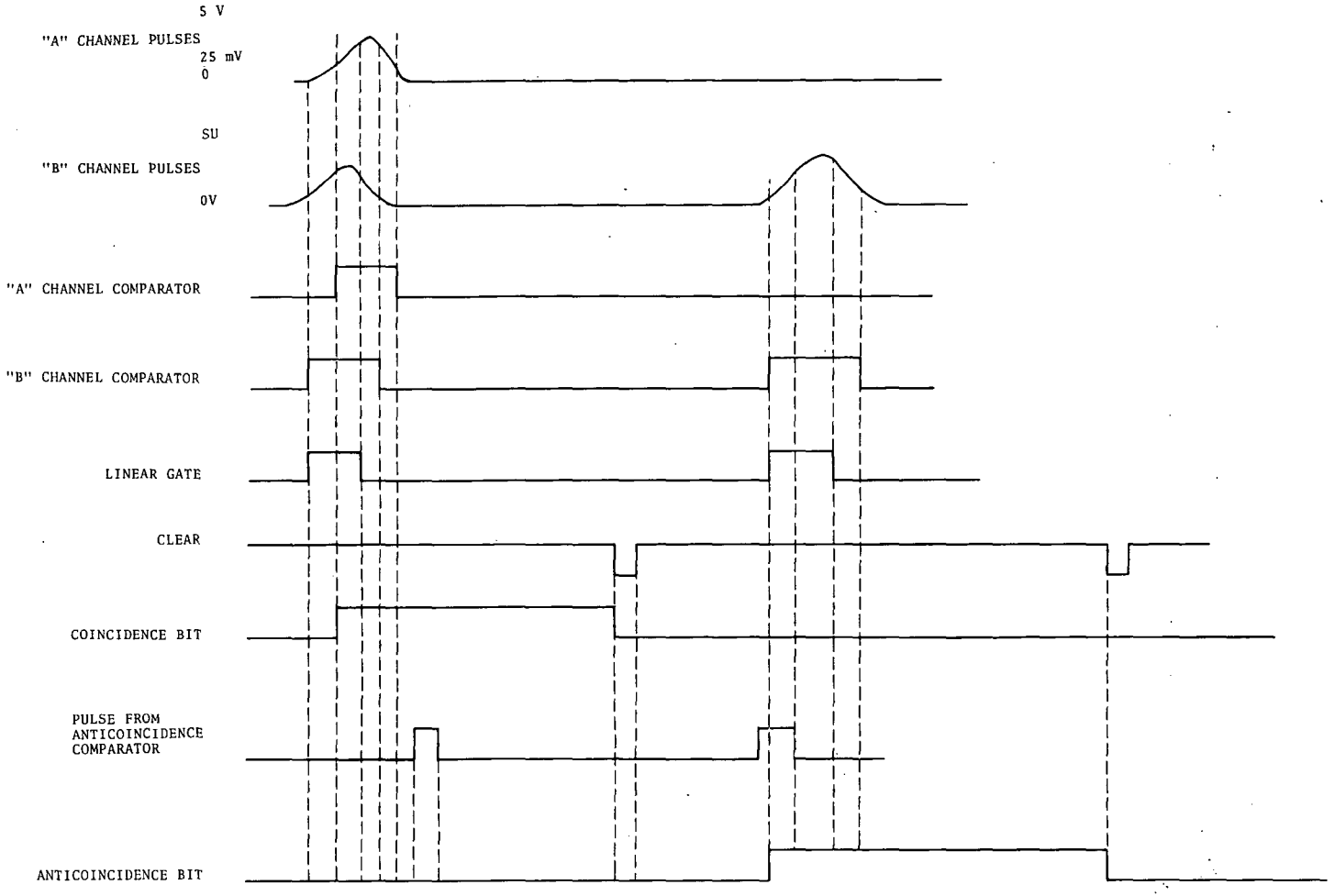


Figure 14-4. – Discriminator Timing Diagrams.

positive AGC discriminator pulse occurs simultaneously with the strobe pulse ($\overline{LG}$), the anticoincidence latch ($Z2_2$) will be set.

15. DC-TO-DC CONVERTER

The DC-to-DC Converter accepts a +24 volt to +32 battery input and supplies the electronics with plus and minus fifteen volts at 300 milliamperes. The output is regulated to within 0.1 percent DC with less than 5 millivolts of output ripple and less than 50 milliamperes current noise fed back on the line.

The schematic diagram is shown in Figure 15-1, the board assemblies in Figures 15-2 and 15-3, and the printed circuit layouts in Figures 15-4 and 15-5.

The power supply consists of a pre-regulator, a DC-to-DC Converter, and a post regulator. The pre-regulator, converts +24 volts to +32 volt input into a constant +21.5 volts at the output of series pass transistor Q_3. The DC-to-DC Converter converts the +21.5 volts into +18 volts and -18 volts at the output of the Π-filter sections. A two-transformer converter is used to increase the efficiency by saturating the smaller core but not the main core. The frequency of the converter oscillator is 10 kilohertz which is mainly controlled by characteristics of the transformer core. The oscillator feedback transformer (T2) has a 2:1 turns ratio which provides enough base-emitter voltage to saturate transistors Q5 and Q6 while providing 300 milliamperes emitter load. Q5 and CR5 are protection diodes. Capacitors C_2 and C_3 reduce the voltage spikes by slowing down the square wave rise time. Resistors R5 and R7 form a resistor divider for starting the oscillator. Zener diodes CR10 and CR11 protect the collector-emitter junctions of transistors Q5 and Q6. The post regulator consists of a Fairchild MA723 positive voltage regulator and a Motorola MC1563R negative voltage regulator which drops ±18 volts at the filter output into ±15 volts at the power supply output.

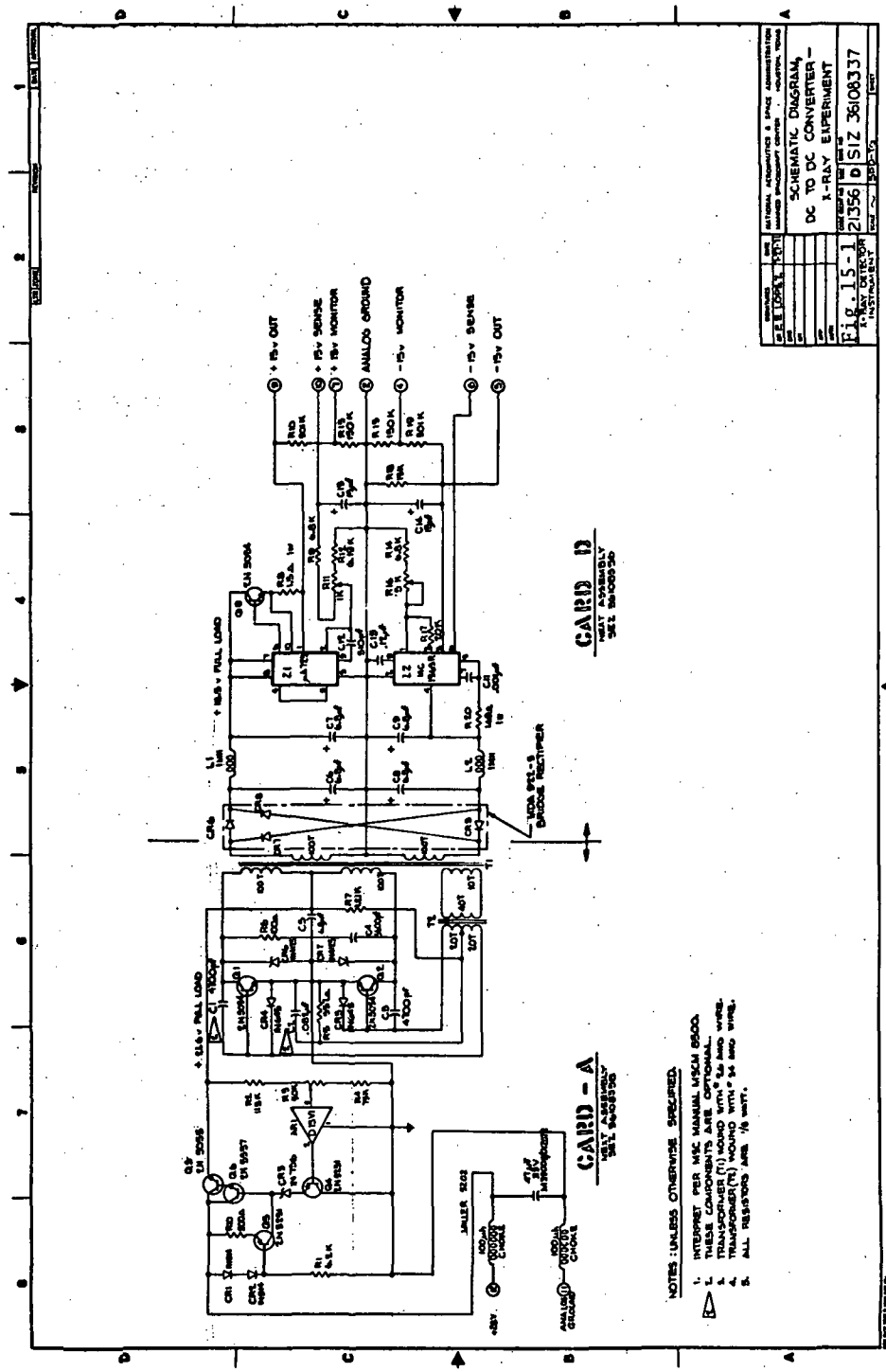


Figure 15-1. — Schematic Diagram, DC/DC Converter

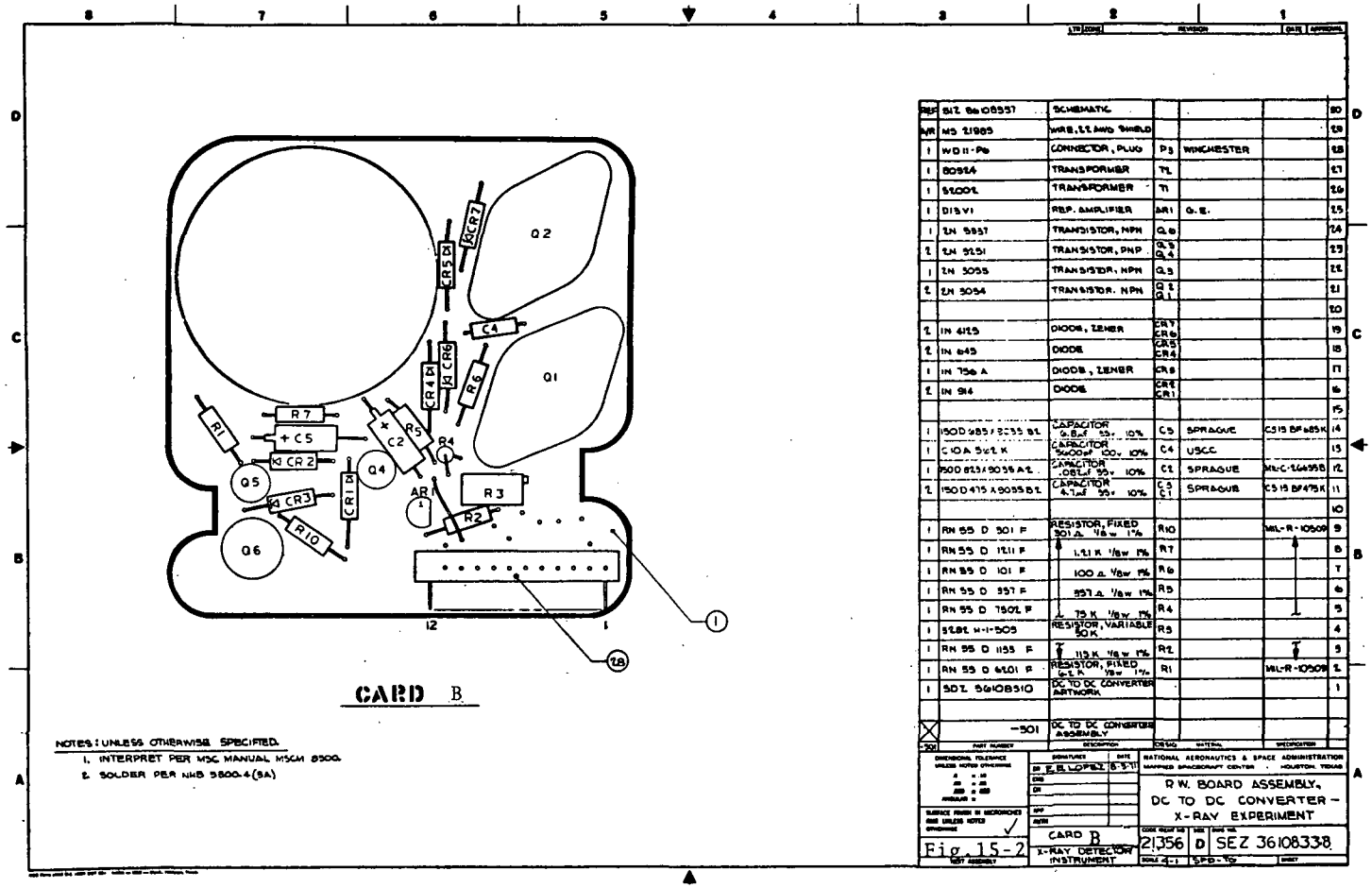


Fig. 15-2

Figure 15-2. — P.W. Board Assembly, (Card B) DC/DC Converter

DRAWING NOT AVAILABLE

Figure 15-3. – P.W. Board Assembly (Card D) DC/DC Converter

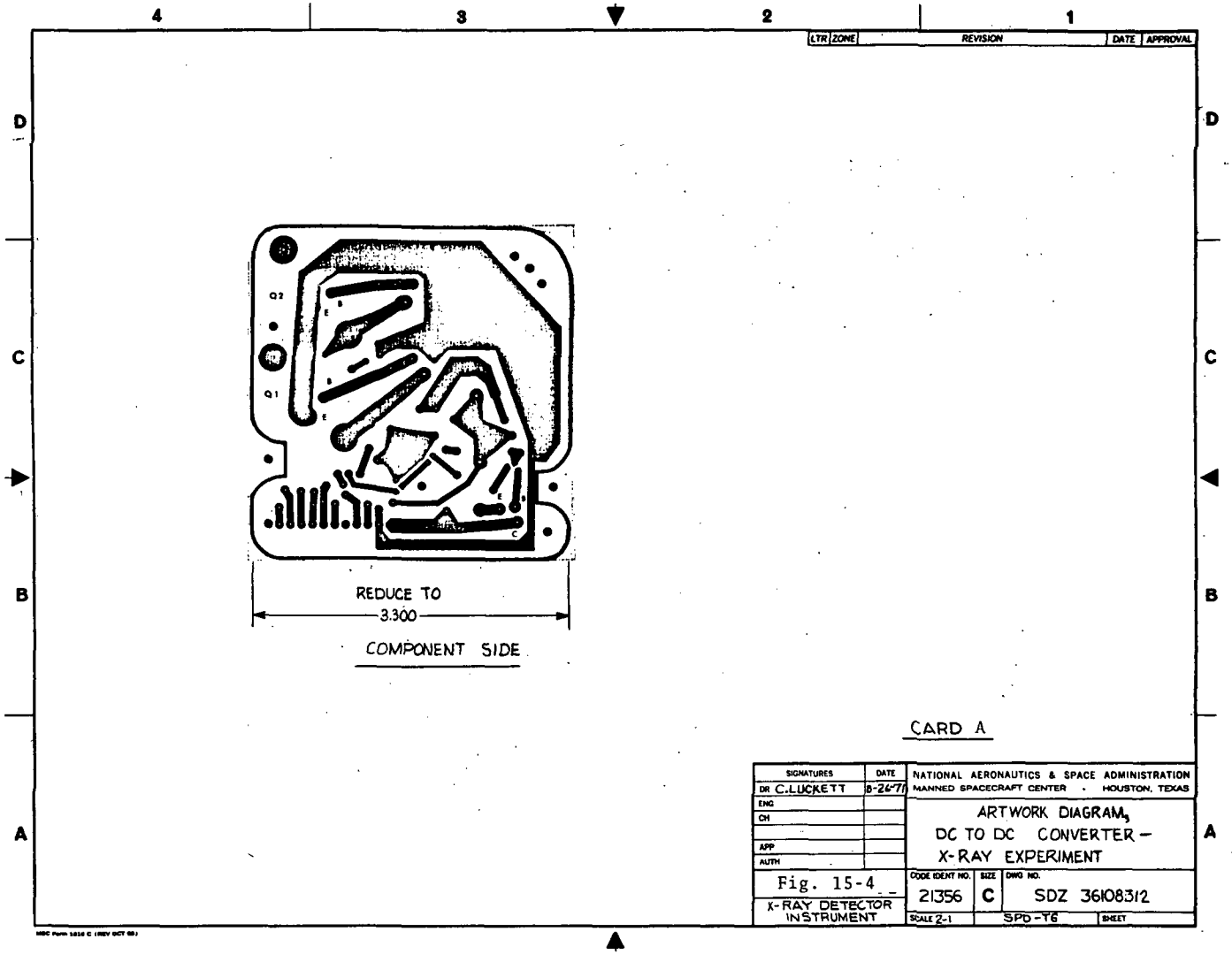


Figure 15-4. – Artwork Diagram (Card A), DC/DC Converter

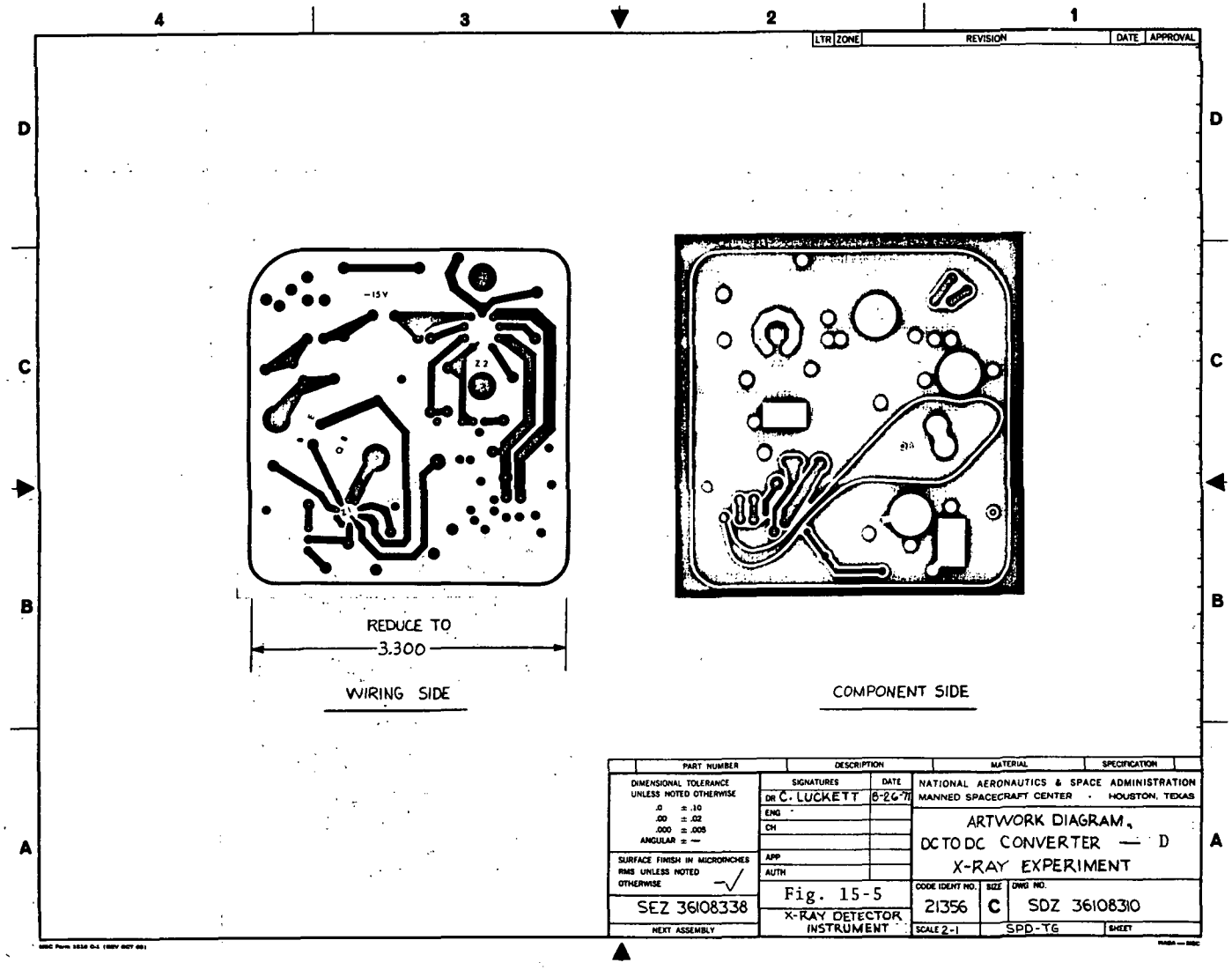


Figure 15-5. – Artwork Diagram (Card D), DC/DC Converter

16. TEST SET

16.1 Introduction

The test set allows rapid ground checkout of the proportional counter electronics. It provides power, simulates the telemetry, provides test pulses for the preamplifier test inputs, stores the pulse height data, and provides for nixie tube or digital printer readout of that data.

The Data Test Set supplies an interrogation signal to the instrument at 1 kHz rate. The data output from the instrument is monitored by the test set. The data is converted from a binary word to BCD for visual and printer monitoring. The data test set identifies the channel and accumulated counts for a selected number of interrogations.

Single channel monitoring is accomplished by using the manual mode of operation.

A selected group of channels can be monitored by using the automatic mode of operation. The selected group of channels are sequentially monitored with each channel being interrogated with a fixed number of interrogations as determined by the operator.

The five prime data bits are converted to channels 1 through 32. The three diagnostic data bits consist of the rise time discriminator signal (channel 33), the coincidence discriminator signal (channel 34), and the anticoincidence discriminator signal (channel 35).

The block diagram of the Data Test Set is shown in Figure 16-1.

The housekeeping test set supplies +28 VDC and +5 VDC to the instrument in the DC power "External" Mode. The housekeeping test set has two monitoring modes of operation. The power mode monitors the external voltages, instrument current drains, and internal voltages applied from another source. The Analog Mode monitors voltages supplied to the instrument and detector housekeeping signals.

The block diagram of the Housekeeping Test Set is shown in Figure 16-2.

16.2 Front Panel Control Functions

16.2.1 Data Test Set

16.2.1.1 POWER switch. Supplies power to the system when in the ON position. Power lamp will indicate system power status.

16.2.1.2 MODE switch. Selects the desired mode of operation (Automatic or Manual).

16.2.1.3 START switch. Starts system operation.

16.2.1.4 STOP switch. Stops system operation.

16.2.1.5 AUTO. STOP switch. Stops system operation after completion of cycle.

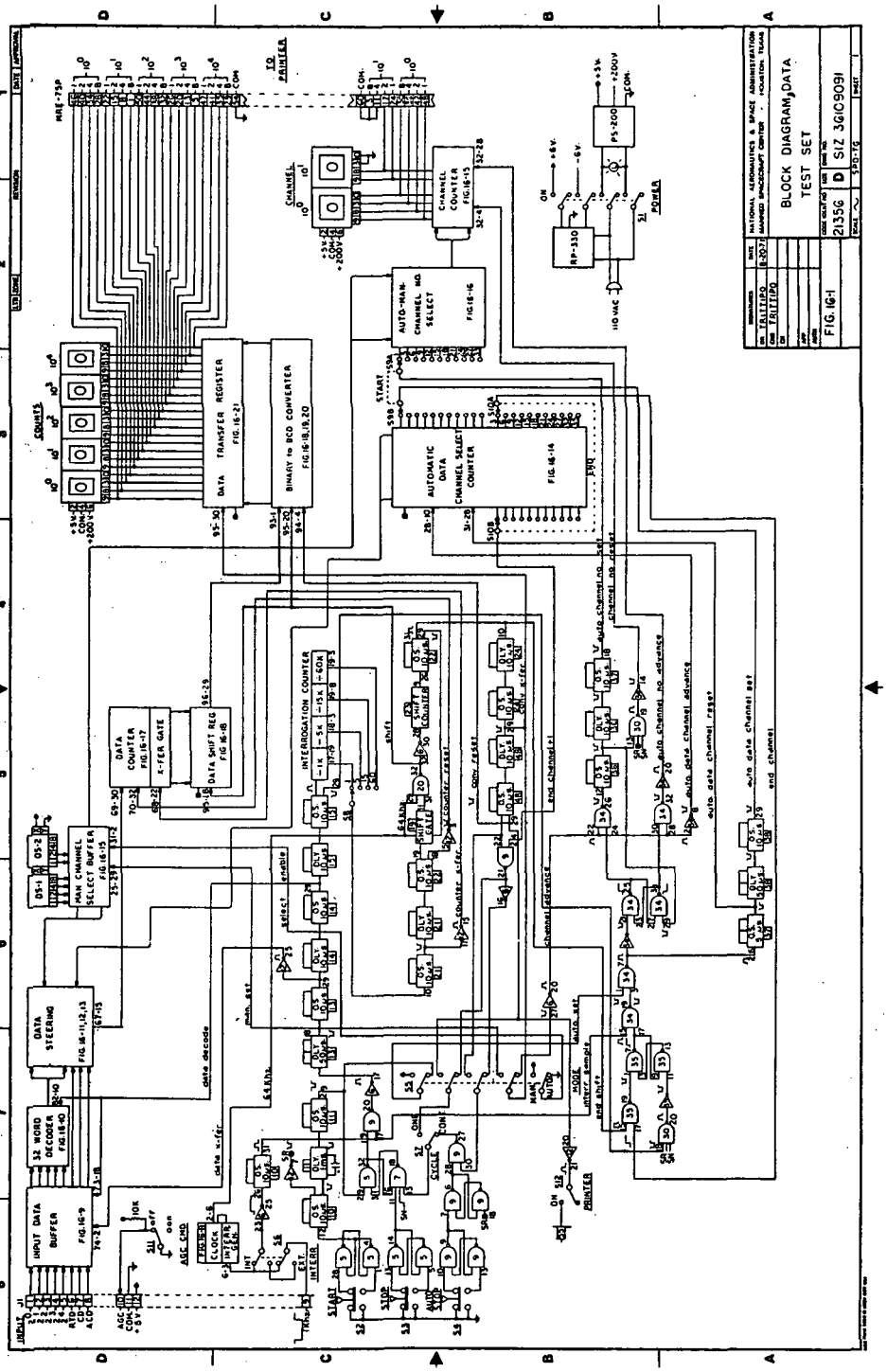


Figure 16-1. — Block Diagram, Data Test Set

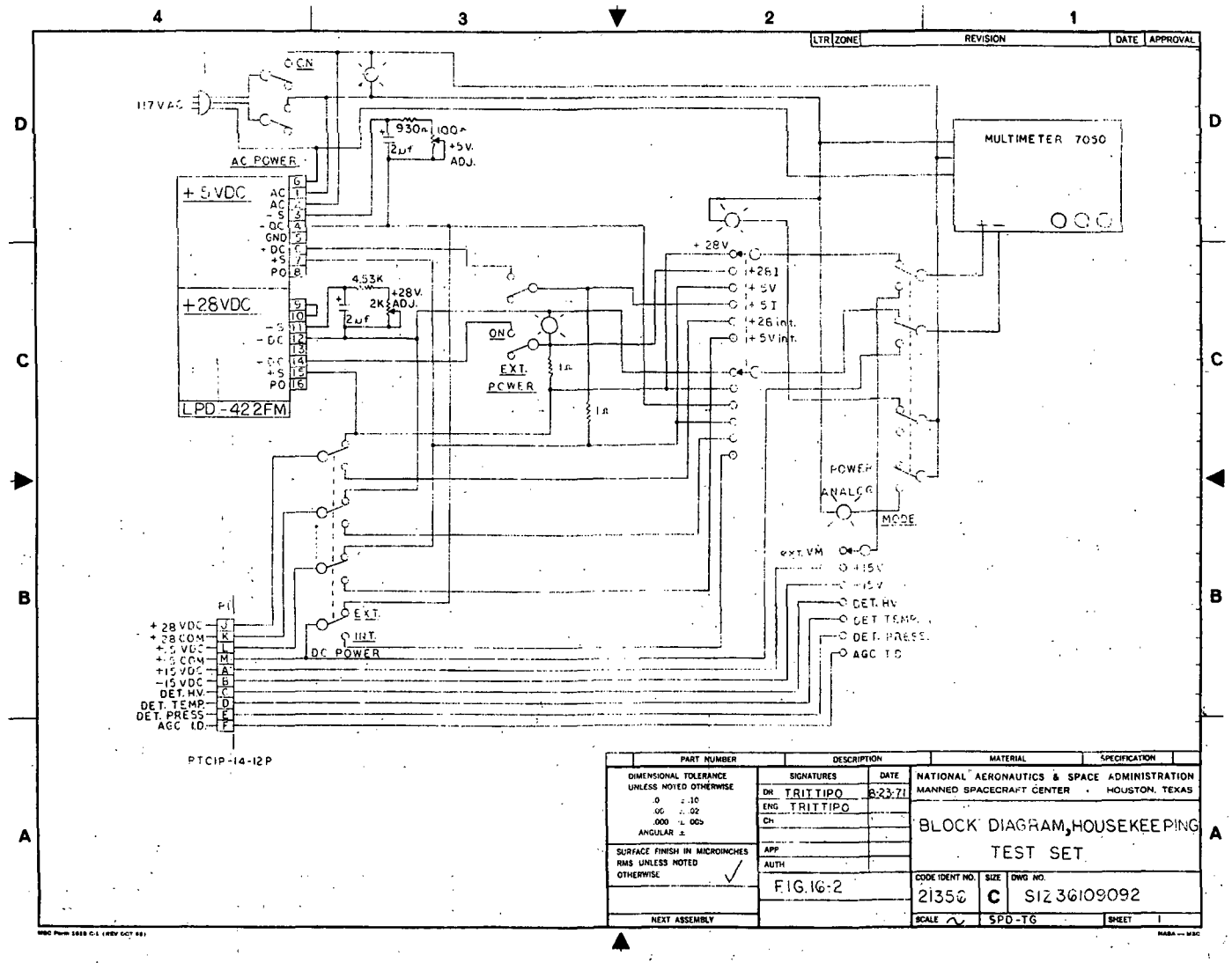


Figure 16-2. – Block Diagram, Housekeeping Test Set

16.2.1.6 CHANNEL START selector. Selects the first channel to be monitored in the Automatic Mode of operation.

16.2.1.7 CHANNEL END selector. Selects the last channel to be monitored in the Automatic Mode of operation.

16.2.1.8 CYCLE, SINGLE/CONTINUOUS switch. In the Single Mode, the system will cycle through the selected channels and stop. In the Continuous Mode, the system will continue to recycle through the selected channels and stop only on a STOP or AUTO. STOP command.

16.2.1.9 INTERROGATIONS/CYCLE ($x10^3$) switch. Selects the desired number of interrogations per channel cycle. This system's interrogation rate is set at 1 kHz, therefore a selection of 1, 5, 15, or 60 seconds is available.

16.2.1.10 INTERROGATE INT./OFF/EXT. switch. Controls the INTERROGATION command. INT. is supplied by the test set and is at a 1 kHz rate. EXT. can be supplied from an external source but can not be greater than a 2 kHz rate (high to low signal compatible with 5 v logic).

16.2.1.11 AGC CMD switch. Supplies a PRINT COND. signal to the printer when in the ON position.

16.2.2 Housekeeping Test Set

16.2.2.1 AC POWER switch. Supplies AC power to the +5 VDC and +28 VDC power supplies when in the ON position. The power lamp indicates that AC power is on.

16.2.2.2 EXT. POWER switch. When in the ON position, it makes +5 VDC and +28 VDC available to the DE POWER switch.

16.2.2.3 DC POWER switch. When in the EXT. position, it provides +5 VDC and +28 VDC to plug P1. When in the INT. position, it exempts +5 VDC and +28 VDC from P1 for monitoring.

16.2.2.4 POWER/ANALOG MODE switch. When in the Power Mode, it specifies the selected power positions to be monitored by the multimeter. When in the Analog Mode, it specifies the selected analog positions to be monitored by the multimeter.

16.3 Operation Procedures

16.3.1 MANUAL MODE of Operation

16.3.1.1 Connect the data and housekeeping cables between the test sets and the instrument.

16.3.1.2 Insure that the EXT. POWER switch is off on the Housekeeping Test Set and then turn on the AC POWER switch. Switch the MODE switch to POWER and monitor the +5 VDC and +28 VDC on the multimeter. Make screwdriver adjustments as necessary. If test set power is to be supplied to the instrument, position the DC POWER switch to the EXT. position.

16.3.1.3 Turn the EXT. POWER switch to ON and monitor +28 VDC, +28 I, +5 VDC, and +5 I with multimeter. +28 I should read approximately 0.540 and +5 I should read approximately 0.510.

16.3.1.4 Switch the MODE switch to ANALOG and monitor the analog signals on the multimeter. Note, all analog signal levels will be between 0 and 5 VDC. The signal level monitored in volts will be a percentage of the maximum signal with 5 VDC being equal to 100 percent.

16.3.1.5 Turn the power supply (RP-330) on.

16.3.1.6 Turn the Data Test Set POWER switch to ON and set the MODE switch to MANUAL.

16.3.1.7 Set INTERROGATIONS/CYCLE to the desired number of interrogations.

16.3.1.8 Set the INTERROGATE switch to either INT. or EXT. If using the EXT. mode, refer to 16.2.1.10 for signal specifications.

16.3.1.9 Set the CYCLE switch to either SINGLE or CONTINUOUS. Refer to 16.2.1.8 for details.

16.3.1.10 Set the CHANNEL SELECT switch to the desired channel.

16.3.1.11 If printout is desired, turn the PRINT CMD. on. (Insure that the printer power is on and check the printer for paper.)

16.3.1.12 If the AGC section of the instrument is to be checked, turn the AGC CMD to ON.

16.3.1.13 Push the START switch for system operation. Note: If the CYCLE switch is in the SINGLE cycle position, the selected channel will be interrogated for the selected number of interrogations, display the channel number and counts on the visual display, print the channel number and counts, and stop the system automatically. To monitor the same channel again, a START CMD. is required. If the CYCLE switch is in the CONTINUOUS cycle position, the selected channel will be monitored until a STOP or AUTO. STOP command is given.

16.3.2 AUTOMATIC MODE of Operation

Set the system controls in the same positions as for the Single Mode of operation with the following exceptions:

16.3.2.1 Set the MODE switch to the automatic position.

16.3.2.2 Set the CHANNEL START and END switches to the channels desired to be monitored.

16.3.2.3 Start and stop the system operation in the same manner as for the Manual Mode of operation.

16.4 Theory of Operation

The Data Test Set electronics system is constructed using Honeywell μ-Pac I/C modules. A block diagram of the system is shown in Figure 16-1. The module location is shown in Figure 16-3.

A 1 kHz 50 percent duty cycle Interrogation signal is provided to interrogate the instrument. Upon interrogation,

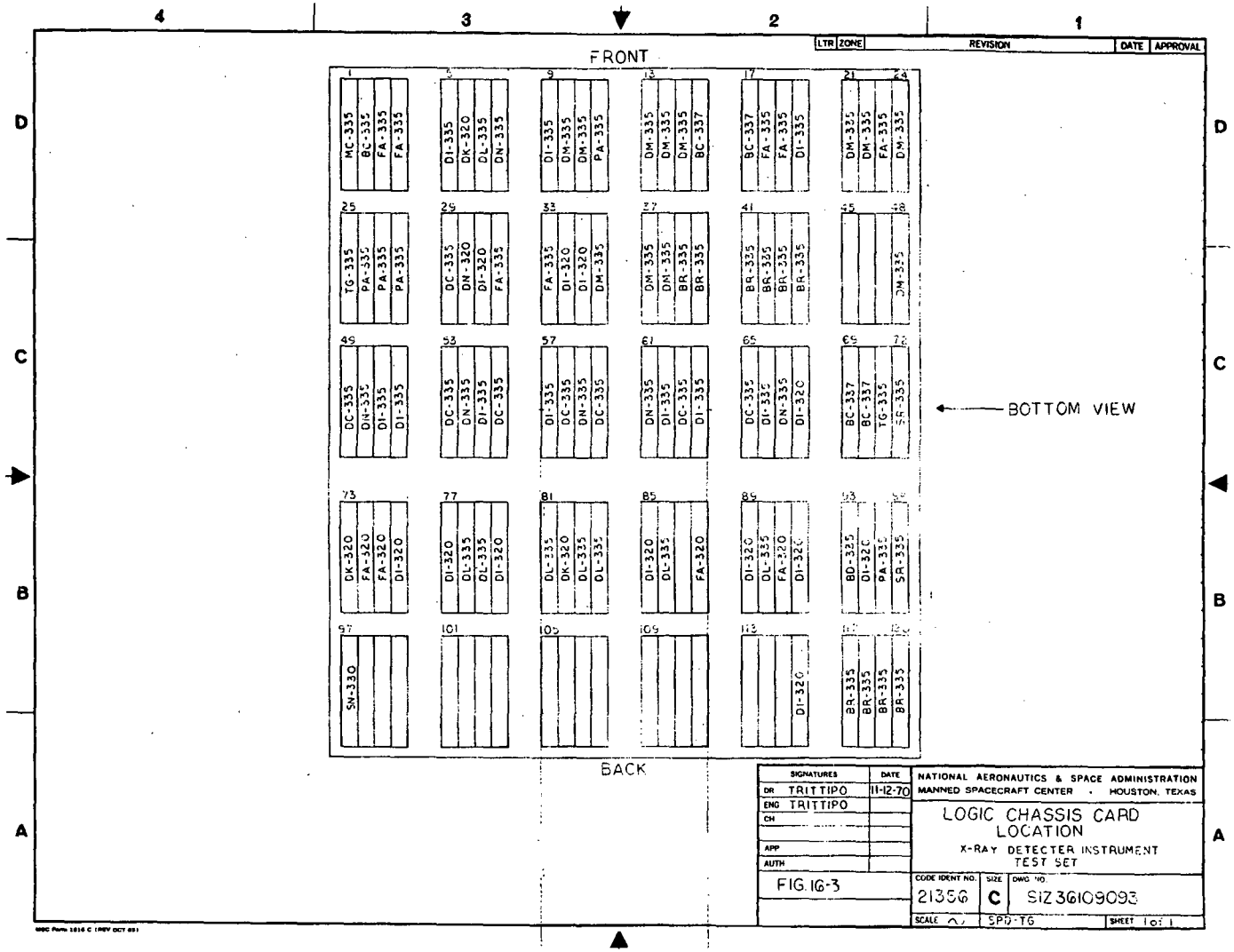


Figure 16-3. – Logic Chassis Card Location

the instrument provides the prime and diagnostic data to the input (J1). On the leading edge of each Interrogation signal a 10 μsec. pulse is generated as an interrogation sample in the control circuits of the test set.

Control signal flow charts, shown in Figures 16-4 and 16-5, may be used as an aid in following the operation of the system. System control circuits are shown in Figures 16-6, 16-7 and 16-16.

On the initiation of a START command (S2), a 10 μsec. signal is generated and used as a system reset (SR). This signal is delayed approximately 1 μsec. and then used as a SYSTEM START command and an AUTOMATIC SET command.

The SYSTEM START command sets latch 5-32, enabling Gate 9-19 to accept the interrogation sample signal. When the system is used in the AUTOMATIC MODE, the SYSTEM START command provides an AUTOMATIC SET command through S5.

After enabling Gate 9-19, each interrogation sample is delayed 50 μsec. and then generates a 10 μsec. pulse used as the Data Transfer signal at 12-25. This signal is delayed 10 μsec. and then generates a 10 μsec. pulse used as the Data Decode signal at 14-29. The Data Decode signal is delayed 10 μsec. and then generates a 10 μsec. pulse used to advance the Interrogation Counter (Figure 16-8) and also as a CONTROL command for the Automatic Mode. The Data Transfer signal transfers the input data at J1 to the input data buffer shown in Figure 16-9. The 50 μsec. dalay between the start of interrogation and the Data Transfer signal allows settling time for the data presented at the instrument output.

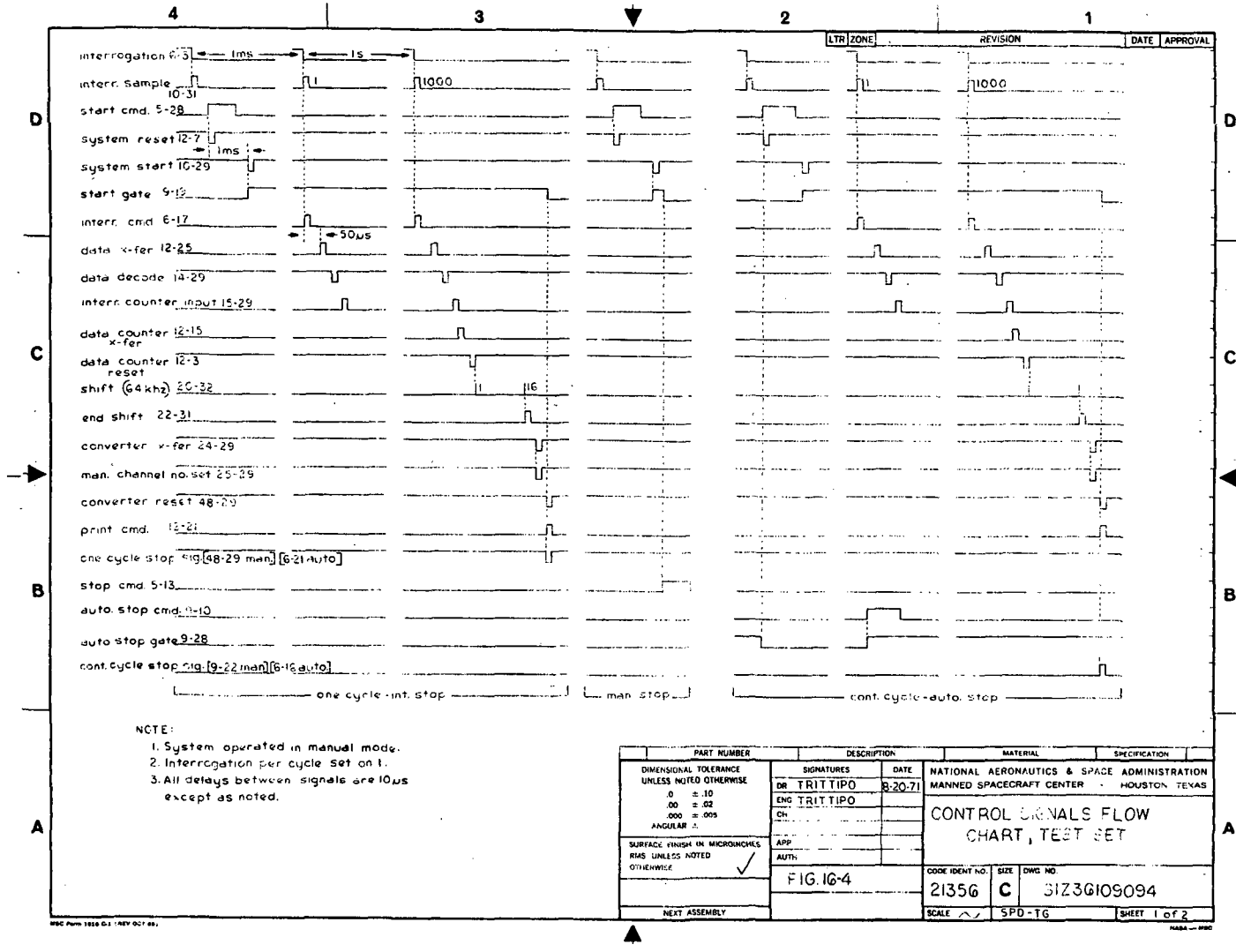


Figure 16-4. – Control Signals Flow Chart

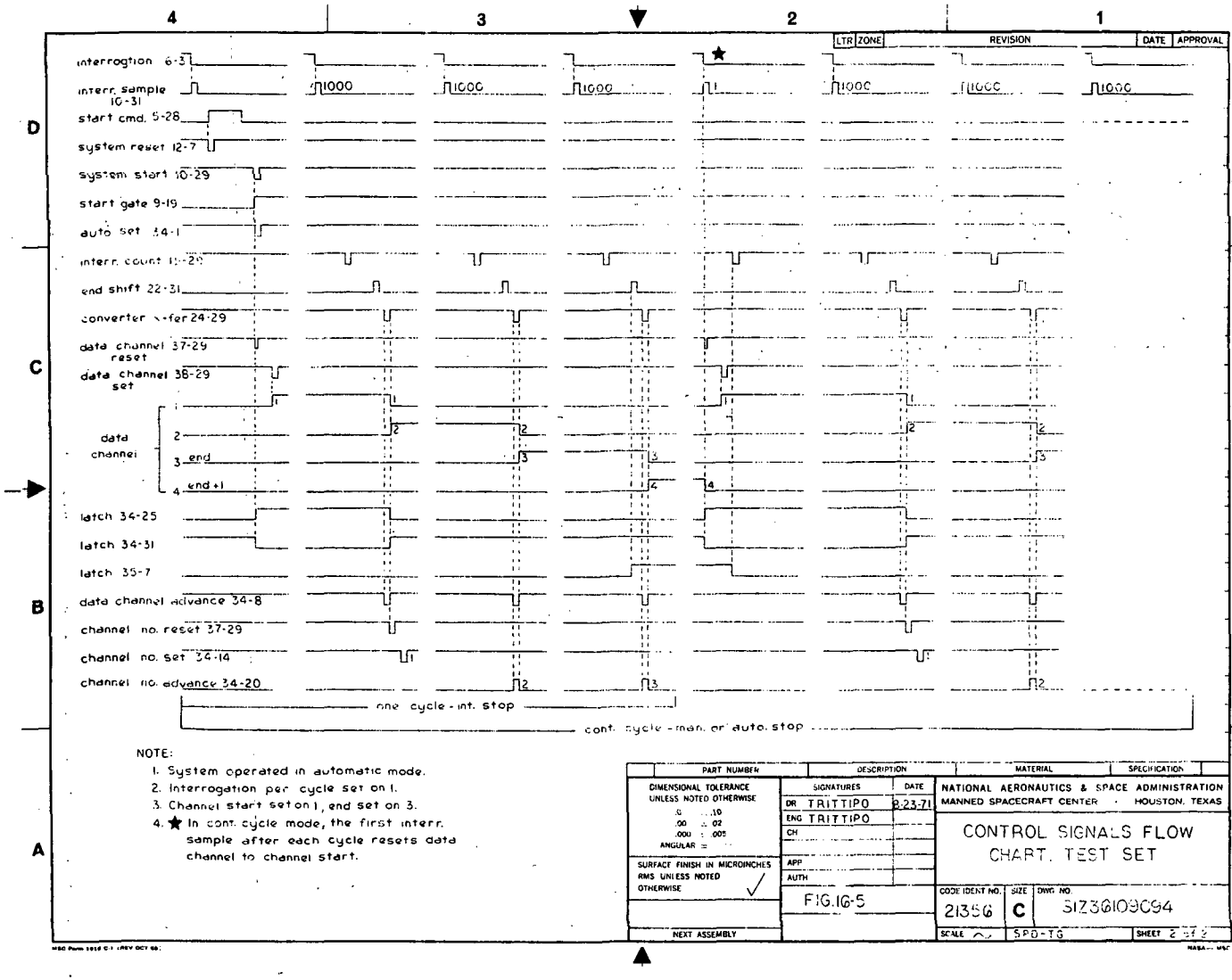


Figure 16-5. – Control Signals Flow Chart

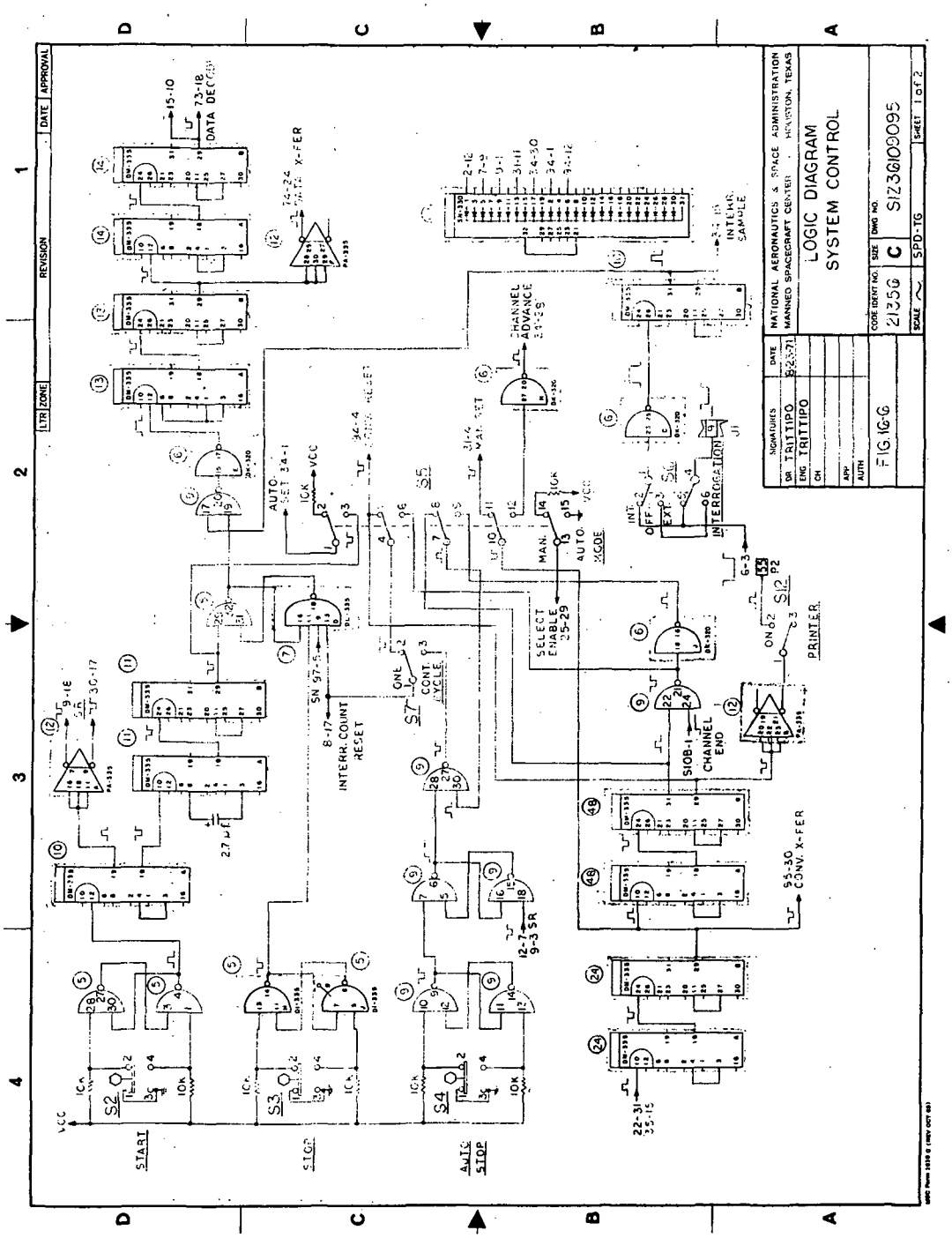


Figure 16-6. — Logic Diagram, System Control

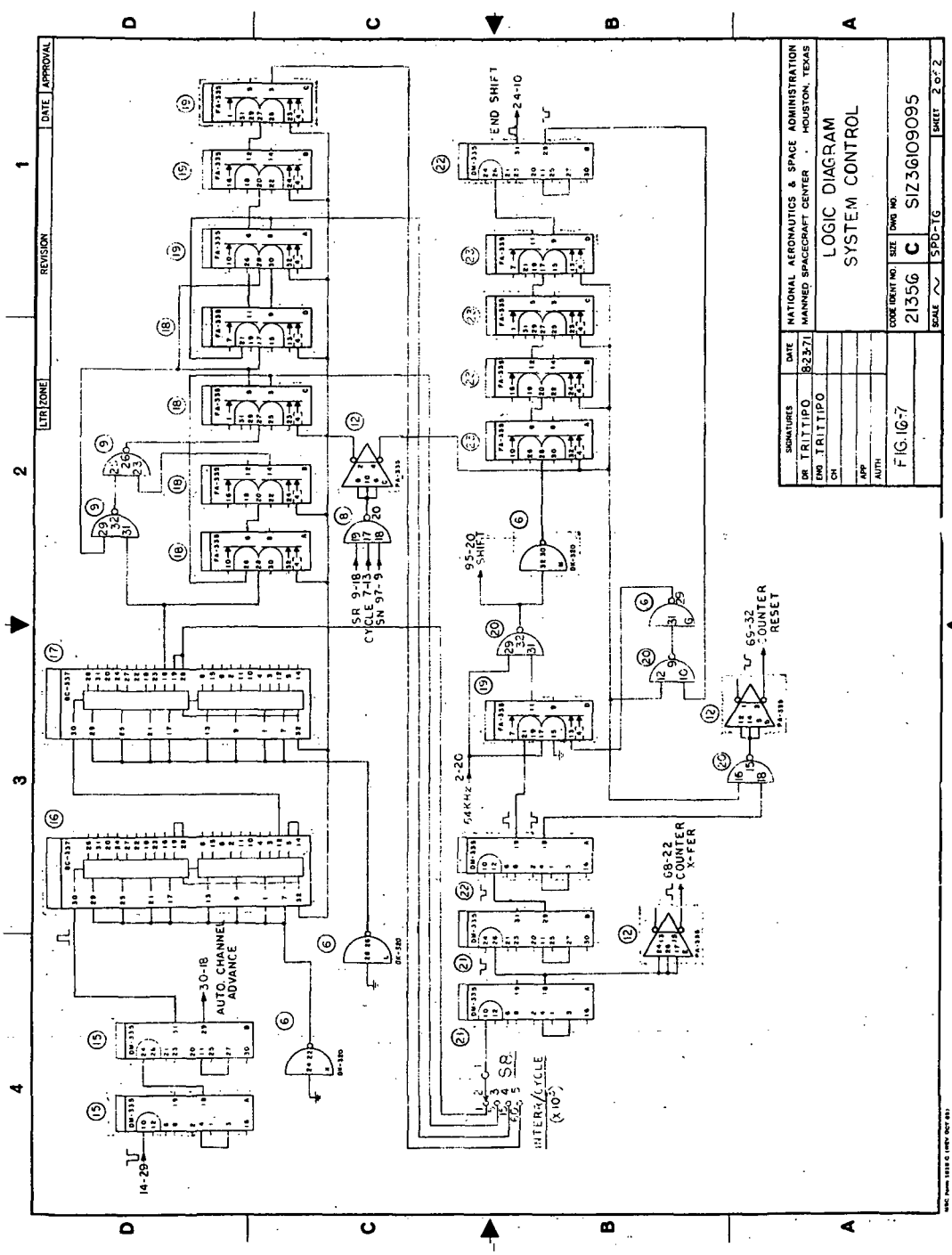


Figure 16-7. — Logic Diagram, System Control

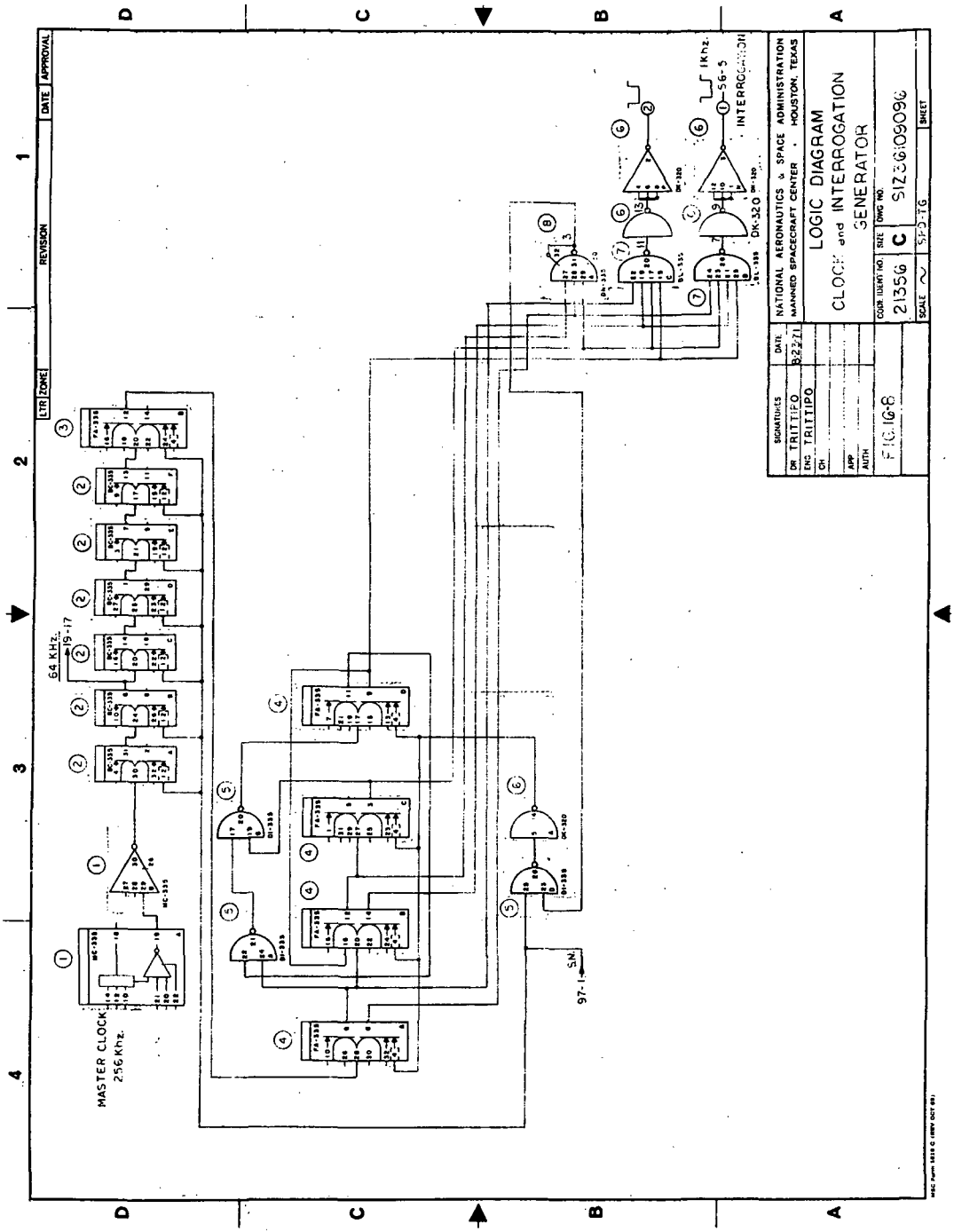


Figure 16-8. – Logic Diagram, Clock and Interrogation Generator

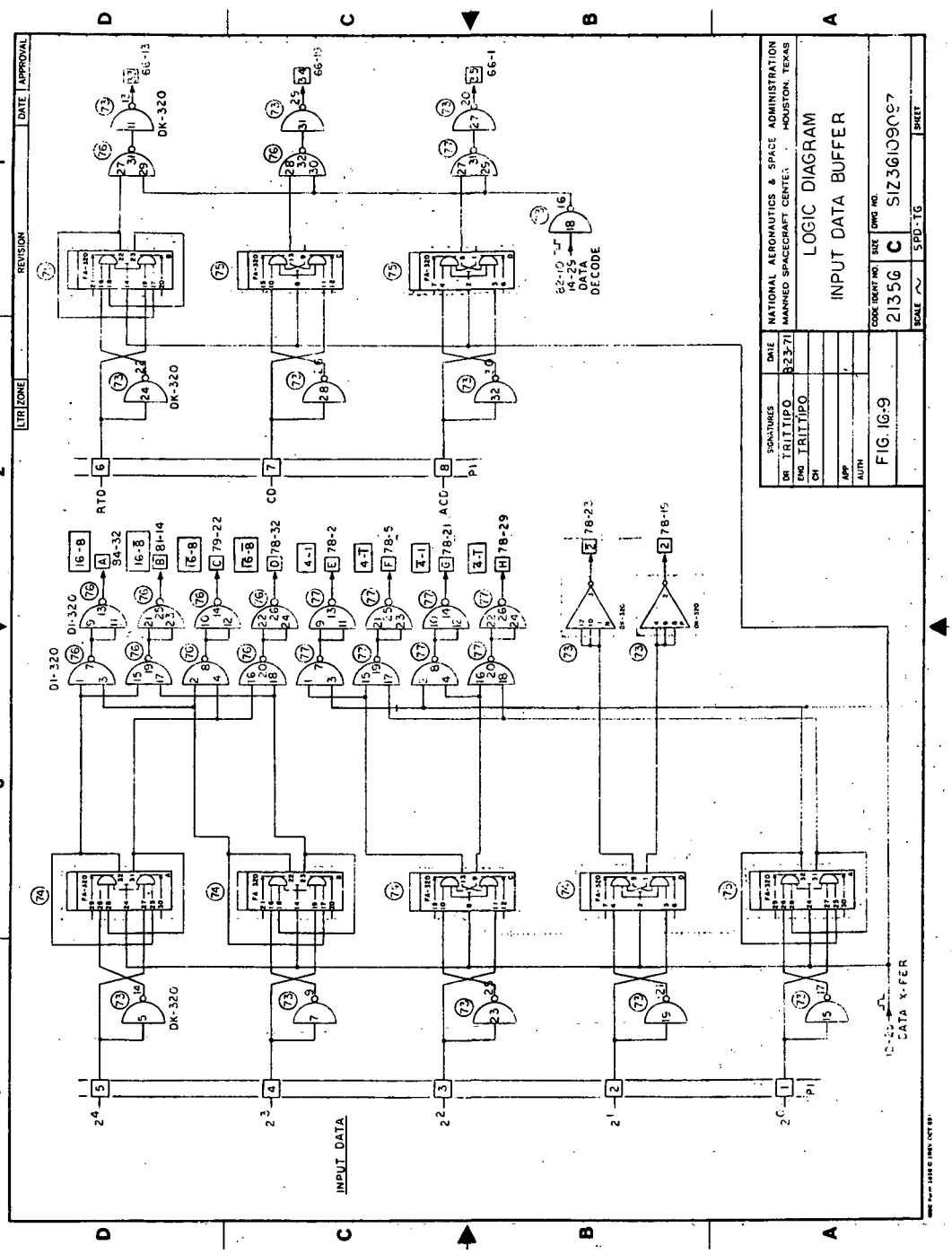


Figure 16-9. – Logic Diagram, Input Data Buffer

The five prime data bits from the input data buffer are presented to a 32-word decoder (Figure 16-10). Upon a Data Decode signal, the decoded prime data and the three diagnostic bits are presented to the data steering circuit (Figures 16-11, 16-12, and 16-13).

The function of the data steering circuit is to select the data channel to be monitored, either manually or automatically (Figures 16-14, 16-15 and 16-16) and steer the selected data to the Data Counter (Figure 16-17).

After a preselected number of interrogations have been counted (determined by the position of the interrogations/cycle switch S8), a 10 μsec. pulse is generated and used as the COUNTER TRANSFER command (12-15) Figure 16-7. This command transfers the accumulated counts in the data counter to the data shift register (Figure 16-18).

The COUNTER TRANSFER command is delayed 10 μsec. and then generates a 10 μsec. pulse used as the shift gate enable and COUNTER RESET command. The COUNTER RESET command resets the data counter. The shift gate enables a 64 kHz. Clock signal to shift the data out of the data shift register (Figure 16-18) and into the Binary to BCD converter (Figures 16-18, 16-19 and 16-20). This command is also monitored by a 16-bit shift counter. At the end of the 16-bit shift, a 10 μsec. pulse is generated to disable the shift gate shutting off the 64 kHz clock.

The end shift command is delayed 10 μsec. and then generates a 10 μsec. pulse used as the CONVERTER TRANSFER command. The

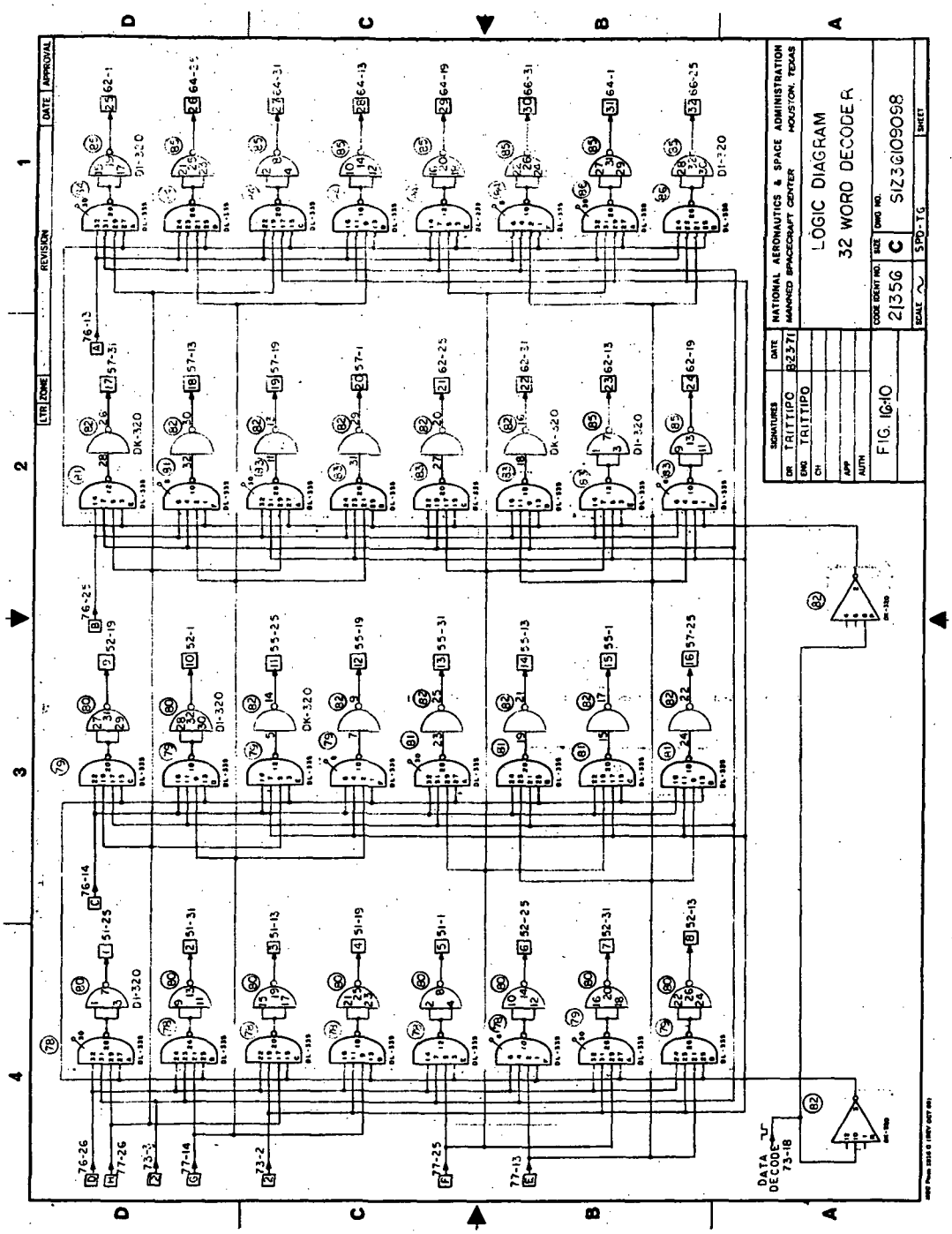


Figure 16-10. – Logic Diagram, 32 Word Decoder

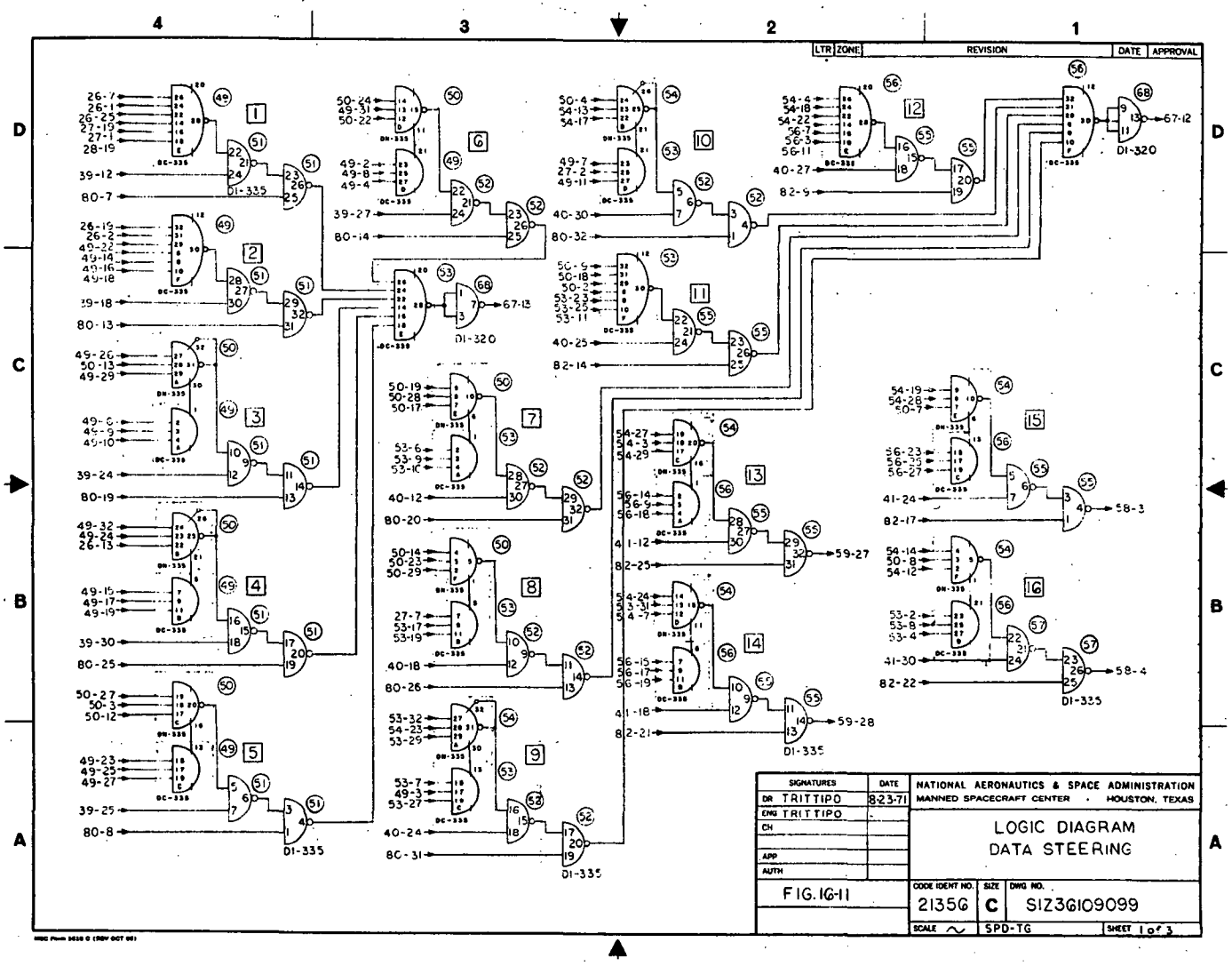


Figure 16-11. – Logic Diagram, Data Steering

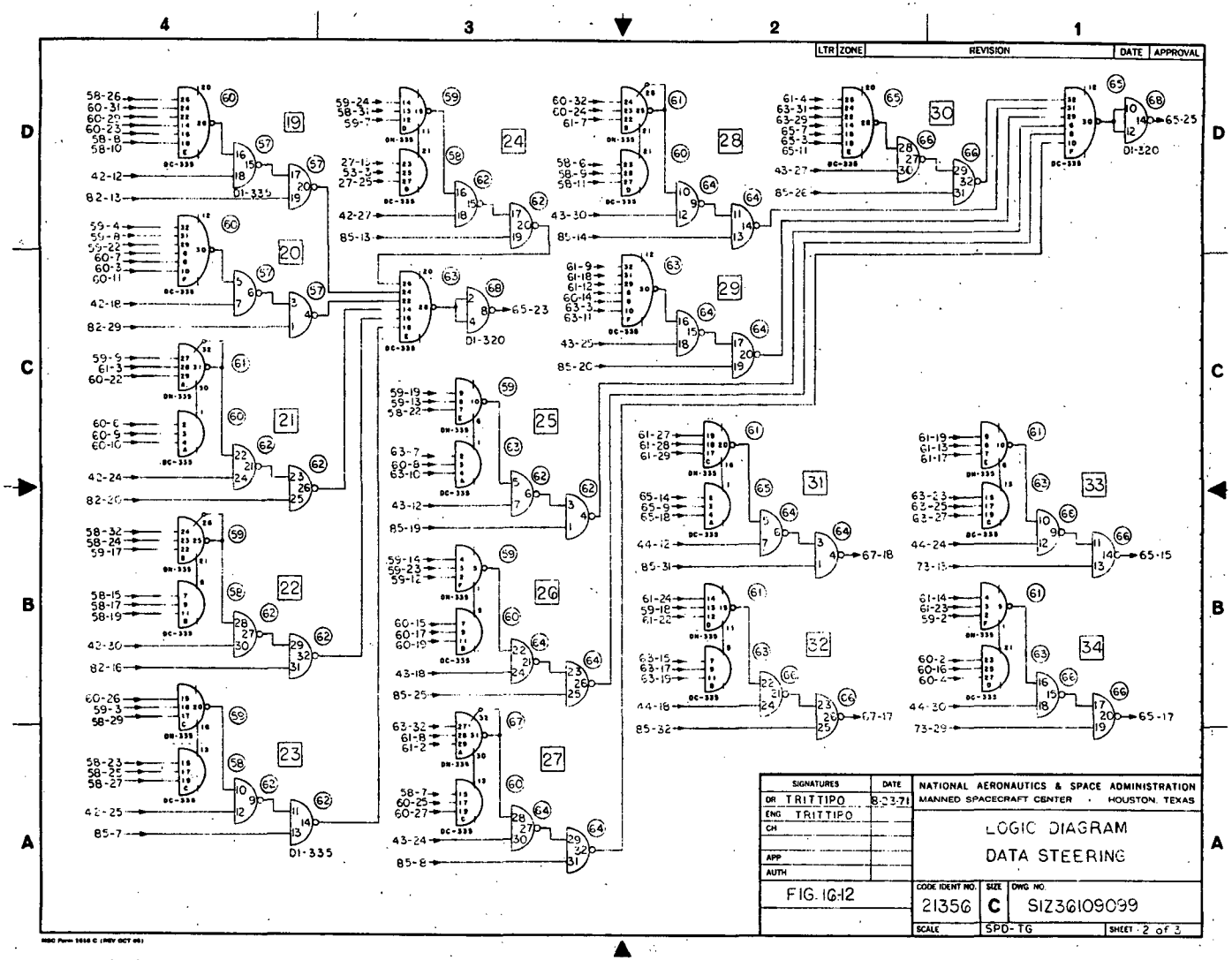


Figure 16-12. – Logic Diagram, Data Steering

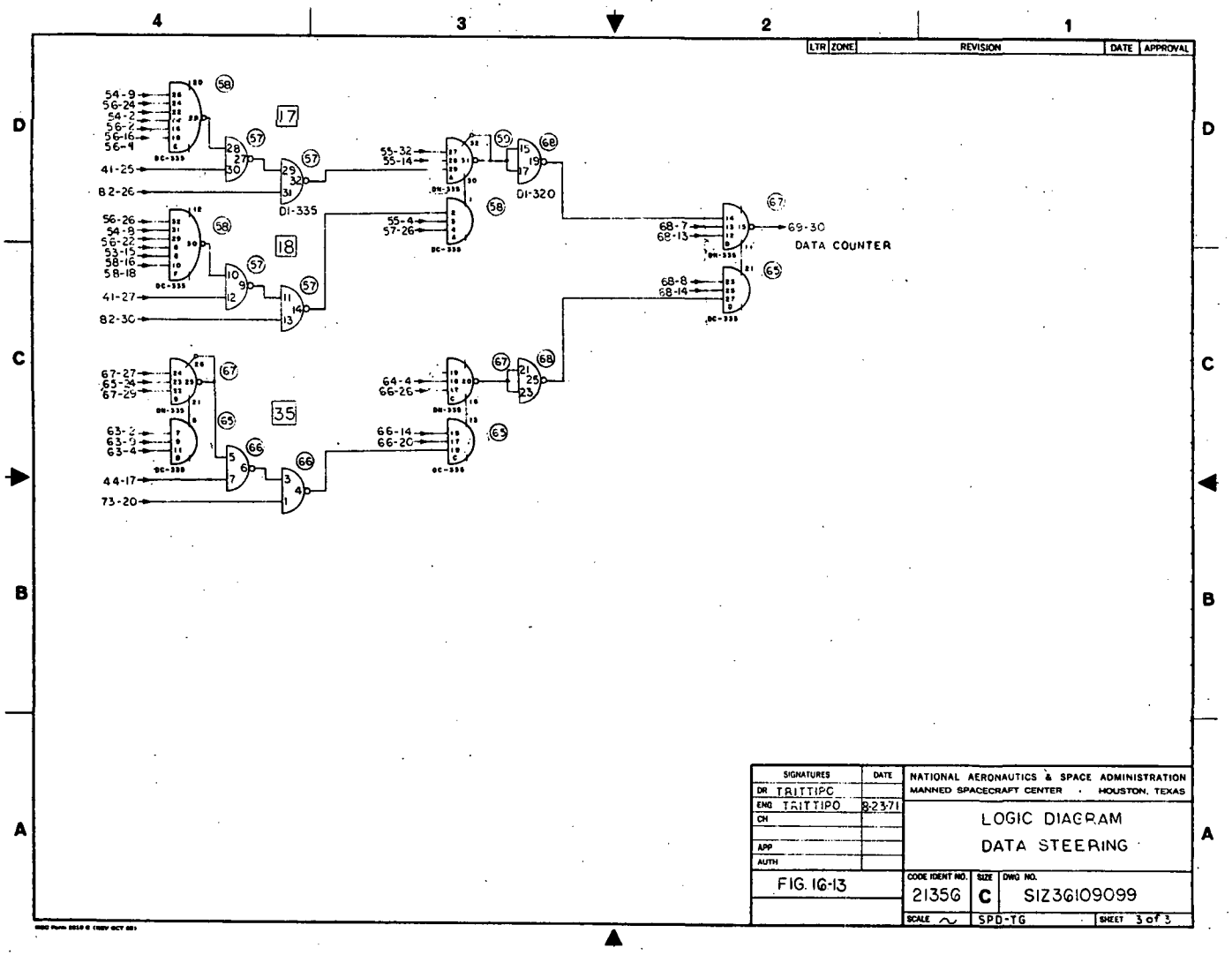


Figure 16-13. – Logic Diagram, Data Steering

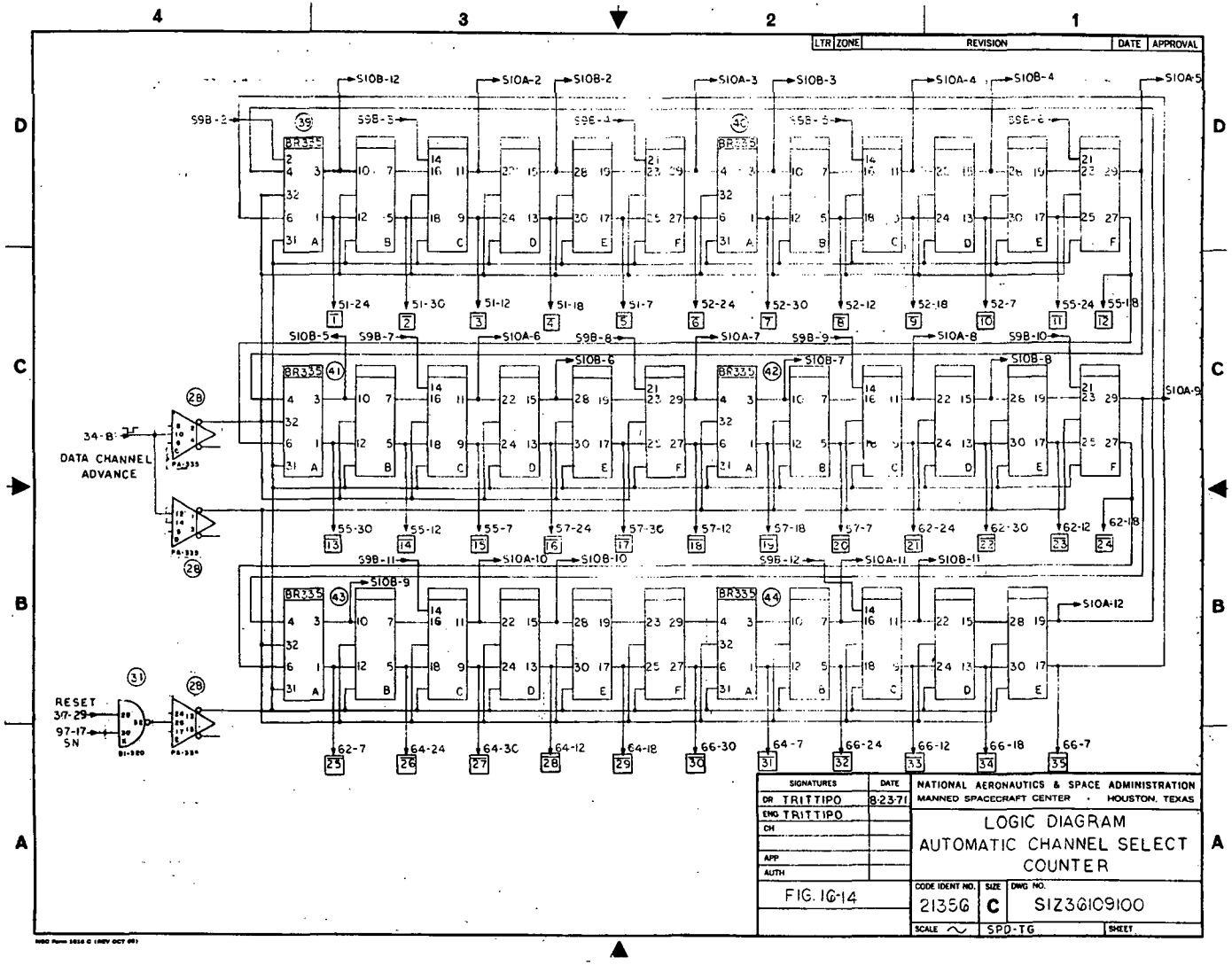


Figure 16-14. — Logic Diagram, Automatic Channel Select Counter

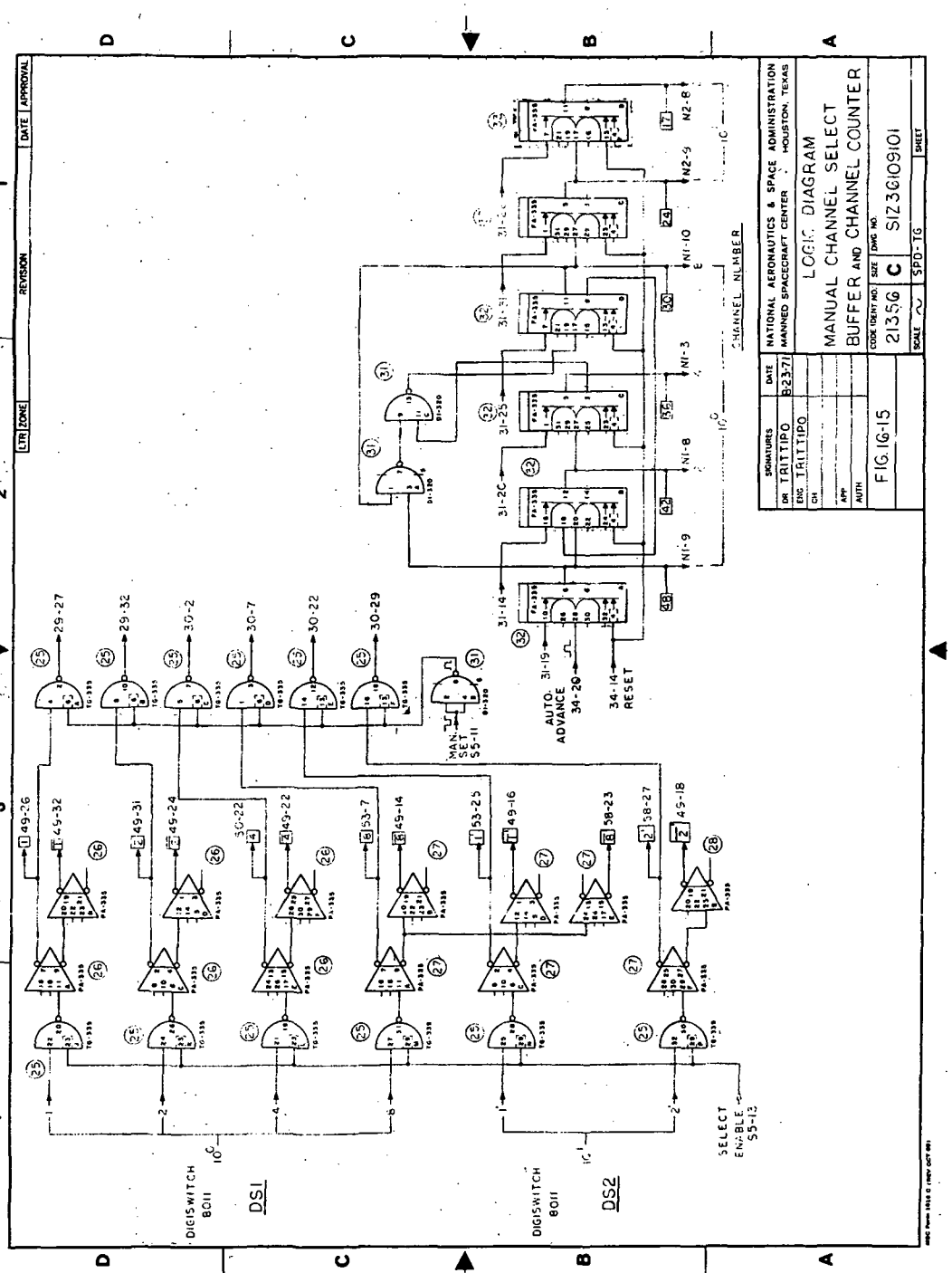


Figure 16-15. — Logic Diagram, Manual Channel Select, Buffer and Channel Counter

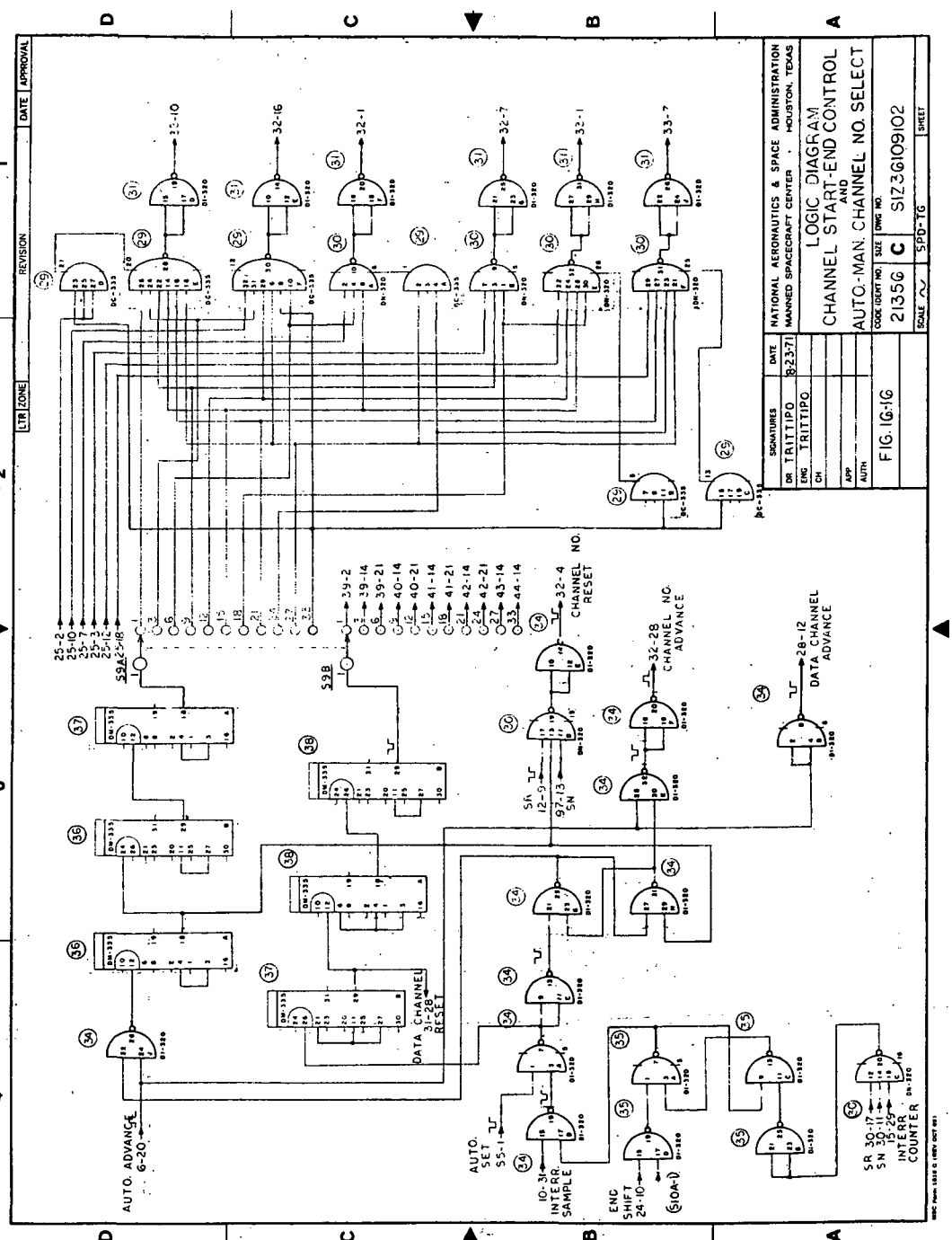


Figure 16-16. - Logic Diagram, Channel Start-End Control

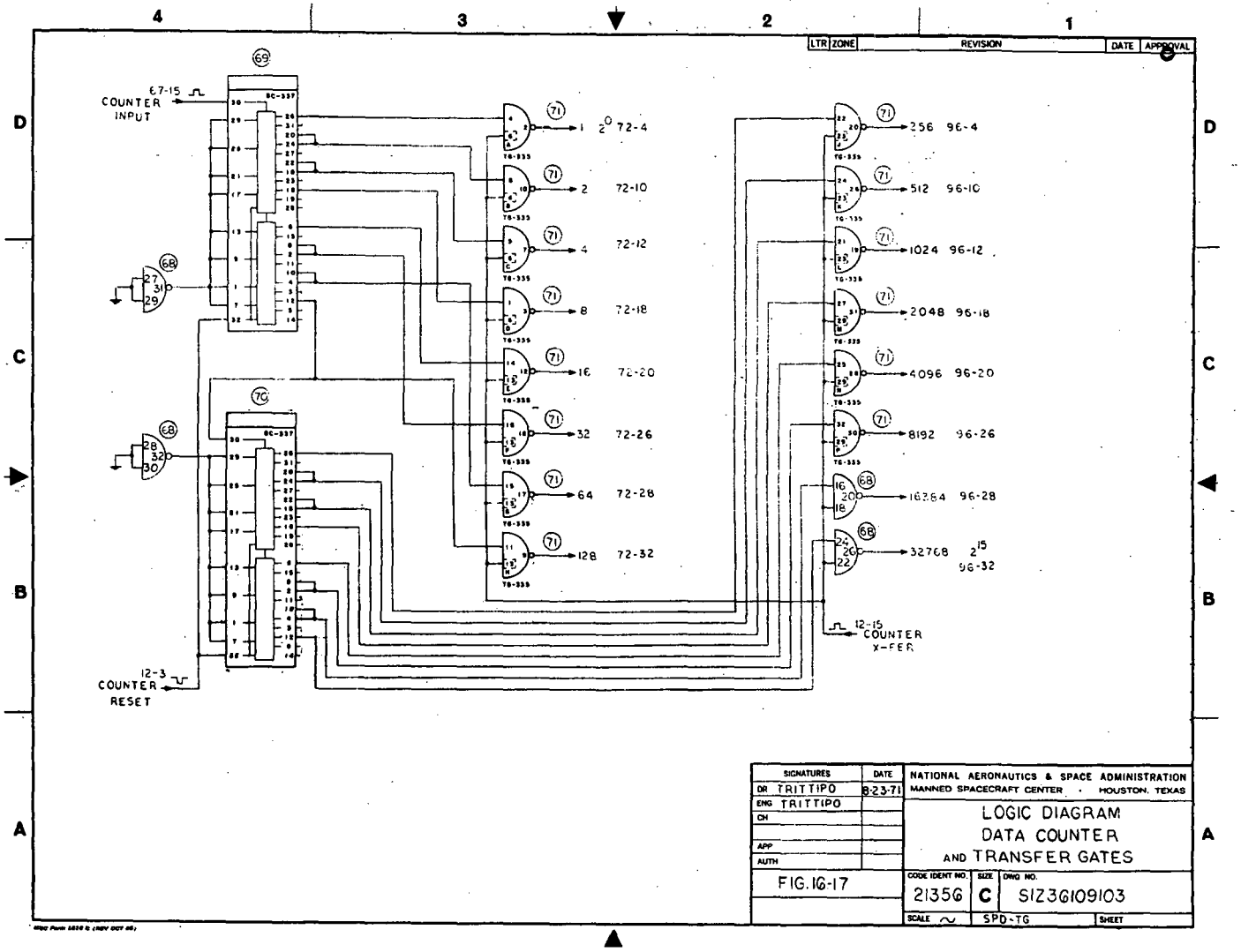


Figure 16-17. – Logic Diagram, Data Counter and Transfer Gates

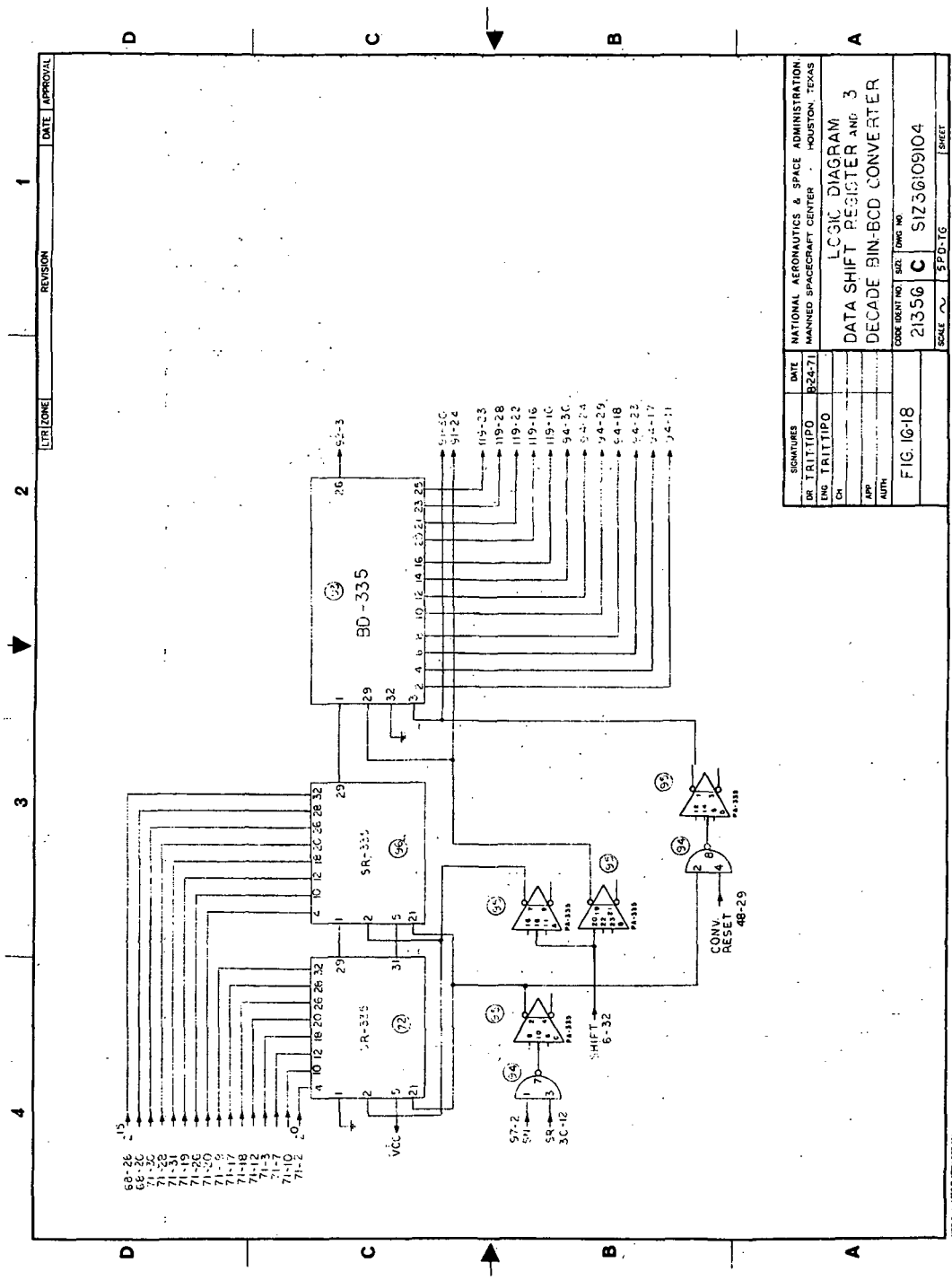


Figure 16-18. - Logic Diagram, Data Shift Register

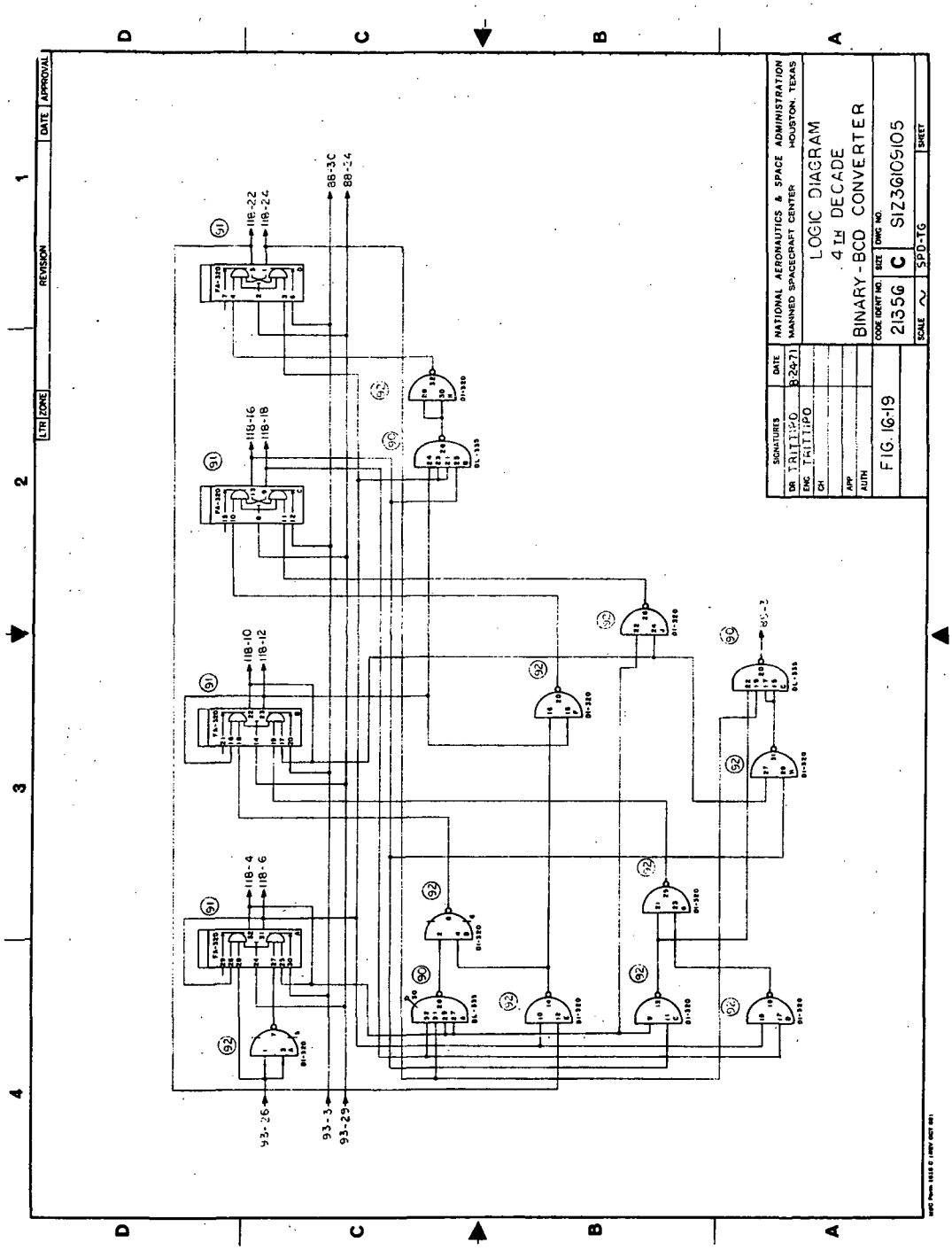


Figure 16-19. — Logic Diagram

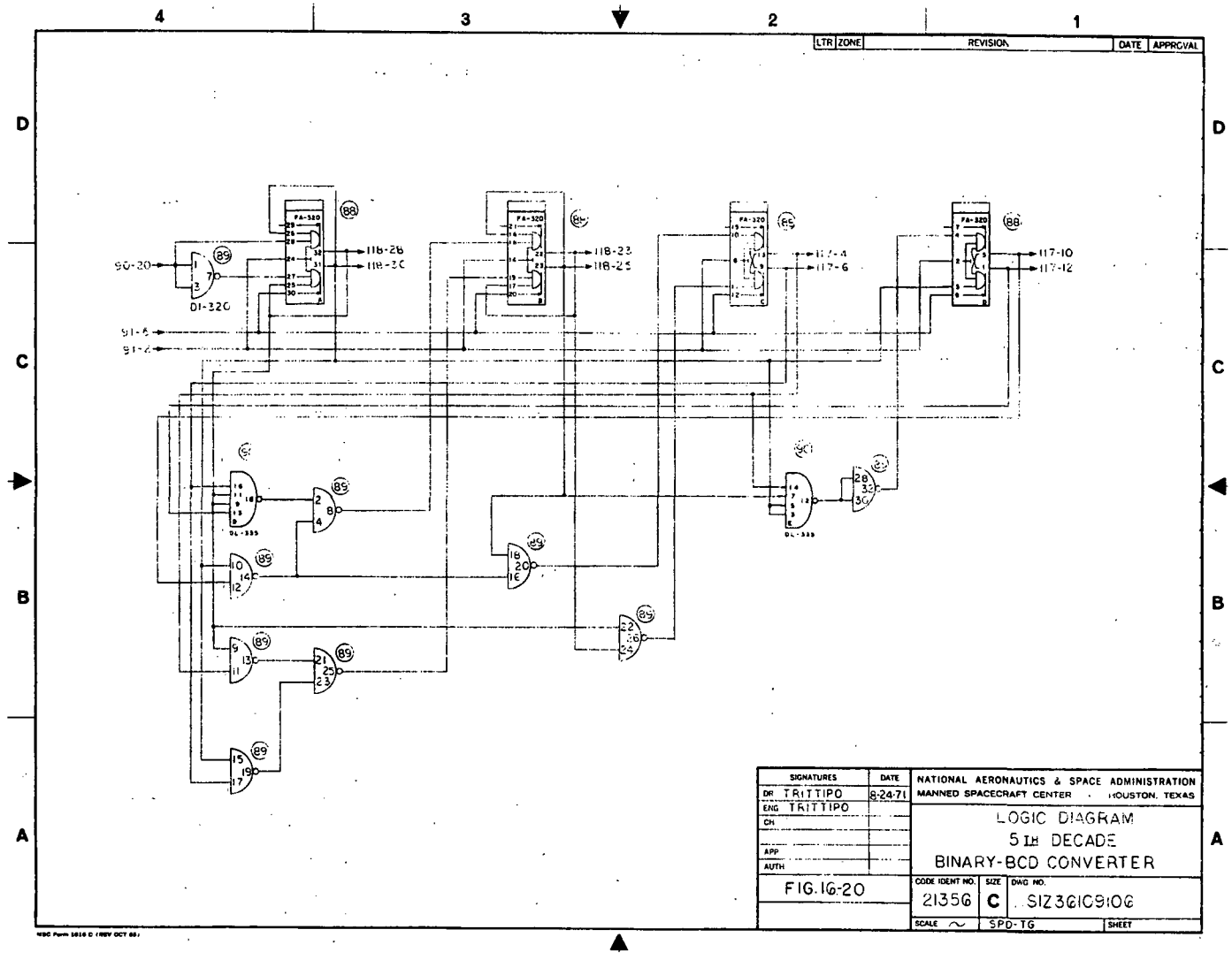


Figure 16-20. – Logic Diagram

CONVERTER TRANSFER command transfers the binary to BCD converted data to the data transfer register (Figure 16-21). The CONVERTER TRANSFER command is also used as a MANUAL SET command in the Manual Mode of operation or a CHANNEL ADVANCE command in the Automatic Mode of operation.

The CONVERTER TRANSFER command is delayed 10 μsec. and then generates a 10 μsec. pulse used as a converter reset, PRINT command and SYSTEM STOP control command.

SYSTEM STOP is derived from several methods. By initiation of a STOP command (S3), start latch 5-32 is reset inhibiting gate 9-19. This action inhibits the Interrogation Sample signal, therefore stopping the system.

A one cycle stop (S7) in the Manual Mode of operation (S5) is derived from each CONVERTER RESET command. This command is directed through (S5) manual and (S7) to start latch 7-13. This command resets the start latch and stops the system.

A continuous cycle stop (S7) in the Manual Mode of operation (S5) is derived from each CONVERTER RESET command. This command is directed through (S5) manual, gate 9-30 and (S7) continuous. In order for this command to be directed through gate 9-27, an AUTO. STOP command has to be initiated. This command sets latch 9-6 which enables gate 9-28. This command is then directed to the start latch through S7 and resets the latch stopping the system.

System stop in the Automatic Mode of operation is derived by the same method except that the CONVERTED RESET command,

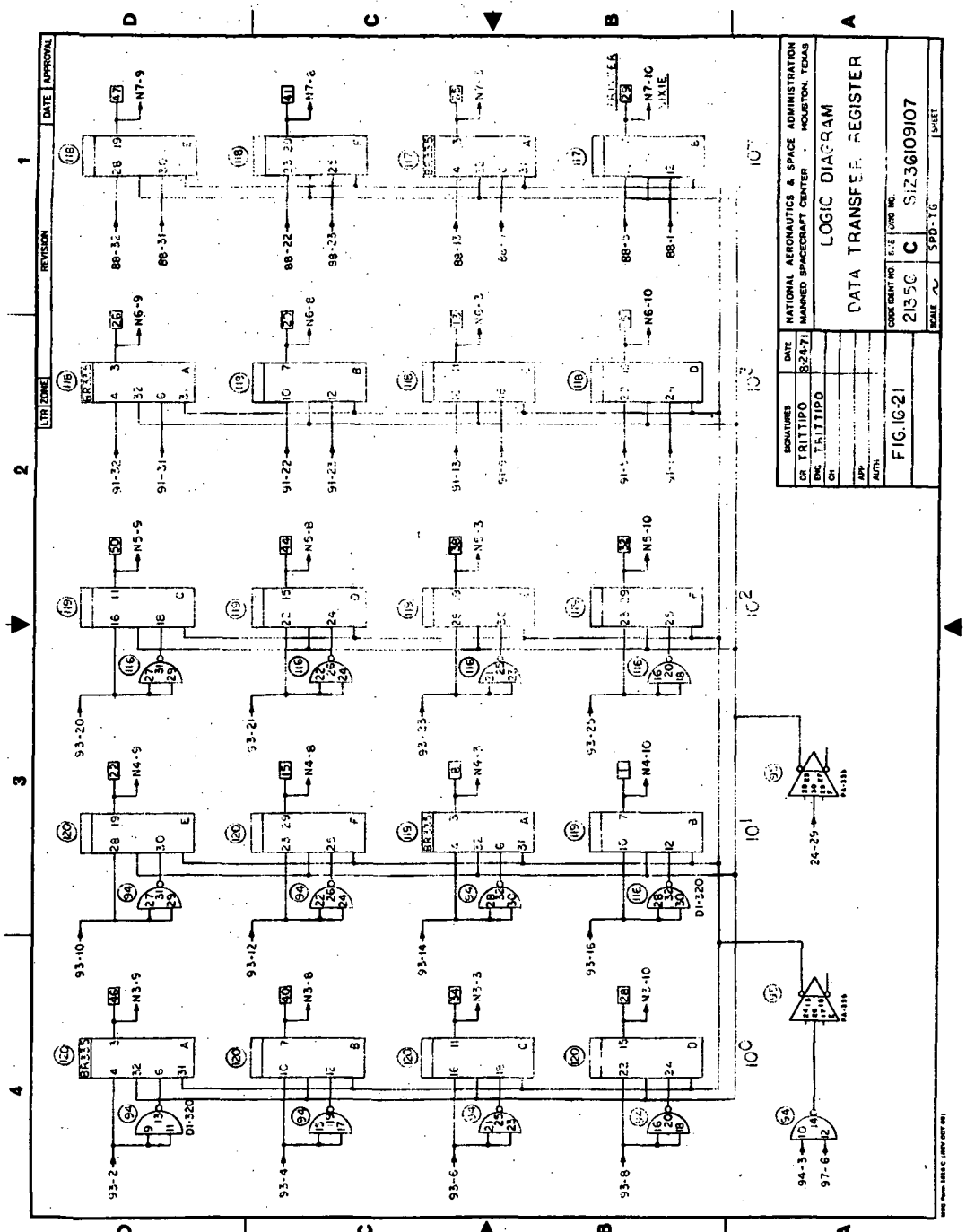


Figure 16-21. — Logic Diagram, Data Transfer Register

generating the STOP command, is controlled by end channel + 1 gate 9-24. The end channel + 1 signal enables gate 9-24 allowing the STOP command to stop system.

In the Manual Mode of operation, the data channel and channel number is selected by setting the digit switches to the desired number. The digit switch output is directed to the Manual Channel select buffer shown in Figure 16-15. The SELECT ENABLE command, when in the Manual Mode, presents the digit switch setting to the data steering circuits (Figures 16-11, 16-12 and 16-13).

Each time a CONVERTER TRANSFER command is initiated, a MANUAL SET command is generated. The MANUAL SET command transfers the digit switch settings to the auto-man channel number select circuit shown in Figure 16-16. The signals are then directed to the channel counter circuit (Figure 16-15) which in turn sets the channel number display to the selected settings.

When operating in the Automatic Mode of operation, the SYSTEM START command is directed through S5 generating a AUTO. SET command. The AUTO. SET command generates a 5 μsec. pulse used to reset the Auto. Data Channel counter (Figure 16-14). The reset pulse is delayed by 50 μsec. and then generates a 10 μsec. pulse used to set the Auto. Data Channel counter. The channel to be set is determined by the setting of the (S9-B) CHANNEL START switch. The AUTO. SET command also sets latch 34-25. Setting latch 34-25 enables gate 34-24 and disables gate 34-30. At the time of each CONVERTER TRANSFER command, a CHANNEL ADVANCE command is generated through S5 and

inverter 6-20. With gate 34-24 enabled, the CHANNEL ADVANCE command generates a channel number counter reset and resets latch 34-25. The CHANNEL NUMBER RESET command is delayed 10 μsec. and then generates a 10 μsec. pulse used as an AUTO. CHANNEL NUMBER SET command. The channel number set is determined by the setting of (S9-A) CHANNEL START switch. The CHANNEL ADVANCE command also generates an Auto. Data Channel advance. With the initiation of the first channel advance, resetting latch 34-25 and therefore enabling gate 34-30, each additional CHANNEL ADVANCE command will generate an Auto. Channel Number advance command as well as an AUTO. DATA CHANNEL ADVANCE command.

When the data channel counter advances to the end channel (determined by the setting of S10-A), a signal is generated which enables gate 35-17. Upon receiving the next END SHIFT command, latch 35-7 is set. Setting latch 35-7 enables the next INTERROGATION SAMPLE command to be gated through gates 34-19 and 34-7. This command resets and sets the Auto. Data Channel counter to the Start Channel and the cycle starts again. The first INTERROGATION COUNTER COMMAND initiates a signal at gate 30-18 to reset latch 35-7.

17. CAMERA CONTROL

17.1 Introduction

The Nikon camera photographs the stars in order to provide rocket orientation to the exact source of X-ray emissions. The camera control circuits open the camera shutter and operate the F-250 film advance motor. The camera takes a total of 250 pictures at the rate of one frame every 1.6 seconds. The shutter speed is set for 1/8 of a second. Photography starts 64 seconds after receipt of a DOOR OPEN signal. If the voltage of the DOOR OPEN signal drops to 0.0 volts, system operation ceases and will not resume again until 64 seconds after the DOOR OPEN. Signal rises to 5.0 volts.

17.2 Theory of Operation

The Block Diagram for the camera control circuits is shown in Figure 17-1. In this diagram, the UJT oscillator provides a pulse rate of 1.6 seconds. This rate, however, can be varied from 1/3 to 3 Hz by adjustment of potentiometer R_1 (shown in Figure 17-2). This pulse triggers a one-shot which provides an 80 msec wide pulse for advancing the counters for the Digital-to-Analog Converter and the 7-Segment LED Displays.

Another UJT oscillator, oscillating at the rate of 1 Hz, provides the 64 second time delay after the circuit receives the DOOR OPEN signal. These pulses are fed to the "÷64" counter which counts 64 pulses and then emits an output which removes the clamp between the first oscillator and the one-shot.

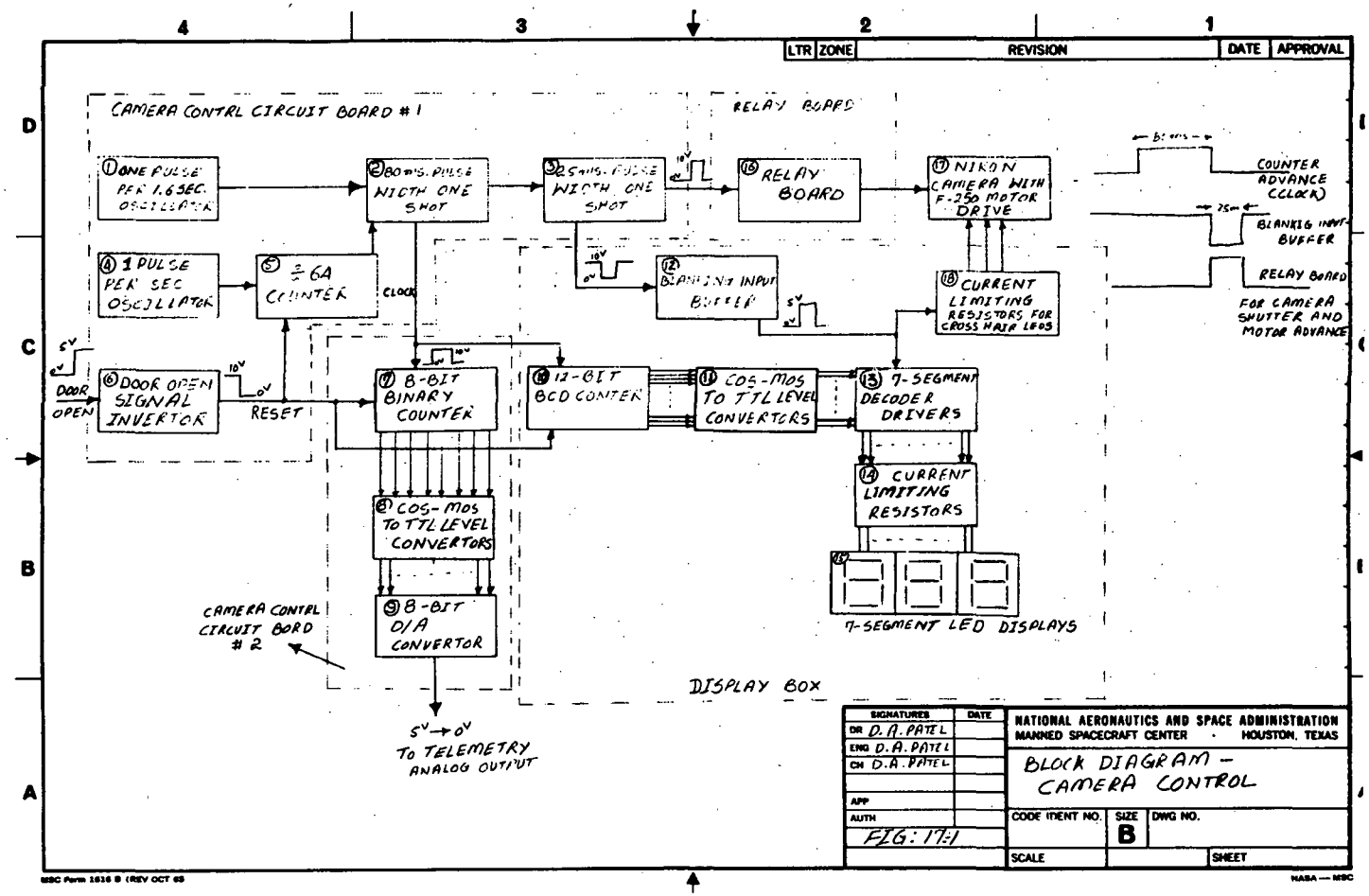


Figure 17-1 Block Diagram, Camera Control

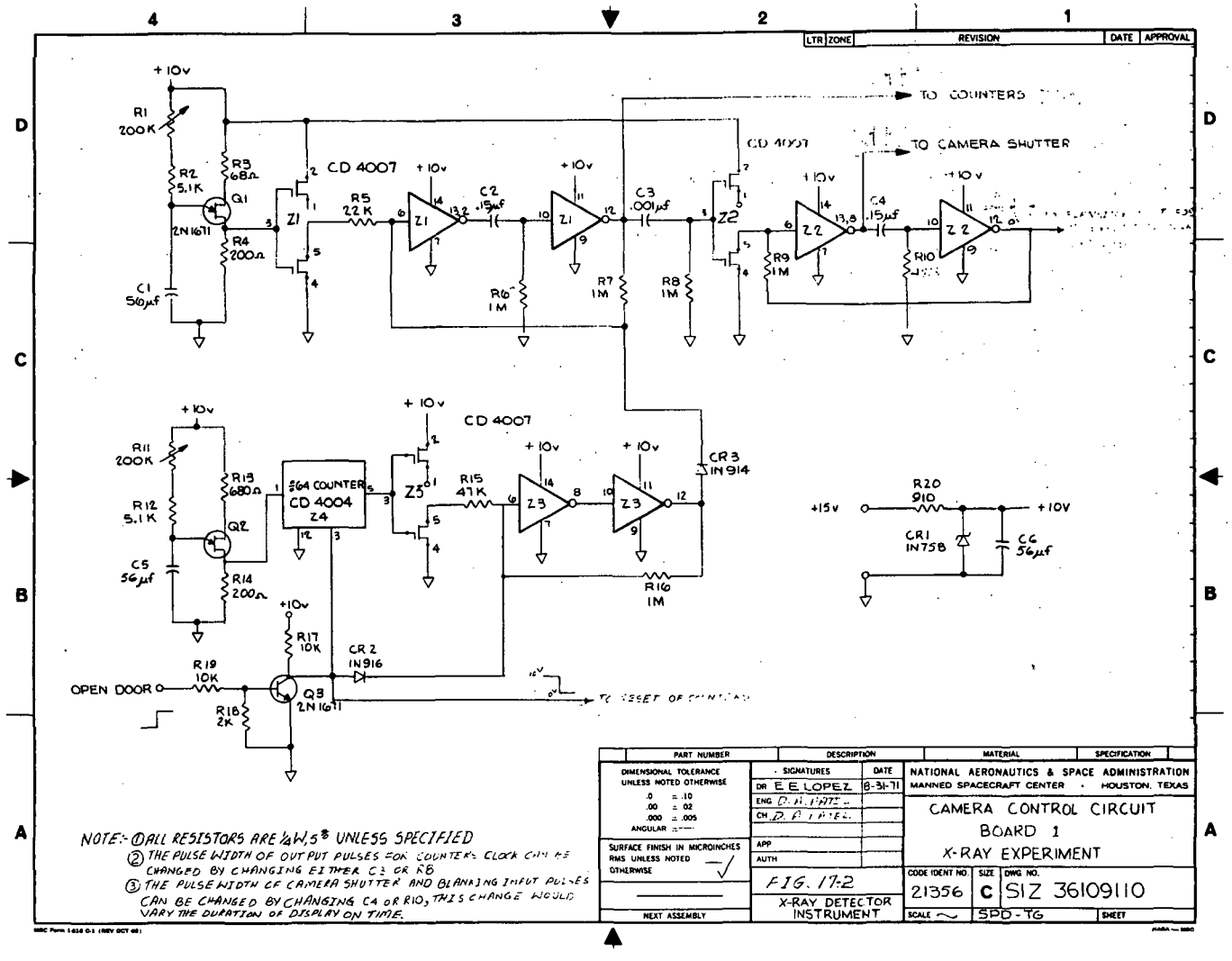


Figure 17-2 Camera Control Circuit, Board 1

The trailing edge of the pulse from the first one-shot fires the second one-shot which provides a 25 msec pulse with both Q and $\overline{Q}$ outputs. The $\overline{Q}$ output is inverted by the blanking input buffer which changes the voltage level from COS-MOS logic levels to TTL logic levels. This signal illuminates the LED display and the cross hair LEDs for a period of 25 msec. The Q output is supplied to the relay board (Figure 17-4). This signal is supplied through an optoelectric isolator to relays which operate the camera shutter and motor. The optoelectric isolator prevents noise fed back from the motor to the logic circuits. The output of this relay board is fed to the camera shutter and the motor through a jack located on the front of the camera. The 25 msec pulse opens the camera shutter. When the shutter closes, the F-250 motor drive advances the film to the next frame. Thus, if the shutter speed has been set for less than 1/40 of a second, the LED display and cross hair LEDs are still illuminated after the shutter has closed and the motor is advancing the film. This can result in a blur on the film. Therefore, shutter speed should be no less than 1/40 of a second.

The pulse output from the first one-shot supplies the 8-bit counter of the Digital-to-Analog Converter. The counter then supplies 8-bit binary output to the converter. The converter, inturn, provides 0-5 volt output corresponding to the digital input. This output is fed to the unity gain inverting amplifiers. This output is proportional to the binary number at the input of the Digital-to-Analog Converter. It will vary from 5 volts to 0 volts as the counter counts from zero to 256. It is fed into telemetry for transmission to the ground along with other data. Ultimately it will be

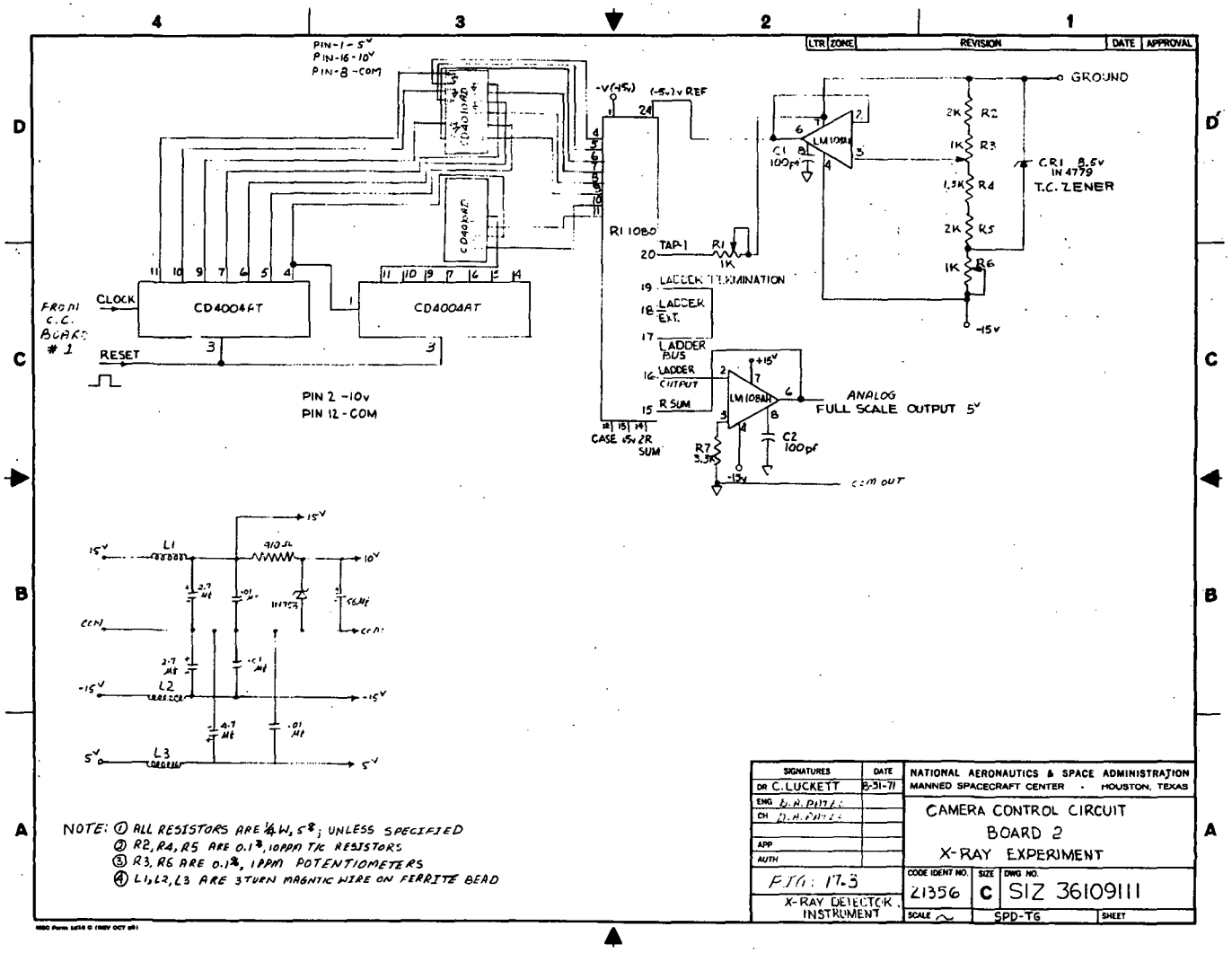


Figure 17-3 Camera Control Circuit, Board 2

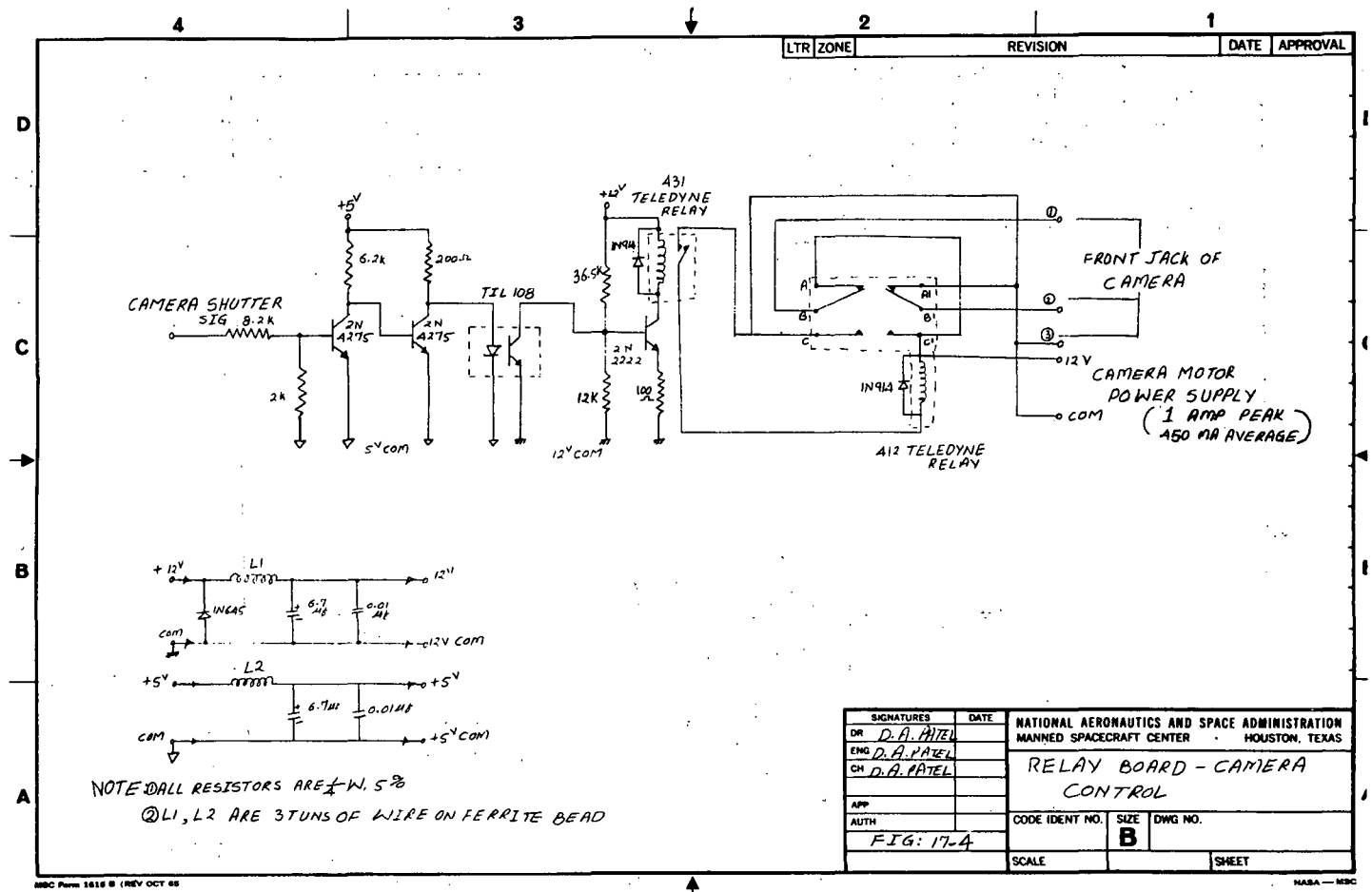


Figure 17-4 Relay Board — Camera Control

used to correlate the exposed number on the film with the X-ray data received.

The clock pulse, which is used to expose the number on the film, also advances both the Digital-to-Analog converter and the 12-bit BCD display counter. The 12 BCD bits, or three decades of information, feed the 7-segment decoder driver which, in turn, provides power to the appropriate segments of the LED Display. The corresponding number on the LED Display will be illuminated when it receives an output pulse from the blanking input buffer. This number is then projected onto the back of the film by means of a mirror and lens arrangement mounted inside of the display box at the rear of the camera. This mirror and lens arrangement provides the adjustment necessary to properly focus the number on the back of the film. This number corresponds to the frame number of the film which has been exposed.

17.3 Figures

The circuits necessary for the generation of the controls to operate the film advance motor, and the LED Display are mounted on printed circuit boards. These boards also include the circuits which insure that the analog voltage corresponds to the exposed number on the film.

Figure 17-2 shows the schematic details of blocks 1 through 6 of Figure 17-1, Figure 17-3 shows the schematic details of blocks 7 through 9 of Figure 17-1, and Figure 17-4 is the schematic diagram of the relay board (block 16 of Figure 17-1). These circuit boards are located in the main housing.

The control circuits for the LED Display and the cross hair LEDs are also mounted on printed circuit boards. These boards are mounted on four of the interior walls of the display box. Since this box must prevent external light from entering the camera through the mirror-lens arrangement, all joints of the box should be sealed with black tape.

The schematic diagram for these circuits is shown in Figure 17-5. The interconnection diagram for the entire system is shown in Figure 17-6.

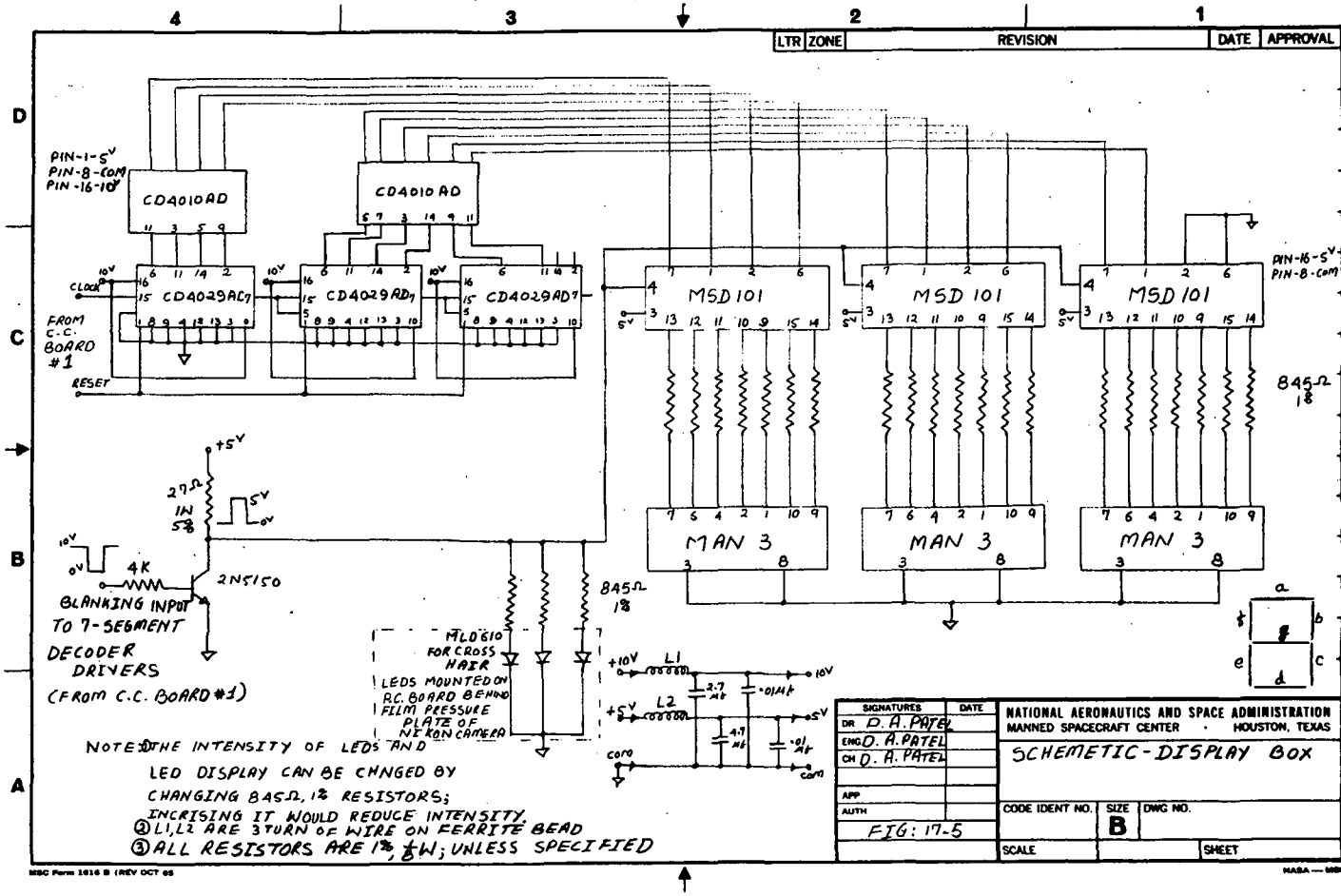


Figure 17-5 Schematic – Display Box

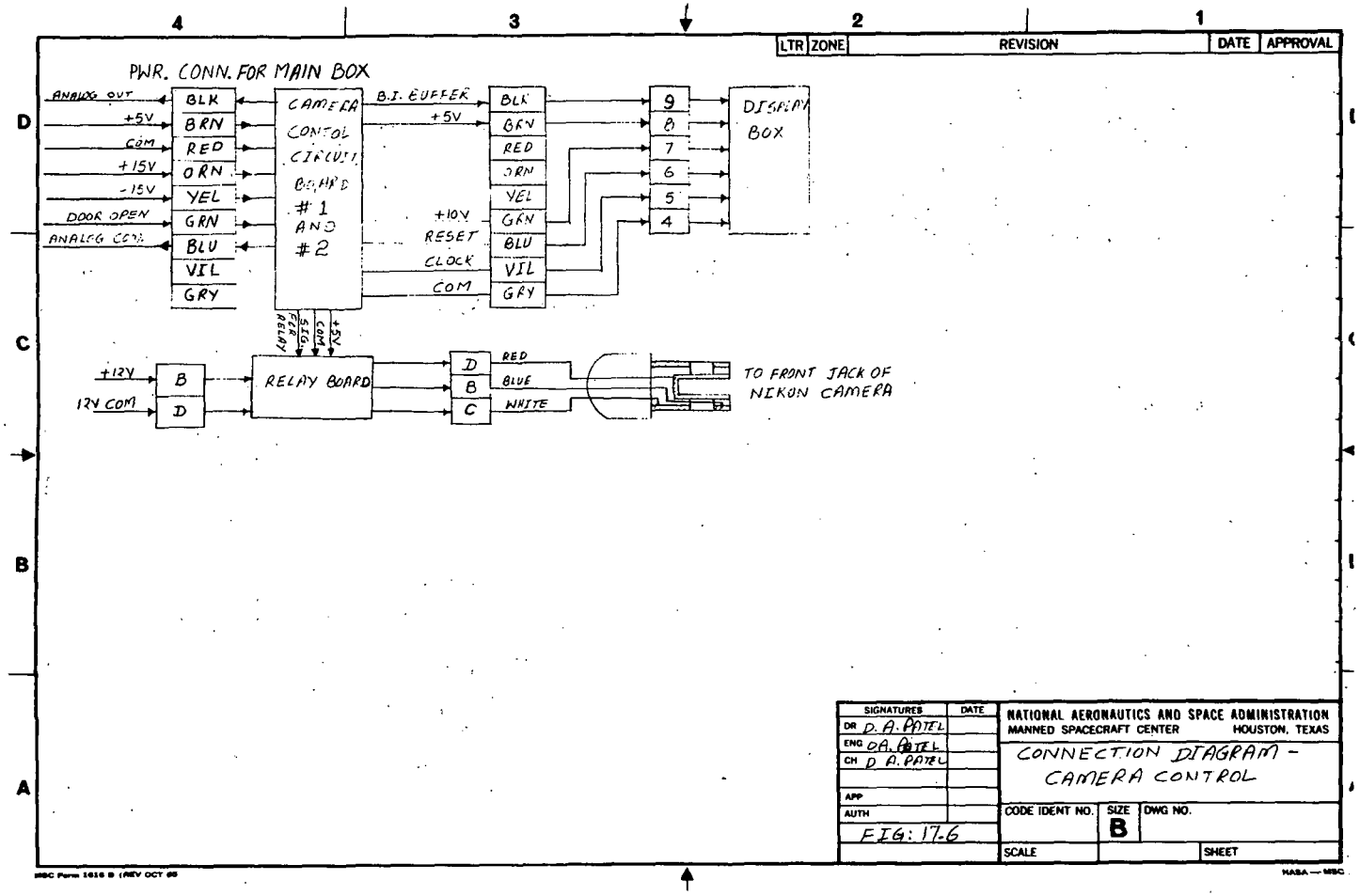
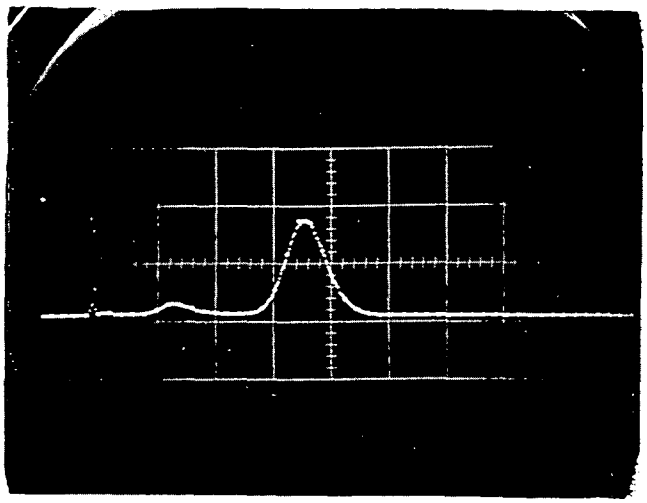


Figure 17-6 Connection Diagram – Camera Control

18. TEST RESULTS

The operation of the automatic gain control system is demonstrated in Figures 18-1 through 18-4. The histograms of a 6 Kev Fe^{55} source with the proportional counter in the Open Loop Mode (fixed high voltage) and in the Closed Loop Mode (Auto-Gain Control operating) are compared. The resolution appears to have deteriorated less than 1 percent by the Automatic Gain Control using either propane or P-10 detector gas. The test hook-up is shown in Figure 18-5.

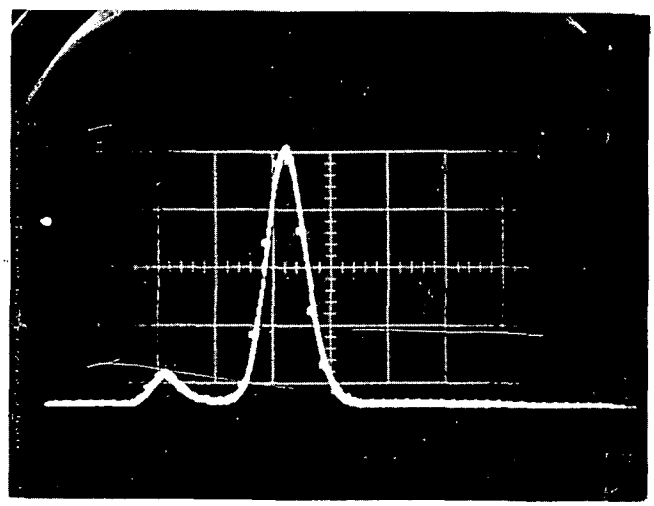
The pulse height calibrations of the five electronic units are given in Tables 18-1 through 18-5. The differential nonlinearity is seen to be less than 1 percent for all five units. The test hook-up is shown in Figure 18-6. The Rise Time Discrimination versus Pulse Height is given in Table 18-6. The Rise Time Discriminator is seen to reject all pulses whose rise time is greater than 50 nanoseconds and to accept all pulses whose rise time is less than 30 nanoseconds for pulses whose heights fall in channels 2 through 32. The test hook-up is shown in Figure 18-7.



R = 17.2%

Figure 18-1

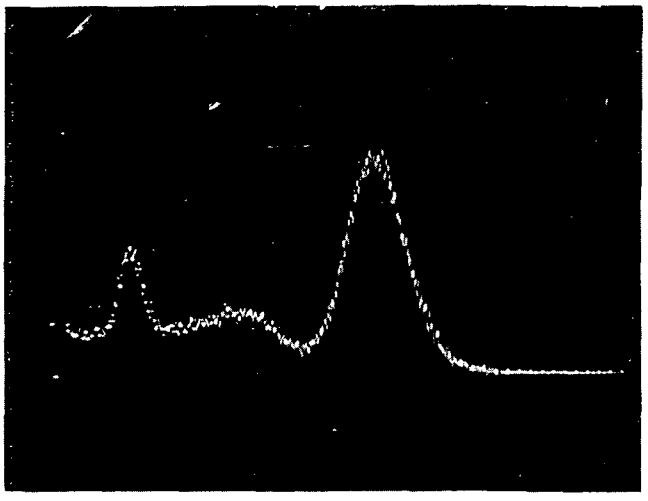
Iron-55 Histogram with P-10 Gas and a Fixed High Voltage



R = 18.85%

Figure 18-2

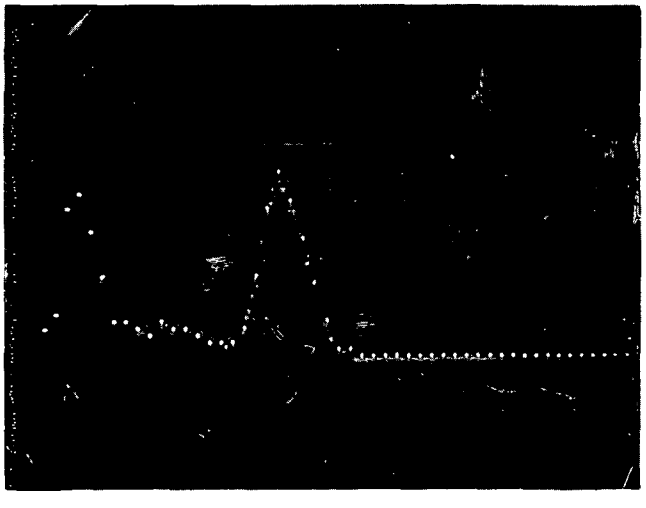
Iron-55 Histogram with P-10 Gas and Automatic Gain Control



R = 20%

Figure 18-3

Iron-55 Histogram with Propane and a Fixed High Voltage



R = 20%

Figure 18-4

Iron-55 Histogram with Propane and Automatic Gain Control

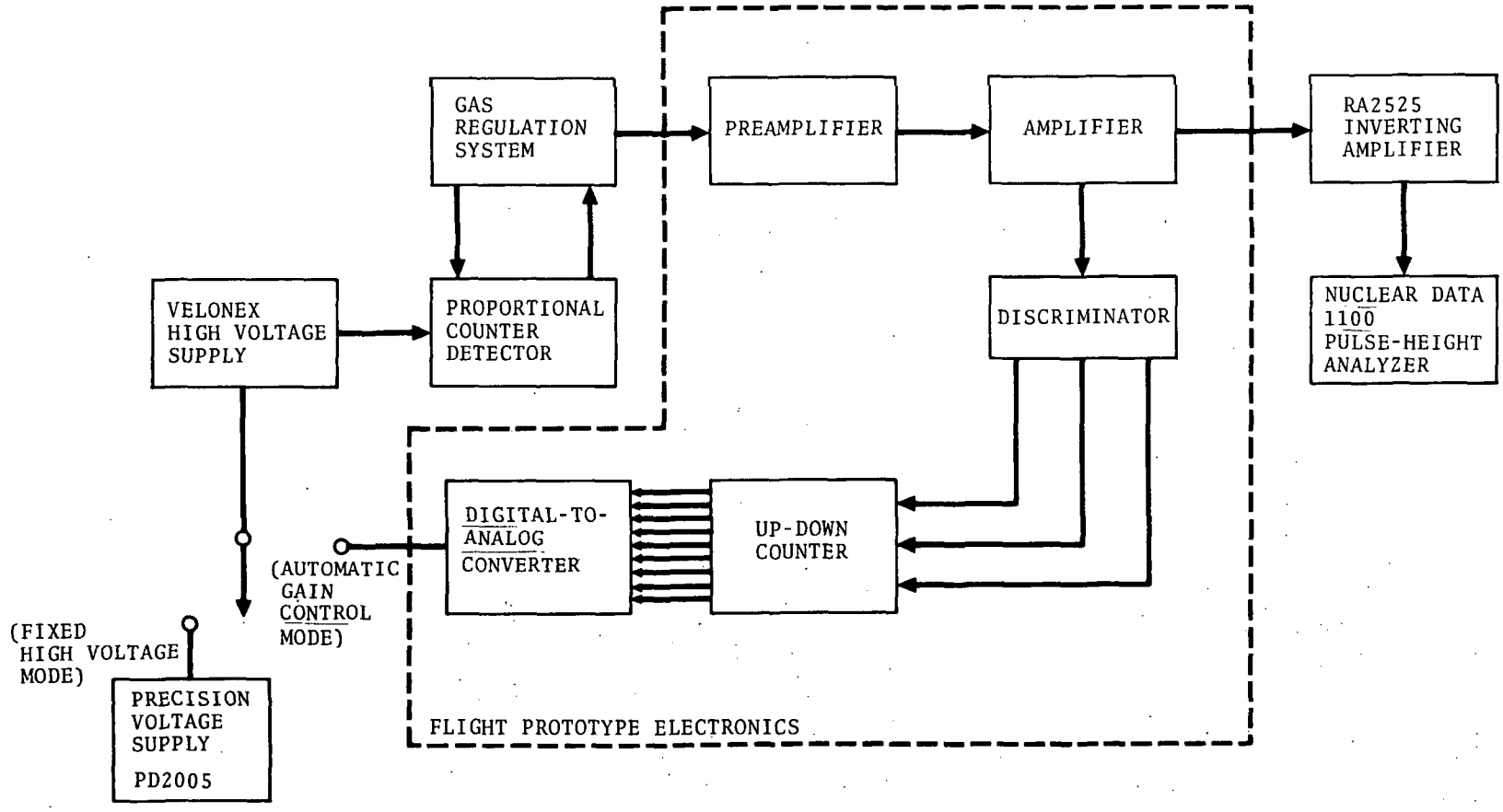


Figure 18-5. – Histogram Test Hook-Up.

TABLE 18-1 PULSE HEIGHT CALIBRATION – UNIT #1

CHANNEL	10°C		30°C		60°C	
	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
32	4.882 to –					
31	4.726 to 4.882	0.156	4.712 to 4.868	0.156	4.736 to 4.892	0.156
30	4.571 to 4.726	0.155	4.555 to 4.712	0.157	4.580 to 4.736	0.156
29	4.416 to 4.571	0.155	4.400 to 4.555	0.155	4.426 to 4.580	0.154
28	4.257 to 4.416	0.159	4.241 to 4.400	0.159	4.266 to 4.426	0.160
27	4.102 to 4.257	0.155	4.087 to 4.241	0.154	4.107 to 4.266	0.159
26	3.945 to 4.102	0.157	3.929 to 4.087	0.158	3.952 to 4.107	0.155
25	3.788 to 3.945	0.157	3.773 to 3.929	0.156	3.795 to 3.952	0.157
24	3.629 to 3.788	0.159	3.613 to 3.773	0.160	3.635 to 3.795	0.160
23	3.475 to 3.629	0.154	3.460 to 3.613	0.153	3.478 to 3.635	0.157
22	3.317 to 3.475	0.158	3.304 to 3.460	0.156	3.322 to 3.478	0.156
21	3.162 to 3.317	0.155	3.148 to 3.304	0.156	3.166 to 3.322	0.156
20	3.003 to 3.162	0.159	2.990 to 3.148	0.158	3.010 to 3.166	0.156
19	2.848 to 3.003	0.155	2.835 to 2.990	0.155	2.849 to 3.010	0.161
18	2.291 to 2.848	0.157	2.678 to 2.835	0.157	2.693 to 2.849	0.156
17	2.535 to 2.291	0.156	2.523 to 2.678	0.155	2.537 to 2.693	0.156
16	2.375 to 2.535	0.160	2.364 to 2.523	0.159	2.379 to 2.537	0.158
15	2.222 to 2.375	0.153	2.211 to 2.364	0.153	2.220 to 2.379	0.159
14	2.064 to 2.222	0.153	2.053 to 2.211	0.158	2.063 to 2.220	0.157
13	1.908 to 2.064	0.156	1.898 to 2.053	0.155	1.908 to 2.063	0.155
12	1.750 to 1.908	0.158	1.740 to 1.898	0.158	1.750 to 1.908	0.158
11	1.595 to 1.750	0.155	1.586 to 1.740	0.154	1.592 to 1.750	0.158
10	1.437 to 1.595	0.158	1.429 to 1.586	0.157	1.436 to 1.592	0.156
9	1.282 to 1.437	0.155	1.273 to 1.429	0.156	1.279 to 1.436	0.157
8	1.123 to 1.282	0.159	1.116 to 1.273	0.157	1.123 to 1.279	0.156
7	0.968 to 1.123	0.156	0.962 to 1.116	0.154	0.964 to 1.123	0.159
6	0.811 to 0.968	0.157	0.804 to 0.962	0.158	0.806 to 0.964	0.158
5	0.655 to 0.811	0.156	0.648 to 0.804	0.156	0.650 to 0.806	0.156
4	0.497 to 0.655	0.158	0.491 to 0.648	0.157	0.493 to 0.650	0.157
3	0.341 to 0.497	0.156	0.336 to 0.491	0.155	0.335 to 0.493	0.158
2	0.184 to 0.341	0.157	0.179 to 0.336	0.157	0.178 to 0.335	0.157
1	0.056 to 0.184	0.128	0.055 to 0.179	0.124	0.054 to 0.178	0.124
0	– to 0.056	0.056	– to 0.055	0.054	– to 0.054	0.054

$$\text{TEMPERATURE COEFFICIENT} = \frac{T_1 - T_2}{T_1} \times 100 \div 30$$

$$= \frac{4.712 - 4.736}{4.712} \times 100 \div 30$$

$$= 0.0169\%/°C$$

TABLE 18-2. — PULSE HEIGHT CALIBRATION-UNIT #2

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
32		
31		
30		
29		
28		
27		
26		
25		
24		
23	INFORMATION NOT AVAILABLE	
22		
21		
20		
19		
18		
17		
16		
15		
14		
13		
12		
11		
10		
9		
8		
7		
6		
5		

TABLE 18-2. — PULSE HEIGHT CALIBRATION-UNIT #2 (CONCLUDED)

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
4		
3		
2		
1		
0		

INFORMATION NOT AVAILABLE

TABLE 18-3. — PULSE HEIGHT CALIBRATION — UNIT #3

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
32		0.151
31	4.703 to	0.150
30	4.552 to 4.703	0.150
29	4.402 to 4.552	0.151
28	4.251 to 4.402	0.150
27	4.101 to 4.251	0.152
26	3.949 to 4.101	0.151
25	3.798 to 3.949	0.154
24	3.644 to 3.798	0.149
23	3.495 to 3.644	0.152
22	3.343 to 3.495	0.151
21	3.192 to 3.343	0.152
20	3.040 to 3.192	0.152
19	2.888 to 3.040	0.152
18	2.736 to 2.888	0.152
17	2.584 to 2.736	0.154
16	2.430 to 2.584	0.152
15	2.278 to 2.430	0.154
14	2.124 to 2.278	0.153
13	1.971 to 2.124	0.157
12	1.814 to 1.971	0.153
11	1.661 to 1.814	0.156
10	1.505 to 1.661	0.155
9	1.350 to 1.505	0.158
8	1.192 to 1.350	0.158
7	1.034 to 1.192	0.161
6	0.873 to 1.034	0.162
5	0.711 to 0.873	0.167
4	0.544 to 0.711	0.170

TABLE 18-3. – PULSE HEIGHT CALIBRATION – UNIT #3 (CONCLUDED)

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
4	0.544 to 0.711	0.170
3	0.374 to 0.544	0.177
2	0.197 to 0.374	0.179
1	0.	
0		

TABLE 18-4 PULSE HEIGHT CALIBRATION – UNIT #4

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
32	4.868 to –	–
31	4.713 to 4.868	0.155
30	4.558 to 4.713	0.155
29	4.403 to 4.558	0.155
28	4.246 to 4.403	0.157
27	4.093 to 4.246	0.153
26	3.937 to 4.093	0.156
25	3.782 to 3.937	0.155
24	3.628 to 3.782	0.154
23	3.473 to 3.628	0.155
22	3.317 to 3.473	0.156
21	3.162 to 3.317	0.155
20	3.004 to 3.162	0.158
19	2.850 to 3.004	0.154
18	2.694 to 2.850	0.156
17	2.538 to 2.694	0.156
16	2.379 to 2.538	0.159
15	2.226 to 2.379	0.153
14	2.069 to 2.226	0.157
13	1.914 to 2.069	0.155
12	1.756 to 1.914	0.158
11	1.601 to 1.756	0.155
10	1.444 to 1.601	0.157
9	1.288 to 1.444	0.156
8	1.130 to 1.288	0.158
7	0.974 to 1.130	0.156

TABLE 18-4 (Concluded)

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
6	0.816 to 0.974	0.158
5	0.660 to 0.816	0.156
4	0.501 to 0.660	0.159
3	0.345 to 0.501	0.156
2	0.187 to 0.345	0.158
1	0.030 to 0.187	0.157
0	— to 0.030	—

TABLE 18-5 PULSE HEIGHT CALIBRATION – UNIT #5

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
32	1.878 to –	–
31	4.722 to 1.878	0.156
30	4.566 to 4.722	0.156
29	4.410 to 4.566	0.156
28	4.252 to 4.410	0.158
27	4.097 to 4.252	0.155
26	3.939 to 4.097	0.158
25	3.783 to 3.939	0.156
24	3.624 to 3.783	0.159
23	3.469 to 3.624	0.155
22	3.310 to 3.469	0.159
21	3.153 to 3.310	0.157
20	2.996 to 3.153	0.157
19	2.839 to 2.996	0.157
18	2.679 to 2.839	0.160
17	2.524 to 2.679	0.155
16	2.363 to 2.524	0.161
15	2.206 to 2.363	0.157
14	2.048 to 2.206	0.158
13	1.890 to 2.048	0.158
12	1.730 to 1.890	0.160
11	1.573 to 1.730	0.157
10	1.413 to 1.573	0.160
9	1.255 to 1.413	0.158
8	1.095 to 1.255	0.160
7	0.935 to 1.095	0.160
6	0.775 to 0.935	0.160
5	0.615 to 0.775	0.160

TABLE 18-5 (Concluded)

CHANNEL	RANGE (VOLTS)	CHANNEL WIDTH (VOLTS)
4	0.454 to 0.615	0.161
3	0.293 to 0.454	0.161
2	0.133 to 0.293	0.160
1	0.025 to 0.133	0.108
0	— to 0.025	—

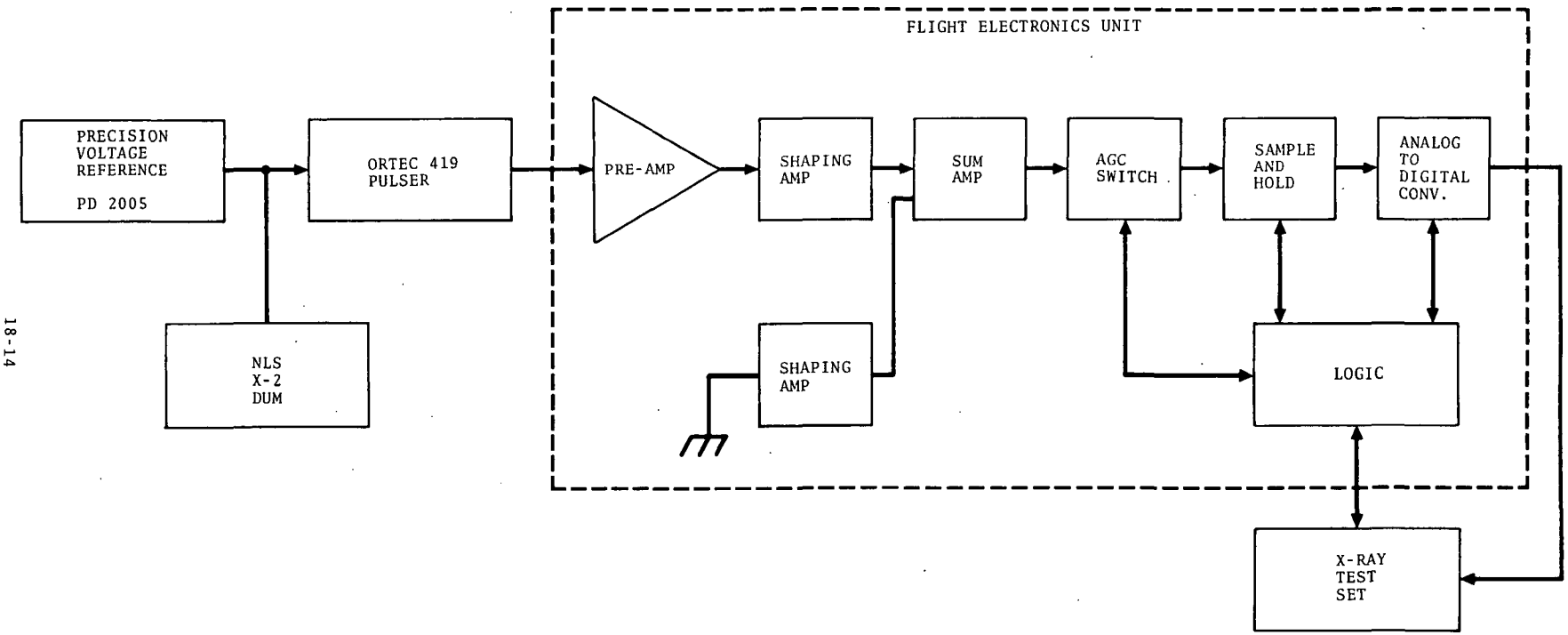


Figure 18-6. – Pulse-Height Calibration Test Hook-Up.

TABLE 18-6 RISE TIME DISCRIMINATION VS PULSE HEIGHT

CHANNEL	Pulse Rise Time (Nanoseconds)	% of 20,000 counts Producing Discriminator Bit
32	30	100%
32	50	0%
17	30	100%
17	50	0%
9	30	100%
9	50	0%
5	30	100%
5	50	0%
3	30	100%
3	50	0%
2	30	100%
2	50	0.7%

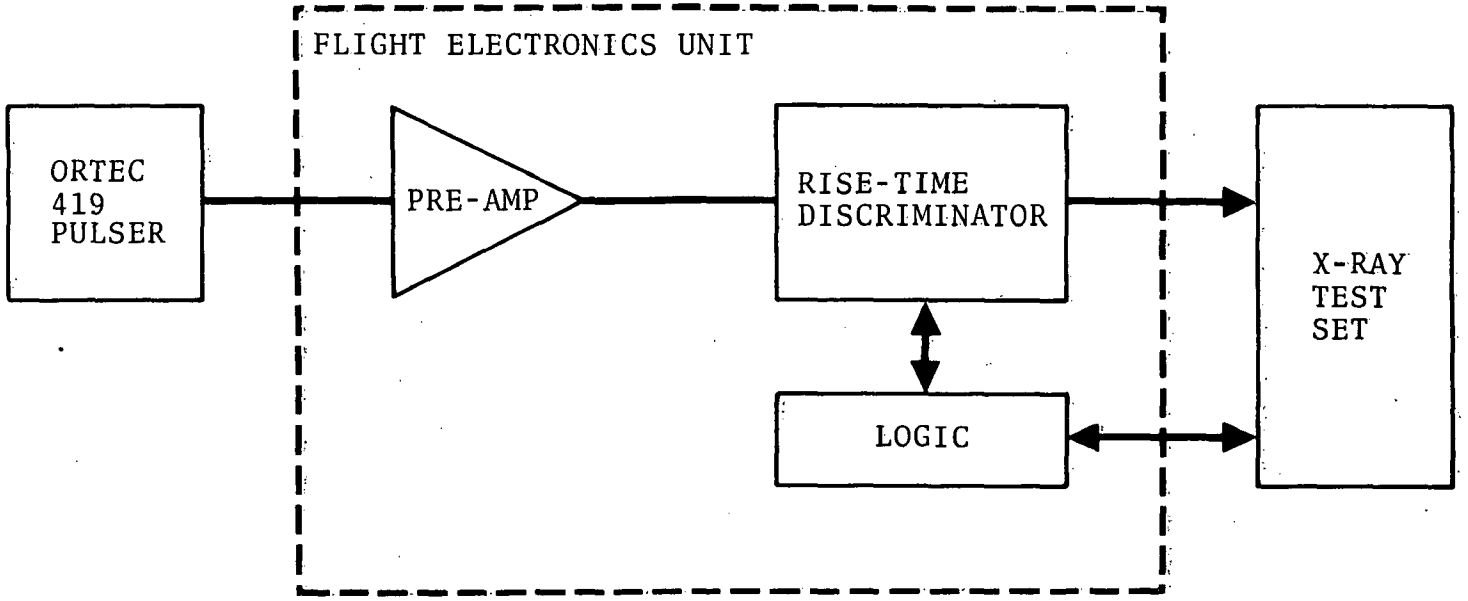


Figure 18-7. — Rise-Time Discriminator Test Hook-Up.

APPENDIX A

Feedback Control of Proportional Counter Gain

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A technique is described for stabilizing the gain of a gas proportional counter system. A feedback signal is derived from an auxiliary calibration counter, which controls the high voltage applied to the detectors. Theoretical speed and accuracy limitations are discussed. Performance of an actual system is described.

INTRODUCTION

WHEN applying gas proportional counting systems to x-ray spectroscopy, it is desirable that the system gain be maintained constant during the data collection. The amplification obtained from the gas counter is, however, critically dependent upon the applied high voltage, the gas pressure, and the presence of impurities. The stabilization technique described below provides rapid and accurate automatic control of system gain with respect to these variations. Briefly, an auxiliary calibration counter shares gas and high voltage with the main detector. The calibration counter is constantly irradiated by a radioactive x-ray emitter, and its performance is electronically monitored. A correction signal, equal to the time integral of a function of the gain error, is fed back to control the high voltage. This feedback loop is shown to have zero steady state average gain error. Furthermore, it can perform corrections quickly and can accommodate a large dynamic range.

I. TECHNIQUE

Consider the feedback loop shown in Fig. 1. A high voltage power supply in controlled by a voltage V. Its output will be taken to be a linear function of V. The high voltage is applied to the detectors to be stabilized, which will be assumed to exhibit an exponential dependence of gain with voltage. The detector signal is amplified electronically. At this point, the system gain G is defined as the ratio of the mean output pulse height to the x-ray energy. Then G can be described as a function of V by

$$G = H e^{SV} \quad (\text{V/keV}), \tag{1}$$

where H and S describe the system gain and control sensitivity, respectively. To close the loop, a discriminator is set at some threshold voltage y_0. The discriminator is so designed as to subtract an amount of charge Q from the storage capacitor C whenever a pulse exceeding y_0 is received; furthermore, it adds charge Q upon receipt of a pulse whose height is less than y_0. Consequently, the discriminator will adjust the system gain in such a manner as to keep the x-ray calibration peak centered on the threshold y_0. Quantitatively, in equilibrium the count rate above y_0 will equal the count rate below y_0. This loop differs fundamentally from that described by Brinkman and de Groene,[1] where a rate meter controls system gain. For example, in our circuit the average loop error is zero, independent of the counting rate.

II. DYNAMICS OF THE LOOP

We first calculate the behavior of the feedback loop, using an average dependence of discriminator output vs gain that ignores statistical rate fluctuations. Owing to the complexity of the resulting differential equation, the approach to equilibrium is described in two regimes: the large correction approximation and the small-error linear approximation. The loop time constant is then defined. Finally, a statistical perturbation analysis is presented, and the trade-off between fast loops (which are subject to increased gain jitter) and accurate loops (which are slow to correct errors) is discussed.

Let R represent the total count rate. If the pulses exhibit a Gaussian height distribution with a mean height E and standard deviation σ, the count rate R_1 of pulses exceeding the threshold y_0 will be

$$R_1 = R\int_{y_0/G}^{\infty} (2\pi\sigma^2)^{-\frac{1}{2}} \exp[-(x-E)^2/2\sigma^2]dx$$
$$= R\Phi\left[\frac{E}{\sigma}\left(1-\frac{G_0}{G}\right)\right],$$

where $G_0 = y_0/E$ is the equilibrium system gain and $\Phi(x)$ is the cumulative normal distribution. From the description of the discriminator, we note that the control voltage V decreases by Q/C for each pulse exceeding y_0 and increases by Q/C for each undersize pulse. Thus the rate of

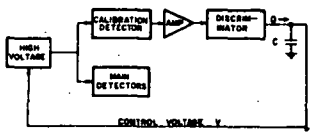

FIG. 1. Block diagram of the gain controlled feedback loop.

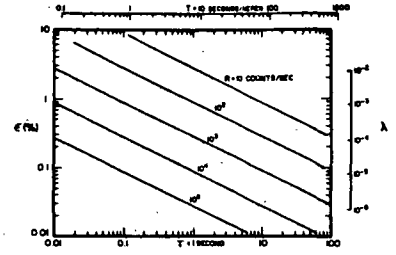

FIG. 2. Root mean square gain jitter ϵ vs time constant τ for several values of the count rate R. Auxiliary scales give $\lambda = QS/C$ in nepers per count and the large-signal time constant T in seconds per neper. Resolution = 10% rms.

change of V is

$$\frac{dV}{dt} = \frac{Q}{C}(\text{rate under } y_0 - \text{rate over } y_0) = \frac{QR}{C}\left\{1 - 2\Phi\left[\frac{E}{\sigma}\left(1 - \frac{G_0}{G}\right)\right]\right\}. \quad (2)$$

III. LARGE CORRECTIONS

For the case where the gain error is substantially greater then the detector resolution, Eq. (2) can be greatly simplified. For $(G-G_0)/G > \sigma/E$, and has $\Phi \approx 1$; if $(G-G_0)/G < \sim \sigma/E$, $\Phi \approx 0$. In either case, essentially all the corrections are in the same direction, and the control voltage moves with its maximum time derivative QR/C V/sec. Thus, the gain falls or rises exponentially with time at a rate of QRS/C Np/sec. The time required to span a large correction from gain G_1 to gain G_2 is

$$(C/QRS)\ln G_2/G_1 = T \ln G_2/G_1. \quad (3)$$

IV. SMALL CORRECTIONS

Equations (1) and (2) can be solved for small variations in gain by linearizing them. This procedure is accurate when the required correction is smaller than a standard deviation, that is, when $|G-G_0|/G < \sigma/E$. For the control voltage change $v = V - V_0$, we write

$$G = av + G_0$$

$$dv/dt = b(G_0 - G),$$

whose solution is

$$v = Ke^{-abt},$$

$$G = G_0 + aKe^{-abt}.$$

Here, K represents any initial error; it is seen to decay exponentially with time constant $1/ab$. These two factors can be obtained from Eqs. (1) and (2) by differentiation

$$a = SG,$$

$$b = (2/\pi)^{\frac{1}{2}} QRE/CG\sigma.$$

Hence, the time constant

$$\tau = \left(\frac{\pi}{2}\right)^{\frac{1}{2}} \frac{C}{QRS} \frac{\sigma}{E}. \quad (4)$$

V. FLUCTUATIONS

The feedback loop at equilibrium is constantly perturbed by the statistical nature of the consecutive gain determinations. On a short time scale, the control voltage V performs a random walk with step size Q/C and mean rate R. On a longer scale, however, the feedback removes the random walk divergence and limits the variance of V to a value

$$\text{var}(V) = (Q^2/C^2)(R\tau/2),$$

where τ represents the small perturbation time constant. Consequently, the root mean square (rms) gain variation ϵ will be

$$\epsilon = \left(\frac{\text{var}(G)}{G_0^2}\right)^{\frac{1}{2}} = \left(\frac{\pi}{8}\right)^{\frac{1}{2}} \left(\frac{SQ}{C} \frac{\sigma}{E}\right)^{\frac{1}{2}}. \quad (5)$$

VI. SYSTEM DESIGN

The performance of the feedback loop has been described by its response time for large corrections, by its time constant for correcting small gain errors, and by its rms gain jitter. Equations (3), (4), and (5) identify the dependence of these properties upon resolution, count rate, and the parameter $\lambda = QS/C$, which describes the fractional change in system gain caused by a single count. The system designer is usually faced with a given detector resolution, for which R and λ must be chosen to provide sufficient speed and accuracy. This choice is conveniently made with the help of a plot of the rms gain jitter ϵ vs τ for several values of the count rate R. In Fig. 2, an example is given for a detector whose resolution $\sigma/E = 10\%$ (23.6% FWHM). In some systems where large gain corrections will be required, the pull-in time per neper T will be the dominant consideration. A scale for T has been shown in Fig. 2, again for 10% rms resolution.

VII. DIGITAL CONTROL

Because the feedback system described above has equally spaced discrete states, a digital servosystem with identical properties can be constructed. The storage function of the capacitor would be performed by a register capable of being incremented up and down by the discriminator. The control voltage must then be obtained from this register by a digital-to-analog converter.

VIII. PERFORMANCE

The accuracy with which one proportional counter can stabilize the amplification of another proportional counter depends, not only upon the accuracy of the feedback loop, but also upon the degree to which the detectors respond equally to gain perturbing influences. Consequently, two kinds of system tests have been performed: measurements of the calibration loop stability, and measurements of the stability of the indirectly controlled proportional counter.

A gain controlled system was assembled as shown in Fig. 1, using series flow proportional counters fed with an argon–methane gas mixture at 760 Torr. These cylindrical side-window counters had anode and cathode radii of 25 μ and 13 mm, respectively. The gas gain was found to vary as exp $(U/120)$. Gain control was obtained with the use of a high voltage converter whose output U varied as $U=1200+200V$ V. The combination then yielded a control sensitivity $S=1.67$ Np/V. For an x-ray energy $E=5.9$ keV, the detector resolution σ/E was approximately 10%. The amplifier employed a 1 μsec clipping time constant and was set to a nominal gain of 10^{12} V/C. From the pulse response data of Mathieson,[2] a discriminator setting $y_0=2.5$ V should correspond to a gas gain of approximately 30 000. The details of the discriminator are shown in Fig. 3. With the values given, $Q/C=1$ mV/count.

In operation, the observed performance of the system agreed closely with the calculated performance. For example, with $R=11$ counts/sec, the measured pull-in time T was 60 ± 5 sec, as compared with the theoretical 54 sec. At higher count rates, even better agreement was obtained. The system gain jitter was measured by calculating the standard deviation of 100 well spaced values of the control voltage. The measured standard deviation (5.7 ± 1 mV) agrees with the predicted standard deviation of 6 mV, and corresponds to an rms gain jitter of 1%. Gain drift of this feedback loop was monitored with a pulse height analyzer; over a 24 h period, the gain varied less than one channel from the channel 93 x-ray peak location. Similar runs without gain stabilization revealed gain drifts of 10 to 20%, presumably owing to changes in barometric pressure, temperature, or gas composition.

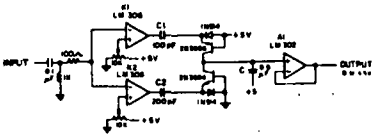

FIG. 3. Schematic diagram of the discriminator servo. Comparator K1 triggers on any pulse exceeding the amplifier noise level; K2 triggers only if a pulse exceeds the desired threshold y_0. For values shown, $Q/C=1$ mV/count.

Gain measurements were also performed on the indirectly controlled gas counter. Accurate stabilization requires that this detector have the same dimensions as the calibration counter, in order that the control sensitivities S be equal: A 1% difference in anode radius will cause a $\frac{1}{4}$% difference in S. Representative spectra were accumulated over several days, using a 5.9 keV ^{55}Fe–^{55}Mn x-ray source at count rates from 50 to 600 counts/sec. The gain drift did not exceed 3% over any 24 h period.

ACKNOWLEDGMENTS

It is a pleasure to acknowledge the many useful discussions with G. J. de Vries. This work was supported in part by the National Aeronautics and Space Administration Grant NGR 05-003-278.

[1] A. C. Brinkman and P. de Groene, Nucl. Instrum. Methods 66, 316 (1968).
[2] E. Mathieson, Nucl. Instrum. Methods 72, 355 (1969).