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NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Technical Report 32-1526

Volume IX

The Deep Space Network

*Progress Report
For March and April 1972*

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**JET PROPULSION LABORATORY
CALIFORNIA INSTITUTE OF TECHNOLOGY
PASADENA, CALIFORNIA**

June 15, 1972

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Preface

This report series presents progress on DSN supporting research and technology, advanced development and engineering, implementation, and operations which pertain to mission-independent or multiple-mission development as well as to support of flight projects. Each issue presents material in some, but not all, of the following categories in the order indicated.

Description of the DSN

Mission Support

- Interplanetary Flight Projects
- Planetary Flight Projects
- Manned Space Flight Project
- Advanced Flight Projects

Radio Science

Advanced Engineering

- Tracking and Navigational Accuracy Analysis
- Communications Systems Research
- Communications Elements Research
- Supporting Research and Technology

Development and Implementation

- Space Flight Operations Facility Development
- Ground Communications Facility Development
- Deep Space Instrumentation Facility Development
- DSN Projects and Systems Development

Operations and Facilities

- DSN Operations
- Space Flight Operations Facility Operations
- Ground Communications Facility Operations
- Deep Space Instrumentation Facility Operations
- Facility Engineering

In each issue, the part entitled "Description of the DSN" describes the functions and facilities of the DSN and may report the current configuration of one of the six DSN systems (tracking, telemetry, command, monitoring, simulation, and operations control).

The work described in this report series is either performed or managed by the Tracking and Data Acquisition organization of JPL for NASA.

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DSN Functions and Facilities

N. A. Renzetti
Mission Support Office

The objectives, functions, and organization of the Deep Space Network are summarized. The Deep Space Instrumentation Facility, the Ground Communications Facility, and the Space Flight Operations Facility are described.

The Deep Space Network (DSN), established by the NASA Office of Tracking and Data Acquisition under the system management and technical direction of JPL, is designed for two-way communications with unmanned spacecraft traveling approximately 16,000 km (10,000 mi) from Earth to planetary distances. It supports, or has supported, the following NASA deep space exploration projects: *Ranger*, *Surveyor*, *Mariner Venus 1962*, *Mariner Mars 1964*, *Mariner Venus 67*, *Mariner Mars 1969*, *Mariner Mars 1971* (JPL); *Lunar Orbiter* and *Viking* (Langley Research Center); *Pioneer* (Ames Research Center); *Helios* (West Germany); and *Apollo* (Manned Spacecraft Center), to supplement the Manned Space Flight Network (MSFN).

The Deep Space Network is one of two NASA networks. The other, known as the Spaceflight Tracking and Data Network, is under the system management and technical direction of the Goddard Space Flight Center. Its function is to support manned and unmanned Earth-orbiting and lunar scientific and communications satellites. Although the DSN was concerned with unmanned lunar spacecraft in its early years, its primary objective now and into the future is to continue its support of planetary and interplanetary flight projects. It has been a development objec-

tive that the network capability be kept at the state of the art of telecommunications and data handling and that it support as many flight projects as possible with a minimum of mission-dependent hardware and software. It provides direct support of each project through that project's tracking and data system. This management element, in concert with the telecommunications and mission operations personnel of the project, is responsible for the design and operation of the hardware and software which are required for the conduct of flight operation. The organization and procedures necessary to carry out these activities are described in Ref. 1.

The DSN function, in supporting a flight project by tracking the spacecraft, is characterized by six DSN systems:

- (1) DSN Tracking System. Generates radio metric data; i.e., angles, one- and two-way doppler and range.
- (2) DSN Telemetry System. Receives, records, and retransmits engineering and scientific data generated in the spacecraft.
- (3) DSN Command System. Sends coded signals to the spacecraft in order to initiate spacecraft functions in flight.

- (4) DSN Monitor System. Instruments, transmits, records, and displays those parameters of the DSN that measure its performance.
- (5) DSN Simulation System. Provides computer-based facilities in order to test and train network functions and assist the flight project in carrying out similar functions for its Mission Operations System.
- (6) DSN Operations Control. Provides the hardware and software, personnel, real-time and non-real-time operational direction of the network, and primary interface with the flight projects Mission Operations personnel.

The facilities needed to carry out these functions have evolved in three technical areas: (1) the deep space stations and the telecommunications interface through the RF link with the spacecraft is known as the Deep Space Instrumentation Facility (DSIF); (2) the Earth-based point-to-point voice and data communications from the stations to the control center is known as the Ground Communications Facility (GCF); (3) the control center, both for network control function and mission control support, is known as the Space Flight Operations Facility (SFOF).

I. Deep Space Instrumentation Facility

A. Tracking and Data Acquisition Facilities

A world-wide set of deep space stations (DSSs) with large antennas, low-noise phase-lock receiving systems, and high-power transmitters provide radio communications with spacecraft. The DSSs and the deep space communications complexes (DSCCs) they comprise are given in Table 1.

Radio contact with a spacecraft usually begins when the spacecraft is on the launch vehicle at Cape Kennedy, and it is maintained throughout the mission. The early part of the trajectory is covered by selected network stations of the Air Force Eastern Test Range (AFETR) and the MSFN of the Goddard Space Flight Center,¹ Normally, two-way communications are established between the spacecraft and the DSN within 30 min after the spacecraft has been injected into lunar, planetary, or interplanetary flight. A compatibility test station at Cape Kennedy (discussed later) monitors the spacecraft continuously dur-

ing the launch phase until it passes over the local horizon. The deep space phase begins with acquisition by either DSS 51, 41, or 42. These and the remaining DSSs given in Table 1 provide radio communications to the end of the flight.

To enable continuous radio contact with spacecraft, the DSSs are located approximately 120 deg apart in longitude; thus, a spacecraft in deep space flight is always within the field-of-view of at least one DSS, and for several hours each day may be seen by two DSSs. Furthermore, since most spacecraft on deep space missions travel within 30 deg of the equatorial plane, the DSSs are located within latitudes of 45 deg north or south of the equator. All DSSs operate at S-band frequencies: 2110-2120 MHz for Earth-to-spacecraft transmission and 2290-2300 MHz for spacecraft-to-Earth transmission.

To provide sufficient tracking capability to enable useful data returns from around the planets and from the edge of the solar system, a 64-m (210-ft) diam antenna network will be required. Two additional 64-m (210-ft) diam antenna DSSs are under construction at Madrid and Canberra, which will operate in conjunction with DSS 14 to provide this capability. These stations are scheduled to be operational by the middle of 1973.

B. Compatibility Test Facilities

In 1959, a mobile L-band compatibility test station was established at Cape Kennedy to verify flight-spacecraft-DSN compatibility prior to the launch of the *Ranger* and *Mariner* Venus 1962 spacecraft. Experience revealed the need for a permanent facility at Cape Kennedy for this function. An S-band compatibility test station with a 1.2-m (4-ft) diam antenna became operational in 1965. In addition to supporting the preflight compatibility tests, this station monitors the spacecraft continuously during the launch phase until it passes over the local horizon.

Spacecraft telecommunications compatibility in the design and prototype development phases was formerly verified by tests at the Goldstone DSCC. To provide a more economical means for conducting such work and because of the increasing use of multiple-mission telemetry and command equipment by the DSN, a compatibility test area (CTA) was established at JPL in 1968. In all essential characteristics, the configuration of this facility is identical to that of the 26-m (85-ft) and 64-m (210-ft) diam antenna stations.

The JPL CTA is used during spacecraft system tests to establish the compatibility with the DSN of the proof test

¹The 9-m (30-ft) diam antenna station established by the DSN on Ascension Island during 1965 to act in conjunction with the MSFN orbital support 9-m (30-ft) diam antenna station was transferred to the MSFN in July 1968.

model and development models of spacecraft, and the Cape Kennedy compatibility test station is used for final flight spacecraft compatibility validation testing prior to launch.

II. Ground Communications Facility

The GCF provides voice, high-speed data, wideband data, and teletype communications between the SFOF and the DSSs. In providing these capabilities, the GCF uses the facilities of the worldwide NASA Communications Network (NASCOM)² for all long distance circuits, except those between the SFOF and the Goldstone DSCC. Communications between the Goldstone DSCC and the SFOF are provided by a microwave link directly leased by the DSN from a common carrier.

Early missions were supported by voice and teletype circuits only, but increased data rates necessitated the

²Managed and directed by the Goddard Space Flight Center.

use of high-speed circuits for all DSSs, plus wideband circuits for some stations.

III. Space Flight Operations Facility

Network and mission control functions are performed at the SFOF at JPL. The SFOF receives data from all DSSs and processes that information required by the flight project to conduct mission operations. The following functions are carried out: (1) real-time processing and display of radio metric data; (2) real-time and non-real-time processing and display of telemetry data; (3) simulation of flight operations; (4) near-real-time evaluation of DSN performance; (5) operations control, and status and operational data display; and (6) general support such as internal communications by telephone, intercom, public address, closed-circuit TV, documentation, and reproduction of data packages. Master data records of science data received from spacecraft are generated. Technical areas are provided for flight project personnel who analyze spacecraft performance, trajectories, and generation of commands.

Reference

1. *The Deep Space Network*, Space Programs Summary 37-50, Vol. II, pp. 15-17. Jet Propulsion Laboratory, Pasadena, Calif., Mar. 31, 1968.

Table 1. Tracking and data acquisition stations of the DSN

DSCC	Location	DSS	DSS serial designation	Antenna		Year of initial operation
				Diameter, m (ft)	Type of mounting	
Goldstone	California	Pioneer	11	26 (85)	Polar	1958
		Echo	12	26 (85)	Polar	1962
		(Venus) ^a	13	26 (85)	Az-El	1962
		Mars	14	64 (210)	Az-El	1966
—	Australia	Woomera	41	26 (85)	Polar	1960
Tidbinbilla	Australia	Weemala	42	26 (85)	Polar	1965
		(formerly Tidbinbilla)				
		Ballima (formerly Booroomba)	43	64 (210)	Az-El	Under construction
—	South Africa	Johannesburg	51	26 (85)	Polar	1961
Madrid	Spain	Robledo	61	26 (85)	Polar	1965
		Cebreros	62	26 (85)	Polar	1967
		Robledo	63	64 (210)	Az-El	Under construction

^aA research-and-development facility used to demonstrate the feasibility of new equipment and methods to be integrated into the operational network. Besides the 26-m (85-ft) diam az-el-mounted antenna, DSS 13 has a 9-m (30-ft) diam az-el-mounted antenna that is used for testing the design of new equipment and support of ground-based radio science.

DSN Monitor Performance Program

J. E. Allen

DSN Engineering and Operations Section

This report provides: (1) a general description of the programs used by DSN monitor analysts in the generation of the weekly and monthly performance summary reports, and (2) the format guide used by the DSN real-time analyst to assist in interpreting the formatted data.

I. Introduction

The DSN monitor system has the responsibility of reporting the performance of the DSN and to ensure that each element of the DSN is properly configured for anomaly-free data flow.

To assist the DSN monitor analysts in the performance of their duties, the Summary Performance Report and the Digital Television (DTV) Format Guide programs were developed and are used to supplement the manual collection of data for analysis and to make real-time determination of the DSN configuration status.

II. Summary Performance Report

Prior to March 1, 1972 the DSN Monitor Weekly and Monthly Performance Report was manually generated and consumed two man days per week for the output. The report contained a listing of the tracking time per deep space station, two-way lock time, number of commands transmitted to the spacecraft from each station, and graphs of the receiver's residual signal strength (AGC)

and signal-to-noise ratio (SNR). Additionally, it contained the up time and down time of the 360/75 computer, the 3100 computer, and DSIF's digital instrumentation system (DIS).

To reduce the man hours involved in the generation of the Summary Performance Report, the function was computerized. The computerized version proved to be more reliable and more dynamic in response to new requirements. The net results were a more meaningful report to the users.

In real-time, the data are collected and coded for key-punching and become the data base for the Traceability and Reporting Program (TRP), which is a file management program providing user visibility in near real-time and/or in an archival mode of data generated by DSN system (Ref. 1).

The program operates on either the 360/75 or 370/155 system. The information is retained within the program and retrieved on command. Depending on the requirements, the data are collected, combined, computed, and

processed according to the pre-established algorithm within the program. The data can be organized into the format desired and extracted on an independent time base, e.g., weekly basis, daily, monthly or cumulative.

Presently the Summary Performance Report is DSN monitor-based, but the provision exists to include DSN tracking, DSN telemetry, and DSN command parameters. The next evaluation of the software program will include parameters from the above three systems and will contain DSN network data on both quantity and quality of data generated within the DSN.

Since the initiation of the automatic generation of the DSN Performance Summary Report, the report users state that they have a better understanding of the DSN, and that they have been able to increase the reliability of their individual system.

See Fig. 1 for an example of the summary performance report generated by the DSN monitor analyst.

Since the requirements for each project are different, the DSN Monitor Performance Summary Report must necessarily be dynamic. The intent is to continue to update the report so that it can serve the needs of each project and DSN management, and provide greater visibility of the DSN and the total support provided by the DSN to the various projects.

III. Format Guide

Within the DSN, the data available through DTV are processed by the DSN Monitor Program operating in the 360/75 Real-Time Software Programs.

The Monitor System is responsible for the output of the DSN DTV Software and the validity of the data extracted

and displayed via DTV Formats. Therefore, a guide was generated showing the definition of the mnemonics used for each format, the High Speed Data (HSD) location, and the algorithm used to generate the displayed parameters.

A software program was generated with a dynamic data base to operate in the Univac 1108 computer. The program has the capability to be updated as changes to the formats are made and to include any new formats that are generated within the DSN systems. As updates are made to the software, a new publication of the "format guide" is made available to Monitor data users.

The "format guide" shows the contents of each format. Presently there are 39 operational formats in use by the DSN. Specifically, the guide shows mnemonic and mnemonic definition, display, data source, word and bit location within the HSD block of the displayed parameter.

With this information, each user can determine if the formats are being processed correctly. In the event that errors show up, the users are encouraged to generate a Discrepancy Report on the erroneous format or parameter within the formats. In this way changes can be initiated to correct format deficiencies.

The DTV format guide program allows the user to generate up to 20 copies of either a single DTV format definition or the entire DTV format catalog. This capability is available to anyone who is familiar with the program.

The program provides the user the ability to edit the DTV format catalog from an 1108 demand terminal. The editing capability includes the provision to add new formats, change parameters within an individual format, and change the algorithm that generates a particular parameter display. See Table 1 for an example of the program output.

Reference

1. Miccio, J. A., "DSN Traceability and Reporting Program: Micrographic Application," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VII, pp. 185-187. Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1972.

Table 1. Example of program output

MNEMONIC	DEFINITION	DISPLAY	DATA SOURCE	WORD	BITS
DSS	STATION I.D.	NN	PERF/STAT	3	18-24
SC	SPACECRAFT NO.	NN	PERF/STAT	26	16-24
SD	STANDARD DEVIATION	+-.NNN	PERF/STAT	27	16-24
	RECEIVER 1				
	RECEIVER 2				
SPE	RECEIVER STATIC PHASE ERROR	+-.NNN	PERF/STAT	30	1-10
	RECEIVER 1				
	RECEIVER 2				
TMB/W	TELEMETRY BANDWIDTH- BIT CONFIG:				
	0111	4.5K	PERF/STAT	20	4-7
	1011	20K	PERF/STAT	20	4-7
	1101	420K	PERF/STAT	20	4-7
	1110	3.3M	PERF/STAT	20	4-7
ABW	RECEIVER AGC BANDWIDTH- RECEIVER 1				
	BIT CONFIG: 101	N	PERF/STAT	20	8-10
	110	M	PERF/STAT	20	8-10
	011	W	PERF/STAT	20	8-10
	RECEIVER 2				
	101	N	PERF/STAT	19	8-10
	110	M	PERF/STAT	19	8-1
	011	W	PERF/STAT	19	8-10
RFL	RECEIVER [R.F.] LOOP BANDWIDTH -RECEIVER 1				
	BIT CONFIG: 0111	NAR	PERF/STAT	20	11-14
	1101	MED	PERF/STAT	20	11-14
	1011	WID	PERF/STAT	20	11-14
	RCV1 ONLY: 1110	3	PERF/STAT	20	11-14
	0111	NAR	PERF/STAT	19	11-14
	1101	MED	PERF/STAT	19	11-14
	1011	WID	PERF/STAT	19	11-14
VC	RECEIVER VCO NUMBER:				
	RECEIVER 1	N	PERF/STAT	19	19-22
	RECEIVER 2	N	PERF/STAT	19	15-18
	RECEIVER LOCK STATUS	TN/OUT			
	RECEIVER 1		PERF/STAT	20	3
	RECEIVER 2		PERF/STAT	19	3
HA-ERR	HOOR ANGLE ERROR	+ OR --.NNNN	PERF/STAT	30	11-17
HA-RES	HOOR ANGLE RESIDUAL	+ OR --.NNNN	PERF/STAT	39-40	20-05
DECERR	DECLINATION ANGLE ERROR	+ OR --.NNNN	PERF/STAT	30	18-24
DECRES	DECLINATION ANGLE RESIDUAL	+ OR --.NNNN	PERF/STAT	40	6-15
DOP	DOPPLER MODE	1,2,OR 3	PERF/STAT	18	1-4
RNL	RANGE RECEIVER LOOP BANDWIDTH				
	BIT CONFIG: 011	NAR	PERF/STAT	20	15-17
	101	MED	PERF/STAT	20	15-17
	110	WID	PERF/STAT	20	15-17
MOD	TRANSMITTER MODULATION STATE				
	BIT CONFIG: 1011	MOO	PERF/STAT	18	5,11,12,14
	1110	TMO	PERF/STAT	18	5,11,12,14
	1101	CMA	PERF/STAT	18	5,11,12,14
	1111	CMB	PERF/STAT	18	5,11,12,14
	0011	RMO	PERF/STAT	18	5,11,12,14
	0101	RCA	PERF/STAT	18	5,11,12,14
	0111	RCB	PERF/STAT	18	5,11,12,14

Table 1 (contd)

MNEMONIC	DEFINITION	DISPLAY	DATA SOURCE	WORD	BITS
DOPRESM	DOPPLER RESIDUAL MEAN	RTM	PERF/STAT	18	5,11,12,14
DOP-SD	DOPPLER STANDARD DEVIATION	+N.NNNN	PERF/STAT	36	1-17
RNG-RESM	RANGE RESIDUAL MEAN	+-.NNNN	PERF/STAT	36	18-24
RNG-SD	RANGE STANDARD DEVIATION	+NN.NNNN	PERF/STAT	37	7-24
TDHRT	TRACKING DATA SAMPLE RATE	+-.NNNN	PERF/STAT	38	1-13
RNG/DOP	RANGE DOPPLER MEAN	NN	PERF/STAT	31	11-24
R/D-SD	RANGE DOPPLER STANDARD DEVIATION	+N.NNNN	PERF/STAT	38-39	14-6
TFREQ	TRANSMITTER VCO FREQUENCY	+-.NNNN	PERF/STAT	39	7-19
TDH DCC	TRACKING DATA CONDITION CODE	NNNN	PERF/STAT	35	1-14
CMAB	COMMAND MODE SELECT	NNNN	PERF/STAT	33	11-24
		CALL	PERF/STAT	41	1-24
		CAL2	PERF/STAT	41	1-24
		IDL 1	PERF/STAT	41	1-24
		IDL2	PERF/STAT	41	1-24
		ACTV	PERF/STAT	41	1-24
		ABRT	PERF/STAT	41	1-24
TCP	TCP ACTIVE RECEIPT OF TRANSMISSION	TP1 OR TP2	PERF/STAT	42	19-21
C	COMMAND RECEIVED IN LAST 5 SECONDS	/ OR *	PERF/STAT	42	19
M	TCP ACTIVE FOR LAST COMMAND	N	PERF/STAT	41	3<15
A	ABORT DETECTED IN LAST 5 SECONDS	/ OR *	PERF/STAT	42	22-24
TCP1SN	TCP1 SIGNAL TO NOISE RATIO	+NN.NN	PERF/STAT	43	13-24
TCP2SN	TCP2 SIGNAL TO NOISE RATIO	+NN.NN	PERF/STAT	45	13-24
SSA1SN	SYMBOL SYNCHRONIZER 1 SIGNAL TO NOISE RATIO	+NN.NN	PERF/STAT	44	1-12
SSA2SN	SSA2 SIGNAL TO NOISE RATIO	+NN.NN	PERF/STAT	46	1-12
BDA1SN	BLOCK DECODER 1 SIGNAL TO NOISE RATIO	+NN.NN	PERF/STAT	44	13-24
BDA2SN	BDA 2 SIGNAL TO NOISE RATIO	+NN.NN	PERF/STAT	46	13-24
TCP-1					
R	CHANNEL 1 RECEIVER LOCK STATUS	/ OR *	PERF/STAT	43	5
D	CHANNEL 1 DEMOD LOCK STATUS	/ OR *	PERF/STAT	43	6
S	CHANNEL 1 BIT SYNC LOOP LOCK STATUS	/ OR *	PERF/STAT	43	7
R	CHANNEL 2 RECEIVER LOCK STATUS	/ OR *	PERF/STAT	43	8
D	CHANNEL 2 DEMOD LOCK STATUS	/ OR *	PERF/STAT	43	9
S	CHANNEL 2 BIT SYNC LOOP LOCK STATUS	/ OR *	PERF/STAT	43	10
Y	CHANNEL 2 SSA LOCK	/ OR *	PERF/STAT	43	11
B	CHANNEL 2 BDA LOCK STATUS	/ OR *	PERF/STAT	43	12
TCP-2	SAME AS TCP-1				
R	CHANNEL 1 RECEIVER LOCK STATUS	/ OR *	PERF/STAT	45	5
D	CHANNEL 1 DEMOD LOCK STATUS	/ OR *	PERF/STAT	45	6
S	CHANNEL 1 BIT SYNC LOOP LOCK STATUS	/ OR *	PERF/STAT	45	7
R	CHANNEL 2 RECEIVER LOCK STATUS	/ OR *	PERF/STAT	45	8
D	CHANNEL 2 DEMOD LOCK STATUS	/ OR *	PERF/STAT	45	9
S	CHANNEL 2 BIT SYNC LOOP LOCK STATUS	/ OR *	PERF/STAT	45	10
Y	CHANNEL 2 SSA LOCK	/ OR *	PERF/STAT	45	11
B	CHANNEL 2 BDA LOCK STATUS	/ OR *	PERF/STAT	45	12
TCP1					
T	TRANSMITTER STATUS	/ OR *	PERF/STAT	41	1
E	EXCITER FREQUENCY LIMIT	/ OR *	PERF/STAT	41	2
C	COMMAND MODULATION STATUS	/ OR *	PERF/STAT	41	3
P	PN MODULATION STATUS	/ OR *	PERF/STAT	41	4
TCP2	SAME AS TCP1				
T		/ OR *	PERF/STAT	41	13
E		/ OR *	PERF/STAT	41	14

Table 1 (contd)

MNEMONIC	DEFINITION	DISPLAY	DATA SOURCE	WORD	BITS
C					
P					
TM	TCP TELEMETRY STATUS	/ OR *	PERF/STAT	41	15
D	DIS DOPPLER PROCESSOR STATUS	/ OR *	PERF/STAT	41	16
A	DIS ANGLE DATA PROCESSOR STATUS	/ OR *	PERF/STAT	49	1-2
R	DIS RANGE DATA PROCESSOR STATUS	/ OR *	PERF/STAT	49	4
L	DIS LOG TAPE STATUS	/ OR *	PERF/STAT	49	5
H	DIS HIGH SPEED RECEIVER STATUS	/ OR *	PERF/STAT	49	6
C	TCP1 COMMAND DATA INDICATOR	/ OR *	PERF/STAT	49	7
D	TCP2 COMMAND DATA INDICATOR	/ OR *	PERF/STAT	49	8
MP0	SCM POLARIZATION	/ OR *	PERF/STAT	49	10
CS	RECEIVER INPUT CHANNEL SELECT	RCP/LCP	PERF/STAT	49	11
AP0	SAA POLARIZATION	M1,M2,BP,NA	PERF/STAT	24	4-6
UR	MICROWAVE INPUT SELECT:	RCP/LCP	PERF/STAT	24	10-13
	MASER 1, RCV 1	11	PERF/STAT	24	7-9
	MASER 1, RCV 2	12	PERF/STAT	24	15-16
	MASER 2, RCV 1	21	PERF/STAT	24	15-16
	MASER 2, RCV 2	22	PERF/STAT	24	15-16
SDA	SIGNAL UEMOD. ASSEMBLY HEADER				
INS	SDA INPUT SELECT				
	SDA 1 BIT CONFIG. 11	11	PERF/STAT	24	15-16
		01	PERF/STAT	24	15-16
		10	PERF/STAT	24	15-16
INS	SDA-2 BIT CONFIG. SAME AS SDA-1	RX1	PERF/STAT	13	1-2
INS	SDA-3 BIT CONFIG SAME AS SDA-1	RX2	PERF/STAT	13	1-2
INS	SDA-4 BIT CONFIG SAME AS SDA-1	AIS	PERF/STAT	13	1-2
OTS	SDA OUTPUT SELECT				
	SDA-1 BIT CONFIG: 01				
		10			
		11			
OTS	SDA-2 SAME AS SDA-1	RX1	PERF/STAT	13	3-4
OTS	SDA-3 SAME AS SDA-1	AIS	PERF/STAT	13	3-4
OTS	SDA-4 SAME AS SDA-1	MMT	PERF/STAT	13	3-4
DB	SDA INPUT ATTENUATION				
	SDA-1 BIT CONFIG: 1111				
		1110	PERF/STAT	13	5-8
		1101	PERF/STAT	13	5-8
		1100	PERF/STAT	13	5-8
		1011	PERF/STAT	13	5-8
		1010	PERF/STAT	13	5-8
		1001	PERF/STAT	13	5-8
		1000	PERF/STAT	13	5-8
		0111	PERF/STAT	13	5-8
		0110	PERF/STAT	13	5-8
		0101	PERF/STAT	13	5-8
		0100	PERF/STAT	13	5-8
		0011	PERF/STAT	13	5-8
DB	SDA-2 SAME AS SDA-1				
DB	SDA-3 SAME AS SDA-1				
DB	SDA-4 SAME AS SDA-1				
BW	SDA BANDWIDTH SELECT				
	SDA-1 BIT CONFIG: 01				
		NAR	PERF/STAT	13	9-10
			PERF/STAT	13	9-10
			PERF/STAT	13	9-10
			PERF/STAT	13	9-10
			PERF/STAT	13	9-10
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			PERF/STAT	13	9-10
			PERF/STAT	13	9-10
			PERF/STAT	13	9-10

Table 1 (contd)

MNEMONIC	DEFINITION	DISPLAY	DATA SOURCE	WORD	BITS
SYMR	10	MED	PERF/STAT	13	9-10
	11	WID	PERF/STAT	13	9-10
	SDA-2 SAME AS SDA-1		PERF/STAT	14	3-4
	SDA-3 SAME AS SDA-1		PERF/STAT	14	21-22
	SDA-4 SAME AS SDA-1		PERF/STAT	15	15-16
	SDA SYMBOL RATE SELECT				
	SDA-1 BIT CONFIG:				
	0001	5.6	PERF/STAT	13	12-15
	0010	12	PERF/STAT	13	12-15
	0011	27	PERF/STAT	13	12-15
	0100	56	PERF/STAT	13	12-15
	0101	120	PERF/STAT	13	12-15
	0110	270	PERF/STAT	13	12-15
	0111	560	PERF/STAT	13	12-15
	1000	1200	PERF/STAT	13	12-15
	1001	2700	PERF/STAT	13	12-15
RA	1010	5600	PERF/STAT	13	12-15
	1011	12K	PERF/STAT	13	12-15
	1100	27K	PERF/STAT	13	12-15
	1101	56K	PERF/STAT	13	12-15
	1110	86K	PERF/STAT	13	12-15
	SDA-2 SAME AS SDA-1		PERF/STAT	14	6-9
	SDA-3 SAME AS SDA-1		PERF/STAT	14-15	24-3
	SDA-4 SAME AS SDA-1		PERF/STAT	15	18-21
	SYNTHESIZER RANGE				
	SDA-1	1X OR 10	PERF/STAT	13	16
SFQ	SDA-2	1X OR 10	PERF/STAT	14	10
	SDA-3	1X OR 10	PERF/STAT	15	4
	SDA-4	1X OR 10	PERF/STAT	15	22
	SYNTHESIZER FREQUENCY STANDARD				
	SDA-1	INT/EXT	PERF/STAT	13	17
L	SDA-2	INT/EXT	PERF/STAT	14	11
	SDA-3	INT/EXT	PERF/STAT	15	5
	SDA-4	INT/EXT	PERF/STAT	15	23
	SDA LOCK STATUS				
	SDA-1	/ OR *	PERF/STAT	13	18
	SDA-2	/ OR *	PERF/STAT	14	12
	SDA-3	/ OR *	PERF/STAT	15	6
	SDA-4	/ OR *	PERF/STAT	15	24

	Deep Space Station							
	11	12	14	41	42	51	61	62
MM actual track time, h	0.0	28.31	496.89	205.27	27.58	0.0	0.0	360.21
MM passes tracked	0	9	40	23	6	0	0	38
PN actual track time, h	118.95	102.27	16.39	54.15	247.92	263.02	49.50	0.0
PN passes tracked	17	14	3	6	24	30	8	0
MM scheduled track time, h	0.0	30.33	507.11	212.12	27.00	0.0	0.0	361.01
PN scheduled track time, h	121.07	105.17	16.18	57.50	251.70	262.70	50.07	0.0
DIS down time, h	N/A	0.55	26.69	0.55	N/A	0.0	N/A	0.24
Total DIS outages	N/A	2	8	2	N/A	0	N/A	2
Total LGWR	N/A	21,697	85,338	41,640	N/A	18,515	N/A	60,965
Total LGER	N/A	13	7372	274	N/A	35	N/A	78
% Scheduled track	98.2%	96.4%	98.0%	96.2%	98.9%	100%	98.9%	99.8%
% DIS support	N/A	96.0%	94.8%	99.7%	N/A	100%	N/A	99.9%
LGWR/hour	N/A	166.9	175.4	165.6	N/A	177.8	N/A	169.4
LGER/hour	N/A	0.1	15.2	1.1	N/A	0.34	N/A	0.22
Mean time between failures, failures, h	N/A	65.02	60.82	129.44	N/A	No failures	N/A	180.0
Average duration of each failure, h	N/A	0.28	3.34	0.28	N/A	-	N/A	0.12

SFOF Systems		
	360/75	3100/DTV
Scheduled support, h	978.84	960.00
Duration of scheduled outages, h	8.31	0.00
Number of scheduled outages	27	0
Duration of unscheduled outages, h	17.71	2.52
Number of unscheduled outages	99	15
% Scheduled support	98.1%	99.7%
Mean time between failures, h	9.71	63.88
Average duration of each failure, h	0.18	0.17

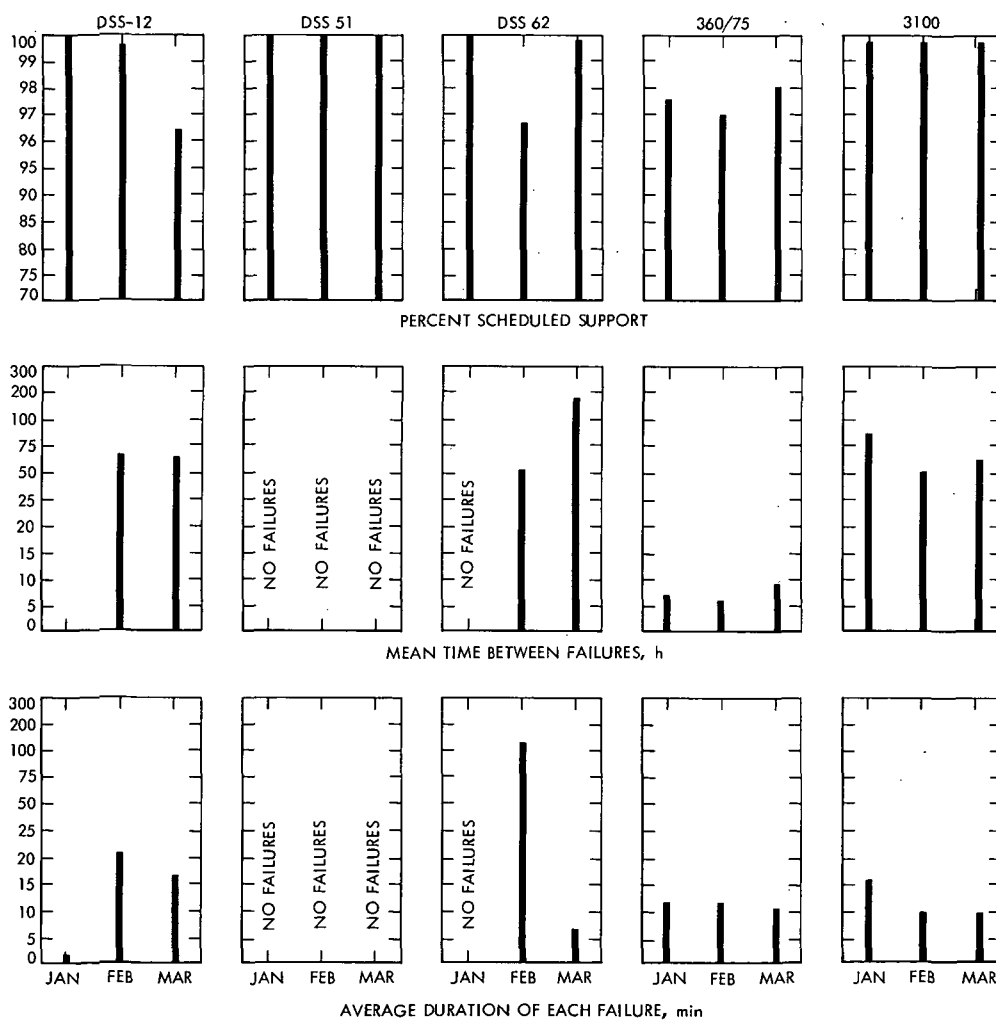


Fig. 1. DSN system performance summary

DSN Monitor and DSN Operations Control System Testing

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In preparation for Mariner Mars 1971 support, the DSN Monitor System and the DSN Operations Control System were extensively tested singly and thereafter furnished test support to combined system tests, rather than being under test themselves. This practice provided valuable test preparation and execution support.

I. Test Philosophy

A DSN single system test consists of data flow tests and parameter variation tests in all applicable data modes and data configurations; the test control, sequence, and acceptance criteria are designed to test the interfaces, continuity, and performance of only a single system. In a multiple system test, data flow tests and parameter variation tests are conducted simultaneously for all systems.

In preparation for MM71 support, DSN system tests were run in December 1971 and January and February 1972. The single system testing of the DSN Monitor System and the DSN Operations Control System was exactly as above; however, the testing of these two systems in multiple system tests differed from the above. After thorough single system testing of these two systems, they actually were used as test support for the DSN Tracking, Telemetry, and Command Systems in multiple system tests and in their single system tests. The extent to which Monitor and Operations Control

were tested in multiple system tests was only to assure that they suffered no degradation caused by interference from the other systems.

II. Scope of DSN Monitor Single System Tests

Previous articles (Refs. 1 and 2) describe the DSN Monitor System. All DSN system tests are an end-to-end test, including DSIF, GCF, and SFOF data processing. The monitor functions tested were as follows:

- (1) Acquisition and display of DSIF and GCF monitor data by the DSN Monitor processor in SFOF.
- (2) Consistency between actual conditions, the facility monitor displays, and the DSN monitor displays in SFOF.
- (3) SFOF monitor displays.
- (4) Consistency between tracking pseudo-residuals computed in the DSIF monitor processor and those computed in the SFOF tracking processor.

- (5) The monitor incoming high-speed data (HSD) line de-log (called the M-66 dump). This dump printed HSD blocks on a 1443 line printer in binary, octal, hex, or only the GCF header in readable form.
- (6) The DSN monitor processor generation and modification of data sets of DSIF configuration and tolerances intended for generating alarms in SFOF (however, the alarm generation itself was not within the scope of the test run for MM'71 support).

III. Scope of Operations Control System Tests

The testing of this system consisted of generation and transmission of files of data to the DSIF and others. An earlier article (Ref. 3) describes the output router, a part of the DSN operations control system. The operations control functions tested were as follows:

- (1) The output router which reads magnetic tape or 360/75 files and encodes the data into HSD blocks for transmission to the DSIF, or encodes into Baudot for transmission via TTY to any destination.
- (2) The generation of transmittable DSN sequence of events files using discrete event inputs and trigger event inputs which caused a stored subsequence associated with the trigger to be automatically inserted. These files were transmitted only by HSD line, because line width exceeded TTY capability.
- (3) The transmission of files of tracking predicts (generated within the SFOF tracking processor) to the DSIF. Two forms of HSD output are available (in addition to TTY): a character format for page prints and a floating point format for making a mag tape.
- (4) The DSIF production of a punched-paper antenna drive tape from the mag tape.
- (5) The transmission via HSD and TTY of DSN schedule tapes.
- (6) The DSIF reception and printing of the above transmission by the Digital Instrumentation Subsystem (DIS) simultaneously with its monitor processing.

IV. Single-System Test Method and Results

Generally, the tests of both monitor functions and operations control functions were straightforward. Monitor tests followed a procedure which specified config-

uration and status as a function of time, with voice coordination of display contents. Discrepancies were documented for corrective action and as "calibration coefficients" to be applied in subsequent tests. Operations control functions were tested with all data received by DSIF being mailed back to SFOF for analysis of transmission errors.

V. Multiple System Test Support and Results

Monitor displays were used extensively by personnel concerned with the testing of other DSN systems; information on known display errors was disseminated during pre-test briefings. (It is now apparent that monitor could not repeat single-system test procedures during multiple system tests, as the continual facility configuration changes would interfere with other systems' tests.)

The M-66 dump was used extensively by command to isolate SFOF/DSIF interface problems. Since only inbound data was read, it was necessary to patch outbound lines in the GCF comm terminal to spare inbound lines, to dump data flowing both directions.

All systems used the sequence-of-events generator to produce their test procedures, and again to merge the independent test procedures into a combined system test procedure. The advantage of fast procedure production or modification, coupled with the ability to transmit it to the DSIF is obvious.

The output router was used extensively for the transmission of procedures, predicts, and schedules during tests. Also, tests were run to assure noninterference between its output and SFOF command output.

The only instance of interference to these systems by other systems was that neither the sequence-of-events generator nor the output router could be exercised simultaneously, with tracking predicts generation or high-rate telemetry processing without causing the 360/75 to fail from overload.

VI. Conclusions

The philosophy of validating the DSN Monitor System and the DSN Operations Control System during single-system testing and then utilizing them as test support during all subsequent testing paid off by providing valuable test preparation and execution support.

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DSN Command System Tests

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The DSN Multiple-Mission Command System is continually being updated to support each successive flight project. DSN Command System tests are scheduled as each new model of Space Flight Operations Facility (SFOF) and Deep Space Instrumentation Facility Command System software is delivered. The DSN Command System test philosophy along with specific test results during the SFOF Mark III, Models 1 through 5 era, is described.

I. Introduction

The purpose of the DSN Command System tests is to verify that the DSN Command System meets the functional requirements specified in DSN System Requirements Document 820-8. The tests are supervised by DSN System Engineering and are performed after the appropriate facility has completed acceptance tests and delivered the system to the DSN. Following acceptance by the DSN based on the results of the DSN tests, the system is transferred to DSN Operations for flight project support.

DSN Command System Test Procedures or Test Sequence of Events (SOEs) are based on the DSN Standard Test Plan (DSN Document 851-1) and are updated to cover the capabilities of each new delivered system. The procedures are designed to test the Command System end-to-end, including all facilities necessary to operate the system, i.e., SFOF, GCF, DSIF, and Remote Information Center (RIC), if applicable.

DSN Command System tests are divided into two types: Single System and Combined System Tests. DSN Single

System Tests are data flow and parameter tests of the Command System operating alone, except for support systems, such as Monitor and Operations Control, and are designed to exercise all of the Command System capabilities and interfaces. Combined System Tests are data flow and parameter tests for the Command System operating simultaneously with all other DSN systems (Telemetry, Tracking, Monitor, and Operations Control) and are designed to evaluate system performance and interaction between systems in a realistic operating environment.

Table 1 shows specific DSN Command System tests and their objectives.

II. Test Activity and Results

The first DSN tests of the Command System portion of SFOF Mark IIIA software (Model I) were conducted during December 1970 and January and February 1971. This test phase was reasonably successful considering the lack of familiarity and training of the test operators and the limited capabilities of the system. For example, Monitor

System display formats were not available and Command System linear display formats were not usable, standards and limits and configuration tables could not be sent to the Deep Space Station (DSS) via high-speed data lines (HSDL) so canned tables had to be entered at the DSS, and test commands were not being accepted by the Telemetry and Command Processor (TCP) at the DSS.

One of the major system problems encountered during the tests was in the HSD message verification cycle. HSD messages from SFOF to the DSS failed to verify at SFOF although they were correct when received by the TCP. A modification to the TCP software was made by DSIF System Engineering which corrected the problem. This was verified by a special test using CTA 21 to simulate a DSS. Another major problem was with erroneous system alarms and aborts generated by the TCP. Several special tests were run with CTA 21 to verify results of TCP software modifications in an attempt to solve the problem, and although the system was significantly improved, the problem still existed at the time the system was transferred to DSN Operations.

The second phase of DSN Command System testing started in March 1971 when the SFOF Mark IIIA, Model II, and DSIF Phase II systems were delivered to the DSN. Standards and limits messages were successfully sent to the TCP via HSDL but did not function properly, and configuration messages still could not be sent. Problems also continued to exist with system alarms and aborts, and destructive overlaying of system linear display formats. Attempts to send commands from a Command Generation Program (COMGEN) file resulted in the 360/75 system going down. This problem was corrected in the SFOF Model IV system. Similar problems were encountered when attempting to command from a file constructed from a card deck.

In August 1971, SFOF Mark IIIA, Model IV, and DSIF Phase IV systems were delivered to the DSN. Single System Tests indicated that configuration and standards and limits messages were now functioning properly, COMGEN and card file commanding was now working,

destructive overlaying was still occurring on system linear displays, and many commands were erroneously being aborted for bit verify failure.

Combined System testing progressed very slowly at first, again due to a high percentage of 360/75 down time as a result of excessive backlogging of telemetry data; however, this problem decreased considerably in the latter portion of the test phase. System Data Record (SDR) validation and confirm/abort merge from an Original Data Record (ODR) playback was accomplished successfully for the first time. The system was transferred to DSN Operations and used to support *Mariner* Mars 1971 encounter.

The SFOF Mark IIIA, Model V System, which was designed to support *Pioneer F* launch together with *Mariner* Mars 1971 orbital operations, was delivered to the DSN in December 1971. Due to time constraints, no DSN Single System Tests were performed for the Command System; however, DSN System Engineering and Operations personnel participated in facility-level Command System Acceptance Tests. The DSN Combined System Tests were divided into two types: Level I tests were performed with a single DSS and used for engineering evaluation, and Level II tests were essentially Mission Operation Sequence tests performed with more than one DSS. All existing capabilities of the Command System together with unique *Pioneer F* command processing and multiple-mission capabilities (processing *Pioneer F* and *Mariner* Mars 1971 data together) were tested with no major problems. The linear display format problem was corrected, which greatly increased visibility into the system by the Command Analysis Group and Project Command. An attempt to operate the DSN Command System in the "hot backup mode" (prime and backup project command areas) under specific data priority and telemetry bit rate conditions resulted in bad data blocks being sent from the DSS. The problem was eventually solved by a hardware patch at the DSS. The system was delivered to DSN Operations in late February 1972, and was used successfully to support *Pioneer F* launch together with *Mariner* Mars 1971.

Table 1. DSN Command System tests and objectives

Test and objectives	Description	Prerequisites	Standards	Resources	Participants
DSN System Test Verifies system integrity, interfaces, data flow.	Commands (priorities and types) are generated by the SFOF command processor, routed via an HSDL to a DSS, modulated by RF and transmitted into dummy load. Verification, confirm abort messages and instructions are composed at the DSS, formatted and transmitted to the SFOF. The data are processed, routed and displayed by the 360/75 to the command analysis area, where the tests are conducted and results are analyzed.	1. Applicable facility systems have been tested and transferred to operations. 2. Test to be run concurrently with DSN Telemetry System Test.	820-8 Latest Edition, Section III	1 DSS: TCD, Receiver/Exciter, Transmitter GCF: 1 HSD, 1 TTY, 1 VOICE SFOF: 360/75, Command Analysis Area SOFTWARE: Multimission Command S/W (at DSS and SFOF); TCD/MMC diagnostics, command MDR/EDR S/W	Test Supervisor: DSN System Engineer Test Conductor: DSN Operations Chief Test Associate: Contemporary Project Engineer DSIF Facility Engineer SFOF Facility Engineer Command Analysis Supervisor Command Analysis Group and Supporting facility personnel
DSN System Multiple Mission Test Verifies multiple mission capability.	Following additions to test 1: Generation of standard and limits instruction by the Command Analysis Group relayed to and executed by the facilities. Periodic generation of command system status messages relayed to Operations control. Demonstration of generation within 24 h of command system data record.	Completion of DSN System Test (Command).	820-8 Latest Edition, Section IIB	Same as above.	Same as above.
DSN System Performance Test Measures system parameters (bit rates, subcarrier frequencies, power levels) and modes of operation.	Following addition to test 2: (a) Manual mode is exercised at the DSS. (b) With manual command input at the SFOF bit rates and power levels are varied and range of subcarrier frequency is checked. For these tests an abbreviated planetary mission profile is followed. Simultaneous sharing of processors with the other DSN systems on a non-interference basis is demonstrated. This includes real-time changes to the command system.	Completion of DSN Multiple-Mission Test (Command).	820-8 Latest Edition, Section IID	Same as above.	Same as above.

Pioneer Mission Support

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This report reviews the status of the second-generation Pioneer missions, Pioneers 6, 7, 8, and 9; and the prelaunch and launch support of Pioneer 10, which is the first member of the third generation, whose destinations are Jupiter and beyond. This mission was identified in previous reports as Pioneer F; it was renamed Pioneer 10 after its successful launch. The planning activities for the second mission of the third generation, Pioneer G, and a summary on the fourth-generation Pioneers planned for the exploration of Venus are also presented.

I. Pioneers 6, 7, 8, and 9

The second-generation *Pioneer* missions are still active. They are the first groups of interplanetary *Pioneers* managed and operated by Ames Research Center (ARC). The tracking and data acquisition support for these *Pioneers* has been furnished by the Deep Space Network since *Pioneer 6* launch in December, 1965.

The second-generation *Pioneers* are actively orbiting the Sun and continue to return data on fields and particles of the solar wind and plasma particles originating from the Sun and the galaxy. In addition, they map the magnetic field of outer space.

The accomplishments of *Pioneers 6* through *9* can be summarized as follows:

- (1) The precise determination of the characteristics of the solar atmosphere called the heliosphere.
- (2) Determination of solar cosmic ray and solar wind flow patterns and the magnetic and electric field mechanisms of the heliosphere.
- (3) The longest-lived operational interplanetary spacecraft were: *Pioneer 6*, launched in December 1965; *Pioneer 7* in August 1966; *Pioneer 8* in December 1967; and *Pioneer 9* in November 1968.
- (4) By the end of April 1972 they will have achieved 245 months of operational life during their solar orbits. The Deep Space Network has collected, during this time, almost 20 billion bits of scientific and engineering data, which were processed by Ames Research Center, and analyzed and reported to the scientific community by the principal scientific investigators. A total of 26,300 commands have been transmitted to these spacecraft.
- (5) These missions used for the first time the signatures of the telecommunications link for the determination of spacecraft spin axis orientation.

- (6) *Pioneers* were first in gathering space weather data for operational use.
- (7) *Pioneer 9* was the first spacecraft which used convolutional coding and sequential decoding resulting in a telemetry signal-to-noise improvement of almost 4 dB.
- (8) *Pioneer 6* and *9* signals had occultations by the solar corona and disk, making possible the measurement of the Faraday rotation as the spacecraft's signal traversed the solar corona. In addition, the spectrum-widening effects of the S-band coherent signal were established.
- (9) *Pioneer 7* was the first interplanetary spacecraft having a lunar occultation.
- (10) The *Pioneer 6* and *7* signals were received by the Goldstone DSCC 64-m-diam antenna station simultaneously as the two spacecraft were flying within the beam of the single ground antenna.
- (11) *Pioneers 6* and *7* were the first missions which established the radial and spiral characteristics of the solar wind and solar cosmic rays.
- (12) *Pioneers 6* and *7* were the first interplanetary spacecraft which defined the characteristics of the Earth's magnetic tail.
- (13) *Pioneers 6* and *9* were the first spacecraft having the capability of a telecommunications range adaptive telemetry system.

During the past year the DSN provided tracking and data acquisition support on a "time available basis" and within the Deep Space Station resource levels set for *Pioneers 10* and *G* and *Mariner 9*.

The actual number of support passes provided for the second-generation *Pioneers* during the past fifteen months is given in Figs. 1, 2, 3, and 4. The telemetry bit rates are also shown.

DSN is still using the *Pioneer* Ground Operations Equipment (GOE) at DSSs 12 and 14 in the Goldstone DSCC, and DSS 51 at Johannesburg, South Africa. This equipment is used to demodulate *Pioneer* telemetry and generate commands. Since DSN's policy is not to use mission-peculiar equipment and support all missions in the standard DSN Mark III system configuration, plans are under way to implement compatible software for *Pioneers 6* through *9* for the DSS Telemetry and Command Processing Systems software and the Space Flight Operations Facility compatible with the second-generation *Pioneers*

and use a configuration similar to the one used for *Pioneer 10*. After these software modifications, DSN plans to retire the *Pioneer* GOE.

II. *Pioneer 10*

During the functional design phase of the *Pioneer 10* and *G* missions in 1968 and 1969, DSN intensively supported all *Pioneer* Project sponsored activities to assure that the spacecraft design was fully compatible with the DSN Mark III system and that every effort was made to obtain a near-optimum type data return.

The results of numerous preliminary design and interface agreements were compiled and published in a document entitled *Tracking and Data System Estimated Capabilities for the Pioneer F and G Missions*. The first edition of this publication was distributed on July 15, 1968, and three revisions followed on March 15, 1969, June 15, 1969, Dec. 15, 1969.

Figures 5 and 6 display the methodology which was applied to coordinate the *Pioneer* planning and implementation activities in the Laboratory's budgetary system. Only validated Project requirements were included in DSN's implementation plans compatible with the framework of the NASA budget.

The formal DSN planning started with the formation of a DSN Capabilities Planning Team (CPT). This team had the following membership:

Chairman: DSN Manager, *Pioneer* Project

Members: DSN Project Engineer, DSN System Engineers in charge of the development of the functional capabilities of the Mark III system, *Pioneer* Project representative, recording secretary

The CPT held twelve scheduled meetings between December 1969 and May 1970.

The purpose of this activity was to establish an overall network capability as required by the *Pioneer* Project and constrained by DSN resources. The CPT has also validated the Project's Support Instrumentation Requirements, which were included in the *Pioneer F & G Support Instrumentation Requirements Document* (SIRD). Prior to *Pioneer 10* launch the Project published five versions of the SIRD in June, July, and September 1970, and February and September 1971.

The CPT activities resulted in a preliminary document entitled: *DSN Operations Plan for Pioneers F and G*,

Vol. III, *DSN System Description*. The summarized contents of this document were published in Refs. 1 and 2.

During the first quarter of CY70, a new central processing system was installed at the SFOF for use by MM71 and the *Pioneer F* and *G* Projects. This system consisted of two IBM 360/75 and two Univac 1108 computers. These machines have replaced the 7044 and 7094 configurations used in the past.

The DSN also started the planning of an interface between the Remote Information Center at Ames Research Center and the Space Flight Operations Facility (SFOF) at JPL. The objective was to give the *Pioneer* Project the capability to interface directly with the SFOF computers via a high-speed data line from Ames Research Center.

As a part of the Multiple Mission Telemetry System, DSN started the planning for the implementation of a sequential decoding capability at the Deep Space Stations. The Ground Communications Facility (GCF) also started the upgrading of the high-speed data line systems to 4800 bps.

In March 1970, the DSN also started the functional design and the implementation of a microwave link between the *Pioneer* spacecraft contractor, TRW, and the Compatibility Test Area (CTA 21) at JPL. This link installed later was used for the *Pioneer* Spacecraft/DSN RF and Data System Interface Compatibility Tests.

At the same time, a new multimission operations organization has been established by DSN. The intent was to organize network operations so that:

- (1) Network integrity will be maintained.
- (2) The Network can support many flights simultaneously.
- (3) A multimission support capability with a more integrated network operation than has been feasible in the past would be possible.

Around May 1970, DSN made the decision to use DSS 11 at Goldstone DSCC, DSS 42 in Tidbinbilla, Australia, and DSS 61 in Madrid, Spain, as the tracking stations for *Pioneers 10* and *G*. NASA planned at that time to make these stations compatible not only with the unmanned planetary and interplanetary missions, but also with the manned missions, such as *Apollo*. Therefore, it was necessary to make these stations compatible with the DSN Mark III-type configuration and also with the Space

Tracking and Data Network (STDN). The Telecommunications Division of JPL was tasked with the implementation of the described combined capability.

In December 1970, DSN started the *Pioneer 10* and *G* compatible design and development of the new real-time Central Processing System of the SFOF. This software system was developed in several phases. The first four models were designed for MM71, and Models 5 and 6 for *Pioneers 10* and *G*. Each model contained the capabilities of its predecessor with additional capabilities as required by the corresponding flight projects. The construction of a new building designed to support the *Pioneer* Mission Support Area was also in progress.

In the same time period, DSN also established a conical scanning (Conscan) project which performed tests to evaluate the capability of the deep space stations to support the spacecraft Conscan system.

A letter of agreement (ARC/PPO-9) between the *Pioneer* Project and the Tracking and Data System management was endorsed. This agreement described all interfacing procedures necessary during the planning, test and flight phases of the *Pioneers 10* and *G* missions.

DSS 12 at Goldstone DSCC, DSS 41 at Woomera, Australia, and DSS 62 at Madrid, Spain, were named as backup stations to DSSs 11, 42, and 61. Detailed implementation schedules for the backup stations were generated.

Based upon trajectory data received from the *Pioneer* Project, DSN has made an initial acquisition study which has shown that neither DSS 42 nor DSS 61 could be used as a backup for the initial acquisition station, DSS 51. As a result, the Project has requested that the STDN station at Ascension Island be equipped with *Pioneer 10* and *G* compatible capabilities and used as a full backup to DSS 51, Johannesburg, South Africa.

A study was made on the Jupiter encounter trajectories provided by the Project. The results indicated that DSN can handle the worst-case doppler variations. Special equipment and procedures will be required to acquire and maintain two-way lock with the spacecraft. It was also determined that the large doppler frequency shift will require new voltage-controlled oscillators (VCOs) in ground receivers during the cruise phases. It was also established that the Project encounter sequence planning of the flight/ground interface needs more detailed analysis in order to ensure the proper support.

The procurement of small computers identified as data decoder assemblies (DDA) was necessary to perform sequential decoding at the deep space stations. The implementation schedule was tight in order to meet the *Pioneer 10* launch readiness date.

An intensive software documentation exchange between the Project and DSN was necessary for the development of the software for the SFOF Central Processing System. There has been a continuing problem in attempting to understand and define the software interfaces inside the CPS.

During the first three months of CY71, the DSN Interface Engineering Team reviewed in detail all schedules necessary to establish a *Pioneer 10* launch readiness status. The schedule review has shown that the operational readiness date for the 26-m network had slipped from October to mid-December 1971, due primarily to late delivery of the TCP software and DDAs. This condition was caused by a manpower resource constraint. It was also established that the SFOF operational readiness date had slipped to November 1971, due to delays in definition of Project/DSN software interfaces and the delivery date of Project software for integration by September 1, 1971. It was seen at that time that the start of MOS testing would slip, and the total network testing would not start until January, 1972. It was also obvious that the DSN would have to combine the mission-independent and mission-dependent testing and training. It was established that the earliest date for complete transfer to DSN operations would be Jan. 1, 1972, with a more likely date of mid-January, which would mean that the testing and training originally planned for five months was contracted to less than six weeks.

During CY71, the building construction and equipment implementation for the mission support area was on schedule. A Conscan project quarterly report was issued in January 1971. This report indicated that DSN could satisfy Project-documented Conscan requirements with the existing hardware and software, and the DSN requirements for the support of the Conscan ground backup systems could be satisfied with TCP operational software and new station procedures. Special tests were performed at Goldstone DSCC to determine the effects of a rotating right circularly polarized antenna on the deep space station subsystems. In addition, plans were made to analyze amplitude modulation tracks during *Pioneer 9* superior conjunction to better understand the effects caused by the solar plasma. Data analysis of

DSS 14 tracks of *Pioneer 9* to evaluate amplitude modulation effects was completed and information forwarded to the Project.

The milestone schedule published during the third quarter of CY71 for the deep space stations showed that they would be ready for operations transfer to DSN by mid-December 1971.

During CY71 the definition of the DSN/Flight Project software interface within the Central Processing System had been defined as a major problem area. Attempts to define this interface in detail were delayed due to available man-power constraints and the high priority of the software testing necessary for MM71 encounter.

DDAs necessary for sequential decoding were installed at DSSs 11, 42, 51, and 61 in November 1971.

During the second quarter of CY71 the DSN installed the S-band RF link between CTA 21 and TRW, and an agreement was reached on the DSS/Spacecraft Compatibility Test Plan. It was expected to perform the first RF portion of the test during August 1971.

Further tests necessary for Conscan support have indicated that the expected degradation of doppler and telemetry data will be small and all data will have an acceptable quality. Plans were developed to simulate the Conscan signal for training of DSS personnel by using a function generator to control a modulator in the radio-frequency test signal path.

To establish the RF amplitude stability at DSSs 11, 42, 51, and 61, and to train the personnel in the use of software analysis programs and measurements techniques, a cognizant engineer visited these stations. All tests and data analysis verified that DSN satisfied the Project-documented Conscan requirements. Demonstration tests of the DSS/Conscan compatibility were included in the standard DSN/Spacecraft Compatibility Test Program.

The DSN and the *Pioneer* Project reviewed the software development plan of the Central Processing System and a decision was made to support the *Pioneer 10* launch essential requirements with the Model 5 real-time software. As a part of the software development activities, the following documents have been approved and published:

- (1) DSN/*Pioneer 10* Project Technical Software Interface Document.
- (2) Management Plan for *Pioneer F* Software Development.

- (3) DSN/*Pioneer F* Software Implementation Plan.
- (4) DSS to SFOF Interface Documents for Telemetry, Tracking, and Command Systems.
- (5) Detailed Milestone Schedules for monitoring the software development.

In mid-CY71, the construction of JPL Building 264, necessary for the *Pioneer* Mission Support Area, was completed and an agreement was reached with the Project on the layout. DSN also secured a 9300 terminal for the Project's Navigation Team.

The DSN's Ground Communication Facility completed their Operating Procedures and Communications Configuration Plan for *Pioneer 10*. All equipment, including high-speed data lines, were installed and tested. The DSN loaned to *Pioneer* Project a high-speed data encoder/decoder and block multiplexer set from the Compatibility Test Station, DSS 71, Cape Kennedy. This equipment was used by the *Pioneer* Project until their vendor delivered their final high-speed data equipment. The loan equipment was returned to DSS 71 in December 1971.

Network training started with orientation lectures given to DSS and SFOF personnel, and training of key station personnel was carried out during September and October 1971. The *Pioneer* Project Manager and the DSN Manager briefed and reviewed the planning of all DSN Stations.

Special documents describing in detail the DSN/Remote Information Center interface have been published and meetings were arranged to plan for and document the contents and generation of network data records.

An agreement between GSFC/STDN and DSN was made and documented on the support by the Ascension Island station (STDN). Decision was made that the *Pioneer 10* commands will be inputted manually by the station computer for transmission to the spacecraft and the station telemetry system was also made compatible with the *Pioneer 10* spacecraft design. To assure spacecraft/Ascension Island configuration compatibility a special test was made later at Cape Kennedy between the spacecraft operating at Hanger AO and the STDN/Merritt Island Launch Area (MILA) station.

During October 1971, the coding and intensive testing phase of the DSN/360/75 *Pioneer 10* mission-independent software development continued. To assure a *Pioneer 10* launch readiness capability, DSN has negotiated with the

Pioneer Project a Launch Essential Software Implementation Plan. In view of the interactive complexity of the DSN/360/75 software, its launch readiness status was only established during the latter part of December 1971. Since DSN had available only one Central Processing System with one spare computer, machine and facility time necessary for *Pioneer* software development was very limited during MM71 orbit operations starting in October 1971.

In November 1971, the *Pioneer 10* launch essential software development of the 360/75 and the TCP continued at a slow pace because of the high activity of MM71 work load and manpower resource constraints. The launch readiness status of the software was still uncertain at that time.

During the last two months of CY71 it was obvious that the short lead time available for the development of the large real-time software for the support necessary for MM71 and *Pioneer 10* taxed every member of the software development team. The coding of the *Pioneer 10* launch essential software was in the completion phase and an intensive facility test program started, which was constrained by limited test time. The combined DSN Network Integration and *Mariner/Pioneer* System Tests were scheduled during the second part of December 1971 with a completion date of latter part of January 1972. It was obvious that because of CPS computer test time constraints, DSN testing and training would be limited.

In the meantime, GCF and NASCOM completed all ground communications circuits and the *Pioneer* Mission Support Area was tested and declared operational. In addition, initial testing of the Remote Information Center's telemetry interface between the 360-75 and ARC was started. Review copies of a preliminary *Pioneer F* and G NASA Support Plan (NSP) were distributed for review and the original document was forwarded for endorsement.

In January 1972, the intensive testing and training of all TDS facilities were underway with the objective to be ready for a nominal *Pioneer* launch support capability by February 1. It was planned to start at this time the Project's Mission Operation System testing. The implementation schedule of the sequential decoding hardware and software at DSSs 42 and 61 had shown further delays with some positive hope of having this capability ready by the launch of *Pioneer 10*.

The Spacecraft/DSN RF and Data System Compatibility tests were performed between the prototype spacecraft at TRW/CTA-21/JPL during August and November 1971 and between the flight spacecraft at TRW and CTA 21 in December 1971. The compatibility verification tests using the flight spacecraft located at Cape Kennedy and DSS 71 were performed on 1/31, 2/1, 2/2 and 2/21 of 1972. A few software compatibility discrepancies were noted and corrected.

The DSN and Project test support summary is given in Fig. 7. The implementation of this busy schedule was only possible because the MM71 Project agreed to process their spacecraft data together with *Pioneer 10* data streams using the same real time software in one of the 360/75 computers. This configuration met the original objectives to operate *Pioneer* and *Mariner* in the same 360/75 in a multimission mode to free the second machine for further software development and testing and also backing up the maintenance of the prime machine.

During flight operations, the prime control of the DSN and the direct operational interface with mission control was exercised by the Operations Control Team. This team consisted of an Operations Control Chief and an Operations Chief from each DSN facility. Supporting at this time were operations groups representing each DSN system, the Deep Space Stations, communications facilities, and the SFOF Central Processing System. Figure 8 displays the DSN operations organization as it was configured during and after *Pioneer 10* launch support. Bringing the network up to a *Pioneer 10* launch support readiness status was the result of systematic planning and coordination work carried out by the members of the *Pioneer*/DSN Interface Engineering Team. This team held for almost two years regular biweekly Operational Support and Planning Group meetings. Each meeting had a pre-arranged agenda and followed up the status of the development of DSN System Engineering, Data Processing, DSIF, GCF and SFOF operations. The meetings were chaired by the DSN PE assigned to the *Pioneer* Project who assigned regular action items to the members of the team. The same team was also responsible for generating and publishing most of the DSN documentation necessary for the orderly preparation of the support of the first Jupiter mission. Twenty-six formal *Pioneer 10* and *G* documents were published, including five Tracking and Data System Progress Reports. These documents were distributed to all DSN personnel engaged in the *Pioneer 10* and *G* support activities and also to the interfacing members of the Flight Project Engineering Team. A detailed account on the described *Pioneer 10* and *G* support planning

activities and on the *Pioneer 10* launch will be given in a final report entitled *Tracking and Data Systems Support for the Pioneer 10 Mission, Volume I*. This report will also include a description of the planning and support activities of the Near-Earth Network.

III. Pioneer 10 Launch

Following a Mission Readiness Review that was held on Feb. 22 at Cape Kennedy, the launch vehicle was subjected to an RF interference test followed by the spacecraft RF signal strength measurement. DSN compatibility test station, DSS 71, supported this activity and validated the design thresholds of the S-band uplink and downlink. On February 26, four radio-isotope thermoelectric generators (RTGs) were installed on the spacecraft. These will provide the principal source of electrical power to all on-board systems and scientific instruments. During the same time, the flight battery was installed and the spacecraft was secured for the countdown.

On March 3, 1972, 01:49 GMT the first *Pioneer* spacecraft destined for Jupiter and beyond was launched from Cape Kennedy. The launch was successful after three previous attempts on Feb. 27 and 28, and March 1, which were canceled because of high winds in the upper atmosphere. All three stages of the launch vehicle performed nominally, and the injection was within a one-sigma dispersion.

The initial DSN down-range acquisition was accomplished by DSS 51 at Johannesburg, South Africa. This station established S-band telemetry downlink contact with the spacecraft twenty two minutes after launch. After the two-way S-band acquisition was completed as planned, the *Pioneer* operations team started to send commands to the spacecraft twenty-six minutes after launch. At the end of the view of DSS 51, the STDN Station at Ascension Island took over the support for one hour to close the gap between the views of Johannesburg DSS, and Goldstone DSCC. This gap was caused by the low declination angle (-33 deg) of the spacecraft trajectory. Nine hours after launch DSS 11 established two-way contact, and at the end of the California view, DSS 42 in Weemala, Australia, tracked *Pioneer 10* and tied the next tracking and data acquisition pass into Johannesburg.

This typical sequence followed during the second, third, and fourth days after launch with the addition that on the third day DSN also provided support from DSS 14, the 64-m antenna station at Goldstone DSCC, which was used to enhance velocity correction measurements. The Project fired the velocity correction thrusters of the spacecraft for

a short time, and DSSs 11 and 14 furnished the telemetry, tracking and command capabilities necessary to make these calibration measurements possible.

During the successful launch of *Pioneer 10* all prime backup facilities operated as planned, and DSN furnished real-time telemetry information almost continuously for the flight control team and for the principal investigators of the scientific experiments. The flight control team transmitted 175 commands during the first 72 hours of flight. DSN also provided two-way precision doppler data which were used by the navigation team to establish and update the spacecraft solar orbit and to prepare for the midcourse maneuvers.

On the sixth day of flight, the first midcourse maneuver was performed. The primary objective of the maneuver was to move the encounter target zone to three radii from the center of Jupiter, 14 deg below a parallel to the ecliptic through the planet center. The periapsis arrival time was placed within the views of the 64-m antennas at Goldstone DSCC, and Canberra, Australia. These conditions would satisfy the design objectives of the science experiments and would ensure against failure to receive data at either tracking station at the most critical hours of data acquisition. Based upon a priority list previously made with the experimenters and upon subsequent analysis, preference was made to attempt occultation by a Jupiter satellite, Io, or closely approach satellites for telemetry imaging. These goals were in addition to accommodating the primary objectives.

During re-orientation of the spacecraft-to-Earth alignment after ejection, signal dropouts were experienced in the interference region between forward and aft spacecraft antennas; therefore, as expected, the maneuvers were restricted to within 45 deg of Earth alignment. Also, equipment compartment temperatures were near the upper design limits, so it was decided to not turn the spacecraft backside toward the Sun during this maneuver. The maneuver strategy was selected 48 hours after launch and sustained by the excellent performance of the propulsion system and DSN's measurements during calibration maneuvers in the ensuing 15 hours.

The aim of the combined first and second midcourse maneuvers was to time the arrival for Dec. 4, 1973 at 02:26 GMT when Io would occult the spacecraft and some optical observations of satellites would be possible. The first midcourse maneuver was accomplished by precessing 45 deg from the Earth line into a plane containing the required velocity vector and the Earth line, accelerating

the spacecraft to a velocity increment of 18 m/s away from the Earth and returning to the Earth line with 9 m/s toward Earth.

On March 24, on the 21st flight day of *Pioneer 10*, the second midcourse maneuver was executed. The midcourse maneuver was accomplished in two components lying very nearly in the spacecraft Earth/Sun plane. The first was directly away from the Earth 1.8 m/s and the second was 2.14 m/s, 24 deg off the Earth line away from the Sun and generally toward the Earth. The Earth line component was trimmed to within an estimated 0.3 mm/s upon completion of the maneuver. The spin axis was then turned 10 deg away from the Earth line toward the Sun to minimize the equipment heating.

Figures 9, 10, and 11 display the relative Earth and spacecraft trajectories and positions, the initial and second midcourse maneuvers, and the DSN support.

IV. Pioneer G

After the launch and first 30 days support of *Pioneer 10* the DSN Interface Engineering Team and the implementing and operations organizations started the planning for the launch of *Pioneer G*. The launch window of this spacecraft opens April 5, 1973 and closes April 17, 1973. This mission will use a direct-ascent trajectory with an Atlas/Centaur TE 364-4 launch vehicle. The initial flight azimuth will be 108 deg with a yaw steering of 107 to 127 deg. This corridor will encompass declination angles from -33 deg all the way down to -42 deg.

V. Pioneer Venus

During the latter part of 1971, NASA Headquarters transferred the project management of the *Planetary Explorer* from Goddard Space Flight Center to the Ames Research Center and renamed the *Planetary Explorer*, "*Pioneer Venus*." This new group can be identified as the fourth-generation *Pioneers*.

The scientific communities are beginning to see Venus as at least equal in scientific importance to any other object in the solar system; therefore, they feel that the exploration and understanding of Venus should be a high priority item in NASA's planetary exploration program. Venus is Earth's closest neighbor in the solar system. Similar to Earth in size and proximity to the Sun, and possibly similar to Earth in origin, Venus' extremely dense

atmosphere, uniform cloud cover, high surface temperature and very low rotation rate make it one of the strangest in the planetary system.

Man's recent knowledge of the Venus environment is based upon the measurements performed by *Mariner 5* and *Venera 4*, *5*, and *6*. *Mariner 5* provided the information on the pressure and temperature near the surface of Venus and the distribution of electron density in the day and night side ionosphere and the termination of the daytime ionosphere by the solar wind. *Mariner 5* has also shown that Venus has a hydrogen corona and may have deuterium in its upper atmosphere. Magnetic field and particle measurements demonstrated that Venus has virtually no magnetic field. *Venera* spacecraft measurements confirmed this result.

The basic results of the *Planetary Explorer* studies were summarized in a GSFC Document, entitled *Phase A Report and Universal Bus Description*, dated May 1971. This study recommended two *Planetary Explorer* launches using multiple entry probes, followed with a Venus Orbiter mission, and the last mission would be again a multiple entry probe type.

The objectives of the entry probe missions were:

- (1) Nature and composition of the Venusian clouds.
- (2) Composition and structure of the atmosphere on the surface to high altitude.
- (3) General circulation pattern of the atmosphere.

The proposed orbiter mission objectives were:

- (1) Measurement of the detailed structure of the upper atmosphere and ionosphere by *in situ* techniques.

- (2) Investigation of the interaction of the solar wind with the Venus ionosphere in the magnetic field in the vicinity of the planet.
- (3) Determination on a planetary scale of the characteristics of the Venus atmosphere and surface by remote sensing experiments.
- (4) Determination from orbiter perturbations of gravitational field harmonics.

On January 10, 1972, GSFC arranged for an Ames/*Pioneer/Planetary Explorer* briefing. This briefing was attended by the Ames Pioneer Study Team of ARC, *Planetary Explorer* Study Team of GSFC, and the DSN Manager for the *Pioneer* Project.

In February 1972, the ARC Scientific Definition Team of Venus *Pioneers* prepared a request proposal on the Phase B Study of the Venus *Pioneers*. In March qualified aerospace companies were invited to submit their study proposals.

ARC plans to review completely the contents of the Phase A study and change or simplify the proposed design. It is assumed that the TDA requirements will also be affected.

The Phase B Study will require six to nine months to be completed. After the scientific details of the missions have been identified and the functional spacecraft design and the mission profiles have been iterated, ARC plans to ask NASA Headquarters to get a formal approval of the official start of the Venus/*Pioneer* missions. This approval will be endorsed by a Venus *Pioneer* Project Approval Document (PAD).

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2. Siegmeth, A. J., "Pioneer Mission Support," in *The Deep Space Network*, Technical Report 32-1526, Vol. VI, pp. 13-24. Jet Propulsion Laboratory, Pasadena, Calif., Dec. 15, 1971.

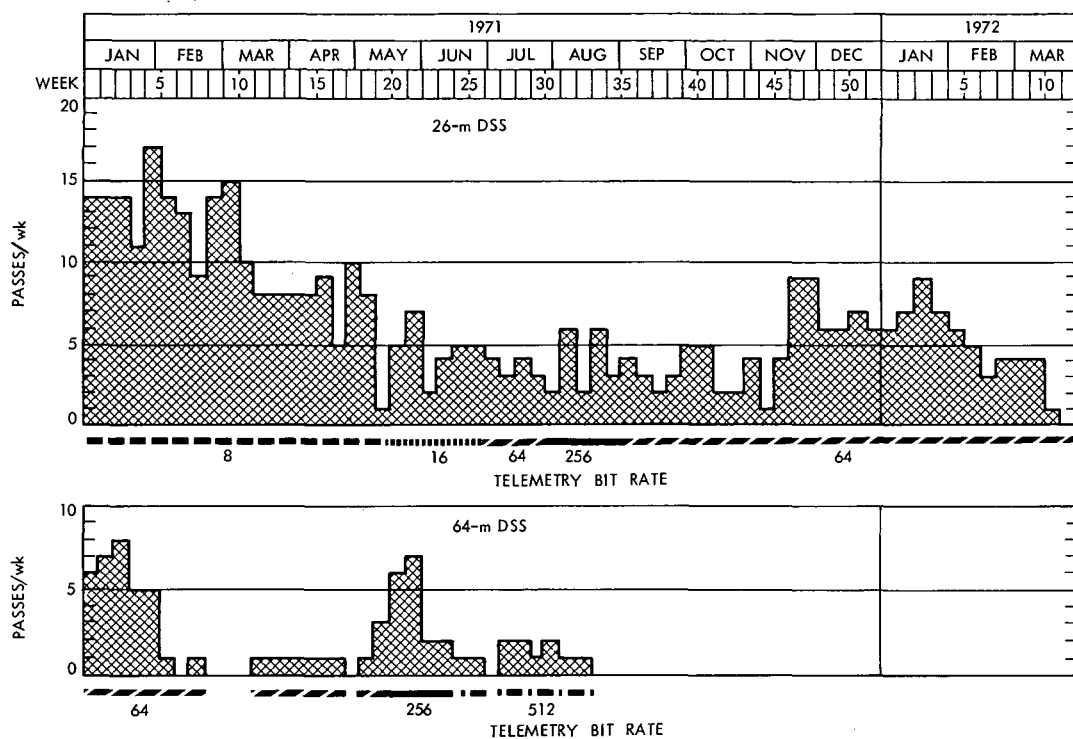


Fig. 1. Pioneer 6 actual DSS passes

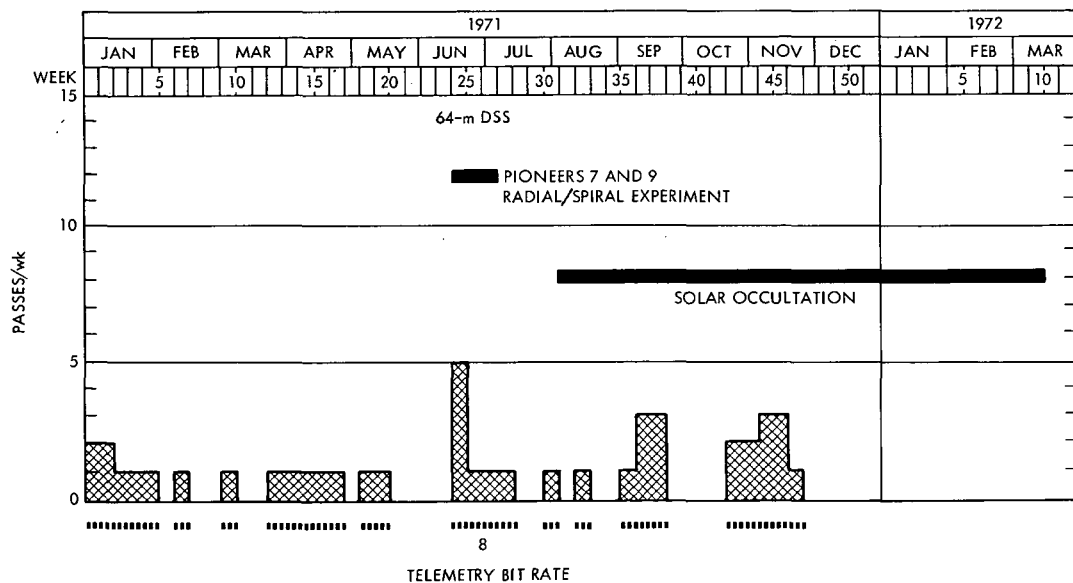


Fig. 2. Pioneer 7 actual DSS passes

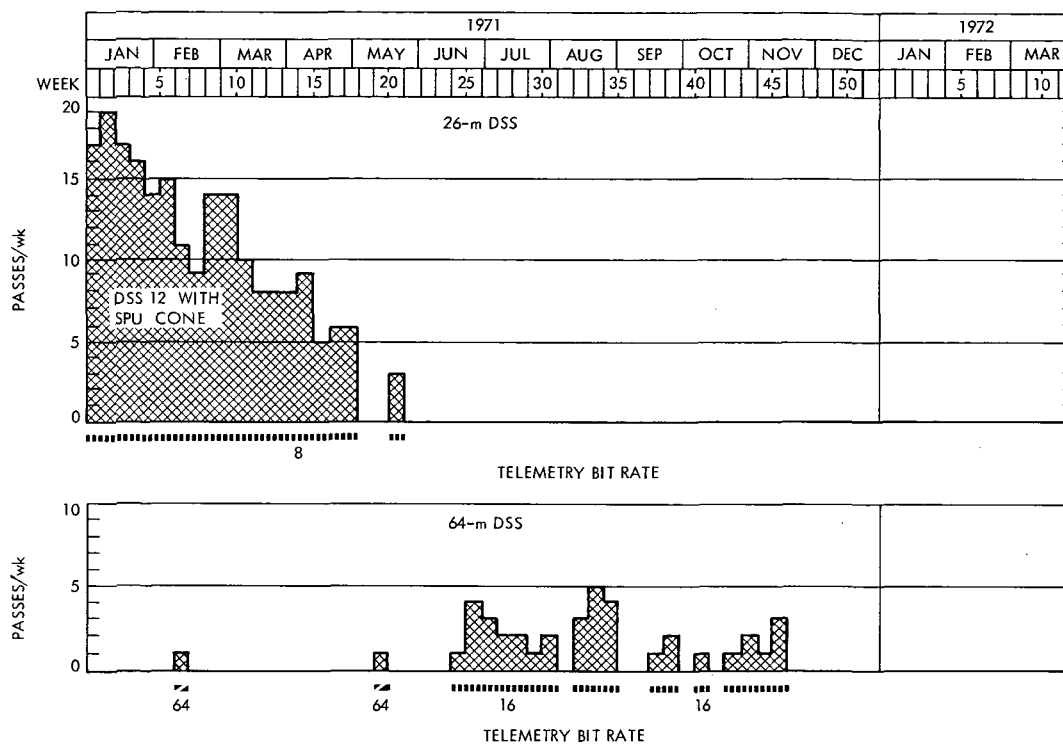


Fig. 3. Pioneer 8 actual DSS passes

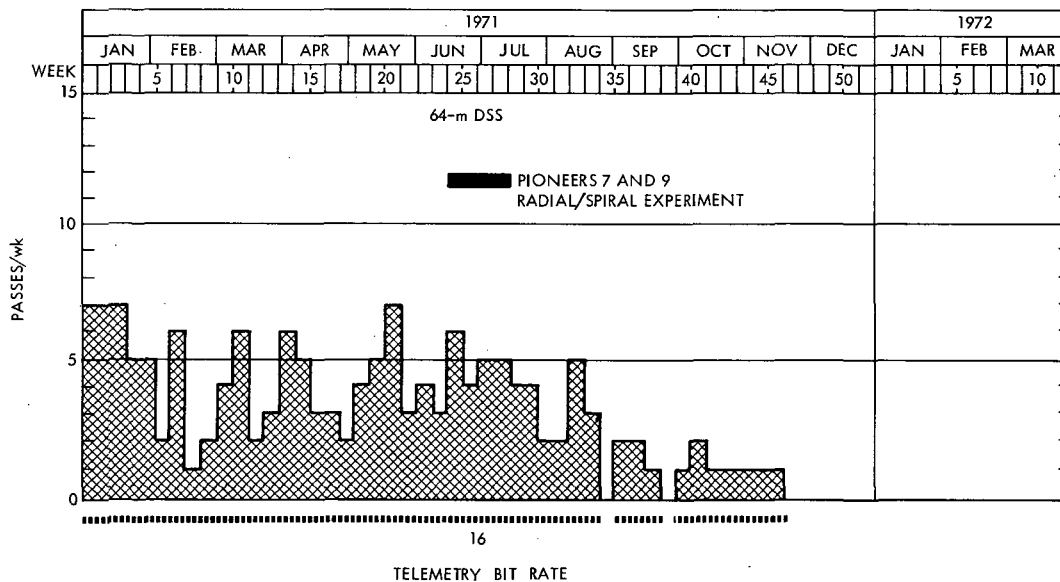


Fig. 4. Pioneer 9 actual DSS passes

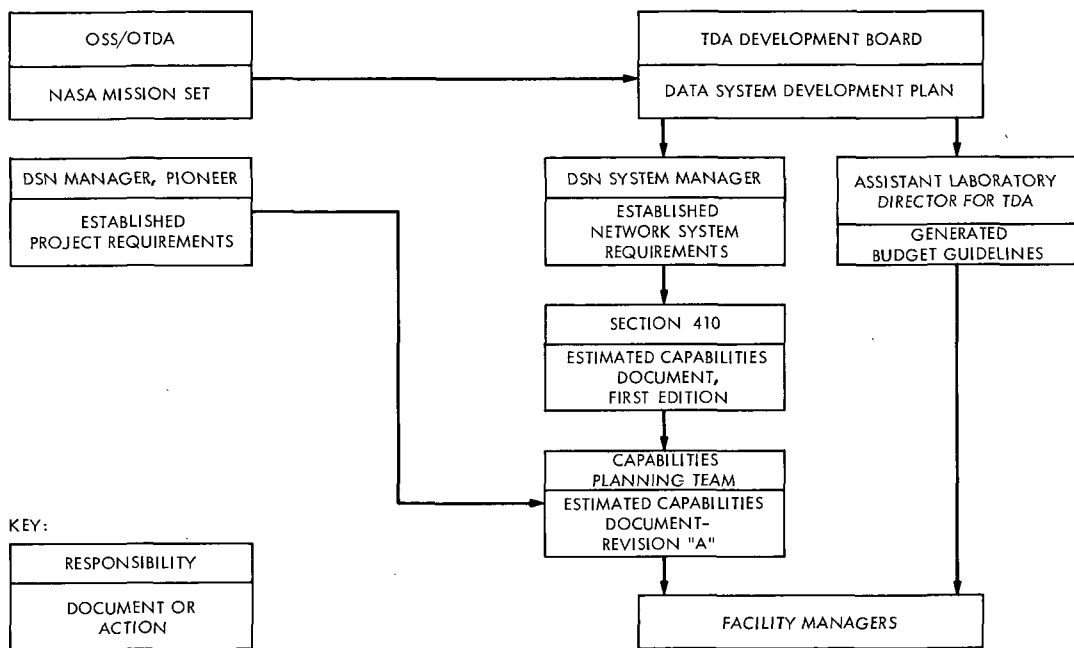


Fig. 5. Pioneer 10 and G DSN planning activities

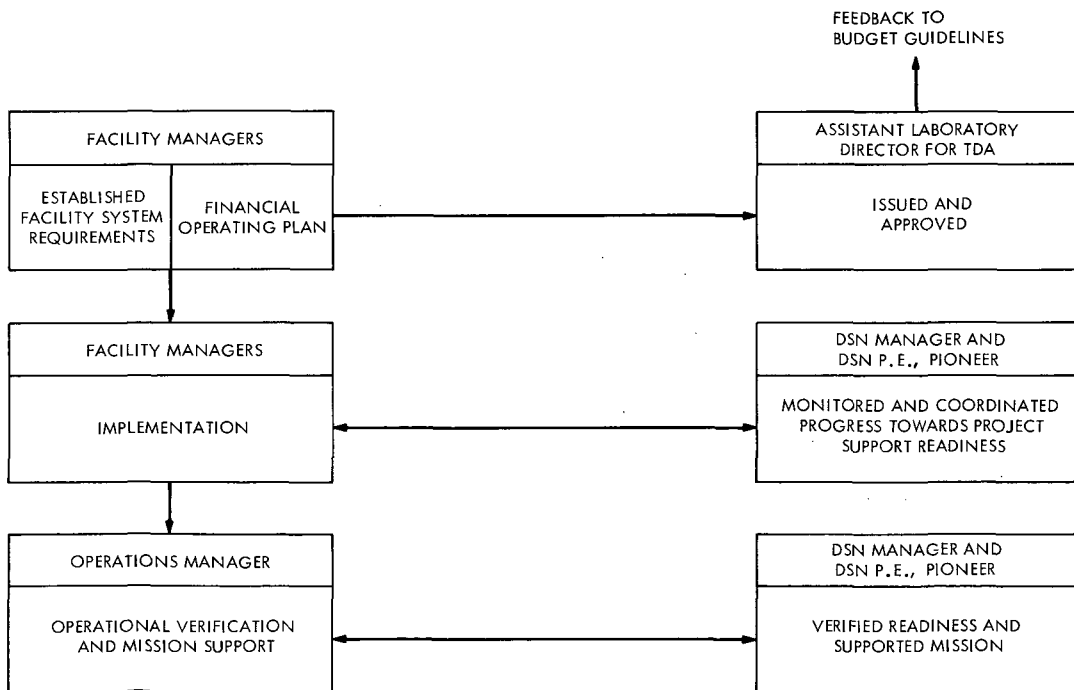


Fig. 6. Pioneer 10 and G DSN implementation activities

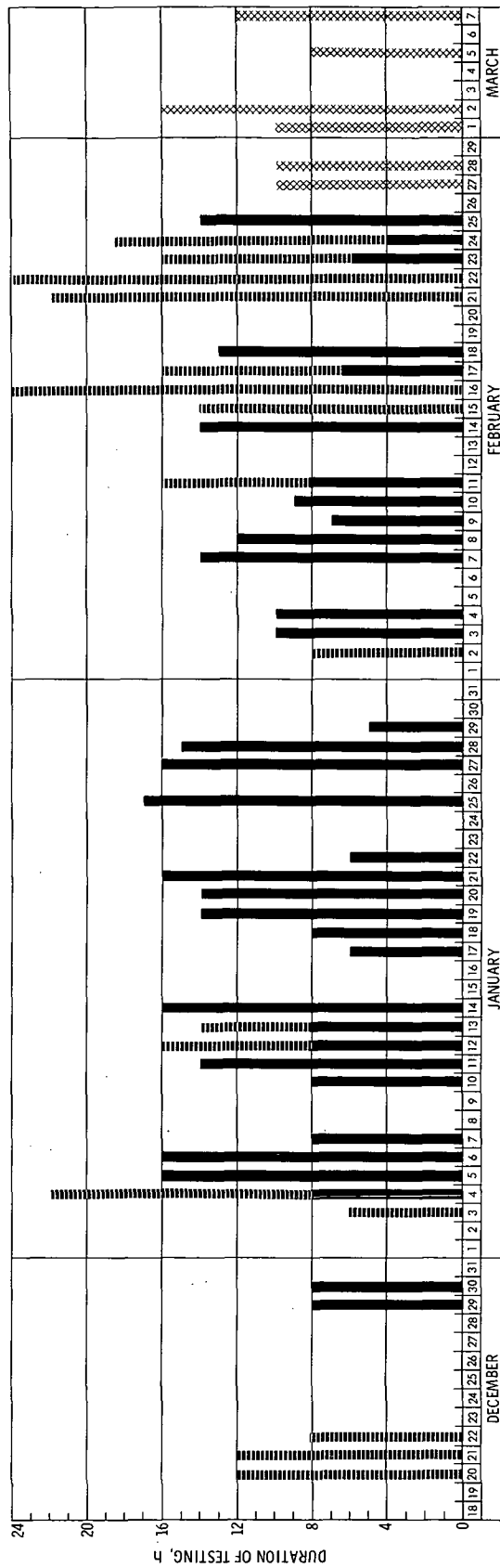


Fig. 7. Pioneer F DSN and project test support summary

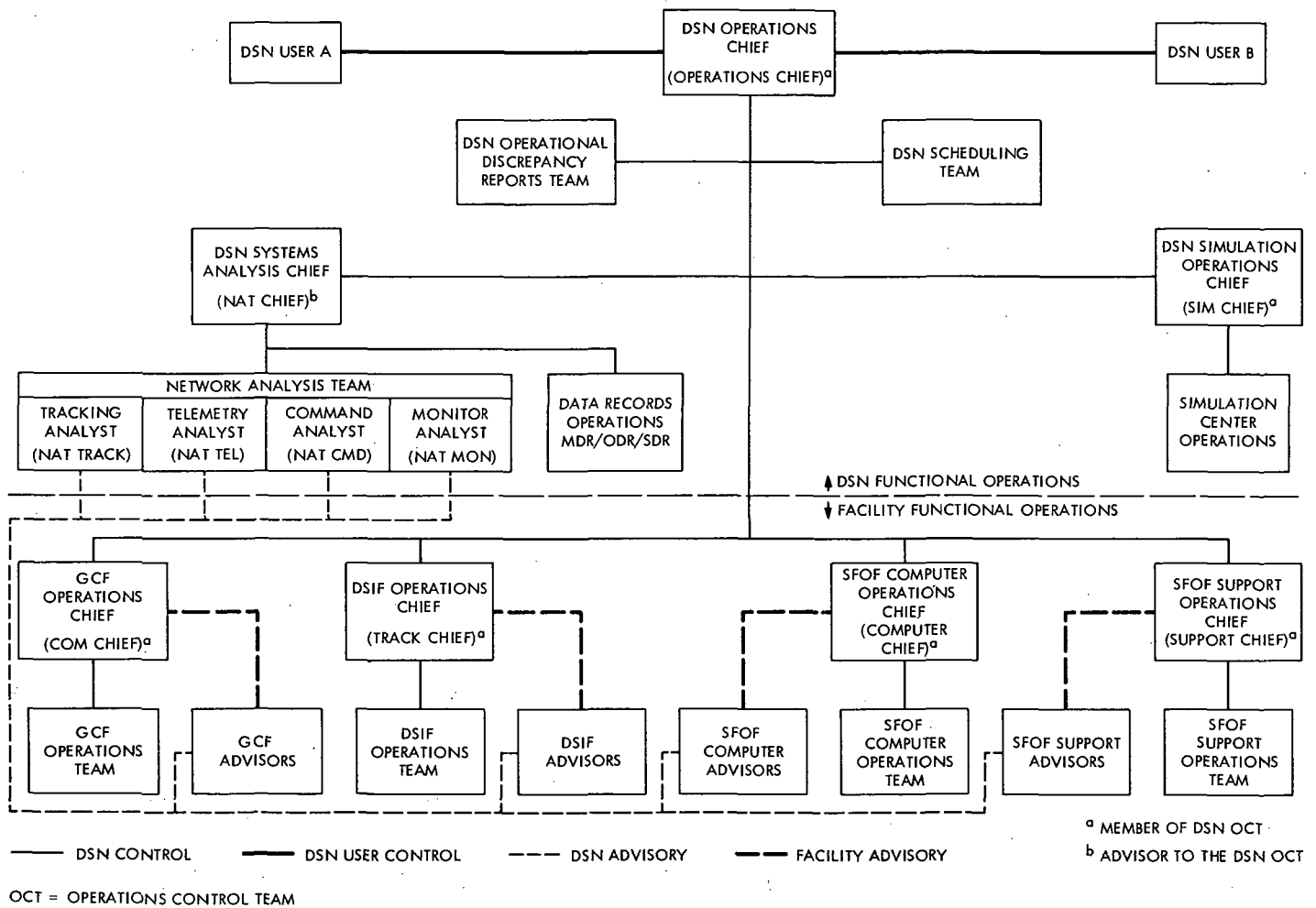


Fig. 8. DSN operations organization

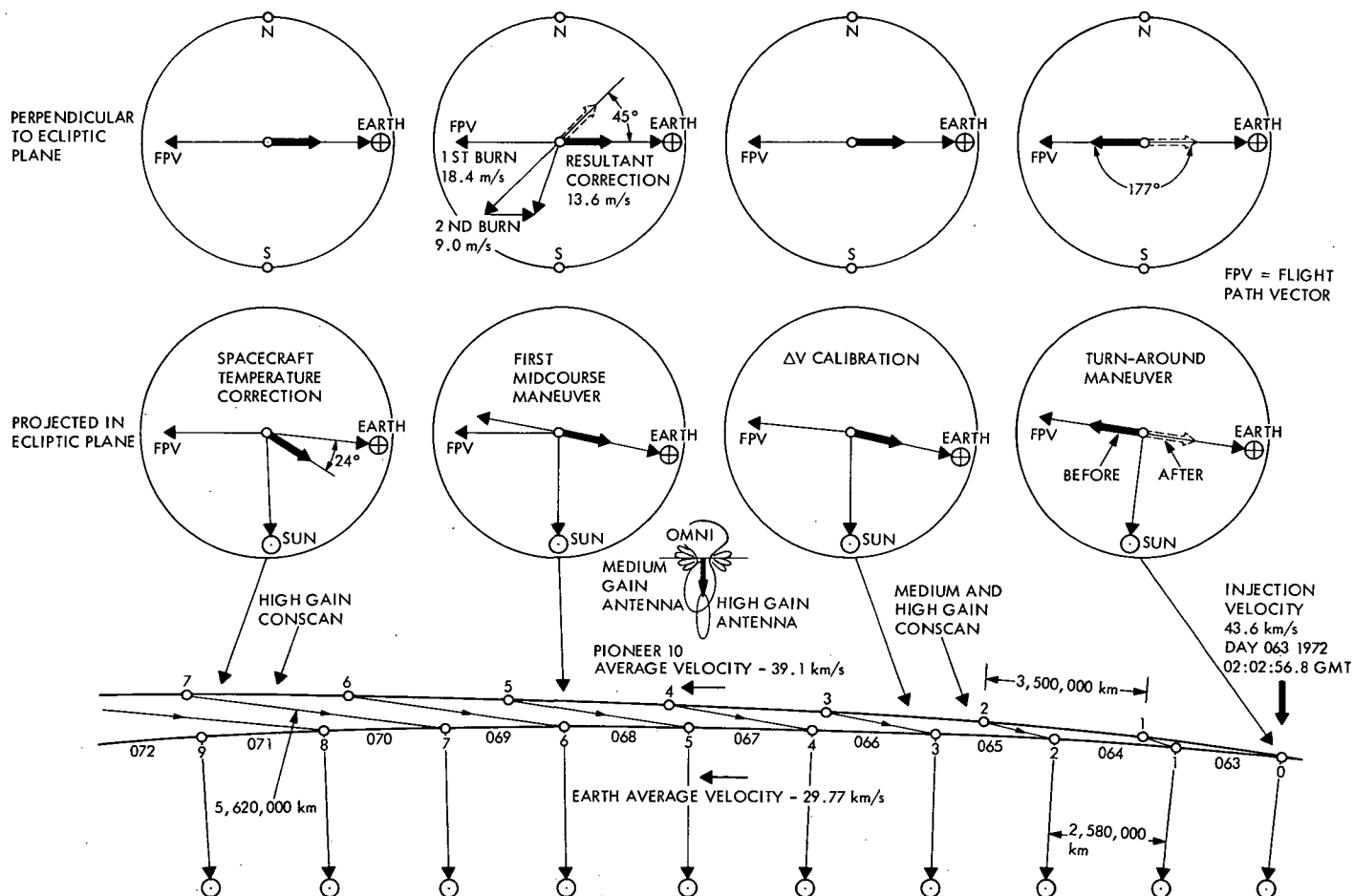


Fig. 9. Pioneer 10 initial maneuvers

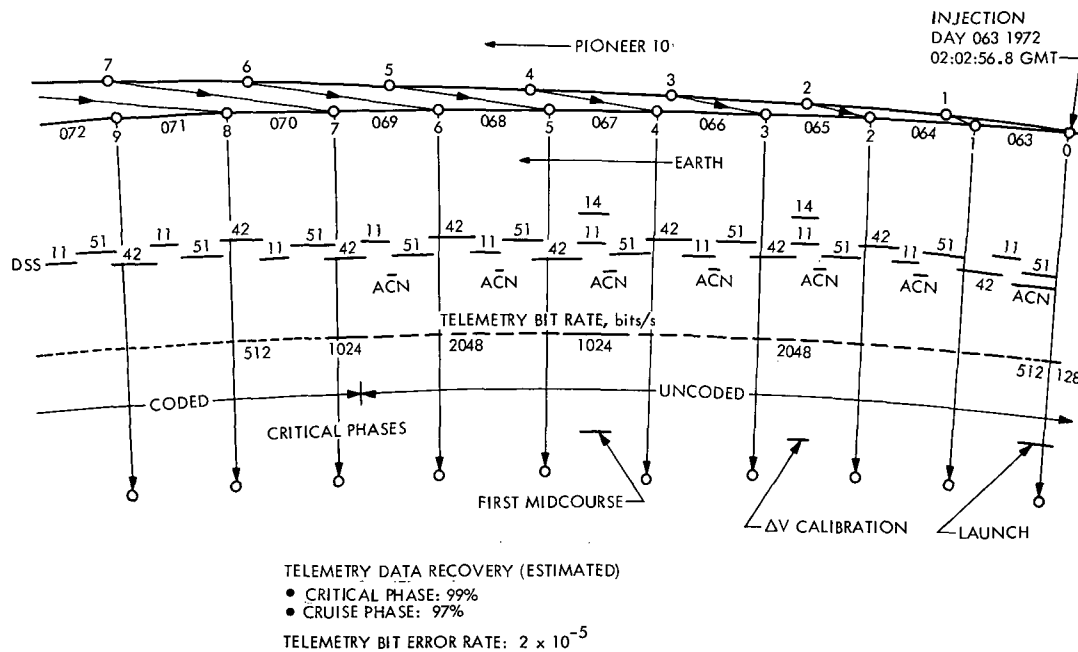


Fig. 10. DSN support

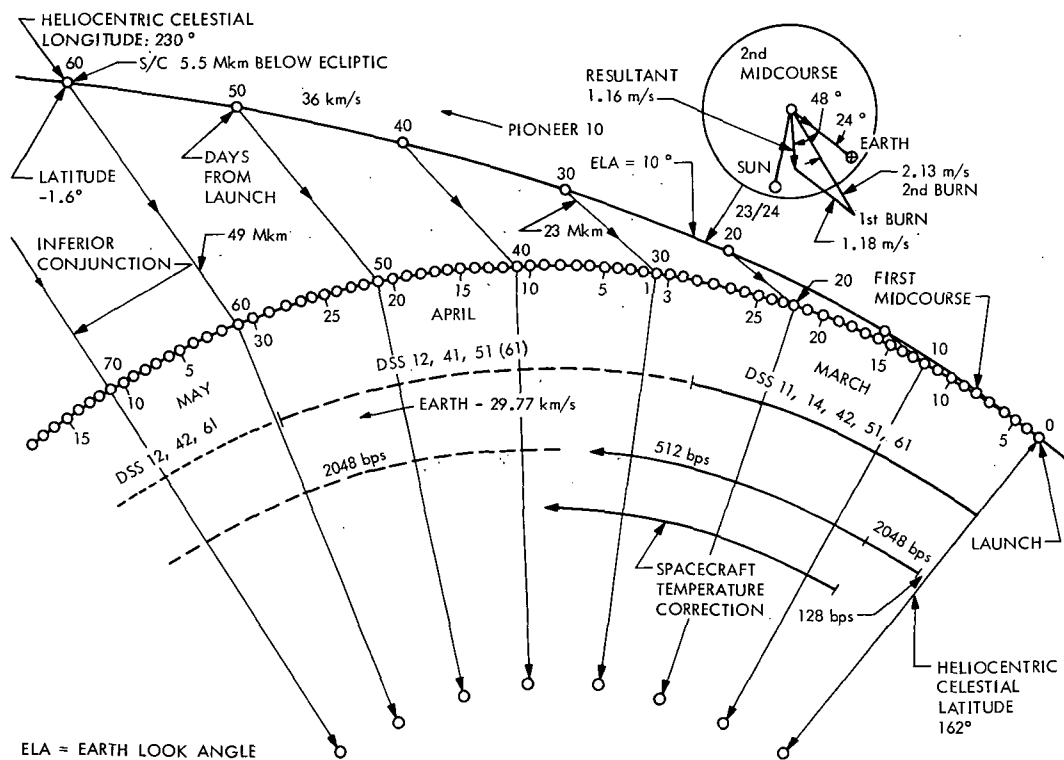


Fig. 11. Pioneer 10, first 60 days of flight

Helios Mission Support

P. S. Goodwin
Mission Support Office

Project Helios is a joint space endeavor between the United States and West Germany, whose objective is to place two unmanned spacecraft into heliocentric orbits whose perihelion distance will come closer to the Sun than any previously or presently planned free-world deep space undertaking. The West German government is designing and fabricating the spacecraft and will conduct Mission Operations. NASA will provide the launch vehicle, the launch facilities, and the major portion of the tracking with respect to this program. The launch of the first spacecraft is planned for mid-1974 and the second in late 1975. This article deals with the DSN support activities to Project Helios during the months of March and April 1972.

I. Introduction

DSN activity in support of Project *Helios* continued at a heavy pace during the past reporting period. Much of this effort, particularly that associated with the Compatibility Test Program, has already been published as part of the JPL 613-series interface documents and therefore will not be repeated in this article. However, it is of interest to highlight the following two significant topics.

II. Preparations for the Sixth *Helios* Joint Working Group Meeting

The Jet Propulsion Laboratory continued its preparations to support the Sixth *Helios* Joint Working Group Meeting to be held April 26 through May 3, 1972. These preparations cover both technical subject matter and Host Committee activities to accommodate an anticipated 150 attendees. In the technical area, the TDS organization has prepared a formal report of its activities during the past six months (i.e., since the Fifth *Helios* Joint Working Group Meeting); agenda material for its multiple meetings with other subgroups; and, of course, the actual presentation material that will be discussed during these sessions. In parallel with this activity, the Host Committee has been very active regarding all of the administrative

details associated with conducting a meeting of this magnitude. These latter activities range from such matters as transportation and hotel accommodations to providing conference rooms, secretarial services, and literature of general interest to the participants. It is hoped that each of these activity areas will result in a very successful Sixth *Helios* Joint Working Group Meeting.

III. *Helios* Engineering Model Transponder Compatibility Tests

As of this writing, the *Helios* Engineering Model Transponder/DSN Compatibility Tests have just been completed at DSS 71, Cape Kennedy. The results of these tests are just now undergoing evaluation; however, preliminary indications are that no catastrophic problems were discovered. Some minor difficulties were encountered in starting the tests due to damage received by the *Helios* transponder support equipment in its shipment from Germany to Cape Kennedy. However, this damage was either repaired at Cape Kennedy or "workaround" techniques were employed in order to proceed with the test schedule. During the tests themselves, certain problems were discovered—particularly around threshold level measurements—but these are of a correctable nature and are not

anticipated to interfere with the development of the prototype spacecraft. Such problems are normal in the development of any flight project spacecraft, which is the reason for early compatibility testing with the Engineering Model Radio System. Both the *Helios* Project Office and the DSN therefore feel that these Engineering Model Compatibility Tests that have just been completed represent an important milestone towards the successful launch of *Helios-A* in the summer of 1974.

IV. Conclusion

Aside from the continuing activity in response to action items generated in previous Joint Working Group Meetings, the above activities represent the major *Helios* effort during the past reporting period. Further details on the above subjects and other activities that will be conducted during the Sixth *Helios* Joint Working Group Meeting will be reported in the official minutes of the meeting which will be published during the next reporting period.

Mariner Mars 1971 Mission Support

G. P. Textor

DSN Engineering and Operations Office

On February 12, 1972, Mariner 9 completed its 180th revolution about the planet Mars and its 90th day of scientific data gathering from orbit. This marked the end of the nominal mission, which was to obtain data from orbit for a minimum of 90 days, and marked the beginning of the Extended Mission. This article presents the objectives, constraints, profile, and present DSN coverage plan for the Mariner Mars Extended Mission.

I. Extended Mission Objectives

The Extended Mission of *Mariner Mars 1971* differs from past *Mariner* missions in that the spacecraft remains at the planet. Data-taking capabilities equal to the nominal mission remain, plus the solar geometry affords a chance to obtain unique data. Table 1 indicates the Extended Mission objectives and the experiments that will achieve them. Key milestones during the Extended Mission are shown in Table 2.

II. Constraints

Ground and spacecraft operations must compensate for the constraints caused by increased Earth-Mars distance and unfavorable Sun-Earth-Mars geometry. The constraints primarily impact three spacecraft functional areas: telecommunications, attitude control, and power management.

A. Telecommunications

During the Extended Mission, *Mariner 9* distance relative to Earth increases from about 250×10^6 km at the beginning to 400×10^6 km at superior conjunction in Sep-

tember 1972. The corresponding decrease in communication performance severely constrains mission operations. Whereas a data rate of 16.2 kbps was used to return data during the nominal mission, only rates of 8.1 kbps and later 4.05 kbps are available for the Extended Mission. Even to achieve these rates requires the maneuvering of the spacecraft to point the high-gain antenna (HGA) at Earth. The reduced data rates will significantly increase the time required to play back data from the spacecraft recorder.

B. Attitude Control

Spacecraft maneuvers to point the HGA at Earth along with the control necessary during the additional scan platform slewing will require moderate budgeting of the attitude control gas expenditure. Excessive control gas usage may restrict data-taking toward the end of the Extended Mission period.

C. Power

The spacecraft is subjected to periods of Sun occultation during April and May of 1972. During occultation the spacecraft must operate on battery power alone. In order to conserve battery power and minimize recharge time, the

spacecraft will be placed in a minimal power consumption state with reduced or no data acquisition during this period.

Power may also constrain the playback time if large maneuvers (about 40-deg cone angle) are required to point the HGA toward Earth. Battery-sharing will result, which will require allocating sufficient battery charging time to replenish battery power.

III. Profile

The Extended Mission began with no change in operating mode from the nominal mission. The prime objective of the first few weeks was to continue the mapping of the Martian surface. As telecommunications performance degraded, selected features of Mars were re-examined.

Presently the spacecraft is encountering the Sun occultation period, which will continue until June. During this period the celestial mechanics experiment will have a unique opportunity to acquire the best possible data on the Martian gravity field. Also the S-band Earth occultation experiments will begin again as once more Earth occultations occur.

When the spacecraft is reconfigured for full operation following the solar occultation period, data-taking and playback operations will resume. Two data-taking days and two playbacks will occur each week during June and July 1972. Since only the 64-m-diameter antenna at Goldstone, California can acquire the spacecraft signal, ground-controlled operations must occur during the DSS 14 view-period.

During the last part of August through September and the first part of October, the celestial mechanics experiment will have another opportunity to gather valuable data as solar conjunction occurs. Data taking and playback will be reduced to once a week during this period and for the remainder of the Extended Mission.

IV. DSN Support

Project requirements for DSS 14 coverage and the planned DSN support are shown in Table 3.

While the DSN cannot meet the total requirements for coverage due to previous commitments of a higher priority, the level of support provided will allow *Mariner* Mars 1971 to fulfill the Extended Mission objectives.

Table 1. Extended Mission objectives

Objective	Experiment
Acquire unique data	Solar conjunction [S-band, Celestial Mechanics Experiment (CME)] High latitude coverage [TV, Infrared Interferometer Spectrometer (IRIS), Infrared Radiometer (IRR), Ultraviolet Spectrometer (UVS)]
Acquire long-time base data (> 90 days)	Meteorology (TV, IRIS, IRR, UVS) Celestial Mechanics
Acquire data supplemental to 90-day observations	Repeated spot coverage of areas of interest (TV, IRIS, IRR, UVS) Monitor Viking landing sites (TV, IRIS, IRR, UVS) Earth occultation (S-band) Cooling data (IRR)

Table 2. Mariner Mars 1971 Extended Mission

Event	Date, 1972
Start Extended Mission	Feb 12
Complete pre-solar occultation science-taking sequences	Mar 27
Start solar occultations	Apr 1
Start orbit edge-on celestial mechanics mass concentration (mascon) period	Apr 22
Start S-band occultations of polar regions	May 6
Complete orbit edge-on period	Jun 1
End solar occultations	Jun 4
Start weekly cycle of high-gain antenna maneuvers with one or two playbacks per week	Jun 5
End Earth occultations	Jun 24
Start solar conjunction period (relativity)	Aug 19
Solar conjunction	Sep 7
Complete solar conjunction period	Oct 18
Complete Extended Mission	Approx Mar 1, 1973

Table 3. DSS 14 coverage and planned DSN support

Date, 1972	DSS 14 passes required by Mariner Mars 1971	Present DSN coverage plan
Apr 1	7 passes/week	Average 5½ passes/week ^a
Jun 24	5 passes/week ^b	3 passes/week
Aug 19	7 passes/week	7 passes/week
Oct 18	7 passes/week ^b	3 passes/week
End of mission		

^aDuring the Apollo 16 mission, the average will not be met.

^bNew project requirement; DSN coverage plan reflects original requirement. The plan will be modified when final approval of the Extended Mission is received.

Navigation Demonstrations With the Mariner Venus-Mercury 1973 Spacecraft Requiring X-Band Receiving Capability at a Second DSN Station

B. D. Mulhall

Tracking and Orbit Determination Section

The opportunities to demonstrate two-station tracking with radio metric doppler and range data calibrated for charged particles by the X- and S-band technique during the Mariner Venus-Mercury 1973 mission are described together with the rationale for undertaking the experiments. The errors which corrupt two-station tracking for single and dual frequency operation are also described.

I. Introduction

The DSN plans to implement one X-band receiver at DSS 14 for the Mariner Venus-Mercury 1973 (MVM73) mission and eventually to have X-band receiver capability at the three 64-m antennas for the Viking 1975 (VK75) mission. If the installation of one of the second X-band receivers could be accelerated, so that it is operational at some point in the MVM73 mission, then two types of navigational accuracy demonstrations described in this article could be undertaken.

The advantages of the second X-band receiver would be:

- (1) An increase in navigational accuracy for MVM73.
- (2) Enhancement of the celestial mechanics experiment with the MVM73 spacecraft.
- (3) Enhancement of the relativity experiment during superior conjunction of the MVM73 spacecraft.
- (4) Demonstration of two-station tracking techniques with X- and S-band (X/S) calibration for use by VK75 and later missions.
- (5) Maintenance of JPL technical leadership in ground-based radio navigation.

The accomplishment of these advantages depends on the timing of the implementation of the second X-band station. It is very likely that the second X-band receiver could not be made available for the prime MVM73 mission. However, as shown in Fig. 1, there are other important events after the prime mission which could employ the second receiver.

Figure 1 depicts a function, which is value divided by risks versus MVM73 mission time. Value is defined as the number of opportunities to exploit the two X-band stations with the MVM73 spacecraft times the expected information gained from each opportunity. Risk is included, since the probability of spacecraft failure increases

with mission time. There is also factored in the risk the fact that the third Mercury encounter (§ ENC 3) is being only considered at present and is not an established objective.

The first opportunity in the MVM73 Extended Mission occurs in June of 1974 when the MVM73 spacecraft is occulted by the Sun. The relativity experiments planned for this period could be greatly enhanced by two-station tracking with the charged-particle errors removed by X/S calibration. The next important demonstration opportunity is the time of second Mercury encounter. As shown in Fig. 1, the spacecraft passes through zero declination in early September 1974, and encounters Mercury for the second time late in September. If two-station tracking with X/S can be shown to overcome zero declination and nongravitational force errors, then this technique can heavily influence VK75 and later missions. This will encourage future missions to request the support of the Deep Space Network 64-m subnet which will be eventually implemented with S-band receiving capability.

After the second Mercury encounter, there may be a third encounter. However, zero declination occurs about a month after the third encounter, making this encounter less attractive and, of course, more risky, in terms of spacecraft reliability, than the second.

Even after the third Mercury encounter there is still the value of gaining experience with two-station X/S tracking in preparation for *Viking*.

II. Navigation Demonstrations

The use of X/S with two-station tracking is intended to overcome two types of problems. Problems in the first group are referred to as navigational problems; those in the second are data noise problems. The navigational problems are:

- (1) The uncertainty in the solar pressure on the spacecraft.
- (2) The gas leaks from pressure tanks on the spacecraft.
- (3) The singularity in the determination of declination which occurs as the spacecraft passes through zero declination.

Reference 1 discusses the problem of various navigational errors, such as nongravitational forces on the MVM73 mission. Figure 2 is taken from Ref. 1 and

shows the effect of nongravitational accelerations at the 5×10^{-12} km/s² level for the Venus encounter. As shown in Fig. 3, the acceleration due to the uncertainty of the solar pressure on the spacecraft could vary from 5 to 20×10^{-12} km/s², depending on the actual distance of the spacecraft from the Sun. Figure 3 was calculated (by O. H. von Roos), using the *Mariner 9* spacecraft area and an uncertainty of 5% in the total solar pressure. The actual uncertainties for MVM73 have yet to be determined. However, Fig. 3 is representative of the level of uncertainty.

The acceleration on the spacecraft due to attitude-control gas leaks can be represented by Fig. 4. Figure 4 (supplied by J. W. Zielenbach) shows the magnitude and time of occurrence of random accelerations due to attitude control gas leaks on *Mariner 9* near the time of encounter. Figures 3 and 4 show that the uncertainty ellipse for nongravitational forces shown in Fig. 2 could be much larger.

There are two techniques for solving the navigational problems mentioned above. The nongravitational errors (solar pressure and gas leaks) can be reduced by taking two-way and three-way doppler simultaneously over a very long baseline. Reference 2 describes how this data type can help in this situation. The zero declination problem is corrected by taking range from stations simultaneously or nearly simultaneously over a long baseline where that baseline has a large north/south component.

In both cases, however, the success of the two-station tracking technique depends on the quality of the data. Figure 5 shows error bars for the components that corrupt two-way versus three-way range. The error bars show optimistic and pessimistic levels for each error. Figure 5 also shows the same errors when X-band reception capability has been added. In almost every case, there are improvements due to the additional information provided by the X-band measurement of range. Appendix A of Ref. 3 describes the details of the improvements due to X-band. The improvement in clock synchronization with X/S is based on the supposition that three-way range can be used to solve for clock offset if charged particle errors are eliminated. Three-way doppler will help to maintain synchronization by measuring clock drifts after clock offset is measured. This approach may not work, but if three-way range data is taken with X/S calibration we may find the technique which does measure clock offset and prove the scheme for use by future missions.

III. Charged Particles

The area of greatest improvement with the X-band receiving capability is the charged-particle calibration. Table 1 shows four different techniques for calibrating the charged-particles present in the Earth's ionosphere and the interplanetary space plasma. As indicated in Table 1, X/S removes the charged-particle effect in both media and provides calibration for both range and doppler. The other three techniques are deficient in one aspect or another. Faraday rotation measurements made from geostationary satellites do provide a way for calibrating range and doppler due to ionospheric effects. However, the space plasma is left uncalibrated. Using Faraday rotation in conjunction with two-way minus three-way differences is a complementary technique. Since the space plasma is almost exactly common to the two-way and three-way measurements, their difference eliminates the error. However, the ionosphere is very different, due to the different elevation angles and seasonal conditions over the two tracking stations and must be calibrated by local measurements.

To summarize the advantages of X/S calibration over the other three charged-particle calibration techniques, we take the X/S advantage over each of its competitive approaches. The advantage of X/S over DRVID is that X/S is potentially more accurate, and will provide a

range calibration, as well as a doppler. X/S has similar advantages over Faraday rotation in that it is more accurate. Besides this, the X-band receiver will be a fully operational part of the Deep Space Network equipment while the Faraday rotation polarimeter at Goldstone DSCC is only an experimental unit of low reliability, and the Faraday rotation data currently being received from Australia is provided by an outside agency. Finally, X/S has an advantage over two-way versus three-way measurement for removing the space plasma effects. The two-way versus three-way data could be used. However, there are other navigational errors in this data which might make it difficult to distinguish between charged-particle errors and equipment delay differences. Consequently, if the charged-particles are removed by X/S, then the two-way versus three-way can be used to solve for clock offsets and drift rates, free from the charged-particle influence.

IV. Conclusions

The nongravitational forces, charged-particle effects, and occurrences of zero declination shown in Figs. 1 through 6 are intended to show that the MVM73 mission is an excellent opportunity to demonstrate the power of two station tracking with X/S calibration which potentially could improve navigational accuracy for the MVM73 and future missions.

References

1. Jordan, J. F., et al., "The Effects of Major Errors on Planetary Spacecraft Navigation Accuracies," paper presented at the AAS/AIAA Conference, Santa Barbara, Calif., August 1970.
2. Ondrasik, V. J., and Rourke, K. H., "Applications of Quasi-VLBI Tracking Data Types to the Zero Declination and Process Noise Problems," paper presented at the AAS/AIAA, Astrodynamics Specialists Conference, Fort Lauderdale, Fla., Aug. 17-19, 1971.
3. Mulhall, B. D., "Navigation Demonstrations With the MVM73 Spacecraft Requiring X-Band Receiving Capability at a Second DSN Station," IOM 391.3-540, Mar. 10, 1972 (JPL internal document).

Table 1. Charged-particle calibration

Area	Calibration			
	X/S	DRVID	Faraday rotation	2-way — 3-way
Ionosphere	Range and doppler	Doppler	Range and doppler	Not calibrated
Space plasma	Range and doppler	Doppler	Not calibrated	Range and doppler

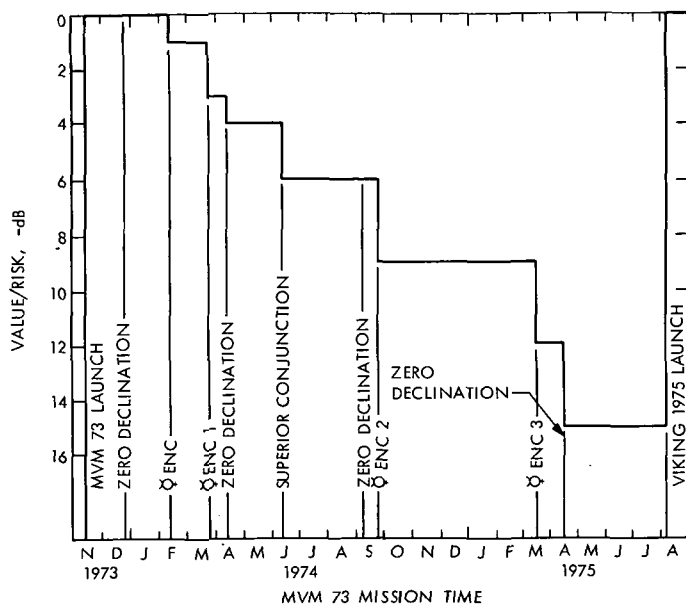


Fig. 1. Two-station tracking opportunities

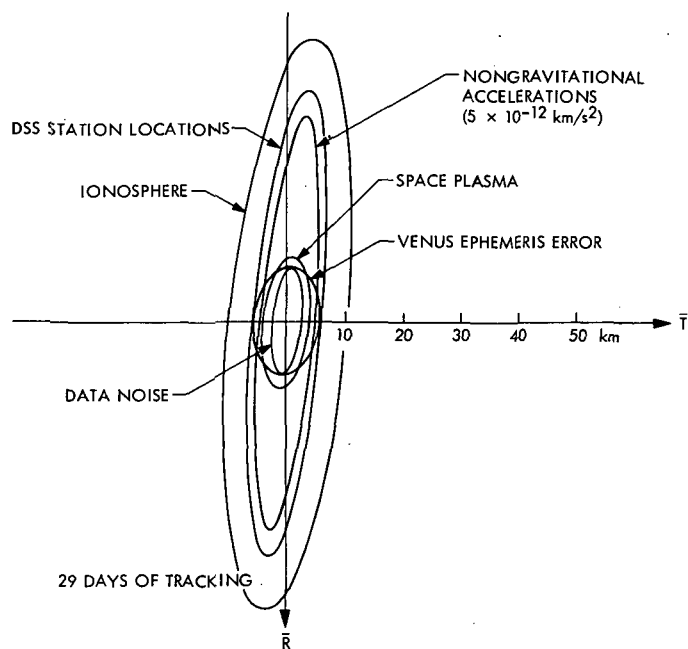


Fig. 2. Target-plane 1-sigma position dispersion

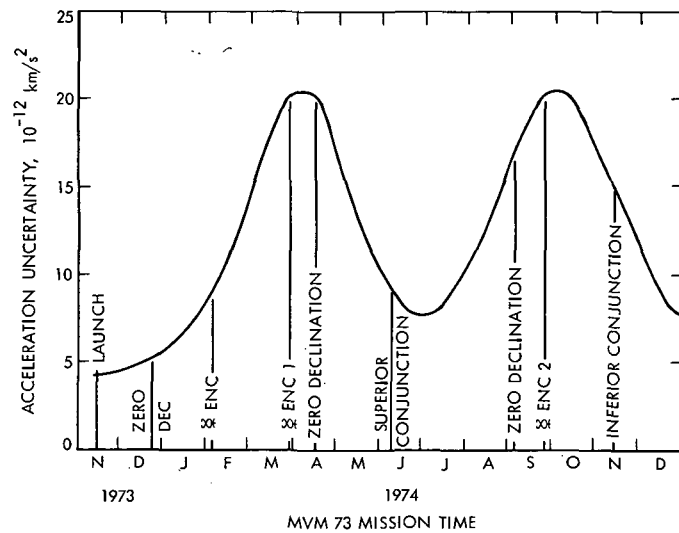


Fig. 3. Acceleration uncertainty due to solar pressure

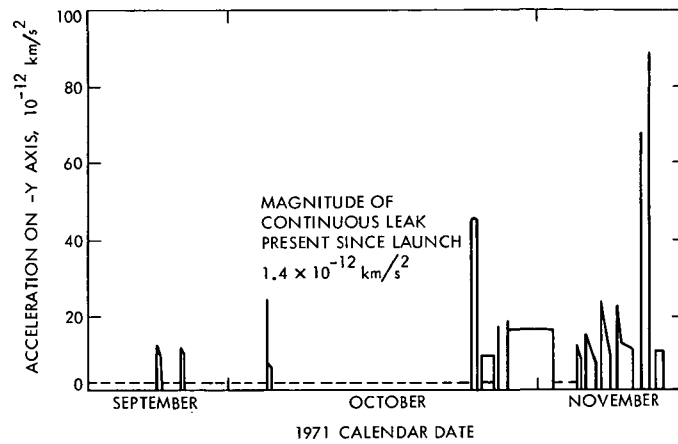


Fig. 4. MM'71 spacecraft accelerations due to attitude-control gas leaks

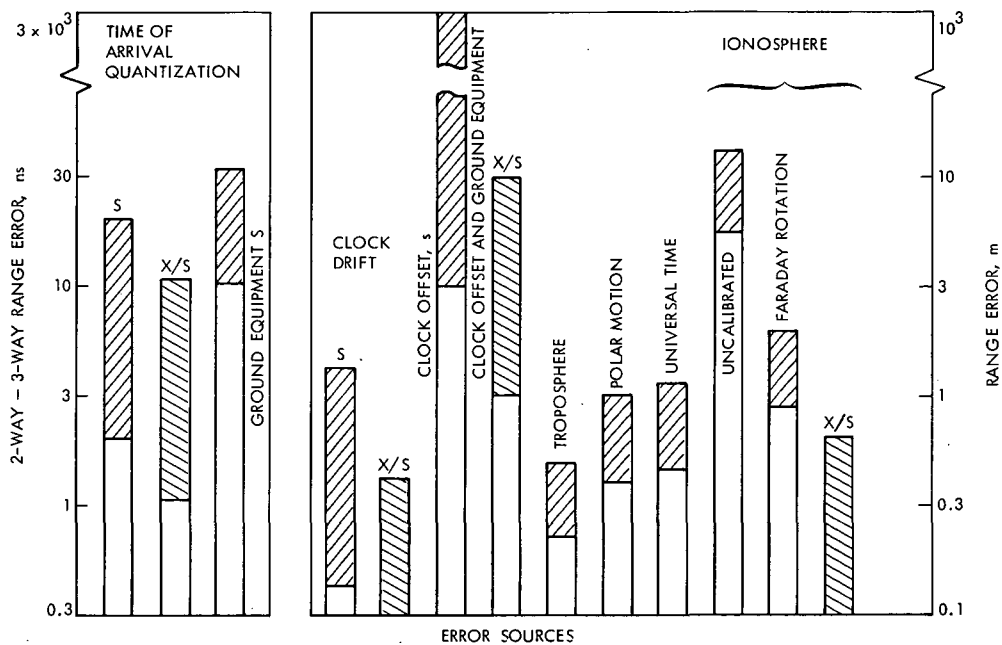


Fig. 5. Two-station tracking error sources

Computer Display and Entry Panel

S. S. Brokl

Communications Systems Research Section

The computer display and entry panel is a programmable high-speed numerical display and entry device for use with XDS 900 series computers. It contains additional sense switch and sense light capability along with a system interrupt. This type of device is expected to find application in troubleshooting DSIF minicomputers in the Network Repair Facility, in developing DSIF minicomputer software, and as a status display device for the DSN Network Operations Control Facility.

I. Introduction

The computer display and entry panel (DEP) is an auxiliary high-speed control panel for XDS 900 series computers. The numerical information may be program selected to represent octal or decimal numbers. The DEP increases the number of sense lights and sense switches available to the operator of the XDS 900 series computers and adds one system interrupt. When the DEP is installed in a XDS 900 series computer and its instructions are included within a program, an operator has an easily interpreted monitoring, entering, and testing device.

II. Problem

A method of displaying numerical information in real time and altering that information is desired. The numerical information may represent octal or decimal numbers, depending upon data requirements. The XDS 900 series computers have a limited number of sense switches and no sense lights; increasing the sensing capability will enhance computer interactions. Such capability is widely

needed in the DSN. It will help troubleshoot minicomputers in the Network Repair Facility, when minis become commonplace in the Network. The display capability will facilitate standard minicomputer software development and checkout as well. The DSN Network Operations Control Facility (NOCF) needs a permanent operational display system of low cost and minimum software burden. Finally, this capability is needed to conduct DSN development demonstrations and support flight project planning by conducting Planetary Radar experiments.

III. Hardware

The DEP (Fig. 1) is a simple program controlled device that allows an operator to see numeric information presented octally or decimally or to enter numeric information octally or decimally. The DEP also contains sense lights and sense switches which can be used in a variety of ways, such as to check the progress of large programs or to sense changes an operator may wish to make within a program.

The display portion of the panel consists of eight HP 5082-7000 solid-state numeric indicators and a HP 5082-7018 plus/minus sign. The display may represent eight octal digits or eight decimal digits plus sign. The mode octal/decimal is programmable and indicated by sense lights at the center of the panel. The sign is not used in the octal mode.

The entry portion of the panel consists of eight thumb-wheel switches and a sign toggle switch. The entry mode octal/decimal for the switches is program selectable and is indicated by sense lights at the center of the panel. The sign switch has no effect in the octal mode.

Sixteen sense lights and sixteen sense switches are provided at the bottom of the DEP. The lights can be individually turned on or off by the computer program and the states can be seen by both the operator and computer. The states of the sense switches can also be seen by the computer program so that test and skip commands can be used in programming. The sense switches are not buffered but are directly connected to a decoder. Care in programming to insure that the switch bounce does not interfere with the operation of the program should be observed.

Two other items on the panel allow added convenience to the operator. An interrupt push-button, which supplies a 3.2 μ s pulse, and can be plugged into any open system interrupt position on the system interrupt card. Also a switch labeled "ST" is supplied. With ST in the ON position, the computer start switch will reset the DEP display blanking all digits. With ST in the OFF position the computer start switch has no effect on the displayed information.

Figure 2 is a block diagram of the display and entry panel. A pair of standard interface boards has been designed for the PIN and POT slots of the XDS 930 computer. The PIN card acts as a receiver buffer for the PIN lines to the computer. The POT card acts as a buffer transmitter for the POT lines from the computer. Figures 3 and 4 illustrate details of the PIN and POT interface cards.

As can be seen on the block diagram, signals flow from the POT interface card to the DEP for decoding and control. Information to be displayed on the light emitting diode (LED) display is stored in a 32-bit hold register and

selected by quad 2-input multiplexers for presentation as octal or decimal numbers. Information to the computer from the thumb wheel switches is similarly processed and sent to the PIN interface card.

IV. Software

Table 1 is a list of EOM POT and EOM PIN instructions for displaying and entering octal or decimal numbers. The decimal numbers appear as two 24-bit words for eight numbers plus sign. The six low order numbers are packed BCD. The two high order numbers plus sign are packed BCD right justified with the sign appearing at the most significant bit position of the 24-bit word. In programming, for entering octal numbers, care should be taken in not placing the thumbwheel switches on decimal numbers, for these will be truncated and result in wrong answers.

Table 2 is a list of EOMs for setting and resetting the 16 sense lights and a list of SKS instructions for testing the set and reset states of the 16 sense lights and 16 sense switches. The position for the set state of the sense switches is up, the reset state is down. Meta symbol mnemonics are available upon request.

Programming of the interrupts is described in the XDS 930 computer reference manual. The interrupt can be plugged into any one of the presently available system interrupt positions so its priority and effects can vary as ordered by the operator.

V. Conclusion

One DEP is permanently installed in the XDS 930 at JPL. A second unit is to be installed on or before May 1, 1972 at DSS 13. A third unit is under construction and planned for installation at DSS 14 before the end of 1972.

The DEP at JPL was used to aid in the 1971 *Viking* Mars radar experiment range/doppler data reduction because of its capability to display rapidly changing numbers. It has also been used to simulate time display of a DSN station during program checkout. The DEP has been used as a debugging and troubleshooting aid in new hardware checkout, and in the development of new 930 software. Finally, the DEP is an integral part of the 1972 Venus radar two-station tracking experiment.

Table 1. EOM PIN and EOM POT instructions for thumbwheel switches and numeric display

Instruction	Code	Followed by instruction	Function
EOM	30021	POT	Load octal: loads contents of computer 'C' register into DEP select register and displays the number.
EOM	30121	POT	Load decimal (low order): loads contents of computer 'C' register into DEP select register and displays it as a 6-digit BCD number.
EOM	30221	POT	Load decimal (high order): loads the six LSB and "CO" into the DEP select registers and displays it as the two MSDF and sign.
EOM	30321	PIN	Load octal: loads the contents of the thumbwheel switches into the computer 'C' register as an octal number.
EOM	30421	PIN	Load decimal (low order): loads the contents of the six LSB thumbwheel switches as a BCD number into the computer 'C' register.
EOM	30521	PIN	Load decimal (high order): loads the content of the two MSD thumbwheel switches and sign switch into the computers 'C' register 'CO' and eight LSBs.

Table 2. EOM and SKS instructions for sense lights and sense switches

Instruction	Code	Function
EOM	3XX21	Where xx equals octal numbers 20 through 37; sets sense lights 1 through 16. Where xx equals octal numbers 40 through 57; resets sense lights 1 through 16.
SKS	3XX21	Where xx equals octal 00 through 17; skips if sense lights 1 through 16 set. Where xx equals octal 20 through 37; skips if sense lights 1 through 16 reset. Where xx equals octal 40 through 57; skips if sense switches 1 through 16 set. Where xx equals octal 60 through 77; skips if sense switches 1 through 16 reset.

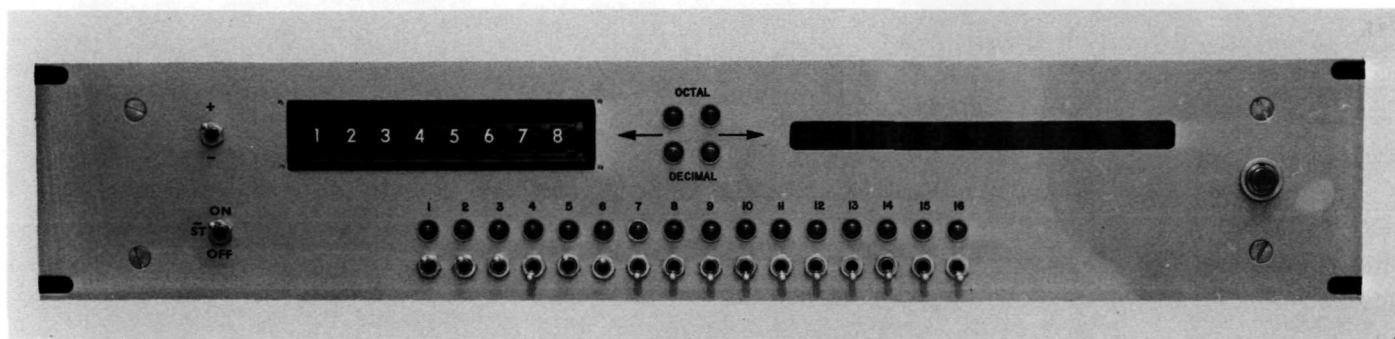


Fig. 1. Display and entry panel, front view

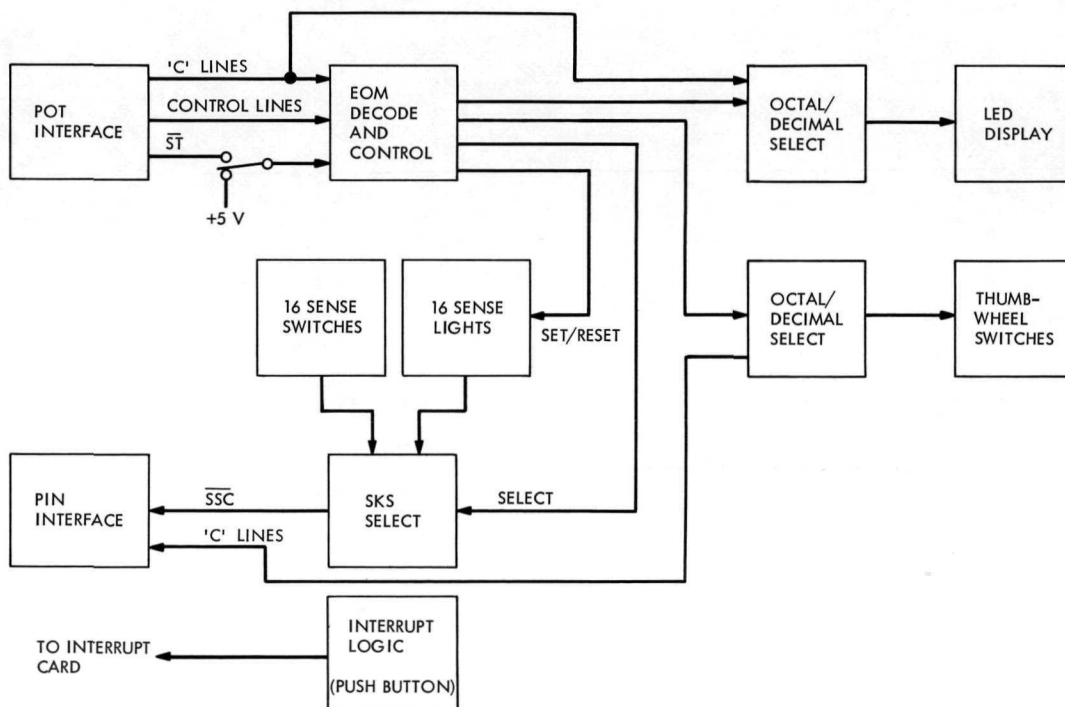


Fig. 2. Block diagram of display and entry panel

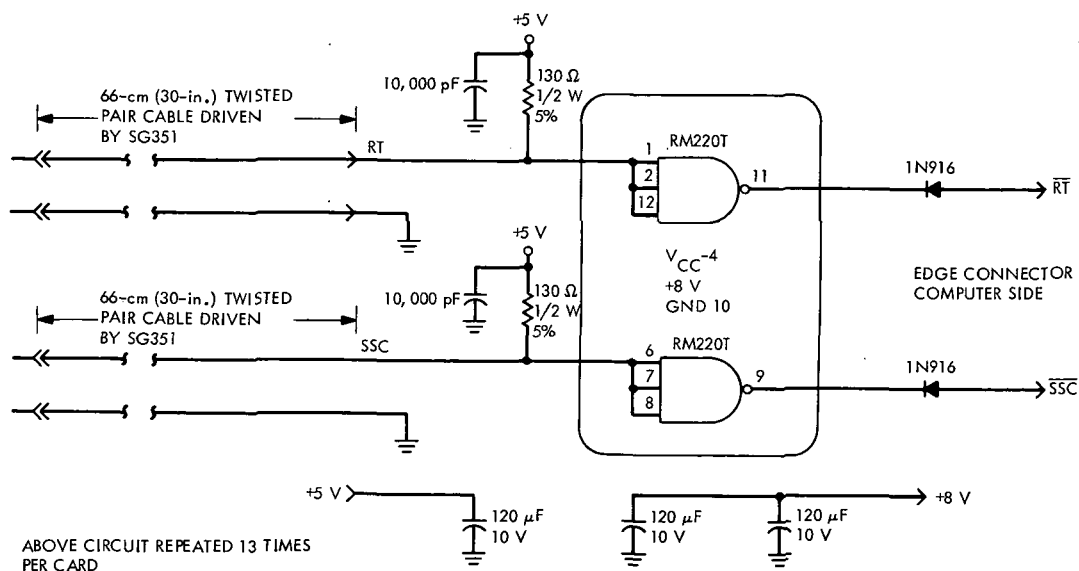


Fig. 3. Standard PIN interface for XDS 930 computer

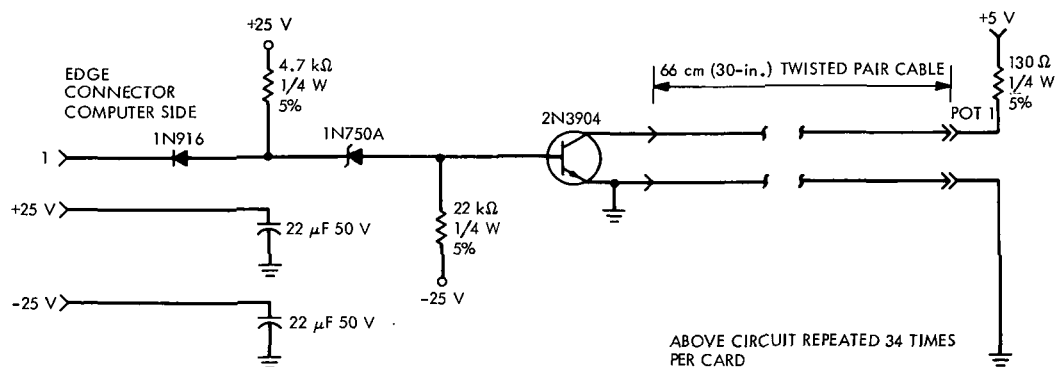


Fig. 4. Standard POT interface for XDS 930 computer

A Note on the Griesmer Bound

L. D. Baumert and R. J. McEliece
Communications Systems Research Section

Griesmer's lower bound for the word length n of a linear code of dimension k and minimum distance d is shown to be sharp for fixed k , when d is sufficiently large. For $k \leq 6$ and all d the minimum word length is determined.

I. Introduction

Denote by $n(k, d)$ the smallest integer n such that there exists an (n, k) binary linear code with minimum distance at least d . In 1960 Griesmer (Ref. 1) proved that

$$n(k, d) \geq \sum_{i=0}^{k-1} \lceil d/2^i \rceil \quad (\text{see footnote 1}) \quad (1.1)$$

and showed that for certain values of k and d the inequality (1.1) was in fact an equality. In 1965 Solomon and Stiffler (Ref. 2) simplified Griesmer's proof of (1.1) and at the same time generalized it to linear codes over an arbitrary finite field $GF(q)$, where it takes the form¹

$$n(k, d) \geq \sum_{i=0}^{k-1} \lceil d/q^i \rceil \quad (1.2)$$

¹Actually these bounds were obtained in the form

$$n(k, d) \geq \sum_{i=0}^{k-1} d_i$$

where $d_0 = d$ and

$$d_i = \lceil d_{i-1}/q \rceil$$

It is easy to see, however, that

$$d_i = \lceil d/q^i \rceil$$

More important, however, Solomon and Stiffler introduced the notion of "puncturing" a $(q^k - 1, k)$ maximal-length shift-register code and showed that for many more values of k and d equality holds in (1.2).

In this note we shall use the technique of puncturing to show that for fixed k , when d is sufficiently large the Griesmer bound (1.2) is sharp. That is, we will show that for each k there exists an integer $D(k)$ such that if $d \geq D(k)$, then

$$n(k, d) = \sum_{i=0}^{k-1} \lceil d/q^i \rceil$$

As a matter of fact we will only prove this for $q = 2$, the extension to general q being easy but notationally awkward.

We shall use the notation

$$g(k, d) = \sum_{i=0}^{k-1} \lceil d/2^i \rceil$$

in the rest of the paper.

II. The Theorem of Solomon-Stiffler

Let V_k denote a k -dimensional vector space over $GF(2)$. Let $S_1, S_2, \dots, S_t$ be subspaces of V_k of dimensions $k_1, k_2, \dots, k_t$ such that no element (except 0) of V_k is contained in more than h of the S_i 's. Then Solomon and Stiffler showed that there exists an (n, k) binary linear code with minimum distance d , where

$$n = h(2^k - 1) - \sum_{i=1}^t (2^{k_i} - 1)$$

and

$$d \geq h2^{k-1} - \sum_{i=1}^t 2^{k_i-1} = d' \quad (\text{see footnote 2})$$

Furthermore if the k_i are distinct, $n = g(k, d')$ and so the code is length-optimal; i.e., $n(k, d) = g(k, d)$. Finally they showed that a sufficient condition for the existence of such subspaces S_i is that

$$\sum k_i \leq kh$$

III. Main Result

THEOREM: For each k there exists an integer $D(k)$ such that $n(k, d) = g(k, d)$ if $d \geq D(k)$.

Proof: We show that

$$D(k) = \left\lceil \frac{k-1}{2} \right\rceil 2^{k-1}$$

will do. Write

$$d = d_0 + (h-1)2^{k-1}$$

where $1 \leq d_0 \leq 2^{k-1}$. Then if

$$d \geq \left\lceil \frac{k-1}{2} \right\rceil 2^{k-1}$$

it follows that

$$h \geq \left\lceil \frac{k-1}{2} \right\rceil$$

Next we write $2^{k-1} - d_0$ in its binary expansion

$$2^{k-1} - d_0 = \sum_{i=1}^t 2^{k_i-1} \quad 0 < k_1 < k_2 < \dots < k_t < k$$

²It can be shown that $d = d'$ unless the dual subspaces $S_i^\perp$ completely cover V_k .

Then

$$\sum_{i=1}^t k_i \leq 1 + 2 + \dots + k-1 = k(k-1)/2 \leq k \cdot h$$

and so by the results of Solomon-Stiffler quoted in Section II, $n(k, d) = g(k, d)$.

IV. Numerical Results:

We have been able to calculate the exact values of $n(k, d)$ for $k \leq 6$ and all d . It turns out that the value

$$D(k) = \left\lceil \frac{k-1}{2} \right\rceil 2^{k-1}$$

given in our theorem is extremely conservative; for example for $k=6$ our theorem only guarantees that if $d \geq 96$, $n(6, d) = g(6, d)$, while $d \geq 20$ would do. Much of this disparity arises from our use of the very weak sufficient condition

$$\sum k_i \leq kh$$

for the existence of subspaces $S_1, S_2, \dots, S_t$.

Thus consider the example $k=6$, $d=35$. Examining the proof in Section 3, we write $35 = 3 + 1 \cdot 32$ ($h=2$), and $32 - 3 = 29 = 2^4 + 2^3 + 2^2 + 2^0$. Thus we need to find subspaces of V_6 dimensions 5, 4, 3, and 1 which cover each nonzero vector of V_6 at most twice. Since $5 + 4 + 3 + 1 = 13 > 6 \cdot 2$, the condition of Solomon-Stiffler does not apply. However, if the vectors of V_6 are coordinatized $x = (x_1, x_2, \dots, x_6)$, consider the following subspaces:

$S_1 = \{x: x_1 = 0\}$	dimension 5
$S_2 = \{x: x_2 = x_3 = 0\}$	dimension 4
$S_3 = \{x: x_4 = x_5 = x_6 = 0\}$	dimension 3
$S_4 = \{111111 \text{ and } 000000\}$	dimension 1

These subspaces have the desired property of covering each nonzero vector at most twice, and so $n(6, 35) = g(6, 35)$.

However, even if we knew exact necessary and sufficient conditions for the existence of the subspaces S_i , we would not always get the best possible code. For $k=6$, $d=17$ we would need subspaces of dimensions 4, 3, 2, and 1 which covered every nonzero element at most once;

but it is easy to see that any two subspaces of dimensions 4 and 3 in V_6 must share at least one nonzero vector. Thus the Solomon-Stiffler results could not yield a (37, 6) code with $d = 17$. However in his original paper (Theorem 5) Griesmer gave a construction which yields such a code.

We conclude the paper with a table of those values of k and d with $k \leq 6$ for which $n(k, d) > g(k, d)$ (Table 1). The column labeled "comments" explains how we calculate $n(k, d)$. "HB" means that the Hamming bound forces

$n(k, d) > g(k, d)$. "Search" means that a computer search found no codes of length $g(k, d)$. An entry like " $n(5, 3)$ " refers to the bound, proved by Griesmer, that

$$n(k, d) \geq d + n(k - 1, \lceil d/2 \rceil)$$

Thus if $n(k - 1, \lceil d/2 \rceil) > g(k - 1, \lceil d/2 \rceil)$, then $n(k, d) > g(k, d)$ as well. We only list odd d because of the relationship $n(k, d) = n(k, d + 1) - 1$ for odd d .

References

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**Table 1. Values of k and d with $k \leq 6$ for which
 $n(k, d) > g(k, d)$**

k	d	$g(k, d)$	$n(k, d)$	Comments
5	3	8	9	HB; (9, 5) = (15, 11) Hamming shortened
5	5	12	13	Search; (13, 5) = (15, 7) BCH shortened
6	3	9	10	HB; (10, 6) = (15, 11) Hamming shortened
6	5	13	14	$n(5, 3)$; (14, 6) = (15, 7) BCH shortened
6	7	16	17	$n(5, 4)$; (17, 6) = (23, 12) Golay shortened
6	9	21	22	$n(5, 5)$; (22, 6) found <i>ad hoc</i> ^a
6	11	24	25	$n(5, 6)$; (25, 6) found <i>ad hoc</i> ^b
6	13	28	29	Search; (29, 6) = (31, 6) RM minus 2 columns
6	19	40	41	Search; (41, 6) = S.-S. construction w. dims. 3, 3, 3, 1. ($h = 1$).

^aTake as columns in the generator matrix the 6-place binary expansions of: 2, 3, 4, 6, 8, 9, 11, 12, 16, 17, 20, 21, 26, 32, 33, 38, 44, 51, 58, 61, 62, 63.

^bTake as columns 1, 1, 2, 4, 6, 8, 10, 13, 16, 18, 21, 27, 28, 31, 32, 34, 37, 43, 45, 46, 53, 54, 57, 58, 60.

On A Communications Strategy for Channels With Unknown Capacity

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When the capacity of a channel cannot be determined in advance, or if it can change unpredictably, there is a problem in selecting the rate of transmission. On the one hand, a design for the worst case prevents recovery of large amounts of data when the situation is better than anticipated. On the other hand, a design based on optimistic assumptions is threatened by total failure when the conditions are bad. This article discusses a strategy that covers the in-between range of possibilities, and its implementation on Mariner-type telemetry systems. It is shown that large increases in expected data rate can be obtained at the cost of small reductions in the minimum rate. Final decisions are made on the ground after all the data are received.

I. Introduction

In this article we shall be concerned with the question of how to maximize the expected data return when the channel capacity cannot be predicted in advance. An example of this type is a planetary entry probe to Venus or Jupiter, whose atmospheric transmission characteristics are not yet fully known. And even if they were known, these transmission characteristics would be subject to unpredictable changes due to planet weather and/or entry trajectory.

II. A Two-State Channel

Consider a situation where it is known that the channel capacity will be either 10 bits/s or 100 bits/s. Furthermore, suppose that the probability of 10 is λ so that the probability of 100 is $\bar{\lambda} = 1 - \lambda$. Also, suppose that the above

information is all that is known prior to launch of a spacecraft whose mission is to explore the atmosphere of a planet by means of an atmospheric entry probe that burns. At what data rate should the probe transmit? No communication is assumed from Earth to probe, and final data rate decisions must be made on the ground, after all the data are in.

III. The Conservative Strategy

A conservative strategy is based on the knowledge that transmission at a rate greater than channel capacity is impossible. Thus, if a transmission rate of more than 10 bits/s is adopted and the channel capacity turns out to be only 10 bits/s no information will be received. Consequently, to prevent a calamity, the conservative approach is to trans-

mit at 10 bits/s (we define channel capacity as the rate achievable with known coding/decoding schemes). Unfortunately, this scheme provides only 10 bits/s even when the capacity turns out to have been 100 bits/s. The transmitter cannot determine the channel capacity and adapt its rate, as assumed, because of the short duration of the mission and minimum complexity of the probe. The expected rate is the same as the minimum rate: $E[R] = R_{\min} = 10 \text{ bits/s}$.

IV. The Aggressive Strategy

An aggressive or gambling approach is to hope for the occurrence of the 100 bit/s situation and elect to transmit at the maximum rate. However, even if the probability $\bar{\lambda}$ of this eventuality is high, say 0.9, there is still a 10 per cent chance that the capacity will be 10 bit/s and no data will be received.

In general, the expected data return is

$$E[R] = 100 \text{ bits/s} \times (\text{probability capacity} = 100 \text{ bits/s}) \\ + 0.0 \times (\text{probability capacity} = 10 \text{ bits/s}) = 100\bar{\lambda}$$

Thus, if $\lambda = 0.9$, $E[R] = 90$, which is much higher than the guaranteed 10 bits/s of the conservative strategy. Although the expected return is now much higher, the 10% possibility of a total failure is, to say the least, disquieting, and almost surely unacceptable; even 1% is probably unacceptable.

V. The Prudent Strategy (α -strategy)

In the above examples we have seen two extremes of system design. The question that remains is whether it is possible to eliminate the risk of the gambler as well as the regret of the faint-hearted conservative. It turns out that a trade-off is possible. If one is willing to accept a guaranteed rate less than 10 bits/s it becomes possible to receive at a greater rate when the capacity is 100.

One method for achieving this intermediate state is to time share the rates. The transmitter is designed to transmit at 10 bits/s for a fraction α of the time and at 100 bits/s for $\bar{\alpha} = 1 - \alpha$ of the time. Another way is to allocate the total power P in the above proportions to two subcarriers, one modulated by high rate data using $\bar{\alpha}$ of the power, the other by low rate data using α of the power. Now, the received data rate is 10α if the capacity is 10 but it is

$10\alpha + 100\bar{\alpha}$ if capacity is 100. The expected rate is, therefore,

$$E[R] = (10\alpha)\lambda + (10\alpha + 100\bar{\alpha})\bar{\lambda} \\ = 10\alpha + 100\bar{\alpha}\bar{\lambda}$$

and the minimum rate is guaranteed to be

$$R_{\min} = 10\alpha$$

Continuing the example with $\lambda = 0.1$, if we can accept an $R_{\min} = 9.0$ we will obtain $E[R] = 18$; i.e., an 80% expected improvement for a 10% risk with a 90% chance of 19 bits/s.

In general, letting C_1 and C_2 designate the low and high capacity values, we have the expected rate vs the guaranteed minimum rate

$$E[R] = \alpha C_1 + \bar{\alpha} C_2 \\ R_{\min} = \alpha C_1 \quad (1)$$

Equation (1) effectively summarizes our three strategies and is plotted in Fig. 1, that of the conservative corresponds to $\alpha = 1$, hence $E[R] = R_{\min}$, while $\alpha = 0$ yields the gamblers approach $E[R] = \bar{\lambda} C_2$, $R_{\min} = 0$.

VI. Extension to Multiple Rates

We shall now find that the α -strategy of transmitting at two rates is optimal even when the number of possible rates is greater than two, provided we restrict ourselves to time-sharing and only constrain the minimum rate. If we restrain rates, also if intermediate conditions occur, then we get a linear programming problem.

Consider a channel with capacities $C_1 \leq C_2 \leq \dots \leq C_n$ occurring with probability $P(C_k) = \lambda_k$. If we allocate the transmission rates in fractions α_k per C_k the expected rate, for a fixed α_1 , is

$$E[R] = \lambda_1 \alpha_1 C_1 + \lambda_2 (\alpha_1 C_1 + \alpha_2 C_2) \\ + \dots + \lambda_n (\alpha_1 C_1 + \alpha_2 C_2 + \dots + \alpha_n C_n) \\ = \sum_{k=1}^n \lambda_k \sum_{i=1}^k \alpha_i C_i \\ = \sum_{k=1}^n \alpha_k C_k \sum_{i=k}^n \lambda_i \\ = \alpha_1 C_1 + \sum_{k=2}^n \alpha_k C_k \left[\sum_{i=k}^n \lambda_i \right] \\ \leq \alpha_1 C_1 + (1 - \alpha_1) \max_{k>1} \left[C_k \sum_{i=k}^n \lambda_i \right]$$

The maximum is achieved by allocating the fraction $(1 - \alpha_1)$ for transmission at the rate $C_{\text{opt}} = C_m$ such that $C_m(\lambda_m + \lambda_{m+1} + \dots + \lambda_n) \geq C_k(\lambda_k + \lambda_{k+1} + \dots + \lambda_n)$ for all $k > 1$. The fraction α_1 is, as before, determined solely by the minimum rate $R_{\text{min}} = \alpha_1 C_1$.

VII. Equivalent and Mixed Strategies

Note that the strategy may not be unique because the function

$$C_k \sum_{i=k}^n \lambda_i$$

may achieve the same maximum for two or more (say M) values of k . In this case there will be an infinite set of equivalent strategies to achieve the maximum expected rate, of which at least M are two-rate strategies. For example, suppose that

$$C_2(\lambda_2 + \lambda_3 + \dots + \lambda_n) = C_m(\lambda_m + \lambda_{m+1} + \dots + \lambda_n) \\ > C_k(\lambda_k + \dots + \lambda_n)$$

for all $k > 1, k \neq 2, m$; then

$$\begin{aligned} \max E[R] &= \alpha_1 C_1 + (1 - \alpha_1) C_2 \sum_{k=2}^n \lambda_k \\ &= \alpha_1 C_1 + (1 - \alpha_1) C_m \sum_{k=m}^n \lambda_k \\ &= \alpha_1 C_1 + (1 - \alpha_1) \left[\beta C_2 \sum_{k=2}^n \lambda_k \right. \\ &\quad \left. + (1 - \beta) C_m \sum_{k=m}^n \lambda_k \right] \end{aligned}$$

where $0 \leq \beta \leq 1$. Therefore, the set of optimal strategies is $\{\alpha_1, \alpha_2 = (1 - \alpha)\beta, \alpha_m = (1 - \alpha_1)(1 - \beta)\}$ for any β in $[0, 1]$, and there are two strategies which can be realized by transmission at only two rates, viz., C_1 and C_2 , or C_1 and C_m , ($\beta = 0$ and $\beta = 1$). The rest require a mixture of the above two and transmission at C_1, C_2 and C_m .

VIII. Higher Order Strategies

When faced with a situation which can be achieved by means of a mixed strategy it is possible to employ the previous ideas to select a unique strategy on the basis of secondary preferences. This is best seen by an example: suppose $C_1 < C_2 < C_3$ and $C_2(\lambda_2 + \lambda_3) = C_3\lambda_3$. For this case we can achieve the maximum expected rate while ensuring a minimum rate by allocating $(1 - \beta)$

$(1 - R_{\text{min}}/C_1)$ to C_2 and $\beta(1 - R_{\text{min}}/C_1)$ to C_3 . Next, we note, on the one hand, that the *probability of receiving more than the minimum rate* is

$$\begin{aligned} P_r\{R > R_{\text{min}}\} &= (1 - \beta)(\lambda_2 + \lambda_3) + \beta\lambda_3 \\ &= \lambda_2 + \lambda_3 - \beta\lambda_2 \\ &\leq \lambda_2 + \lambda_3, \end{aligned}$$

and this probability achieves a maximum for $\beta = 0$. On the other hand, the probability of receiving at the highest rate (should it occur) is now nil. Thus, if we wish to *minimize the probability of missing the high-rate situation* we should consider

$$\begin{aligned} P_r\{R < C_3\} &= 1 - \beta\lambda_3 \\ &\geq 1 - \lambda_3, \end{aligned}$$

which is minimal when $\beta = 1$.

It is now evident that by varying β we can vary the apportionment of medium and high rate possibilities without affecting the maximum expected rate. (It is possible to present arguments for or against any such combination.) The most convincing case against mixed strategies, however, is that they require a greater variety of transmission rates, and thus, higher cost and other unavoidable losses, e.g. crossmodulation for frequency multiplexed channels or frame synchronization for time shared channels.

IX. Channels with a Continuum of Capacities

We conclude this topic by noting that the two-rate strategy is also valid for channels with capacity $C_\infty [C_1, \infty]$ and an associated probability distribution $F(C) = Pr\{x < C\}$. In this case

$$E[R] = R_{\text{min}} + (1 - R_{\text{min}}/C_1) \sup_C [C(1 - F(C))]$$

and the value of C which achieves the supremum is the maximum transmission rate for us.

X. Implementation on Mariner Type Telemetry Systems

Mariner-type telemetry systems are particularly suited to the implementation of an α -strategy because they have been designed to transmit at two independent rates simultaneously, provided carrier phase coherence can be maintained. However, of the total power transmitted, some must be dedicated to a carrier phase reference, and some is lost due to crossmodulation between the two channels

(Ref. 1). Since the crossmodulation loss is absent in the case of a single channel, it must be included in the evaluation of a two channel strategy as a reduction of channel capacity.

The total power is

$$P_T = P_a + P_b + P_c + P_{cm}$$

where P_a, P_b are the power allocations for the two channels, P_c is the carrier reference power and P_{cm} is the crossmodulation power. The crossmodulation power depends on the modulation scheme as well as upon P_a, P_b and P_c as follows:

$$P_{cm} = \begin{cases} \frac{\min(P_a, P_b) P_c}{\max(P_a, P_b)} & \text{for Interplex modulation (Ref. 1)} \\ P_a P_b / P_c & \text{for conventional PSK/PCM/PM} \end{cases}$$

Since $P_a P_b = \min(P_a P_b) \max(P_a P_b)$ we have, from above, that Interplex is preferable when $P_c \leq \max(P_a P_b)$, otherwise the conventional modulation scheme is better.

Now we shall be concerned with the quantity

$$P = P_a + P_b + P_{cm}$$

which represents the maximum amount of power the system can transmit as data, as, for instance, in the case of a single channel where P_{cm} and either P_a or P_b is zero. The practical capacity of the channel is $C = (P/N) \times \text{const}$ where N is the spectral density of additive Gaussian white noise and the constant is about 0.4 for practical encoding/decoding schemes. We are supposing that for one reason or another this channel capacity is either C_1 with probability λ or $C_2 > C_1$ with probability $1 - \lambda = \bar{\lambda}$. This may be due to changes in the strength of the noise (or lack of prior knowledge thereof), or fading of signal strength due to mispointing of the transmitting antenna, caused by meteor impact, or, when entering a planetary atmosphere slowing due to gusts.

The power allocation called forth by the α -strategy is

$$P_a = \alpha(P - P_{cm}) = \alpha P(1 - P_{cm}/P)$$

$$P_b = 1 - \alpha(P - P_{cm}) = \bar{\alpha} P(1 - P_{cm}/P)$$

Therefore, in the case of Interplex modulation,

$$\frac{P_{cm}}{P} = \Delta \frac{\min(\alpha, \bar{\alpha})}{\max(\alpha, \bar{\alpha})}$$

where

$$\Delta = P_c/P,$$

and, in the case of conventional PSK/PM

$$\frac{P_{cm}}{P} = \begin{cases} (2\sqrt{\alpha\bar{\alpha}} - \Delta)/(1 + 2\sqrt{\alpha\bar{\alpha}}) & \text{if } \sqrt{\alpha\bar{\alpha}} \geq \Delta \\ 1 + \frac{\Delta}{2\alpha\bar{\alpha}} - \sqrt{\frac{\Delta}{\alpha\bar{\alpha}} + \left(\frac{\Delta}{2\alpha\bar{\alpha}}\right)^2} & \text{otherwise} \end{cases}$$

The above expressions for P_{cm}/P must be included in plotting the "operating characteristics" ($E[R]$ vs $R_{\min}$) of the α -strategy, since

$$E[R] = (\alpha C_1 + \bar{\lambda} \bar{\alpha} C_2)(1 - P_{cm}/P)$$

and

$$R_{\min} = \alpha C_1(1 - P_{cm}/P)$$

Figure 2 is a sample plot of the operating characteristics for the case $C_1 = 10$ bits/s, $C_2 = 100$ bits/s and $\lambda = 0.1$.

It is important to stress that the operating characteristics of Fig. 2 compare only the efficiency of systems with the same net power $P = P_T - P_c$. This is done because the carrier reference power has, until this writing, been set by doppler navigation considerations beyond the control of the telemetry systems engineer. Keeping this in mind it is evident that the overall system efficiency $(P_a + P_b)/P_T$ decreases as Δ increases in both single channel and double channel systems.

Under most normal conditions, however, Δ is small ($\Delta < 0.2$) and Interplex modulation becomes almost as good as ideal time share and may even be better after provisions for timing sync in time share are taken into account.

We conclude this section with an example based on Fig. 2, with $\Delta = 0.1$, which shows that an α -strategy using two-channel Interplex increases the expected data rate from 10 bits/s of the conservative design ($\max R_{\min}$) to 23 bits/s if we can accept a minimum guarantee of 8 bits/s. Moreover, the probability of achieving this 3 + dB gain is 90%. Had C_2/C_1 been equal to 100 the gain would have been in excess of 12 dB.

XI. Conclusion

This article presented a practical approach toward improving the cost effectiveness of deep space telemetry sys-

tems for missions in which the transmission rate cannot be ascertained in advance, or altered after launch. The key idea is to back off from the maximum data rate in the worst case in order to have some facility for high rate transmission in case conditions are better.

We conclude by noting that the approach presented here appears to be applicable to situations where the state of the channel may require different signaling methods, i.e., in one state, non-coherent communications may be required while in other states coherent communication,

with or without coding, may be possible; or, non-coherent transmission may be required in all cases. The latter could occur if carrier frequency and/or phase synchronism cannot be maintained due to rapidly varying doppler, as when approaching a planet.

Another possibly fruitful endeavor is the development of signaling schemes that can be decoded not only at high rates when conditions are favorable, but, also at low rates to recover part of the transmitted data when conditions are adverse.

Reference

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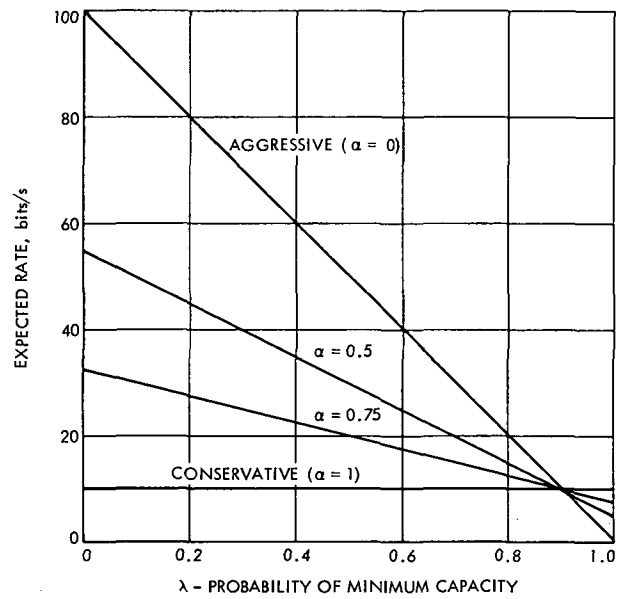


Fig. 1. Illustration of α -strategy

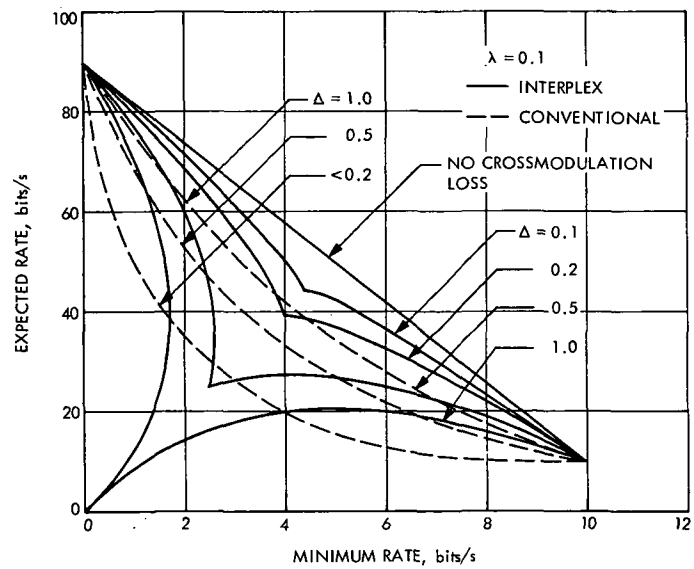


Fig. 2. Operating characteristics of Mariner telemetry using α -strategy

Hiding and Covering in a Compact Metric Space

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This article studies the relationship between games of search on a compact metric space X and the absolute epsilon entropy $I(X)$ of X . The main result is that $I(X) = -\log v_L^$, v_L^* being the lower value of a game on X we call "restricted hide and seek."*

I. Introduction

Let X be a set, S a collection of subsets of X with $\cup S = X$. The two-person zero-sum game "hide and seek" $G(X, S)$ is played as follows. Player 1 (the "hider") chooses a point $x \in X$, and player 2 (the "seeker") chooses $s \in S$. If $x \in s$, player 1 pays player 2 one unit; otherwise no payoff occurs. Let us denote the value of this game, if it exists, by v . (We assume that X has enough structure so that mixed strategies can be defined.)

Now, for each integer N , let c_N be the smallest integer such that the cartesian power X^N can be covered with c_N sets from S^N , and let

$$c = \lim_{N \rightarrow \infty} c_N^{1/N}$$

The main theorem of a previous paper (Ref. 1) was that if X is finite, $v = c^{-1}$. It is the object of this article to

study the relationship between v and c when X is a compact metric space, and S is the set of closed spheres of radius ϵ .

Our first main result (Theorem 1) is that in this situation, the game G still has a value. For finite X , von Neumann's fundamental theorem on finite two-person zero-sum games immediately implies that v exists, and so in Ref. 1 this problem did not arise.

Our second main result is that $c = v^{-1}$ is not true in general, but rather that $c = (v^*)^{-1}$, where v^* is the best expected gain the "seeker" can guarantee himself when he must restrict his sets to a finite subset of X he has chosen in advance. It is always true that $v^* \leq v$, and for a fixed X , $v^* = v$ except for at most countably many values of ϵ . In Section IV, however, we give an example of a compact metric space for which $v^* < v$. In Section V, we prove that $c = (v^*)^{-1}$.

These problems arise in information theory. The logarithm of the limit c is the least average number of bits per sample necessary to describe X modulo S ; i.e., to identify an s containing x , when block coding is used, and when there is no *a priori* probability distribution on X . We shall show at the end of Section V that $-\log v$ represents the maximum, over all Borel *a priori* probability distributions on X , average number of bits per sample necessary to describe X to within an ambiguity of ϵ , when variable-length coding is used. Thus, when $v = c^{-1}$ (the usual state of affairs in spite of our counterexample), there exist probability distributions on X which render variable-length coding useless.

II. General Hide and Seek

If the hider chooses his point x according to a probability distribution λ on (a Borel field containing the points of) X , we say he uses strategy λ . Similarly a strategy μ for the seeker is a probability distribution on (a Borel field containing the points of) S . Let $E = \{(x,s): x \in s\}$, a subset of the product space $X \times S$. The expected value of the payoff, given that the hider plays strategy λ_x for the hider as that strategy which always $\lambda \times \mu$ being the product measure induced by λ and μ on $X \times S$.

If the hider uses a fixed strategy λ , then from his point of view the worst possible expected payoff is

$$\sup_{\mu} v(\lambda, \mu)$$

Hence he will choose a λ which makes

$$\sup_{\mu} v(\lambda, \mu)$$

as small as possible. Thus we define the *upper value* of $G(X, S)$ as

$$v_U(X, S) = \inf_{\lambda} \sup_{\mu} v(\lambda, \mu) \quad (1)$$

Similarly the seeker will choose a μ which makes

$$\inf_{\mu} v(\lambda, \mu)$$

as large as possible, and we define the *lower value* of $G(X, S)$ as

$$v_L(X, S) = \sup_{\mu} \inf_{\lambda} v(\lambda, \mu) \quad (2)$$

It is an easy exercise to show that $v_L \leq v_U$. If it happens that $v_L = v_U$, we denote this common value by $v(X, S)$, and say that the game $G(X, S)$ has a value. If the game has a value, then for every $\eta > 0$, there exist strategies λ and μ such that if the hider plays λ , his expected loss is $\leq v(X, S) + \eta$ no matter how the seeker plays, and if the seeker plays μ , his expected gain is $\geq v(X, S) - \eta$ no matter how the hider plays. If it happens that there exist strategies λ for the hider which guarantee an expected loss no greater than $v(X, S)$, these strategies are called *optimal* strategies. Optimal strategies for the seeker are defined similarly.

There is another form of the definitions of v_U and v_L which will be useful in what follows. By the definition of product measure we can write $v(\lambda, \mu)$ as either of the integrals

$$\begin{aligned} v(\lambda, \mu) &= \int_X \mu(\text{star}(x)) d\lambda \\ &= \int_S \lambda(s) d\mu \end{aligned} \quad (3)$$

where $\text{star}(x) = \{s \in S \mid x \in s\}$. Now if we define the *pure strategy* λ_x for the hider as that strategy which always chooses x ; i.e., $\lambda(x) = 1$, $\lambda(x') = 0$ if $x' \neq x$, we see that $\mu(\text{star}(x)) = v(\lambda_x, \mu)$. Similarly, if μ_s is a pure strategy for the seeker, $\lambda(s) = v(\lambda, \mu_s)$. Thus from Eq. (3), we obtain the estimate

$$v(\lambda, \mu) \leq \sup_{s \in S} \lambda(s) = \sup_{s \in S} v(\lambda, \mu_s)$$

Hence, for a fixed λ ,

$$\sup_{\mu} v(\lambda, \mu) = \sup_{s \in S} v(\lambda, \mu_s)$$

and so

$$v_U(X, S) = \inf_{\lambda} \sup_{s \in S} \lambda(s) \quad (4)$$

and similarly

$$v_L(X, S) = \sup_{\mu} \inf_{x \in X} \mu(\text{star}(x)) \quad (5)$$

Let us remark finally that if the set X is finite, it is a consequence of the fundamental theorem of finite two-person, zero-sum games that $G(X, S)$ has a value (Ref. 2, Chap. 7).

III. Hide and Seek in a Compact Metric Space

For the remainder of the article, X will be a compact metric space, and S will be the set of closed spheres¹ of radius ϵ for a fixed ϵ : $s_\epsilon(x) = \{y \in X: d(y, x) \leq \epsilon\}$. This game is denoted by $G(X, \epsilon)$. In this case strategies for the hider and the seeker will both be Borel probability distributions on X , since the seeker need only specify the center of the sphere he wishes to select. In the product space $X \times X$, the set $E = \{(x, y): d(x, y) \leq \epsilon\}$, and for strategies λ and μ , $v(\lambda, \mu) = (\lambda \times \mu)(E)$. Before proceeding we need a result on weak convergence.

Let $B(X)$ be the space of all Borel probability distributions on X , and $C(X)$ the space of real-valued continuous functions on X . The topology of weak convergence on $B(X)$ is defined as follows (Ref. 3, Chap. II): $\mu_n \rightarrow \mu$ in $B(X)$ if for every $f \in C(X)$ $\int f d\mu_n \rightarrow \int f d\mu$. $B(X)$ is compact in this topology (Ref. 3, p. 64), and if F is any closed subset of X and $\mu_n \rightarrow \mu$, then (Ref. 3, p. 40)

$$\mu(F) \geq \limsup_{n \rightarrow \infty} \mu_n(F) \quad (6)$$

We now consider probability distributions on the product space $X \times X$. The following proof, as are all proofs in this article, is omitted.

LEMMA 1. If $\mu_n \rightarrow \mu$ and $\lambda_n \rightarrow \lambda$, then $\mu_n \times \lambda_n \rightarrow \mu \times \lambda$.

LEMMA 2. If $\lambda_n \rightarrow \lambda$ and $\mu_n \rightarrow \mu$, then

$$v(\lambda, \mu) \geq \limsup_{n \rightarrow \infty} v(\lambda_n, \mu_n)$$

We now have the main theorem of this section.

THEOREM 1. $G(X, \epsilon)$ has a value $v(\epsilon)$ which is continuous from above in ϵ , and the seeker has an optimal strategy. For every $\delta > 0$ the hider has a strategy with finite support which guarantees that he loses no more than $v(\epsilon) + \delta$. The set of optimal strategies for the seeker is closed in the topology of weak convergence.

We conclude this section with three examples which show the necessity of certain of the hypotheses in Theorem 1.

Example 1. The hider need not have an optimal strategy. X will be a countable subset of the unit circle, under the geodesic metric. Let $x_n = \exp(\pi i / 2^{n+1})$. X will

¹However, the results in this article also hold when S is the set of closed sets of diameter $\leq \epsilon$.

consist of the points $\pm x_n, \pm ix_n$ for all n . Then X is closed and so compact. Let $\epsilon = \pi/2$; for each $x \in X$ we adopt the abbreviation $s(x) = s_{\pi/2}(x)$. Then if the seeker plays ± 1 each with probability $1/2$, his expected gain against any pure hider's strategy will be $\geq 1/2$ and so $v_L \geq 1/2$. On the other hand if the hider uses the strategy λ_N defined by $\lambda_N(x) = 1/2N$ for $x = \pm x_1, \pm x_2, \dots, \pm x_N$; $\lambda_N(x) = 0$ otherwise, then $\lambda_N(s(x)) = 1/2 + 1/2N$ if $x = \pm ix_n$ for some $n \leq N$; $\lambda_N(s(x)) = 1/2$ otherwise, and so the hider's expected loss is $\leq 1/2 + 1/2N$ for any pure seeker's strategy. Thus $v_U \leq 1/2 + 1/2N$ for any N , and so $G(X, \pi/2)$ has value $1/2$. If, however, the hider had an optimal strategy λ , $\lambda(s(x)) \leq 1/2$ for all $x \in X$, then it would follow from $\lambda(s(x)) + \lambda(s(-x)) = 1 + \lambda(ix) + \lambda(-ix)$ that $\lambda(ix) = \lambda(-ix) = 0$ for all $x \in X$, a contradiction.

Example 2. The set of optimal strategies for the hider, if nonempty, need not be closed. Let X be the closed interval $[0, 4]$ under the usual metric, and $\epsilon = 1$. Then $v(X, \epsilon) = 1/2$, and if λ_n is the strategy $\lambda_n(0) = \lambda_n(2 + (1/n)) = 1/2$, λ_n is optimal for all $n \geq 1$. However $\lambda_n \rightarrow \lambda$ where $\lambda(0) = \lambda(2) = 1/2$, but λ itself is not optimal since if the seeker always picks the sphere centered at 1 his gain against λ is always 1.

Example 3. The seeker need not have finitely based nearly optimal strategies such as the hider has; i.e., it is possible that there exists $\delta > 0$ such that if μ is any finitely based strategy (a probability distribution on X which is zero outside a finite subset of X), then $\mu(s_\epsilon(x)) \leq v(\epsilon) - \delta$ for some $x \in X$. This example is best understood in the context of a game we call "restricted hide and seek," introduced in the next section, so we postpone it until then.

IV. Restricted Hide and Seek

In restricted hide and seek, before play begins the seeker is required to choose a finite subset X' of X (unknown to the hider) and then must always choose a sphere of radius ϵ whose center is in X' . Of course, a referee who knows X' will be needed to keep the seeker honest, since there is no way the hider will be able to tell whether or not the seeker is staying in X' . We denote this game as $G^*(X, \epsilon)$ and define $v_L^*(\epsilon)$, $v_U^*(\epsilon)$ as in Section II. Let

$$v(\epsilon-) = \lim_{\epsilon' \uparrow \epsilon} v(\epsilon')$$

LEMMA 3. $v(\epsilon-) \leq v_L^*(\epsilon) = v(\epsilon)$.

LEMMA 4. $v_L(\epsilon) = v(\epsilon)$ with at most countably many exceptions.

If X has only two points x, y and $d(x, y) = 1$, then $v(X, 1-) = 1/2$ but $v(X, 1) = v_L^*(X, 1) = 1$. It is much more difficult to give an example which shows that v_L^* may be strictly less than v_L . We now mention such an example. Details are omitted.

Example 3. There exists a compact metric space X such that $v(X, 1-) < v_L^*(X, 1) < v(X, 1)$. Let C be a circle of circumference 4, d the geodesic metric on C , and let H_C be the space of closed subsets of C under the Hausdorff metric d' :

$$d'(E, F) = \max \left(\max_{e \in E} \min_{f \in F} d(e, f), \max_{f \in F} \min_{e \in E} d(e, f) \right)$$

H_C is a compact metric space under d' (Ref. 4). The set Z of all closed subsets of C of Lebesgue measure 2 is a closed, hence compact, subspace of H_C and is therefore separable. Let $\{B_i, i \geq 1\}$ be a countable dense subset of Z . No finite subset $\{b_k\}$ of C has the property that every B_i contains a b_k . For $\{b_k\}$ can be covered by an open set of arbitrarily small Lebesgue measure and so there exists a set $B \in Z$ and $d_0 > 0$ such that $d(B, b_k) \geq d_0$ for all k . Thus a B_i such that $d'(B, B_i) < d_0$ cannot contain a b_k .

The space X of this example will have C as a subspace, the metric restricted to C being the geodesic metric. It also contains points $a; a_i, i \geq 1$, where

$$\begin{aligned} d(a, c) &= 1 \text{ for } c \in C \\ d(a, a_i) &= 2^{-i} \\ d(a_i, a_j) &= |2^{-i} - 2^{-j}| \\ d(a_i, c) &= 1 + \min(d(B_i, c), 2^{-i-1}) \text{ for all } c \in C \end{aligned}$$

In addition X contains three points c'_1, c'_2, c'_3 which are to be thought of as outside the circle C and equally spaced in angle. The point on C closest to c'_i is labeled c_i . The metric is extended as follows:

$$\begin{aligned} d(c'_i, a) &= d(c'_i, a_j) = \frac{15}{8} \text{ for all } i, j. \\ d(c'_i, c_i) &= \frac{7}{8} \\ d(c'_i, c) &= \begin{cases} \frac{7}{8} + d(c_i, c), & \text{if } d(c_i, c) \leq \frac{1}{8} \\ 1, & \text{if } \frac{1}{8} \leq d(c_i, c) \leq 1 \\ d'(c_i, c), & \text{if } d(c_i, c) \geq 1 \end{cases} \text{ for } c \in C \end{aligned}$$

We assert that (X, d) as defined above is indeed a compact metric space, but omit the tedious verification that d satisfies the triangle inequality. Compactness is best verified by checking sequential compactness, which is equivalent to compactness for a metric space. The space X is sketched in Fig. 1, topologically embedded in three-space.

It can be shown that

$$v(X, 1-) = \frac{1}{3}, \quad v_L^*(X, 1) = \frac{2}{5}, \quad v(X, 1) \geq \frac{1}{2}$$

Details are omitted.

V. Absolute Epsilon Entropy

Let us use the term " ϵ -set" to describe a subset of a compact metric space which is contained in some sphere of radius ϵ . The *epsilon entropy* $H_\epsilon(X)$ is then defined to be $\log_2 N$, where X can be covered with N ϵ -sets, but no fewer. $H_\epsilon(X)$ can be interpreted information theoretically as the minimum average number of bits per sample needed to describe X to within an error of at most ϵ .

If $(X_i, d_i), i = 1, 2, \dots, n$, are compact metric spaces, we shall make the cartesian product $X_1 \times X_2 \times \dots \times X_n$ into a compact metric space by defining

$$d((x_1, \dots, x_n), (x'_1, \dots, x'_n)) = \max_i d(x_i, x'_i)$$

With this definition, products of ϵ -sets are ϵ -sets and projections of ϵ -sets onto the coordinate spaces X_i are ϵ -sets; hence it is a suitable definition for dealing with uniform approximation. If $X_i = X$ for all i , we shall write X^n instead of $X_1 \times \dots \times X_n$.

The *absolute epsilon entropy* $I_\epsilon(X)$ is defined by

$$I_\epsilon(X) = \lim_{n \rightarrow \infty} \frac{1}{n} H_\epsilon(X^n)$$

That the limit exists is a consequence of the simple property $H_\epsilon(X^{n+m}) \leq H_\epsilon(X^n) + H_\epsilon(X^m)$. $I_\epsilon(X)$ can be interpreted as the minimum average number of bits per sample needed to describe X to within ϵ when an unlimited number of samples can be stored prior to transmission.

Theorem 2, the main result of this article, identifies $I_\epsilon(X)$ in terms of the game "restricted hide and seek."

THEOREM 2. $I_\epsilon(X) = -\log v_L^*(X; \epsilon)$.

Theorem 2 requires two lemmas.

LEMMA 5. $H_\epsilon(X) = -\log v_L^*(X; \epsilon)$.

LEMMA 6. $v_L^*(X \times Y, \epsilon) = v_L^*(X, \epsilon) v_L^*(Y, \epsilon)$.

We conclude the article with two corollaries to Theorem 2. Let p be a Borel probability measure on X , and let $H_{\epsilon,p}(X)$ be the infimum of over all partitions

$$X = \bigcup_i A_i, A_i \cap A_j = \emptyset \text{ if } i \neq j$$

each A_i being a Borel ϵ -set of X , of the Shannon entropy

$$-\sum_i p(A_i) \log p(A_i)$$

$H_{\epsilon,p}$ is called the $\epsilon;p$ entropy of X (Ref. 5). Also define the absolute $\epsilon;p$ entropy of X by

$$I_{\epsilon,p}(X) = \lim_{n \rightarrow \infty} \frac{1}{n} H_{\epsilon,p} n(X^n)$$

p^n being the product measure induced on X^n by p . $I_{\epsilon,p}(X)$ then represents the minimum average number

of bits per sample necessary to describe X with an error not exceeding ϵ , with p as the *a priori* probability distribution on X , when arbitrarily long variable-length codes are used. Combining Theorem 2 with Theorem 2 of Ref. 1, which had $-\log v(X, \epsilon) = \sup_p I_{\epsilon,p}(X)$, we conclude:

Corollary 1.

$$I_\epsilon(X) = \sup_p I_{\epsilon,p}(X)$$

whenever $v_L^*(X, \epsilon) = v(X, \epsilon)$; in particular equality holds for all but at most countably many ϵ .

Hence most of the time "nature" can choose a p on X which is so "bad" that prior knowledge of p could not be used to increase the transmission rate.

Our final result is a simple consequence of Theorem 2 and Lemma 6, and tells us that one cannot save anything by encoding two sources simultaneously:

Corollary 2. $I_\epsilon(X \times Y) = I_\epsilon(X) + I_\epsilon(Y)$.

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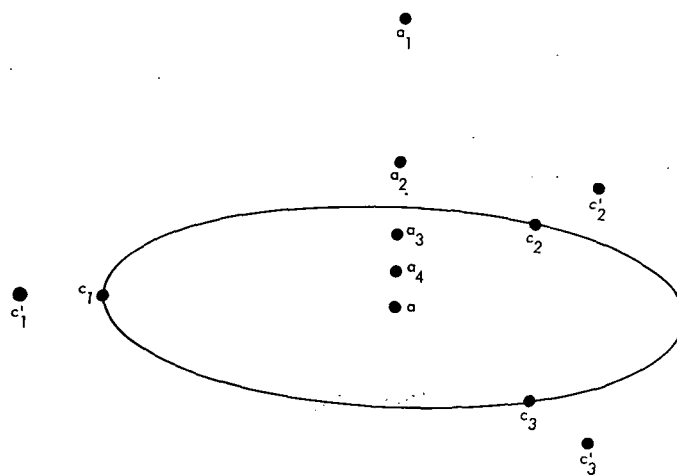


Fig. 1. The space X of counterexample 3

New Hardware Realizations of Non-Recursive Digital Filters

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Analysis of the bit-level operations involved in the convolution realizing a non-recursive digital filter leads to hardware designs of digital filters based on the operation of counting. Two distinct designs are outlined: The first one is capable of very high speed, but is rather expensive. The second one is quite slow, but has the advantages of low cost and high flexibility. The basic designs considered utilize fixed point representation for the data and filter coefficients. Variants which allow floating point representation of the coefficients are also described.

I. Introduction

Digital filters are fast becoming an important element in all DSN data handling systems. They are particularly advantageous in systems which are digital throughout. In many applications they also offer significant reductions in data storage requirements.

Consider a filter which transforms its input time function $\xi(t)$ ¹ to the filtered time function $\eta(t)$. A non-recursive digital filter simulates such a filter by computing samples of the filtered signal,

$$\eta_k = \eta(kT_s) \quad (1)$$

¹All quantities dealt with in this paper are real.

from samples of the input signal,

$$\xi_k = \xi(kT_s), \quad (2)$$

according to the formula

$$\eta_m = \sum_{k=0}^{K-1} \xi_{m-k} \alpha_k \quad (3)$$

in which the coefficients α_k are obtainable from the filter transfer function.

There is a growing need for special-purpose machines that would implement such a filter. Particularly attractive here are machines that would produce filtered output

samples at the rate input samples are generated in the data acquisition environment.

An obvious strategy in realizing such a machine is to compute η_m via the following rephrasing of Eq. (3):

$$\left. \begin{aligned} p_{mk} &= \xi_{m-k} \alpha_k \\ \eta_m &= \sum_{k=0}^{K-1} p_{mk} \end{aligned} \right\} \quad (4)$$

that is, the desired output, η_m , is evaluated through the intermediate entities p_{mk} which require the use of a multiplier.

We propose here a different strategy in which the intermediate entities are obtained by counting. Our main purpose in this paper is to survey the various possible designs implementing this strategy. Interesting and promising designs are indicated in the high-speed high-cost category as well as the low-speed low-cost class. The paper is organized along the following lines: A master design is developed in *Sections II* and *III*. This design serves as the starting point for developing two different basic designs in *Sections IV* and *V*. *Section IV* presents a high-speed design involving high cost. *Section V* is devoted to an inexpensive low-speed design. Several variants of these two designs are also considered.

II. The Master Design

Let us assume (temporarily) that the data and coefficients satisfy

$$\xi_k, \alpha_k \geq 0 \quad (5)$$

This assumption simplifies the presentation of the main features of the master design and will be removed in *Section III*.

In representing ξ_k, α_k in the machine, we assign J_x bits to each input data word and J_a bits to each coefficient. Denoting by primes the truncated versions of ξ_k, α_k consistent with the finite J_x, J_a , we represent the data and coefficients by the integers x_k, a_k defined as follows:

$$\left. \begin{aligned} \xi'_k &= 2^{-x} x_k \\ \alpha'_k &= 2^{-A} a_k \end{aligned} \right\} \quad (6)$$

Suitable values of A, X can be determined from the known ranges of α_k, ξ_k .

The immediate effect of the above representation is that the machine will substitute the approximation η'_m for the true η_m where

$$\eta'_m = \sum_{k=0}^{K-1} \xi'_{m-k} \alpha'_k \quad (7)$$

η'_m may be regarded as a sample of the approximated output $\eta'(t)$.

Note that the adopted representation is equivalent to a fixed-point binary representation. Adaptations employing floating point representation for the coefficients are possible with a reasonable amount of extra hardware. Such adaptations are described in *Sections IV* and *V*.

Substituting Eq. (6) in Eq. (7) we get

$$y_m = \sum_{k=0}^{K-1} x_{m-k} a_k \quad (8)$$

where

$$y_m = 2^{(A+X)} \eta'_m \quad (9)$$

is an integer.

Let us examine now the implication of Eq. (8) in terms of bit-level operations. We start by writing down explicitly the binary representations of a_k, x_k

$$\left. \begin{aligned} a_k &= \sum_{j=0}^{J_a-1} u'_{kj} 2^j & u'_{kj} &= 0,1 \\ x_k &= \sum_{j=0}^{J_x-1} v'_{kj} 2^j & v'_{kj} &= 0,1 \end{aligned} \right\} \quad (10)$$

Using the representation (10) in Eq. (8), we get an explicit expression for y_m as a triple sum

$$y_m = \sum_{k=0}^{K-1} \sum_{r=0}^{J-1} \sum_{i=0}^{J_a-1} u'_{ki} v'_{m-k, r-i} 2^r \quad (11)$$

where

$$J = J_a + J_x - 1 \quad (12)$$

Application of the "multiply-then-add" strategy of Eq. (4) is equivalent to summing over i, r first (thus getting the p_{mk} 's) and only then performing the k summation. In the scheme proposed here, we change the order of summa-

tion, making the r summation the last one. Thus, denoting

$$\sum_{k=0}^{K-1} \sum_{i=0}^{J_a-1} u'_{ki} v'_{m-k, r-i} = h'_r \quad (13)$$

we have

$$y_m = \sum_{r=0}^{J-1} h'_r 2^r \quad (14)$$

Strictly speaking, the entity defined in Eq. (13) should be denoted h'_{mr} . However, since in most of the following discussion m is constrained to a specific constant value, the simpler notation, h'_r , will do.

Equations (13) and (14) embody the basic strategy of the proposed machine. Let us examine Eq. (13) first. Each element of the double sum is a product of two 1-bit entities. Such a product is either 0 or 1 and, practically speaking, no multiplication is involved in its evaluation. A dual input AND gate is all that is needed. Equation (13) is a summation of KJ_a such terms. Thus, if we design a system in which KJ_a dual input gates are fed by the pairs of bits specified in Eq. (13), a count of the number of TRUE gates, will equal h'_r .

Equation (14) is implemented by regarding its right-hand side as a polynomial with coefficients h'_r , evaluated for the argument 2. Applying the well-known polynomial algorithm we get

$$y_m = (\cdots (h'_{J-1} \cdot 2 + h'_{J-2}) 2 + \cdots + h'_1) 2 + h'_0 \quad (15)$$

The realization of Eq. (15) can now be carried out in a sequence of shift and add operations in a standard accumulator.

The above discussion leads to the general outline of the machine shown in Fig. 1. We see here four basic elements:

- (1) A fixed register (A) holding the coefficients a_k prescribing the filter transfer function. Its contents would normally stay fixed throughout a specific filter simulation. They may, however, be varied in the course of the filtering process to realize an adaptive filter.
- (2) A shift register (X) holding the input words x_i . These are fed on the right, a bit at a time. Registers A, X are cross-linked by AND gates.

- (3) A counter that counts the number of TRUE gates after every shift of register X. Each such count will be shown to equal a specific h'_r .
- (4) An accumulator that combines J counter outputs through a shift and add sequence to generate the output word y_m .

A. A Detailed Example

We turn our attention now to the data configuration in registers A and X. This is most easily illustrated in terms of a specific example. We adopt the following parameters for our example:

$$K = 3; \quad J_a = 5; \quad J_x = 3 \quad (16)$$

These values (particularly K) are too low to be realistic. Their adoption, however, facilitates the presentation of detailed bit configurations and thus makes it easier to grasp the details of the proposed machine. This example is adopted in most of the figures in this paper.

The situation at some intermediate point in the computation of y_m is shown in Fig. 2b where the following convention is followed: A numeral in a register cell represents the radix power assigned to a 1 bit in that location. This power is referred to as the weight of the bit. We shall find it convenient to designate the bit itself by its weight. Thus, we may say that the first cell on the right of register A contains bit 4 of a_0 . Some of the bits are zero independently of the data. These are indicated by the letter z .

We note first that successive x_i 's are separated by $J_a - 1$ ($=4$) zero bits. Thus, it takes J ($=7$) bit times (shifts) to feed one input word.

Similarly, the A register indicates a separation of $J_x - 1$ ($=2$) zero bits between successive words. Here, however, there is no need to have a hardware implementation of these zero bits so that the A register could be split into K independent registers.²

Next, we observe that the x_i 's have their most significant bit on the left, while the a_k 's have their most significant bit on the right. The spacing and the reversed

²One would still implement the A register as a single continuous register when it turns out to be convenient to perform the initial loading of A serially. In this case, A would be a shift register. Another argument for a single A register is the flexibility it allows in modifying word size. (Note that for 1-bit x_k 's, there is no spacing in the A register).

bit arrangement guarantee that all pairs of bits feeding a common gate satisfy the index relation required by Eq. (13). The double summation appearing there translates simply into a count of all TRUE gates in Fig. 2b. In the specific situation shown here, the count would yield h'_4 . Similarly, shifting the X register one bit to the left will now yield h'_3 , and so on.

Having seen how an h'_r is generated in the counter output, we can consider now the overall scheme culminating in the output y_m .

The processing starts with the initial situation shown in Fig. 2a where a count yields h'_6 of y_m (h'_{j-1} in the general case). We load this count into the accumulator and proceed to compute h'_5 . This is done by shifting the X register one bit to the left and counting the TRUE gates. We return now to the accumulator, shift its contents left one bit (equivalent to multiplying by 2) and add h'_5 . The succession of these shift and add operations is the step by step implementation of Eq. (15). We proceed with this sequence up to the last cycle depicted in Fig. 2c. A count here yields h'_0 . We return now for the last time to the accumulator, shift its contents one bit to the left and add h'_0 . It now contains the final result, y_m .

Examination of Fig. 2c shows that when the above process is continued, the next 1-bit left shift will bring into the X register the most significant bit of x_{m+1} . The resulting configuration is almost identical with the one initiating the computation of y_m (Fig. 2a). The only difference is the replacement of m by $m+1$. Hence, the sequence of operations described here automatically leads to the computation of y_{m+1} following the computation of y_m , and so on.

The basic design outlined here is valid only when both data and coefficients are non-negative. In the next section we proceed to remove this constraint.

III. Modified Design to Allow Negative Numbers

General-purpose computers usually handle negative numbers either by the "sign-magnitude" representation or via the use of "2's-complement." Both methods are quite inappropriate in the present application, as they would drastically increase the complexity of the machine.

A possible solution³ is to apply bias to both data and coefficients so that the numbers presented to the ma-

chine are always positive. This requires corrective measures to compensate for the bias. The logic implementation of these measures has been worked out⁴ but will not be presented here. Instead, a simpler more attractive solution based on a negative radix number representation (Refs. 1, 2) will be described in detail. Specifically, we consider representing data and coefficients in base (-2) . As a simple illustration, consider the number 3:

$$\begin{aligned} 3 &= 1 \cdot 2^1 + 1 \cdot 2^0 = 11_2 \\ &= 1 \cdot (-2)^2 + 1 \cdot (-2)^1 + 1 \cdot (-2)^0 = 111_{-2} \end{aligned}$$

Similarly,

$$\begin{aligned} -3 &= 1 \cdot (-2)^3 + 1 \cdot (-2)^2 + 0 \cdot (-2)^1 \\ &\quad + 1 \cdot (-2)^0 = 1101_{-2} \end{aligned}$$

We see that both positive and negative numbers are accommodated with one and the same representation.

Let us examine now the effect of such a representation on the design of our machine. We start with Eq. (10) which will now be replaced by Eq. (17)⁵.

$$\left. \begin{aligned} a_k &= \sum_{j=0}^{J_a-1} u_{kj}(-2)^j & (u_{kj} = 0,1) \\ x_k &= \sum_{j=0}^{J_x-1} v_{kj}(-2)^j & (v_{kj} = 0,1) \end{aligned} \right\} \quad (17)$$

This in turn leads to the modification of Eqs. (13), (14), and (15) as follows:

$$\sum_{k=0}^{K-1} \sum_{i=0}^{J_a-1} u_{ki} v_{m-k, r-i} = h_r \quad (18)$$

$$y_m = \sum_{r=0}^{J-1} h_r (-2)^r \quad (19)$$

$$y_m = (\cdots (h_{J-1} \cdot (-2) + h_{J-2})(-2) + \cdots + h_1)(-2) + h_0 \quad (20)$$

We conclude that if we remove the constraint (5) and adopt a negative binary representation for ξ_k, α_k , the machine design of Section II is still applicable, provided we modify the sequence of operations in the accumulator, combining the counts so as to realize Eq. (20) rather than Eq. (15).

⁴Author's unpublished manuscript.

⁵ u_{kj} is the j th bit of a_k in radix (-2) . This is different from u'_{kj} which is the j th bit of a_k in radix $(+2)$.

The count h_r is a function of the bits in the negative binary representation of the data and coefficients; h_r itself, however, may be represented in any system. For obvious reasons we adopt a standard (base 2) counter to determine h_r . Therefore, Eq. (20) should be implemented in a standard (base 2) accumulator thus yielding the result y_m in binary.

The modification to realize Eq. (20) is particularly simple if the accumulator is of the magnitude-sign-bit type. In this case, each shift operation will simply be accompanied by a simultaneous sign reversal. This is all it takes to ensure that the negative radix inputs, x_k , are processed to yield positive radix outputs, y_m .

We consider now the implications of the adopted negative radix representation. The a_k 's are usually computed on a general-purpose binary computer. Their negative binary representation can be easily obtained by incorporating in the coefficient program a subroutine converting from positive binary to negative binary representation. A suitable algorithm for this subroutine is described in Ref. 3.

The situation with respect to the data is somewhat different. The basic configuration of Fig. 1 shows the data already in digital form. In most practical situations, the data are available in analog form so that the very first element in the input of a practical machine would have to be an A/D converter. The above discussion then indicates that we ought to interpose a radix converter (Ref. 3) between the A/D converter and the X register. This is a reasonable approach when a standard commercially available A/D converter is to be used.

A more logical approach, however, would combine the negative radix converter with the A/D converter in a single functional unit that would directly convert the analog input to its negative binary representation. The design of such a converter operating in serial fashion is discussed in detail in Ref. 4. Such a device is particularly attractive in that one does not have to wait for the complete conversion of an analog sample. Thus, the first bits of a data word may be in register X and partly processed before its last bits have even been determined.

An overall outline incorporating the modifications introduced in this section is shown in Fig. 3. We have added here a D/A converter as the last link in the processing. The transformation (9) is effected here. Note in this context that the digital word to be converted is available in the accumulator with more bits than the

input x_k 's. Usually, a few of the lower bits will simply be discarded at this point.

Figure 3 serves as the starting point for the more specific designs considered in the following two sections. In preparation for this, we introduce here some necessary terminology.

Let f_b be the rate at which input bits are fed to the machine (bit rate). The corresponding period (bit time) T_b is then

$$T_b = \frac{1}{f_b} \quad (21)$$

From the previous discussion it is obvious that T_b is also the period of the clock pulses controlling the X register shifts. Thus, the entities h_r are produced at the rate f_b and the accumulator shown in Fig. 3 is required to complete a shift-and-add cycle in the interval T_b .

The sampling rate, f_s , of the analog input signal ξ , is related to f_b by

$$f_s = \frac{f_b}{J} \quad (22)$$

or equivalently,

$$T_s = \frac{1}{f_s} = JT_b = (J_x + J_a - 1)T_b \quad (23)$$

Of this, $J_x T_b$ is the time required to feed one data word into the X register, while $(J_a - 1)T_b$ is the time required to feed the associated $(J_a - 1)$ zeros.

Another important parameter is the delay time T_d . Thus, while η'_m is the approximation to the output of a zero delay filter at time mT_s , a practical filter will produce this output at time $(mT_s + T_d)$ where $T_d > 0$.

IV. The Partitioned-Counting Filter

We consider here an elaboration of the master design that achieves high-speed by performing the counting indicated in Fig. 3 in a special way.

Let $N(=KJ_a)$ be the number of gate outputs to be counted and let N satisfy

$$2^{M-1} \leq N < 2^M \quad (24)$$

The total count, h , is therefore bounded by

$$0 \leq h < 2^M \quad (25)$$

and is representable by an M -bit binary number.

If we use a standard M -bit binary counter with clock time T_c , the counting time will be NT_c . Hence

$$T_b = (N + 1)T_c \quad (26)$$

and the result is a low-speed machine. Such a design has its merits and is pursued further in *Section VI*.

Our concern here is with a high-speed design. Realizing that the low speed associated with the above approach is a direct result of the serial nature of the counting, we propose to subdivide the N gates into groups of q gates each and count all these groups in parallel. We refer to this method as partitioned counting. In the following, we examine this approach in detail.

First, we note that in the interest of efficiency, q should satisfy

$$q = 2^r - 1 \quad (r = 2, 3, \dots) \quad (27)$$

so that the count of each group is representable as an r -bit binary number. The method considered here would replace the single M -bit counter with a large number of smaller elementary r -bit counters.

Using the bit terminology of *Section II*, we may say that the initial N gates are a representation of the number h as a sum of N zero-weight bits. Similarly, the binary number representing the final count is a representation of h as a sum of M ($\ll N$) bits whose weights range from zero to $M - 1$. In partitioned counting, the transition from one representation to the other is effected in a large number of small steps. In each such step, the weights are increased while the total number of bits is decreased.

The large number of elementary counters required, means that the investment in hardware is quite high. However, the resulting speed increase is significant. Thus, assuming the same clock time T_c , as before, counting of q gates is accomplished in time qT_c . This, however, does not yield the final count yet. The outputs of these counters will now have to be operated on in a similar fashion (described later in detail). Hence they

should remain undisturbed for another qT_c interval. This means that

$$T_b = 2qT_c \quad (28)$$

It follows that the speed increase over the single counter method is given by the factor $(N + 1)/2q$. For large N and small q ($q_{\min} = 3$), this factor may be quite large.

To obtain the speed improvement while minimizing the amount of hardware, we try to make sure that all r -bit counters are fed $q = 2^r - 1$ inputs. This is most easily facilitated when

$$N = q^v \quad (v \text{ integer}) \quad (29)$$

If N does not satisfy Eq. (29), lower efficiency will usually result, though there are various ways to minimize this effect. To simplify the presentation here, we assume from now on that Eq. (29) is satisfied.

We turn now to the details of the scheme. Consider an r -bit counter, counting q bits of weight k . The result is a sum of r bits ranging in weight from k to $k + r - 1$. The number of bits has thus been reduced, having been multiplied by

$$\beta = \frac{r}{q} = \frac{r}{2^r - 1} < 1 \quad (r \geq 2) \quad (30)$$

Applying q^{v-1} such counters to the $N (= q^v)$ zero-weight bits yields a sum of $\beta N = q^{v-1}r$ bits with weights ranging from 0 to $r - 1$. Now we consider all bits of the same weight as inputs for further counting. $q^{v-2}r$ counters will be required at this level and the result will be a sum of $q^{v-2}r^2$ bits with weights ranging from 0 to $2(r - 1)$.

The pattern emerging from the above description is best illustrated in terms of an array such as that of Fig. 4 which applies for $r = 3$. This is essentially an ordered listing of the number of bits as a function of weight (k) and counting level (n). The numbers for each level have a common multiplier indicated on the left. Thus, the initial situation referred to as level 0 has $q^v \cdot 1$ bits of weight zero. In level 1 (following first count), we have q^{v-1} bits of each of the weights 0, 1, 2 and so on. Factoring out the common level multiplier is particularly convenient since the resulting numbers in the array are quite easy to compute in this case.

Let us assign the symbol B_{nkr} to the array element corresponding to level n , weight k in a partitioned count-

ing scheme using r -bit counters. (Example: $B_{2,1,3} = 2$). The earlier description of the bit transformation effected by a single r -bit counter, implies that the elements of level n are derived from those of level $n - 1$ as follows: Element $B_{n-1,kr}$ contributes a term $B_{n-1,kr}$ to each of the following: $B_{nkr}, B_{n,k+1,r}, \dots, B_{n,k+r-1,r}$. Equivalently,

$$B_{nkr} = \sum_{i=0}^{r-1} B_{n-1,k-i,r} \quad (31)$$

The other obvious properties are

$$B_{0kr} = \delta_{ko} \quad (\delta_{ij} \text{ is Kronecker's } \delta) \quad (32)$$

$$B_{nkr} = 0 \quad \text{for } k < 0 \quad (33)$$

The last equation is a direct result of the fact that we are dealing here with integers so that no bits are assigned negative weights. Equations (31) to (33) form a prescription for the computation of any B_{nkr} .

We note in passing that the array of Fig. 4 is actually a generalized Pascal triangle. The special case $r = 2$ yields the standard Pascal triangle. Similarly, B_{nkr} is a generalized binomial coefficient. Indeed, the above eqns. imply that

$$B_{nkr} \equiv \binom{n}{k}$$

The B_{nkr} parameters prescribed by Eqs. (31) to (33) are involved only in the initial levels of counting. The terminating levels display a different pattern. We illustrate this with a particular example involving $N = 2401 = 7^4$ (that is, $r = 3$, $v = 4$). The corresponding array is shown in Fig. 5. Obviously, the initial levels of Fig. 5 are identical with those of Fig. 4. Up to level 4, the elements are generated in a unique fashion following Eqs. (31) to (33). At this level, the multiplier is 1 so that the elements in row 4 ($n = 4$) directly specify the number of bits for each weight. Note that while the single zero-weight bit has reached its final value, there are still 19 bits of weight 4. Further counting is therefore required, but the organization will now be different. Obviously, nothing more is to be done with the zero-weight single bit. The 4 bits of weight 1 will require one counter thus entailing a somewhat reduced efficiency. On the other hand, one may postpone action relating to the 4 bits of weight 7, arguing that counting of lower weight bits will increase the number of weight 7 bits at the upper levels. Thus, by postponing their count, we increase the overall efficiency. The same argument

applies to the 10 bits of weight 2. Instead of assigning 2 counters to them, we count only 7 of them in one counter, postponing the counting of the remaining 3. Following these reasonable (but not unique) guidelines, we arrive at the numbers shown in levels 5-14.

The numbers on the right margin of the array in Fig. 5 represent the number of elementary counters used between the levels bracketing their position. Thus, 3^3 elementary counters are required to transform the bits of level 3 to the configuration of level 4. The total number of counters is 602 as indicated. The major part of this is contributed by the counters operating below level v . It can be shown that the sum of these is in general $(q^v - r^v)/(q - r)$. For Fig. 5, this value is 580. In comparison, we see from the indicated total that only 22 counters are involved in the terminating levels.

Since the last level has $n = 14$ and transferring from one level to the next takes the time qT_c , the final count of the N gates will be ready for the accumulator after a delay $14qT_c = 98T_c$. Successive counts, however, are separated by the shorter interval T_b . From Eq. (28) we get $T_b = 2qT_c = 14T_c$.

An even faster design is illustrated in Fig. 6 which applies 2-bit elementary counters to the slightly smaller $N = 2187 = 3^7$ (that is, $r = 2$, $v = 7$). Each counter uses fewer components but more counters are needed. The counting delay is given by $20qT_c = 60T_c$, while $T_b = 6T_c$. These figures should be compared to $2187T_c (= NT_c)$ and $2188T_c (= (N + 1)T_c)$ which are the corresponding values for the single, 12-bit counter. The reduction from $2187T_c$ to $60T_c$ is due to the parallel counting of bits comprising a specific count. The further reduction of the spacing to $6T_c$ depends on the fact that at each particular instant during the $60T_c$ required to produce a single count, only a small portion of the elementary counters is needed for that specific count. This permits the initiation of a new count long before the earlier count has been completed. In Fig. 6, 10 distinct h_r 's are being simultaneously counted in a staggered arrangement. This is further illustrated in Fig. 7. Note that during the interval qT_c starting at t_1 , the counting of h_3 is initiated, that is, its bit configuration is transformed from level 0 to level 1. At the same time, the counting of the earlier input, h_4 , (the evaluation sequence prescribed in Section II is $h_r, h_{r-1}, h_{r-2}, \dots$) is further processed by transforming from level 2 to level 3, the still earlier input h_5 is transformed from level 4 to level 5 and so on.

The processing of h_3 is continued in the next interval (t_2, t_3) . Note that the new input, h_2 , is not entered yet in

order to not disturb the bits in level 1 which are being counted during this interval. The input spacing of $2qT_c$ and its implications are evident in Fig. 7.

The simultaneous counting of several h_r 's means that storage has to be provided for those bits of h_r which attain their final value before termination of the count. Consider Fig. 6: The final value of bit 0 of h_r is established at level 7. No further counting involving this bit is required. At this point it resides in a flip-flop of one of the elementary counters. This counter will preserve its information during the next qT_c interval but following that, it will be zeroed and start counting a term of h_{r-1} . Evidently, the quiescent interval has to be used to transfer the h_r bit elsewhere. The simplest solution is to transfer the zero bit to a shift register and step this register at intervals $2qT_c$. With the proper number of cells (7 in this case), this register will output the zero bit of h_r at the time all its other bits are ready. Needless to say, this shift register will serve in the same capacity for the zero bits of h_{r-1} , h_{r-2} and so on. Inspecting Fig. 6 and repeating the above arguments we find that accommodation of the finalized bit 1 requires a 6-bit shift register, bit 2 needs a 5-bit shift register and so on, down to bit 9 calling for a single flip-flop (1-bit shift register).⁶

A. Possible Variations

We turn our attention now to three important variations.

The first variant counts q gates in time T_c (rather than qT_c). The idea is to replace the elementary counters, serially counting q inputs, with elementary adders which add the q inputs on parallel.

For $q = 3$, the well-known "full adder"⁷ (Ref. 5) is just such a device. It has three inputs (a carry and the two bits to be added) and produces two output bits (The sum bit and the new carry bit). These may be regarded as the bits of the output count (the sum is bit zero, the new carry is bit one).

Alternatively, one might consider the q input bits as specifying an address in a ROM organized as 2^q words of r bits each. "Counting" in this case is effected by reading the r -bit word stored in the corresponding address. This should obviously be restricted to low r .

⁶The handling of bits 3, 4, 6, 8 is slightly different, calling for a 1-bit buffer interposed between the finalized counter bit and the shift register.

⁷Plus two latches to store the count.

Actually it can be shown that the combination $r = 2$, $q = 3$ requires the smallest overall number of memory bits. However, for higher r (which might be dictated by availability of off-the-shelf ROMs), Eq. (27) does not prescribe the optimum q .

A second variation is based on the use of buffers to increase speed. If the output of each elementary r -bit counter is transferred to an r -bit buffer rather than feeding directly the next level counters, the bit period should consist of qT_c to count and T_c to transfer the counts (in parallel) to the buffers. Thus, Eq. (28) should now be replaced by

$$T_b = (q + 1) T_c \quad (34)$$

Speed is increased by the factor of $2q/(q + 1)$ at the expense of essentially doubling the number of flip-flops. Therefore, this method should always be compared to the alternative of reducing q . Consider for example the case of Fig. 5 ($q = 7$). With 1806 ($= 602 \cdot r$) flip-flops assigned to the elementary counters, we got $T_b = 14T_c$. Adding buffers, we have 3612 flip-flops yielding $T_b = 8T_c$. This should be compared to Fig. 6 ($q = 3$) which assigns 4364 ($= 2182 \cdot r$) flip-flops to get $T_b = 6T_c$ for a slightly lower N .

Note the disadvantage of a counting delay of $14 \cdot (q + 1)T_c = 112T_c$ for the buffered, $q = 7$, case as compared to $60T_c$ for the unbuffered, $q = 3$, case.

The third variant considered relates to the use of floating point representation for the filter coefficients α_k . Let the ratio of the largest $|\alpha_k|$ to the smallest $|\alpha_k|$ be ρ . If ρ is a large number, then even if we allot only a very small number of bits to the smallest $|\alpha_k|$ we still end up with a large J_a . This hurts us in two ways:

- (a) The sampling rate is reduced (see Eq. 23).
- (b) $N = KJ_a$, the number of gates to be counted is increased, sharply increasing the cost.

We consider here a simple strategy which accepts (a) but provides an answer for (b). To illustrate the strategy, consider the following example: We wish to assign 5 bits to each coefficient but if the lowest $|a_k|$ satisfies that, we find that we need $J_a = 20$ to represent the highest $|a_k|$. We organize registers A, X on the basis of $J_a = 20$ but attach gates and counters only to the 5 most significant bits of each a_k . This is equivalent to the adoption of a floating point representation for the coefficients.

It should be noted that we are considering here a general-purpose machine that should be able to accommodate a wide range of requirements. In view of this, the best way to implement the above strategy is to use a single, sufficiently long, register for the coefficients but effect the connection of its cells to the gates with relays or switches under the control of the machine operator. In addition to loading the coefficients a_k into the machine, the operator will also set the switches.

It has already been mentioned that the coefficients a_k will usually be computed on a general-purpose computer. Assume then that they are punched on a paper tape which is fed into the digital filter. In situations where the additional expense is justified, this paper tape could be made to command the switches and set them directly without the intervention of the operator.

V. The Circulating-Lines Filter, A Low-Speed Low-Cost Approach

In the introduction to *Section IV* we considered briefly a design based on a serial counter. We concluded there that such a machine would be very slow. In the present section we proceed to show that this disadvantage is coupled with the advantage of low cost, which makes such a design quite attractive in some applications.

Consider Fig. 3 and assume that counting is to be done serially. Obviously, there is no need in this case to produce all the gates' outputs simultaneously as shown there. Rather, one could take advantage of the serial nature of the counting and produce the gate outputs serially. This suggests using circulating delay lines or MOS shift registers to replace the X and A registers of Fig. 3^a.

We shall see that the hardware simplification accruing to serial counting extends also to the accumulator appearing in Fig. 3. Thus, it will be shown that a somewhat more complex serial counter eliminates the need for the accumulator altogether. We consider now the various aspects of a serial counting design in some detail.

The basic design of Fig. 3 shows the data words being fed into the X register with the most significant bits leading. This means that the h_r 's are computed in the time sequence $h_{J-1}, h_{J-2}, \dots, h_0$. In the present case, we find it more convenient to feed the least significant bits first, generating the h_r 's in the time sequence $h_0, h_1, \dots$,

h_{J-1} . Since serial A/D converters produce the most significant bit first, this sequencing means that we have to wait for complete conversion of a word prior to using any of its bits. However, as the evolving design is characterized by long delay, the additional delay due to this effect is negligible.

The A/D converter could be either of the type producing the negative binary representation directly (Ref. 4) or a commercial low-speed A/D converter followed by a radix converter. Taking advantage of the adopted bit sequence, a very simple radix converter is feasible (Ref. 3, Sect. IV).

Use of circulating lines for the A, X registers allows one gate to replace the KJ_a gates shown in Fig. 3. It takes one complete revolution of the coefficients line, A, to sweep all coefficients past the single gate and generate h_r . For the next computation (h_{r+1}), the relative alignment of the X and A registers must be changed by one bit position. Also, register X must discard one old bit and admit one new bit. All these objectives are easily attained by applying a widely used "trick," namely, adding an extra cell to the X register and using the flip-flop implementing it, to inject new data bits.

The design is illustrated in Fig. 8a. The extra bit is stored in cell B whose input is controlled by switch S. The indicated state of S refers to its state during the immediately following 1-bit shift. The example shown is the simple one adopted in Eq. (16). Fig. 8a shows the situation following the evaluation of the first term of h_0 of y_m (see Eqs. 18 and 19). As the two registers are swept in step past the single gate, the remaining terms of h_0 are evaluated. During all these operations, switch S remains as shown in Fig. 8a so that any bit shifted out of the gate feeding cell, lands in cell B.

Fig. 8b shows the situation following the evaluation of the last term of h_0 of y_m . Note that switch S now connects to the right. This means that in the next shift, the leftmost bit will be lost, and cell B will be loaded with the new data input bit (bit 2 of word x_m). This new state of affairs is shown in Fig. 8c. Note that switch S has now returned to its left position and we have here the evaluation of the first term of h_1 of y_m .

The time difference between Figs. 8a and 8c corresponds to one full revolution of the coefficients line. Hence, these figures represent the state of affairs that would emerge in "strobing" the lines to "freeze" the motion of the coefficients line. The resulting pattern in

^aSuggested by H. C. Wilck of the Communications Systems Research Section.

the X register (excluding cell B) is a 1-bit shift to the right with a new bit being fed on the left and the oldest bit being ejected on the right. This is almost identical with the basic pattern considered in *Section II*. The only difference is in the shift direction since the order of computing the h_r 's is now the reverse of that of *Section II*.

We are now in position to consider the overall design of the machine as shown in Fig. 9. The right part of this figure is essentially a redrawing of Fig. 8a. Switch S of that figure is replaced here with an implementation using three gates controlled by clock sequences C_1 , C_2 . Sequence C_2 steps the circulating lines, while clock C_1 controls the serial radix converter and hence the rate of feeding new bits.

As we have already seen, counting the TRUE outputs of gate G over the proper time interval, will yield h_r . This counting as well as the assembly of counts to get the output word y_m , is implemented in a modified up-down counter. Unlike the standard up-down counter which accepts inputs into bit 0 only, here we allow inputs to be delivered to the other bits too. This is permissible as long as only one input at a time is activated and the rate of input is sufficiently low so that rippling through of carries resulting from the last bit fed has terminated before a new bit is applied.

The effect of the above modification is that rather than counting (up or down) by ones only, this counter can count by any power of 2. This immediately suggests its application in the construction of the output word y_m according to Eq. (19) which may be rephrased as:

$$y_m = \sum_{r=0}^{J-1} (-1)^r \left\{ \sum_{k=1}^{h_r} 2^r \right\}$$

All we have to do is steer the sequence of bits coming out of gate G to the proper input terminal and properly set the (up/down) mode of counting. Specifically, bits comprising h_0 should be steered to input 0, counting up, bits comprising h_1 should be steered to input 1, counting down and so on.

As long as the counter does not overflow, this automatically yields the correct y_m with negative numbers appearing in their 2's complement representation.⁹ This

⁹A D-bit up-down counter will properly represent any integer N constrained as follows:

$$-2^{D-1} \leq N \leq 2^{D-1} - 1$$

means that the counter output can be fed directly to a D/A converter to produce the analog output.

Steering the output of gate G to the proper counter input is controlled by circulating line D. It has $J(=7)$ cells. One of these is set to one. The rest are set to zero. Being controlled by clock C_1 , line D automatically enables bit r input when the bits comprising h_r are coming out of gate G. Circulating line D also controls the up-down mode in an obvious way using two OR gates.

Transfer of the final output to the digital-to-analog (D/A) converter poses an interesting problem. In principle, this could be done in two count cycles, one for copying out and one for zeroing the counter in preparation for the next word. However, this would entail interruption of the flow of input bits during these two cycles. We prefer to implement the data transfer and initialization without interrupting this flow. This can be achieved by the simple expedient of segregating the counter flip-flops into words L and H as shown in Fig. 9 and transferring the data from these two words at different times. Word L is copied out simultaneously with activating the gate connected to the lowest bit of word H. Zeroing of word L follows in the next count cycle. Word H is copied out immediately after its assembly is complete, that is, simultaneously with the entry (to the counter) of the first bit of the next filter output word. Zeroing of word H follows in the next count cycle.

To understand why this scheme works, note that the counter input gates are activated in a sequence leading from the low-order bits to the high-order bits. This means that by the time any gate connected to word H is activated, the assembly of word L is complete and it may be copied out. Furthermore, in assigning the partitioning into words H, L, we make sure that the lowest bit of H has an odd weight. This means that when the first H gate is accessed, the counter is in a down-counting mode. In this mode a $1 \rightarrow 0$ change in flip-flop i does not affect flip-flop $i+1$. Hence, zeroing of word L has no effect on word H. Similarly, entry of the first two bits of the new word (with gate 0 activated) affects at most bit 1 and thus the copying out and zeroing of word H are not disturbed.

Note that this method would not be applicable in a system where the higher weights are computed first (as in Fig. 3). This is the motivation for the input bit sequence adopted here. The basic characteristics of this design, however, are independent of the input sequence adopted.

We turn now to some operational details. Figure 8 indicates that each filtering task will require a specific number of cells in the circulating lines $[KJ - (J_x - 1)]$ for the coefficients line and $[KJ - (J_x - 2)]$ for the data line. An important feature of a practical implementation would therefore be an array of line segments of various lengths which are to be switched into the circulating lines by the machine operator. The flexibility and possibilities of such an arrangement are quite attractive. Yet, all of this is obtained with a relatively modest investment in hardware.

The major disadvantage is of course the low speed. Let T_g be the period of clock C_2 stepping the circulating lines. In discussing Fig. 8, we saw that a new input bit is fed with each revolution of the coefficients line. Hence,

$$T_b = \{KJ - (J_x - 1)\} T_g \quad (35)$$

and (see Eq. 23)

$$T_s = KJ^2 T_g \left\{ 1 - \frac{J_x - 1}{KJ} \right\} \quad (36)$$

Obviously the penalty for reducing the amount of hardware is quite severe.

We consider now briefly the question of floating point representation for the filter coefficients. When the range of coefficients results in a large J_a , the effect on the speed will be quite pronounced (Eq. 36). However, if the up-down counter is sufficiently large so as not to overflow under these conditions, the only hardware adjustments required are the patching together of sufficiently long circulating lines. Thus, the main argument for floating point representation is speed increase rather than hardware economy.

We give here only a rough outline of a floating point implementation based on approximating a_k by $a'_k(-2)^{e_k}$ in which e_k is a positive integer and a'_k is an integer representable by J_a bits in base (-2) . We store $\{a'_k\}$ in the data line and $\{e_k\}$ in an extra register used to control the access to the counter in such a way that a bit belonging to h_r and generated by a'_k is steered to input $(r + e_k)$. This guarantees the correct result. However, the result-

ing non-monotonic steering raises some difficulties which will not be discussed here.

VI. Concluding Remarks

We have seen that the counting strategy provides the basis for a fast machine. How does such a design compare with one based on Eq. (4)? In comparing the two, coarse estimates of the amount of hardware will suffice. Using r -bit elementary counters to count N gates in groups of q , the total number of counters is $N/(q - r)$.¹⁰ Hence, the fast design using "full-adders" ($q = 3, r = 2$) requires N counters. On the other hand, to attain the same bit rate with serial multipliers applying Eq. (4), we have to use K multipliers operating in parallel and K accumulators¹¹ to sum their outputs. Each of these accumulators must handle at least J_a bits and thus consist of at least J_a "full-adders" and their associated storage elements. Hence, with $N = KJ_a$, the K accumulators alone will use more hardware than the N elementary counters of the counting design. The K multipliers are therefore extra hardware to be weighed against the single fast accumulator of the counting design.

There is no question, therefore, that the counting design is more economical for the fast machine.¹² However, it should be realized that the partitioned counting approach is also applicable to slow designs, since increasing q will drastically reduce both speed and cost. Thus, adopting q as the basic design parameter, machines of widely different characteristics may be built.

All of the designs described here are conceptual entities. None have been practically implemented. They all look promising, each with its own particular balance of performance versus cost. Particularly intriguing in this context are the possibilities opened by large-scale integration. It remains to be seen, however, whether these expectations will actually materialize in a practical implementation.

¹⁰ $(N/q)\{1 + (r/q) + (r/q)^2 + \dots\} = N/(q - r)$

¹¹ $(K/2)\left(1 + \frac{1}{2} + \frac{1}{2^2} + \dots\right) = K$

¹²It is also more precise (1 round-off error insertion versus K such insertions).

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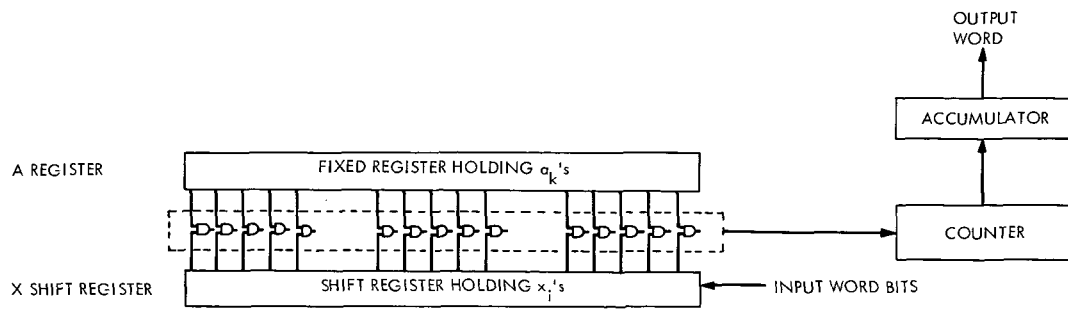


Fig. 1. Preliminary outline of master design

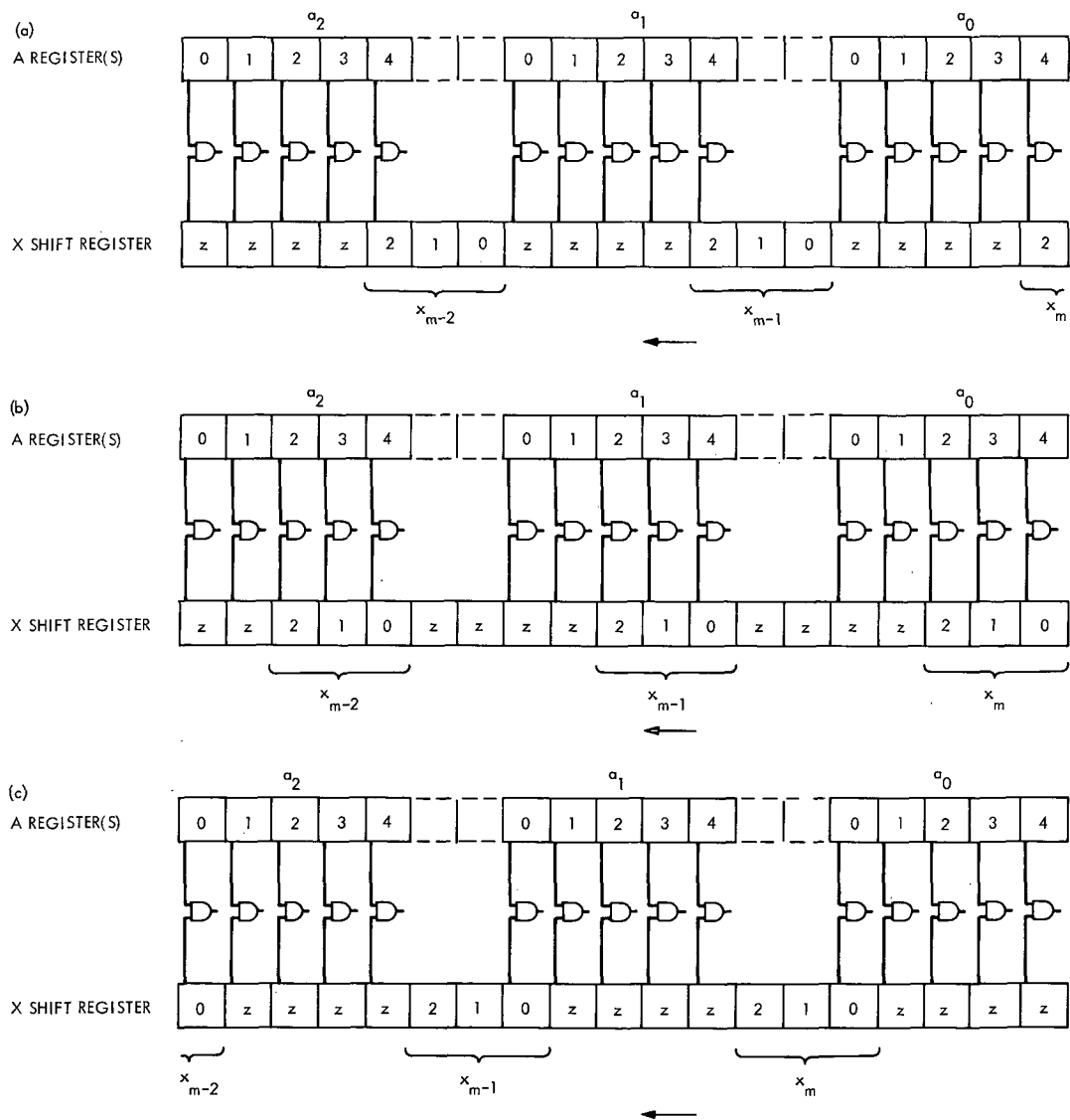


Fig. 2. Bit sequences in registers A, X

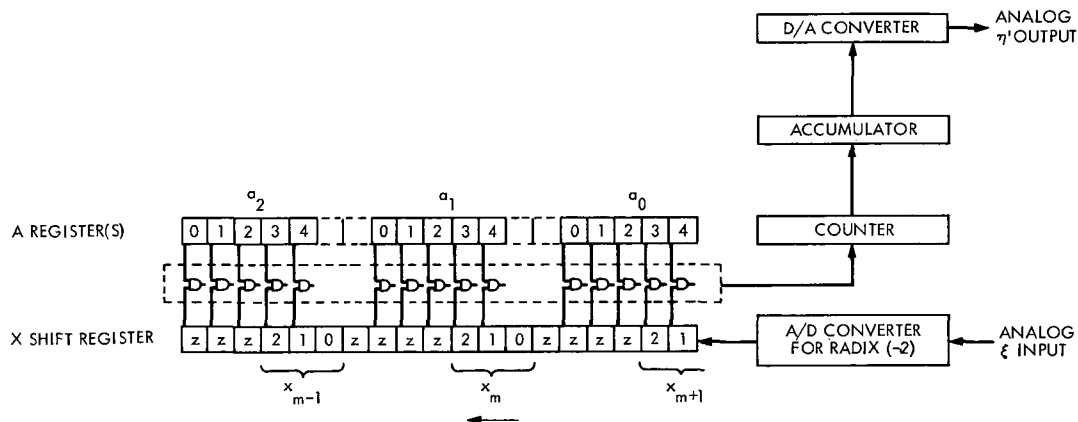


Fig. 3. The master design

MULT	$n \backslash k$	0	1	2	3	4	5	6
q^ν	0	1						
$q^{\nu-1}$	1	1	1	1				
$q^{\nu-2}$	2	1	2	3	2	1		
$q^{\nu-3}$	3	1	3	6	7	6	3	1

Fig. 4. Initial stages of partitioned counting for $r = 3$

MULT	$n \backslash k$	0	1	2	3	4	5	6	7	8	9	10	11	CNTRS
7^4	0	1												7^3
7^3	1	1	1	1										$7^2 \cdot 3$
7^2	2	1	2	3	2	1								$7 \cdot 3^2$
7	3	1	3	6	7	6	3	1						3^3
1	4	1	4	10	16	19	16	10	4	1				9
1	5	1	1	5	6	10	8	8	7	2				5
1	6	1	1	1	7	5	3	4	3	4	1			1
1	7	1	1	1	1	6	4	4	3	4	1			1
1	8	1	1	1	1	1	5	5	3	4	1			1
1	9	1	1	1	1	1	1	6	4	4	1			1
1	10	1	1	1	1	1	1	1	5	5	1			1
1	11	1	1	1	1	1	1	1	1	6	2			1
1	12	1	1	1	1	1	1	1	1	1	3	1		1
1	13	1	1	1	1	1	1	1	1	1	1	2		1
1	14	1	1	1	1	1	1	1	1	1	1	1	1	1

TOTAL 602

Fig. 5. Partitioned counting for $r = 3; \nu = 4$

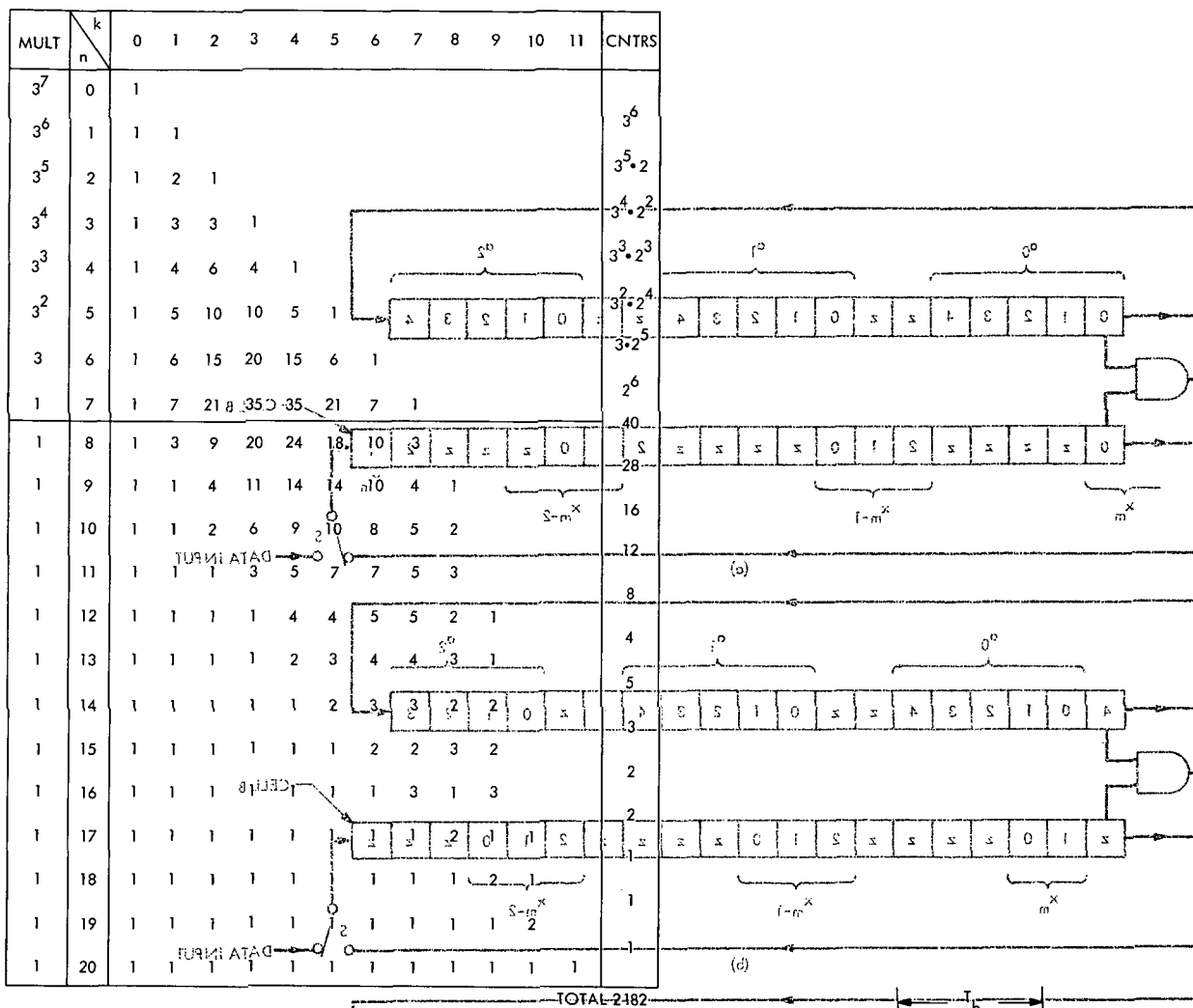


Fig. 6. Partitioned counting for $r = 2$; $v = 7$

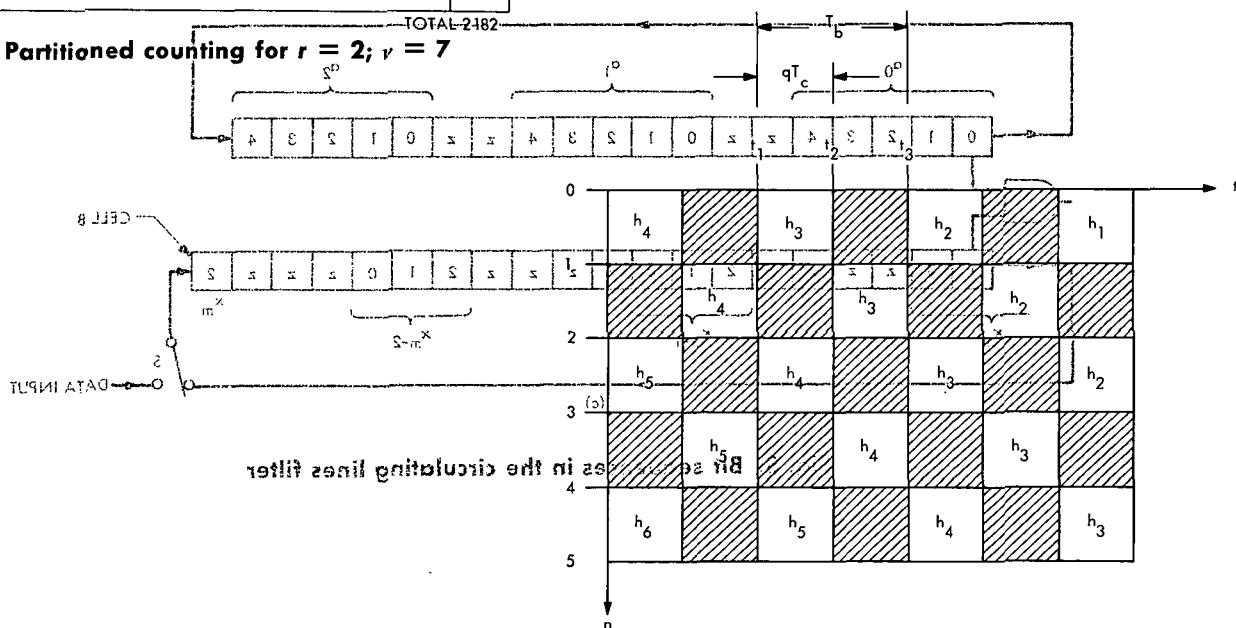


Fig. 7. Time dependence in partitioned counting

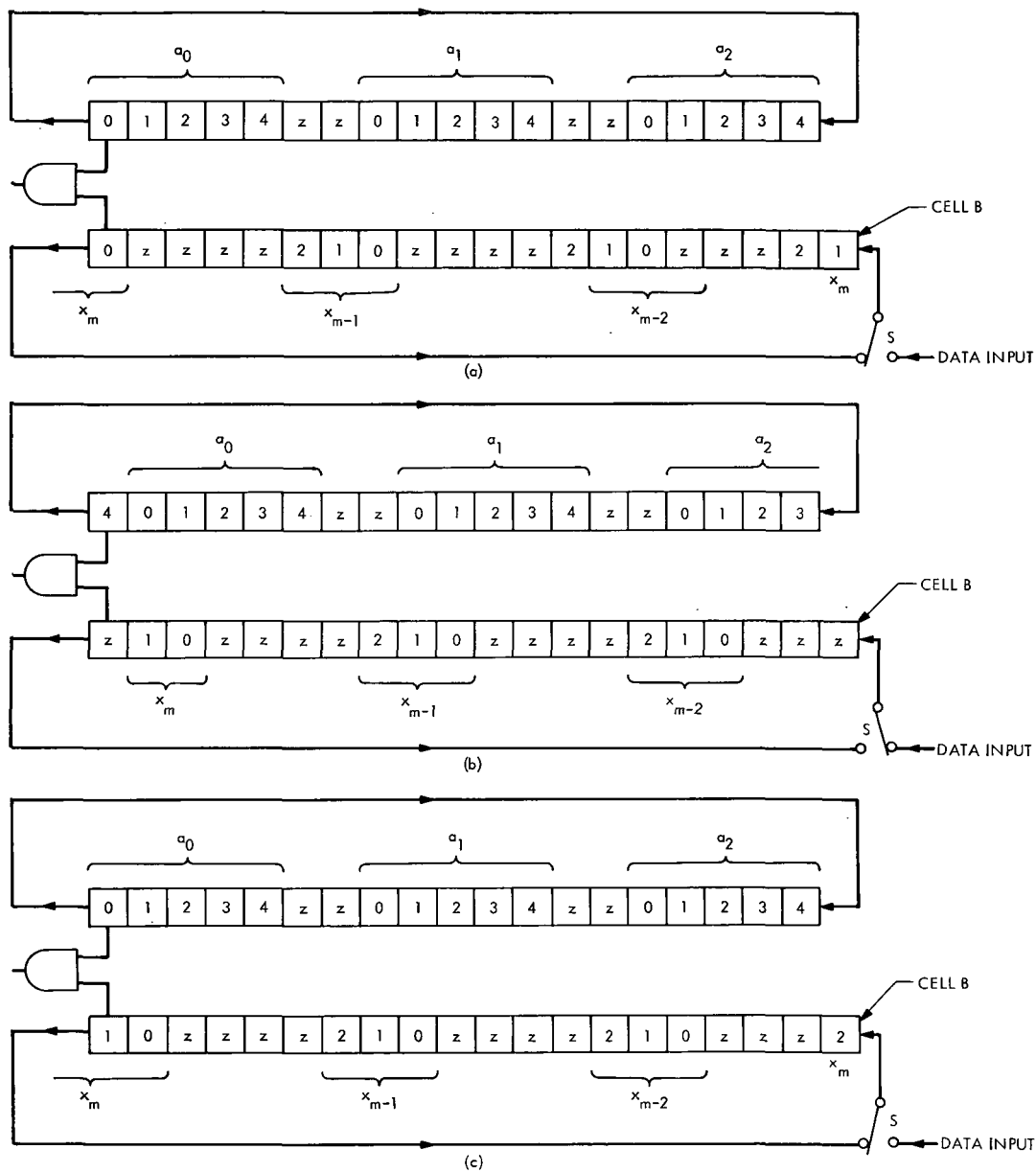


Fig. 8. Bit sequences in the circulating lines filter

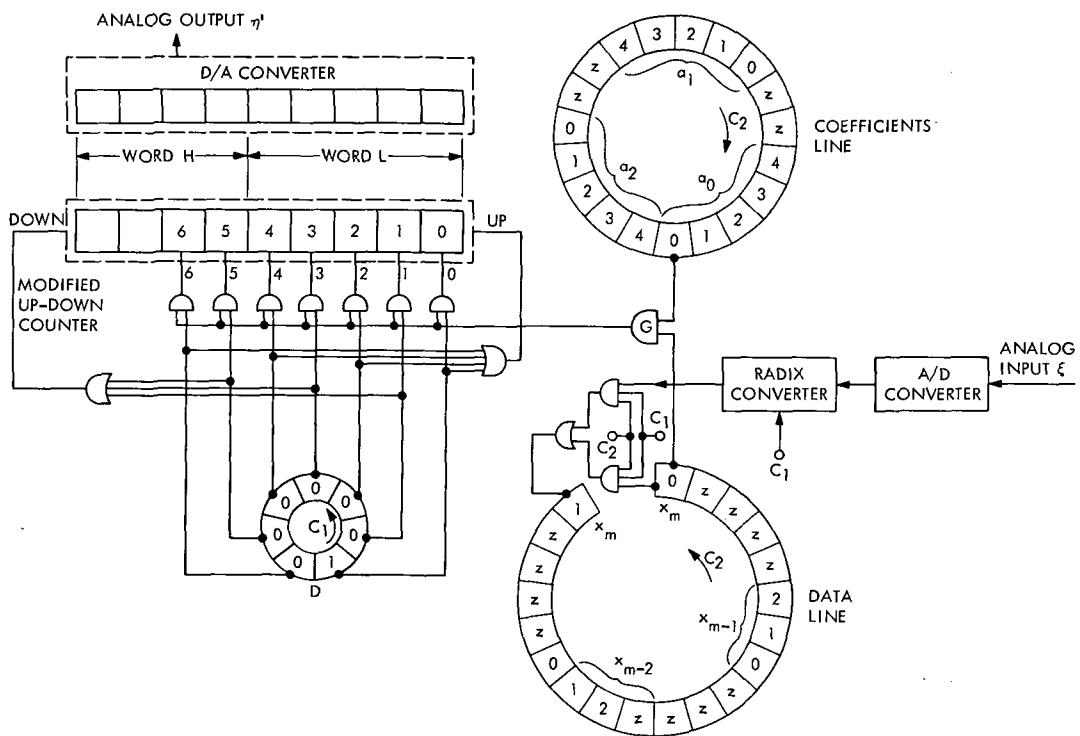


Fig. 9. The circulating lines filter

A Note on Kerdock Codes

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The performance of an important class of low-rate nonlinear binary codes recently discovered by A. M. Kerdock is superior to linear codes with the same parameters. Before these codes can be put to practical use, several questions remain to be answered. This article considers one of the questions and shows that the nonlinear Kerdock codes are systematic; i.e., they have distinguishable information and check positions.

I. Introduction

Recently A. M. Kerdock (Ref. 1) discovered an important class of low-rate *nonlinear* binary codes whose performance is superior to linear codes with the same parameters. However, before these very powerful codes can be used practically, several questions remain to be answered. The question we shall be concerned with is whether or not the codes are *systematic*. A binary code with 2^k codewords is said to be systematic if there exists a fixed set of k positions in the code which can take on any of the 2^k binary k -tuples as values. If this is so, the code has distinguishable information and check positions, a very useful property. (Every linear code is systematic, so this question rarely arises in the literature, most of the well-known codes being linear.) In this article, we shall prove that Kerdock's codes are indeed systematic.

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II. Definition of Kerdock Codes and Proof That They Are Systematic

Let $m = 2l - 1$, α be a primitive root of $GF(2^m)$ and $Tr(\cdot)$ the trace of $GF(2^m)$ over $GF(2)$. Define

$$Q(x) = Tr(x^3 + x^5 + x^9 + \cdots + x^{1+2^{l-1}})$$

For $A, B \in GF(2)$ and $\eta, \gamma \in GF(2^m)$ define two polynomials

$$f_L(x) = Tr(\eta x) + Q(\gamma x) + A$$

$$f_R(x) = Tr(\eta x + \gamma x) + Q(\gamma x) + B$$

Then the vector of length 2^{2l}

$$(A, s_0, s_1, \cdots, s_{2^m-2}; B, t_0, t_1, \cdots, t_{2^m-2}) \quad (1)$$

$$s_i = f_L(\alpha^i), \quad t_i = f_R(\alpha^i), \quad i = 0, 1, \cdots, 2^m - 2$$

is a word in the Kerdock code of length $2^{2'}$. There are two choices for A , two for B , 2^m for η , and 2^m for γ for a total of $2^{2'}$ codewords. Kerdock (Ref. 1) proved that the minimum distance of this code is $2^{2'-1} - 2^{1'-1}$. (The best known $(2^{2'}, 4\ell)$ linear code has only $d = 2^{2'-1} - 2^{1'}$.) We shall prove that the code is systematic by showing that the 4ℓ components $A, s_0, \dots, s_{m-1}, B, t_0, \dots, t_{m-1}$ determine A, B, η , and γ uniquely. We begin with a lemma.

LEMMA. *Let α be a primitive element of $GF(2^m)$. Then for $x \in GF(2^m)$ the m elements $Tr(x\alpha^i)$, $i = 0, 1, \dots, m-1$, of $GF(2)$ determine x uniquely.*

Proof. If the lemma is false, there are elements $x \neq y$ such that $Tr(x\alpha^i) = Tr(y\alpha^i)$ for $i = 0, 1, \dots, m-1$. Then if $z = x - y$, $z \neq 0$, and $Tr(z\alpha^i) = 0$ for $i = 0, 1, \dots, m-1$. Let β be chosen with $Tr(\beta) = 1$. Since

$1, \alpha, \dots, \alpha^{m-1}$ is by hypothesis a basis for $GF(2^m)$ over $GF(2)$, we may write $z^{-1}\beta = w_0 + w_1\alpha + \dots + w_{m-1}\alpha^{m-1}$ for suitable $w_i \in GF(2)$. Then $Tr(\beta) = Tr(z \cdot z^{-1}\beta) = Tr(\sum zw_i\alpha^i) = \sum w_i Tr(z\alpha^i) = 0$, a contradiction.

We can now easily prove our main result.

THEOREM. *The elements A, B, η and γ can be recovered uniquely from the 4ℓ components $A, s_0, \dots, s_{m-1}, B, t_0, \dots, t_{m-1}$ of the codeword Eq. (1).*

Proof. Of course A and B can be read off directly. Now $s_i + t_i + A + B = Tr(\gamma\alpha^i)$ and so by the lemma γ can be recovered. Finally, knowing γ we can calculate $s_i + Q(\gamma\alpha^i) + A = Tr(\eta\alpha^i)$ and so again by the lemma η can be recovered.

Reference

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An Inventory Policy for the Deep Space Network

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This article describes a proposed inventory and procurement policy for optimal procedures for ordering and allocating for the Network Supply Depot (NSD). The policy defined differs from conventional inventory stockage and resupply systems in that it takes into consideration the inventory status not only at NSD but also at each of the Complex Supply Facilities.

I. Basic Features of the Proposed Policy

For each item the Network Supply Depot (NSD) supplies to the Complex Supply Facilities (CSFs), there are three fundamental questions that the policy must answer:

- (1) When should NSD reorder the items?
- (2) How much should be ordered?
- (3) How should the NSD supply be allocated among the CSFs?

(1) Any policy, such as the present system, in which NSD reorders whenever its own inventory reaches a prescribed minimum is wasteful, incurring excessive inventory costs. This is because NSD's inventory may reach its minimum at a time when the levels of inventory on hand at the CSFs are large. An efficient cost-minimizing policy must base reorder decisions upon the state of the entire system, i.e., the levels of inventory

on hand at the CSFs (continuously monitored by the Integrated Logistics System) as well as the NSD level. The proposed policy establishes a safe minimum inventory level for each CSF and requires NSD to reorder whenever one or more CSFs reach the prescribed minimum.

(2) The conventional economic lot size model (Refs. 1 and 2) has been modified to take into account the effects of ordering simultaneously for all CSFs. An equation is set up which expresses for each item the average cost per year incurred in operating the inventory system. The optimal mean time between orders can be calculated, and from this the order size is determined, using estimated mean demand levels for the CSFs.

(3) A mathematical analysis based upon the average cost equation reveals that optimality is achieved by distributing the NSD supply to the CSFs in such a way

as to minimize the average total inventory in the system at reorder time. Since each CSF has at least its prescribed minimum inventory level, this amounts to minimizing on the average the sum of the "excess" inventories (over minimum levels) of the CSFs. The "ideal" situation is one where all the CSFs reach minimum at the same time. However, this ideal is seldom attained because the model assumes the CSF inventories are depleted by orders arriving at random. The next section deals with minimization of excess inventories.

II. Allocation of NSD Supply Among CSFs

It is conceivable that NSD could distribute items to the CSFs one at a time as the CSFs' inventories are depleted, thereby keeping each CSF from accumulating any excess inventory. The time required for shipping and the cost of handling these shipments render such an approach obviously impractical. Two practical approaches are considered. A *no-resupply policy* (NR-policy) and a *one-stage resupply policy* (R-policy) under which NSD distributes a resupply inventory R among the CSFs the first time one of them reaches its minimum.

Under the NR-policy, an optimal allocation for a given order size can be computed by means of an algorithm based only on estimated ratios of mean demand between CSFs. These estimates can be based on demand experienced during previous order cycles. Tables listing these optimal allocations are easily constructed for a variety of demand ratios.

An advantage of the NR-policy is that it permits NSD to process an incoming order and send shipments to the CSFs without maintaining an inventory of its own. However, the excess inventory at reorder time is further reduced by the R-policy, a fact which may justify the cost of additional shipping and handling, particularly for high-cost items. The following example illustrates the comparison of excess inventories between the two policies.

Starting with an initial inventory 142 larger than the sum of the CSF minimum levels, the NR-policy optimum allocation based upon six CSFs with demand ratios 7:8:9:10:11:12 is 19, 21, 23, 25, 26, 28, respectively. The resulting excess inventory averages 34.8. Using the R-policy with $R = 10$, the excess inventory averages 19.5, a reduction of 44%.

III. Setting Minimum Levels

If the demand distribution for a CSF is known, then for each possible value of the minimum stockage level s , one can compute the expected shortage (i.e., demands not satisfied) during the lead period required for resupply. One also computes the average level of inventory resulting from the choice of s . The standard inventory model based upon known demand distribution (Ref. 2) then proceeds by choosing s so as to minimize a performance criterion of the form

$$cs + \mathcal{E}(s) \quad (1)$$

where

$\mathcal{E}(s)$ — expected shortage per lead period

and c depends upon the frequency of lead periods and the relative importance of shortages.

Of course, the true distribution of demand for an individual CSF is not known and must be estimated. A natural approach is first to estimate this distribution and then, using the estimated distribution, choose the optimal s by the standard methods. This approach is unsatisfactory because it fails to weigh the consequences of errors of estimation. To illustrate the nature of the difficulty, let us suppose that the demand is subject to a Poisson distribution with mean demand (per lead period) M , assumed unknown. The usual estimate of M is D/T , where D is the observed demand over a period of time equal to T lead periods. If $M = 10$ and $T = 3$, then the probability that the estimate $D/T = M$ is 0.073, and the probabilities of other values are shown by the heights of the bars in Fig. 1. To each value of D there corresponds a value of $s = s(D/T)$ (chosen optimally for mean demand D/T). As a consequence of using $s(D/T)$ rather than $s(M)$ (the optimal s -value for the true mean demand, M), one incurs a change in expected shortage,

$$E = \mathcal{E}\left(s\left(\frac{D}{T}\right)\right) - \mathcal{E}(s(M)),$$

and a (possible) savings in the inventory term in expression (1),

$$I = c \cdot \left(s(M) - s\left(\frac{D}{T}\right) \right),$$

which are plotted in Fig. 1 for $c = 0.02$. The term *regret* will be used to refer to

$$E - I = \left[c \cdot s\left(\frac{D}{T}\right) + \mathcal{E}\left(s\left(\frac{D}{T}\right)\right) \right] - [c \cdot s(M) + \mathcal{E}(s(M))]$$

which is the increase in expression (1) resulting from using $s = s(D/T)$ rather than the $s = s(M)$ (recall that since M is the actual mean demand, $s = s(M)$ minimizes expression (1)). The effect of errors of estimation (deviations of D/T from M) are apparent from Fig. 1. While the regret increases as D/T moves away from M in either direction, note that the regret rises much more sharply for D/T less than M , i.e., underestimating M is much more costly than overestimating M . The explanation of this profound asymmetry is that the term $c \cdot s$ grows linearly with s , while $\mathcal{E}(s)$ is nonlinear, being very small for s comfortably larger than M (when the probability of incurring any shortage is small), but rising steeply as s decreases to M and below (where the expected shortage is roughly $M - s$).

Obviously, what would be desirable is a procedure for setting s (based on D and T) that minimizes the average regret. The problem is complicated because the average regret of a given procedure depends on the true M and no procedure minimizes it for all M . Appli-

cation of statistical decision theory leads to a class of readily computable procedures which have certain optimal properties. Selection of procedures within this class is greatly facilitated by a specially developed computer program which evaluates and plots average regret as a function of M . One can thus select a procedure whose performance is reasonably good for a broad range of values of M and is particularly strong for M in a smaller range where the mean demand is thought to lie. Preliminary investigations have led to some useful formulas for choosing s .

Several refinements of this basic approach have already been made and incorporated into the general policy and associated computer programs. One of these concerns the modifications required to deal with items which are dispensed by a CSF in different quantities, e.g., one or two items, a dozen, or two dozen. Another concerns the problem of sporadic demand. Any procedure for setting s based on observed demand over time T may encounter, particularly if T is small, the difficulty that only small-size orders were observed during time T but large orders may occur occasionally. This calls for a substantially larger s to keep the expected shortage under control. A flexible and efficient way of setting s in such cases has been developed, and its performance studied using the computer evaluation program referred to above.

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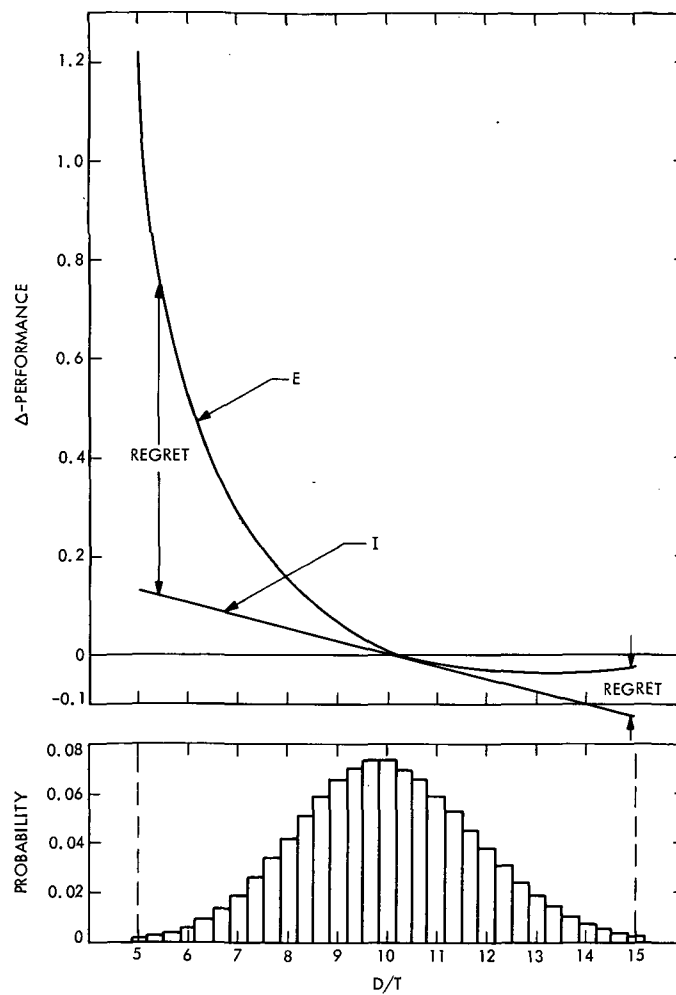


Fig. 1. Effect of the error in estimating demand

Performance of an Optimum Buffer Management Strategy for Sequential Decoding

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Sequential decoding has been found to be an efficient means of communicating at low undetected error rates from deep space probes, but a failure mechanism known as erasure or computational overflow remains a significant problem. The erasure of a block occurs when the decoder has not finished decoding that block at the time that it must be output.

A recent article developed a technique for scheduling the operations of a sequential decoder which has the potential for significant reduction in erasure probability relative to a decoder with the same parameters and using the conventional method of scheduling. Performance results reported previously depend upon the accuracy of an accepted model for the number of computations needed to decode a block of data. This article presents a reevaluation of decoder performance using actual sequential decoding data. Results are generally unchanged: a decoder with a 10-block buffer will achieve less than a 10^{-4} erasure probability with the new scheduling technique whenever a similar decoder had achieved less than a 10^{-2} erasure probability in conventional operation.

I. Introduction

A recent article (Ref. 1) described the characteristics of a buffer memory management strategy for sequential decoding which is capable of significantly reducing erasure probability for fixed values of speed advantage, buffer size, etc. Both the analytic work and the simulation results presented there relied upon a hypothesized theoretical distribution for the number of decoder computations needed to decode a fixed-length block of data. Subsequent work, described herein, has focused upon

the behavior of the memory management algorithm with real data from a sequential decoder, and in determining the distribution of per-block computations for sequential decoding. Although the hypothesized distribution of decoding is not, in fact, completely correct, the results obtained previously for sequential decoding with feedback queuing memory management (FBQM) are essentially unchanged; i.e., for a decoder with a speed advantage of 10 and buffer size of 10 blocks operating with an erasure probability of 10^{-2} , use of the FBQM technique reduces the erasure probability to less than 10^{-4} .

II. The Distribution of Computations-per-Block for Sequential Decoding

It is well established that the number of computations c performed by a sequential decoder in incrementing by one the number of bits for which a local estimate has been made has a Pareto distribution, i.e.,

$$Pr\{c > N\} \sim k N^{-\alpha} \quad (1)$$

The exponent α is a positive increasing function of the bit signal-to-noise ratio E_b/N_0 . The constant k has been estimated by Heller (Ref. 2, p. 41) to be 1.9.

The distribution of the number of computations C_L required to decode a block of length L has not been extensively studied, owing in large part to the amount of time required to decode enough blocks to obtain a statistically accurate estimate of this parameter. Since it is C_L which determines the performance of a decoder using FBQM, the performance evaluation of FBQM, and accurately determining the distribution of C_L are essentially the same problem. Previous work on determining the distribution of C_L has established that it is lower bounded by a linear function of L (Refs. 3 and 4); i.e.,

$$Pr\{C_L > N\} \gtrsim k L N^{-\alpha} \quad (2)$$

The parameters k and α are as before. Additional arguments have tended to show that Eq. (2) is both a lower bound and a reasonable approximation to the distribution of C_L . The simulations to be presented here, performed with block lengths of 256 and 1024 bits, show that the best first-order approximation to the distribution of C_L is instead

$$Pr\{C_L > N\} \sim k(N/L)^{-\alpha} \quad (3)$$

The parameters k and α are as before. A more accurate approximation with a wide range of applicability was used in the FBQM simulations, discussed in Section IV. This approximation is shown in the solid lines in Fig. 1.

The dotted lines in Fig. 1 represent an experimental distribution of computation-per-block for the decoding of blocks of length 1024 bits. Each line resulted from approximately 15 h of decoding on a Sigma 5, using a program which emulates the operations of the high-speed multi-mission sequential decoder (Ref. 5). The software simulation was used because of the existence of instrumentation within it to measure the desired parameter. Sample-sizes range from 3×10^2 blocks at the

lowest signal-to-noise ratios (SNRs) up to 10^4 blocks at the highest. The list of the number of computations required to decode each block in the sample set was sorted to define the experimental distribution function. The dots appearing in Fig. 1 correspond to samples from this list spaced approximately uniformly in the computation variable.

At low signal-to-noise ratio, the experimental distribution is closely approximated by the simple Pareto distribution of Eq. (3) with $k \approx 3$ and α as defined from theory. This approximation is poor at high signal-to-noise ratios where the distribution exhibits two distinct behavior patterns dependent upon the range of the computation variable being considered. At relatively large values the distribution is roughly Paretian, as in Eq. (3), with approximately the correct exponent, but with a very small value of k . At small values of the computation variable, if the distribution is assumed to be Paretian, the apparent exponent is much higher than the per-bit computation exponent. This seeming anomaly can be explained on the basis of the following model for per-block computation. (A similar model was used in Ref. 4.) Let us divide the block into a number of sub-blocks, each one of which is entered and exited on the correct path, and suppose that the distribution of computations for each sub-block is given by Eq. (3), with L replaced by L_s , the sub-block length. Both the exponent α and the lengths of the sub-blocks L_s depend on the signal-to-noise ratio. Each sub-block is terminated by a sequence of bits for which no searching is required; for which the initial best-bit estimate is correct; and which is never changed by back-tracking. As such, they represent independent regions of decoding computation. The number of computations needed to decode a block is thus the sum of several independent variables: the number of computations needed to decode each of the component sub-blocks. At low signal-to-noise ratios, the sub-block length L_s is large—so large, in fact, that there is only one sub-block in the complete block, and the computation distribution for the entire block is well approximated by Eq. (3). At higher signal-to-noise ratios, the sub-block length decreases, so that several sub-blocks exist within a block of 1024 bits. When a number of independent Pareto random variables are added, large values of the sum occur most likely as a result of one large component value. Contrarily, small values would arise as sums of small values on each of the sub-blocks. The result is that for small values of the computation variable, the distribution falls off rapidly; more in the manner of a gaussian distribution than Pareto, as indeed the true distribution does.

If the model just proposed is valid, the distribution of computation for other block lengths will differ in a specific fashion from the distribution in Fig. 1. For shorter block lengths, the SNR above which the two-part distribution exists is higher than the SNR threshold for the same effect with 1024 bit blocks, because the typical sub-block length must be less than the block length for the averaging of shorter computations to take place. This appears to have happened in Fig. 2, which shows the experimental computation distribution for a block length of 256 bits. The averaging effect has only begun to be apparent at $E_b/N_0 = +3.5$ dB with the shorter block length, whereas the appearance is at about 2.25 dB with 1024 bits/block.

The solid lines in Fig. 1 represent a constructive approximately least-square error fit to the experimental distributions on the same figure. Since the primary purpose in determining an analytical formulation for the distribution was to generate pseudo-random variables with that distribution, the function fitted determines the computation variable from the probability value, rather than vice versa. The computation variable is segmented into two parts, $C_L = C_1 + C_2$. Each part, C_i , has a distribution given by

$$Pr\{C_i > N_0\} = 1/(1 + k_i(R)(N/L)^{\alpha_i(R)}) \quad (4)$$

The values, $k_i(R)$ and $\alpha_i(R)$, are slowly varying functions of the bit SNR, R (in dB), and L is the block length = 1024. The C_i are treated as if completely dependent random variables, so that determining either determines the other, and hence their sum. The constants have been computed so that, in general, C_1 fits well to the computation distribution for large values of the computation variable; C_2 fits the distribution for small values; and their sum fits quite well over the entire range. The parameter values which resulted from a computer-aided search are

$$\left. \begin{aligned} k_1 &= 0.1069 + 0.7651 \cdot \exp [2.98 \cdot (E_s/N_0)] \\ \alpha_1 &= 1.327 + 0.583 \cdot (E_s/N_0) \\ k_2 &= 1.07 \cdot 10^{-6} + 2.84 \cdot 10^{-6} \cdot \exp [3.776 \cdot (E_s/N_0)] \\ \alpha_2 &= 13.1 + 6.67 \cdot (E_s/N_0) \end{aligned} \right\} \quad (5)$$

for the 1024 bit blocks. No attempt has been made to fit a similar distribution to the experimental data for the 256 bit blocks. The intent here was not to exhaustively study the computation behavior of sequential decoding, but to assist in the evaluation of the performance of sequential decoding with FBQM.

III. Decoding With a Magic Genie

Two hypothetical magic genie-aided decoders were analyzed in Ref. 1. Before proceeding further, we will present revised versions of those analyses using as a basis the first-order approximation to the computation distribution in Eq. (3). Both decoders are able to perform μ computations during the time one bit is being received and have an infinitely large buffer to hold data waiting to be decoded.

The magic genie which aids the first decoder is benevolent and informs the decoder before starting decoding each block whether it should or should not decode that block in order to minimize the fraction of blocks erased. That is, the genie identifies to the decoder those blocks for which the total computation requirement is above a threshold, T_0 . On the average, the number of computations available to decode each block is $\mu * L$ while the number actually expended is

$$\int_0^{T_0} N dP(N)$$

where $P(N) = Pr\{C_L > N\}$. Since the number of computations expended cannot exceed the supply, and the decoder is doing as well as possible, T_0 is the largest value for which the following relation holds.

$$\int_0^{T_0} N dP(N) \leq \mu * L \quad (6)$$

The parameter of interest is $P(T_0)$, the fraction of blocks erased by this decoder. Using Eq. (3) for $P(N)$, we find

$$\left. \begin{aligned} p(T_0) &= \exp(-\mu/k) & \alpha &= 1 \\ P(T_0) &= \left[1 + \mu k^{-\frac{1}{\alpha}} \left(\frac{1-\alpha}{\alpha} \right) \right]^{-\frac{\alpha}{1-\alpha}} & \alpha &\neq 1 \end{aligned} \right\} \quad (7)$$

For $\alpha > 1$, $P(T_0)$ can be made zero by making μ sufficiently large.

The magic genie which aids the second decoder is whimsical and only informs the decoder that it should erase a block after it has expended as much computational work toward decoding an erased block as in decoding the most difficult block which does get decoded. In this case all blocks requiring more than T_1 units of computation are erased after having received T_1 units. Using the requirements that computation ex-

pended cannot exceed the supply, T_1 is the largest value for which the following inequality holds.

$$T_1 P(T_1) + \int_0^{T_1} N dP(N) \leq \mu^* L \quad (8)$$

The erasure probability is $P(T_1)$.

$$\left. \begin{aligned} P(T_1) &= \exp[-\{(\mu/k) - 1\}] & \alpha &= 1 \\ P(T_1) &= [\mu k^{-1/\alpha}(1 - \alpha) + \alpha]^{-\alpha/(1-\alpha)} & \alpha &\neq 1 \end{aligned} \right\} \quad (9)$$

For $\alpha > 1$, $P(T_1)$ can be made arbitrarily small by making μ sufficiently large.

IV. Simulated Performance of a Practical Decoder

A practical decoder which performs similarly to the hypothetical decoder aided by the whimsical genie can be developed by treating the problem of allocating the decoder's efforts as time-sharing processor allocation problem (Ref. 6). We observe that for a Pareto distribution of computation, the block which is most likely to be completely decoded by applying to it Δc computations is that block which has received the least amount of computation among all of those undecoded blocks in the buffer.

Decoder operation is as follows: The decoder begins decoding on each block immediately after it is received. If it is not completely decoded by the time the next block becomes available, it is labeled as having received $\mu^* L$ computations and is stored in the buffer. If decoding is completed before the next block is available, the block in storage which has received the least amount of computation is brought out and decoding performed upon it until either the next new block is available, or until this block too has been decoded. A flow-chart of this process was given in Ref. 1, Fig. 1.

This memory management scheme was recently simulated in two ways using the decoding data set discussed in Section II. Initially, this data was fed directly into the memory management model with various values for speed advantage and buffer size. Since the sample-sizes obtained from the decoder simulations were too small to adequately mask the "end-effects" due to the starting and stopping of the memory management process, another sequence of simulations were performed using pseudo-random data generated to conform to the distribution families described by Eq. (4) and (5). The result of this latter simulation is the family of performance

curves in Fig. 3. At all values of speed advantage considered, FBQM provides a considerable improvement over the linear buffer strategy at erasure rates of 10^{-2} and below.

The curves in Fig. 4 represent a comparison between performance data obtained using pseudo-random data with the distribution of Eqs. (4) and (5), and using the actual sequential decoding data. The solid lines represent 10^5 blocks of pseudo-random data at $E_b/N_0 = 3.0$ dB. The circles represent approximately 5×10^3 blocks of simulated sequential decoder data at $E_b/N_0 = 3.0$ dB. Most of the difference can be explained on the basis of the small sample size: Either buffer management scheme is capable of abandoning a buffer-full (in this case 10 blocks) of data when the simulation is abruptly terminated, and the FBQM process has a relatively high probability of doing so. A partial verification of this assertion can be found in the triangular marks in Fig. 4 which represent the result of treating the 5×10^3 actual decoding samples as a finite population from which 10^5 samples are drawn with replacement. Even with this device for extending the apparent sample size, the tails of the distribution are only represented as well as is done by the smaller sample size. However, if the fitted distribution function has been built correctly, the tails should be accurately represented at any sample size, and hence the performance curves of Fig. 3 more accurately reflect the performance to be achieved in practice than performance curves derived directly from the samples of the sequential decoder computation variable.

Another view of the performance difference between the FBQM process and linear buffer management can be gained by considering the SNR required for a decoder with a given speed advantage to achieve some fixed erasure rate, e.g., 5×10^{-3} or 5×10^{-4} . This is shown in Fig. 5. A performance advantage in excess of 0.5 dB is evident for a wide range of speed advantage.

V. Time-Sequence Un-Scrambling

It should be apparent from the behavior of the FBQM algorithm that it possesses one drawback which could seriously detract from its usefulness. That is, that decoded blocks do not emanate from the decoder in strict time-sequence but are reordered and delayed an amount which depends upon the difficulty encountered in decoding. If the data is spacecraft video, the reordering should pose little difficulty, as it would be a relatively small increment to the already extensive picture processing. Other potential users might well be deterred by the

reordering, so it is worthwhile to consider a combination FBQM decoder and unscrambler which emits decoded data blocks in the same order as the corresponding undecoded data is received.

Suppose a decoder has been implemented using FBQM which performs with essentially zero erasure probability, and suppose that the output of this machine is the input to a buffering machine capable of holding N blocks of decoded data. An erasure occurs in this combination whenever the buffer is filled with blocks $m, m+1, \dots, m+k$, and block $m-1$ has not yet been output from the decoder. Let us assume that the decoder and unscrambler buffers were empty when block $m-1$ was received, and that blocks $m, m+1, \dots, m+N-1$ required negligible effort to decode. Under these circumstances, the probability that block $m-1$ is erased is the probability that the number of computations needed to decode block $m-1$ exceeds $N^*\mu^*L$, the number of computations that can be performed while blocks $m, m+1, \dots, m+N-1$ are being received. This is, in effect, a lower bound on the probability that block $m-1$ is erased. Using Eq. (3):

$$P_a^u \leq k(N^*\mu)^{-\alpha} \quad (10)$$

Suppose instead of the FBQM decoder/unscrambler combination we substitute a decoder with linear buffer management which has the same number of bits of storage as the unscrambler had. If the code rate is $1/\nu$ and the received symbols are quantized to 3-bits each, that memory is now able to store $N/(3^*\nu)$ blocks of data. Assuming that this buffer is empty when block $m-1$ is received, the probability of erasing it is the probability that it requires more than $N^*\mu^*L/(3^*\nu)$ computations.

$$P_a^l \leq k(N^*\mu/(3^*\nu))^{-\alpha} \quad (11)$$

The assumptions in both cases are approximately equivalent: both saying that long computations are isolated events.

It remains to estimate or eliminate the buffer in the FBQM decoder itself. If it is negligible, the FBQM decoder/unscrambler pair will be equivalent to a normal sequential decoder with $3^*\nu$ times as much memory! We can, in fact, force a dynamic trade-off between storage utilized by the FBQM decoder and storage utilized by the unscrambler, by fixing their total size in bits, and

erasing the oldest block or blocks whenever needed storage for an incoming block is not available. The memory, e.g., would be capable of holding 10 blocks of raw partially decoded data, or 70 blocks of fully decoded data, or any integer solution in between. This is a relatively simple modification to the FBQM algorithm, requiring the addition of an information chain which identifies the age of each block in storage, and the storage of decoded data from completely decoded blocks until the undecoded blocks which are older are either decoded or erased. This modified FBQM algorithm has been simulated using pseudo-random data for several SNR values. The results for $E_b/N_0 = 3.0$ dB are shown in Fig. 6 where they are compared to the full FBQM and to a linearly buffered decoder. With the rate $1/2$ code simulated, the FBQM/unscrambler combination is equivalent to a linearly managed decoder with approximately a threefold increase in buffer-size at higher values of μ . Since a sixfold increase is conceptually possible, a different algorithm could perhaps be found for decoder scheduling which would show significant improvement over the FBQM/unscrambler combination, and still satisfy the time-sequence constraint.

VI. Summary

This article has presented the results of a sequence of simulations intended to evaluate the performance of a sequential decoder employing the FBQM memory management algorithm. A model for the number of computations required to decode a fixed-length block of data was also developed to aid in the evaluation. Performance curves for the FBQM decoder have been presented which show that significant performance improvements are possible: i.e., reduction by 0.5 dB in the value of E_b/N_0 required to achieve an erasure rate of 10^{-3} or a reduction in erasure rate of from 10^{-2} to 10^{-4} by the addition of the feedback queuing memory management strategy, with all other decoding parameters held constant.

A brief discussion was also presented of the problems associated with the reordering into strict time-sequence of the FBQM decoder output data. It was shown that even if this unscrambler must share memory with the FBQM decoder itself, a performance improvement equivalent to a better than threefold increase in buffer size is possible, relative to a strictly linear-management decoder.

For JPL's Deep Space Network, however, a preferable solution would seem to be a FBQM decoder in the DSSs cascaded with a separate unscrambler in the net-

work control center. The data rate out of the FBQM decoder is as low as can be achieved—the true data rate from the spacecraft, and for a fixed dollar outlay, a con-

siderably larger descrambler buffer could be acquired for the central facility than could be deployed at each of the affected DSSs.

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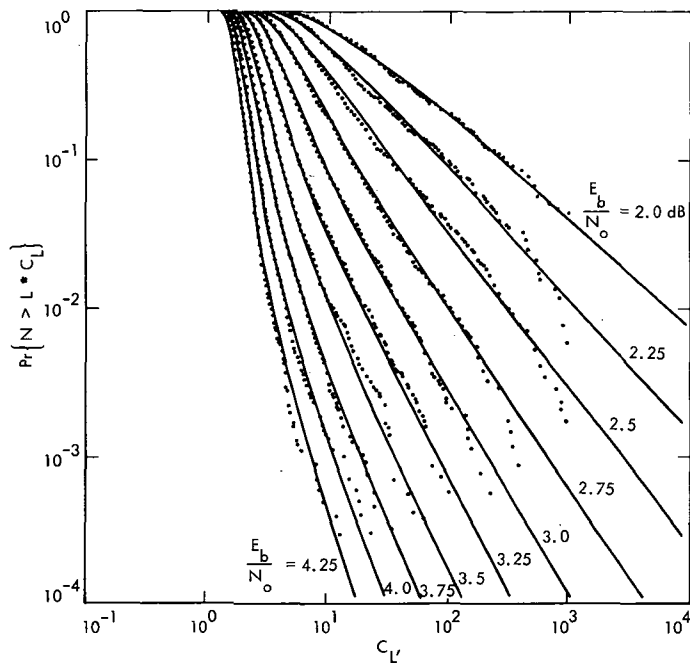


Fig. 1. Distribution of per-block computation with 1024 bits/block

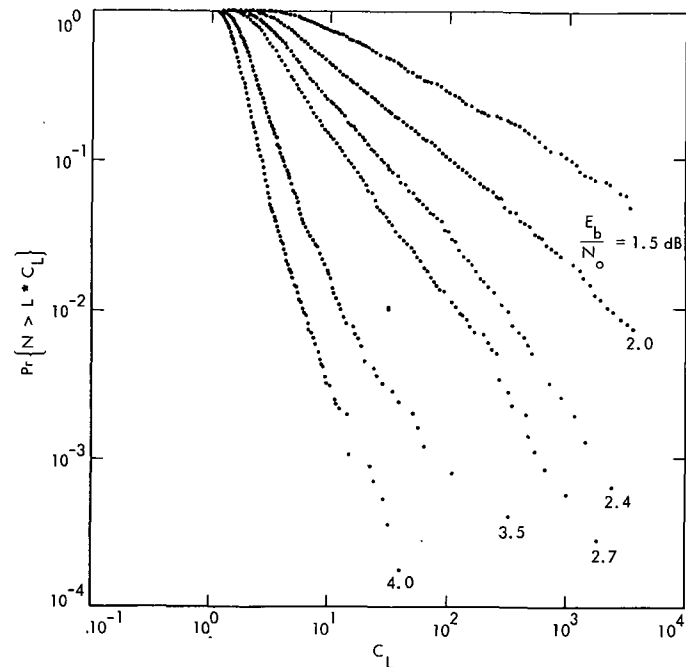


Fig. 2. Distribution of per-block computation with 256 bits/block

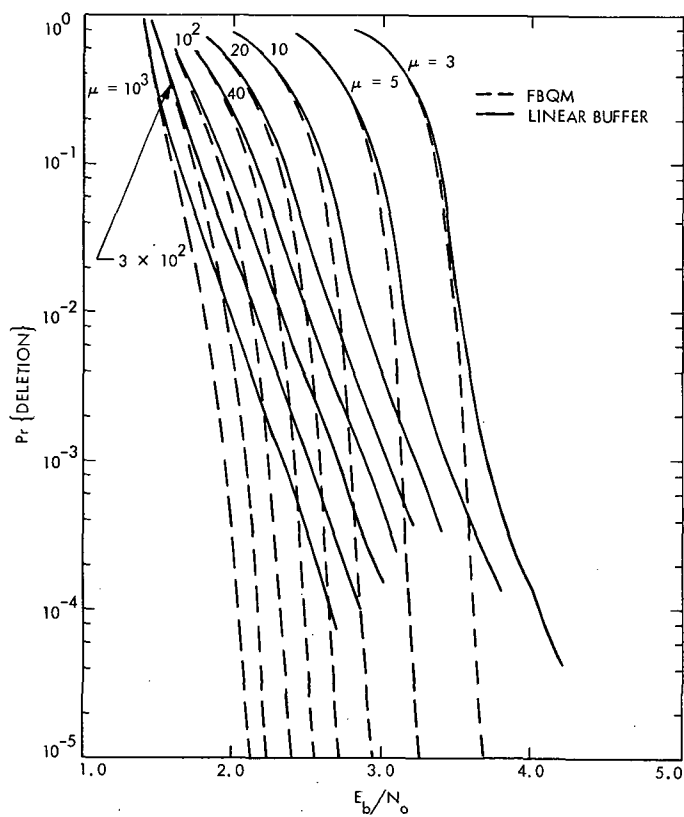


Fig. 3. Comparison of erasure performance for sequential decoding with FBQM and linear buffer management

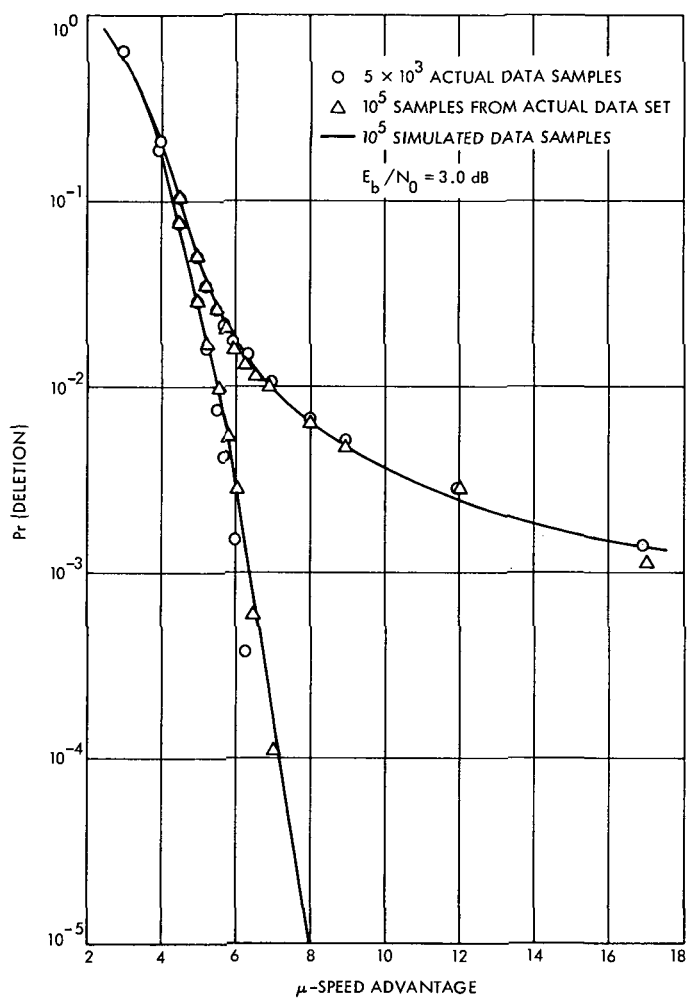


Fig. 4. Comparison between simulation and actual data

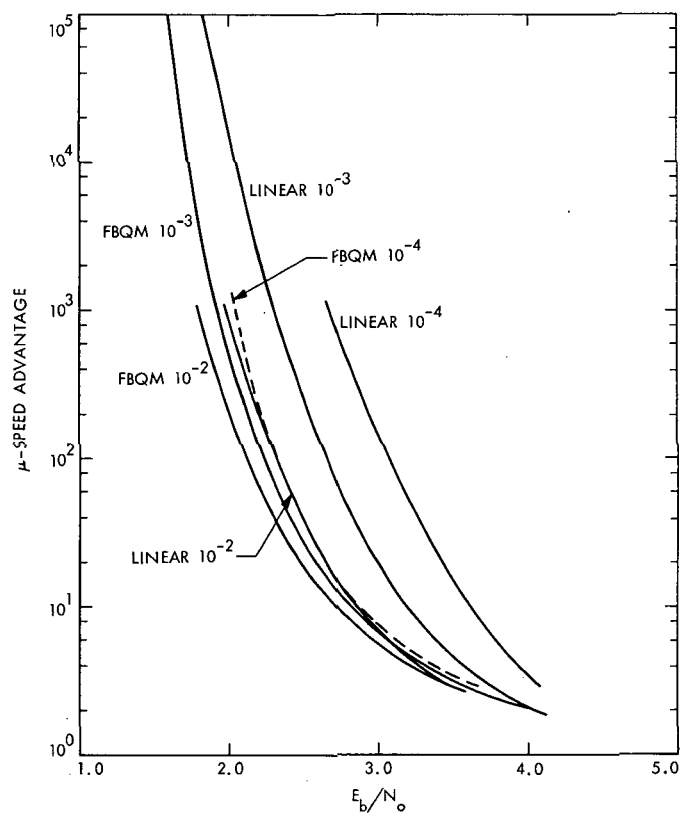


Fig. 5. Signal-to-noise ratio required to achieve desired erasure probability for varying decoder speed

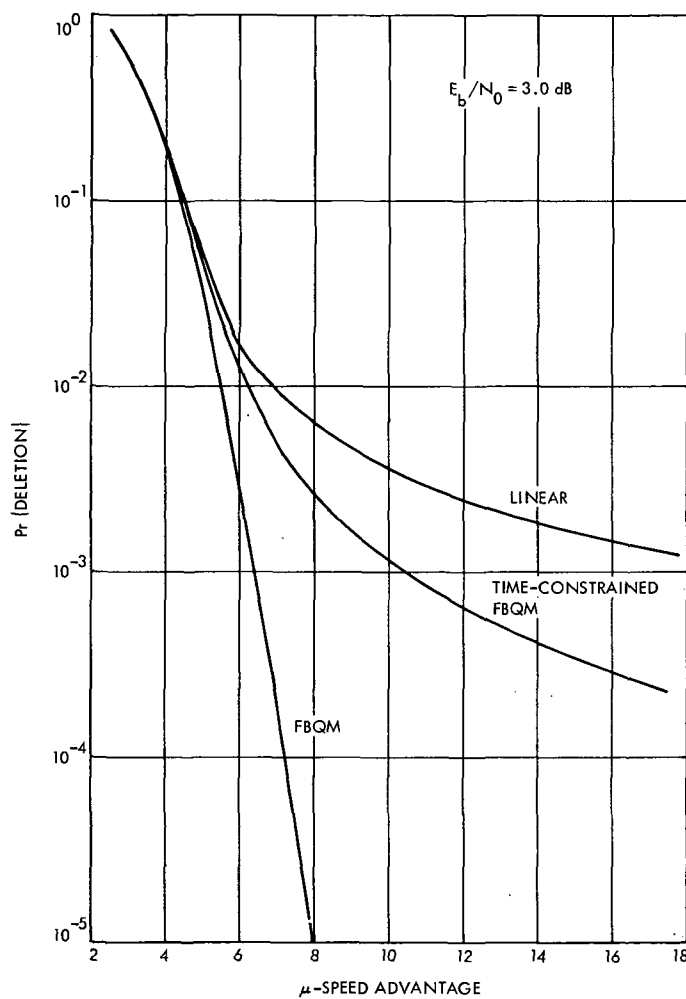


Fig. 6. Performance of FBQM as modified to observe a time-ordering constraint on emitted data

Variable Length Short Constraint-Length Convolutional Codes: A Comparison of Maximum Likelihood and Sequential Decoding

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Maximum likelihood decoding of short constraint-length convolutional codes is one of the likely candidates for implementing high-performance telemetry systems for future deep-space missions. It has, in fact, been considered to be the best choice for video missions, providing better performance at the design point of 5×10^{-3} than other systems of comparable complexity. Recent advances in knowledge of sequential decoding have posed the question as to whether sequential decoding might, in fact, be preferable to maximum likelihood decoding. The answer, developed here in terms of a hypothesized maximum likelihood decoder built technologically similar to the JPL high-speed multi-mission sequential decoder, is that maximum likelihood decoding is preferable to sequential decoding at a 5×10^{-3} bit error rate. The reverse is true at 10^{-3} and below.

Two code families of variable constraint length are also developed which permit easy implementation of encoders for this hypothesized maximum-likelihood decoder.

I. Introduction

Maximum-likelihood decoding of short constraint-length convolutional codes is one of the likely candidates for implementing high performance telemetry systems for future deep-space missions. Proposed designs have variously ranged over constraint-lengths from five to eight. Almost always the proposed decoder is capable of decoding the longest code at the highest anticipated bit rate. A number of future missions will involve more than one planetary encounter with a significantly lower maximum data rate capability at the second encounter than at the first. The

question arises in this circumstance whether it might be desirable to consider a coding system for which moderate coding gain is achieved at the highest bit rate, but with significantly better performance at lower data rates. This article proposes characteristics for such a decoder, presents codes which might be used with it, and compares its performance with that of a sequential decoder built using the same technology.

By way of example, consider a possible mission to Jupiter, Uranus, and Neptune at the end of this decade,

having a maximum data rate of 10^6 bits/s at Jupiter. The proposed decoder would operate at constraint length $K=5$ for the Jupiter encounter. The usable constraint length would increase to $K=8$ at Uranus and $K=10$ at Neptune. At 5×10^{-3} BER, this increase in constraint length is comparable to an increase of 0.85 dB in bit signal-to-noise ratio at the Neptune encounter.

II. The Proposed Decoder

Most decoders for short constraint-length convolutional codes built or proposed to date are of one of two types; either a fully parallel multiple processor device capable of very high-speed operation (Ref. 1), or a single processor device using a somewhat larger constraint length code, having a fast enough semiconductor memory to permit operation at the desired constraint length and data rate. Suppose instead of asking for the fastest technically feasible memory, the designer of the single-processor decoder had asked for the fastest mass-produced complete memory system. Today, the answer to such an inquiry would be a core memory system with approximately a $1\text{-}\mu\text{s}$ cycle time. A decoder implemented with this memory would operate perhaps one fifth as fast as a decoder with high-speed semi-conductor memory. In exchange for this decrease in speed, the designer would have obtained the use of a mature and very reliable memory technology; technology where he could easily obtain memory of the size needed to decode codes of constraint length 12 or longer; technology where the difficulty of testing and maintaining the memory is a very slowly increasing function of the memory size. He could almost ignore memory size as a constraining factor in determining the longest constraint length that his decoder would decode.

Choosing the slower core memory would naturally reduce the upper limit of data rates which could be decoded. It would also reduce the constraint length of the code which could be decoded at the highest data rate designed. However, depending upon mission parameters, the bigger but slower core could increase the usable constraint length, and hence increase the coding gain at the lower data rates occurring later in the mission where the coding gain may be more needed. Let us examine the decoder's behavior. The convolutional encoder at constraint-length k can assume 2^{k-1} possible "states." For each encoder state, the decoder must record a likelihood and a most-likely data path leading to that state. Data for the possible encoder states are accessed two-at-a-time for decoding computations, and data can be arranged so that the pairs of states can be simultaneously accessed from separate memory units. Thus, 2^{k-2} computations are required to decode

one bit of a constraint length- k code. Using TTL logic, the decoder computations could be easily performed within the memory cycle in which the needed data is fetched. The hypothetical decoder is thus able to decode one bit of a constraint length k code in $2^{k-2} \mu\text{s}$.

To see what this means in terms of code performance, examine the curves shown in Fig. 1 where the SNR needed to achieve a fixed design-goal bit error probability is plotted with respect to data rate, assuming that the decoder is operating at as long a constraint length as possible for each data rate. The performance-intercepts for the various codes were obtained from previously published simulation results (Ref. 2). Performance-intercepts for several other existing or proposed coding systems are included for comparison.

III. Variable Constraint-Length Codes

The codes displayed in Fig. 1 are in all cases the best-known codes at each constraint length. They do not in any sense form a family with common characteristics, so implementation on a spacecraft would require almost a complete encoder for each constraint length. Codes which form a nested family could, however, be implemented with little more logic than a single encoder of the longest constraint length involved.

The rate 1/2 quick-look code devised by Massey (Ref. 3) is a code of this type. It was defined for a constraint length $k=48$ bits, but can be truncated to $k < 48$ by the addition of coder taps at depth k to both generators and the deletion of all taps beyond k . Very slight modifications to Massey's algorithm are needed to produce a rate 1/3 quick-look code. At $k=32$, the tap matrix of the resultant code is

$$7630 \ 7777 \ 0000 \ 7707 \ 0700 \ 7700 \ 0077 \ 0777 \quad (1)$$

In Eq. (1), 7s represent taps at that depth on all generators, the 6 represents taps on the first and second generators at delay one, and the 3 represents taps on the second and third generator at delay two. This code is quick-look in the sense that it allows two independent estimates of each bit, each one of which requires only one mod-2 operation. The direct inverse for this code has the lowest possible error probability of any nonsystematic rate 1/3 code. The code can be truncated to any depth k , by insertion of a 7 there, and setting all entries beyond k to 0. This code has been simulated in the vicinity of 5×10^{-3} bit error rate at various constraint lengths. The results are plotted in Fig. 2.

Another family of nested codes has been hand constructed with the aid of the hill-climbing code construction software (Ref. 2). We observe, first of all, that the best $k=4$ code is nested within the best $k=5$ code. Starting at that $k=5$ code, a $k=6$ code was constructed by inserting a 0 into the tap matrix at depth 5, a 7 at depth 6, and asking the hill-climb software to insert taps—hopefully at depth 5. The process then proceeded to $k=7$, $k=8$, etc., and involved frequent back tracking, and compromise between performance at different constraint lengths. At $k=11$, the tap matrix of the resultant code is

$$75651234357 \quad (2)$$

The result was a satisfying rather than optimizing one, and could doubtless be improved; but even so, the family of codes performs very close to the non-nested set of "best" codes in the vicinity of 5×10^{-3} error rate. The results of simulating several members of this code family are shown in Fig. 3. In that region, the codes which were compromised to improve others appear to be no worse than 0.1 dB below the best codes (Ref. 2, Fig. 27), while the best members of the nested code family are essentially equal in performance to the overall best code of the same length.

Fig. 4 shows the E_b/N_0 required to achieve a 5×10^{-3} bit error probability as a function of data rate for the three sets of rate 1/3 codes discussed here using the decoder with 1- μ s computation time. The quick-look codes perform significantly poorer than the other two types, and could reasonably be dropped from consideration for short constraint-length application. The nested non-quick-look codes appear to be a good choice if a corresponding spacecraft encoder is to be implemented at several constraint lengths.

IV. Comparison to Sequential Decoding

The performance variation over the (varying constraint-length) set of convolutional codes is analogous to the performance variation of a sequential decoder with decreasing data rate and increasing speed advantage. Recent work¹ has related the performance of an optimally buffered sequential decoder to the decoding unit speed only, and has dispelled the illusion that arbitrary increases in buffer size can produce arbitrary improvement. A hardware sequential decoder exists at JPL which can perform a decoding computation in 1 μ s (Ref. 4). This decoder was

constructed from approximately the same technology as the decoder for short constraint length codes proposed in Section II.

Let us hypothesize, for comparison purposes, a sequential decoding machine using optimum buffer management and capable of performing one computation in 1 μ s. The amount of logic necessary to implement this decoder is judged by this writer to be approximately equal to the logic required to implement the decoder of Section II. Assuming that this is true, the comparison between the two types of codes is directly meaningful. The speed of either decoder could, doubtless, be pushed upward by factors of 2 to 4 by clever design, at some increase in cost, and, perhaps, flexibility. The 1- μ s figure for both represents a straight-forward design of unarguable feasibility. At the very least, comparison with that figure provides a reference point from which more detailed studies could start, if needed.

The proper comparison point corresponds to an error probability for the optimum decoder of P_E , and a deletion probability for the sequential decoder of approximately $2 * P_E$, since on the average, between $\frac{1}{4}$ and $\frac{1}{2}$ of the bits in a deleted block will be in error. The graphical comparison in Fig. 5 is at 5×10^{-3} and 5×10^{-4} bit error probability. Data for these curves was extracted from Fig. 1, and from Fig. 5 in "Performance of an Optimum Buffer Management Strategy for Sequential Decoding," by J. W. Layland, in this issue. At the higher failure rate, the short constraint-length codes and decoder appear preferable, unless the customer for the data wishes to use the fact that nondeleted blocks from the sequential decoder have an error probability of 10^{-6} or less. At the lower error probability, the sequential decoder performs better, owing, of course, to the greater steepness of the sequential decoding deletion probability versus signal-to-noise ratio (SNR) curves.

Note that the preferences just observed do not change if either of the decoders is sped up small amounts by clever design!

V. Summary

This article has developed a hypothesized convolutional decoder capable of optimum decoding of "short" constraint length codes of perhaps length 12 or more; has developed a workable nested family of codes such that an encoder for all constraint lengths from $K=4$ to $K=K_m$ is little more complex than an encoder for $K=K_m$ alone; and has compared the performance of this hypothesized

¹See "Performance of an Optimum Buffer Management Strategy for Sequential Decoding," by J. W. Layland in this issue.

decoder with a sequential decoder built with comparable technology. The presented curves show clearly that if the design failure probability is 10^{-3} or less, the sequential decoder is somewhat superior, whereas with the 5×10^{-3}

error rate at which conventional deep-space video missions operate, the softer threshold of the short-constraint length codes means superior performance with the decoder described here.

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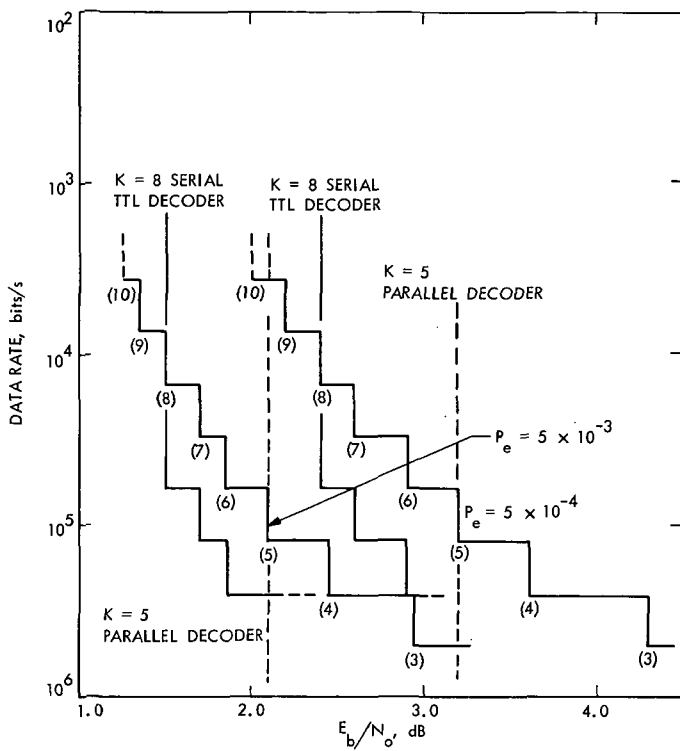


Fig. 1. Signal-to-noise ratio required to achieve desired error probability versus data rate for hypothesized decoder

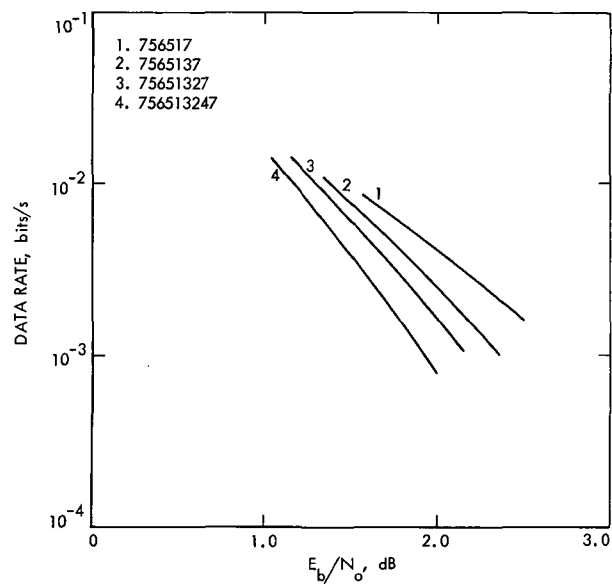


Fig. 3. Performance of a nested family of rate $1/3$ convolutional codes

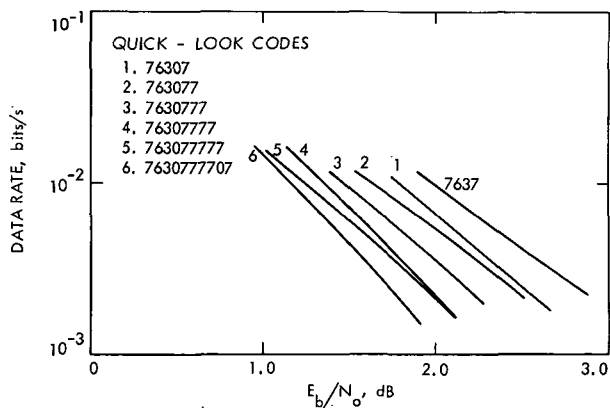


Fig. 2. Performance of a quick-look rate $1/3$ convolutional code at various constraint lengths

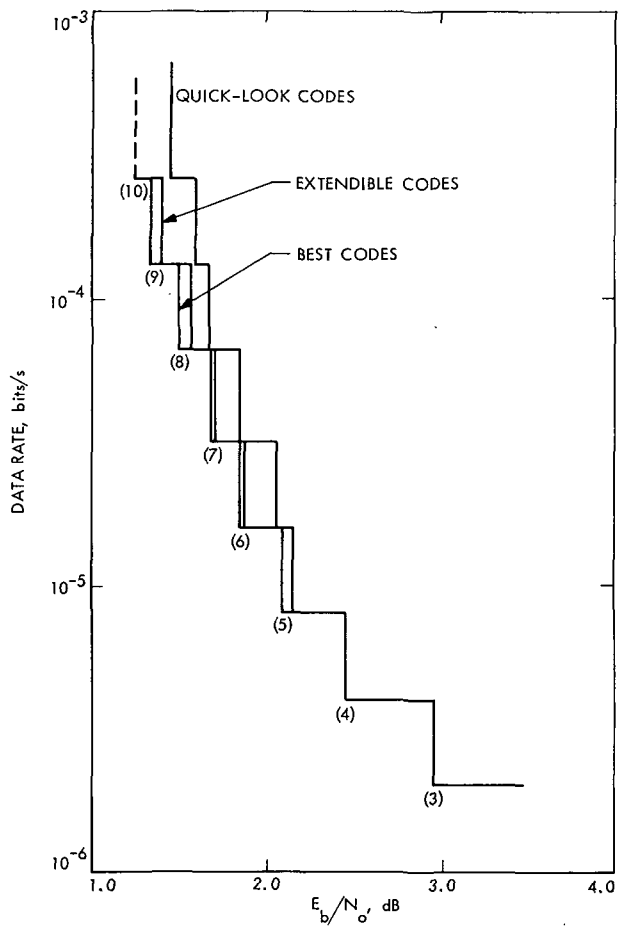


Fig. 4. Signal-to-noise ratio required to achieve 5×10^{-3} bit error probability versus data rate for different codes

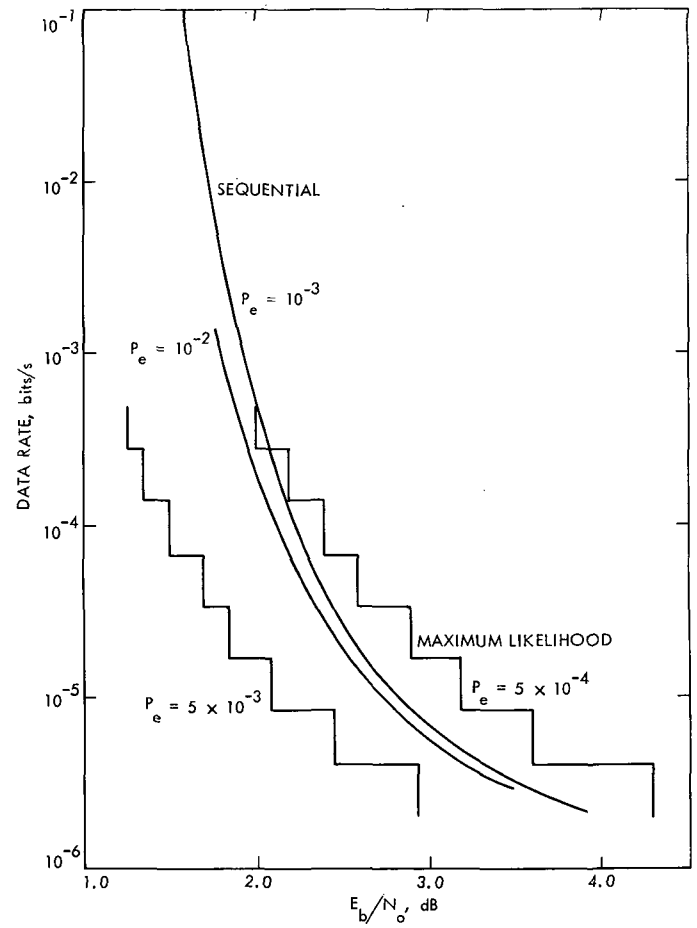


Fig. 5. Comparison of sequential and maximum-likelihood decoding

The Development of a Dual-In-Line Package Microcircuit Card and Card Cage Assembly

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An improved Dual-In-Line Package Microcircuit Card and Card Cage Assembly have been developed. The external dimensions and the basic configuration of a previously developed card have been essentially maintained. However, the number of microcircuit socket locations has been increased from 106 to 126 by compressing dimensions, and the number of interface plug connections has been raised from 82 to 240 by using a new high-density connector. Also the physical size of the filtering capacitors has been reduced by selecting a miniaturized version. All wire-wrap terminals have been placed on 2.5-mm (0.100-in.) centers, with the exception of the capacitor terminals, to allow the card to be wired on an automated wire-wrap machine for potential savings of time, effort, and cost.

I. Introduction

This article discusses the development of an improved Dual-In-Line Package Card and Card Cage Assembly for use in DSN digital systems. A microcircuit card and associated cage assembly had previously been designed and developed; however, both units possessed certain inherent limitations which restricted their use for specific digital subsystem applications. The purpose of this article is to describe the manner in which this card and cage were re-designed to accept the imposed restraints.

II. The Dual-In-Line Package Microcircuit Card

The Dual-In-Line Package (DIP) Microcircuit Card is a high-density packaging panel designed to accommodate a wiring process referred to as automated wire-

wrapping. It is a universal card of modular construction which provides flexibility in integrated microcircuit packaging and prototyping. The card is designed to accept either 14- or 16-lead plug-in integrated microcircuits. The front and rear views of the card are illustrated in Figs. 1 and 2, respectively.

The card is composed of the following basic material and hardware: (1) a copper clad epoxy glass laminate, (2) wire-wrap socket terminals, (3) interconnect plugs with guide pins, (4) insertion/withdrawal pressure levers, and (5) spring pins. The characteristics of these parts along with their functional applications will be discussed.

The primary board material is a flame retardant composite which consists of a laminate base of continuous-filament-type glass fabric impregnated with an impig-

mented epoxy resin binder in the form of a sheet. The sheet is over-laid and bonded with copper on both sides. The technical designation for the composite is FR-4 glass epoxy NEMA grade-type FL-GE 125 C2/2 AIIB per MIL-P-13949. The material covering the copper is an Electro Tin Plate of 0.005-mm (0.0002-in.) minimum thickness per MIL-T-10727.

The tin-plated copper surfaces on either side of the card form the power distribution and ground planes which connect to each DIP pattern. On the ground plane, centered within each pattern, is a unique numbering system which is silk screened in black epoxy ink. Ground is typically provided at socket terminal No. 7 for both 14- and 16-lead DIPs. Socket No. 16 only supplies power for a 16-lead microcircuit; however, power may be provided to a 14-lead DIP by jumping terminal 16 to 14. The character configuration may be observed in Fig. 2.

There are 126 DIP patterns located on the 34.8 cm (13.70 in.) wide $\times$ 14 cm (5.50 in.) high $\times$ 3.17 mm (0.125 in.) thick microcircuit card. Each pattern contains 16 wide-angle tapered entry socket terminals (P/N LSG-1FG-1) manufactured by Augat Inc. in Massachusetts. This device, which extends through and anchors into the board, performs two functions. It serves as a socket on the component side and a wire-wrap terminal on the opposite side. The body (or "sleeve") of the socket terminal is retained in the laminate by means of a "barbed" design shown in Fig. 3. Tests have indicated that this "barb" will maintain its locking function when a maximum force of 5.4 kg (12 pounds) is applied. If there should be a requirement to replace the socket terminal, because of contact or terminal damage, it may be removed simply by means of a special extraction tool (P/N 8136-23G1) made by Augat. It is advisable to insert the new one by using a swaging tool designed to accommodate the form of the sleeve. Note that the removal and insertion processes do no significant damage to the board material. The socket terminal sleeve is made of hard F.C. yellow brass per QQ-B-626 which is gold-plated over nickel per MIL-G-45204. The wire-wrap terminal portion is 13 mm (0.510 in.) long and 0.63 mm $\pm$ 0.08 mm (0.025 in. $\pm$ 0.003 in.) square with 0.08 mm (0.003 in.) maximum radii on corners. A wide tapered entry has been designed into the socket portion for ease of DIP lead insertion. The socket contact is a 4-fingered closed-entry device made of beryllium copper per QQ-C-530, heat-treated to maximum tensile strength. The contact finish is gold-plated per MIL-G-45204, 0.001 mm

(0.00004 in.) thick over stress-free nickel 0.002 mm (0.00008 in.) thick per QQ-N-29. The socket is designed to accept a DIP lead diameter of from 0.41 mm (0.016 in.) to 0.48 mm (0.019 in.). To avoid potential contact damage, it is advised that the diagonal measurement of the DIP lead should not exceed 0.48 mm (0.019 in.).

Augat Inc. has performed extensive life testing of the socket terminal contact. Their main concern was to develop a contact that would maintain its prescribed retention force after one or more pin insertions. To measure the insertion and withdrawal forces in grams, Augat used a Hunter Spring Gauge Model No. 1-10000M. A selected number of socket contacts were probed 5000 times, first with a 0.41-mm (0.016-in.) and second with a 0.48-mm (0.019-in.) diameter round head test probe attached to the gauge. The results of the tests indicate that the contact pressure does decrease slightly with probing, but that the contact establishes a set relatively early in the probing cycle. In the first experiment, the average insertion force was 88 grams and withdrawal was 61 grams. Using the 0.48-mm (0.019-in.) probe, the average insertion registered 650 grams and the withdrawal force 260 grams. The requirement established was for insertion and withdrawal forces to be no less than 50 grams. Due to improved control of their manufacturing process, Augat exceeded our requirement by a wide margin.

There are a total of 2368 wire-wrap terminals on the back side of the board. With the exception of 96, which are designated for capacitors, all terminals are spaced on 2.5-mm (0.100-in.) centers to accommodate automatic wire-wrapping. To insure that the terminal hole positions are held within the required $\pm$ 0.06-mm ($\pm$ 0.002-in.) tolerance, an automatic tape-controlled drilling machine should be employed. All board tolerances must be held tightly because of the critical nature of the automatic wire-wrapping process.

Two high-density right-angle connectors, secured to the bottom of the board, provide a potential of 240 interconnect contacts. The connector is manufactured by Viking Industries (part number 000240-0003). The plug is composed of 3 rows of 40-blade contacts with 2.5-mm (0.100-in.) centers to accommodate automatic rows. Dialyl Phthalate per MIL-P-19833, Type GD1-30, constitutes the insulation material. The contact material is phosphor bronze per MIL-QQ-8-750, which is gold-over-nickel-plated. The contacts bend on a 90-deg angle within the connector body and protrude on the side as

wire-wrap terminals. The current-carrying capacity of each contact is limited to 3 amperes. Because of close tolerance mating problems, a precision guide pin assembly was fabricated which fits into holes provided on each side of the connector body. To prevent misalignment damage, these pins assist in guiding the plug contacts directly into their receptacle contacts. It might be noteworthy to mention that after extensive research into the connector field, it was found that this was the only high-density, right-angle, wire-wrap connector that could meet our specific stringent requirements.

There are two insertion/withdrawal pressure levers mounted at the top on each side of the card. This unique device is shown in Fig. 2. The lever is fabricated from 3.17-mm (0.125-in.) stainless steel for strength and rigidity. Through the lever is mounted a 19-mm (0.750-in.) long spring pin, which is used both as a handle and a board locking device. The lever serves a three-fold function. It inserts the card plug into its receptacle, locks the card in, and releases the card from the mating grip of the connectors. The lever was designed to produce the force required to insert and release the card with a very moderate amount of finger pressure. A spring pin is mounted in the board as a stop to prevent the lever from possibly shorting the wiring terminals. This unique type of hardware was selected because it has the capability of retaining a tight fit when subjected to external pressures.

There are 48 socket locations provided on the card for the installation of filtering capacitors. These locations, constituting the topmost and bottommost rows of sockets, are patterned to accommodate capacitors with either 5-mm (0.200-in.) or 8-mm (0.300-in.) spaced leads. Because of limited packing density, it was imperative that a capacitor of miniature size be selected. A study and survey of the miniature capacitor market was accomplished, which yielded the monolithic-type CY30 produced by the U.S. Capacitor Corp. It is basically a radial lead, epoxy-coated, ceramic capacitor with a rated value of $1.0 \mu\text{F}$ at 50 Vdc. The physical size is $8 \times 8 \times 3.8$ mm ($0.300 \times 0.300 \times 0.150$ in.) with a lead center spacing of 5 mm (0.200 in.). The lead diameter is 0.5 mm (0.020 in.), which allows the capacitor to be held firmly in its socket.

III. The DIP Microcircuit Card Cage Assembly

The DIP Microcircuit Card Cage is basically an angled-metal structure which serves as a facility for mounting 10 DIP cards. The cage may be observed in Figs. 4

and 5. The cage is composed of 12 individual pieces of angled aluminum, 20 aluminum card guides, an aluminum conductor plate, and 20 connector receptacles. The parts of the cage are fabricated from No. 2024-T4 aluminum alloy per QQA-A-225/6. The basic purposes for using the angled-aluminum approach are for strength, rigidity, and prevention of warpage. This design concept was necessary because great stress is exerted on the entire framework as the microcircuit cards are inserted into their respective sockets.

The base plate provides the surface in which to mount the connector receptacles. It was necessary for the plate to be 6.3 mm (0.250 in.) thick because of pressures incurred while inserting the card plug into the cage receptacle. The plate is perforated to permit an unobstructed flow of air onto the DIP cards for cooling purposes.

The connector that mounts in the base plate is a Viking receptacle No. 00241-0021 with the same technical specifications as its mating counterpart. The receptacle contacts are commonly referred to as "fork contacts." These fork contacts terminate into wire-wrap terminals on the opposite side of the connector body. All connector terminals are placed on 2.5-mm (0.100-in.) centers to allow automatic wire-wrapping of the entire bottom plane. Two guide bushing receptacles were developed and installed into each connector body. These bushings mate with the card connector guide pins to prevent misalignment of the connectors upon initial contact.

For each card there are two guides, which are simply slotted square bars with a pivot pin inserted near the top edge. The card guides serve four distinct functions: (1) they align the card plug with the plate receptacle, (2) they add vertical strength to the cage structure, (3) they provide a spring pin on which the insertion lever pivots to insert the card, and (4) they serve as a platform on which the withdrawal lever presses against to release the mated connectors.

The entire card cage assembly is gold-plated, with the exception of the card guides, for the vital purpose of ground integrity. Listed in Table 1 is a unique plating process developed to prevent tarnishing of the cage members.

All of the aforementioned parts, along with all 10 cards installed, constitute the total assembled Integrated

DIP Microcircuit Card and Cage Package, which is illustrated in Fig. 6.

IV. The Card Cage Mounting Enclosure

In order to mount the card cage into a rack assembly, an enclosure was developed that serves as a medium for securing the cage, the drawer slide assemblies, the system interface connectors, and the front panel assembly. The enclosure is easily fabricated from an inexpensive 43-cm $\times$ 43-cm $\times$ 10-cm $\times$ 1.6-mm (17.00-in. $\times$ 17.00-in. $\times$ 4.00-in. $\times$ 0.0625-in.) universal Bud radio chassis.

V. The Extender Card

A device was needed to remotely interface a DIP card with its mating connector for check-out or modification purposes. Therefore, a piece of hardware referred to as an *extender card* was developed which elevates the DIP card above the others to permit unobstructed access to all electrical points. This extender card, into which is plugged a standard card, is illustrated in Fig. 7. The device is simply an epoxy glass board on which is mounted card guides, 2 mating plugs, and 2 mating receptacles which are wired in consecutive order.

VI. Wire-Wrapping Procedures

There are three basic methods used at this time for the wire-wrapping of card terminals: (1) the manually operated portable hand tool method, (2) the semi-automatic machine process, and (3) the procedure involving the use of a totally automated wire-wrapping machine.

Extensive use has been made of a Model 14R2 Gardner Denver battery-operated hand tool which accepts various sizes of bits and sleeves for different wire and insulation diameters. The wire generally used is described as a No. 30 solid conductor with Kynar insulation, P/N KN-30-130-6, MIL-UL-1423. A bit (No. 507063) and a sleeve (No. 500350) are required for the installation of this particular wire on 0.63-mm (0.025-in.) wire-wrap terminals spaced on 2.5-mm (0.100-in.) centers. On each Augat socket terminal, it is possible to make 3 connections of 8 wraps each using a No. 30 gauge wire. If a connection should necessitate removal, it is easily accomplished by the use of a Gardner Denver unwrapping tool No. 505244.

The semi-automatic method is achieved by employing a computer-fed manually controlled wiring machine. The automated wire-wrapping procedure is typically accomplished by the use of a computer-controlled Gardner Denver machine.

VII. Conclusion

The design characteristics of the DIP Microcircuit Card and Card Cage Assembly provide a wide latitude of flexibility and versatility in their application. There are numerous distinguishing features included in the design philosophy which contribute to freedom in application procedures.

The DIP microcircuit card has several universal applications. It may be used simply as a breadboard, as a prototype model, or as a sophisticated piece of hardware around which to design the most complex of systems. The general approach allows any combination of logic and or analog microcircuitry to be inserted and interconnected for any desired function.

The attributes of this unique design, versus the widely accepted printed circuit (PC) approach, allow the engineer to considerably reduce his design and development time. PC boards possess distinctive problems which make them impractical for general application purposes. If a circuit change should occur, an entirely new PC layout is required which is both costly and time consuming. In addition, PC boards have proven to be very difficult to change or repair in the field. Where sophisticated logic or frequent design changes exist, economic and time factors favor the plug-in wire-wrapped card approach.

The elements that comprise the DIP card produce several significant advantages for design applications. For instance, the power and ground planes, covering each side of the board, improve high-frequency performance and reduce electrostatic coupling between each microcircuit. Power and ground are supplied to each DIP, which eliminates the need for additional wiring. The use of Augat-type wide-entry socket terminals allows any dual-in-line package to be easily plugged in and removed without the cumbersome task of soldering and unsoldering leads. The closed-entry socket will indefinitely maintain a secure retention force on the DIP leads by nature of their inherent design. If for any reason a socket terminal requires replacement, it may simply be removed and a new one installed without damage to the board material. At times, situations arise

that prevent the use of DIP circuits. When this occurs, discrete components may be mounted on an adaptor plug which may be inserted into any of the card socket patterns.

The wire-wrap approach also provides several distinct advantages. The solderless wrap termination technique produced such favorable application results that it is currently considered the most preferred method by many electronic system manufacturers. Extensive use by the aerospace industry, the military, computer manufacturers, and the Bell System has proven that the wire-wrap process is much higher in reliability, less time

consuming in application, and less costly than other established techniques for wiring. Wire-wrap's initial and most consistent advantage has been the significant cost savings inherent to the process.

With the design concepts described throughout this article, the design engineer is provided with the potential to develop any digital or analog system whether it be simple or highly sophisticated. It was the basic intent of this article to describe a new design approach that can be used to replace other packaging techniques which previously created rigid restraints in the design of DSN digital systems.

**Table 1. Gold-plating procedure for the Card
Cage Assembly^a**

Sequence	Procedure
1	Polish each piece carefully.
2	Mask all tapped holes.
3	Treat all parts with zincate.
4	Electroless nickel plate surfaces to 0.254-mm (0.001-in.) thickness.
5	Bake all parts at 149°C (300°F) for 1 hour.
6	Repolish all pieces as necessary to obtain smooth surface.
7	Expose each part to "gold strike" process.
8	"Sel-Rex" hard gold plate to all surfaces to minimum of 0.0254-mm (0.0001-in.) thickness.
9	Alodine tapped holes.
10	Buff all surfaces to mirror-bright finish.
^a For all cage parts except card guides.	

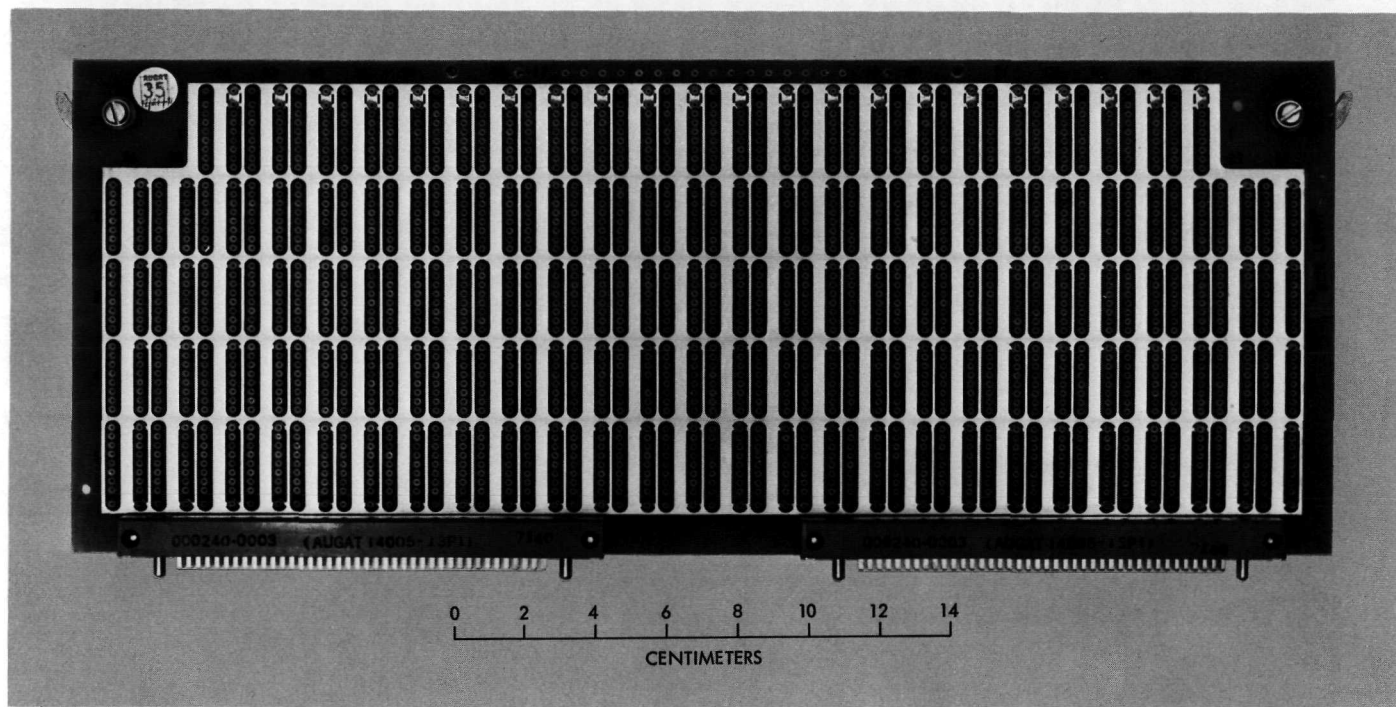


Fig. 1. DIP Microcircuit Card—microcircuit plane

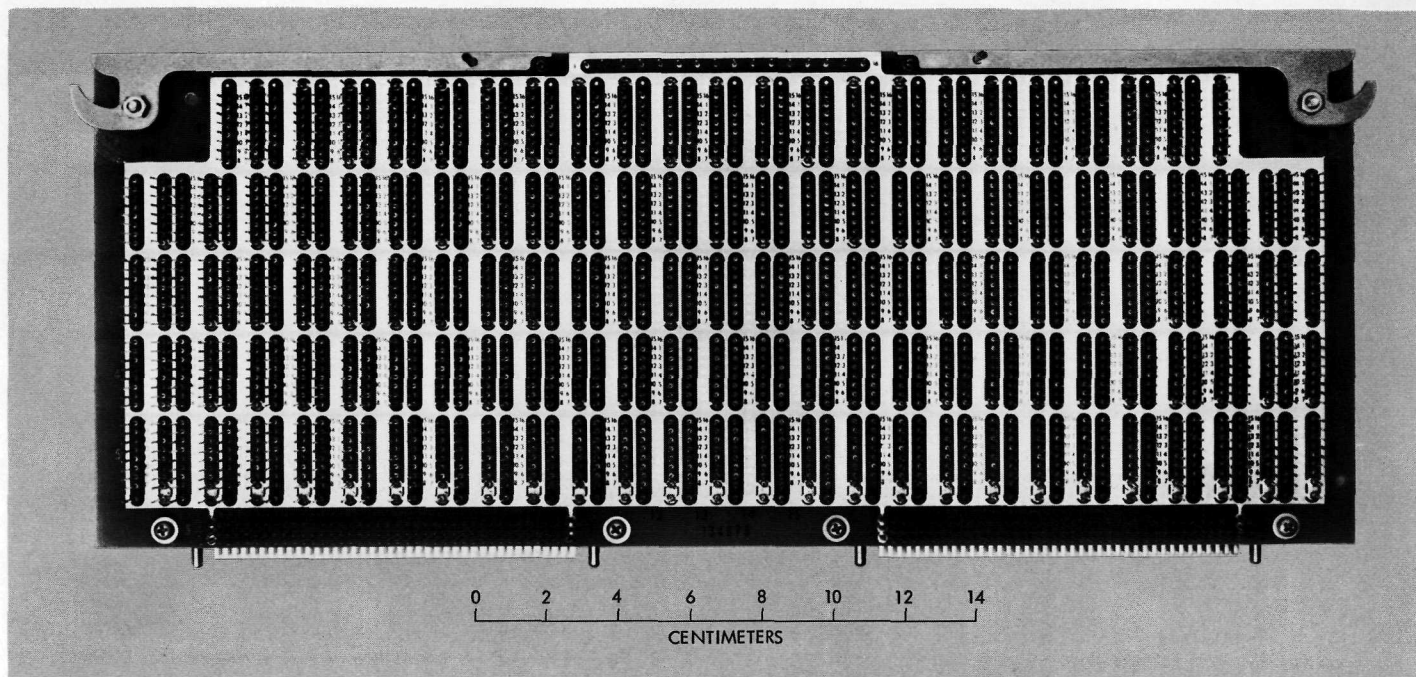


Fig. 2. DIP Microcircuit Card — wire-wrap plane

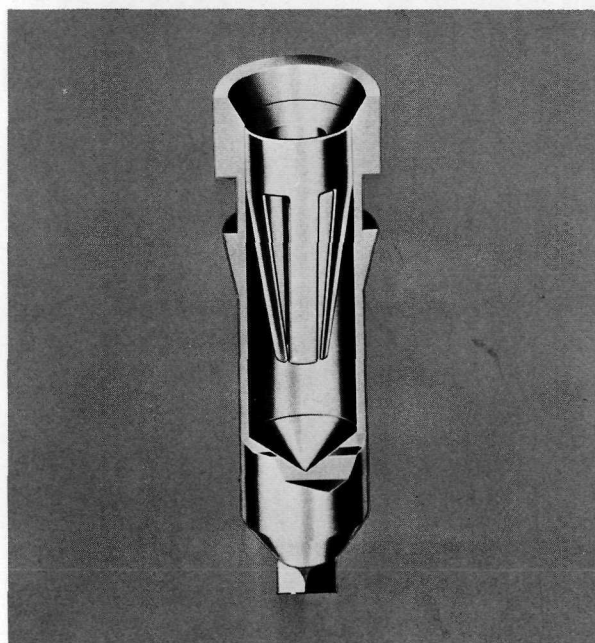


Fig. 3. Cut-away view exposing contact configuration of Augat wide-angle tapered entry socket terminal

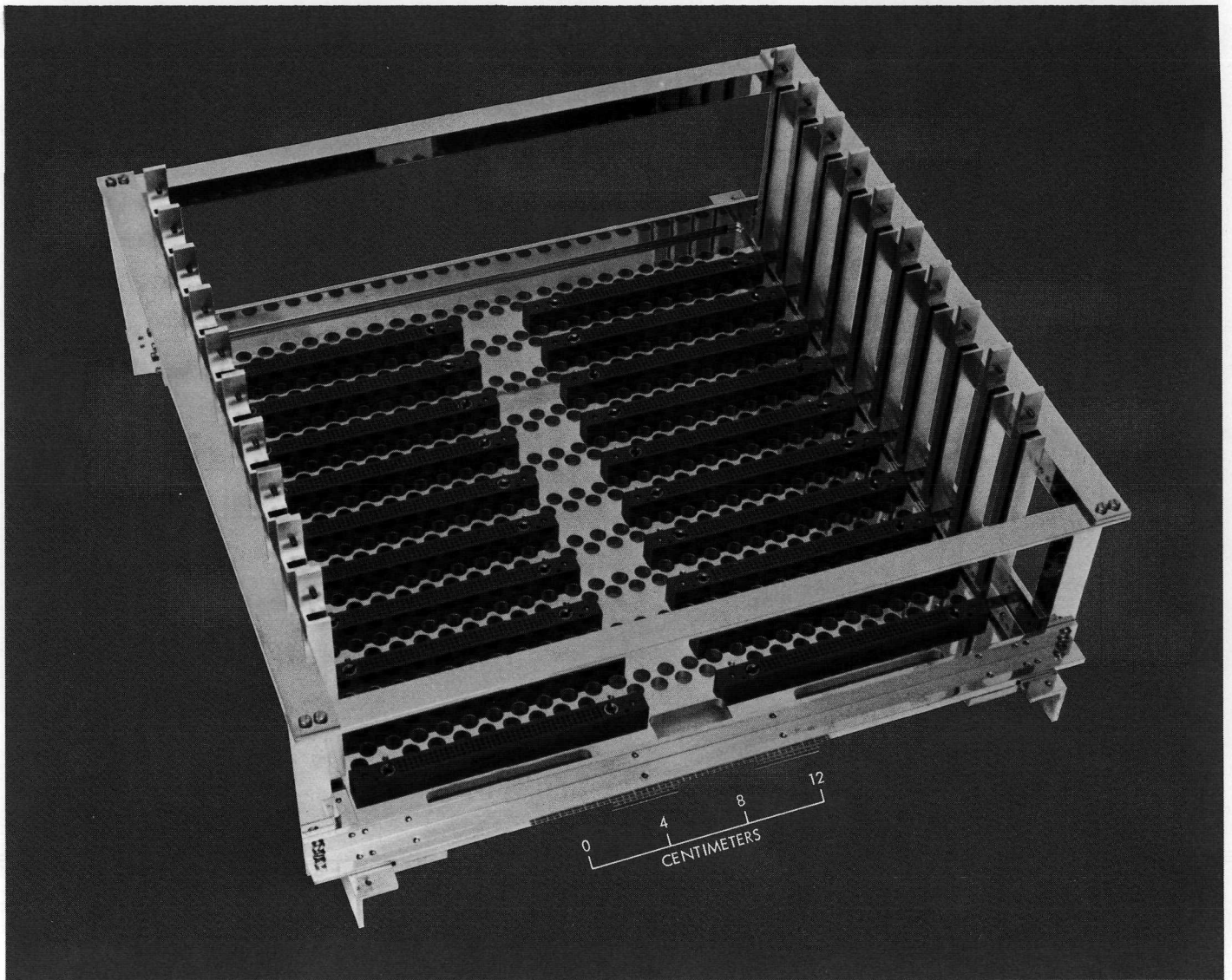


Fig. 4. Top view of Card Cage Assembly

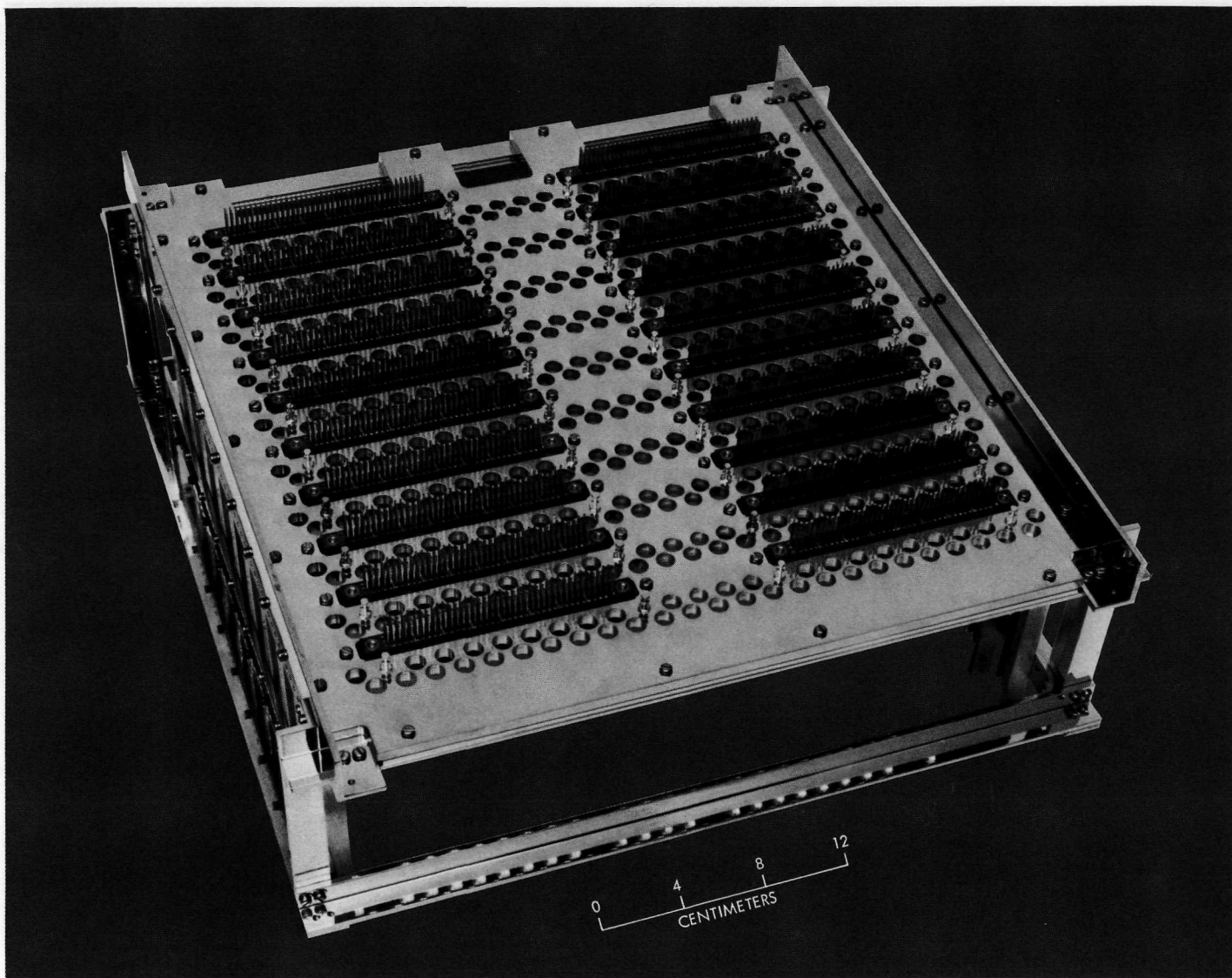


Fig. 5. Bottom view of Card Cage Assembly

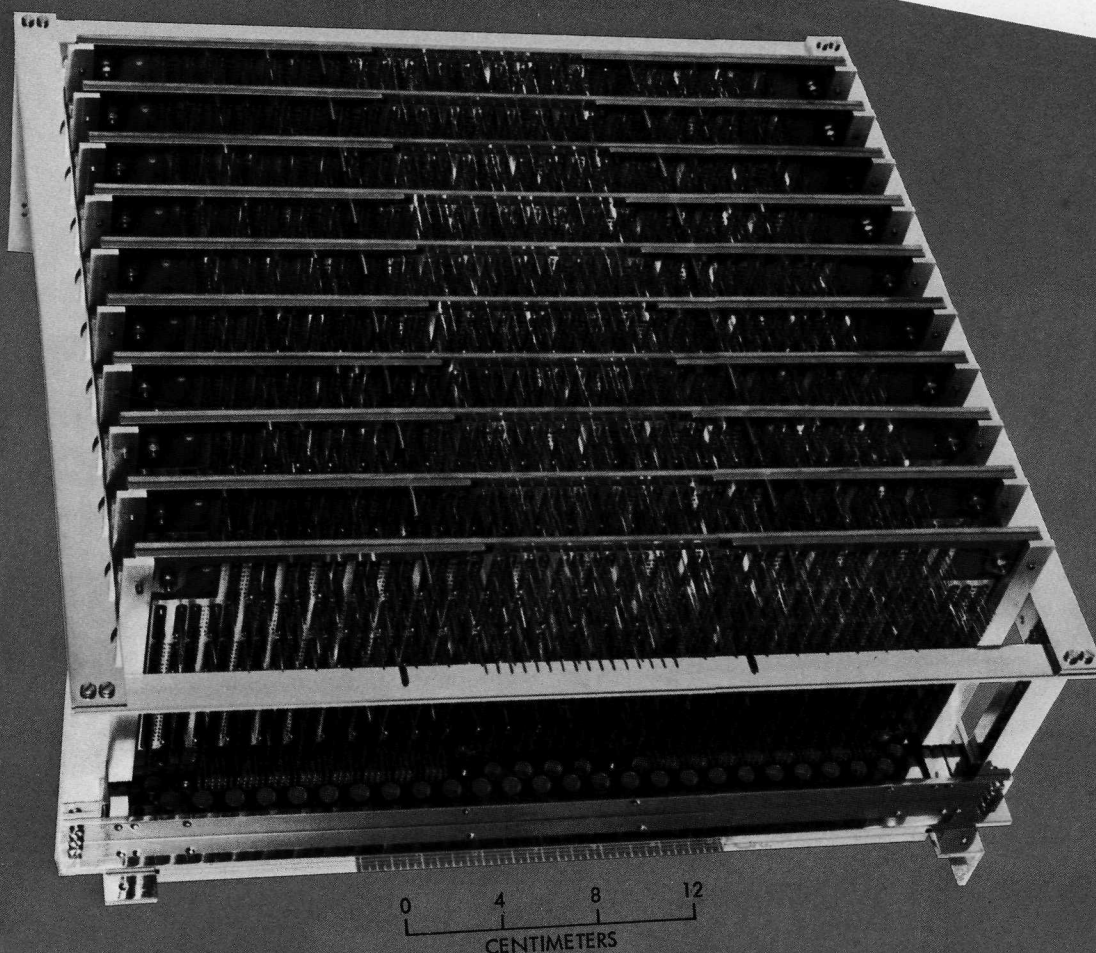


Fig. 6. Total Integrated DIP Microcircuit Card and Cage Packaging Assembly

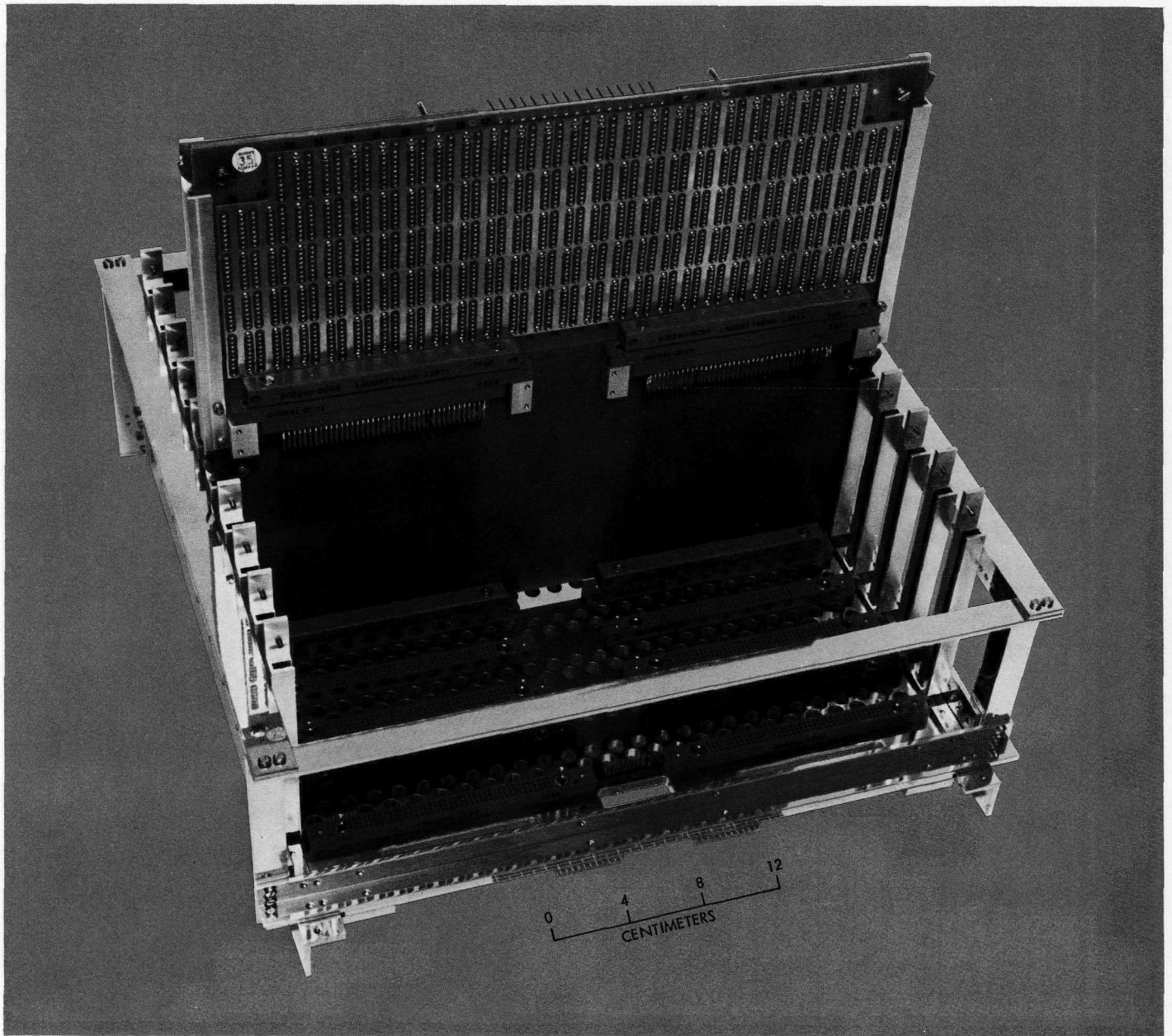


Fig. 7. Extender Card

Predetection Recording and Dropouts

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Predetection recording of spacecraft telemetry data allows for possible future analysis of data records in the event of failures of transmitted signals. Dropouts occurring in the playback process necessarily cause loss of information and, more importantly, loss of time synchronization with the remaining data. The object of this study is to show that, with proper digital handling of a timing signal initially recorded along with telemetry data using a device incorporating a proposed digital dropout detector, time synchronization can be maintained throughout dropouts of lengths less than 100 ms, within some small probability of error. Uses extend to recording of planetary entry low-rate and very long baseline interferometry data and, in particular, to planetary radio occultation information, which is already recorded with a timing signal on the same tape track.

I. Introduction

Currently, the DSN operates with more than one ground station tracking during critical phases of a spacecraft mission. This technique ensures that an entire ground station is available as backup if any failure occurs at the prime tracking station. The ground-based equipment, however, is designed to process the normal signal with small ability to accommodate changes in the spacecraft signals. Hence, it is rendered useless if failures of signal data rates or subcarriers, for example, occur during tracking. Recovery of the data transmitted during such a failure can be achieved if the spacecraft signal is continuously recorded on analog magnetic tape at intermediate frequency, before any subcarrier or data demodulation stages. Linear direct magnetic recording utilizing wideband instrumentation

recorders such as the Ampex FR 1400 units presently installed at DSN stations is a cost-effective way of creating real-time predetection telemetry data records for future analysis. Imperfect tape drives and the imperfect magnetic recording medium cause tape speed variations, or flutter, and random data dropouts (Ref. 1), respectively. Loss of some data and, more importantly after a dropout, loss of synchronization with the subcarrier, bit, word, and frame syncs are the detrimental results.

A realistic solution to this problem is to record a sinusoidal reference signal on the same tape track with the data. Due to the present limitations on speed of data reconstruction equipment, there needs to be a speed reduction from 304.8 cm/s (120 ips) at record to 4.76 cm/s

(1½ ips) at playback. Flutter frequency modulates the reproduced signal at the low playback rate, necessitating some type of flutter frequency model if the timing sequence is to be predictable during and after a dropout.

This article assumes that the effective flutter can be approximated as a single-frequency FM modulating signal. Results of frequency and time-domain analyses of a reproduced sinusoid are shown, verifying the assumption for short time intervals (<100 ms). Computer simulation of a digital dropout detector, consisting essentially of a phase discriminator and a function generator, the latter incorporating the appropriate flutter model, is described. Probability density curves of the phase errors occurring during randomly initiated dropouts, of duration less than 100 ms, are presented. Applications extend to recording of planetary entry low-rate data, two station and very long baseline interferometry (VLBI) data, and also to planetary radio occultation experiment IF. The latter is presently detected and then recorded along with a timing signal on the same tape track. Occultation information lies primarily in the phase variations of the signal, making information extraction very vulnerable to both flutter and dropouts.

II. Frequency and Time Domain Analysis of Flutter

A. Frequency Analysis

Most approaches (Refs. 2 and 3) characterize flutter as a random Gaussian process, with a rather uniformly distributed power spectrum, from 1 Hz to 10 kHz. In this analysis, the intention is to establish that flutter can be approximated as a single-frequency FM modulating signal.

A timing sinusoid with a frequency of 320 kHz was recorded at 304.8 cm/s (120 ips) and played back at 4.76 cm/s (1½ ips), resulting in a flutter-modulated signal centered at 5 kHz. This was then sampled at 20 kHz, and the data were used in a computer routine in order to isolate the flutter sidebands.

A Fast Fourier Transform (FFT) computer algorithm was then applied to the sampled data; Fig. 1, representing 15 averaged spectra, clearly shows the predominant playback flutter sidebands, displaced 7.5 Hz from the center frequency, in this case 4994.83 Hz. The resolution of this particular FFT was set to 0.57 Hz, with 2048 points used. The most immediate side lobes around each of the major peaks are displaced by about 0.9 Hz and believed to be due to the record flutter, affecting the playback flutter as

well as the carrier. The record flutter is substantially smaller than the playback flutter, supporting the view that at high speeds the tape drive is more linear.

B. Time Domain Analysis

A series of second-order Chebyshev polynomials were fitted to the original sampled timing sinusoid for every cycle of the sinusoid. Curves were fitted to each set of 4 sample points for every successive point, thereby resulting in a set of values of crossover times at each half-cycle of the function. These values were correlated for similarity and then averaged to give the net phase response of the sinusoid, with an estimated error of ± 10 degrees for every 180-degree phase interval. Figure 2 is a block diagram of the program.

The ideal phase $\omega_0 t$ (where $\omega_0 = 4995$ Hz from the FFT analysis) was subtracted from the net phase estimate $\hat{\phi}(t)$ to give $\hat{\theta}(t)$, an estimate of the phase variations due to flutter. A continuous average of $\hat{\theta}(t)$ with an averaging period of 50 cycles of the original sinusoid (about 0.01 s) resulted in the phase function $\hat{\theta}_A(t)$. As expected, it was found that $\hat{\theta}_A(t)$ is the sum of several sinusoids. The predominant term is of the form $K_m(t) \sin(\omega_m t + \alpha_m)$, where ω_m , agreeing with the FFT, is 7.5 Hz, and $K_m(t)$ varies between about 1.0 and 2.0 radians.

Three other sinusoidal components were detected: one continuous term at a frequency of 0.2 Hz and amplitude of about 1.7 radians, and two lesser sinusoids, one at 0.5 Hz (~ 0.3 radians), and the other at 1.73 Hz (~ 0.8 radians), which alternated with a period of 0.5 s. It was difficult to accurately define these latter amplitudes due to the predominance of the 7.5-Hz term with its large varying amplitude. These lower frequency terms did not show up in the FFT analysis, due to the resolution limitations in defining the spectrum.

III. Discussion of Results

The main playback flutter component at 7.5 Hz was traced to the drive motor, which, at a tape speed of 4.76 cm/s (1½ ips), rotates at 7.5 rps (450 rpm) in an Ampex FR 1400 machine, the type on which the signal was originally reproduced. At the record speed of 304.8 cm/s (120 ips), the tape drive motor rotates at 3600 rpm. This translates down to a frequency of about 0.9 Hz at a playback speed of 4.76 cm/s (1½ ips), agreeing with the spectrum record flutter value.

The continuous 0.2-Hz component may be due to the irregular rotation of the 25.4-cm (10-in.) takeup reel on

playback, which rotates at about 0.12 rps when empty and at 0.06 rps when full. This requires that the reel have two "bumps" occur for every revolution.

If the phase were observed for a longer period of time (i.e., the length of the tape), the frequency of this component should decrease to about 0.1 Hz. The other two alternating low-frequency signals, each present for about 0.5 s, were not traced to any specific mechanical rotation. In any event, the speed control built into the machine cannot compensate for these low-frequency flutter components.

IV. Dropout Detector Simulation

Several tracking devices were simulated on a computer, utilizing the same sampled sinusoid data. They all basically performed the function of extracting the average phase and frequency variations $\hat{\theta}_A(t)$ and $\hat{\omega}_A(t)$ as shown in Fig. 2. Whenever a dropout occurred, a sine function was then generated, in the form $\hat{\theta}_e(t) = K_m(t) \sin(\omega_m t + \alpha_m)$. For any dropout, $K_m(t)$ was set equal to the average of the magnitudes of all the preceding maxima and minima values of $\hat{\theta}_A(t)$. The distribution of these magnitudes was observed to be unevenly spread about 1.5 radians, with a maximum deviation of ± 0.5 radians. ω_m was in turn set equal to the rate of change of the most recent pair of maximum and minimum values of $\hat{\theta}_A(t)$. The resulting model

phase values $\hat{\theta}_e(t)$ were compared at crossover times of the real phase function $\hat{\theta}(t)$, and the errors for each half-cycle of the sinusoid obtained. Figure 3 shows the measured probability density of phase error for two typical dropouts. The dropout intervals were both 100 ms, resulting in sample sets of about 1000 half-cycles, with error windows of 5 degrees used in establishing phase error magnitudes. It should be noted that for the Rayleigh-type density curve, the majority of error values is concentrated in the region of less than 20 degrees, while the other curve exhibits a broader error distribution, with a secondary peak in the range of 35 to 40 degrees. It was found that this latter curve represents a time interval during which there is a rapid rate of change in the magnitudes of the maximum and minimum values of $\hat{\theta}_A(t)$, resulting in a higher probability of error for the estimated value of $K_m(t)$ used in the model, and hence a larger error distribution. During both dropouts, the magnitudes of the phase errors tended to increase with the length of time of dropout, with errors exceeding 20 degrees occurring typically well after 50 ms.

Hence, this simple form of detector, containing essentially a phase discriminator and a sine function generator, could track through a dropout of length 100 ms or less, predicting the number of lost timing pulses (180 degrees apart) with a maximum error of ± 60 degrees for any one pulse.

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2. Abramson, N., "Bandwidth and Spectrum of Phase and Frequency Modulated Waves," *IEEE Trans. Comm. Sys.*, Vol. CS-II, pp. 407-414, Dec. 1963.
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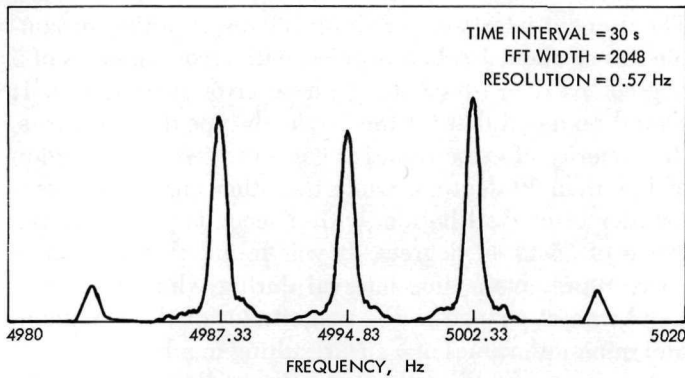


Fig. 1. Power spectrum of timing sinusoid showing flutter sidebands

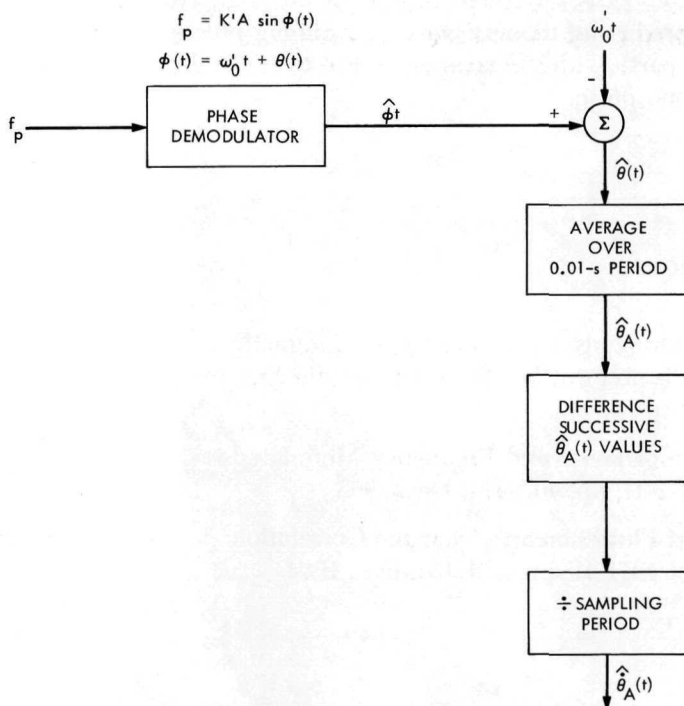


Fig. 2. Block diagram analog of the time domain analysis program

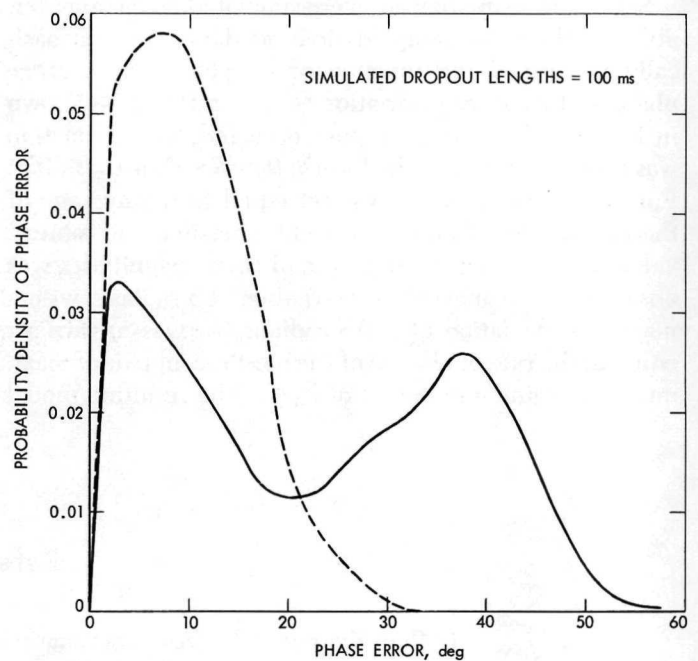


Fig. 3. Probability density of phase error between timing sinusoid and model for two randomly initiated dropouts

Wide Range, Essentially Linear Control Circuit for Control of the Reference Frequency in Digital Phase-Locked Loops

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A simple all-digital control circuit intended for control of the frequency of the reference signal in all-digital phase-locked loops is presented. Such control circuits, of prior art, are often nonlinear and provide only for narrow frequency range. The present control circuit, though very simple, provides for essentially linear control for a wide frequency range. The circuit presented in this article is intended for use in all-digital phase-locked loops and described in this context.

I. Introduction

A phase-locked loop implemented entirely with digital circuits references all its operations to a fixed high-frequency service clock. This clock is derived from a simple crystal oscillator operating at the maximum operating speed of the digital circuits. To keep the step size as small as possible and also of the same general size for correction in either direction, the general principle of the frequency correction mechanism is that of deleting every n th pulse in the pulse train from the oscillator to an output divider for the steady state and $(n - m)$ and $(n + m)$, respectively, for correction in either direction.

The output from a simple counter/divider which can be programmed to divide by one of a set of integers controls a pulse delete gate resulting in the instantaneous frequency of the reference signal: $f_n = [(n - 1)/n] f_0$, where

f_0 corresponds to the uncontrolled frequency of the reference signal. A change of n to the next larger or next smaller integer does not result in the same frequency change, i.e., for small n 's the changes are large and for large n 's the changes are small. For $(n < 10)$ the frequency changes are too large and too nonlinear to be usable in a control system. For these reasons n must be limited to $(n > 10)$, which in turn limits the acquisition range to $\sim 5\%$ about the center frequency.

In Ref. 1 an entirely digital implementation of a bit synchronizer for noiseless binary data is described. This synchronizer includes one search and one track mode, both using the control circuit indicated above. For the search operation n is varied from 10 to 20 and for track operation from 20 to 30. For many purposes the search range of only $\pm 5\%$ may, however, be too narrow.

This article presents a simple control circuit which makes the control of the frequency of the reference signal essentially linear and extends the acquisition range from 10 to 50%.

The design strategy is explained first as it was conceived for the simplest possible implementation. The new control circuit is then discussed in reference both to its block diagram and detail logic diagram.

II. Design Strategy

Deleting one pulse every n th pulse requires that n be an integer. For smallest possible control steps n must then include all possible integers ≥ 2 . The implementation of $f_n = [(n-1)/n] f_0$, which is shown as plot B in Fig. 1, contains a programmable counter/divider which can be programmed to divide by 2,3,4,5, $\dots$, n . The output of this counter controls a pulse delete gate in the pulse train from the oscillator to the output divider.

Another simple counter is a binary ripple counter which divides by 2,4,8,16,32, $\dots$, 2^n . Selection of any one stage of such a counter for control of a pulse delete gate results in function $f_n = (2^n - 1/2^n) f_0$. This function, although simple to implement, is by itself essentially unusable as a control function. For reference see plot A, Fig. 1.

However, if one subtracts the difference $A - B$ from B , the result, shown in plot C Fig. 1, becomes a desirable function. For control purposes this function is essentially linear and usable for all n 's ($2 \leq n$) resulting in a 50% control range.

As will be shown, both the $A - B$ and $B - (A - B)$ functions are very simple to implement, each requiring only a flip-flop (F-F) and a gate.

III. Functional Block Diagram

For references see Fig. 2. The inputs to the divide by n divider and the divide by 2^{n-1} divider are derived from the true and complement output from the oscillator, respectively. This will assure that A and B are of different phase and that for $n = 2$, $A - B = 0$. As is readily ap-

parent from the block diagram (Fig. 2), if the same phase were used for both A and B , $A - B$ would be ambiguous.

IV. Detail Logic Connections

The $A - B$ and $2B - A$ circuits are identical and very simple, as shown in Fig. 3. An F-F is set and reset on the A and B pulses, respectively. If two B pulses occur within the period between two A pulses, an output pulse is registered.

The divide n counter/divider is implemented by simply setting a number of counter F-Fs to the binary equivalent of n . The set operation takes place over set gates and the F-Fs are connected to count down. The output of an all-zero gate will enable the set gates and again set the F-Fs to n . Setting takes place from a zero condition requiring only a single set term for each F-F. For references see logic diagram (Fig. 4). Only four bits are shown in the figure; however, the design is iterative.

The counter/divider which divides by 2^n is in itself trivial. Only with n being the selection number and available in binary notation a base-two to base-ten conversion network is required.

As apparent from the expression $f_n = [(2^n - 1)/2^n] f_0$, the frequency change for ($n > 8$) is negligible. n can then be limited to ($2 < n < 8$). For ($n < 8$) the ($n_{(2)} \rightarrow 2^n_{(10)}$) conversion network simply reduces to a readily available binary-to-decimal decoder. Two design versions of the divide by 2^n counter programmable by n in binary notation and where ($n < 8$) are considered. The first is identical to the divide by n counter, the only difference being that the ($n_{(2)} \rightarrow 2^n_{(10)}$) decoder is inserted between the selection terms and the set gates as shown in Fig. 5.

In the second version shown in Fig. 6, the output from the ($n_{(2)} \rightarrow 2^n_{(10)}$) converter selects the output from any one stage of the counter as the final output. With the output from any one F-F being a square wave, a circuit is required to form a one clock period pulse of that periodicity.

For ($n > 8$) the divide by 2^n counter/divider or its effect on the system should be inhibited. The inhibit term may be the output from an OR-function whose inputs are all the ($2^n_{(10)}$) terms for ($n > 3$).

Reference

1. "Digital Data Transition Tracking Bit Synchronizers for Noiseless Binary Waveforms," *Communications Designer's Digest*, p. 12, Nov.-Dec. 1971.

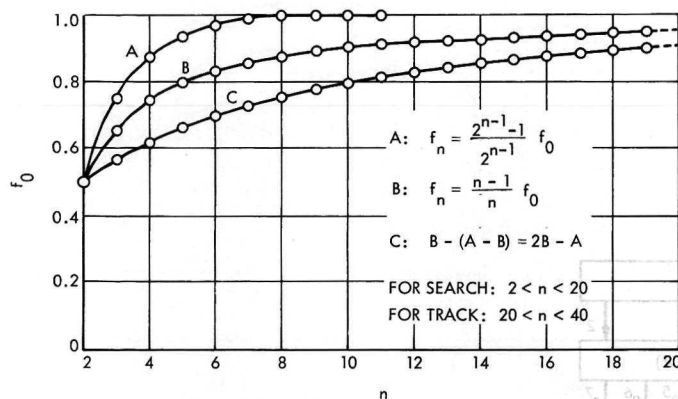


Fig. 1. Control function graphs

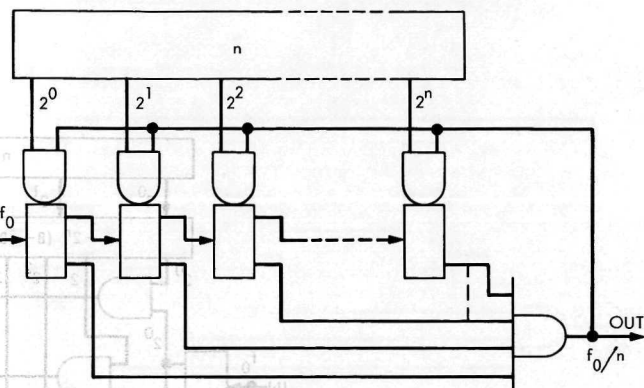


Fig. 4. Logic diagram of a programmable divide by n counter

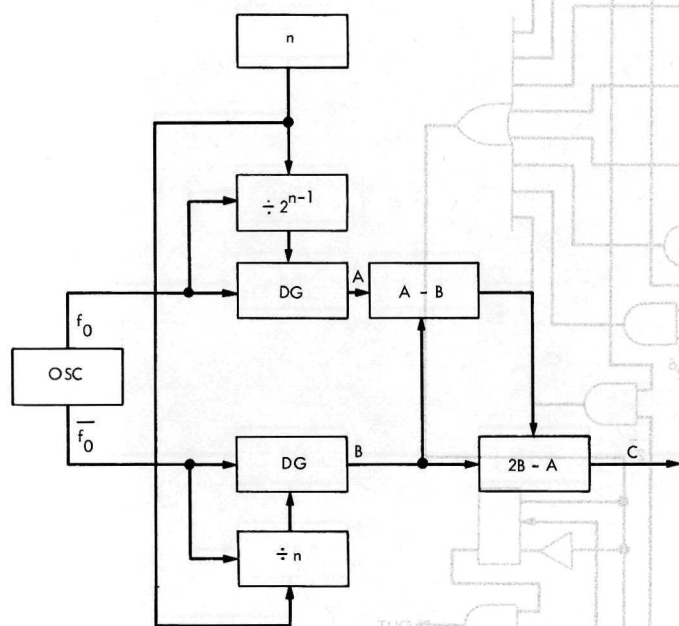


Fig. 2. Functional block diagram for implementing the $2B - A$ function

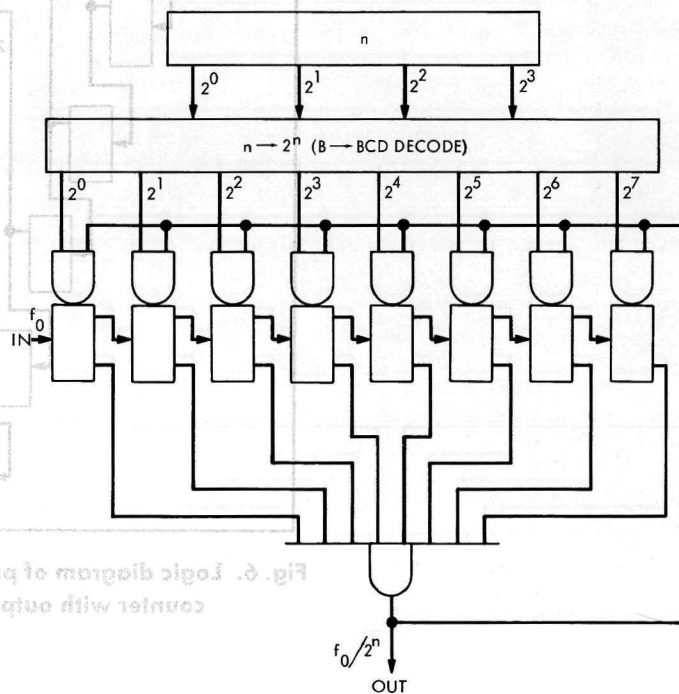


Fig. 5. Logic diagram of a programmable divide by 2^n counter with parallel set gates

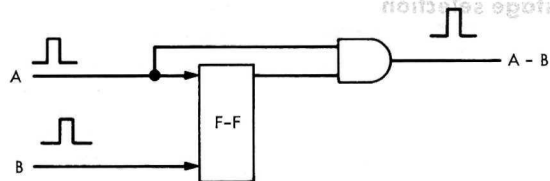


Fig. 3. Detail logic diagram showing an $A - B$ logic

CLOCK

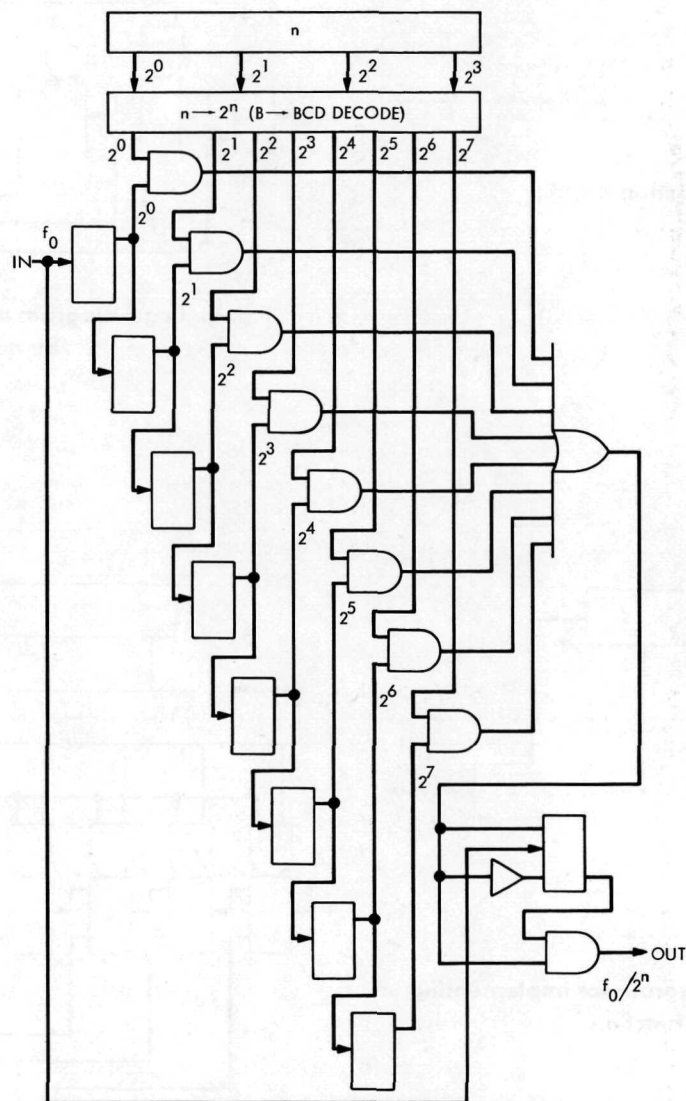


Fig. 6. Logic diagram of programmable divide by 2^n counter with output stage selection

Efficient Implementation of a Multichannel High-Speed Correlator

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The correlator presented in this article is an all-digital or sampled real-time signal processing system. It is intended for applications requiring wide bandwidth and high resolution such as measurement of spacecraft spectra or the close scrutiny of a wide bandwidth for interference to validate performance of the new dual S/X DSN system. The detection of signals in noise upon reception of radio astronomy signals is yet another application for which the present instrumentation would be useful.

I. Introduction

Earlier DSN correlators were of the serial type such as described in Refs. 1 and 2. These were generally slow but efficient as to component count. Other DSN correlators have been designed and constructed of parallel designs. These were generally very fast but their high cost often limited the number of channels. The present correlator design combines some of the cost efficiency of the serial correlator, yet it operates at the speed of the parallel designs.

The input signal is sampled at a 20-MHz rate and quantized to one bit. The correlation function involves time separation. One thousand twenty-four (1024) time lags or channels are considered. The efficiency in implementation is derived from novel design strategies coordinated with the most efficient functional components presently available. As the switching rates of the more significant bits of the accumulators decrease, the accumu-

lators are sampled via a multiplexer, and continued accumulation is performed using a random access memory (RAM). The multiplexer, which must operate at the maximum rate, is implemented using a parallel-in-serial-out shift register. This design also separates the time base between the input and output systems.

II. Background

For an autocorrelation function, the processing operation compares a waveform with a time shift of itself. For a cross-correlation function, two different waveforms are compared. In the continuous domain,

$$\text{(Auto)} \quad R_{xx}(\tau) = \frac{1}{T} \int_0^T x(t) x(t + \tau) dt$$

$$\text{(Cross)} \quad R_{xy}(\tau) = \frac{1}{T} \int_0^T x(t + \tau) y(t) dt$$

In the discrete domain, the formulas become

$$R_x(r) = \frac{1}{N} \sum_{k=1}^N x_k x_{k+r}$$

$$R_{xy}(r) = \frac{1}{N} \sum_{k=1}^N x_k y_{k+r}$$

One particular system, a computer preprocessor, is described here in detail.

The present implementation derives its efficiency from novel design strategies coordinated with the most efficient functional elements presently available.

III. Basic Design

As shown in the block diagram (Fig. 1), the input signal is assumed quantized to one bit. The binary waveform is entered, at its clock rate, serially into a 1024-bit shift register. The register has an output or tap for each bit, each corresponding to one-bit time lag. Each such output from the shift register is multiplied, or added mod-2, with the reference signal. In the case of autocorrelation, the input signal is the reference signal. The output from each mod-2 circuit feeds an integrator or accumulator, each with a capacity of 2^n counts ($8 \leq n \leq 12$). The most significant bits of the accumulators are sampled via a digital multiplexer, and its single-term output feeds the low-speed accumulator system which contains the random access memory.

IV. Detail Design

Once the block diagram (Fig. 1) has been established, the design reduces to the selection of the most efficient high-speed functional components. In cases where ideal components were not available, special design measures have been considered. The most important of such special cases occurred in the design of the high-speed high-capacity accumulator.

V. Data Entry

A high-speed shift register (20–30 MHz) with one parallel output for each bit is required in the data entry section. Eight-bit 20-MHz shift registers in 16-pin packages are available from several manufacturers, 8 being a convenient binary integer for efficient physical groupings. One manufacturer also markets a 10-bit serial-in-parallel-out shift register.

VI. Multiplier

Four regular mod-2 circuits are the most that can be contained in a 14- or 16-pin package that is readily available. Six circuits could be contained in a 16-pin package if one term were common as is the present case. Such an element is, however, not yet made. Another design problem in conjunction with the mod-2 circuit is that the presently available high-speed high-capacity accumulators are not equipped with clock inhibit terms. Again only four clock gates per package are available, while six would be possible with one term common.

If one, however, examines the logic of 74H87 (shown in Fig. 2) and the mod-2 arithmetic,

$$C(A \oplus B) = AC \oplus BC$$

$$\overline{A \oplus B} = \overline{A} \oplus B = A \oplus \overline{B}$$

$$\overline{\overline{A} \oplus \overline{B}} = A \oplus B$$

one finds that 74H87 will perform the combined function of mod-2 and clock gating for four channels.

VII. High-Speed Accumulator

No single package capable of accumulating at 20 MHz with a capacity of 2^{16} bits or higher is presently available. The most suitable is the dual 8-bit shift register which can be connected as a cascaded "Johnson-counter" with a total accumulator capacity of 2^8 . The one package per accumulator described above will be referred to as the *high-speed accumulator*. If one would have to resort to two packages per accumulator, the complete correlator would be large in size and cost. Having accumulated up to 2^8 , the switching rate of the most significant bit is reduced accordingly and continued accumulation can be performed in a more efficient manner, as will be discussed in the following.

VIII. Low-Speed Accumulator

The design of the low-speed accumulator exhibits the major novelty of this correlator design. For its description and explanation, reference is made to the right side of Fig. 1.

A multichannel low-speed accumulator may be designed using a multiplexer and a random access memory with the multiplexer and the memory being commonly ad-

dressed. Assume that the input to a low-speed accumulator channel is the most significant bit of a high-speed accumulator. This bit is sampled, via the multiplexer, and if the sample is affirmative, the count stored in the RAM is accessed, augmented, and the augmented count restored. It goes without saying that the speed of the multiplexer must be adjusted to the speed of the RAM's access-augmentation-store operation and that the number of multiplexed channels for input to one RAM must be such that all channels can be processed in the time between two events of the highest rate channel. An event in this case is the high-speed accumulator reaching full scale. The augmentation circuit is a passive parallel adder.

The event of the high-speed accumulator reaching full scale is the input to a low-speed accumulator. Detection of a high-speed accumulator full scale requires that a storage bit be set upon the transition of the most significant bit (MSB) of the accumulator from a one to a zero and that this storage bit be reset upon an affirmative sample. The design of the low-speed accumulator outlined above becomes especially attractive, because the high-speed accumulator transition detection storage bit may be located on the output side of the multiplexer in the already available RAM. A single bit in the RAM is used to store the condition of the MSB of each high-speed accumulator as detected at sample time. Upon an address, the previous condition of its MSB is accessed. If the previous condition is a *one* and the present condition a *zero*, *full scale* has occurred in the high-speed accumulator and its count at that address is augmented and restored. The present condition of the MSB, which is now a *zero*, is also stored.

The augmentation circuit consists of a passive parallel adder followed by a hold register. The RAM read/write control is a single term. A word is available at the output of the RAM for the duration of the read cycle which is half the clock cycle. During the read cycle the word is augmented through the passive adder. An intermediate hold register is required to hold the augmented word during the write cycle, which is the second half of a clock cycle. Reset of the intermediate hold register for one multiplexer cycle will assure that the RAM is initially cleared.

IX. Multiplexer

A number of addressable multiplexer packages, designed as 16 to 1, 10 to 1, 8 to 1 switching networks, are readily available. A large tree of such multiplexer packages exhibits a considerable propagation delay. This type of multiplexer samples the inputs sequentially. The opera-

tion of such a multiplexer requires that the input and the output, namely, the high-speed accumulators and the RAM, be operated on the same time base, or special sync circuits must be inserted between the multiplexer output and RAM input.

A simpler and more efficient multiplexer consists of a string of parallel-in-serial-out shift registers. All channels are then sampled simultaneously, and the multiplexer clock system is entirely independent from the input clock system.

This is especially important because the multiplexer and the RAM interface with the computer and operate on the computer time base.

X. Random Access Memory

Little else need be discussed about the random access memory except its size and/or grouping of packages to form the required total capacity. The memory and its associated multiplexer are dimensioned so that in the time it takes a high-speed accumulator to reach full scale, all channels are able to be sampled and updated, i.e., their content read out from memory, augmented if called for, and rewritten in memory. Popular memory sizes are 16×4 , 64×4 , 256×1 , 1024×1 per 16-pin dual in-line package (DIP). The access time is typically 75 ns and the write-pulse width is of the same order.

XI. Speed of Operation and Component Grouping

With eight bits in the high-speed accumulator, at 20-MHz input rate, 64 channels can be multiplexed and updated in the time it takes to reach full scale. For 1024 channels, 16 such multiplex MUX/RAM entities must then be multiplexed for output. Regular sequential multiplexer packages are used for this purpose.

With nine bits in the high-speed accumulator, only eight MUX/RAM entities are required, and with ten only four, i.e., one per 256-channel chassis.

With a 12-bit accumulator, only a single RAM is required and no output MUX. RAMs are conveniently available in 1024×1 , requiring one package per low-speed accumulator bit. The entire 1024 channel low-speed accumulator section with eight bits per accumulator, ex-

cepting the multiplexer, can then be implemented with only 13 packages.

XII. Packaging

The 1024-channel correlator can be packaged in four 7.6 cm (3 in.) high standard 48.3 cm (19 in.) cabinet drawers, each containing a checker-board pattern of 32×20 sixteen-pin wire-wrap DIP sockets. The detail design of the drawer may not be of any particular interest here but is described in Ref. 3.

XIII. Conclusion

An all digital design and implementation of a 1024-channel 20-MHz correlator has been presented which coordinates novel design strategies with the most efficient presently available circuit packages. Such a coordination, for example, is the high-speed accumulator which uses a dual 8-bit shift register package connected as a cascaded

"Johnson counter" resulting in a counting capacity of 2^8 . Another is the "true/complement" element used as a combined mod-2 input and clock inhibit gate.

The digital multiplexer, yet another coordination, uses a parallel-in-serial-out shift register. This is an especially important innovation as it assures simultaneous sampling of all channels. It also forms a partition between the input and output system so that these systems can be operated on individual and independent time basis with no other sync measures required.

The most important innovation in the correlator design presented is the low-speed accumulator design. Two very attractive design coincidences have been capitalized on. One is the requirement for an output multiplexer, which makes possible the use of a RAM for accumulation. The second is that once a multiplexer and a RAM are included in the system, the status (most significant bit) of the high-speed accumulators can most conveniently be stored in the RAM.

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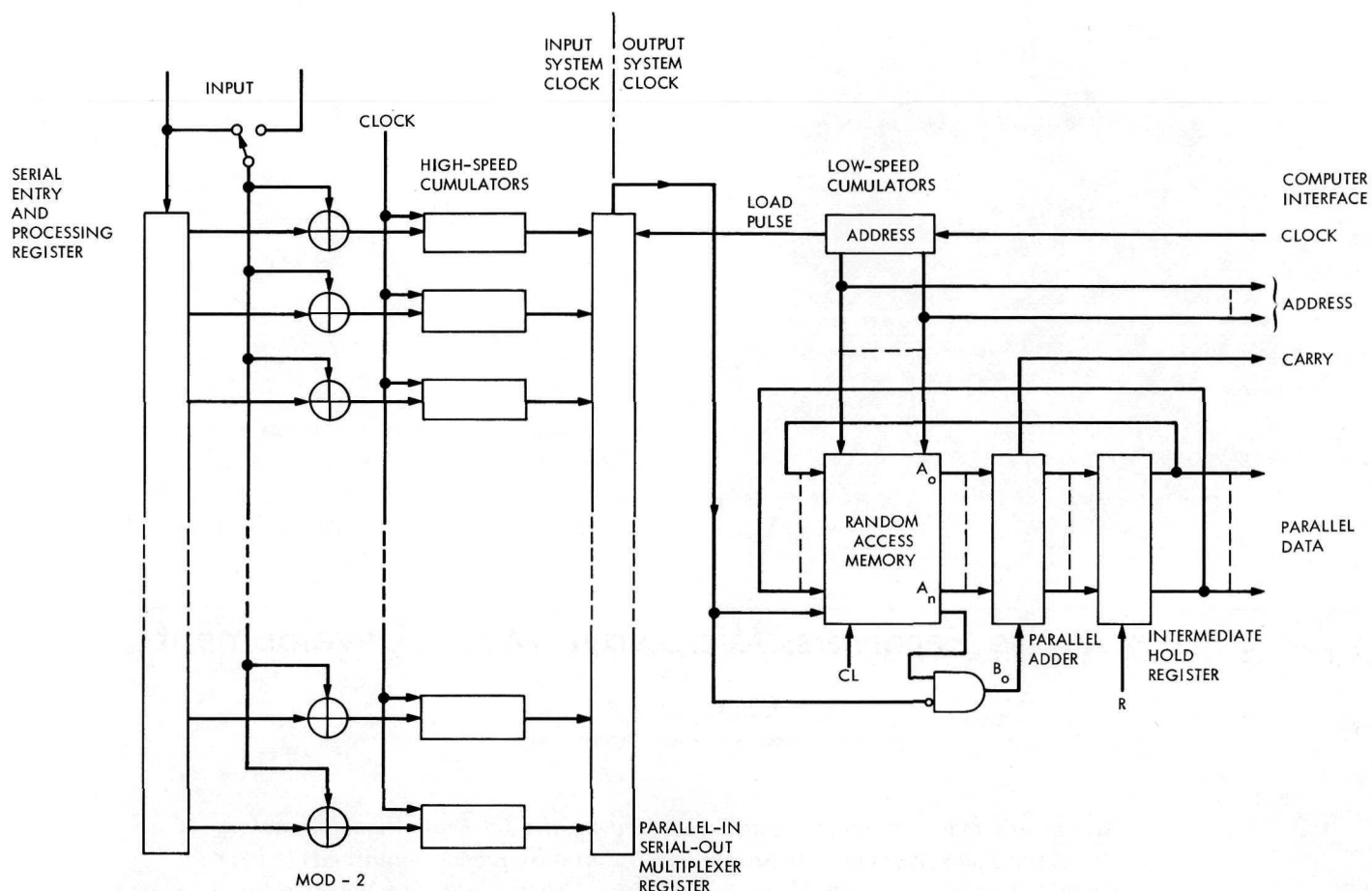


Fig. 1. Block diagram of a multichannel high-speed correlator

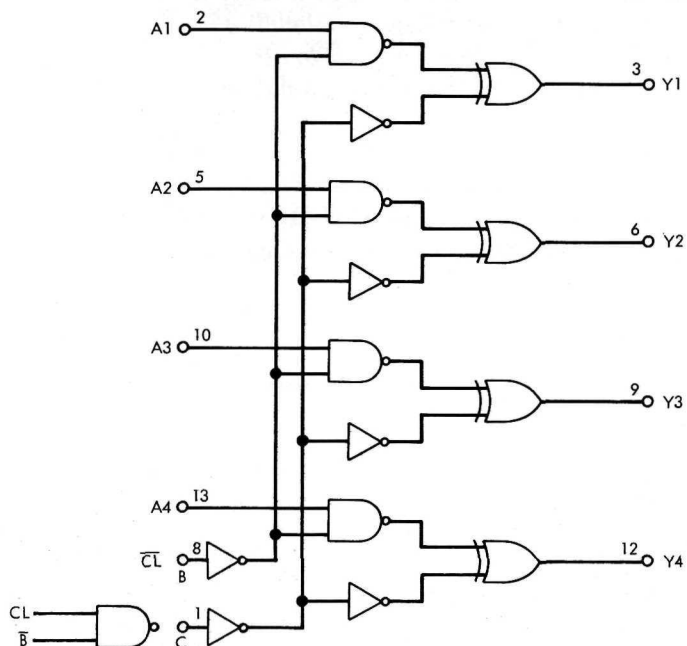


Fig. 2. Logic diagram of combined mod-2 and clock gate

Low Noise Receivers: Microwave Maser Development

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Microwave maser amplifiers have been used by the Jet Propulsion Laboratory in the Deep Space Network for twelve years. Pump frequency requirements have been met mainly with reflex klystron oscillators. Other microwave power sources have been tested for use as maser pump sources. Successful performance tests have been achieved with backward-wave oscillators, crystal-controlled oscillators using solid state multipliers, impatt oscillators, and an impatt noise generator. Current maser pump source requirements have a frequency range of 12.5 to 45 GHz. Power required is approximately 150 mW. Cost, availability, reliability, frequency and power stability, tunability, and power requirement considerations have resulted in the use of klystrons as pump sources for all maser amplifiers now operating in the Deep Space Network.

I. Introduction

The use of microwave maser amplifiers in the Deep Space Network (DSN) began in 1960 at Goldstone, California. A 960-MHz cavity maser was used on a 26-m-diameter antenna. A reflex klystron oscillator at 10.6 GHz was used to pump the maser. Since 1960, 44 maser systems have been installed on antennas in the DSN at L-, S-, X-, and Ku-band frequencies (960 MHz to 16.3 GHz).

Five different types of microwave power sources have been used to provide pump power for masers at the Jet Propulsion Laboratory (JPL). Many considerations led

to the selection of reflex klystron oscillators as pump sources for all maser amplifiers currently in use in the DSN.

II. Maser Pump Requirements

Maser pump frequency requirements are determined by the maser signal frequency and the type and orientation of the maser material used. Ruby material oriented with $\theta = 90$ deg in comb-type traveling-wave masers is now used in all DSN maser amplifiers. Maser signal and pump frequencies used in the DSN or in tests at JPL are listed in Table 1. The pump frequency required for

optimum maser performance is within 30 MHz of the value listed in Table 1. Individual masers of the same design vary in the precise pump frequency needed for optimum performance. These pump requirement variations are caused by slight differences of ruby size, orientation, microwave structure size, signal coupling circuits, and pump coupling circuits in different amplifiers. Once optimized, the pump frequency should be held constant within 1 MHz. The effects of pump frequency and amplitude changes on maser performance have been reported previously (Refs. 1 and 2). Improved maser stability achieved by pump frequency modulation (described in Ref. 2) has been implemented in some masers operating at S-, X-, and Ku-band frequencies. The optimum pump power level for these masers is between 100 and 200 mW.

The selection of pump sources for maser systems used in the DSN is influenced by many considerations. A 200-mW output power capability is desirable. 50-MHz electronic tunability is required in most applications; 200-MHz to 4-GHz tunability is advantageous in some systems. High input voltage requirements result in the use of expensive power supplies and antenna cables (systems now in use have 800-volt klystron beam voltage capability). Information about cost, availability, life expectancy, operating history, and stability is also considered in the selection of maser pump sources.

III. Pump Source Types

An impatt noise generator was used to pump an S-band maser in the laboratory. The Varian VSU-9560N produced more than 200 mW total integrated noise power between 12.63 and 12.75 GHz. The gain and noise temperature of the maser (when "noise pumped") measured the same as when the maser was pumped with a klystron. Additional tests of noise amplitude stability, load impedance change effects, environmental effects, and repeatability of the output noise spectrum in several units will be required before a determination of field worthiness can be reached.

Impatt oscillators operating between 12.5 and 13 GHz are in use for maser tests in the laboratory. These simple, easy to use oscillators are useful where maser performance can be optimized by mechanical tuning. Limitations of electronic tunability and frequency instability are reasons for not using impatt oscillators in the field at the present time.

A voltage-controlled crystal oscillator with a solid-state multiplier produced more than 200-mW power and

was tunable from 12.66 to 12.72 GHz. The temperature coefficient of power measured -0.08 dB/°C between 40 and 60°C, -0.03 dB/°C from 20 to 40°C, and less than 0.01 dB/°C from 0 to 20°C. The maximum temperature coefficient of frequency was 2.4 kHz/°C at 55 to 60°C; 0.2 kHz/°C was measured between 10 and 20°C. This solid-state source was used with a 2295-MHz maser in the field for a period of one year. No degradation in maser performance was detected during the year. The oscillator/multiplier assembly is eight times the cost of a klystron which gives comparable maser performance.

Backward-wave oscillators have been used in the laboratory as pump sources at frequencies between 26.5 and 90 GHz. Performance characteristics and life test data to 18,000 hours have been reported by Dr. Gross in 1971 (Ref. 3). Backward-wave oscillator types used at JPL are: Siemens Model RWO 40, RWO 60, and RWO 90. High costs and high input voltage requirements (2600 V) have resulted in limited use of these tubes. Antenna installation is being considered only for the 14.3- to 16.3-GHz maser where week-to-week retuning is a requirement.

Varian VA-246E reflex klystrons are used in 14 maser systems (2270–2300 MHz signal frequency). These tubes provide more than 200 mW within an electronically tunable range of 12.66 to 12.72 GHz. The typical frequency/temperature coefficients are -70 kHz/°C. Warranted tube life is 1000 hours. Average tube life in the field is 8000 hours.

A more versatile klystron, with longer life, is now used with a tunable maser (2240–2420 MHz). The klystron (VA-287P) has a 5000-hour warranted life. Output power can be adjusted with beam voltage from 25 to 1000 mW. A long-life choke-type tuner is motor driven to cover the entire maser tuning range. The klystron tunes from 12.5 to 13.0 GHz. Resettability of the mechanical tuning system is within 5 MHz. The electronic tuning range is 70 MHz and the frequency/temperature coefficient is -50 kHz/°C. The system has been in continuous use on the 64-m antenna for 9 months. The system is tuned for signal frequencies of 2295 and 2388 MHz on a weekly basis. No degradation in maser performance has been detected during the 9-month operation. A VA-287N without a tuning motor has been operating continuously in the field without noticeable degradation for more than 2 years.

A pump package using two klystrons in push-push operation is shown in Fig. 1. A block diagram of the

package is shown in Fig. 2. Figure 3 shows the loss through isolators, filters, and a power combiner as a function of frequency; the paths are as indicated by letters A, B, and C on Fig. 2. An explanation of push-push pumping and a maser description (using this technique) has been published in previous reports (Refs. 4 and 5). The klystron used in the 35- to 40-GHz range is a Varian VA-302. Three tubes of this type, presently used in the field, have demonstrated more than 5000 hours of life without noticeable degradation (warranted life is 2000 hours). The VA-302 must be mechanically retuned (at the antenna package) or replaced to accomplish a maser frequency change. The klystron used in the 25- to 28-GHz range is a Varian EM-1138. Warranted life is 5000 hours.

Figure 4 shows a pump package for a tunable X-band maser using the push-push pumping scheme. Two EM-1138 klystrons are remotely tuned to cover a 500-

MHz portion of the maser's tunable range (7700-8600 MHz). The block diagram is shown in Fig. 5. Full waveguide bandwidth circulators (18.0 to 26.5 GHz) are used as isolators and as a power combiner. Total loss, from klystron to maser connections, is shown in Fig. 6.

IV. Concluding Remarks

Today the reflex klystron is used as a pump source for every maser amplifier operating in the Deep Space Network. New solid-state devices will be tested to determine future usefulness as pump sources. Extended maser tuning ranges present the most difficult requirements for pump sources of any type. A new pump device must (at reasonable cost) exceed the high-performance level achieved by today's klystrons if the device is to be used in the DSN.

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Table 1. Pump sources used with JPL masers

Maser frequency, MHz	Pump frequency, GHz	Pump device	Where used ^a	Number of systems
960	10.6	Klystron	Field	4
1420	11.2	Klystron	Lab	1
2270-2300	12.66-12.72	Klystron	Field	28
2270-2300	12.66-12.72	Multiplier	Field	1
2270-2300	12.66-12.72	Impatt oscillator	Lab	2
2270-2300	12.66-12.72	Impatt noise generator	Lab	1
2388	12.87	Klystron	Field	3
2295/2388	12.7/12.87	Klystron	Field	4
2240-2420	12.5-13.0 ^b	Klystron	Field	1
8488	21.85	Klystron	Field	2
7700-8600	41-43.8 ^c	Klystron	Field	1
7700-8600	18.4-19.4 and 22.6-24.6 ^b	Klystrons	Lab	1
7600-8900	40-45	Backward-wave oscillator	Lab	1
14,300 to 16,300	25.4-27.8 and 35.4-39.3 ^c	Klystrons	Lab	1
12,500 to 18,000	26.5-40 40-60 60-90	Backward-wave oscillators	Lab	1

^aField use is in the DSN on 26-m or 64-m antennas; lab use is at JPL for development or test purposes.

^bPump range is covered by tuning motor with remote control.

^cPump range is covered by replacement and mechanical tuning of klystrons.

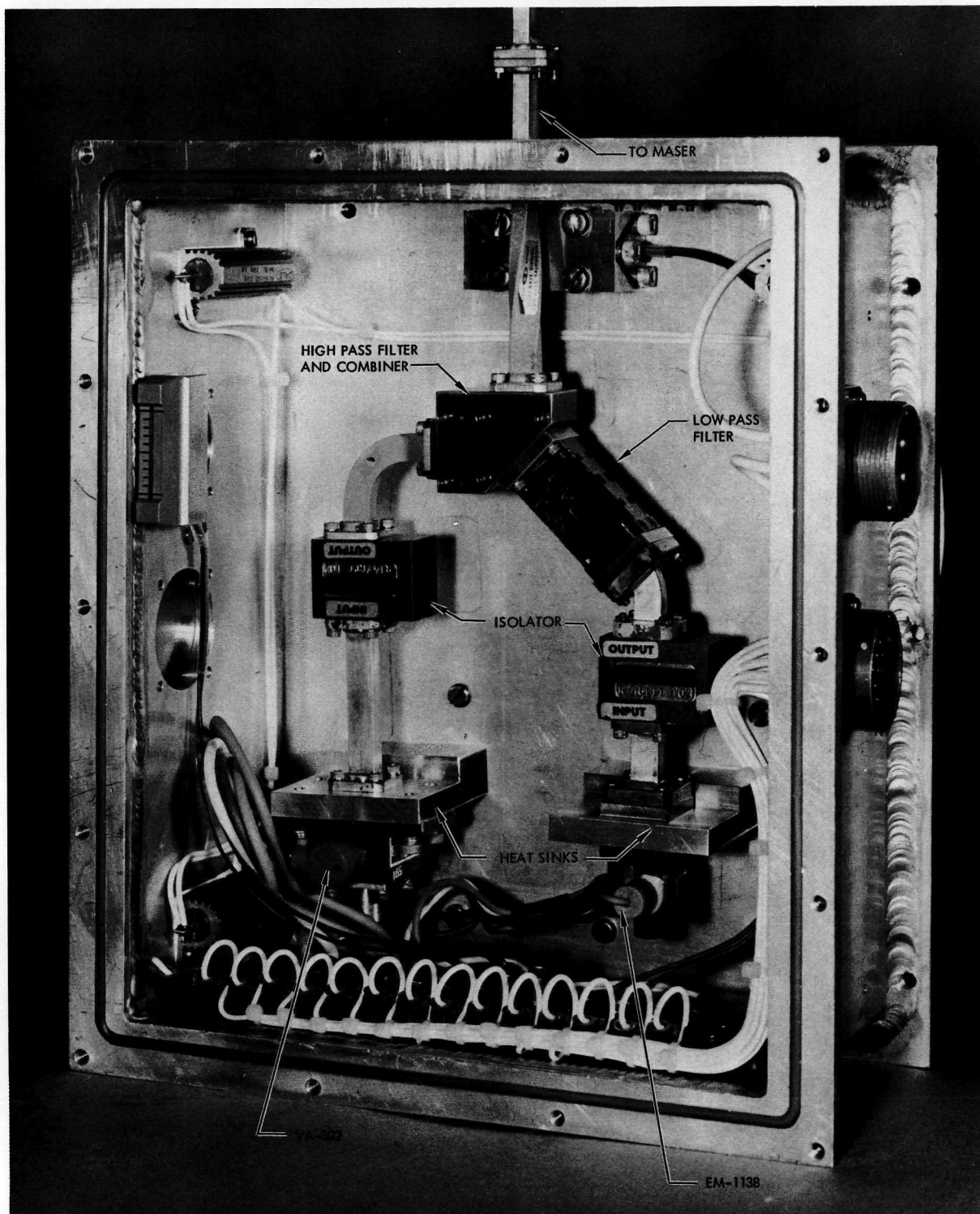


Fig. 1. Pump package for 14.3 to 16.3 GHz maser

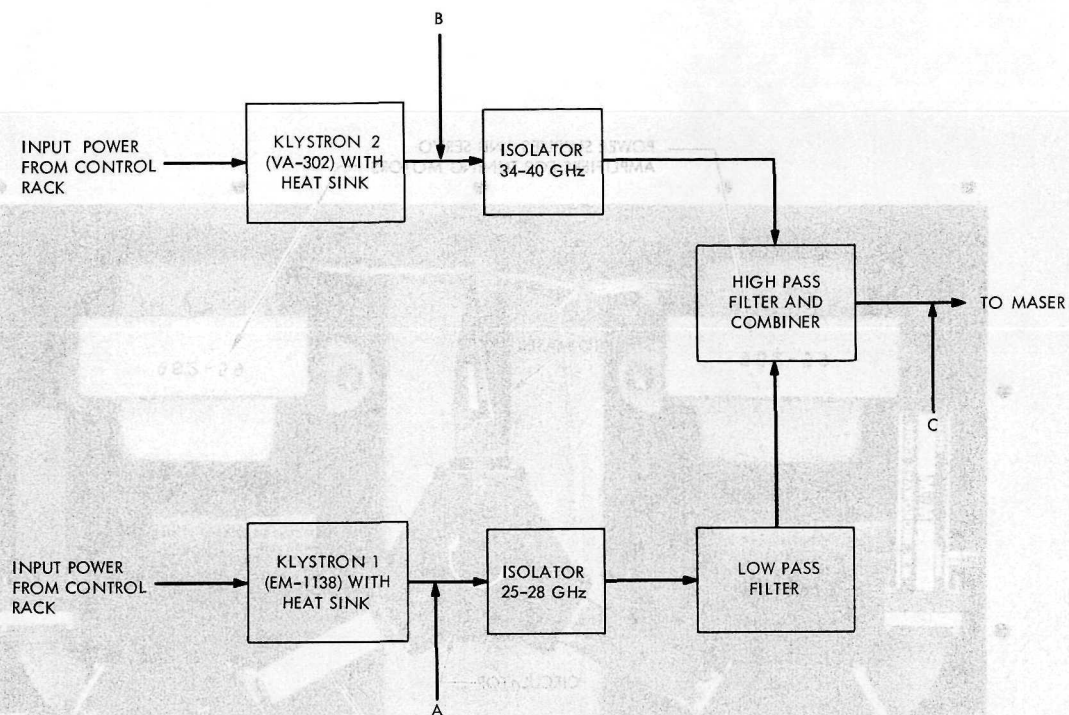


Fig. 2. Block diagram for 14.3 to 16.3 GHz maser pump package

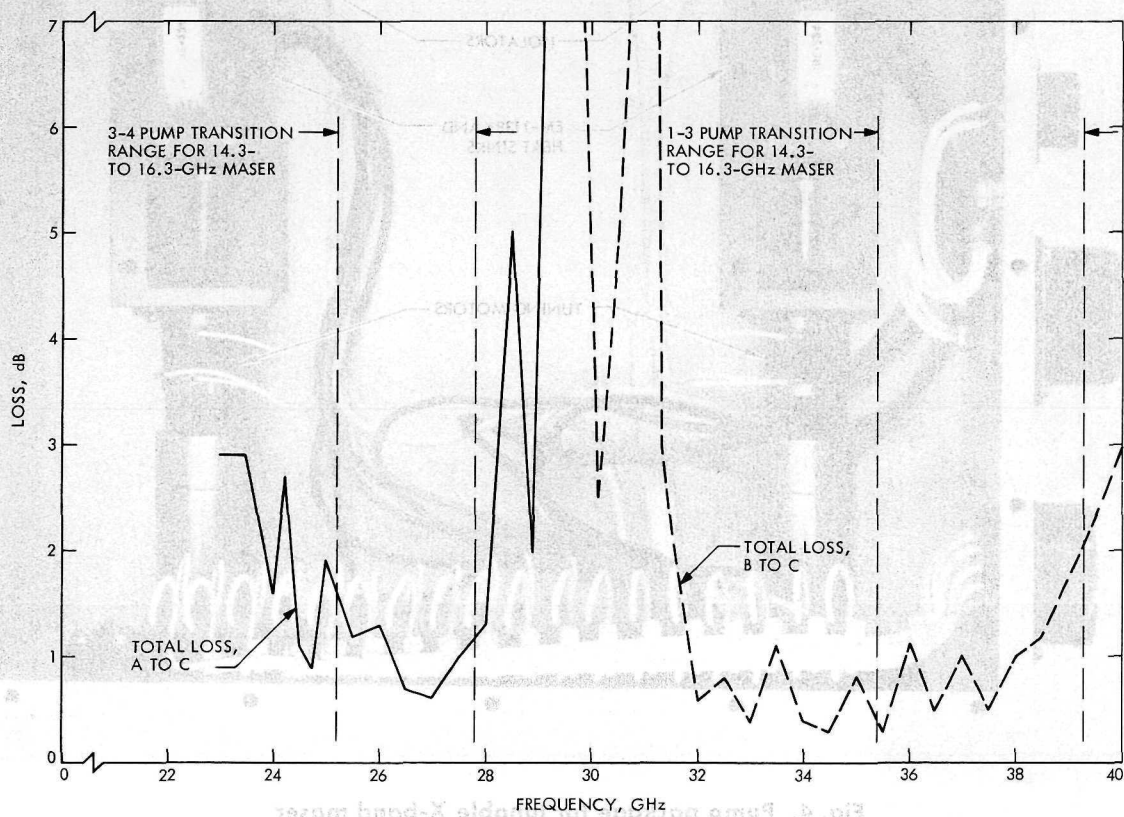


Fig. 3. Loss vs frequency for 14.3 to 16.3 GHz maser pump package

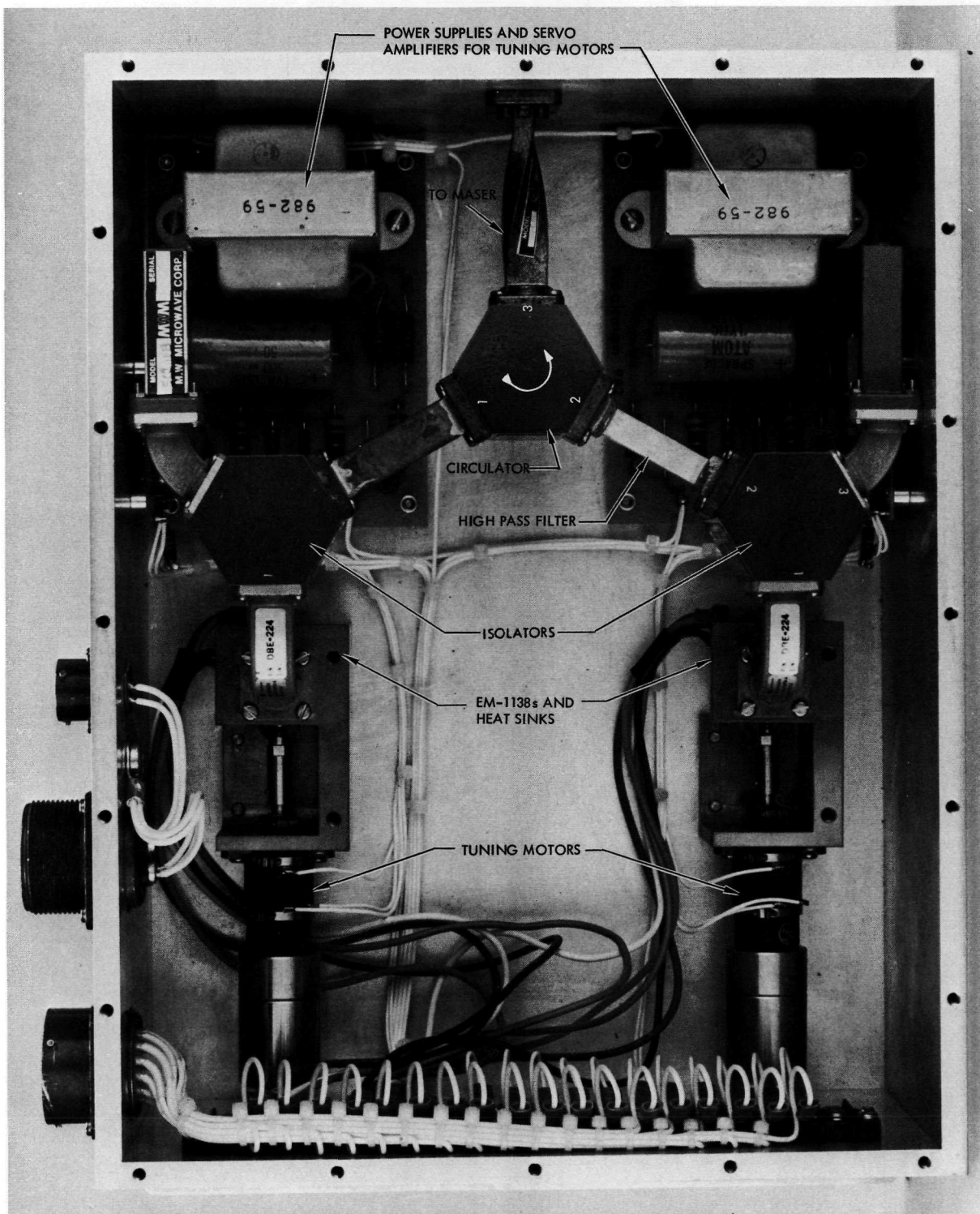


Fig. 4. Pump package for tunable X-band maser

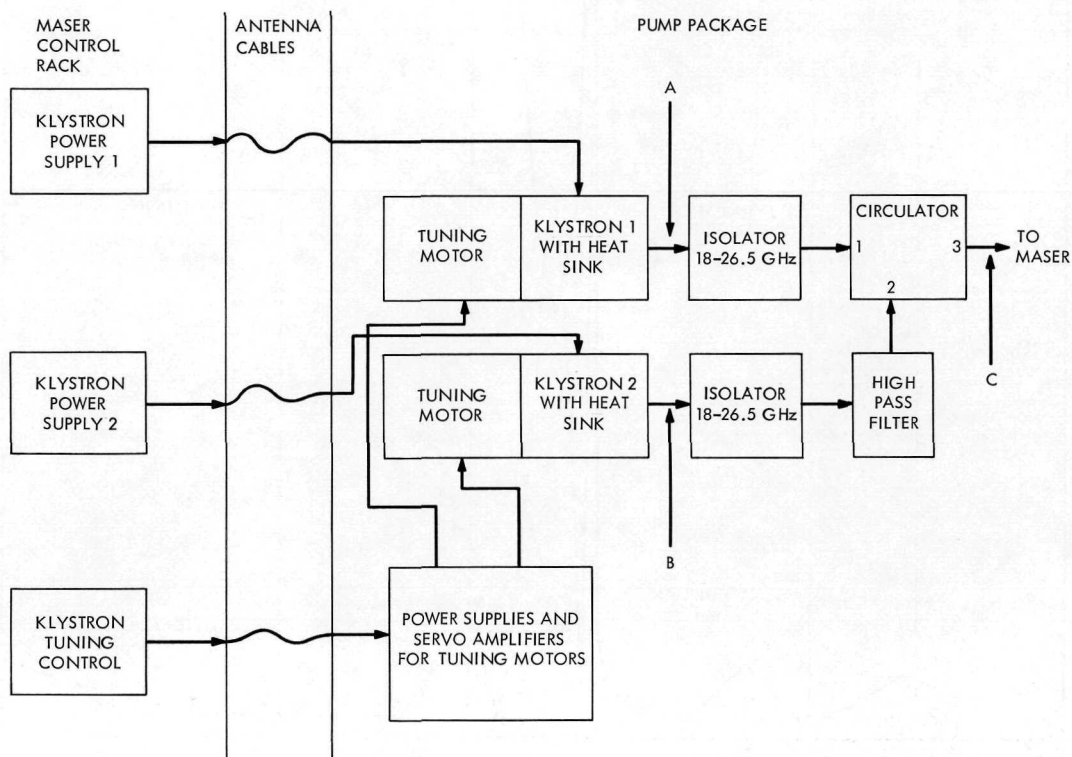


Fig. 5. Block diagram for tunable X-band maser pump package and control

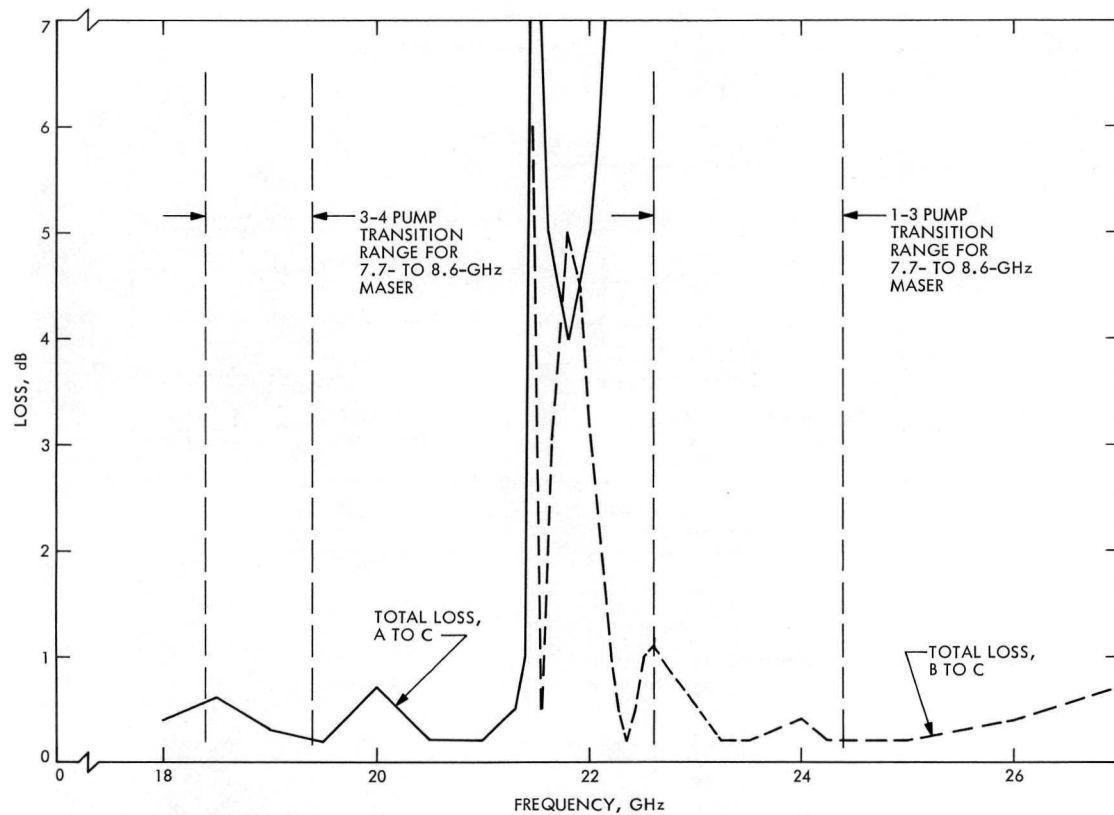


Fig. 6. Loss vs frequency for tunable X-band maser pump package

Radio Source Calibration Program (RASCAL) — Phase I: Antenna Gain Calibration

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A new program for measuring antenna gain of the large DSN antenna is described. The gain measurement procedure is outlined. Improvements over past techniques have resulted in better knowledge of Gain Standard Horn calibrations, in more compact procedure, and in changes in the precision comparison attenuator. The gain accuracy goal of the primary station is ± 0.05 dB, 1σ .

I. Introduction

JPL has used tracking of well-known radio sources as a means of measuring the aperture efficiency of its large DSN antennas for the past several years. Recently, a technique to establish a firmer foundation for these measurements has been undertaken. This new technique employs a horn antenna as a primary gain standard. (This gain standard is presently being subjected to an absolute gain calibration in cooperation with the National Bureau of Standards.)

The first phase involves using the Moon-based ALSEP (Apollo Lunar Surface Experiments Package) as a far-field beacon to transfer the horn calibration to the 26-m-diameter antenna at DSS 13, Goldstone. The second phase uses the 26-m antenna to precisely measure the absolute flux density of Cygnus A. Once the radio source has been "calibrated" by the primary station, the resulting value can be used by any secondary station to measure its antenna efficiency. The primary station effort has been given the acronym RASCAL for Radio Source Calibration.

II. Functional Description

A block diagram is shown in Fig. 1. Conceptually, the procedure in obtaining a single gain data point is:

- (1) Boresight the 26-m antenna (the beam of the Gain Standard Horn (GSH) is parallel to the 26-m antenna).
- (2) Phase-lock the receiver to the ALSEP carrier and note the automatic gain control (AGC) voltage.
- (3) Phase-lock the receiver to the test transmitter (50 kHz above ALSEP) and adjust the test transmitter signal to achieve the same AGC noted in Step 2 using the RF attenuators.
- (4) Switch to the GSH, again phase-lock the receiver to the ALSEP carrier and note the AGC voltage.
- (5) Again, phase-lock the receiver to the test transmitter and, using the RF attenuators, adjust the signal to achieve the same AGC noted in Step 4.

The gain of the 26-m antenna is equal to the gain of the GSH, plus the attenuation difference between Steps 3 and 5, less the differential waveguide loss between antennas:

$$G_{26} = G_{\text{GSH}} + \Delta\alpha - \alpha_{\text{WG}} \quad (1)$$

Figure 2 shows the Gain Standard Horn mounted on the 26-m antenna at DSS 13.

III. Improvements in Absolute Gain Calibration

An important improvement since the antenna gain calibration of Ref. 1 has been the improved absolute calibration of the Gain Standard Horn (Ref. 2). This subject will be covered in detail in a separate article. Briefly, it is expected that the old calibration uncertainty of ± 0.13 dB (1σ) will be reduced to approximately ± 0.033 dB (1σ).

In the test of Ref. 1 the RF attenuator used was an S-band rotary vane attenuator. While this is an excellent laboratory tool, its use for this application showed several problem areas. The device demonstrated a position sensitivity. A temporary remote drive readout mechanism was necessary. Finally, the field use of this precise laboratory

device was felt to be undesirable. For these reasons, the rotary vane device has been replaced with a fixed switchable step attenuator plus a series vernier attenuator. The attenuation of the step attenuator was adjusted during fabrication to the expected gain difference between the large paraboloid and the Standard Horn, nominally 31 dB.

The vernier attenuator is a PIN diode modulator used in a duty-cycle-switching mode, i.e., the modulator is biased on and the average RF attenuation is increased by turning it off with pulses at a 4-kHz rate. The width of the pulses can be digitally adjusted so that the RF duty cycle and, hence, the average RF power correspondingly changes. The device is a modified form of that described in Ref. 3. These attenuators will be discussed in detail in a later article.

IV. Goal

The goal of the first phase of RASCAL is to determine the absolute antenna gain of the primary station antenna at DSS 13 to an accuracy of ± 0.05 dB, 1σ . The effort will be a continuous one since improvements are scheduled to be made in the antenna, and the RASCAL program will be used to evaluate these improvements.

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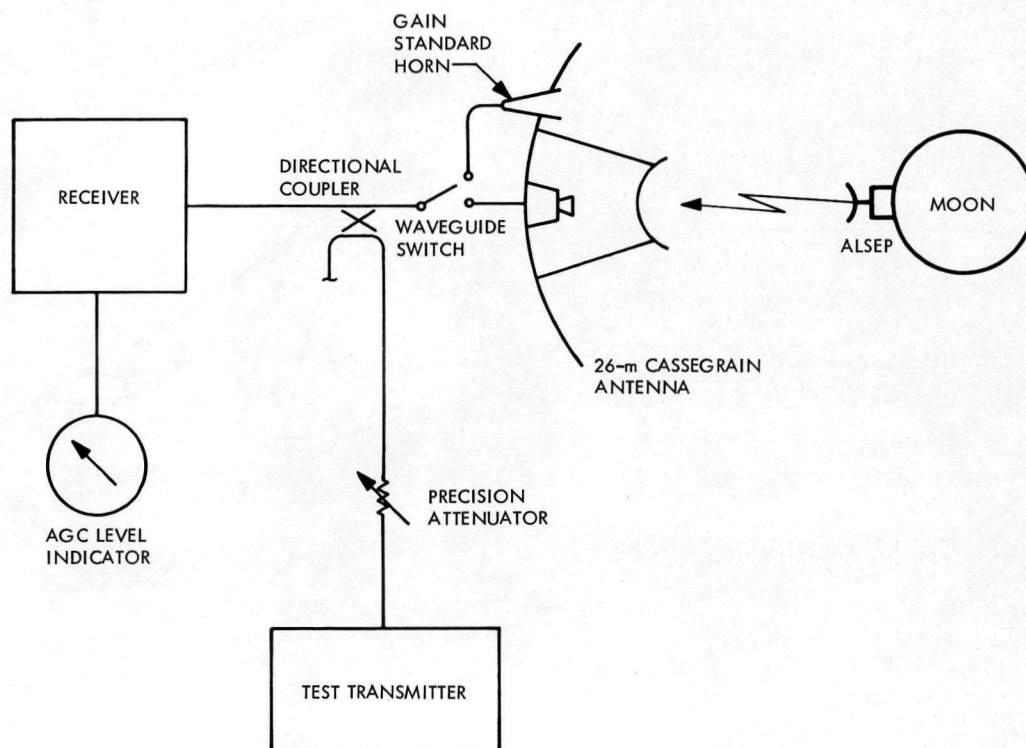


Fig. 1. Gain block diagram

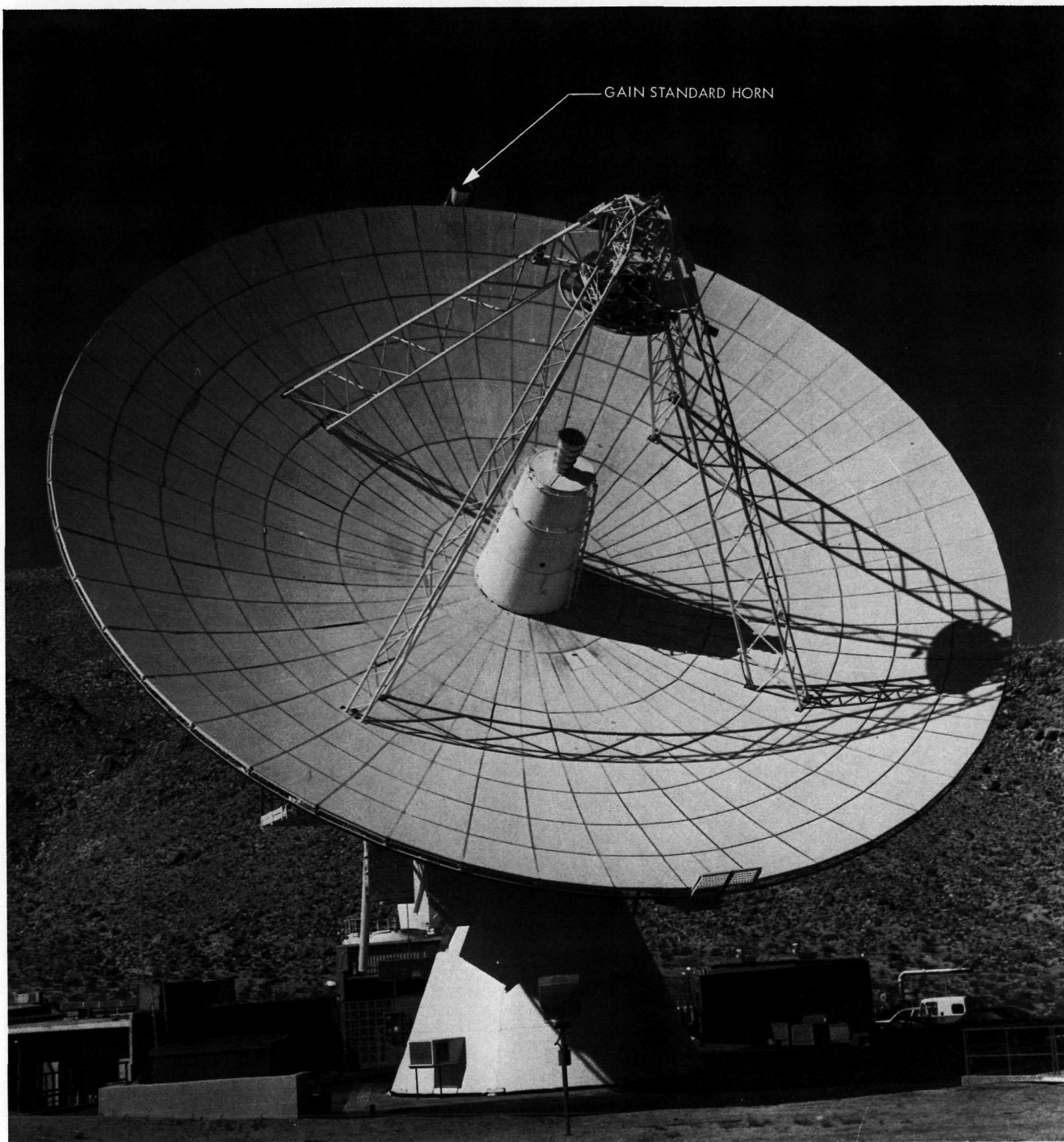


Fig. 2. DSS 13 26-m antenna with mounted Gain Standard Horn

III. Power Loss in the Flat Plate

Because of the importance of RF heating of the flat plate and the difficulty of accurate field measurements of this effect, a new computer program, CUMVEX, has been recently completed, to accurately calculate the power incident on and absorbed in any general quadratic surface illuminated by an arbitrary field. Near-field effects are taken account of by spherical wave techniques. Figure 4 shows the power distribution profile in the H-plane (plane of the paper in Fig. 1) and Fig. 5 shows the profile in the E-plane. A total power of 400 kW at frequency of 2.115 GHz and a pure copper reflector are assumed. It can be seen that, due to the focusing action of the ellipsoid, the power distribution is mainly in a small central "hot spot". It is presently planned that data such as those in Figs. 4 and 5 will be utilized to perform laboratory heating and surface distortion tests.

S- and X-Band RF Feed System

P. D. Potter

Communications Elements Research Section

In support of the Mariner 1973 X-band experiment, it is necessary to implement a dual-frequency microwave feed system for the DSS 14 64-m-diameter antenna. To fulfill this requirement, a particularly attractive approach, the reflex feed system, is being implemented. The reflex feed configuration and the analytical techniques used for its analysis were described in a previous report. This article describes the calculated gain performance of the system at S-band and discusses the heating of the reflex feed dichroic reflector caused by high-power S-band transmission.

I. Comparison of Measured and Computed Feed System Radiation Patterns

A cross-sectional view of the reflex feed system geometry is shown to scale in Fig. 1. The analytical technique used to predict the S-band radiation patterns of this system was described in a previous reporting (Ref. 1), and a comparison of measured and calculated radiation patterns was presented for feed configuration number 1. Figure 2 shows the final configuration (number 3) E-plane measured and calculated patterns; Fig. 3 shows the H-plane measured and calculated patterns. The analytical technique utilized for these patterns differs somewhat from that previously described in that the ellipsoid scattered fields are expanded about the Point I (Fig. 1), rather than the phase center C. By using the Point I, the flat plate is kept outside of a sphere containing all of

the sources located on the ellipsoid surface and in the horn aperture. By maintaining this condition, the spherical wave expansion is rigorously correct. For the calculated patterns shown in Figs. 2 and 3, three azimuthal modes ($m = 0, 1$, and 2) and sixty polar modes were utilized.

Table I gives the gain calculation results for the reflex feed system with a spherical reflector. It can be seen that the calculated gain is approximately 0.5 dB above the measured gain. This difference is due to the neglected surface deformation loss of the planar reflector. This deformation is caused by gravity and by non-uniform heating from the high power S-band transmission. The best section describes the calculated power loss in the flat plate which gives rise to physical distortion of the flat plate.

the sources located on the ellipsoid surface and in the horn aperture. By maintaining this condition, the spherical wave expansion is rigorously correct. For the calculated patterns shown in Figs. 2 and 3, three azimuthal modes ($m = 0, 1$, and 2) and sixty polar modes were utilized.

II. Calculated Antenna Gain at S-Band

Using the digital antenna pattern (DAP) recording system in the 60-ft anechoic chamber, complete feed data were taken at the 2.295-GHz scale-model frequency. Data were taken at 1-deg increments in polar angle and 15-deg increments in azimuthal angle. After processing by the DAP software, the patterns were resolved into azimuthal Fourier component patterns, and the total pat-

tern power was calculated. Of the total pattern power, 98.8% was in the first three azimuthal modes; $m = 0$, 1, and 2. Next, the fraction of the $m = 0$, 1, and 2 mode energy intercepted by the tricone subreflector, relative to the total feed power, was calculated and defined as the forward spillover ratio. Then, each of the three m patterns was expanded in spherical waves. Each of these expansions was separately scattered off the tricone subreflector. The three scattered patterns were vectorally added and used to compute various efficiency components.

Table 1 gives the gain calculation results for the reflex feed together with a similar calculation for the present standard feed. It can be seen that the reflex feed degrades performance by approximately 0.15 dB. Almost two-thirds of this loss is due to the estimated surface deformation loss of the planar reflector. This deformation is caused by gravity and by non-uniform heating from the high power S-band transmission. The next section describes the calculated power loss profile in the flat plate which gives rise to physical distortion of the flat plate.

III. Power Loss in the Flat Plate

Because of the importance of RF heating of the flat plate and the difficulty of accurate field measurements of this effect, a new computer program, *CURRENT*, has been recently completed¹ to accurately calculate the power incident on and absorbed in any general quadric surface illuminated by an arbitrary field. Near-field effects are taken account of by spherical wave techniques. Figure 4 shows the power dissipation profile in the H-plane (plane of the paper in Fig. 1) and Fig. 5 shows the profile in the E-plane. A total power of 400 kW, a frequency of 2.115 GHz, and a pure copper reflector are assumed. It can be seen that, due to the focusing action of the ellipsoid, the power dissipation is mainly in a small central "hot spot." It is presently planned that data such as those in Figs. 4 and 5 will be utilized to perform laboratory heating and surface distortion tests.

¹By Richard Norman, JPL Communications Elements Research Section.

Reference

1. Potter, P. D., "S- and X-Band RF Feed System," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VIII, pp. 53-60. Jet Propulsion Laboratory, Pasadena, Calif., Apr. 15, 1972.

Table 1. Reflex and standard feed gain, 2.295 GHz

Factor	Standard feed		Reflex feed	
	Ratio	dB	Ratio	dB
Forward spillover	0.94470	-0.2471	0.96982	-0.1331
Rear spillover	0.99738	-0.0114	0.99779	-0.0096
Non-uniform amplitude illumination	0.84207	-0.7465	0.82423	-0.8395
Non-uniform phase illumination ^a	0.97999	-0.0878	0.98408	-0.0697
Cross polarization	0.99982	-0.0008	0.99876	-0.0054
Energy ($m \neq 1$)	0.99805	-0.0085	0.97968	-0.0892
Central blockage ^a	0.94148	-0.2619	0.94195	-0.2597
Quadripod blockage	0.87498	-0.5800	0.87498	-0.5800
Paraboloid/subreflector surface tolerance loss (0.1524 cm rms)	0.97876	-0.0932	0.97876	-0.0932
Ellipsoid surface tolerance loss (0.0508 cm rms)	—	—	0.99762	-0.0103
Planar reflector surface tolerance loss (0.1524 cm rms)	—	—	0.97876	-0.0932
Transmission loss through planar reflector (-23 dB)	—	—	0.99499	-0.0218
Total	0.62557	-2.0372	0.60191	-2.2047
Gain for 100 % efficiency	2.366795 $\times 10^6$	63.7416	2.366795 $\times 10^6$	63.7416
Gain	1.480608 $\times 10^6$	61.7044	1.424590 $\times 10^6$	61.5369

^aPhase and central blockage factors are based on a standard feed subreflector focus position of 0.928 cm in and a reflex feed subreflector position of 0.046 cm out.

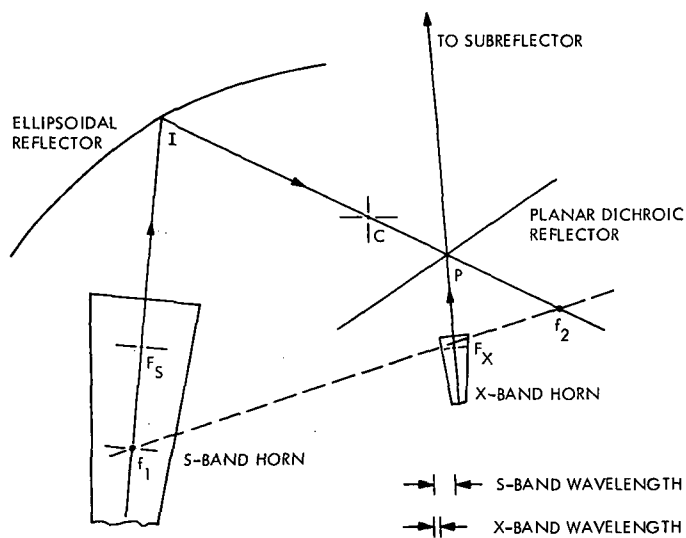


Fig. 1. Reflex feed system

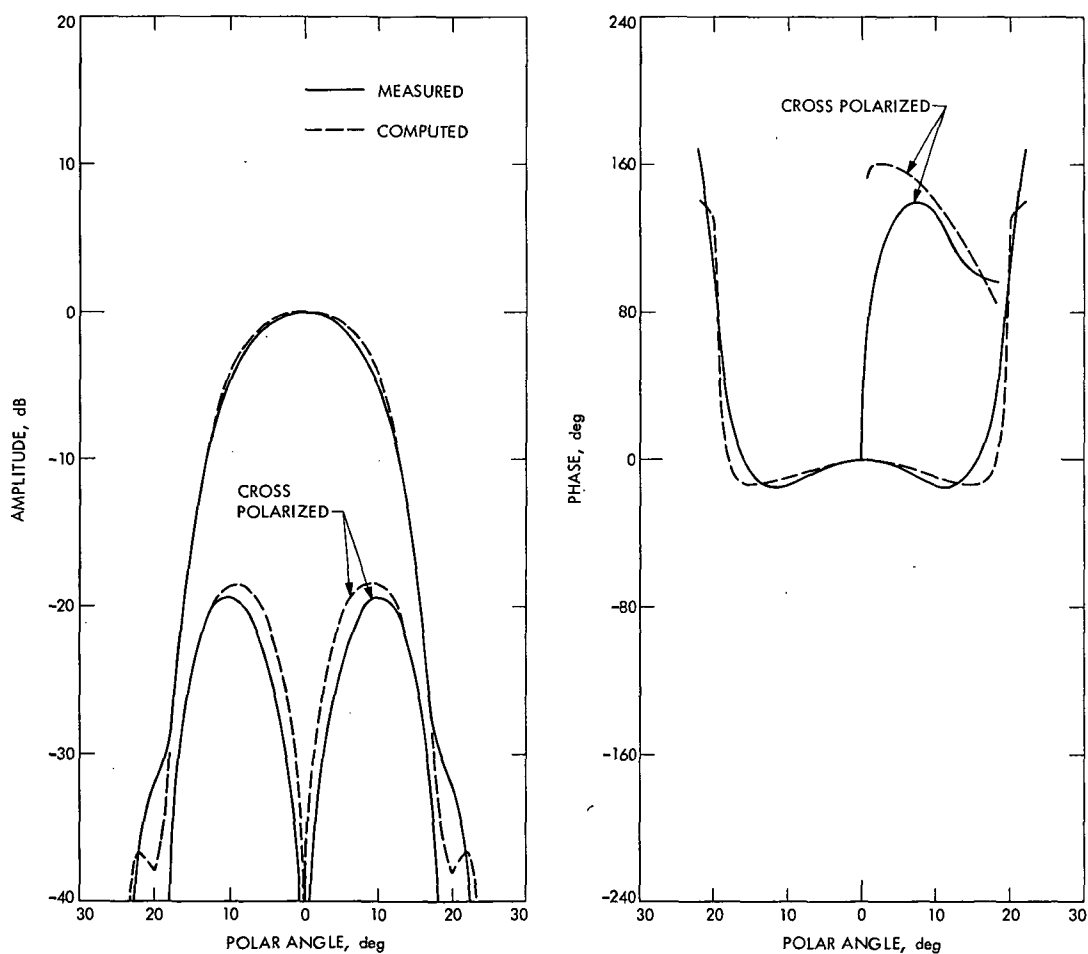


Fig. 2. E-plane reflex feed patterns

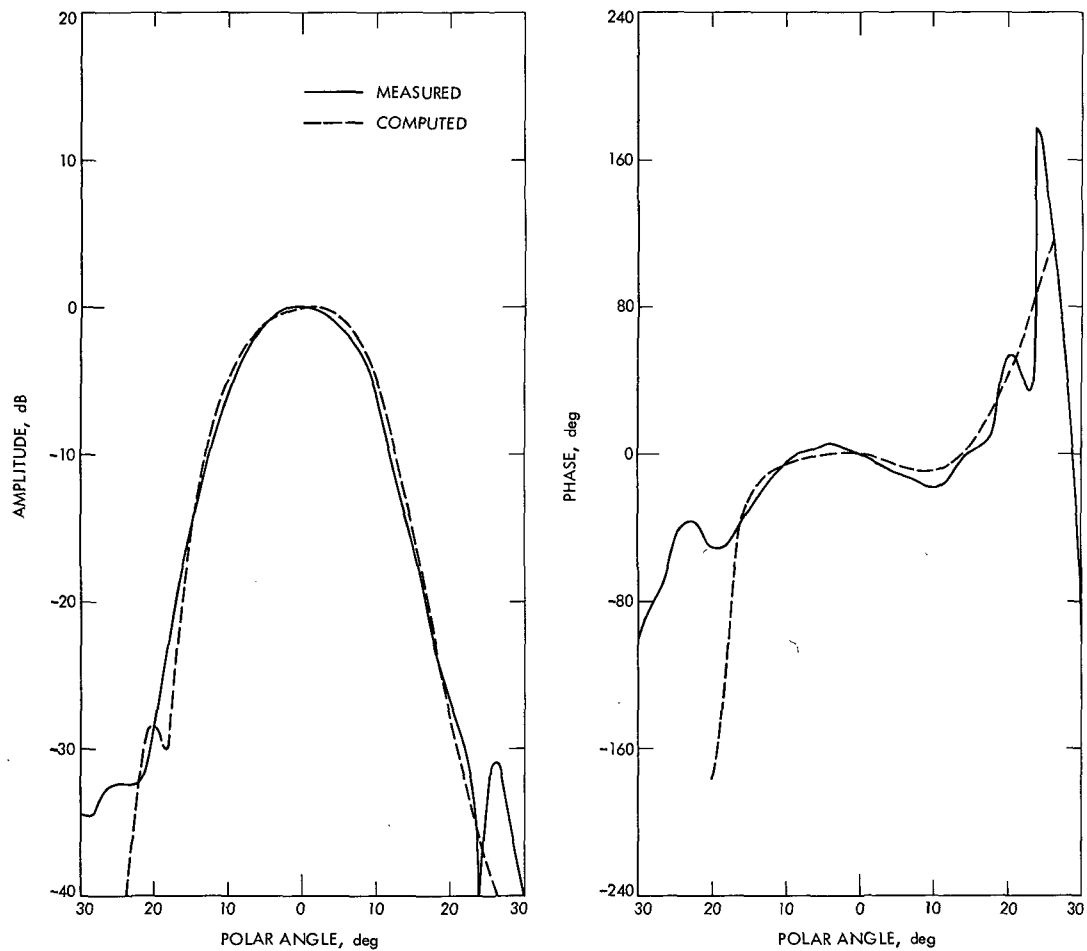


Fig. 3. H-plane reflex feed patterns

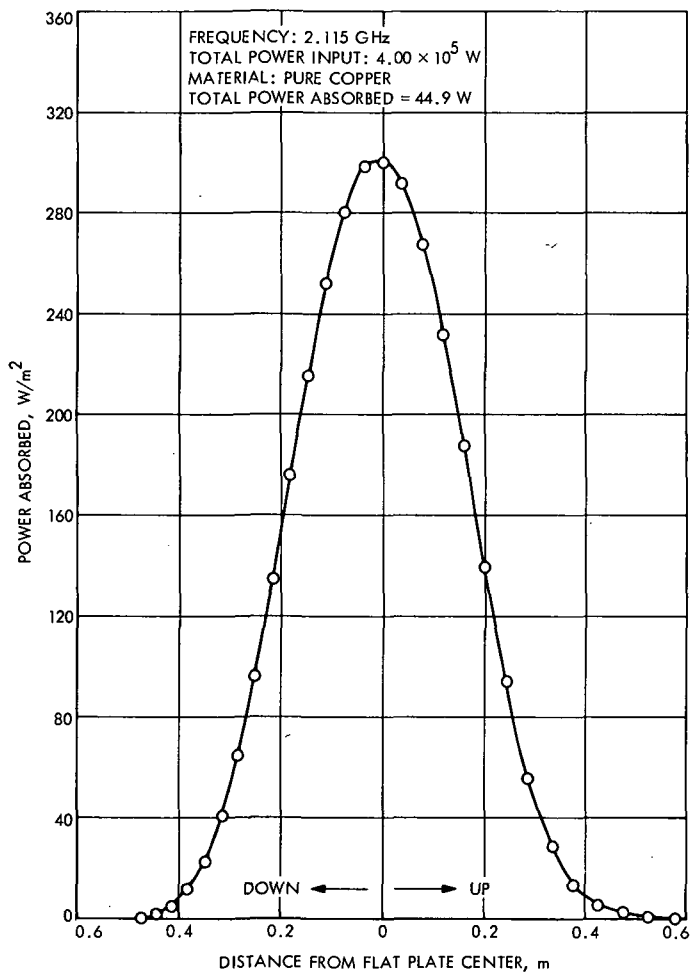


Fig. 4. H-plane flat plate power dissipation profile

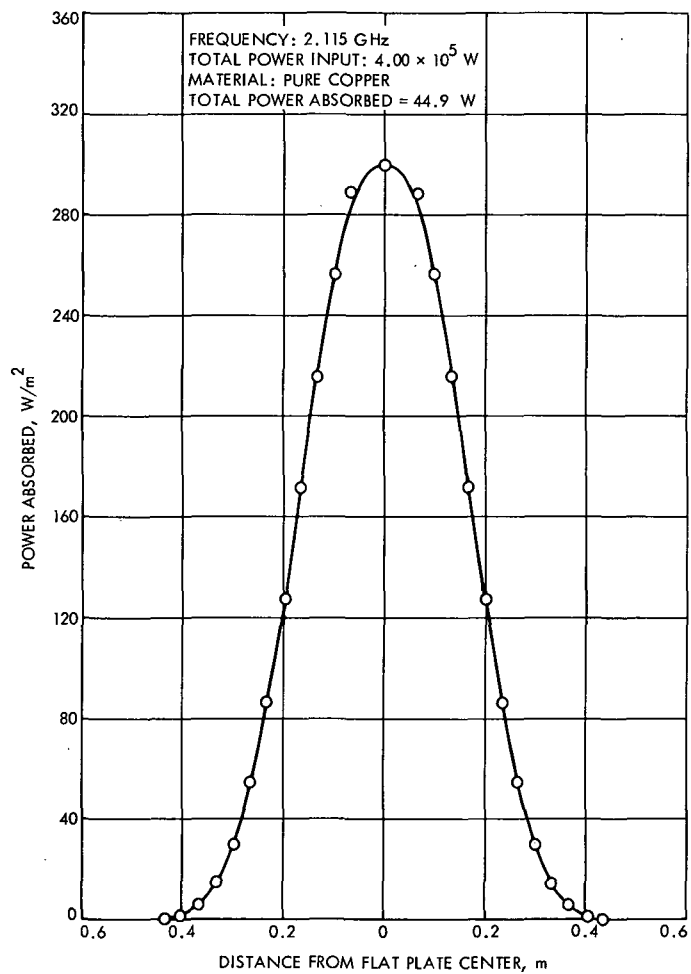


Fig. 5. E-plane flat plate power dissipation profile

DSN Research and Technology Support

E. B. Jackson and R. B. Kolbly
R. F. Systems Development Section

The activities of the Development Support Group, including the Microwave Test Facility, during the two-month period ending April 15, 1972 are summarized. Activities include operational clock synchronization, precision antenna gain measurement, weak source observation, pulsar observation, tricone support structure testing, and planetary radar preparation and execution. Activities at the Microwave Test Facility include special klystron testing and tuning for the Manned Spaceflight Tracking and Data Network, special part fabrication for the tricone support structure, and design and fabrication of the flow panel and crowbar subassemblies for the clock synchronization transmitting system. Significant maintenance items include replacement of the azimuth drive gear reducer on the 26-m-diameter antenna and modification of the power distribution system associated with the 100-kW clock synchronization transmitter.

During the two months ending April 15, 1972, the Development Support Group was engaged in the following activities.

I. DSS 13 Activities

A. In Support of Section 331

1. Pulsars. The Venus Deep Space Station (DSS 13) continues to devote approximately twenty-four hours per week (a total of 182 hours during this period) to the observation of pulsars. Information obtained includes pulse-to-pulse spacing, pulse time of arrival, and pulse shape. Pulsars regularly observed (about 22 of the 50 known pulsars) were tabulated in Ref. 1.

2. Planetary radar. In preparation for the Mercury-Venus planetary radar observations, the 400-kW development transmitter (2388 MHz), which had been removed from DSS 14 in late 1971, was completely tested at the Venus station and reinstalled at DSS 14. The development receiver at DSS 14 was modified by adding a new wide band "front end" converter, which operates from 2290 to 2390 MHz, with intermediate frequencies of 30 and 2.5 MHz (double conversion). Phase-lock capability is not provided and first local oscillator frequency control is accomplished with a programmed oscillator.

Manual gain control is provided in the 30-MHz portion of the receiver with a local control at the DSS 14 64-m-diameter antenna pedestal control room, while a remote

control is provided at DSS 13 via telephone lines. The 2.5-MHz intermediate frequency output is typically connected to the Venus station via the microwave link for signal processing.

To facilitate generation and control of ranging modulation for the transmitter in these observations, the Station Control and Monitor (SCAM) at the Venus station was modified and reprogrammed to provide real-time evaluation of the range polynomial. Previously the range polynomial had been evaluated "off line" with a large computer, and the range as a function of time had been punched onto paper tape at 60-second intervals. The generation and handling of this tape was not only burdensome, but the tape reader represented a significant portion of the computer failures. Real-time polynomial evaluation not only saves time and effort, but also provides a measurable increase in reliability.

These changes were tested on April 7, 1972 when the planet Mercury was successfully ranged on the first attempt using a pseudonoise (PN) code having a digit period of 10 microseconds, resulting in a range resolution of 750 m, two-way, without interpolation.

3. Hydrogen maser installation. In preparation for planned interferometer experiments in cooperation with DSS 14, a hydrogen maser, installed in a special trailer, has been placed just south of the Operations Building (G-51) and provisions made for hooking into the station's Central Frequency Synthesizer. (The trailer blocks the operator's view of the 9-m antenna so a closed-circuit television system was installed to allow the operator to see the 9-m antenna and the surrounding area to ensure safety during operation of the 100-kW X-band transmitter.)

B. In Support of Section 332

1. Tricone support structure (TCSS). The TCSS destined for DSS 61A has been completely tested, including testing at 400-kW radio frequency of all components which are designed to handle that power level. The feed cone used for testing has been dismantled, packed, and shipped to DSS 61A. The remainder of the TCSS will be dismantled and shipped, in conjunction with the subreflector for the 64-m antenna, in late June of 1972.

2. 26-m antenna azimuth drive maintenance. The 26-m antenna is normally driven in azimuth by four hydraulic motors individually driving the azimuth drive gear through gear reducers having a reduction ratio of 239.96. The hydraulic pressure on these motors, arranged in pairs, is controlled so that two drives "lead" and two

"lag," thus providing reduced backlash operation and reversal. In August 1970 one of the gear reducers failed and was removed, and operation continued on an unbalanced arrangement of two and one. In September 1971 the system was balanced by the removal of a second gearbox, and operational limitations were imposed which required cessation of tracking at wind velocities of 72 km/h (45 mi/h) and "stowing" the antenna in the zenith look position. With all four gearboxes connected, tracking had been permitted at wind speeds up to 80 km/h (50 mi/h).

In March 1972 one of the two remaining gearboxes developed failure symptoms and was replaced to avoid possible catastrophic failure. Removal and replacement of this gearbox was accomplished in 3½ days of sustained effort by personnel of the Development Support Group. The removed gearboxes have been returned to the manufacturer for repair as necessary.

C. In Support of Section 333

1. Precision antenna gain measurements. Continuing this important development project, extensive data taking continues with Cygnus A and the *Apollo* Lunar Surface Experiments Package (ALSEP) as sources. While phase-lock-tracking the ALSEP transmitter, received signal strength ratios are established between the 26-m antenna and the gain standard horn. After correction for differential path losses in the interconnecting waveguide, waveguide switches, and coaxial cables, a measurement of the absolute gain of the 26-m antenna is obtained in comparison to the gain of the gain standard horn whose gain has been carefully measured by the National Bureau of Standards (NBS). The observed system temperature of the radio source Cygnus A is then measured. After correction to an equivalent 100% efficient antenna temperature, Cygnus A can then be used by other DSIF stations to measure their antenna gain at the same frequency. During this period 98 hours were devoted to tracking Cygnus A and 124 hours to tracking ALSEP.

2. Weak source observation. Using almost completely automated data-taking procedures, measurements continue to be made of a number of radio sources and radio emissions from planets. The sources observed during this period are tabulated in Table 1, with 251 hours being devoted to tracking and 298 hours to equipment stability and "sky survey" measurements.

3. Faraday rotation. A long-term program (see Ref. 2) for collection of Faraday rotation data from geostationary satellite ATS-1 continues. Although other techniques for

obtaining ionospheric correction information have been proposed and tested, Faraday rotation data represent a developed technique whose accuracy has been ascertained and confidence established. These data can be used to provide corrections to observed doppler and range measurements made on spacecraft. Data collection at DSS 13 is automated and continues 24 hours per day, 7 days per week.

D. In Support of Section 335

1. Automated subsystem and system operational technique development. In a continuing development of automated subsystem and system operational techniques, a PDP-11 digital computer has been interfaced with the control circuitry of the 400-kW development transmitter in such a way that full start-up, operation, and status monitoring can be accomplished by the computer at the command of the operator. Extensive support has been given this effort under the direction of personnel from Section 335 at Pasadena. The effort during the past two months was focused on initial hook-up, development of suitable programming, and initial testing. At the present time the computer has approximately 100 combined input and output connections and monitors the values of all meters and makes comparisons with stored limits to ensure that ratings are not exceeded. Error messages are typed out as necessary when a command input by the operator brings any parameter to a stored limit. Development in this area will continue with the number of outputs and inputs to be expanded to include monitoring of the status of the various interlocks as well as provision of greater control capability.

E. In Support of Section 337

1. Clock synchronization transmissions. Under the scheduled control of DSN scheduling, and as constrained by the availability of a mutual Moon view period, regular clock synchronization transmissions are made to each of the overseas DSN stations with calibration transmissions being made to DSS 14 and the United States Naval Observatory (USNO). The number of transmissions for the two-month period ending April 9 is tabulated in Table 2. (Each transmission is 30 minutes in duration.)

II. Microwave Test Facility Activities

A. In Support of Section 332

1. Tricone support structure (TCSS). Fabrication of various brackets, waveguide spacers, and special machine shop support continues at a steady pace. However, this

effort is now finished with the completion of the final testing of the DSS 61A system.

2. Perimeter surveillance. A low key program, pursued on a noninterference basis, to provide perimeter surveillance at the Goldstone Space Communication Complex has been underway for some time. Basically, the concept calls for detecting the passage of a vehicle along approximately 24 of the desert roads leading into the Complex. The passage of a vehicle would initiate telemetering, via an inexpensive battery-powered transmitter, of the code assigned to that location which would then display at both the central security post and the mobile "roving patrol." By reference to an assignment sheet, the displayed two-digit number will be converted to a location, and the roving patrol will then investigate.

Suitable transmitters are available as "off the shelf" items, and control of power drain, design of rugged, inconspicuous vehicle detectors, and suitable telemetry encoding has drawn the most attention to date. Design of the detection/transmission/encoding unit is well along, and work on the receiver/decoder/display will start soon.

B. In Support of Section 333

1. Antenna panel noise burst generation. To reduce noise burst generation to a minimum, the joints between antenna surface panels are taped with metallic tape. To ensure that optimum results are obtained from this taping, a section of antenna with several surface panels has been set up at an approximate angle of 45 deg with the ground. These surface panels are irradiated from a standard Cassegrain feedcone which has been installed a few feet away in a horizontal position in a shipping cradle. The cone is fed by a 20-kW transmitter at 2110 MHz and receives with a maser at 2295 MHz via the usual diplexed arrangement. Total noise power output is recorded while various techniques of taping are tried and irradiated. Results of these tests will be used to choose a taping technique for the joints on the 64-m antennas.

C. In Support of Section 335

1. Clock synchronization transmitter. Design and construction of a water flow monitor panel and low (1 kV) voltage crowbar continues.

2. Transmitter development. The continuing testing of the 400- and 20-kW transmitters at DSS 13 requires fabrication of various support bracketry, special chassis, connectors, etc. Additionally, the machine shop has supported the interfacing of the PDP-11 computer with the development 400-kW transmitter.

D. In Support of Section 337

1. *Acceptance klystron testing.* In preparation for the *Apollo 16* flight, a 20-kW transmitter klystron was care-

fully tested and tuned to specific frequencies. All operational parameters were documented and the data and test results were included with the tube when it was turned over to Section 337.

References

1. Jackson, E. B., "DSN Research and Technology Support," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VIII, pp. 68-73. Jet Propulsion Laboratory, Pasadena, Calif., Apr. 15, 1972.
2. Jackson, E. B., "DSN Research and Technology Support," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VII, pp. 124-125. Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1972.

Table 1. Sources and source positions used in weak source observation program

Source	Position at time of observation	
	Right ascension, deg	Declination, deg
3C33	16.850	13.179
3C218	139.178	-11.981
3C270	184.502	5.975
3C348	252.452	5.000
3C353	259.772	-0.957
Cygnus X1	299.326	35.266
Beta Persei	46.500	40.850
Beta Lyrae	282.267	33.324
Jupiter	278.658	-22.895
Venus	63.419	24.706

Table 2. Clock synchronization activity from DSS 13

Station	Number of transmissions
DSS 14	44
DSS 41	33
DSS 42	32
DSS 51	29
DSS 62	26
USNO	30

Photon Noise Generation of Cathode-Ray Tube Display Systems

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SFOF/GCF Development Section

The mean square fluctuation components associated with the various luminous fluxes of ambient and generated light emitted from a cathode-ray tube (CRT) system are derived and combined to represent the photon noise component. A rationale for the criteria required for the discernment of noisy shades of gray as displayed by CRT systems is developed. The criteria are applied to an actual CRT system and verified with experimental results.

I. Introduction

The importance of determining photon noise relates to the evaluation of the photometric quality and discernible limitation of the reproduced image displayed on a cathode-ray tube (CRT) system. Fluctuations in the stream of photons, commonly known as photon noise, are generated by various phenomena occurring in the light dynamics of the CRT system. The fluctuations of the light emitted from a typical CRT system are divided into two parts in this article. The first part describes the fluctuations related to the ambient light reflected from the system. The second part describes the fluctuations of the light which is generated in the CRT. These fluctuations are then combined to represent the total mean fluctuation of the total light emitted from the system. Calculated luminance levels required for the discernment of noisy

gray shades generated by a selected CRT system are also shown and compared to experimental results.

II. Photon Noise Derivations

Light emitted from a CRT system (Fig. 1) is comprised of external light reflected from the CRT system, and light generated by the impingement of the electron beam upon the cathodoluminescent material. The fluctuations associated with these two light sources are derived and combined in the subsequent sections.

A. Ambient Light

The energy E of a photon is the product hf , where h is Planck's constant and f is the frequency. Consider a monochromatic flux of photons $n(\lambda)$ with wavelength λ flowing

through an area dA . The energy of these photons may be expressed photometrically as

$$\frac{dE}{dA} = dL = K_v c h n(\lambda) V(\lambda) \frac{d\lambda}{\lambda} \quad (1)$$

where K_v is a factor to convert energy to lumens, c is the velocity of light, and $V(\lambda)$ is the visual response. Integrating Eq. (1) over an incremental wavelength $\Delta\lambda$ at a wavelength λ results in

$$L = K_v h c n(\lambda) V(\lambda) \int_{\lambda}^{\lambda+\Delta\lambda} \frac{d\lambda}{\lambda} \quad (2)$$

or

$$L = K_v h c n(\lambda) V(\lambda) \frac{\Delta\lambda}{\lambda} \quad (3)$$

where L is the luminous flux at wavelength λ . The radiant flux of photons $n(\lambda)$ may be written from Eq. (3) as

$$n(\lambda) = \frac{L\lambda}{K_1 V(\lambda) \Delta\lambda} \quad (4)$$

where $K_1 = K_v h c$.

It also follows that the average radiant flux of photons $\bar{n}(\lambda)$ at wavelength λ required to produce a mean luminous flux $\bar{L}$ is

$$\bar{n}(\lambda) = \frac{\bar{L}\lambda}{K_1 V(\lambda) \Delta\lambda} \quad (5)$$

1. Noise from the filter screen. A monochromatic radiant flux of photons $n_a(\lambda)$ external to the CRT system enters at the filter screen having a transmissivity coefficient $\tau_f(\lambda)$. Of the amount which does not pass on to the faceplate, a portion is absorbed $\alpha_f(\lambda)$ by the filter screen and the remaining is reflected from the screen by the amount $\rho_f(\lambda)$ (Ref. 1). The reflectance factor $\rho_f(\lambda)$ may be interpreted to represent the probability of the incident photons not dissipated, whereas the factor $\alpha_f(\lambda) = 1 - \rho_f(\lambda)$ represents the probability of the incident photons dissipated. These probabilities are valid provided that the individual events of the photons are completely random.

Because the considered beam of light is monochromatic, the values of all parameters will be understood to be a function of wavelength and will not be expressed as such unless noted otherwise. This is made to simplify expressions and thereby provide ease of reading.

From the theory of partition noise (Ref. 2), the mean square fluctuation in the radiant flux of photons

$$\rho_f(1 - \tau_f)n_a$$

reflected from the filter screen may be expressed as

$$\overline{(n_a - \bar{n}_a)^2} = \rho_f(1 - \rho_f)(1 - \tau_f)n_a = F_f^2 n_a \quad (6)$$

where

$$F_f^2 = \rho_f(1 - \rho_f)(1 - \tau_f) \quad (7)$$

2. Noise generated by the glass faceplate. The radiant flux of photons impinging upon the outer surface of the glass faceplate is $\tau_f n_a$. By nature of the randomness of the reflection and absorption processes which these photons encounter, partition noise is generated. The mean square noise component associated with the flux of photons reflected from and those entering the faceplate can be written as

$$\overline{(n_a - \bar{n}_a)^2} = k_p \tau_f n_a \quad (8)$$

where

$$k_p = \rho_g(1 - \rho_g) \quad (9)$$

and ρ_g is the reflectivity coefficient of the glass faceplate. The mean square noise component associated with the flux of photons $\rho_g \tau_f^2 n_a$ reflected from and finally passing through the filter screen can be expressed as

$$\overline{(n_a - \bar{n}_a)^2}_{g1} = \tau_f^3 k_p n_a \quad (10)$$

Equation (10) is the first noise component term of the light reflections from the glass faceplate. The flux of photons $(1 - \rho_g) \tau_f n_a$ entering the faceplate proceed to be reflected from the inner surface of the faceplate and finally emerge out of the CRT system carrying the second noise component term. The flux impinging upon the inner surface is $\tau_g(1 - \rho_g) \tau_f n_a$ of which $\rho_g \tau_g(1 - \rho_g) \tau_f n_a$ is reflected and $\tau_g(1 - \rho_g)^2 \tau_f n_a$ passes to the cathodoluminescent material (Ref. 3). This material is commonly called the phosphor screen (Ref. 4) and will be denoted as such here.

As the light passes through the glass faceplate, the portion absorbed by the faceplate is proportional to $(1 - \tau_g)$. The transmission process, therefore, generates partition noise to the flux of photons passing through. Assuming that τ_g is not a function of faceplate thickness, the average

flux of photons in the considered stream passing through the faceplate is $[(1 + \tau_g)/2] (1 - \rho_g) \tau_f n_a$.

The mean square noise component generated during the transmission process is

$$\tau_g (1 - \tau_g) \frac{(1 + \tau_g)}{2} (1 - \rho_g) \tau_f n_a$$

This quantity can be related to the flux of photons transmitted and expressed as

$$\overline{(n_a - \bar{n}_a)_{\tau_1}^2} = k_\tau \tau_g (1 - \rho_g) \tau_f n_a \quad (11)$$

where

$$k_\tau = \frac{(1 - \tau_g)^2}{2} \quad (12)$$

The flux of photons entering the faceplate, however, contains a noise component given in Eq. (10). This component is contained in the flux being transmitted through the glass faceplate. The mean square components by Eqs. (10) and (11) can be algebraically added to give the total mean square noise component associated in the flux of photons impinging upon the inner surface of the faceplate as follows:

$$\overline{(n_a - \bar{n}_a)_{\tau_2}^2} = \tau_g^2 \tau_f^2 k_\rho n_a + k_\tau \tau_g (1 - \rho_g) \tau_f n_a \quad (13)$$

Similarly, the mean square noise component associated with the flux reflected from the inner surface can be written as

$$\overline{(n_a - \bar{n}_a)_{\tau_3}^2} = \rho_g^2 \overline{(n_a - \bar{n}_a)_{\tau_2}^2} + k_\rho \tau_g (1 - \rho_g) \tau_f n_a \quad (14)$$

As these photons are transmitted through the faceplate until they impinge upon the outer surface for another series of re-reflections and transmissions, partition noises are again generated in the transmission and reflection processes. By applying the noise generation argument described for Eqs. (13) and (14), the flux of photons $(n_a)_{g_2}$ emerging from the filter screen as the second reflection term is

$$(n_a)_{g_2} = (1 - \rho_g) k_\rho \tau_g^2 \tau_f^2 n_a \quad (15)$$

and the mean square fluctuation associated in the flux $(n_a)_{g_2}$ can be shown to be

$$\begin{aligned} \overline{(n_a - \bar{n}_a)_{g_2}^2} &= \tau_f^2 \tau_g^2 \left\{ k_\rho^2 + (1 - \rho_g)^2 k_\tau k_\rho \right. \\ &\quad \left. + \frac{(1 - \rho_g)^2}{n_a} \overline{(n_a - \bar{n}_a)_{\tau_3}^2} \right\} n_a \quad (16) \end{aligned}$$

Equation (16) is the second noise component term of the light reflections. Since there are an infinite number of subsequent reflections and mean square fluctuation components which can be continually described, the total mean square fluctuation component $\overline{(n_a - \bar{n}_a)_g^2}$ associated with the cumulative reflective fluxes is

$$\overline{(n_a - \bar{n}_a)_g^2} = \overline{(n_a - \bar{n}_a)_{g_1}^2} + \overline{(n_a - \bar{n}_a)_{g_2}^2} + \cdots + \overline{(n_a - \bar{n}_a)_{g_n}^2} \quad (17)$$

Combining this series expression, and eliminating the products having second order effects, Eq. (17) reduces to

$$\begin{aligned} \overline{(n_a - \bar{n}_a)_g^2} &\cong \tau_g^2 \tau_f^2 \{ k_\rho^2 + (1 - \rho_g)^2 [k_\tau k_\rho \\ &\quad + k_\rho \tau_g (1 + \tau_g - \rho_g) + k_\tau \tau_g (1 - \rho_g)] \} \cdot n_a \\ &= F_\rho^2 \cdot n_a \quad (18) \end{aligned}$$

The inter-reflections of the radiant fluxes impinging upon the filter screen and reflecting back to the outer surface of the glass faceplate for similar light dynamics described above were surveyed. Each reflected flux of photons would be reduced by the factor $\rho_f \rho_g (1 - \tau_f)$. Substituting values for the parameters of practical CRT systems, the resulting reflection terms would have less than a second-order effect upon the value of the total mean square fluctuation component generated in the system. These inter-reflections are considered negligible and therefore are not included.

3. Noise from the phosphor screen. The series of radiant fluxes emerging from the inner surface of the glass faceplate toward the phosphor screen including their respective mean square fluctuation components can be combined and expressed as a single radiant flux of photons including a mean square fluctuation component associated with it. This flux then impinges upon the phosphor screen and generates partition noise due to the random distribution occurring in the reflection and absorption processes. The reflective flux proceeds through the glass faceplate and filter screen, during which further partition noises are generated during transmission and reflection processes. The subsequent reflection terms were neglected because their values contribute less than third-order effects to the total mean square fluctuation component. The first term only was, therefore, considered.

The total flux impinging upon the phosphor screen from the faceplate can be shown to be (Ref. 3)

$$(n_a)_i = \frac{(1 - \rho_g)^2 \tau_g \tau_f}{(1 - \rho_g^2 \tau_g^2)} \cdot n_a \quad (19)$$

The mean square fluctuation contained in $(n_a)_i$ in its reduced expression is

$$\overline{(n_a - \bar{n}_a)_i^2} \cong (1 - \rho_g) \tau_g \tau_f \{k_p [1 + \tau_g (1 - \rho_g)] + k_r (1 - \rho_g)^2\} \cdot n_a \quad (20)$$

The flux of photons emerging from the CRT system through the filter screen because of $(n_a)_i$ can be shown to be (Ref. 3)

$$(n_a)_s = \frac{(1 - \rho_g)^3 \tau_g^2 k_s \tau_f}{(1 - \rho_g^2 \tau_g^2)} \cdot n_a \quad (21)$$

where $k_s = \rho_s (1 - \rho_s)$, and ρ_s is the reflectivity coefficient of the phosphor screen. The mean square fluctuation component in its reduced form associated with $(n_a)_i$ is

$$\overline{(n_a - \bar{n}_a)_s^2} \cong \tau_f^3 \tau_g^2 (1 - \rho_g)^2 [J_1 + (1 - \rho_g)^2 \rho_s k_s \tau_g J_2] \cdot n_a = F_s^2 \cdot n_a \quad (22)$$

where

$$\begin{aligned} J_1 &= k_p k_s + (1 - \rho_g)^2 k_r k_s \\ &\quad + (1 - \rho_g)^2 \tau_g k_p \rho_s + (1 - \rho_g)^4 \tau_g k_s \\ J_2 &= k_p [1 + \tau_g (1 - \rho_g)] + k_r (1 - \rho_g)^2 \end{aligned}$$

4. Combining the fluctuations. The total flux of photons $(n_a)_t$ emerging from the CRT system due to the reflections of the incident flux of ambient light n_a is given as (Ref. 3)

$$(n_a)_t = \tau_f^2 \left\{ \rho_g + \frac{(1 - \rho_g)^2 \tau_g^2 H_a}{(1 - \rho_g \tau_g^2 H_a)} \right\} \cdot n_a \quad (23)$$

where

$$H_a = \rho_g + \frac{\rho_s (1 - \rho_g)^2}{1 - \rho_g \rho_s} \quad (24)$$

The mean square fluctuation component $\overline{(n_a - \bar{n}_a)_t^2}$ associated with the total radiant flux output $(n_a)_t$ is found by combining the results of Eqs. (6), (18), and (22) as follows:

$$\overline{(n_a - \bar{n}_a)_t^2} = (F_f^2 + F_p^2 + F_s^2) \cdot n_a \quad (25)$$

B. Generated Light

The phosphor screen, comprised of cathodoluminescent material, will luminesce when impacted by electrons. The light produced at the emitting surface of the phosphor screen will fluctuate and is characterized by the quality of the electron beam and the properties of the cathodoluminescent material. The three prime sources which can cause

the fluctuation to occur are the residual noises in the electron beam, the process of photon conversion, and the granularity of the phosphor screen.

1. Noise in the electron beam. The electron beam current will fluctuate because of noise generated in the CRT circuit. Initially, the signal entering the CRT circuit may contain a mean square fluctuation voltage $(v_{in} - \bar{v}_{in})^2$ produced through the receiver system, transmitter power, etc. This fluctuation is usually low (Ref. 4).

The fluctuation generated in the CRT amplifier is characterized by thermal agitation caused by the random motion of the free electrons in the resistor in the input stage of the amplifier (Refs. 4 and 5). The mean square fluctuation voltage can be expressed as

$$\overline{(v - \bar{v})^2} = 4KT \int_{f_1}^{f_2} R(f) A(f) df \quad (26)$$

where K is Boltzmann's constant, T is the absolute temperature of the resistor, $R(f)$ is the equivalent noise resistance of the system impedance, and $A(f)$ is the power amplification of the system. The values of $R(f)$ and $A(f)$ may be a function of the frequency f within the bandwidth $f_2 - f_1$.

The electron beam also contains shot noise developed by the emission anode current i of the beam. The mean square fluctuation current is given by

$$\overline{(i - \bar{i})^2} = 2e(f_2 - f_1) i \quad (27)$$

where e is the charge of an electron, and i is the dc anode current. There are other noise components in the electron beam current which occur from flicker effects, space-charge limitations, transit-time effects and secondary emission. However, these noise components are low relative to the value developed by shot noise in typical well-designed CRT systems operating at common frequency levels (Refs. 4 and 6). These noise components can, therefore, be neglected.

The total mean square fluctuation current in the electron beam can now be written from Eqs. (26) and (27) as

$$\begin{aligned} \overline{(i - \bar{i})^2} &= \int_{f_1}^{f_2} \overline{(v_{in} - \bar{v}_{in})^2} \frac{A(f)}{R_1^2(f)} df \\ &\quad + 4KT \int_{f_1}^{f_2} F(f) R(f) df + \overline{(i - \bar{i})^2} \end{aligned} \quad (28)$$

where $F(f)$ is the noise figure of the amplifier system.

2. Photon conversion. The energy of the electron beam upon impact with the phosphor screen is converted to quencher center recombinations, backscattering of incident electrons, long-wavelength radiation from the electron, production of secondary electrons, thermal heat transfer to environs, and finally the emission of the generated photons (Ref. 7).

Let $\bar{n}_e$ be the average arrival of electrons per second at the phosphor screen, and cover an area dA visible at the light emitting surface of the screen. The average radiant flux of generated photons $\bar{n}_g$ emitted as a function of wavelength can then be written as

$$\overline{n_g(\lambda)} = \overline{\eta(\lambda, i)} \cdot \bar{n}_e \quad (29)$$

where $\overline{\eta(\lambda, i)}$ is the mean electron-photon conversion function of the given cathodoluminescent material and may be a function of λ and beam current i . Since $\overline{\eta(\lambda, i)}$ represents the fraction of electron energy converted to light and $(1 - \overline{\eta(\lambda, i)})$ represents the fraction transferred to other mechanisms, it follows that partition noise is developed in the emitted radiant flux of photons n_g and expressed as

$$[n_g(\lambda) - \overline{n_g(\lambda)}]^2 = [\overline{\eta(\lambda, i)}]^2 [1 - \overline{\eta(\lambda, i)}] \cdot \bar{n}_e \quad (30)$$

3. Granularity. The cathodoluminescent material is comprised largely of inorganic crystalline particles of sizes varying in accordance with their size distribution. These particles are usually deposited on the CRT glass faceplate either by a settling process or by electrophoresis (Ref. 8). Settled films are not as homogeneous and appear to have higher graininess than do films processed by electrophoresis. The amplitude of randomness of cathodoluminescence was measured and shown to be greater for settled films because of the greater nonhomogeneity of particle size and deposition (Ref. 8). It follows that granularity, the objective measurement of the diffusion of light by the grains in the granular structure, must be considered as a noise generating source.

Let $\eta(\lambda, i)$ signify the electron-photon conversion function at an arbitrary position located on the faceplate. Equation (29) describes the mean photon radiant flux with wavelength λ generated for the phosphor screen. However, the photon radiant flux generated at the arbitrary position can similarly be written as

$$n_g(\lambda) = \eta(\lambda, i) \cdot \bar{n}_e \quad (31)$$

By squaring the difference between these two emissions, the mean square fluctuation component of the emitted photon flux is

$$[\overline{n_g(\lambda) - \overline{n_g(\lambda)}}]^2 = [\overline{\eta(\lambda, i) - \overline{\eta(\lambda, i)}}]^2 \cdot (\bar{n}_e)^2 \quad (32)$$

Let the granularity factor σ be defined as

$$\sigma(i) = \int_{\lambda} [\eta(\lambda, i) - \overline{\eta(\lambda, i)}] d\lambda \quad (33)$$

It follows that the mean square fluctuation component of the radiant flux over the spectrum generated is

$$(\overline{n_g - \bar{n}_g})^2 = \sigma^2(i) \cdot \bar{n}_e^2 \quad (34)$$

4. Combining the fluctuations. The current fluctuation of the electron beam (Eq. 28) directly converts to a photon fluctuation component. If the root mean square (rms) value of this fluctuation in the beam current were divided into the beam current, $i/[(i - \bar{i})^2]^{1/2}$, the quotient is identified as the rms signal to noise ratio (SNR) of the beam current. Equation (28) can then be converted to a mean square fluctuation component of the photon radiant flux generated as follows:

$$[n_g(\lambda) - \overline{n_g(\lambda)}]^2 = \left[\frac{\overline{\eta(\lambda, i)}}{\text{SNR}(i)} \right]^2 \left(\frac{i}{e} \right)^2 \quad (35)$$

where $\text{SNR}(i)$ may be a function of the beam current.

Combining Eqs. (30), (34), and (35) yields the total mean square fluctuation of the total generated photon radiant flux emitted from the phosphor screen surface as follows:

$$\begin{aligned} [\overline{n_g(\lambda) - \overline{n_g(\lambda)}}]^2 &= \left[\left\{ \eta^2(\lambda, i) [1 - \overline{\eta(\lambda, i)}] + \frac{i}{e} \left[\sigma^2(i) + \left(\frac{\overline{\eta(\lambda, i)}}{\text{SNR}(i)} \right)^2 \right] \right\} \cdot \bar{n}_e(\lambda) \right. \\ &= N_g^2(\lambda, i) \cdot \bar{n}_e(\lambda) \end{aligned} \quad (36)$$

This noise component characterized by the factor $N_g^2(\lambda, i)$ passes through the CRT system in which partition noises due to reflection and transmission processes enhance the noise component of the generated beam. Following the same arguments described in Section A, it can be shown that the total mean square fluctuation component of the

generated beam emitted from the filter screen of the CRT system is

$$\begin{aligned} [n_g(\lambda) - \overline{n_g(\lambda)}]_{\text{sum}}^2 &= \tau_f^2 \{ \tau_g (1 - \rho_g) [(1 - \rho_g) \tau_g k_p \\ &\quad + k_\tau (1 - \rho_g)^2 + k_p] \\ &\quad + (1 - \rho_g)^2 \tau_g^2 N_g^2(\lambda, i) \} \cdot \overline{n_e}(\lambda) \\ &= F_g^2(\lambda, i) \cdot \overline{n_e}(\lambda) \end{aligned} \quad (37)$$

The total radiant flux of photons generated ($n_g(\lambda)$)_t by the electron beam and emitted from the CRT system including all the inter-reflections (Ref. 3) is given as

$$[n_g(\lambda)]_t = \frac{(1 - \rho_g) \tau_f \tau_g K_g}{Q} \cdot n_g(\lambda) \quad (38)$$

where

$$K_g = \frac{1 - \rho_g}{1 - \rho_s \rho_g} \quad (39)$$

$$Q = \frac{1 - \rho_s \rho_g - \rho_g^2 \tau_g^2 - \rho_s \rho_g \tau_g^2 + 2\rho_g^2 \rho_s \tau_g^2}{1 - \rho_s \rho_g} \quad (40)$$

III. Total Noise and Total Light Emitted

The mean square fluctuation component of the ambient photon flux can be converted to luminance by using the square of the difference of Eqs. (4) and (5). As an example, Eq. (25) can be rewritten as

$$(\overline{L - \bar{L}})_a^2 = [F_f^2 + F_p^2 + F_s^2] \cdot \left(K_1 V(\lambda) \frac{\Delta\lambda}{\lambda} \right)^2 \cdot n_a \quad (41)$$

Similarly Eq. (37) can be converted to luminance. The sum of this result with Eq. (41) will give the total mean square fluctuation component of the total light generated and reflected from the CRT system. This is written as

$$\begin{aligned} (\overline{L - \bar{L}})_t^2 &= \left(K_1 V(\lambda) \frac{\Delta\lambda}{\lambda} \right)^2 [(F_f^2 + F_p^2 + F_s^2) \cdot n_a \\ &\quad + F_g^2(\lambda, i) \cdot \overline{n_e}] \end{aligned} \quad (42)$$

Since all the parameters expressed in Eq. (42) are functions of wavelength, the total root mean square (rms) component of the total luminance emitted over the visual spectrum is

$$\begin{aligned} \sqrt{(\overline{L - \bar{L}})_t^2} &= \int_{\lambda_1}^{\lambda_2} [(F_f^2 + F_p^2 + F_s^2) \cdot n_a \\ &\quad + F_g^2(\lambda, i) \cdot \overline{n_e}]^{1/2} K_1 V(\lambda) \frac{\Delta\lambda}{\lambda} \end{aligned} \quad (43)$$

The total radiant flux of photons emitted at wavelength λ out of the CRT system by both the ambient light and generated light is the sum of Eqs. (23) and (38). This flux can be converted to luminance by applying Eq. (4). Hence the total luminous flux L_t emitted from the CRT system over the visual spectrum is

$$L_t = K_1 \int_{\lambda_1}^{\lambda_2} V(\lambda) [(n_a(\lambda))_t + (n_g(\lambda))_t] \frac{d\lambda}{\lambda} \quad (44)$$

IV. Rationale for Discerning Gray Shades

To just discern the luminous flux of two adjacent gray-shade objects on a CRT screen, a certain minimum contrast between the displayed gray shades is required. This minimum contrast, called the threshold contrast factor C_T for a given spectrum, is a function of luminous flux of the object, the visual angle subtended, and the spatial frequency related to either the object domain or the retinal domain (Ref. 9). To just discern two adjacent equally sized gray-shade objects of uniform luminance levels L_1 and L_2 respectively viewed from a given distance, the minimum luminance difference is described by the relationship (Ref. 9)

$$L_1 - L_2 = C_T (L_1 + L_2) \quad (45)$$

However, when a fluctuation is associated with the luminous flux of each shade, the quality of the luminous flux is degraded and is said to be noisy. Let the fluctuation be described as the rms luminous noise component ΔL_0 of the object at luminance level L_0 , and defined by the mean square fluctuation component as

$$\Delta L_0 = \sqrt{(\overline{L_0 - \bar{L}_0})^2} \quad (46)$$

In the presence of noise, the fluctuating luminance levels of the two gray shades are such that the upper rms peak level of the lower luminance level L_2 will tend to blend in with the lower rms peak level of the higher luminance level L_1 as shown in Fig. 2. This blending results in lowering the probability of discernment of the gray shades, thereby not satisfying Eq. (45). When the luminance level of the lower peak of the upper shade ($L_1 - \Delta L_1$) equals the luminance level of the upper peak of the lower shade ($L_2 + \Delta L_2$), discernibility is not possible since the two gray shades in this condition at the interface blend together and appear as one shade. It is reasonable to conclude that the reliability of discernment can be increased to the threshold value if the difference of the luminance levels between the gray shades is increased. Therefore, to

make certain that discernibility can be achieved, it is concluded that the described peak luminance levels be spread to satisfy Eq. (46) as follows:

$$(L_1 - \Delta L_1) - (L_2 + \Delta L_2) = C_T [L_1 - \Delta L_1 + L_2 + \Delta L_2] \quad (47)$$

The luminance difference ΔL_t required for the discernment of adjacent noisy gray shades is $L_1 - L_2$, the difference of the luminance levels described in Eq. (47). This luminance difference required for gray-shade discernment at a constant reliability was experimentally found for a given CRT system utilizing a P4 phosphor. These results are shown in Fig. 3 as a function of the brighter luminance level L_B of the gray shade (Ref. 10). The CRT configuration and operating conditions are given in Ref. 11. The measured rms SNR at white level was 110. The luminance output at the faceplate as a function of current density is given in Table 1 (Ref. 4).¹

The luminance difference ΔL_t can also be determined from Eq. (47) by evaluating the noise components given in Eq. (47) by Eq. (43). The luminance level of each gray

shade is described by Eq. (44). This computation was performed for a given CRT system for a luminance range extending over three orders of magnitude and based on the current densities given in Table 1 and the granularity factor of the phosphor screen to be 0.025.² The computation results are shown as a dashed curve in Fig. 3 and are in good agreement with the experimental results.

It can be seen in Fig. 3 that a progressive deviation of the computed result from the experimental result occurs at luminance levels above 171.3 cd/m² (50 ft-L). This deviation is due to the glaring characteristics of CRT screens which was not included in the computations. Figure 3 also includes a curve for a noiseless CRT system. The luminance difference required to discern noisy CRT gray shades is about four times greater than that required for noiseless gray shades.

V. Concluding Remarks

The luminance fluctuations generated in a CRT system are formulated and were verified by their application to an actual CRT system whose parameters and operating conditions were known.

¹Also communication with Conrac Corp., CRT Dept.

²Communication with CBS Laboratories, Electron Physics Dept.

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Table 1. Luminance output versus current density

Luminance output		Current density, A/cm ²
ft-L	cd/m ²	
140	479.6	0.2
115	394.0	0.1
80	274.1	0.06
60	205.6	0.04
32	109.6	0.02
0.32	1.1	0.0002

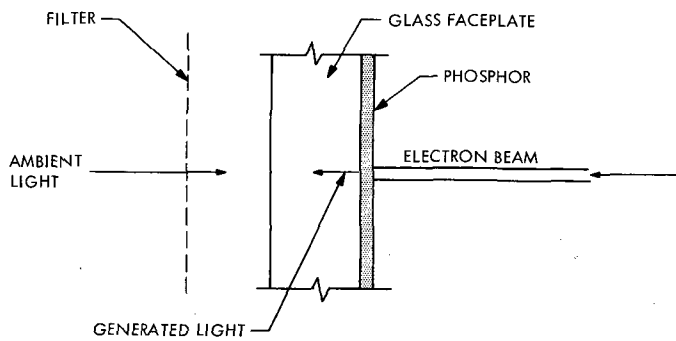


Fig. 1. Cathode-ray tube configuration

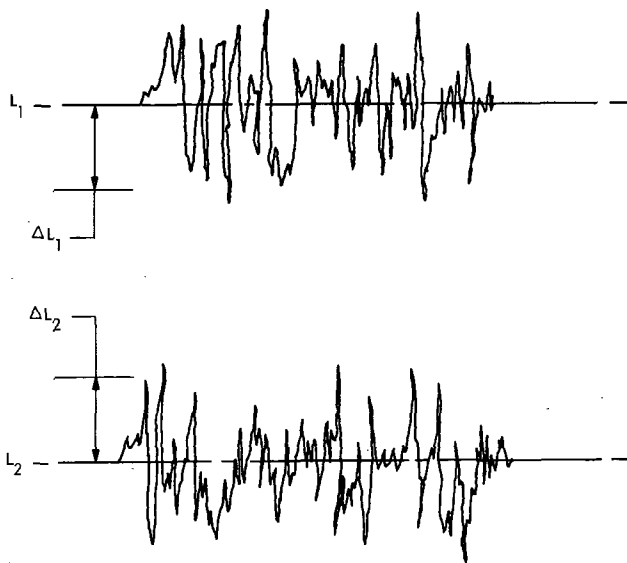


Fig. 2. Gray-shade luminous flux

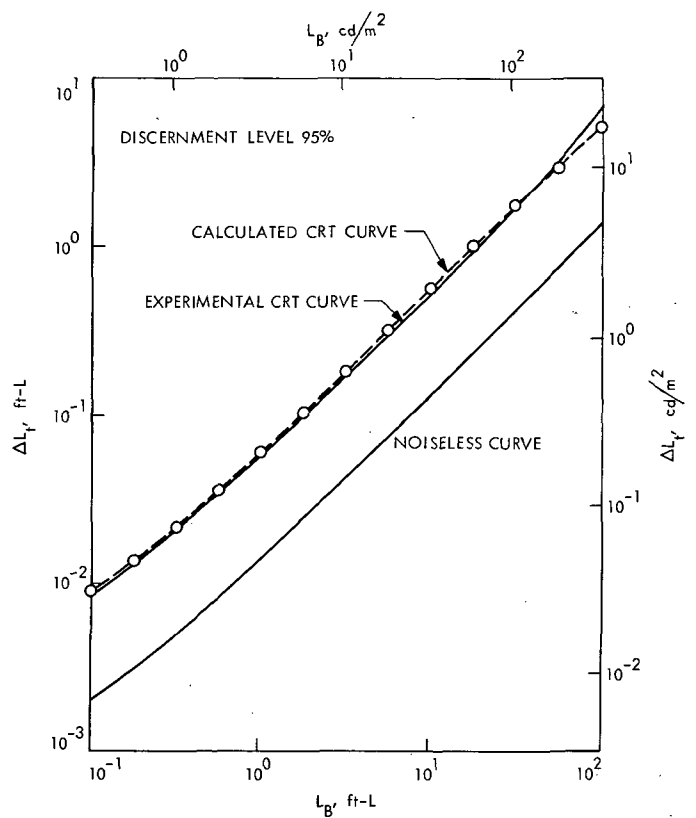


Fig. 3. Difference of luminance ΔL_t to discern gray shades vs luminance of brighter gray shade L_B

Mariner Mars 1971/Pioneer 10 Multi-Mission Level Modeling Runs Using the SFOF Mark IIIA Central Processing System Model

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Simulation models are currently being used for Space Flight Operations Facility (SFOF) development at the Jet Propulsion Laboratory. This article documents the results of a series of modeling runs made during January and February 1972. The model contained a majority of the SFOF Mark IIIA Central Processing System capabilities required to simultaneously support the orbital phase of the Mariner Mars 1971 mission and the early cruise phase of the Pioneer 10 mission.

I. Introduction

Simulation models are currently being developed in the SFOF/GCF Development Section to support the design and implementation of the SFOF Mark IIIA Central Processing System (CPS). SFOF Mark IIIA modeling studies began in May 1969 when it was learned that NASA would be providing JPL with IBM 360 Model 75 digital computers to form the nucleus of the SFOF Mark IIIA CPS.

The IBM Computer System Simulator (CSS) program was selected for model development activities since it runs on the 360/75 and the program itself applies specifically to computer systems. The results of previous modeling studies that were performed during the early stages of SFOF Mark IIIA development are described in Refs. 1 and 2.

This article summarizes the results of seven modeling runs made during January and February 1972 to evaluate the performance of the SFOF Mark IIIA CPS, con-

figured to simultaneously support the orbital phase of the Mariner Mars 1971 mission and the early cruise phase of the Pioneer 10 mission. A more detailed summary is contained in JPL IOM 9181-35-72, dated February 16, 1972 (JPL internal document).

II. Objectives

There were several objectives associated with this series of modeling runs:

- (1) Use the model to analyze the overall performance of the Central Processing System under conditions of dual mission loading.
- (2) Alleviate problem areas (primarily main memory core lockout) by changing the hardware and software characteristics of the model.
- (3) Determine the effect of heavy external loading on the system and change the model characteristics in order to support this level of loading.

III. Model Description

The SFOF Mark IIIA hardware configuration that was modeled is shown in Fig. 1. The following changes were made to this normal configuration:

- (1) *Runs 3, 6, and 7.* A 4-megabyte IBM 2301 drum was installed on channel 1 of the 2860-2. The 2314 disk files were relocated to channels 2 and 5.
- (2) *Run 4.* The Large Capacity Storage (LCS) was expanded from 2 to 4 megabytes. The read/write storage cycle in the model, for a double word, was reduced from 8 to 4 microseconds to reflect the two-way interleaving addressing structure.

The line assignments for the 2909-3 input and output high-speed data (HSD) subchannels were arbitrarily chosen.

The software configuration that was modeled defined the functional capabilities at the following levels:

Operating System: JPLOS, Version 3.0
Applications Software: Mission Build, Model 5,
Version 18

The allocation of disk resident load modules and data tables for each of the runs are shown in Table 1. In the model, information from a Model 5, Version 25 listing was used as the basis for organizing the data on the mission disk packs.

The size and residency of permanently allocated system core is shown in Table 2.

The Statistics Gathering System (SGS) that functions under the control of the 360/75 operating system provided timing information from the "live" system that was used to calibrate the model. In addition, data obtained from listings, flow charts, and other design information provided a percentage of manual calibration. It is estimated that the model used for this series of runs received approximately 30% SGS and 60% manual calibration.

IV. Description of Modeling Runs

The seven runs were executed in the following sequence:

Run	Hardware configuration	System activity	Results
1	Normal	Processing and display of real-time input data, E140 site playback data, and TTY recall data.	Ran to completion. No problems or anomalies observed.
2	Normal	Same processing as for Run 1, <i>and</i> the generation of Predicts and Sequence of Events files.	Terminated by core lockout.
3	Drum	Same as for Run 2.	Same as for Run 2.
4	4 megabytes of LCS	Same as for Run 2.	Ran to completion. No problems or anomalies observed.
5	Normal	Processing and display of real-time input data and the generation of Predicts and SOE files. Playback and recall data were eliminated from the script.	Terminated by core lockout.
6	Drum	Same as for Run 2.	Terminated due to backlogging of queues in the model. System heading for core lockout.
7	Drum	Same as for Run 5.	Ran to completion. No problems or anomalies observed.

V. Environment and Sequence of Events

The types and number of simulated input data streams are listed in Table 3.

Other significant events, with their occurrence in time relative to the beginning of the run (t_0), were:

- (1) $t_0 + 25$ seconds. Predicts (phi-factor) file generation of 2 passes for each of 4 stations.
- (2) $t_0 + 70$ seconds. Telemetry SDR recall for *Mariner*.
- (3) $t_0 + 70$ seconds. Sequence of Events file generation of approximately 360 lines of data.
- (4) $t_0 + 100$ seconds. Telemetry SDR recall for *Pioneer*.
- (5) $t_0 + 150$ seconds. Recall of 100 records of *Mariner* tracking data from the 490 Communications Processor.

Additionally, a commanding sequence to DSS 14 for *Mariner*, consisting of manual entry, transmission, and enabling of a command block, was executed during each run. A TCP stack-loading sequence to DSS 51 for *Pioneer* was also simulated. Pseudo-residuals were calculated for all input tracking streams.

Table 4 lists the displays that were initialized during each run.

VI. Results

The results of the seven runs are summarized in Tables 5 through 11. Each of the snap intervals represents one minute of simulated real time. A glossary of terms used in these tables appears in Table 12.

The following is a summary of significant items:

- (1) Runs 1, 4, and 7 were considered successful in that they executed to completion (a minimum of 5 one-minute snap intervals).
- (2) Runs 2, 3, 5, and 6 terminated prematurely due to main memory core lockout conditions.
- (3) Run 1 was the base run. There were no significant problems or anomalies observed during this run.
- (4) Runs 2 and 3 both terminated at approximately 50 seconds into the third snap. Core lockout occurred about 20 seconds after the recall of tracking data from the Communications Processor was initiated.
- (5) A higher CPU utilization occurred during the third snap interval of Run 3 (82% vs 45% for Run 2). This reflects the increase in execution of user tasks resulting from the relocation of JOBLIB load modules to the drum and marking them non-LCS allocatable.
- (6) Only minor changes were made to the software functions in the model for Run 4. An improvement in system performance would be expected if significant changes were made to take advantage of the additional 2 megabytes of LCS.
- (7) The elimination of E140 playback and CP recall data did not prevent core lockout from occurring during Run 5 when the normal configuration was utilized. Making Sequence of Events load modules non-LCS allocatable and eliminating playback and recall resulted in no significant difference. System performance was not degraded by in-line execution of the Sequence of Events generator (SEG) load modules. Approximately 300 kbytes of LCS were made available during this run. CPU utilization during snap intervals 4 and 5 decreased drastically due to lack of main memory core. During interval 5, the entire CPU utilization is attributable to the system's unsuccessful searches for available core.
- (8) During Runs 6 and 7, a quantity of load modules was left on disk pack 133 and marked LCS allocatable. All other M3A5.RTDS.GO load modules were placed on the drum and marked non-LCS allocatable.
- (9) Run 6 was terminated approximately 10 seconds into the fifth snap as a result of queues in the model overflowing. While core lockout was not the immediate cause of the run termination, there was much purging required to satisfy GETMAIN requests. The resulting delay led to data being backlogged. The backlog increased at such a rate that even if queue overflow had not occurred it is reasonable to assume that core lockout would have occurred before the backlog could have been processed.
- (10) The same hardware configuration was utilized for Runs 6 and 7. Elimination of E140 playback and CP recall data from Run 7 removed the catalyst that caused core lockout in Run 6.
- (11) By eliminating the playback and recall data, and placing some of the JOBLIB load modules on drum, it was possible to complete Run 7 without the loss of other real-time input data.

- (12) The tapes on Channel C, used primarily for data logging, were utilized approximately 25%.
- (13) Printer 460, used to display the telemetry latest available data (LAD) dump, is the only device that approaches saturation for each run.
- (14) The outbound HSD channel to Ames was also very active, with a channel utilization of near 70% for each run.
- (15) Input/output (I/O) channel and subchannel utilization figures indicate there were no serious problems in this area.
- (16) The maximum backlog of output queues, related to the line printer, for six of the seven runs was 20 kbytes.

- (6) No tasks had to wait while storage management attempted to satisfy their core requests.
- (7) No backlogging or loss of data.

The very high level of CPU utilization prevalent in Run 7 can be attributed to (1) use of LCS for user GETMAINS with an accompanying increase in execution time, and (2) the presence of the SEG and PREDICTS load modules, which once in core will absorb most of the CPU time not used by the real-time subsystems.

Generally, main core is the limiting resource in the system. The CORE=(LCS, MAIN) option results in improved overall system performance when used on a system-wide basis. The additional main core freed up allows load modules to be more readily loaded and decreases the number of main core purges required. In order to avoid "overuse" of LCS, it is necessary to exercise sound judgment when marking load modules non-LCS allocatable in order to have LCS available for *user* GETMAINS.

The runs show that tasks which buffer large amounts of data in core (either directly or indirectly by queuing it for someone else) will cause a heavily loaded system to collapse. The recall of tracking data from the CP is the obvious example on the input side of the system, but telemetry playback can have the same effect if data are arriving faster than they can be processed.

In order to study the core lockout problem resulting from the fragmentation of core over a period of time, longer modeling runs would be required.

VII. Conclusions

Based upon the assumptions made for each run, Run 7 provided the best overall results as summarized below. The run was operationally terminated after 6½ snap intervals due to the expiration of available 360/75 computer time.

- (1) Operating system overhead was a lower percentage of total CPU utilization.
- (2) Highest amount of phi-factor file and SEG program execution.
- (3) No main core user requests had to wait.
- (4) No load modules purged from LCS.
- (5) Main core and LCS usage less than maximum.

References

1. Simon, H. S., "SFOF Mark IIIA Central Processing System Model Development," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. I, pp. 95-102. Jet Propulsion Laboratory, Pasadena, Calif., Feb. 15, 1971.
2. Simon, H. S., "Mariner Mars 1971 Launch Phase Study Using the SFOF Mark IIIA Central Processing System Model," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. III, pp. 179-186. Jet Propulsion Laboratory, Pasadena, Calif., June 15, 1971.

Table 1. Allocations of frequently accessed load modules and data tables

Load modules and data tables	Run 1	Run 2	Run 3	Run 4	Run 5	Run 6	Run 7
<i>Tracking</i>							
SDR data table	132	132	232	132	132	232	232
<i>Telemetry</i>							
Mariner load modules	133	133	Drum	133	133	133	133
Mariner SDR data table	232	232	532	232	232	532	532
Pioneer load modules	133	133	Drum	133	133	Drum	Drum
Pioneer SDR data table	133	133	233	133	133	233	233
<i>Monitor and Ops Control</i>							
Load modules	133	133	Drum	133	133	133	133
<i>Pioneer</i>							
Data table	134	134	234	134	134	234	234
<i>Near real-time processors</i>							
PREDICTS load modules	133	133	Drum	133	133	Drum	Drum
PREDICTS data tables (1)	133	133	233	133	133	233	233
PREDICTS data tables (2)	233	233	533	233	233	533	533
SEG data tables (2)	133	133	233	133	133	233	233
SEG data tables (1)	134	134	234	134	134	234	234
SEG data tables (2)	233	233	533	233	233	533	533
UI display and output load modules	133	133	Drum	133	133	133	133
Format modules	133	133	Drum	133	133	Drum	Drum
RTSPOOL	237	237	537	237	237	537	537
MDR WRITE	237	237	537	237	237	537	537

Table 2. Permanently allocated system core

Description	Size, kbytes	Residence
Nucleus	124	Main
Nucleus	46	LCS
System queue area	30	Main
Trace table	14	Main
Resident job queue	10	LCS
LINKLIB directory	88	LCS
SVCLIB directory	56	LCS
Master scheduler	22	Main
RTDS.GO directory	50	LCS
RESIDENT RTPRGLIB	42	LCS
RT error message LMs	16	LCS
Non-UPDA data tables	898	LCS

Table 3. Simulated input data streams

Type	Spacecraft	Station	Rate	Via
E140	<i>Mariner</i>	14	33 1/3 bps	HSD
O420	<i>Mariner</i>	14	50 bps	HSD
E140 Playback ^a	<i>Mariner</i>	62	33 1/3 × 8 bps	HSD
Tracking	<i>Mariner</i>	14	1 sample/min	CP ^b
Tracking	<i>Mariner</i>	62	1 sample/min	CP
Tracking recall	<i>Mariner</i>	62	46 samples/sec	CP
Perf/status	N/A	14	12 blocks/min	HSD
Summary	N/A	14	2 blocks/min	HSD
Perf/status	N/A	62	12 blocks/min	HSD
Summary	N/A	62	2 blocks/min	HSD
F384	<i>Pioneer</i>	51	2048 bps	HSD
Tracking	<i>Pioneer</i>	42	1 sample/min	HSD
Tracking	<i>Pioneer</i>	51	1 sample/min	CP
Perf/status	N/A	42	12 blocks/min	HSD
Summary	N/A	42	2 blocks/min	HSD
Perf/status	N/A	51	12 blocks/min	HSD
Summary	N/A	51	2 blocks/min	HSD
Status	N/A	GCF	3 blocks/min	CP
AGC	<i>Pioneer</i>	42	1 block/74 sec	HSD

^aE140 playback rate = 8 times original data rate.

^bCP = UNIVAC 490 Communications Processor.

Table 4. Initialized displays

User	Display device	Quantity	Active displays
<i>Mariner</i>	DTV channels	35	32
	F-132 printers	9	18
	TTY printers	14	19
<i>Pioneer</i>	DTV channels	18	26
	F-132 printers	6	41
	TTY printers	10	23
DSN	DTV channels	17	18
	F-132 printers	4	5
	TTY printers	18	21

Table 5. Statistics from Run 1

Item measured	SNAP1	SNAP2	SNAP3	SNAP4	SNAP5
<i>CPU utilization (total)</i>	58%	67%	77%	76%	67%
Applications	21%	24%	26%	26%	24%
Operating system overhead	37%	43%	50%	48%	42%
<i>CPU utilization (task breakdown)</i>					
Tracking Subsystem	2%	1%	7%	6%	1%
Telemetry Subsystem	11%	18%	15%	15%	17%
Command Subsystem	0.2%	0.1%	0.2%	0.4%	0.5%
Monitor and Ops Control Subsystem	8%	9%	9%	9%	9%
User Interface Subsystem	30%	31%	36%	36%	24%
Operating system tasks	7%	7%	8%	8%	7%
<i>Main core usage</i>					
Average in use	630K	726K	806K	792K	784K
Average amount allocated	932K	961K	972K	970K	961K
Number of purges	10	21	70	63	39
Number of requests that had to wait	0	0	0	0	0
Number of LM's scatter loaded	0	0	0	0	0
<i>LCS usage</i>					
Maximum	1995K	2043K	2039K	2044K	2046K
Average	1920K	2001K	1995K	2009K	2026K
LCS GETMAIN'ed core (average)	142K	174K	175K	191K	204K
Number of LM's purged from LCS	0	10	3	0	11
<i>I/O utilization</i>					
2860-2 Selector Channel					
Channel 1 (disk)	6%	9%	24%	19%	11%
Channel 2 (disk)	5%	16%	12%	12%	13%
Channel 6 (LCS)	12%	16%	23%	22%	18%
2870 Multiplexer Channel					
Selector subchannel 1 (tapes)	23%	24%	26%	24%	23%
Selector subchannel 4 (Pioneer devices)	0%	0%	0%	0%	0%
Printer (0F9)	13%	33%	13%	12%	12%
2909-3 Asynchronous Data Channel					
HSD08 (output subchannel to Ames)	79%	71%	72%	77%	71%
Subchannel 46x	0%	0%	0%	0%	0%
Printer (460)	85%	93%	93%	93%	93%
<i>Task queues</i>					
CPU					
Number	10004	13546	16128	15627	13829
Average time	6 ms	5 ms	6 ms	6 ms	4 ms
Core					
Number	0	0	0	0	0
<i>Task response times</i>					
Tracking	196 ms	224 ms	161 ms	179 ms	123 ms
Telemetry	131 ms	193 ms	274 ms	276 ms	229 ms
Monitor and Ops Control	417 ms	244 ms	206 ms	249 ms	236 ms
<i>Backlog</i>					
Tracking data	0	0	41	0	0

Table 6. Statistics from Run 2

Item measured	SNAP1	SNAP2	SNAP3 ^a
CPU utilization (total)	76%	95%	45%
Applications	34%	41%	13%
Operating system overhead	43%	53%	31%
CPU utilization (Task breakdown)			
Tracking Subsystem	2%	1%	2%
Telemetry Subsystem	11%	18%	8%
Command Subsystem	0.2%	2%	2%
Monitor and Ops Control Subsystem	9%	10%	5%
User Interface Subsystem	31%	32%	15%
Operating system tasks	7%	8%	7%
Predicts (phi-factor file) generation	12%	21%	5%
Sequence of events generation	—	1%	1%
Main core usage			
Average in use	690K	884K	1007K
Average amount allocated	944K	970K	1011K
Number of purges	28	739	767
Number of requests that had to wait	0	30	55
Number of LM's scatter loaded	0	101	108
LCS usage			
Maximum	2045K	2044K	2041K
Average	1975K	2020K	2018K
LCS GETMAIN'ed core (average)	173K	218K	220K
Number of LM's Purged from LCS	38	45	2
I/O utilization			
2860-2 Selector Channel			
Channel 1 (disk)	25%	24%	8%
Channel 2 (disk)	16%	18%	4%
Channel 6 (LCS)	16%	28%	19%
2870 Multiplexer Channel			
Selector subchannel 1 (tapes)	34%	28%	16%
Selector subchannel 4 (Pioneer devices)	0%	0%	0%
Printer (OF9)	14%	50%	28%
2909-3 Asynchronous Data Channel			
HSD08 (output subchannel to Ames)	80%	71%	35%
Subchannel 46x	0%	0%	0%
Printer (460)	78%	93%	39%
Task queues			
CPU			
Number	12878	17210	7393
Average time	8 ms	11 ms	0 ms
Core			
Number	0	527	671
Average time	—	21 ms	310 ms
Task response times			
Tracking	256 ms	3328 ms	2832 ms
Telemetry	141 ms	273 ms	894 ms
Monitor and Ops Control	456 ms	301 ms	398 ms
Backlog			
Tracking data	0	0	99
Telemetry data	0	15	10
Input TTY and HSD lost	0	0	117

^aCore lockout occurred 50 seconds into snap interval 3.

Table 7. Statistics from Run 3

Item measured	SNAP1	SNAP2	SNAP3 ^a
CPU utilization (total)	82%	92%	82%
Applications	38%	45%	43%
Operating system overhead	42%	46%	38%
CPU utilization (task breakdown)			
Tracking Subsystem	1%	1%	2%
Telemetry Subsystem	14%	16%	11%
Command Subsystem	0.2%	0.2%	0.2%
Monitor and Ops Control Subsystem	13%	13%	14%
User Interface Subsystem	39%	42%	29%
Operating system tasks	7%	7%	7%
Predicts (phi-factor file) generation	5%	9%	7%
Sequence of events generation	—	1%	11%
Main core usage			
Average in use	653K	835K	945K
Average amount allocated	950K	974K	985K
Number of purges	16	66	82
Number of requests that had to wait	0	0	23
Number of LM's scatter loaded	0	9	72
LCS usage			
Maximum	1504K	1564K	1603K
Average	1462K	1519K	1559K
LCS GETMAIN'ed core (average)	216K	273K	313K
Number of LM's purged from LCS	0	0	0
I/O utilization			
2860-2 Selector Channel			
Channel 1 (drum)	23%	46%	74%
Channel 2 (disk)	5%	5%	12%
Channel 5 (disk)	14%	11%	7%
Channel 6 (LCS)	12%	11%	9%
2870 Multiplexer Channel			
Selector subchannel 1 (tapes)	31%	29%	22%
Selector subchannel 4 (Pioneer devices)	0%	0%	0%
Printer (OF9)	13%	34%	6%
2909-3 Asynchronous Data Channel			
HSD08 (output subchannel to Ames)	74%	68%	53%
Subchannel 46x	0%	0%	0%
Printer (460)	78%	84%	84%
Task queues			
CPU			
Number	12307	15228	11465
Average time	13 ms	16 ms	10 ms
Core			
Number	0	0	0
Task response times			
Tracking	282 ms	670 ms	1201 ms
Telemetry	240 ms	383 ms	725 ms
Monitor and Ops Control	630 ms	531 ms	658 ms
Backlog			
Tracking	0	0	96
Telemetry	0	16	93

^aCore lockout occurred 51 seconds into snap interval 3.

Table 8. Statistics from Run 4

Item measured	SNAP1	SNAP2	SNAP3	SNAP4	SNAP5
CPU utilization (total)	87%	99%	99%	100%	99%
Applications	42%	51%	47%	46%	46%
Operating system overhead	44%	47%	50%	52%	51%
CPU utilization (task breakdown)					
Tracking Subsystem	1%	1%	5%	8%	5%
Telemetry Subsystem	14%	18%	15%	13%	15%
Command Subsystem	0.2%	0.2%	0.2%	0.4%	1%
Monitor and Ops Control Subsystem	13%	13%	13%	14%	14%
User Interface Subsystem	42%	43%	43%	46%	46%
Operating system tasks	7%	8%	8%	8%	7%
Predicts (phi-factor file) generation	7%	15%	10%	7%	8%
Sequence of events generation	—	1%	1%	1%	1%
Main Core Usage					
Average in use	646K	809K	925K	950K	956K
Average amount allocated	936K	960K	985K	988K	995K
Number of purges	13	73	224	310	404
Number of requests that had to wait	0	0	4	8	17
Number of LM's scatter loaded	0	5	26	37	75
LCS Usage					
Maximum	2364K	2639K	2638K	2718K	2745K
Average	2148K	2518K	2606K	2670K	2714K
LCS GETMAIN'ed core (average)	217K	273K	290K	311K	328K
Number of LM's purged from LCS	0	0	0	0	0
I/O utilization					
2860-2 Selector Channel					
Channel 1 (disk)	16%	9%	12%	17%	11%
Channel 2 (disk)	11%	12%	11%	11%	8%
Channel 6 (LCS)	15%	18%	27%	32%	29%
2870 Multiplexer Channel					
Selector subchannel 1 (tapes)	35%	30%	29%	29%	27%
Selector subchannel 4 (Pioneer devices)	0%	0%	0%	0%	0%
Printer (0F9)	13%	46%	34%	11%	10%
2909-3 Asynchronous Data Channel					
HSD08 (output subchannel to Ames)	79%	72%	66%	77%	76%
Subchannel 46x	0%	0%	0%	0%	0%
Printer (460)	85%	93%	92%	88%	86%
Task queues					
CPU					
Number	12471	15014	15818	15860	15832
Average time	14 ms	19 ms	20 ms	23 ms	19 ms
Core					
Number	0	0	10	15	98
Average time	—	—	42 ms	30 ms	26 ms
Task response times					
Tracking	319 ms	334 ms	314 ms	322 ms	297 ms
Telemetry	241 ms	341 ms	493 ms	626 ms	485 ms
Monitor and Ops Control	583 ms	368 ms	373 ms	441 ms	378 ms
Backlog					
Tracking data	0	0	71	28	0
Telemetry data	0	0	15	52	50
Monitor and Ops Control data	0	0	10	0	0

Table 9. Statistics from Run 5

Item measured	SNAP1	SNAP2	SNAP3	SNAP4	SNAP5 ^a
CPU utilization (total)	70%	92%	89%	33%	6%
Applications	32%	45%	41%	14%	0%
Operating system overhead	37%	46%	47%	8%	6%
CPU utilization (task breakdown)					
Tracking Subsystem	2%	1%	1%	1%	0%
Telemetry Subsystem	6%	14%	14%	2%	0%
Command Subsystem	0.2%	0.2%	0.3%	1%	0%
Monitor and Ops Control Subsystem	8%	10%	10%	4%	0%
User Interface Subsystem	29%	31%	29%	10%	0%
Operating system tasks	7%	7%	7%	5%	6%
Predicts (phi-factor file) generation	15%	27%	24%	3%	0%
Sequence of events generation	—	1%	2%	5%	0%
Main core usage					
Average in use	663K	869K	966K	1016K	1024K
Average amount allocated	947K	973K	991K	1016K	1024K
Number of purges	32	195	767	1231	0
Number of requests that had to wait	0	5	80	90	0
Number of LM's scatter loaded	0	30	176	99	0
LCS Usage					
Maximum	2042K	2047K	2045K	2043K	2024K
Average	1965K	2027K	2030K	2023K	2024K
LCS GETMAIN'ed core (average)	148K	193K	195K	206K	207K
Number of LM's purged from LCS	17	32	24	0	0
I/O Utilization					
2860-2 Selector Channel					
Channel 1 (disk)	19%	23%	25%	8%	
Channel 2 (disk)	17%	19%	13%	4%	
Channel 6 (LCS)	13%	24%	31%	9%	
2870 Multiplexer Channel					
Selector subchannel 1 (tapes)	31%	29%	25%	8%	
Selector subchannel 4 (Pioneer devices)	0%	0%	0%	0%	
Printer (0F9)	13%	33%	12%	0%	
2909-3 Asynchronous Data Channel					
HSD08 (output subchannel to Ames)	77%	76%	66%	8%	
Subchannel 46x	0%	0%	0%	0%	
Printer (460)	78%	86%	92%	26%	
Task queues					
CPU					
Number	10206	15050	14812	4072	
Average time	10 ms	10 ms	8 ms	14 ms	
Core					
Number	0	11	358	1080	
Average time	—	16 ms	36 ms	554 ms	
Task response times					
Tracking	207 ms	341 ms	1109 ms	3726 ms	
Telemetry	188 ms	211 ms	337 ms	7763 ms	
Monitor and Ops Control	450 ms	314 ms	256 ms	4059 ms	
Backlog					
Tracking data	0	0	0	0	
Telemetry data	0	0	12	71	
Monitor and Ops Control data	0	0	0	3	
Input TTY and HSD lost	0	0	0	116	

^aCore lockout occurred 10 seconds into snap interval 5.

Table 10. Statistics from Run 6

Item measured	SNAP1	SNAP2	SNAP3	SNAP4	SNAP5 ^a
CPU utilization (total)	83%	95%	97%	97%	97%
Applications	40%	46%	44%	42%	48%
Operating system overhead	42%	47%	51%	53%	48%
CPU utilization (task breakdown)					
Tracking Subsystem	1%	1%	7%	9%	4%
Telemetry Subsystem	14%	17%	14%	11%	8%
Command Subsystem	0.2%	0.2%	0.2%	1%	7%
Monitor and Ops Control Subsystem	13%	14%	14%	14%	14%
User Interface Subsystem	40%	43%	44%	45%	29%
Operating system tasks	7%	8%	8%	7%	6%
Predicts (phi-factor file) generation	5%	10%	6%	5%	13%
Sequence of events generation	—	1%	2%	2%	14%
Main core usage					
Average in use	653K	835K	937K	980K	990K
Average amount allocated	927K	969K	990K	996K	992K
Number of purges	15	73	257	919	1264
Number of requests that had to wait	0	1	13	88	15
Number of LM's scatter loaded	0	5	36	206	57
LCS usage					
Maximum	1747K	1815K	1838K	1800K	1878K
Average	1695K	1773K	1804K	1843K	1863K
LCS GETMAIN'ed core (average)	216K	275K	306K	344K	364K
Number of LM's purged from LCS	0	0	0	0	0
I/O utilization					
2860-2 Selector Channel					
Channel 1 (drum)	19%	25%	27%	31%	42%
Channel 2 (disk)	5%	6%	11%	14%	15%
Channel 5 (disk)	14%	15%	15%	21%	22%
Channel 6 (LCS)	13%	16%	26%	31%	24%
2870 Multiplexer Channel					
Selector subchannel 1 (tapes)	31%	29%	30%	26%	20%
Selector subchannel 4 (Pioneer devices)	0%	0%	0%	0%	—
Printer (OF9)	13%	51%	11%	5%	—
2909-3 Asynchronous Data Channel					
HSD08 (output subchannel to Ames)	74%	71%	69%	66%	28%
Subchannel 46x	0%	0%	0%	0%	0%
Printer (460)	78%	93%	86%	76%	49%
Task queues					
CPU					
Number	12003	15320	15686	15364	2531
Average time	13 ms	16 ms	16 ms	19 ms	13 ms
Core					
Number	0	1	26	530	366
Average time	—	10 ms	17 ms	28 ms	44 ms
Task response times					
Tracking	285 ms	353 ms	314 ms	414 ms	716 ms
Telemetry	234 ms	332 ms	525 ms	1015 ms	1657 ms
Monitor and Ops Control	599 ms	375 ms	340 ms	556 ms	796 ms
Backlog					
Tracking data	0	0	71	38	35
Telemetry data	0	12	34	118	149

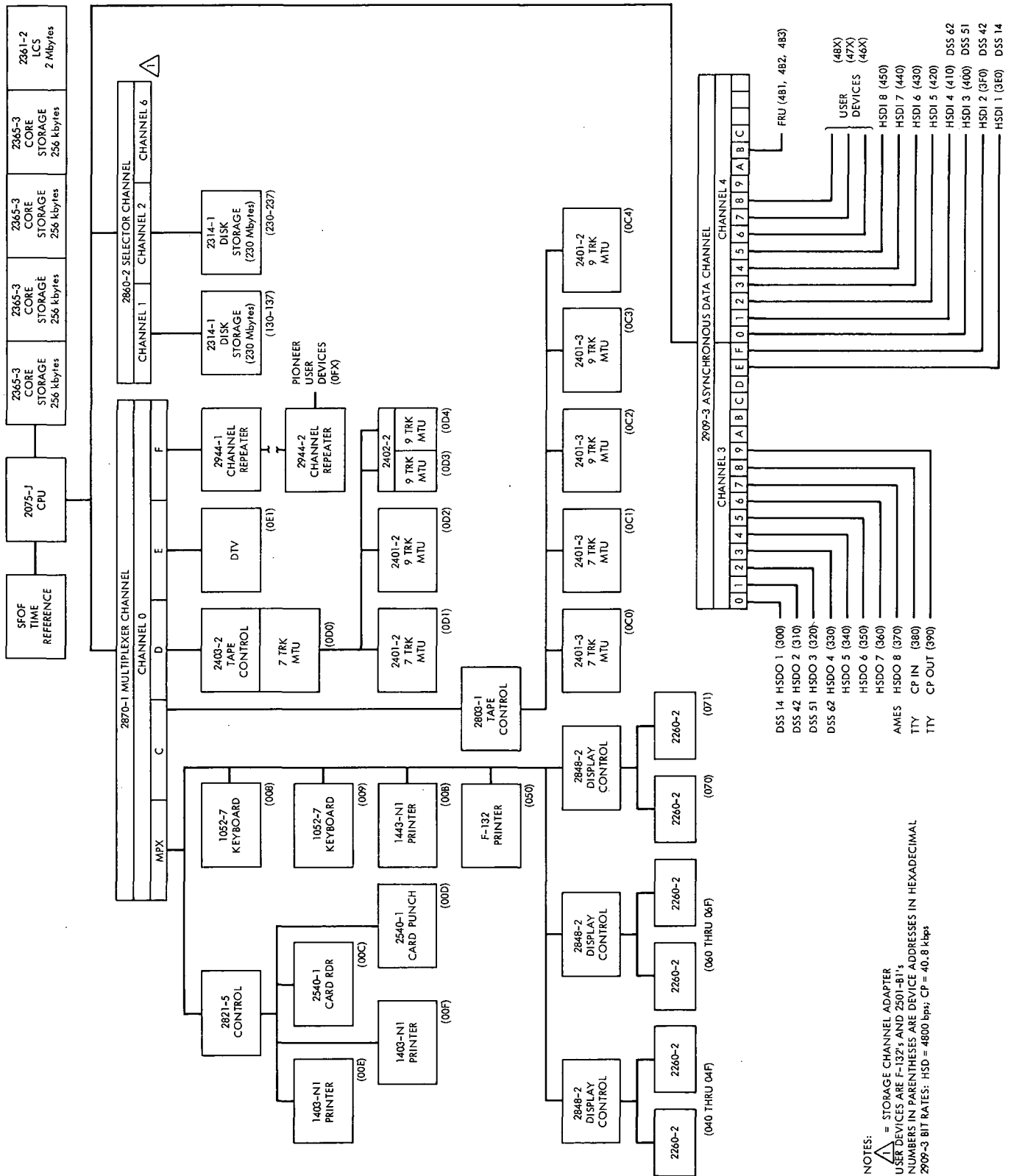
^aModel queue overflow due to backlog; 10 seconds into snap interval 5.

Table 11. Statistics from Run 7

Item measured	SNAP1	SNAP2	SNAP3	SNAP4	SNAP5
<i>CPU utilization (total)</i>	78%	98%	94%	97%	99%
Applications	40%	53%	50%	52%	55%
Operating system overhead	36%	43%	43%	43%	43%
<i>CPU utilization (task breakdown)</i>					
Tracking Subsystem	1%	1%	1%	1%	0.3%
Telemetry Subsystem	7%	15%	15%	14%	15%
Command Subsystem	0.2%	0.1%	0.2%	0.3%	0.5%
Monitor and Ops Control Subsystem	13%	13%	13%	14%	13%
User Interface Subsystem	38%	40%	40%	42%	42%
Operating system tasks	6%	7%	7%	7%	7%
Predicts (phi-factor file) generation	9%	19%	15%	15%	14%
Sequence of events generation	—	1%	1%	2%	7%
<i>Main core usage</i>					
Average in use	619K	767K	784K	791K	801K
Average amount allocated	937K	980K	957K	969K	961K
Number of purges	12	46	52	55	67
Number of requests that had to wait	0	0	0	0	0
Number of LM's scatter loaded	0	0	0	0	1
<i>LCS usage</i>					
Maximum	1723K	1770K	1770K	1834K	1850K
Average	1668K	1736K	1743K	1787K	1817K
LCS GETMAIN'ed core (average)	189K	239K	245K	288K	319K
Number of LM's purged from LCS	0	0	0	0	0
<i>I/O utilization</i>					
2860-2 Selector Channel					
Channel 1 (drum)	15%	14%	20%	22%	26%
Channel 2 (disk)	5%	4%	3%	5%	2%
Channel 5 (disk)	16%	17%	15%	15%	14%
Channel 6 (LCS)	10%	13%	14%	14%	14%
2870 Multiplexer Channel					
Selector subchannel 1 (tapes)	31%	28%	27%	27%	29%
Selector subchannel 4 (Pioneer devices)	0%	0%	0%	0%	0%
Printer (OF9)	13%	33%	13%	12%	12%
2909-3 Asynchronous Data Channel					
HSD08 (output subchannel to Ames)	74%	70%	75%	74%	72%
Subchannel 46x	0%	0%	0%	0%	0%
Printer (460)	71%	93%	93%	93%	93%
<i>Task queues</i>					
CPU					
Number	9899	13134	12905	13305	13759
Average time	13 ms	18 ms	13 ms	15 ms	12 ms
Core					
Number	0	0	0	0	0
<i>Task response times</i>					
Tracking	290 ms	273 ms	507 ms	226 ms	136 ms
Telemetry	254 ms	206 ms	211 ms	222 ms	183 ms
Monitor and Ops Control	550 ms	299 ms	283 ms	287 ms	227 ms

Table 12. Glossary of terms

CPU utilization (total)		I/O Utilization	
	Percentage of the snap interval the 360/75 CPU was in use, i.e., not idle or waiting.	Channel utilization	Percentage of the snap interval the channel was busy. For the disk channels, the channel is not made busy by seek operations.
Applications	Percentage of the snap interval the CPU was in use by a user program.	Subchannel and device utilization	Percentage of the snap interval the sub-channel or device was busy.
Operating system overhead	Percentage of the snap interval the processor was in use by the operating system servicing user requests or interrupts.	Task queues	
Main core usage		Number (No.)	
Average in use	Average amount of core in use during the snap.	CPU	Number of times tasks were queued for control of CPU. (Zero-time entries are included.)
Average amount allocated	Average amount of core in use plus the average amount allocated for inactive load modules.	Core	Number of times tasks waited while storage management attempted to satisfy their core requests.
Number of purges	The number of times during the snap that purge attempts were made to free inactive load modules to satisfy a GETMAIN request.	Average time	The average time in milliseconds that tasks were queued for the reasons stated above.
Number of requests that had to wait	The number of GETMAIN requests which caused the calling task to be delayed until sufficient main storage became available.	Task response times	The average time all tasks in the indicated category required to process a unit of work, i.e., from the time the unit (RTQEL) is activated to the final EXIT under the task.
Number of load modules scatter loaded	The number of load modules loaded into main storage in segments rather than as single blocks, due to excessive fragmentation of available storage.	Backlog	The number of unprocessed work units at the end of the snap.
LCS usage		Input TTY and HSD Lost	The number of teletype and high speed data messages discarded by the I/O interrupt processor due to its inability to obtain core.
GETMAIN'ed core	The average amount of LCS allocated via the LCS option of GETMAIN calls.	Core = (LCS, MAIN)	When executing a user GETMAIN, attempts are first made to obtain core from LCS, before main memory.
Load modules purged from LCS	The number of load modules that were purged from LCS in order to satisfy other LCS requests.		



Madrid-to-JPL 50 kbits/s Wideband Error Statistics

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Detailed analysis of the results of wideband data tests conducted at 50 kbits/s in June 1971 between Madrid and the SFOF confirms the burst nature of the transmission errors.

Measured burst length depends critically on the definition of a burst. A typical burst length of 200 bits was determined for the error model and method of measurement employed. During good circuit conditions the block error rate varies directly with block length; however, this proportionality does not hold during poor circuit conditions. The average number of error bits in an error block holds reasonably constant even as the error rate changes several orders of magnitude.

I. Introduction

During the period June 8-14, 1971, a lengthy wideband data test was conducted between the SFOF Comm Terminal at JPL and the NASCOM Madrid Switch Center adjacent to DSS 61. The test, which was run at 50 kbits/s, had two objectives: (1) to determine the error rates of a circuit generally comparable to those expected to be used in support of MVM73, and (2) to determine the statistical distribution of these errors.

An earlier report (Ref. 1) presented data on the first objective, i.e., the general error rates. This article provides information on the second objective, the fine-grained distribution of the errors.

II. Configuration

The complete test configuration is described in detail in the earlier report. The arrangement consisted of a full-duplex 50-kbit/s circuit between the SFOF Comm Terminal and the NASCOM Madrid Switch Center. The circuit was regenerated at the main NASCOM switch at the Goddard Space Flight Center. A communication satellite link was used between the United States and Spain. Test data consisted of the 2047-bit pseudo-random pattern generated by Fredricks Model 600 Test Sets (F600). The received data was normally accepted by an F600, synchronized, and the bit/block errors counted and recorded.

During two different four-hour periods, however, the receive line at JPL was diverted from the F600 and routed to the Simulation Center where the incoming bits were logged on magnetic tape by the 6050 computer. This special configuration, shown in Fig. 1, provided the raw data for the fine-grained error analysis.

The 6050 tapes were reduced by two 360/75 programs. The first program compared the recorded sequence against the known 2047 bit pseudo-random pattern, noting the distance between errors. The second program calculated various statistics from the distance-between-errors data.

During the processing of the twenty-five reels of 6050 raw data, it was determined that the information on thirteen of the reels could not be readily reduced for several reasons, including lack of knowledge of where the data stopped on each reel. These thirteen reels were subsequently discarded, since the remaining twelve sequences provided a very adequate sample (5.73×10^8 bits, about 3.17 h) distributed over several different times and line conditions.

III. Results

Table 1 depicts some statistical parameters for each of the sequences. The sequences have been divided into groups according to the bit error rate of each sequence.

Characteristics of the three groups are as follows:

Group	Bit error rate X of each sequence	Number of sequences	Proportion of the total
Green	$X < 10^{-5}$	6	48.7%
Amber	$10^{-5} < X < 10^{-4}$	5	42.2%
Red	$X > 10^{-4}$	1	9.1%

The three groups, in order, represent excellent, normal, and poor error performance.

Burst length, an important statistical quantity, was measured using the simplifying assumption that bursts are separated by at least n good bits. Credit for this simple method is given to the Bell Telephone System who has used it in arriving at some of their published data. The value of n , 400 in this case, was chosen empirically after examining a large number of data runs.

Table 1 shows the average burst length for each sequence. The longest burst, 13,636 bits, occurred in Sequence 11. The shortest burst, 17 bits, occurred in nearly every sequence and is caused by the data set scrambler, which causes three output bit errors to occur every time a line error occurs.

The block error rate is shown for three different block lengths: 1200, 2400, and 4800 bits. Lengths of 6 and 10 bits were also calculated but are not shown. At low bit error rates (green and amber groups) the block error rate is generally proportional to the block length, substantiating that the error burst is short compared to a block length. As the error rate worsens (red group) this relationship no longer holds.

Table 1 also shows values of K for the three block lengths. K represents the average number of error bits in each error block. Restated, K is the number of bad bits in each bad block. It is significant in that it indicates how badly typical blocks are mutilated. Surprisingly, K remains reasonably constant over all block sizes and color groups, even as the error rate shifts nearly two orders of magnitude and the burst length changes by nearly an order of magnitude.

The burst ratio column is the ratio of the good (error free) bits to the bad (error) bits *within* a burst. If there were 50% errors inside a burst (as you might imagine), this ratio would be 1.0. As indicated, the ratio is always well above 1.0, indicating that most of the bits within a burst are error-free. In the red group the ratio climbs to almost nine, leading to speculation that some different error-producing mechanism (other than impulse noise) must come into play when such substandard error rates are produced. Such a mechanism could be a general decrease in the S/N ratio to the point where the random noise peaks produce errors.

The last set of columns shows the quantity of various bit transitions experienced in each sequence. Using a model developed by D. Card, of the DSN Engineering and Operations Section, the circuit and its delivered bits, can be considered to always be in one of two states—burst or error-free. During the error-free state all bits are delivered without errors. During the burst state, some bits are delivered in error and some are error-free, as evidenced by the good/bad ratio discussed earlier. Each bit may thus be classified as one of three types:

0. An error-free bit occurring during a non-burst state. (This is the "normal" state which we would like all bits to occupy.)

- 1 An error bit occurring within a burst.
- 2 An error-free bit occurring within a burst.

One further note on the model: A burst always starts with an error and ends with an error. This permits a firm determination of the beginning and end of each burst and eliminates the spectre of "bursts" which contain no errors.

Using the above tags, a 0-to-0 (0-0) transition occurs between two bits, both of which are error-free and outside a burst. A 0-to-1 (0-1) transition marks the beginning of a burst and is ultimately followed by a 1-to-0 (1-0) transition at the end of the burst. The transition columns in Table 1 contain counts of each of the seven permissible types of transitions (0-2 and 2-0 transitions are not permissible since category 2 bits can only occur within a burst while 0 bits only occur outside a burst).

From the transition data presented, it is possible to construct the Card transition probability matrices shown in Table 2. These matrices depict, for each of the groups and the total, the probability of occurrence of each of the transitions. The bit types across the top represent the state of bit n and the types along the left show the state of the $n + 1$ bit. For instance, in the green group, the probability of a 1-to-2 transition is 0.500, whereas the probability of a 1-to-0 transition is 0.016. As earlier discussed, 0-2 and 2-0 transition are not permitted and are not shown in the matrix.

The matrices readily show many of the characteristics previously pointed out, the burst nature of the errors, good/bad ratio in a burst, etc.

Figure 2 is a plot of the distance between bit errors for each of the three groups. For example, for the green group there were 600 cases where bits in error were only one bit apart, i.e., they were adjacent. There were 300 cases where error bits were two bits apart, that is, there was one good bit between two error bits.

The curves all have an initial slope of $1/2^n$ up to a distance of 8-10 bits, indicating a complete burst condition where half the bits are in error and half are correct. Beyond the 8-10 bit distance the curves flatten and enter a random error region where most of the bits are good and only a few are in error. The peak at 17 bits distance is caused by the data set and is not a "natural" phenomenon.

As may be deduced from the curves (and seen in the raw data) most of the errors occur in the burst condition. The occasional random-type errors, however, generate "bursts" containing many good bits. These good bits, in turn, cause the good/bad bit ratio to climb.

The good/bad ratio (Table 1) should, therefore, be viewed with a wary eye. The values shown are true, but only for the model described and then only when the burst length is determined as previously discussed.

An alternate model has been devised which permits both burst and random errors. Future effort may be devoted to determining the parameters of this expanded model.

IV. Applicability to MVM '73

The circuit tests reported on herein were run at 50 kbits/s. The wideband network now being implemented to support MVM'73 will operate at 28.5 kbits/s. Performance at the lower rate can only be determined by measurement after the new network is installed. Nevertheless, the performance prediction for the lower rate as compared to the 50-kbits/s data presented herein is as follows:

<i>Parameter</i>	<i>Effect of decreasing rate from 50 to 28.5 kbits/s</i>
Bit error rate	No change
Burst length	Will decrease in proportion to rate decrease
Block error rate	Will increase in inverse proportion to rate decrease
K	Will decrease in proportion to rate decrease
Burst good/bad ratio	No change
Transition probabilities	No change

V. Conclusions

- (1) The typical burst length ($200 \pm$ bits) is short compared to the present wideband block length (1200 bits).

- (2) The number of bits in error per block in error (K) is reasonably constant over large changes in bit error rate.
- (3) The idea that most of the bits in a burst are error-free must be tempered with the definition of what constitutes a burst. Most of the errors actually occur in tight groups. Within these groups the bits are nearly totally random.
- (4) Most of the time the error rate is better than the average. In fact, this gets even more so as the sample interval is decreased.

Reference

1. McClure, J. P., "Ground Communications Facility 50-kbps Wideband Data Error Rate Test," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VI, pp. 149-151. Jet Propulsion Laboratory, Pasadena, Calif., Dec. 15, 1971.

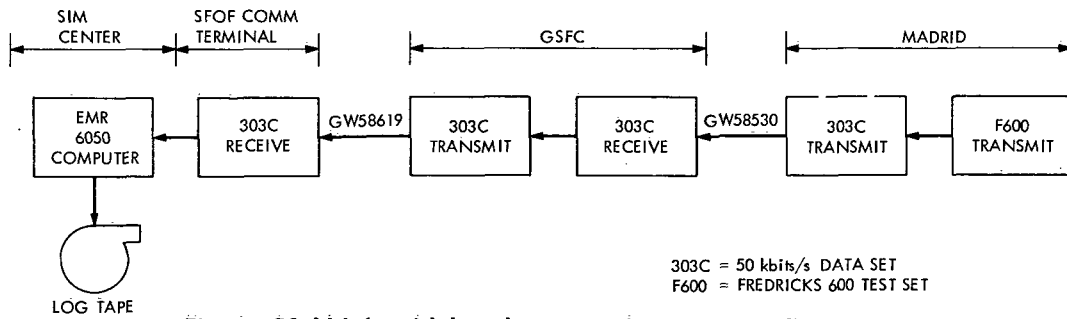


Fig. 1. 50-kbit/s wideband error statistics test configuration

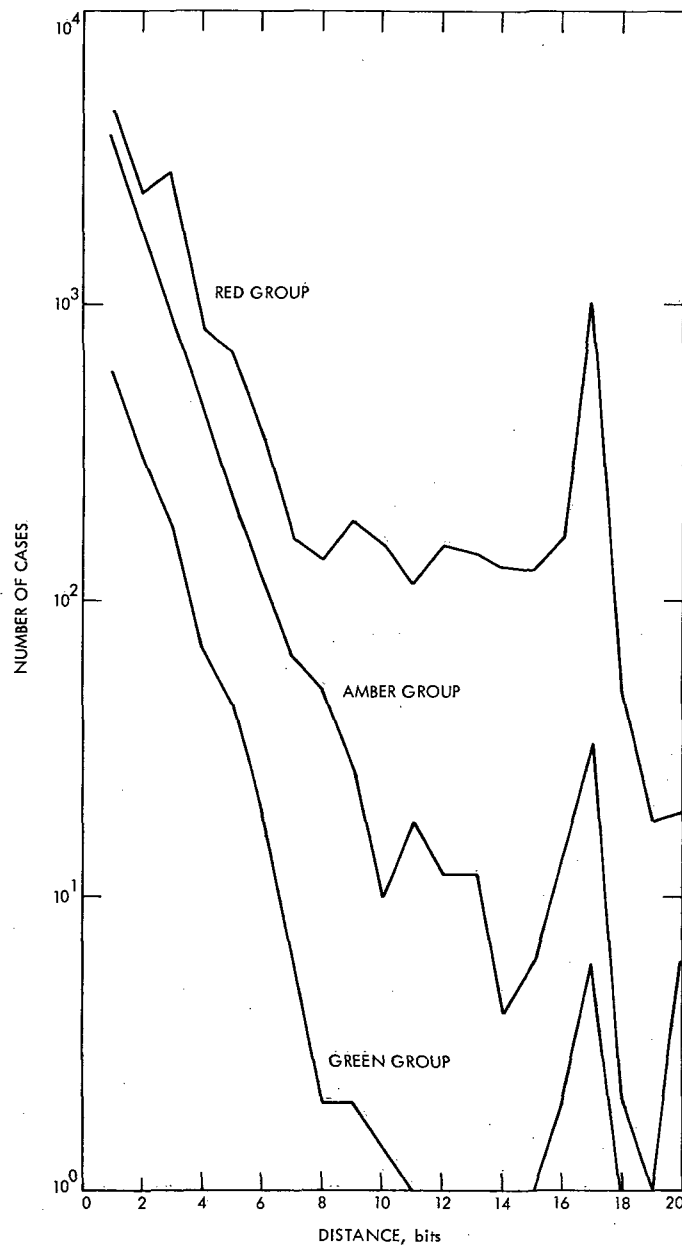


Fig. 2. Distance between bit errors

Group	Sequence No.	Total bits	Bits in error	Bit error rate	Number of bursts	Average burst length	Block error rate		
							1200	2400	4800
Green	13	51451345	87	0.0000017	3	132.0	0.0000700	0.0001399	0.0002799
	14	46043171	260	0.0000056	4	151.5	0.0001043	0.0002085	0.0004170
	15	41468126	229	0.0000055	3	216.0	0.0001158	0.0001736	0.0003473
	16	44651211	177	0.0000040	3	178.0	0.0000806	0.0001613	0.0003225
	17	44301174	233	0.0000053	3	188.0	0.0001084	0.0002167	0.0003251
	18	51389935	248	0.0000048	4	171.2	0.0000934	0.0001868	0.0003736
Amber	3	39198003	2009	0.0000509	35	167.4	0.0012552	0.0022655	0.0041636
	6	42681997	1747	0.0000409	13	481.2	0.0004780	0.0007872	0.0014620
	8	62300445	1150	0.0000185	16	165.6	0.0003274	0.0005393	0.0010016
	19	54343756	1233	0.0000227	22	146.9	0.0005079	0.0009274	0.0018550
	20	43441434	1554	0.0000357	18	216.1	0.0005801	0.0009392	0.0017680
Red	11	52020411	15203	0.0002922	100	1513.9	0.0047982	0.0057670	0.0069207
Green total		279304962	1234	0.00000442	20	171.1	0.0000945	0.0001804	0.0003437
Amber total		241965635	7592	0.00003138	104	226.4	0.0005901	0.0010216	0.0019242
Red total		52020411	15203	0.0002922	100	1513.9	0.0047982	0.0057670	0.0069207
Grand total		573291008	24029	0.00004191	224	1037.6	0.0007305	0.0010424	0.0016076

Table 1. Error statistics

Average K			Burst good/bad ratio	Transitions						
1200	2400	4800		0-0	0-1	1-1	1-0	1-2	2-1	2-2
29.00	29.00	29.00	3.552	51450945	3	40	3	44	44	265
64.75	64.75	64.75	1.335	46042560	4	119	4	136	136	211
57.25	76.33	76.33	1.830	41467474	3	111	3	115	115	304
59.0	59.0	59.0	2.017	44650673	3	96	3	78	78	279
58.25	58.25	77.67	1.421	44300606	3	104	3	126	126	205
62.0	62.0	62.0	1.762	51389245	4	127	4	117	117	320
48.76	54.03	58.79	1.921	39192109	35	917	35	1047	1047	2812
102.71	124.71	134.31	2.581	42675727	13	859	13	874	874	3636
67.71	82.21	88.54	1.304	62297778	16	622	16	512	512	988
53.61	58.71	58.71	1.621	54340501	22	541	22	670	670	1329
74.0	91.41	97.13	1.503	43437525	18	759	18	777	777	1559
73.08	121.61	202.68	8.957	51868923	100	4695	100	10406	10406	125780
56.09	58.76	61.70	1.783	279301503	20	597	20	616	616	1584
63.80	73.71	78.27	1.871	241943640	104	3698	104	3880	3880	10324
73.08	121.61	202.68	8.957	51868923	100	4695	100	10406	10406	125780
68.85	96.50	125.15	6.350	573114066	224	8990	224	14902	14902	137688

Table 2. Card transition probability matrices

Green set	0	1	2
0	$1 - (7.17 \times 10^{-8})$	0.016	—
1	7.17×10^{-8}	0.484	0.280
2	—	0.500	0.720
Amber set	0	1	2
0	$1 - (4.30 \times 10^{-7})$	0.014	—
1	4.30×10^{-7}	0.481	0.273
2	—	0.505	0.727
Red set	0	1	2
0	$1 - (1.93 \times 10^{-6})$	0.007	—
1	1.93×10^{-6}	0.309	0.076
2	—	0.684	0.924
Total set	0	1	2
0	$1 - (3.91 \times 10^{-7})$	0.009	—
1	3.91×10^{-7}	0.373	0.098
2	—	0.618	0.902

Prototype S- and X-Band Feed System Hardware

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The hardware for supporting the prototype S- and X-band feed system on the 64-m-diameter antenna is described. The S-band ellipsoid reflector is supported on flexures which provide for thermal expansion. The X-band dichroic/S-band flat reflector assembly consists of a welded assembly of aluminum plates with provisions to mount the X-band transparent sheet.

I. Introduction

The S- and X-band feed system on the 64-m-diameter antenna will provide simultaneous S-band diplexed operation and X-band receiving capabilities along the same RF boresight direction. The functional descriptions of the physical hardware assemblies were noted in Ref. 1, and the radio frequency techniques were described in Ref. 2.

This article describes the hardware designs of the reflectors and their supporting system. Photographs of the top portion of the supporting truss for the ellipsoid undergoing fabrication are included. The descriptive photos of the dichroic plate assembly will follow in later articles along with detailed descriptions of the retraction mechanisms.

Additional analyses of radio frequency techniques are found in another article¹ in this technical report.

¹See "S- and X-Band RF Feed System," by P.D. Potter in this issue.

II. Hardware Design Description

The ellipsoid reflector over the S-band feed horn of the tricone RF feed system is supported by an aluminum truss assembly attached to the S-band cone. Mechanism will be provided for retraction of the ellipsoid reflector from the S-band RF boresight line and allow normal use of the feed horn with the Tricone Cassegrain System.

The ellipsoid will be formed from 3.2-mm (0.125-in.)-thick 1100-H14 aluminum sheet. This material was selected because of its availability from stock (large width requirement) and its high electrical conductivity, which should minimize the RF surface current losses and the resulting heating effects on the ellipsoid's shape. A special drop hammering process will form the dish-like shape. With the use of an egg-crate type of male form, to be described in detail in a later article, the ellipsoid shape may be qualified continuously during the shaping process.

To provide for thermal expansion of the ellipsoid reflector, it will be mounted from the truss structure by a flexure-type of tangential shear supporting means. The

flexures consist of 1.7-mm (0.06-in.)-thick aluminum sheets fastened to the nonagon-shaped mounting face of the supporting truss structure. By attaching these sheets to the ellipsoid sheet with clips at short intervals, the ellipsoid is effectively supported by a round-like tube of approximately 1.7-m (64-in.) diameter. The nonagonal shape of the tube provides for both the thermal expansion of the ellipsoid by the bending action of the flexures and its rigid support from the nonagonal truss face by the flexures' tangential shear stiffness.

Figure 1 shows the nonagonal-faced truss being fabricated on a fixture plate. A close-up is shown in Fig. 2 with a round fixture spacer in place.

The combination S-band flat reflector and X-band dichroic plate assembly will be 1.58 m (62 in.) in diam-

eter and supported from the X-band cone. The assembly will also be retractable by a mechanism under remote control. This movement provides for use of the other experimental feed horns on the X-band cone in the normal Cassegrainian system.

The 1.58-m (62-in.)-diameter flat will be a welded fabricated assembly of aluminum plates forming a boxed structure with an opening covered by the dichroic plate.

III. Future Work

The retraction mechanisms for both reflectors will be described in a future article. Means to control the heat distortions of the dichroic plate when it is reflecting the 450-kW S-band RF will also be discussed later.

References

1. Katow, M., "S- and X-Band RF Feed System," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VI, pp. 139-141. Jet Propulsion Laboratory, Pasadena, Calif., Dec. 15, 1971.
2. Potter, P. D., "S- and X-Band RF Feed System," in *The Deep Space Network Progress Report*, Technical Report 32-1526, Vol. VIII, pp. 53-60. Jet Propulsion Laboratory, Pasadena, Calif., Apr. 15, 1972.

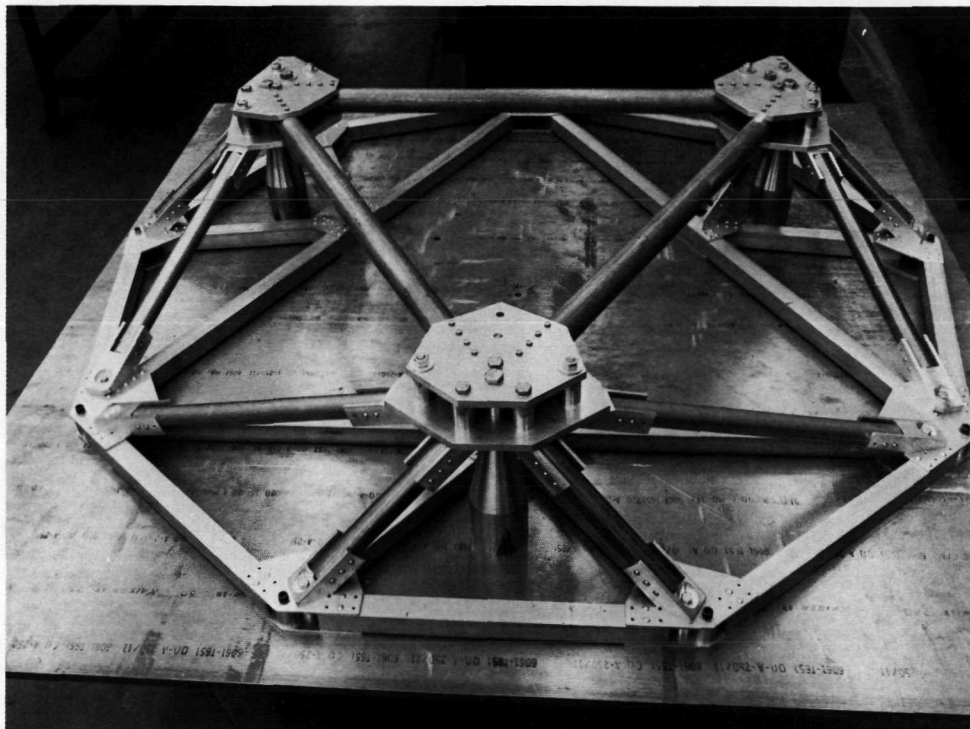


Fig. 1. Ellipsoid support truss

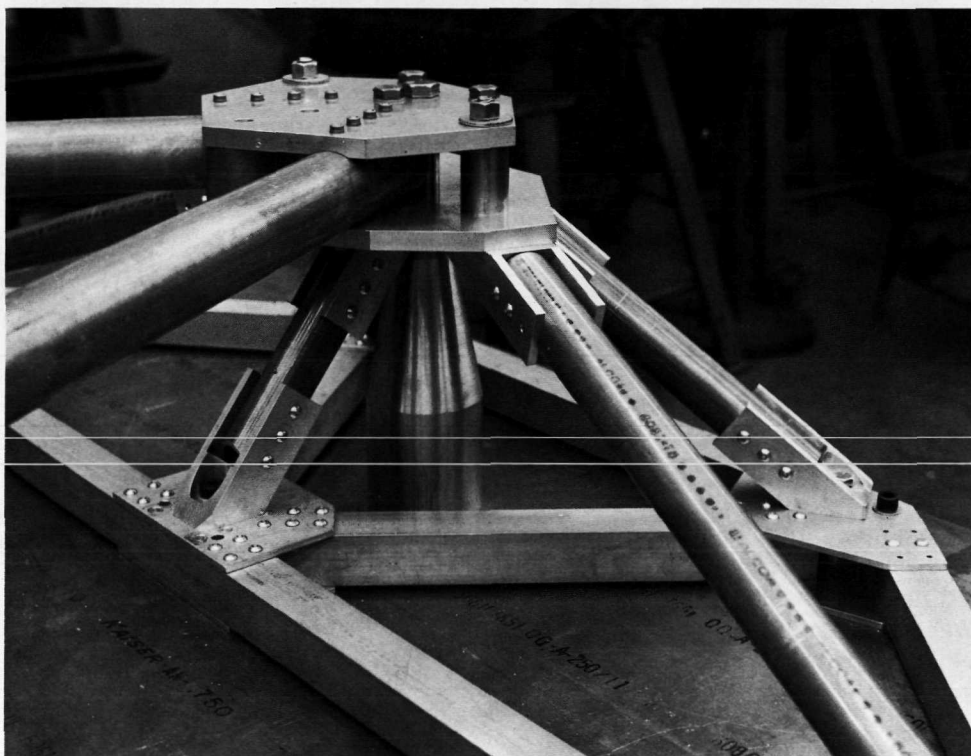


Fig. 2. Ellipsoid support truss close-up

Firmware Control of Block IV Ranging Demodulator Assembly

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The Mark III Data System Development Plan is encouraging engineers designing equipment for use in the Deep Space Network to utilize computer control and monitoring. It is becoming apparent that the difficulty of development and cost of software are prohibitive. A concept called firmware is proposed. Firmware is a design concept which directs the engineer to employ special-purpose digital and/or analog circuitry whenever possible to reduce software or interface requirements. The Ranging Demodulator Assembly (RDA) is being developed under the firmware concept. By employing firmware, the RDA interface and software requirements have been kept to a minimum. The phase calibration of the RDA is achieved with a single switch or one-line command from the computer. Monitoring is handled by the firmware which supplies one line to the computer indicating the operability of the RDA.

I. Introduction

The Mark III Data System Development Plan (DSDP) is encouraging engineers designing equipment for use in the Deep Space Network to utilize computer control and monitoring. It is tempting for the circuit designers to design and build equipment as in the past and simply use the computer as a substitute for man. This approach requires the computer to be programmed to perform those operations, both open loop and closed loop, that have been performed manually in the past. It is becoming apparent, however, that the difficulty of development and cost of software are perhaps prohibitive. The Command System, for example, was designed to operate with a symbol rate of one kilobit per second. This machine was built with the idea in mind that the computer would monitor and control all possible functions, and it was

subsequently found that under computer operation the symbol rate was reduced to a maximum of 1.6 bits per second. The limitations were due to the number of operations imposed upon the computer to perform in real time. Our observations lead us to two conclusions concerning computer-controlled hardware:

- (1) Computer-controlled hardware should be designed and built to minimize the number of functions to be controlled and monitored by the machine.
- (2) Software to control computer-controlled hardware should be kept to a minimum by judicious design of the hardware to be controlled.

The Block IV Ranging Demodulator Assembly (RDA) is being designed based on these two conclusions.

II. Firmware

Firmware as used here is a system design concept directed toward optimizing the interface between a computer and the hardware it controls. The firmware concept is to employ special-purpose digital and/or analog circuitry whenever possible to reduce software or interface requirements. The circuitry is developed from a flow chart which describes the operations and sequence to be performed. We are employing firmware in both control and monitor applications.

The expense of developing software is reduced by performing repetitive operations with firmware. Software development cost is therefore reduced by the elimination of control and monitor subroutines. Additionally, costs are reduced because the engineer most familiar with the hardware to be controlled is the one developing the control and monitor circuitry.

The use of firmware will save significant time in the real-time operations of the computer since the computer will not have to perform closed-loop operations but will only be required to signal to the firmware to do its special-purpose job. The firmware will flag the computer at the completion of its task. The ensuing time can be utilized by the computer to perform jobs with other pieces of hardware or computational tasks. Computer time will also be economized since the machine will not have to observe a large number of monitor points but will simply monitor a few firmware outputs to determine the total health and operability of the hardware.

There are also advantages due to firmware accruing to manual control. Since the firmware can be used by the controlling computer to perform simple repetitive tasks, it will likewise be available to the man operating the machine or checking out the machine when the computer is not in control. Hence, phase calibration of an RDA will be achieved by the operator depressing a single pushbutton. Another advantage that will accrue to manual control through the use of firmware is the uniformity of the control of the machine. Jobs performed by firmware will always be performed in the same sequence, thereby eliminating any variance due to differences between operators.

With the use of firmware to perform control and monitor operations, there will be a reduction in the complexity of the interface with the computer. There will be, for instance, fewer lines, or points, for the computer to monitor to determine operability. A particular operation

involving a control loop will require only one line from the computer since the firmware will handle the control and monitor required to close the loop.

III. Block IV RDA Control Unit

A simplified block diagram of the Ranging Demodulator Assembly is shown in Fig. 1. The firmware may be conveniently divided between that firmware applied to monitor and that firmware applied to control. One example of each of these two categories of firmware is discussed below beginning with monitor firmware.

A. Monitor Firmware

The monitor firmware approach is to compare the control input with the state of the controlled device. If the result disagrees with the control input, an alarm is initiated. This technique is applied wherever possible in a module, and the results are logically combined into one alarm. In the RDA this approach is used to monitor the reference phase shifters and also the input attenuator. Housed within the IF and phase switch module in the RDA is an eight-bit digital attenuator. This attenuator is comprised of eight switched T-pad attenuators under control of a binary weighted word. Shown in Fig. 2 is the attenuator confirmation firmware flow chart. The firmware compares the state of the command line with the condition of the relay and signals an alarm if the two are different. This is repeated for each of the eight attenuator steps. The alarm indicators are then combined into a single line that controls the confirmation lamp on the front panel of the control unit and will also be available to the computer as a monitor of the operational capability of the input attenuator of the RDA.

B. Phase Calibrate Firmware

The 10-MHz signal in the Ranging Demodulator Assembly is coherently detected in the bandpass amplifier and coherent amplitude detector (CAD) module. Phase calibration is achieved when the reference is aligned with the ranging modulation which is equivalent to being orthogonal to the carrier. Figure 3 is a simplified diagram of the coherent amplitude detector and the phase calibrate hardware of the RDA. The scheme employed by the firmware phase control, in very general terms, is to step the control voltage to the linear analog phase shifter by one least-significant bit (LSB) and then, after a suitable delay, to take account of the lowpass delay characteristic of the dc amplifier, to initiate an analog-to-digital (A/D) conversion and observe the most-significant bit

(MSB). When an occurrence of sign change occurs (MSB changes state), the direction of steps into the digital-to-analog converter (D/A) is reversed, and the next step to the linear analog phase shifter will be in the opposite direction. Therefore, if one were to observe the analog control voltage to the phase shifter during a phase calibrate cycle, one would observe that the voltage ramps upward (in LSB steps) until the analog output of the coherent amplitude detector/lowpass amplifier reaches zero, at which time the control voltage would oscillate up and down in increments of one least-significant bit of the D/A converter. The output of the D/A converters will step for approximately 46 seconds (256 counts), which is guaranteed to be adequate to ramp the phase shifters to a null.

The phase calibrate firmware may be examined in more detail by studying Fig. 4, phase calibrate firmware flow chart, and Fig. 5, phase calibrate firmware (which is offered as an aid in understanding the flow chart). A phase calibrate operation may be initiated by either an operator or the computer. Given a request for a phase calibrate cycle from either of these two sources, a start pulse is generated. Without reference to the order in which they occur, the following operations are performed by the start pulse:

- (1) The Channel 1 and Channel 0 up/down counter indicated by the position of the SOURCE selector switch (RCV 1, RCV 2, PHASE) on the front panel of the RDA control unit is set to one quarter of its full-scale value. This aspect of the initialization is done in order to guarantee that the final value of the phase angle will not be at one end of the linear region of the phase shifter.
- (2) The initial sign (IS) one-shot is enabled.
- (3) The clock counter (CC) is cleared. The clearing operation generates the PHASING signal.

The PHASING signal generated in paragraph (3), above, performs a sequence of initializing operations which are enumerated below:

- (1) Release the up/down counter gates selected by the SOURCE selector switch so that the control voltage can begin to ramp toward its final value.
- (2) Light the PHASE CALIBRATE lamp.

- (3) Enable the delay counter (DC) which will be used to delay the up/down count long enough for the MSB/ $\overline{\text{MSB}}$ of the A/D converter to reach its final value each cycle.
- (4) Start the clock.

The clock pulse performs two operations. It increments the clock counter and initiates an A/D converter start pulse (ADC ST). The ADC ST pulse sets the delay counter to its starting value and also initiates a conversion by both the Channel 0 and Channel 1 A/D converters. If the last increment of the clock counter pushed its sum to final value, then the clock will be halted and the PHASING signal will be inhibited. Since the PHASING signal is used as a gating signal to the up/down counters, the up/down counters will be halted at their present values.

Several cycles of the Channel 0 A/D clock output are counted by the delay counter to generate a delayed clock pulse. In general, the delayed clock pulse is used to increment or decrement the appropriate up/down counters based upon the state of the current most significant bit as compared to the initial sign (sign of output at start of counting). If the initial sign and most significant bit agree, the counters will be incremented, thereby causing the circuitry to seek the null closest to the midrange of the phase shifter. If they disagree, the counter will be decremented. The state of the initial sign is determined after a delay of four delayed clock pulses. The four-count delay is necessary in order to give the lowpass filter in the output of the CAD time to respond to the initial setting of the phase shifter.

Time delay between a clock pulse and an up/down count is approximately 10 microseconds. Hence there is about 180 milliseconds between one count and the next. The above operations are repeated each 180 milliseconds for 256 times, which is sufficient to step the D/A converters through the entire range of the phase shifters. After the cycle is repeated 256 times the CADs are phased to within ± 3 degrees of optimum and the PHASE CALIBRATE indicator is extinguished. The firmware will remember (for both channels) the control voltage required for any SOURCE (RCV 1, RCV 2, PHASE) used during the calibrate cycle. This feature permits the operator/computer to phase calibrate, prior to a mission, RCV 1 and RCV 2 in case receivers need to be changed during the mission.

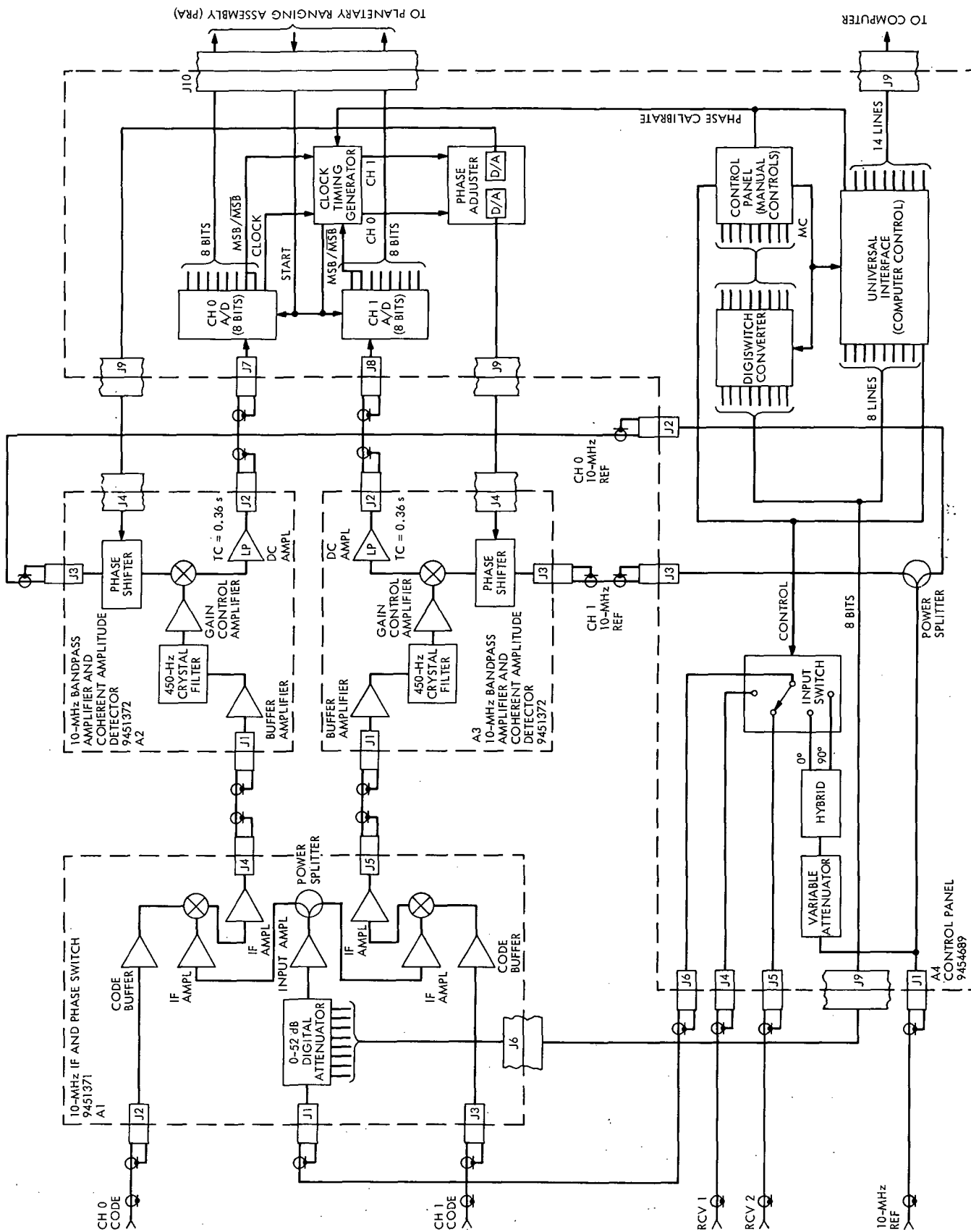


Fig. 1. Functional block diagram of the ranging demodulator assembly

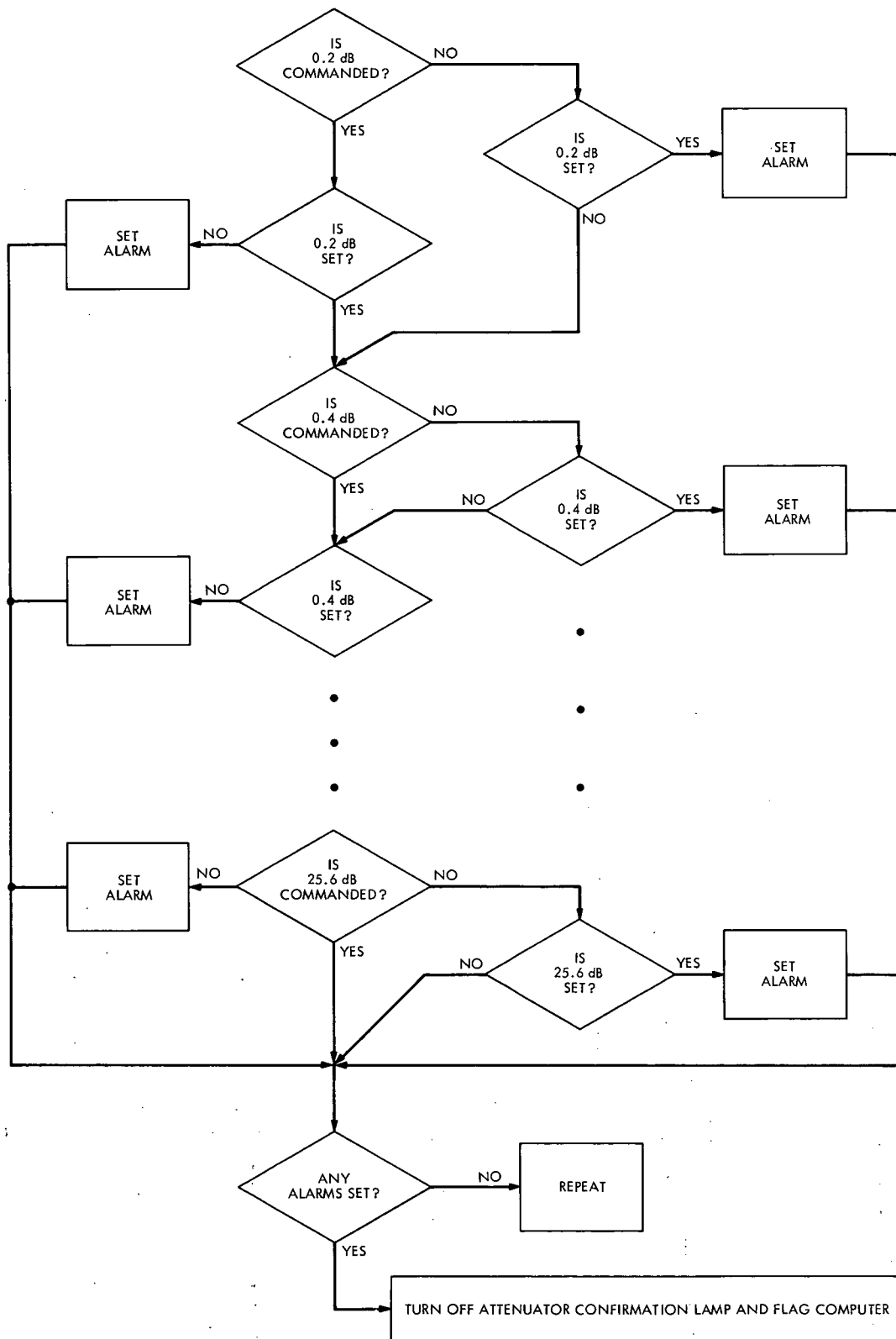


Fig. 2. Attenuator confirmation firmware flow chart

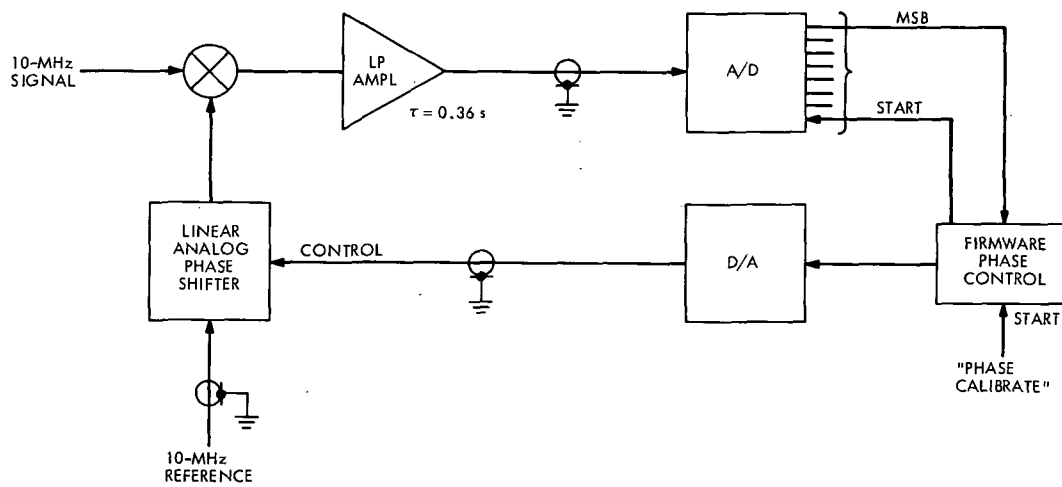
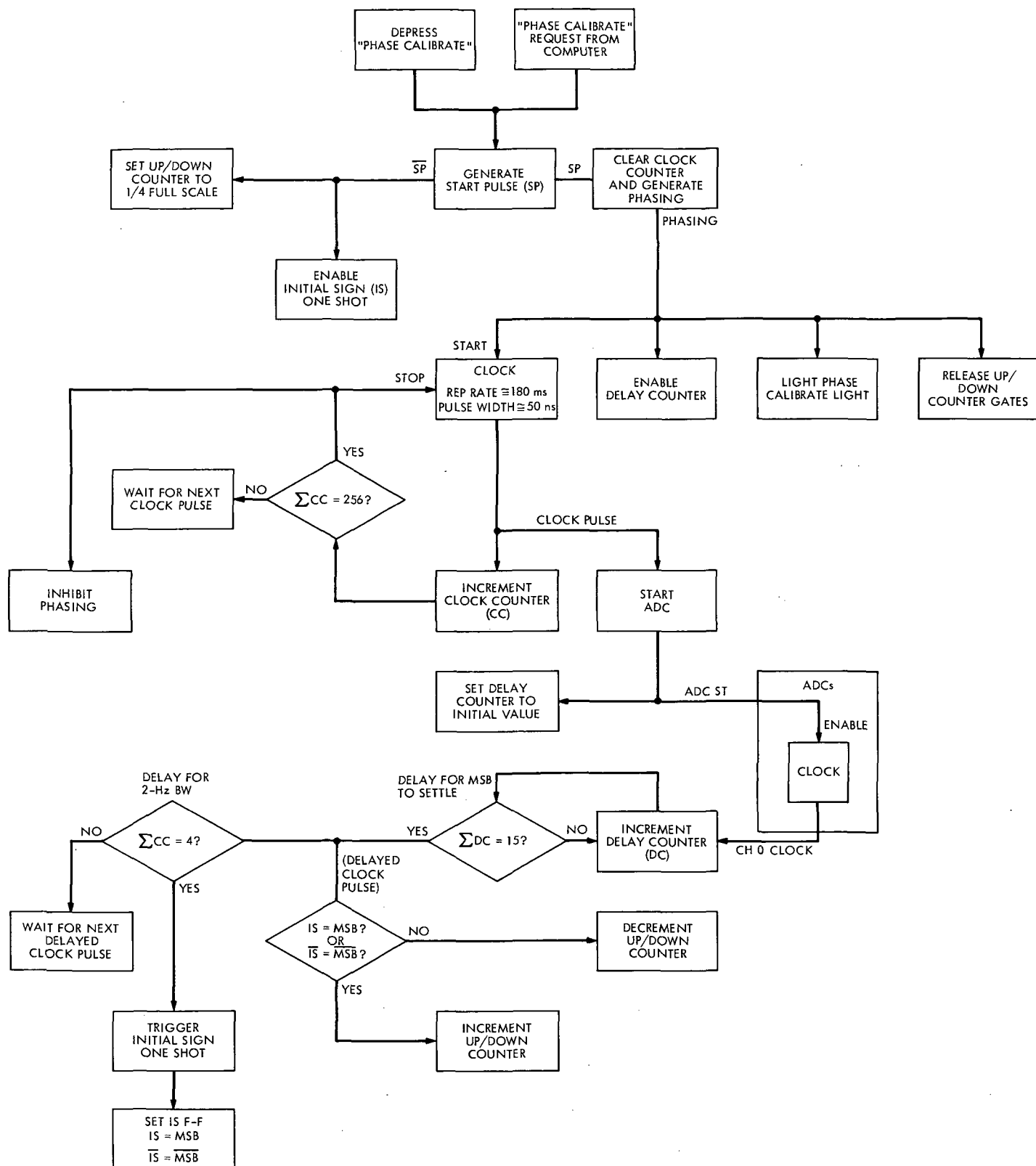


Fig. 3. Coherent amplitude detector



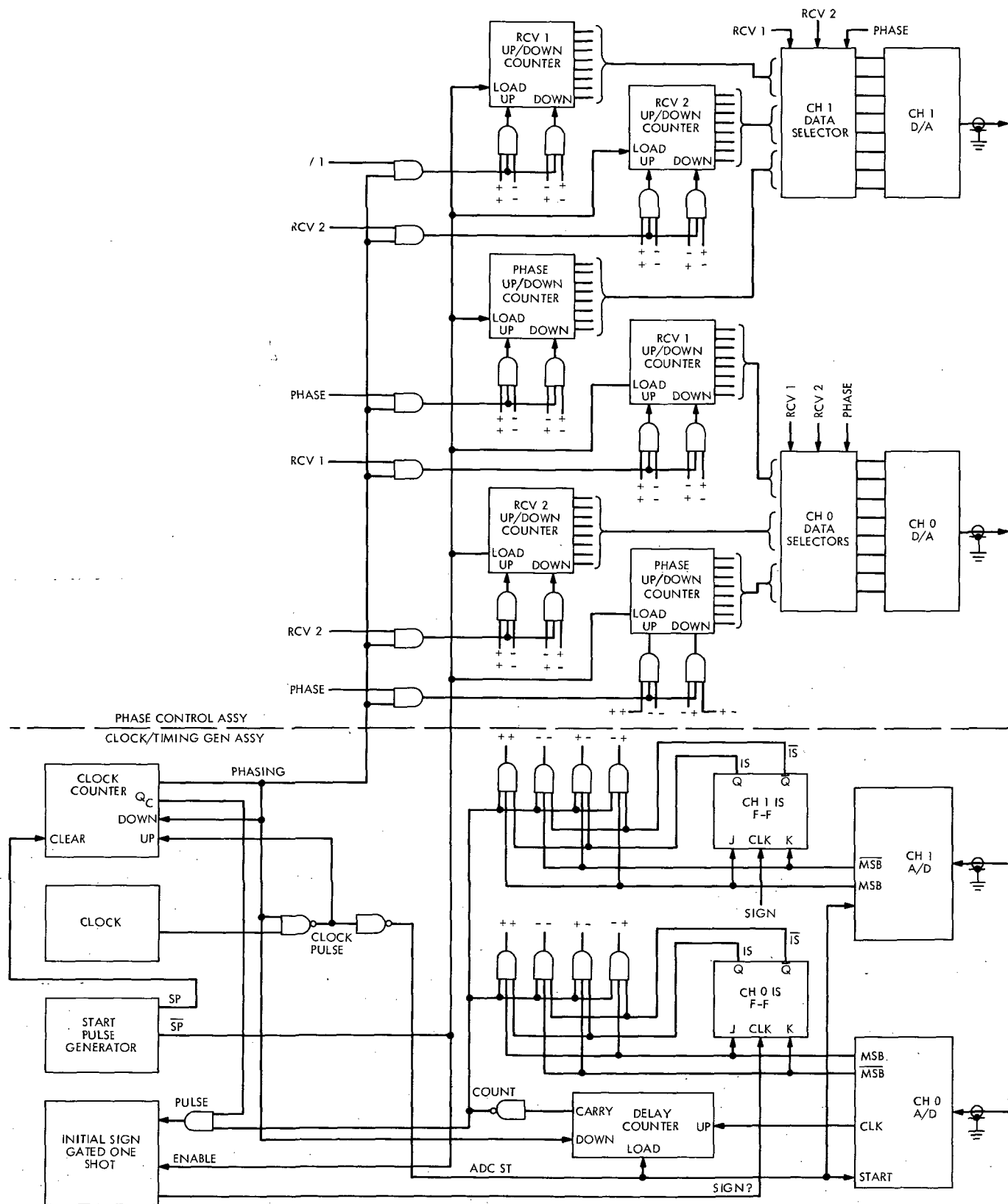


Fig. 5. Phase calibrate firmware

10-W S-Band Amplifier

R. H. Smith

R. F. Systems Development Section

A more powerful S-band amplifier was needed to drive the high-power transmitters of the Deep Space Network. Two types of 10-W solid-state amplifiers with 23-dB gain and operating at 2115 MHz for the DSN 400-kW transmitter and 2388 MHz for the 450-kW R&D transmitter were developed.

I. Introduction

This report covers the development of two S-band amplifiers for operation with high-power DSN and R&D transmitters. During the development of the 400-kW transmitter and the development of the 450-kW R&D transmitter it was determined that a more powerful buffer amplifier than the triode amplifier used in the Block IIIC receiver/receiver exciter chain was needed. Two S-band 10-W solid-state amplifiers were developed for this purpose (Fig. 1.) The specifications for these two amplifiers are listed in Table 1 for the 2115-MHz DSN amplifier, and Table 2 for the 2388 R&D amplifier.

II. Description

A three-stage Class C amplifier was developed (Fig. 2.) This Class C amplifier turns on very abruptly at approximately 50 mW of drive and is completely saturated 2 or

3 mW beyond this point. The first stage consists of a single transistor with a gain of 12 dB. The second stage is also a single transistor with a gain of 9 dB. The third stage consists of two transistors with inputs and outputs combined by hybrids. A circulator with a load is placed on the output of the second hybrid. The circulator is used to maintain a constant 50- Ω load to the last stage of the amplifier and to protect it in the event of an open- or short-circuit load. Normally the amplifier is intended to operate into a VSWR of 1.2:1.

The two amplifiers are identical with two exceptions. The first exception is that the circuitry is scaled to appropriate frequency for each amplifier. The second exception is a resistor in the supply circuit used to drop the voltage to the first and second stages, thereby reducing the gain of these stages for the 2115-MHz DSN amplifier.

III. Performance

Fourteen 2115-MHz DSN amplifiers have been evaluated. Six of these have outputs between 11 and 12 W. Five have outputs between 12 and 13 W. Two have outputs between 13 and 14 W, and one has an output in excess of 14 W. Six 2388-MHz R&D amplifiers have been evaluated. Two amplifiers have an output between 11 and 12 W, and four units have an output in excess of 12 W. A typical frequency response is shown in Fig. 3. The units have a response that is flat within 0.5 dB from 2070 to 2200 MHz. The requirement is ± 1 dB from 2105 to 2125 and ± 0.5 dB from 2110 to 2120 MHz. All spurious harmonics up to the fifth are at least 40 dB down from the fundamental.

IV. Problem Area

During the development of the two amplifiers several problems were encountered. All of them have been solved with the exception of one. The first problem encountered was with the 2388-MHz R&D amplifier. When the first 2388-MHz R&D amplifier was being bench-tested at JPL, the output of the amplifier dropped to zero. An extensive investigation showed that the circulator used would handle only 4 W CW, and that the 10-W output level of

the amplifier had burned out the circulator. A new higher-power circulator was installed by the manufacturer and the amplifier was retested. No problems with the circulator have occurred since this change. The first 2115-MHz DSN amplifier was tested at JPL and installed for evaluation at DSS 13. After several weeks of operation the output of the amplifier dropped to zero. An investigation made into the problem showed that the first two stages were overdriving the third stage. To correct this problem a resistor was used to drop the supply voltage to the first and second stages thereby reducing their gain. A second 2115-MHz amplifier was placed on evaluation test at DSS 13. This amplifier performed properly for about two weeks at which time the output dropped 3 dB due to a defective solder connection on one of the two output transistors. Overdriving the input to the amplifiers above 100 mW may cause the first-stage base emitter junction to break down. A warning has been issued to all operating personnel using these amplifiers to be very cautious in applying drive to the amplifiers.

All the problems encountered have occurred with very few hours of operation accumulated on each amplifier. A policy of testing each amplifier on the bench for 14 straight days, running 24 h a day, has eliminated these early failures.

Table 1. 2115-MHz amplifier specifications

Output	10 W (+40 dBmW) min
Input	50 mW (+17 dBmW) max
Supply voltage	$+28 \pm 0.5$ Vdc
Supply current	2 A max
Frequency response	
2105 to 2125 MHz	± 1 dB
2110 to 2120 MHz	± 0.5 dB
Spurious harmonics (2, 3, 4 and 5 down from fundamental)	-35 dB
Stability	Unconditional
Load VSWR	1.2:1 max
No damage	Any VSWR
Temperature operation	10 to 50°C

Table 2. 2388-MHz amplifier specifications

Output	10 W (+40 dBmW) min
Input	50 mW (+17 dBmW)
Supply voltage	28 ± 0.5 Vdc
Supply current	2 A max
Frequency response	
2383 to 2393 MHz	± 1 dB
Spurious harmonics (2, 3, 4 and 5 down from fundamental)	-35 dB
Stability	Unconditional
Load VSWR	1.3:1 max
No damage	Any VSWR
Temperature operation	10 to 50°C

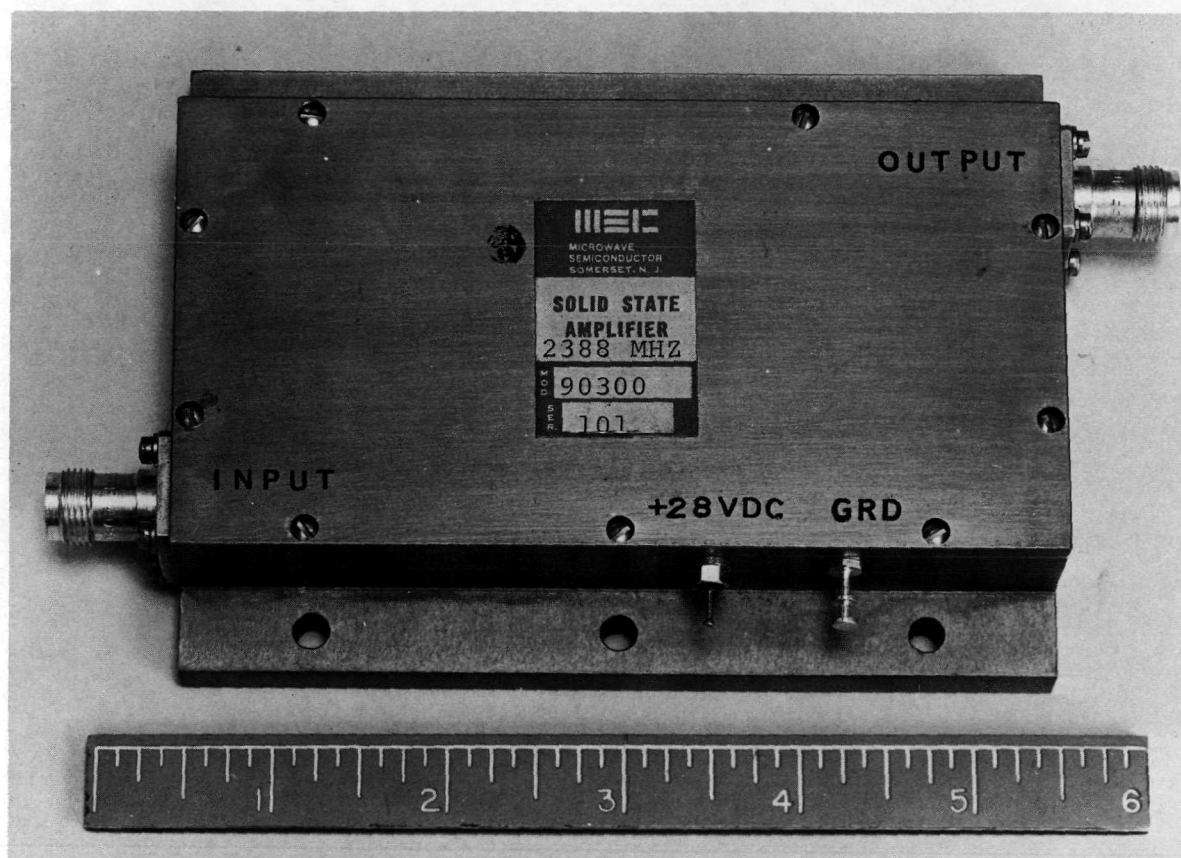


Fig. 1. Solid-state 10-W 5-band amplifier

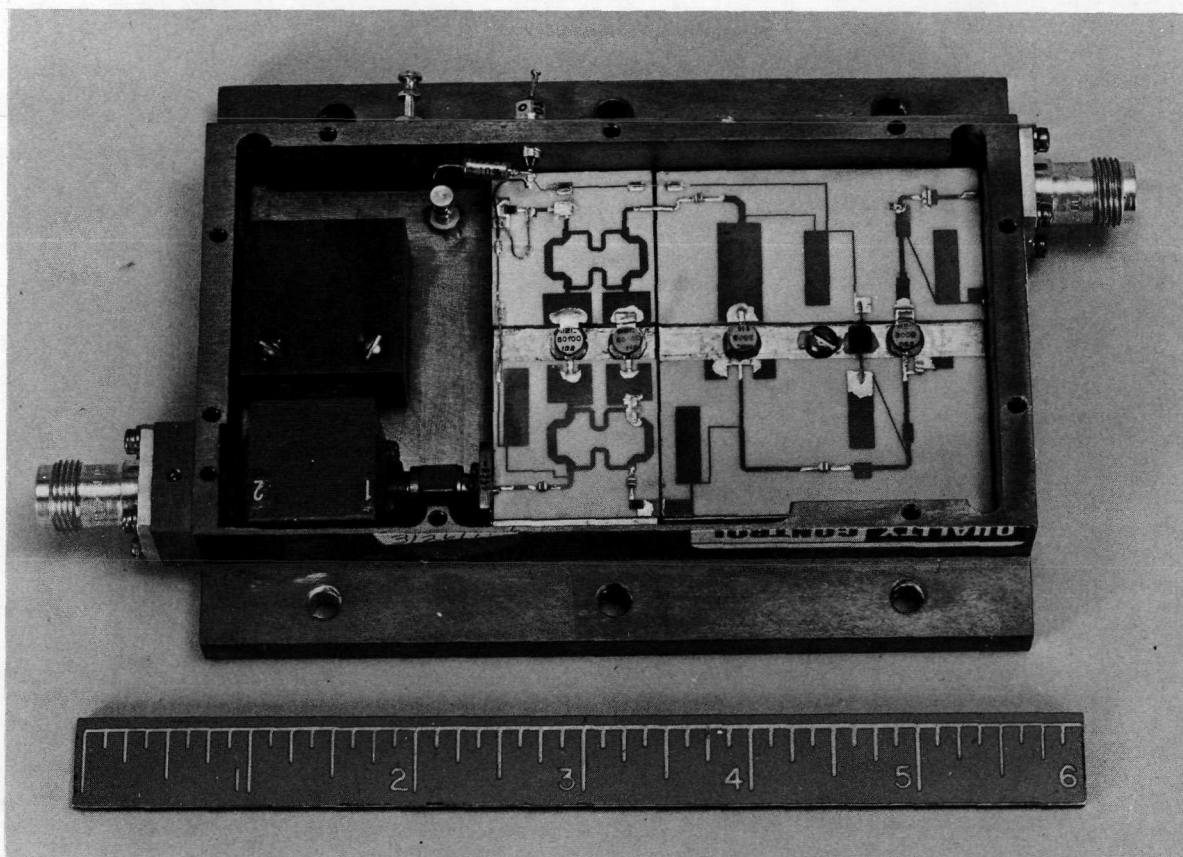


Fig. 2. Solid-state 10-W S-band amplifier with cover removed

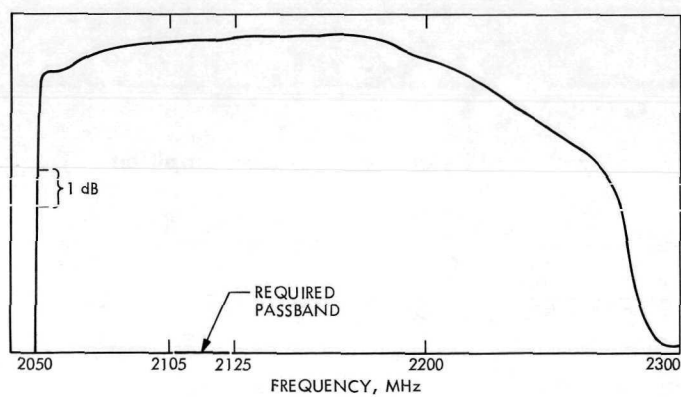


Fig. 3. S-Band amplifier output and passband output versus frequency

Effects of the Pioneer 10 Antenna Polarization and Spacecraft Rotation as Seen in the Radio Metric Data

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The Pioneer 10 antenna polarization and spacecraft rotation introduce a signature into the radio metric doppler data, which, unless otherwise noted, might be confused with a degradation of the tracking system. This signature, especially in regard to effects as seen in doppler residuals and doppler noise, is here analyzed in detail.

I. Introduction

Certain unusual effects are introduced into the Pioneer 10 radio metric data due to the fact that the spacecraft antenna is circularly polarized and that the spacecraft itself is rotating, combined with the fact that the spin axis of the spacecraft is aligned at various angles with the Earth/spacecraft line of sight.

The Network Analysis Team/Tracking Group (NAT TRK) is charged with continuously monitoring the Pioneer 10 radio metric data in order to assess the performance of the tracking system. It was therefore necessary for the Network Operations Analysis Tracking Group to analyze the polarization and rotation effects so that the spacecraft effects can be separated from possible system contributions. Briefly, the antenna polarization adds a bias to the radio metric data, while the spacecraft rotation adds a sinusoidal "ripple" to the data, which, of

course, increases the data noise. These two effects are now examined in detail.

II. Pioneer 10 Antenna Polarization Effects

The antenna on Pioneer 10 is both rotating and right-hand circularly polarized. In this case, the received signal can be thought of as a rotating vector with the frequency being equal to the number of rotations of this vector per unit time. For each complete rotation of the antenna, the number of counts lost from the frequency in two- or three-way is:

$$2 + \frac{19}{221}$$

This is due to one count being lost when the signal is received, and 240/221 of a count being lost after the spacecraft multiplies the signal by 240/221 and transmits it:

$$\text{Total} \left\{ \begin{aligned} 1 + \frac{240}{221} &= 1 + \frac{221}{221} + \frac{19}{221} \\ &= 2 + \frac{19}{221} \end{aligned} \right.$$

For one way, the number of counts lost from the frequency for each complete rotation is 1.

Since the antenna rotation rate is approximately 4.85 rev/min, the number of counts in the data over 1 min will be

$$\begin{aligned} -4.85 \left(2 + \frac{19}{221} \right) & \quad 2,3 \text{ way} \\ -4.85 & \quad 1 \text{ way} \end{aligned}$$

and the equivalent biases to be observed in the data will be

$$-4.85 \left(2 + \frac{19}{221} \right) / 60 = -0.168616 \text{ Hz for 2,3 way}$$

and

$$-4.85/60 = -0.08083 \text{ Hz for 1 way}$$

III. Pioneer 10 Spacecraft Rotation Effects

The *Pioneer 10* spacecraft has three conditions which cause a sinusoidal "ripple" in the radio metric data (i.e., the spacecraft antenna is alternately moving with a small velocity toward and away from the ground observer). These three conditions are:

- (1) The spacecraft is rotating.
- (2) The spacecraft spin axis does not coincide with the Earth line of sight.
- (3) The antenna center point is not on the spacecraft spin axis.

The antenna geometry is presented in Fig. 1 where

$$r = 8 \text{ in.} = 0.2032 \text{ m}$$

$$\omega = \text{rotation rate (nominally 4.85 rev/min)}$$

$$\phi_{\text{MAX}} \cong 24 \text{ deg}$$

As per the above figure, a ground observer sees a back-and-forth antenna movement (velocity) of:

$$V = r\omega' \sin \phi \sin \omega't$$

Converting from rev/min to rad/s, we have

$$\omega' = \frac{\omega \text{ rev}}{\text{min}} \cdot \frac{2\pi \text{ rad}}{\text{rev}} \cdot \frac{\text{min}}{60 \text{ s}}$$

$$\omega' = \frac{2\pi\omega}{60} \frac{\text{rad}}{\text{s}}$$

so that the velocity is

$$V = r \sin \phi \left\{ \frac{2\pi\omega}{60} \right\} \sin \frac{2\pi\omega}{60} t$$

Since the standard radio metric sample rate is 60 s, we are most interested in how much effect this sinusoidal movement will have over a 60-s doppler sample. To do this, we integrate the velocity over a 60-s interval and divide by the sample rate:

$$\begin{aligned} \frac{1}{T} \int_{\gamma}^{\gamma+T} V(t) dt &= \frac{1}{60} \int_{\gamma}^{\gamma+60} V(t) dt \\ &= \frac{1}{60} \int_{\gamma}^{\gamma+60} r \sin \phi \left\{ \frac{2\pi\omega}{60} \right\} \sin \frac{2\pi\omega}{60} t dt \end{aligned}$$

We also need to find the particular time γ which causes the integral to be a maximum. To accomplish this, we require the following condition:

$$\frac{\partial}{\partial \gamma} \left\{ \frac{1}{60} \int_{\gamma}^{\gamma+60} r \sin \phi \left\{ \frac{2\pi\omega}{60} \right\} \sin \frac{2\pi\omega}{60} t dt \right\} = 0$$

Or, since in regard to the integration, the term

$$\frac{r \sin \phi}{60} \left\{ \frac{2\pi\omega}{60} \right\}$$

is constant, we have

$$\frac{\partial}{\partial \gamma} \int_{\gamma}^{\gamma+60} \sin \frac{2\pi\omega}{60} t dt = 0$$

As regards differentiation under the integral sign, we have the general relationship:

If

$$H(\alpha) = \int_{g_0(\alpha)}^{g_1(\alpha)} F(x, \alpha) dx$$

we then have

$$\begin{aligned}\frac{\partial H}{\partial \alpha} &= \int_{\rho_0}^{\rho_1} \frac{\partial F(x, \alpha)}{\partial \alpha} dx - F(g_0, \alpha) \frac{\partial g_0}{\partial \alpha} \\ &\quad + F(g_1, \alpha) \frac{\partial g_1}{\partial \alpha}\end{aligned}$$

Substituting into the above equation, we have

$$\begin{aligned}\frac{\partial}{\partial \gamma} \int_{\gamma}^{\gamma+60} \sin \frac{2\pi\omega}{60} t dt \\ &= \int_{\gamma}^{\gamma+60} \frac{\partial}{\partial \gamma} \left\{ \sin \frac{2\pi\omega}{60} t \right\} dt - \sin \frac{2\pi\omega}{60} \gamma \frac{\partial}{\partial \gamma} (\gamma) \\ &\quad + \sin \frac{2\pi\omega}{60} (\gamma + 60) \frac{\partial}{\partial \gamma} (\gamma + 60) \\ &= \sin \frac{2\pi\omega}{60} (\gamma + 60) - \sin \frac{2\pi\omega}{60} \gamma \\ &= \sin \left(\frac{2\pi\omega\gamma}{60} + 2\pi\omega \right) - \sin \left(\frac{2\pi\omega}{60} \gamma \right) \\ &= 0\end{aligned}$$

using the trigonometric identity

$$\sin(A+B) = \sin A \cos B + \cos A \sin B$$

we have

$$\begin{aligned}\sin \frac{2\pi\omega}{60} \gamma \cos 2\pi\omega + \cos \frac{2\pi\omega}{60} \gamma \sin 2\pi\omega \\ - \sin \left(\frac{2\pi\omega\gamma}{60} \right) = 0\end{aligned}$$

Let

$$\sin \frac{2\pi\omega}{60} \gamma = x$$

$$\cos 2\pi\omega = a$$

Then, since

$$\cos^2 A + \sin^2 A = 1$$

we have

$$\cos \frac{2\pi\omega}{60} \gamma = \sqrt{1 - \left(\sin \frac{2\pi\omega}{60} \gamma \right)^2} = \sqrt{1 - x^2}$$

and

$$\sin 2\pi\omega = \sqrt{1 - (\cos 2\pi\omega)^2} = \sqrt{1 - a^2}$$

so that

$$xa + \sqrt{1-x^2}\sqrt{1-a^2} - x = 0$$

$$x(a-1) + \sqrt{(1-x^2)(1-a^2)} = 0$$

$$x(1-a) = \sqrt{(1-x^2)(1-a^2)}$$

$$x^2(1-a)^2 = (1-x^2)(1-a^2)$$

$$x^2(1-a) = (1-x^2)(1+a)$$

$$x^2(1-a+1+a) = 1+a$$

$$x^2 = \frac{1+a}{2}$$

$$x = \pm \sqrt{\frac{1+a}{2}}$$

$$x = \pm \sqrt{\frac{1+\cos 2\pi\omega}{2}}$$

$$\sin \frac{2\pi\omega}{60} \gamma = \pm \sqrt{\frac{1+\cos 2\pi\omega}{2}}$$

and

$$\left(\sin \frac{2\pi\omega}{60} \gamma \right)^2 = \frac{1+\cos 2\pi\omega}{2}$$

$$1 - \left(\cos \frac{2\pi\omega}{60} \gamma \right)^2 = \frac{1+\cos 2\pi\omega}{2}$$

$$\left(\cos \frac{2\pi\omega}{60} \gamma \right)^2 = \frac{1-\cos 2\pi\omega}{2}$$

$$\cos \frac{2\pi\omega}{60} \gamma = \pm \sqrt{\frac{1-\cos 2\pi\omega}{2}}$$

To produce a maximum, we require

$$-\frac{\pi}{2} < \frac{2\pi\omega}{60} \gamma < 0$$

so that the conditions for a maximum become

$$\sin \frac{2\pi\omega}{60} \gamma = - \sqrt{\frac{1+\cos 2\pi\omega}{2}}$$

$$\cos \frac{2\pi\omega}{60} \gamma = + \sqrt{\frac{1-\cos 2\pi\omega}{2}}$$

We can now solve for the maximum velocity in a 60-s sample:

$$\begin{aligned}
\frac{1}{T} \int_{\gamma}^{\gamma+T} V(t) dt &= \frac{1}{60} \int_{\gamma}^{\gamma+60} r \sin \phi \left(\frac{2\pi\omega}{60} \right) \sin \frac{2\pi\omega}{60} t dt \\
&= \frac{r \sin \phi}{60} \left(\frac{2\pi\omega}{60} \right) \int_{\gamma}^{\gamma+60} \sin \frac{2\pi\omega}{60} t dt \\
&= \frac{r \sin \phi}{60} \left(\frac{2\pi\omega}{60} \right) \left[-\frac{60}{2\pi\omega} \cos \frac{2\pi\omega}{60} t \right]_{\gamma}^{\gamma+60} \\
&= -\frac{r \sin \phi}{60} \left[\cos \frac{2\pi\omega}{60} t \right]_{\gamma}^{\gamma+60} \\
&= -\frac{r \sin \phi}{60} \left[\cos \frac{2\pi\omega}{60} (\gamma + 60) - \cos \frac{2\pi\omega}{60} \gamma \right]
\end{aligned}$$

Using the trigonometric identity

$$\cos(A + B) = \cos A \cos B - \sin A \sin B$$

we have

$$\begin{aligned}
&= -\frac{r \sin \phi}{60} \left[\cos \frac{2\pi\omega}{60} \gamma \cos 2\pi\omega \right. \\
&\quad \left. - \sin \frac{2\pi\omega}{60} \gamma \sin 2\pi\omega - \cos \frac{2\pi\omega}{60} \gamma \right]
\end{aligned}$$

and substituting the conditions for a maximum into the above equations, we have

$$\begin{aligned}
\frac{1}{T} \int_{\gamma}^{\gamma+T} V(t) dt &= -\frac{r \sin \phi}{60} \left[\sqrt{\frac{1 - \cos 2\pi\omega}{2}} \cos 2\pi\omega \right. \\
&\quad \left. + \sqrt{\frac{1 + \cos 2\pi\omega}{2}} \sin 2\pi\omega - \sqrt{\frac{1 - \cos 2\pi\omega}{2}} \right]
\end{aligned}$$

Using $\omega = 4.85$ we have

$$\cos 2\pi\omega = 0.58779$$

$$\sin 2\pi\omega = -0.80902$$

$$\sqrt{\frac{1 - \cos 2\pi\omega}{2}} = 0.45399$$

$$\sqrt{\frac{1 + \cos 2\pi\omega}{2}} = 0.89101$$

Therefore

$$\begin{aligned}
\frac{1}{T} \int_{\gamma}^{\gamma+T} V(t) dt &= -\frac{r \sin \phi}{60} \{ (0.45399) (0.58779) \\
&\quad + (0.89101) (-0.80902) - 0.45399 \} \\
&= -\frac{r \sin \phi}{60} \{ 0.26685 - 0.72084 - 0.45399 \} \\
&= -\frac{r \sin \phi}{60} \{ -0.90798 \} \\
\frac{1}{T} \int_{\gamma}^{\gamma+T} V(t) dt &= -\frac{r \sin \phi}{60} \{ 0.90798 \}
\end{aligned}$$

We wish to know the period of this sinusoidal "ripple" in the data. Since we are sampling at 60 s and the frequency is 4.85 rev/min, the new period will be

$$\begin{aligned}
\frac{60 \text{ s}}{5.00 - 4.85} &= 400 \text{ s} \\
&= 6.67 \text{ min}
\end{aligned}$$

We therefore expect to see in the data a sine wave of amplitude

$$\frac{r \sin \phi}{60} \{ 0.90798 \}$$

and of period

$$400 \text{ s}$$

We would now like to verify this in the actual pseudo-residual output. On March 13, 1972, the Earth line of sight/spin axis angle was approximately 24° and $r = 8$ in. $= 0.2032$ m.

This would give us an amplitude of

$$\begin{aligned}
\frac{r \sin \phi}{60} \{ 0.90789 \} &= \frac{(0.2032) (0.40674)}{60} (0.90798) \\
&= 0.0012507 \text{ m/s}
\end{aligned}$$

and using 15.28 Hz/m/s, we have

$$= 0.019111 \text{ Hz}$$

Figure 2 consists of pseudo-residual two-way doppler residuals from DSS 11 on March 13, through which an arbitrary sine wave of amplitude 0.020 Hz and of period 400 s has been fit. As can be seen, the data is in good agreement with the modeled effect. With a sine wave of

this magnitude, one would expect a doppler noise figure of approximately 0.012 Hz, and this is quite close to the average noise value of 0.011 Hz observed in the two-way doppler data during the period when the Earth line of sight/spin axis was 24 deg and the doppler sample rate was 60 s.

For 1-s doppler samples, a sinusoid with the full amplitude V

$$\begin{aligned} V &= r \sin \phi \left\{ \frac{2\pi\omega}{60} \right\} \\ &= (0.2032) (0.4067) (0.5079) \\ &= 0.04197 \text{ m/s} \\ &= 0.64130 \text{ Hz} \end{aligned}$$

should be visible in the data. On March 11, DSS 51 took 2-way, 1-s sample doppler data. These data showed a sinusoid of period 12.364 s and of amplitude 0.55 Hz. The small discrepancy between the calculated amplitude and the observed amplitude in the 1-s data is not explainable at this time.

IV. Conclusion

In summary, the *Pioneer 10* antenna polarization and rotation introduces a bias of -0.168616 Hz into the two-

way doppler data. This is quite small and in general is masked by the fact that the predicts usually have an absolute error of greater than 0.1 Hz at any given time. The *Pioneer 10* rotation also causes a sinusoid of period 400 s and of amplitude

$$\begin{aligned} & - \frac{r \sin \phi}{60} \left[\sqrt{\frac{1 - \cos 2\pi\omega}{2}} \cos 2\pi\omega \right. \\ & \left. + \sqrt{\frac{1 + \cos 2\pi\omega}{2}} \sin 2\pi\omega - \sqrt{\frac{1 - \cos 2\pi\omega}{2}} \right] \end{aligned}$$

to be introduced into the 60-s data. During the time when

$$\phi = 24 \text{ deg}$$

$$\omega = 4.85 \text{ rev/min}$$

$$r = 0.2032 \text{ m}$$

the expected amplitude was 0.01911 Hz, and both the calculated period and amplitude agree very well with the observed data as seen in Fig. 2. This also produces an expected noise in the two-way 60-s sample doppler data of approximately 0.012 Hz, which closely agrees with the noise actually observed in the data.

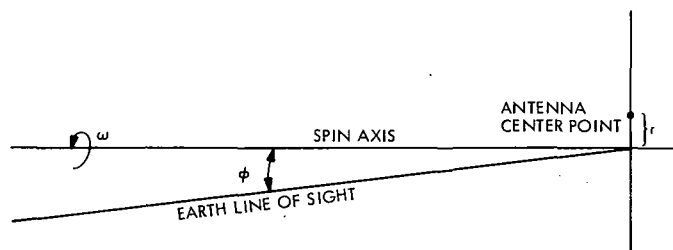


Fig. 1. Antenna geometry

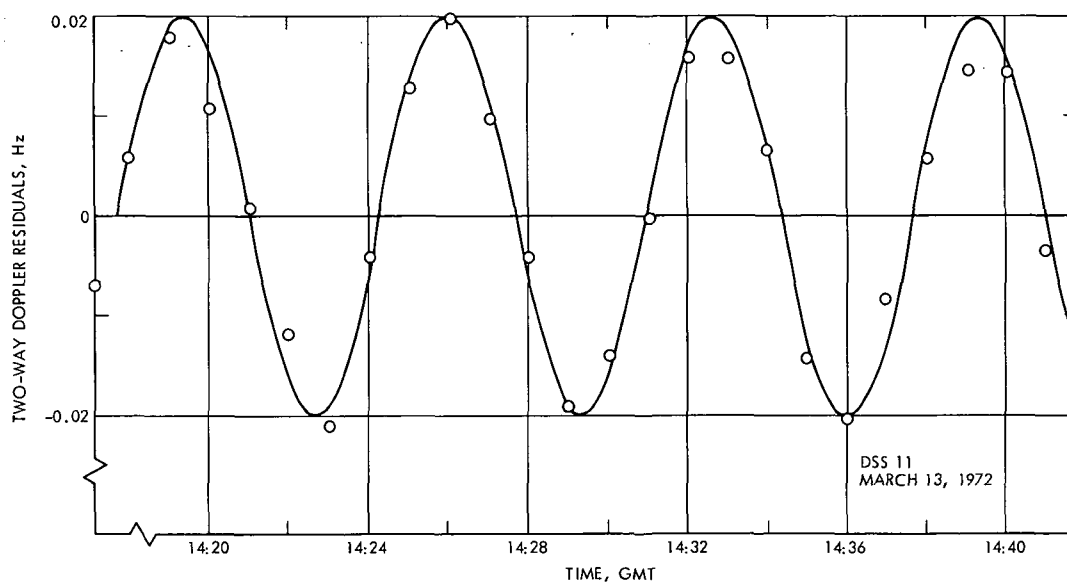


Fig. 2. Pioneer 10 two-way doppler versus time

Carrier Power Estimation Accuracy

J. Lesh

DSIF Operations Section

In this article estimation theoretic techniques are used to derive expressions for the accuracy of the digital instrumentation subsystem (DIS) and telemetry and command processor (TCP) computer methods of carrier power estimation. Upon evaluation of these expressions it is found that the TCP method is presently far more accurate than the DIS method. A procedure by which the DIS accuracy can be greatly improved is also presented.

I. Introduction

At present there are two automated methods for estimating the incoming carrier signal power at the DSIF receivers. Both of these methods involve evaluation of polynomial expressions of the receiver automatic gain control (AGC) voltage. The coefficients of these polynomials are determined during a pre-track calibration period by applying least squares curve fitting techniques to a set of carrier power versus AGC voltage data pairs. The two estimation methods differ only in the number of calibration data pairs supplied, the range over which calibration data pairs are obtained, the degree of curve fitting attempted and the sampling scheme used to measure the AGC voltage during actual operation.

The first of these methods resides in the DIS monitor computer. Calibration of this method involves establish-

ing ten signal power levels covering the full dynamic range of the receiver. For each of these levels the DIS computer samples the resulting receiver AGC voltage, takes 1000 samples within a one-second period and forms a sample mean. The least squares fitting algorithm operates on the resulting ten pairs of data to determine either a third-order or second-order fitted polynomial. During operation the AGC voltage is sampled at a sampling interval of 1.0 seconds and a mean is computed after five samples. The calibration polynomial is then evaluated using this mean to produce an estimate of the received carrier power.

The second method utilizes the TCP computer in essentially the same way as the DIS computer is used in the above method. Calibration in this case consists of establishing three power level-AGC voltage pairs cover-

ing an 8-dB range which is centered around the expected power level for the pass. These three pairs of data are then approximated by a first order least squares polynomial. During operation the AGC voltage is also sampled using a 1.0-second sampling interval. In this case, however, each AGC voltage sample is used to produce a signal power estimate.

To study the errors associated with these methods we shall first consider the errors resulting from the calibration (i.e., curve fitting) process. At first this may appear to be a classical problem of parameter estimation well documented in the literature. For example, if we define the parameter ρ to be a vector whose components are the ideal polynomial coefficients, the matrix H to be the transformation taking ρ into the noise-free observables (calibration power levels), and the vector n to be the vector of observation noise then it is a well-known result (see, for example, Ref. 1) that the minimum variance estimate of ρ and the resulting mean square error are functions of the matrix H and the covariance matrix of the noise vector n . However, in our problem there are three deviations from the classical model. These are:

- (1) The dimension of the ideal parameter is unknown.
- (2) The dimension of the estimated parameter will be less than (or at most equal to) the ideal parameter.
- (3) Over the set of observations the noise variance may vary over several orders of magnitude, yet the curve fitting algorithms in the DIS and TCP assume equal uncertainty in these observations.

The only deviation which causes any significant difficulty is the first. Consequently, the dimension of the ideal parameter will be approximated using as much insight as possible.

After evaluating the calibration errors the operational errors will be considered and the total estimation accuracies computed. In doing this we will find that the TCP method of estimation is more accurate than the DIS method, provided the received power level is within the range of the TCP calibration. Techniques by which the accuracy of the DIS method can be improved will also be presented.

II. Calibration Accuracy

A. Determination of the Noise-Free Model

In order to begin the analysis, we need some model for the ideal (noise free) carrier power versus AGC

voltage curve. To determine this model, extensive data were taken at each of the six Deep Space Stations. Using the station operating noise temperature, the variance of each AGC voltage was computed. These data, consisting of from 17 data pairs (for DSS 14) to 40 data pairs (for DSS 12), were then exercised by a curve fit subroutine available in the Univac 1108. This subroutine (Ref. 2) examines polynomials of degree less than or equal to some specified maximum (NMAX) which minimize the weighted mean square error, where the weighting is performed in accordance with the user's *a priori* estimate of the observation errors. The coefficients of the highest degree polynomial which produces a significant decrease in this weighted mean square error are then outputted from the subroutine. Note that the degree of this polynomial will not necessarily be NMAX since the remaining higher order polynomials may produce only an insignificant decrease in the mean square error.

The above program was executed for each set of data and for $NMAX = 2, 3, 4, \dots, 10$. The following observations were made on the results:

- (1) In all cases a sizable reduction in the mean square error occurred when NMAX (and subsequently the degree of the fitted polynomial) was allowed to increase to three.
- (2) In all cases where NMAX exceeded three, the subroutine either retained the third-order polynomial or fitted higher order polynomials with only a slight decrease in the mean square error.

Based on these observations we can model the ideal signal power y given the AGC voltage (x) by

$$y = a_0 + a_1x + a_2x^2 + a_3x^3 \quad (1)$$

where a_i , $i = 0, 1, 2, 3$ are the coefficients of the third-order polynomial determined by the subroutine and will be different for each receiver (data set).

B. Derivation of the Mean Square Estimation Error

Using this noise-free model we can now derive the expressions for the mean-square estimation error for each of the curve-fitting algorithms.

1. *Third-order curve fitting.* For a specific value of AGC voltage x let the corresponding power level be given by Eq. (1) and let the estimated power level be given by

$$\hat{y} = b_0 + b_1x + b_2x^2 + b_3x^3 \quad (2)$$

Then, the mean-square error conditioned on a value of x is given by

$$\begin{aligned}
 E\{(y - \hat{y})^2/x\} = & E\{(a_0 - b_0)^2\} + 2E\{(a_0 - b_0)(a_1 - b_1)\}x \\
 & + [2E\{(a_0 - b_0)(a_2 - b_2)\} + E\{(a_1 - b_1)^2\}]x^2 \\
 & + 2[E\{(a_1 - b_1)(a_2 - b_2)\} + E\{(a_0 - b_0)(a_3 - b_3)\}]x^3 \\
 & + [2E\{(a_1 - b_1)(a_3 - b_3)\} + E\{(a_2 - b_2)^2\}]x^4 \\
 & + 2E\{(a_2 - b_2)(a_3 - b_3)\}x^5 + E\{(a_3 - b_3)^2\}x^6 \quad (3)
 \end{aligned}$$

Now, if we define the ideal coefficient vector $\mathbf{a}$ and the estimated coefficient vector $\mathbf{b}$ by

$$\mathbf{a} = \begin{bmatrix} a_0 \\ a_1 \\ a_2 \\ a_3 \end{bmatrix} \quad \mathbf{b} = \begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ b_3 \end{bmatrix} \quad (4)$$

and consider the coefficient estimation error covariance matrix

$$\mathbf{G} = E\{(\mathbf{a} - \mathbf{b})(\mathbf{a} - \mathbf{b})^T\} = [g_{ij}]; \quad i, j = 1, 2, 3, 4 \quad (5)$$

then Eq. (3) can be more compactly expressed as

$$\begin{aligned}
 E\{(y - \hat{y})^2/x\} = & g_{11} + 2g_{12}x + [2g_{13} + g_{22}]x^2 \\
 & + 2[g_{23} + g_{14}]x^3 + [2g_{24} + g_{33}]x^4 \\
 & + 2g_{34}x^5 + g_{44}x^6 \quad (6)
 \end{aligned}$$

This sixth-order polynomial yields the desired mean-square error for a specific value of AGC voltage once we have determined the matrix $\mathbf{G}$.

2. Second-order curve fitting. For a given value of x the ideal power level is again given by Eq. (1). However, we now estimate this power level by

$$\hat{y} = b'_0 + b'_1x + b'_2x^2$$

The conditional mean-square error is then given by

$$\begin{aligned}
 E\{(y - \hat{y})^2/x\} = & E\{(a_0 - b'_0)^2\} + 2E\{(a_0 - b'_0)(a_1 - b'_1)\}x \\
 & + [2E\{(a_0 - b'_0)(a_2 - b'_2)\} + E\{(a_1 - b'_1)^2\}]x^2 \\
 & + 2[a_3E\{a_0 - b'_0\} + E\{(a_1 - b'_1)(a_2 - b'_2)\}]x^3 \\
 & + [2a_3E\{a_1 - b'_1\} + E\{(a_2 - b'_2)^2\}]x^4 \\
 & + 2a_3E\{a_2 - b'_2\}x^5 + a_3^2x^6 \quad (7)
 \end{aligned}$$

If we define the vectors

$$\mathbf{a}' = \begin{bmatrix} a_0 \\ a_1 \\ a_2 \end{bmatrix} \text{ and } \mathbf{b}' = \begin{bmatrix} b'_0 \\ b'_1 \\ b'_2 \end{bmatrix} \quad (8)$$

and consider the coefficient estimation error covariance matrix

$$\mathbf{H} = E\{(\mathbf{a}' - \mathbf{b}')(\mathbf{a}' - \mathbf{b}')^T\} = [h_{ij}]; \quad i, j = 1, 2, 3 \quad (9)$$

then the mean-square error polynomial becomes

$$\begin{aligned}
 E\{(y - \hat{y})^2/x\} = & h_{11} + 2h_{12}x + [2h_{13} + h_{22}]x^2 \\
 & + 2[a_0a_3 - a_3E\{b'_0\} + h_{23}]x^3 \\
 & + [2a_1a_3 - 2a_3E\{b'_1\} + h_{33}]x^4 \\
 & + 2a_3[a_2 - E\{b'_2\}]x^5 + a_3^2x^6 \quad (10)
 \end{aligned}$$

Note that this time we must not only compute the covariance matrix of the coefficient estimation error but also the mean of the estimated coefficients as well.

3. First-order curve fitting. Defining the power level estimate as $\hat{y} = b''_0 + b''_1x$ and repeating the above steps we have that

$$\begin{aligned}
 E\{(y - \hat{y})^2/x\} = & f_{11} + 2f_{12}x + [2a_0a_2 - 2a_2E\{b''_0\} + f_{22}]x^2 \\
 & + 2[a_0a_3 - a_3E\{b''_0\} + a_1a_2 - a_2E\{b''_1\}]x^3 \\
 & + [a_2^2 + 2a_1a_3 - 2a_3E\{b''_1\}]x^4 \\
 & + 2a_2a_3x^5 + a_3^2x^6 \quad (11)
 \end{aligned}$$

where f_{ij} , $i, j = 1, 2$ are the elements of the coefficient estimation error covariance matrix

$$\mathbf{F} = E\{(\mathbf{a}'' - \mathbf{b}'')(\mathbf{a}'' - \mathbf{b}'')^T\} = [f_{ij}] \quad (12)$$

and the vectors $\mathbf{a}''$ and $\mathbf{b}''$ are defined by

$$\mathbf{a}'' = \begin{bmatrix} a_0 \\ a_1 \end{bmatrix}, \quad \mathbf{b}'' = \begin{bmatrix} b''_0 \\ b''_1 \end{bmatrix} \quad (13)$$

C. Derivation of the Mean and Error Covariance of the Estimated Coefficients

To evaluate the statistical properties of the estimated coefficient vectors we must determine the effects of the calibration data errors on the curve fitting routines. Let us consider a set of established power levels y_i , $i = 1, 2, \dots, n$.

For each y_i there corresponds some ideal AGC voltage x'_i such that

$$y_i = a_0 + a_1 x'_i + a_2 (x'_i)^2 + a_3 (x'_i)^3$$

However, when y_i is established during the calibration phase, the computer (DIS or TCP) measures the AGC voltage $x_i = x'_i + \Delta_i$ where it is assumed that Δ_i is a zero mean gaussian random variable with $E(\Delta_i^2) = \sigma_i^2$. Furthermore, we assume $E\{\Delta_i \Delta_j\} = 0$ for $i \neq j$. In order to consider the calibration error problem as a parameter estimation problem we need to translate the error in the AGC voltage into an equivalent error in the carrier power level. Therefore, let us consider some ideal carrier power y_{0i} which corresponds to the measured value of AGC voltage; that is

$$y_{0i} = a_0 + a_1 x_i + a_2 x_i^2 + a_3 x_i^3$$

Substituting $x_i = x'_i + \Delta_i$

$$y_{0i} = y_i + [a_1 + 2a_2 x'_i + 3a_3 (x'_i)^2] \times \Delta_i + (a_2 + 3a_3 x'_i) \Delta_i^2 + a_3 \Delta_i^3$$

Substituting again for x'_i and solving for y_i yields

$$y_i = y_{0i} - (a_1 + 2a_2 x_i + 3a_3 x_i^2) \times \Delta_i + (a_2 + 3a_3 x_i) \Delta_i^2 - a_3 \Delta_i^3 \quad (14)$$

Thus, the power level supplied to the computer can be considered as consisting of an ideal power level y_{0i} plus an error term where both depend on the known (sampled) value of the AGC voltage.

When all of the data have been entered into the computer the curve fitting program first places the AGC voltage values in a matrix of the form (Ref. 3)

$$\mathbf{X} = \begin{bmatrix} 1 & x_1 & x_1^2 & \cdots & x_1^m \\ 1 & x_2 & x_2^2 & \cdots & x_2^m \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 1 & x_n & x_n^2 & \cdots & x_n^m \end{bmatrix} \quad (15)$$

where the number of rows equals the number of data pairs entered and the number of columns m is one larger than the degree of polynomial to be fitted. The program also arranges the signal power levels in a vector of the form

$$\mathbf{Y} = \begin{bmatrix} y_1 \\ y_2 \\ \vdots \\ y_n \end{bmatrix} \quad (16)$$

The coefficients of the fitted polynomial are then determined by the expression

$$\mathbf{b} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T \mathbf{Y} \quad (17)$$

where $\mathbf{b}$ is the estimated coefficient vector

$$\mathbf{b} = \begin{bmatrix} b_0 \\ b_1 \\ b_2 \\ \vdots \\ b_m \end{bmatrix}$$

and b_i are the fitted coefficients of x^i . We can now consider the statistics of $\mathbf{b}$ for the three curve fitting algorithms. For notational simplicity, it is assumed that the $\mathbf{X}$ matrix has been restricted to the proper dimension for the degree of polynomial to be estimated (i.e., the number of columns is one larger than the degree of the fitted curve).

1. Third-order curve fitting. For the third-order algorithm we only need to compute the covariance matrix of the coefficient estimation error $\mathbf{G}$. From Eqs. (14) and (16) we see immediately that the vector $\mathbf{Y}$ can be expressed as

$$\mathbf{Y} = \mathbf{Y}_0 - \boldsymbol{\alpha} \quad (18)$$

where

$$\mathbf{Y}_0 = \begin{bmatrix} y_{01} \\ y_{02} \\ \vdots \\ y_{0n} \end{bmatrix} \quad (19)$$

and the error vector $\boldsymbol{\alpha}$ is given by

$$\boldsymbol{\alpha} = \begin{bmatrix} (a_1 + 2a_2 x_1 + 3a_3 x_1^2) \Delta_1 - (a_2 + 3a_3 x_1) \Delta_1^2 + a_3 \Delta_1^3 \\ (a_1 + 2a_2 x_2 + 3a_3 x_2^2) \Delta_2 - (a_2 + 3a_3 x_2) \Delta_2^2 + a_3 \Delta_2^3 \\ \vdots \\ (a_1 + 2a_2 x_n + 3a_3 x_n^2) \Delta_n - (a_2 + 3a_3 x_n) \Delta_n^2 + a_3 \Delta_n^3 \end{bmatrix} \quad (20)$$

Now, if we use the definitions of $\mathbf{a}$ and $\mathbf{b}$ given in Eq. (4) and note that

$$\mathbf{Y}_0 = \mathbf{X} \mathbf{a} \quad (21)$$

then Eq. (17) becomes

$$\mathbf{b} = \mathbf{a} - (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T \boldsymbol{\alpha} \quad (22)$$

and the covariance matrix is given by

$$\mathbf{G} = E\{(\mathbf{a} - \mathbf{b})(\mathbf{a} - \mathbf{b})^T\} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T E\{\boldsymbol{\alpha} \boldsymbol{\alpha}^T\} \mathbf{X} (\mathbf{X}^T \mathbf{X})^{-1} \quad (23)$$

Now consider the components of the matrix $E\{\boldsymbol{\alpha} \boldsymbol{\alpha}^T\}$. From Eq. (20) if we let α_i be the i^{th} component of $\boldsymbol{\alpha}$ then we have for $i \neq j$

$$E\{\alpha_i \alpha_j\} = (a_2 + 3a_3 x_i)(a_2 + 3a_3 x_j) \sigma_i^2 \sigma_j^2 \quad (24)$$

and for $i = j$

$$\begin{aligned} E\{\alpha_i^2\} &= (a_1 + 2a_2 x_i + 3a_3 x_i^2) \sigma_i^2 \\ &+ 3[(a_2 + 3a_3 x_i)^2 + 2(a_1 + 2a_2 x_i + 3a_3 x_i^2)] (\sigma_i^2)^2 \\ &+ 15 a_3^2 (\sigma_i^2)^3 \end{aligned} \quad (25)$$

Or, by defining the matrix $\mathbf{C} = [C_{ij}]$; $i, j = 1, 2, \dots, n$ where

$$C_{ij} = E\{\alpha_i \alpha_j\}$$

then the final form of the covariance matrix is

$$\mathbf{G} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T \mathbf{C} \mathbf{X} (\mathbf{X}^T \mathbf{X})^{-1} \quad (26)$$

2. Second-order curve fitting. To evaluate the errors associated with the second-order algorithm we must compute the mean of the estimated coefficient vector as well as the error covariance matrix. We still have the relationship

$$\mathbf{Y} = \mathbf{Y}_0 - \boldsymbol{\alpha}$$

However, due to the decreased dimension of the $\mathbf{X}$ matrix, Eq. (21) is no longer valid. We can nevertheless use the definitions given in Eq. (8) and show that

$$\mathbf{Y} = \mathbf{X} \mathbf{a}' + a_3 \mathbf{x}^3 - \boldsymbol{\alpha} \quad (27)$$

where the vector $\mathbf{x}^3$ is given by

$$\mathbf{x}^3 = \begin{bmatrix} x_1^3 \\ x_2^3 \\ \vdots \\ x_n^3 \end{bmatrix} \quad (28)$$

Making this substitution Eq. (17) becomes

$$\mathbf{b}' = \mathbf{a}' + (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T (a_3 \mathbf{x}^3 - \boldsymbol{\alpha}) \quad (29)$$

From this equation we see that the expected value of $\mathbf{b}'$ is

$$E\{\mathbf{b}'\} = \mathbf{a}' + (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T (a_3 \mathbf{x}^3 - E\{\boldsymbol{\alpha}\}) \quad (30)$$

or by defining

$$\alpha'_i = a_3 x_i^3 + (a_2 + 3a_3 x_i) \sigma_i^2 \quad (31)$$

then

$$E\{b'_j\} = a_j + \sum_{k=1}^n U_{j+1, k} \alpha'_k, \quad j = 0, 1, 2 \quad (32)$$

where $U_{i,j}$ is the $(i,j)^{\text{th}}$ element of the matrix $(\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T$.

For the error covariance matrix we have from Eq. (9)

$$\begin{aligned} \mathbf{H} &= E\{(\mathbf{a}' - \mathbf{b}')(\mathbf{a}' - \mathbf{b}')^T\} \\ &= (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T E\{(a_3 \mathbf{x}^3 - \boldsymbol{\alpha})(a_3 \mathbf{x}^3 - \boldsymbol{\alpha})^T\} \mathbf{X} (\mathbf{X}^T \mathbf{X})^{-1} \end{aligned} \quad (33)$$

Considering the components of this expectation we have

$$\begin{aligned} E\{(a_3 x_i^3 - \alpha_i)(a_3 x_j^3 - \alpha_j)\} \\ = a_3^2 x_i^3 x_j^3 - a_3 x_j^3 E\{\alpha_i\} - a_3 x_i^3 E\{\alpha_j\} + E\{\alpha_i \alpha_j\} \end{aligned} \quad (34)$$

Using Eq. (24) we see that for $i \neq j$

$$\begin{aligned} E\{(a_3 x_i^3 - \alpha_i)(a_3 x_j^3 - \alpha_j)\} \\ = a_3^2 x_i^3 x_j^3 + a_3 x_i^3 (a_2 + 3a_3 x_j) \sigma_j^2 \\ + a_3 x_j^3 (a_2 + 3a_3 x_i) \sigma_i^2 \\ + (a_2 + 3a_3 x_i)(a_2 + 3a_3 x_j) \sigma_i^2 \sigma_j^2 \end{aligned} \quad (35)$$

and with the aid of Eq. (25) we have for $i = j$

$$\begin{aligned} E\{(a_3 x_i^3 - \alpha_i)^2\} \\ = a_3^2 x_i^6 + [2a_3 x_i^3 (a_2 + 3a_3 x_i) + (a_1 + 2a_2 x_i + 3a_3 x_i^2)] \sigma_i^2 \\ + 3[(a_2 + 3a_3 x_i)^2 + 2a_3 (a_1 + 2a_2 x_i + 3a_3 x_i^2)] (\sigma_i^2)^2 \\ + 15 a_3^2 (\sigma_i^2)^3 \end{aligned} \quad (36)$$

As in the previous case we will define a matrix

$$C' = [C'_{ij}]; \quad i, j = 1, 2, \dots, n$$

where

$$C'_{ij} = E\{(a_3 x_i^3 - \alpha_i)(a_3 x_j^3 - \alpha_j)\}$$

so that the error covariance matrix can be more compactly given by

$$H = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T C' \mathbf{X} (\mathbf{X}^T \mathbf{X})^{-1} \quad (37)$$

3. First-order curve fitting. The procedure for the first order algorithm is essentially the same as the second order case above. That is, we use the definitions of $\mathbf{a}''$ and $\mathbf{b}''$ in Eq. (13), recognize that

$$\mathbf{Y}_0 = \mathbf{X} \mathbf{a}'' + a_2 \mathbf{x}^2 + a_3 \mathbf{x}^3 - \boldsymbol{\alpha} \quad (38)$$

and use Eq. (17) to obtain

$$\mathbf{b}'' = \mathbf{a}'' + (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T (a_2 \mathbf{x}^2 + a_3 \mathbf{x}^3 - \boldsymbol{\alpha})$$

where

$$\mathbf{x}^2 = \begin{bmatrix} x_1^2 \\ x_2^2 \\ \vdots \\ x_n^2 \end{bmatrix} \quad (39)$$

The expected value of $\mathbf{b}''$ is

$$E\{\mathbf{b}''\} = \mathbf{a}'' + (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T (a_2 \mathbf{x}^2 + a_3 \mathbf{x}^3 - E\{\boldsymbol{\alpha}\}) \quad (40)$$

or in terms of its components

$$E\{b_j''\} = a_j + \sum_{k=1}^n U'_{j+1, k} a_k'' \quad (41)$$

where $U_{i, j}$ is the $(i, j)^{\text{th}}$ component of $(\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T$ and

$$a_k'' = a_2 x_k^2 + a_3 x_k^3 + (a_2 + 3a_3 x_k) \sigma_k^2 \quad (42)$$

Likewise, the covariance matrix F is given by

$$\begin{aligned} F = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T E\{(a_2 \mathbf{x}^2 + a_3 \mathbf{x}^3 - \boldsymbol{\alpha}) \\ \times (a_2 \mathbf{x}^2 + a_3 \mathbf{x}^3 - \boldsymbol{\alpha})^T\} \mathbf{X} (\mathbf{X}^T \mathbf{X})^{-1} \end{aligned} \quad (43)$$

where we have for $i \neq j$

$$\begin{aligned} E\{(a_2 x_i^2 + a_3 x_i^3 - \alpha_i)(a_2 x_j^2 + a_3 x_j^3 - \alpha_j)\} \\ = x_i^2 x_j^2 [a_2^2 + a_3^2 x_i x_j + a_2 a_3 (x_i + x_j)] \\ + (a_2 x_j^2 + a_3 x_j^3)(a_2 + 3a_3 x_i) \sigma_i^2 \\ + (a_2 x_i^2 + a_3 x_i^3)(a_2 + 3a_3 x_j) \sigma_j^2 \\ + (a_2 + 3a_3 x_i)(a_2 + 3a_3 x_j) \sigma_i^2 \sigma_j^2 \end{aligned} \quad (44)$$

and for $i = j$

$$\begin{aligned} E\{(a_2 x_i^2 + a_3 x_i^3 - \alpha_i)^2\} \\ = (a_2 + a_3 x_i)^2 x_i^4 \\ + [2x_i^2 (a_2 + a_3 x_i)(a_2 + 3a_3 x_i) + (a_1 + 2a_2 x_i + 3a_3 x_i^2)] \sigma_i^2 \\ + 3[(a_2 + 3a_3 x_i)^2 + 2a_3 (a_1 + 2a_2 x_i + 3a_3 x_i^2)] (\sigma_i^2)^2 \\ + 15 a_3^2 (\sigma_i^2)^3 \end{aligned} \quad (45)$$

Using a more compact notation

$$\mathbf{H} = (\mathbf{X}^T \mathbf{X})^{-1} \mathbf{X}^T C'' \mathbf{X} (\mathbf{X}^T \mathbf{X})^{-1} \quad (46)$$

where

$$C'' = [C''_{ij}]; \quad i, j = 1, 2, \dots, n$$

and

$$C''_{ij} = E\{(a_2 x_i^2 + a_3 x_i^3 - \alpha_i)(a_2 x_j^2 + a_3 x_j^3 - \alpha_j)\} \quad (47)$$

D. Calculations

A computer program was written to evaluate the coefficients of Eqs. (6), (10) and (11) using the appropriate covariance matrices (Eqs. 26, 37 and 46) and coefficient mean expressions (Eqs. 32 and 41). To determine the DIS computer calibration errors, calibration data sets for each of six Deep Space Stations were compiled. Each data set consisted of ten uniformly spaced values of AGC voltage covering the full dynamic range of the associated receiver as well as the variance for each value of voltage. For the

sake of definition the "full dynamic range" was defined as AGC voltages corresponding to signal power levels from -110 dBmW to 4 dB above threshold. The resulting sixth-order polynomials in x (AGC voltage) were then plotted for AGC voltages in the range from 0 to -8.0 V. Figure 1 shows these results where the number associated with each curve indicates the degree of the curve-fitting algorithm. Similar plots were obtained for each of the other data sets.

To better understand the behavior of the DIS calibration errors, the above quantities were recomputed using semi-full and restricted range calibration data sets. The semi-full range consisted of ten uniformly spaced values covering power levels from -110 dBmW to -160 dBmW. The restricted range data set consisted of ten uniformly spaced values covering the power range from -130 dBmW to -150 dBmW. The results are shown in Figs. 2 and 3.

The calibration accuracy expressions (Eqs. 10 and 11 only) were also evaluated for the TCP calibration method. To accomplish this, data sets of three AGC values covering an 8-dB signal power range and centered at -144 dBmW were formed. A typical result is shown in Fig. 4.

Figures 1 to 4 may be of interest in showing how the calibration errors behave but are of limited use in making quantitative comparisons of calibration techniques. What is needed is some kind of a figure of merit for each calibration technique. The most logical quantity is to consider the integral mean square error defined by

$$I = \frac{1}{x_u - x_v} \int_{x_v}^{x_u} E\{(y - \hat{y})^2/x\} dx \quad (48)$$

x_u and x_v are normally taken to be the extreme values of AGC voltage associated with the calibration data range. This quantity was computed for each of the six stations and each of the calibration techniques discussed above. Then an average over the six stations was taken to determine the figure of merit (actually figure of error) for each technique. A comparison of these quantities for the DIS computer is given in Table 1.

Comparison of these quantities for TCP and DIS computers might be somewhat misleading due to the large differences in calibration ranges. Consequently, Eq. (48) was reevaluated for the DIS using values of x_u and x_v which correspond to the calibration limits of the TCP. The results are given in Tables 2, 3 and 4.

We see from Table 1 that the present method of DIS calibration is quite inaccurate and in fact produces a calibration error standard deviation in excess of 0.3 dB. Comparing the DIS and TCP in Table 2 we find that the DIS has a calibration error more than two orders of magnitude larger than the TCP. Also from Tables 1 and 2 we see that the DIS error can be significantly reduced by using the third order algorithm in the DIS.

The DIS error can be further reduced by restricting its calibration range. From Table 3 it is evident that the DIS and TCP have equivalent calibration errors when the DIS uses the third order method and the semi-full calibration range. By further restriction of the DIS range we see from Table 4 that the DIS actually becomes more accurate.

III. Total Carrier Power Estimation Accuracy

The total estimation mean square error will be the sum of the calibration and the operational mean square errors. The operational errors include the effects of AGC variation (from receiver front end noise), operational AGC sampling and A/D converter quantization. Evaluation of the operational errors results in the curves shown in Fig. 5 (for the DIS) and Fig. 6 (for the TCP).

Also shown in Figs. 5 and 6 are certain calibration errors. In Fig. 5, we see that for the present method of calibration, the DIS estimation accuracy is completely dominated by the calibration accuracy and is much more inaccurate than the TCP method of carrier power estimation. Furthermore, the accuracy of the DIS can be significantly improved by using the techniques described above. For example, by using the semi-full calibration range and the third-order algorithm, the standard deviation of the DIS estimation error will drop from approximately 0.3 to about 0.01 dB, allowing the TCP and DIS to have approximately the same accuracies.

IV. Conclusion

In this article the expressions for the mean square calibration errors of the TCP and DIS computer algorithms used in carrier power estimation were presented and evaluated. When these results were combined with the associated operational errors, it was found that for the present calibration methods the TCP method of estimation is far more accurate than the DIS method. Also, it was noticed that the accuracy of the DIS method can be significantly improved by a slight alteration of the DIS calibration method.

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Table 1. DIS computer mean square calibration error

AGC Bandwidth	Degree of curve fit	Integral mean square calibration error, (dB) ²		
		Full calibration range	Semi-full calibration range	Restricted calibration range
Narrow	3	4.67×10^{-3}	1.78×10^{-4}	2.97×10^{-5}
	2	* 9.35×10^{-2}	5.51×10^{-2}	9.47×10^{-4}
Medium	3	2.24×10^{-2}	8.23×10^{-4}	1.38×10^{-4}
	2	* 1.11×10^{-1}	5.59×10^{-2}	1.05×10^{-3}
Wide	3	3.13×10^{-2}	1.04×10^{-3}	1.67×10^{-4}
	2	* 1.26×10^{-1}	5.60×10^{-2}	1.08×10^{-3}

* = present method of calibration.

Table 2. Comparison of DIS and TCP computer mean square calibration errors when the DIS is calibrated using the full data range

AGC bandwidth	DIS calibration error, (dB) ²		TCP calibration error, (dB) ²
	NFIT = 3	NFIT = 2	
Narrow	1.88×10^{-3}	* 6.40×10^{-2}	1.66×10^{-4}
Medium	4.58×10^{-3}	* 6.66×10^{-2}	1.63×10^{-4}
Wide	5.82×10^{-3}	* 6.75×10^{-2}	1.62×10^{-4}

* = present method of calibration.

Table 3. Comparison of DIS and TCP computer mean square calibration errors when the DIS is calibrated using the semi-full data range

AGC bandwidth	DIS calibration error, (dB) ²		TCP calibration error, (dB) ²
	NFIT = 3	NFIT = 2	
Narrow	5.31×10^{-5}	9.51×10^{-2}	1.66×10^{-4}
Medium	2.46×10^{-4}	9.73×10^{-2}	1.63×10^{-4}
Wide	3.08×10^{-4}	9.73×10^{-2}	1.62×10^{-4}

Table 4. Comparison of DIS and TCP computer mean square calibration errors when the DIS is calibrated using the restricted data range

AGC bandwidth	DIS calibration error, (dB) ²		TCP calibration error, (dB) ²
	NFIT = 3	NFIT = 2	
Narrow	9.16×10^{-6}	4.98×10^{-4}	1.66×10^{-4}
Medium	4.23×10^{-5}	5.24×10^{-4}	1.63×10^{-4}
Wide	5.28×10^{-5}	5.32×10^{-4}	1.62×10^{-4}

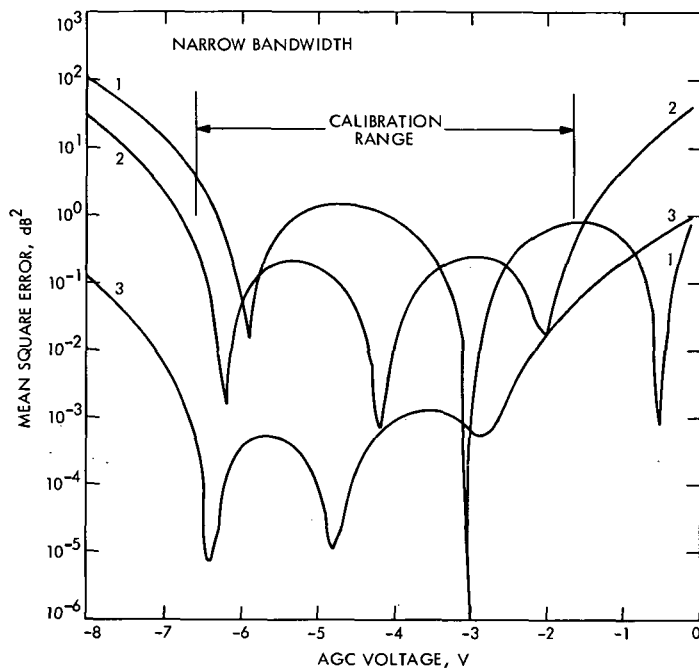


Fig. 1. DIS mean square calibration error when calibrated over full dynamic range for: (1) first-order, (2) second-order, and (3) third-order curve fitting

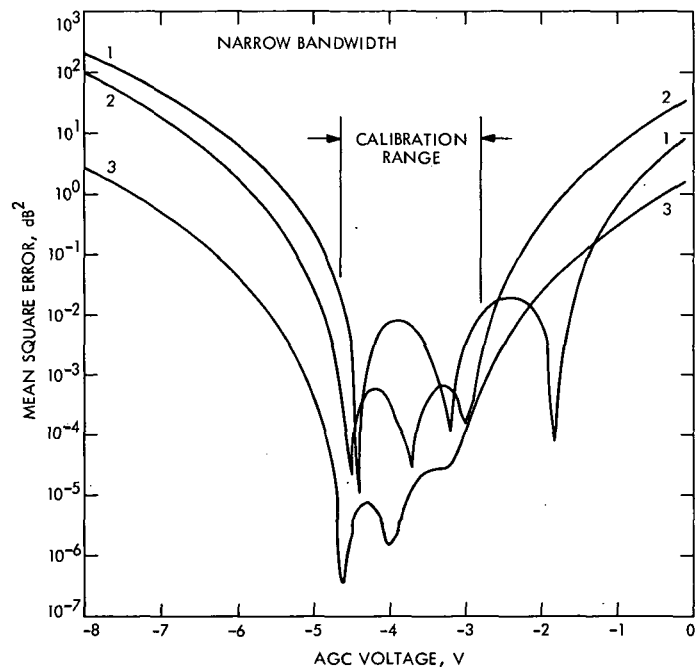


Fig. 3. DIS mean square calibration error when calibrated over restricted range for: (1) first-order, (2) second-order and (3) third-order curve fitting

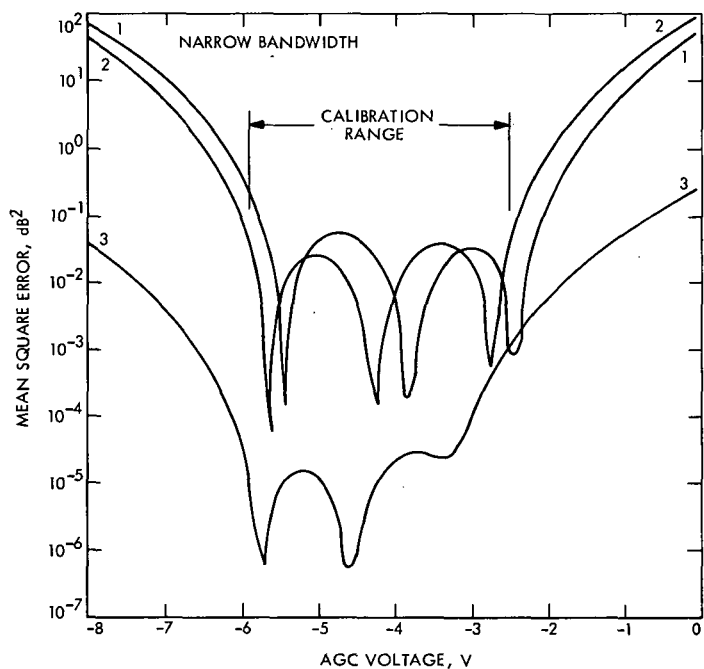


Fig. 2. DIS mean square calibration error when calibrated over semi-full dynamic range for: (1) first-order, (2) second-order, and (3) third-order curve fitting

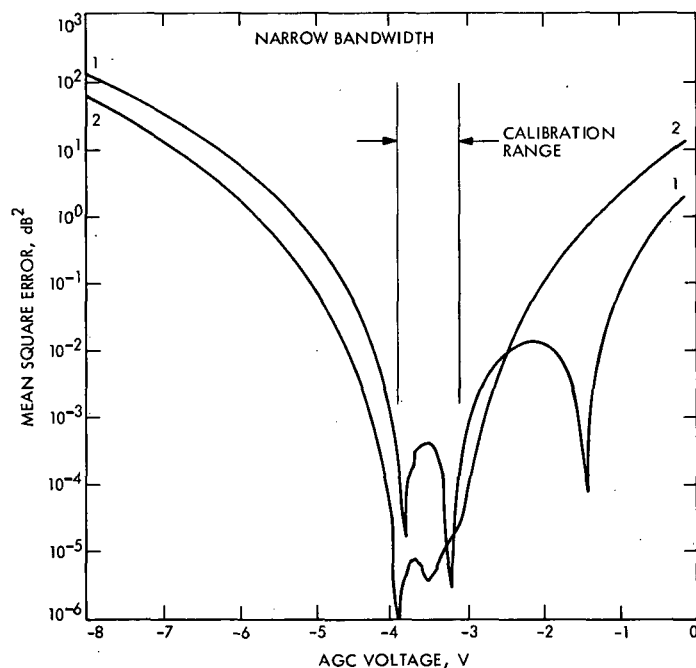


Fig. 4. TCP mean square calibration error for: (1) first-order, and (2) second-order curve fitting

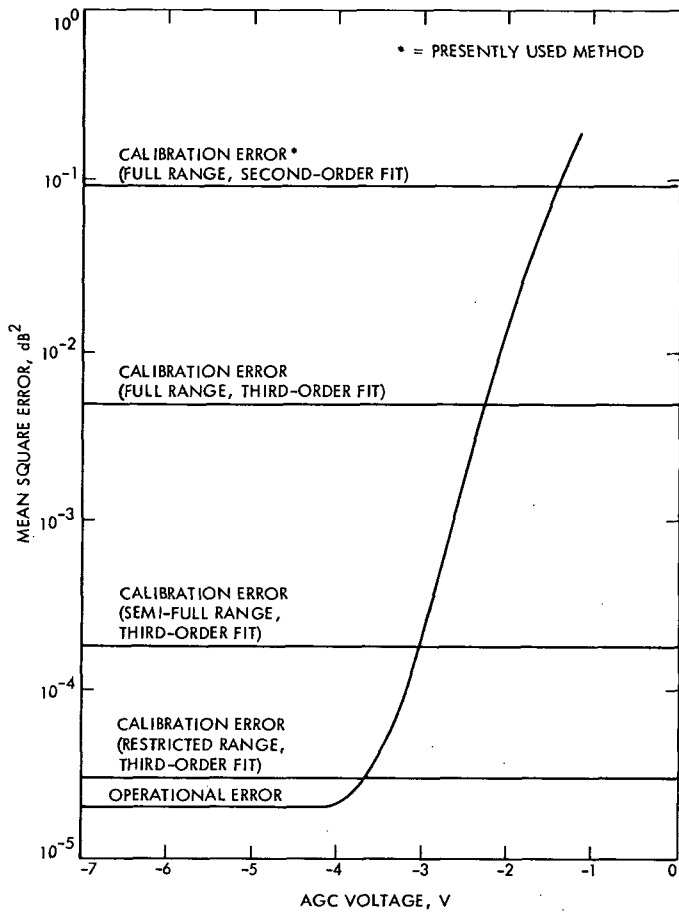


Fig. 5. Comparison of the DIS calibration and operational errors

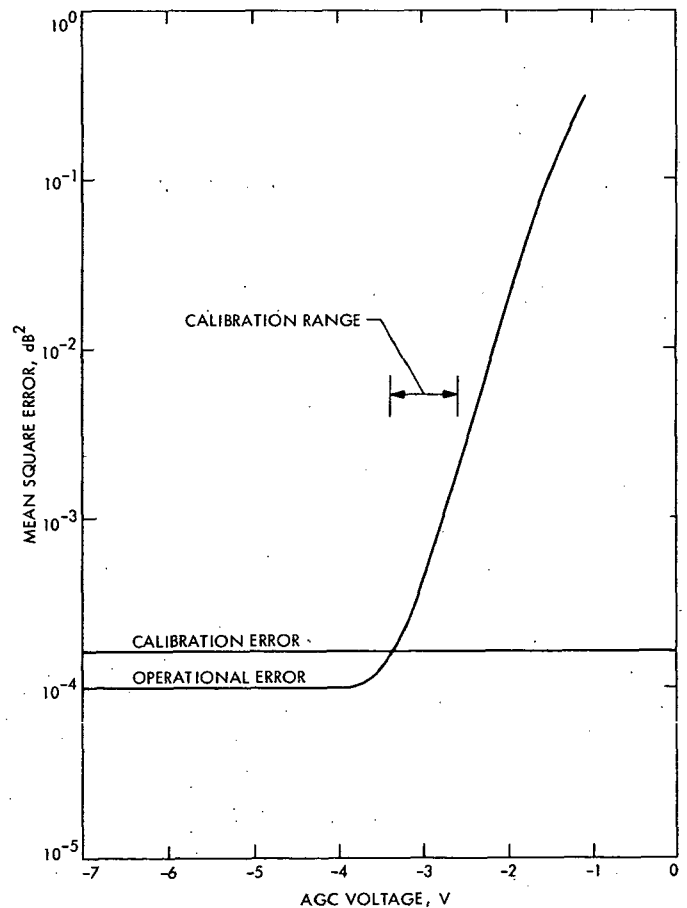


Fig. 6. Comparison of the TCP calibration and operational errors

Overseas 64-m-Diameter Antenna Power Configuration

J. Dorman

DSIF Engineering Section

The construction of the two new 64-m-diameter antennas located at DSS 63 (Madrid) and DSS 43 (Tidbinbilla) required additional power generating equipment at these sites. As the new sites were in close proximity to the existing DSS 61 (Madrid) and DSS 42 (Tidbinbilla), the new equipment was designed to integrate with the existing power generating and distribution systems. This integration will enable the new and existing generators to be combined into a single generating system and provide total site power for both 64-m and 26-m antenna station requirements. Studies are being made to determine the economic and technical advantages of using commercial power. If proved favorable, the equipment presently being installed is designed to provide parallel operation of the generating system with commercially produced power.

The new equipment is equipped with automatic generator starting and stopping features and power demand sensing monitors. The monitors automatically start, synchronize, and connect generators to share load demand equally between running generators as power demand increases. Conversely, if the demand decreases, unnecessary generators are removed from the generating system. This article describes the techniques developed and incorporated in the design of the new generation and distribution equipment and the proposed future development of the power generating systems.

I. Introduction

This progress report describes the engineering development of the power generation and distribution systems for the 64-m-diameter antennas. Interconnection with existing 26-m-diameter antenna power generation and distribution systems and future commercial power source is also described.

II. Existing Power Generation and Distribution Systems at DSS 61 (Madrid) and DSS 42 (Canberra)

At both of the existing sites, power is derived from diesel engine-driven generators which deliver 480 volts, three phase, 60 hertz. Equipment requiring other voltages or frequencies is supplied through transformers or fre-

quency converters which are powered from the 480-volt 60-hertz main power system. Figure 1 is a simplified single line diagram of the system. Figure 2 gives a picture of a typical engine-generator line-up.

The generating equipment is controlled manually by operating personnel on a three-shift work schedule. Starting, stopping, synchronizing, and load control of diesel engine-driven generators for required power loads are under the control of these personnel.

The generating capacity of the system is adequate for the power demands imposed, which are relatively small. Sudden loads imposed by equipment such as air conditioners and relatively large motors could cause transient voltage and frequency fluctuations outside acceptable limits for other electronic equipment. This problem has been solved by providing switching devices which allow electrical separation of the system into two independent power subsystems which are entitled "U" bus for utility loads and "E" bus for more sensitive electronic loads. Completely separate operation of these subsystems prevents fluctuations of "E" bus voltage or frequency due to load changes on the "U" bus.

Although the "U" loads can tolerate momentary voltage and frequency fluctuations to a greater degree than electronic loads, large motors connected to the "U" power distribution subsystem are equipped with reduced voltage starters to prevent sudden application of large power demands.

Some limited testing at DSS 14, with an adequate number of generators connected to interconnected "E" and "U" bus power distribution subsystems, indicates that present day electronic equipment may tolerate fluctuations presently experienced by the "U" bus system. Further research is being conducted to establish the adequacy of a single bus power system. The advantages of a single bus power generation and distribution system in terms of simplicity of design and operation with accompanying equipment cost savings are very desirable but need careful evaluation to ensure that the operation of electronic equipment is not endangered.

III. Requirement for New Generation and Distribution Systems for 64-m Antennas at DSS 63 (Madrid) and DSS 43 (Tidbinbilla)

The new 64-m antennas at both sites require an initial generating capacity of 3000 kilowatts. This power requirement led to an economic choice of a higher generated

voltage level of 2400 volts rather than the 480-volt level presently used by existing 26-m antenna power systems, and the use of four generators each rated at 750 kilowatts for each site. Future increase in power requirements will be met by adding similarly rated generators. Figure 3 is a single line diagram for a 64-m antenna power system.

A study was made to establish the best performance capability available from proven, commercially available, diesel-driven generating equipment and compared with up-to-date performance requirements established by the National Communication System as shown in Fig. 4.

The required performance for normal operation of the system with steady, continuous load could easily be met by commercially produced equipment. The transient voltage and frequency fluctuations allowable during application or removal of sudden loads required more careful study. The maximum value of sudden load application or removal was established at 75% of connected generator capacity as discussed in *Section V* of this article. Turbo-charged diesel engines rely on exhaust gas volume to drive the turbo-charger and thereby supplement naturally aspirated air to the diesel engine. Sudden application of load momentarily slows the engine and turbo-charger, which stifles air supply at the precise moment the engine requires it to recover normal speed.

To maintain the required frequency performance, a supplementary combustion air system was fitted to each engine. This consists of a simple compressed air storage tank connected to the engine air inlet manifold through an electrically controlled valve. The valve opens only when a sudden load application occurs, and the resulting improvement in diesel engine recovery is well within performance requirements as indicated in Fig. 4.

As mentioned in *Section II* of this article, the need for separate "E" and "U" systems at the 26-m antenna sites is doubtful and is being studied. The greater generating capacity and superior performance of the generators equipped with supplementary air systems at the 64-m antenna sites led to the design of a single operational "O" system.

The design includes a second bus for the testing of generators designated "T." The "T" bus will allow generator testing without interference with normal operation of the power system, will allow for personnel training and may be used for future power to the high power transmitter. If, for some presently unforeseen reason, the single opera-

tional bus system proves to be unsatisfactory, the system can be easily converted to the conventional "E" and "U" two-bus system.

Recently available control components using solid-state components have been used to improve the performance and relieve the sometimes tedious manual control of generator equipment at the 26-m antenna stations. Improved voltage regulators with automatic kilovar equalizing controls and automatic electronic governor controls with kilowatt load equalizing features are in this category and have proven their usefulness and reliability at these stations. A new automatic synchronizer with double-check features and an automatic generator start-stop device based on demand load have been produced commercially. These devices have been used in the generator control system to provide fully automated control of the new 64-m antenna generating systems. After initial settings have been made, the control operations usually performed by shift personnel will be automatically performed by the control devices. During initial operation, to allow familiarization by personnel and as an insurance against malfunction, the equipment can be switched to completely conventional manual control.

IV. Integration of New and Existing Power Generation and Distribution Systems

The intention is to operate the existing 26-m and 64-m antenna power generation and distribution systems as a single integrated power system. This will not preclude the operation of the systems individually or the preselection of either automatic or manual control mode. Mode control is by simple control switch operations.

The integration of the two antenna power systems will be in two phases. The first phase of the integration will be accomplished on completion of the initial installation of the 64-m antenna equipment. Interconnection of the power systems will be through power switching circuit breakers when desired. The integrated power system diagram is shown in Fig. 5. Synchronizing equipment provided allows connecting generators to generator bus systems but is not provided across tie circuit breakers during this phase of the systems integration. This means that shut down of one of the systems is necessary to make the tie between the power systems.

During the first phase of integrated operation of the two power systems, the 26-m antenna power generators remain under control of operating personnel. The 64-m antenna power generators are "slaved" to the 26-m an-

tenna power generation system and will share that portion of load on the total system not being provided by the 26-m antenna generating system. Voltage and frequency control of the integrated power system will be completely manual by operating personnel at the 26-m antenna power generation control console.

Phase 2 of the power systems integration will be implemented in the near future. It will provide for interconnecting the 64-m and 26-m antenna power system with both systems energized, without momentary shut down of either system. This will be accomplished by provision of synchronizing equipment across the interconnecting tie circuit breaker.

Another feature planned under this phase of the power systems integration is the addition of equipment to allow automatic start-stop control, automatic load sharing, and kilovar sharing to the existing 26-m antenna power generators. This will completely integrate the 26-m/64-m antenna power system with fully automatic control capabilities.

V. Integration of Commercial Power With the Generator Power Systems

The capital expenditure, amortization period, cost per kilowatt hour, and costs for maximum power demand for commercial power are presently being compared with fuel savings, maintenance and repair cost savings for reduced operating time and operating personnel costs associated with the generating plant operation. Comparison will determine the possible economic advantages of purchasing commercial power at the sites.

If the results of this study indicate that commercial power should be used, there will be the operational advantages of using this power source as an alternative backup in case of critical failure of the generating system.

The equipment presently provided will accommodate an incoming commercial power source, and control devices included will permit operation of the 64-m antenna generators in parallel with the commercial power source.

In this mode of operation, simple controls will allow a preset percentage of the total system kilowatt load to be assumed by the connected generators and the major portion of the system kilowatts to be derived from the commercial power source. Other controls allow setting of kilovars drawn from the commercial power source. Normal setting of this control will be to minimize kilovars

from the commercial source, so that generators will supply most of the kilovar load demand. It will be noted that kilowatt and kilovar loads drawn from the commercial source and the generators source are functionally opposite, the least expensive kilowatts being derived from the commercial and the least expensive kilovars being derived from the generators. Kilovar loading of generators has negligible effect on diesel engine fuel consumption.

For critical mission operation the most reliable operation of the power system will be with a sufficient number of generators connected to satisfy the total load of the system and the commercial power source connected in parallel with the generators. This mode of operation will provide 100% power source capability in excess of re-

quirements. The load kilowatts derived from the engine-generators will be the minimum consistent with stable governor and clean engine performance, nominally 25% of generator rating. Total kilovar load of the power system will be shared equally by the generators.

The commercial source will provide 75% of the power system kilowatt loading and none of the system kilovars. Worst case voltage and frequency fluctuations would occur in case of loss of the utility power source. There would be no increase in generator kilovar loading but kilowatt loading on the generator would rise from 25 to 100%. As indicated in Fig. 4, the engine-generators will maintain voltage and frequency well within specified requirement under these conditions.

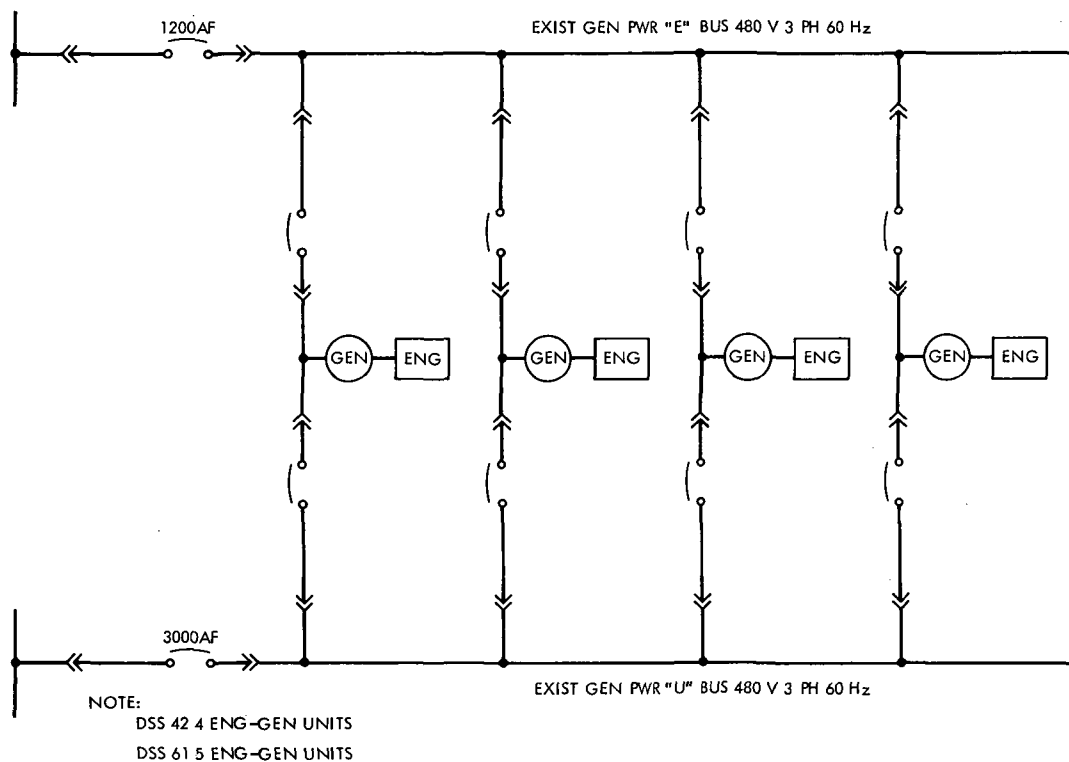
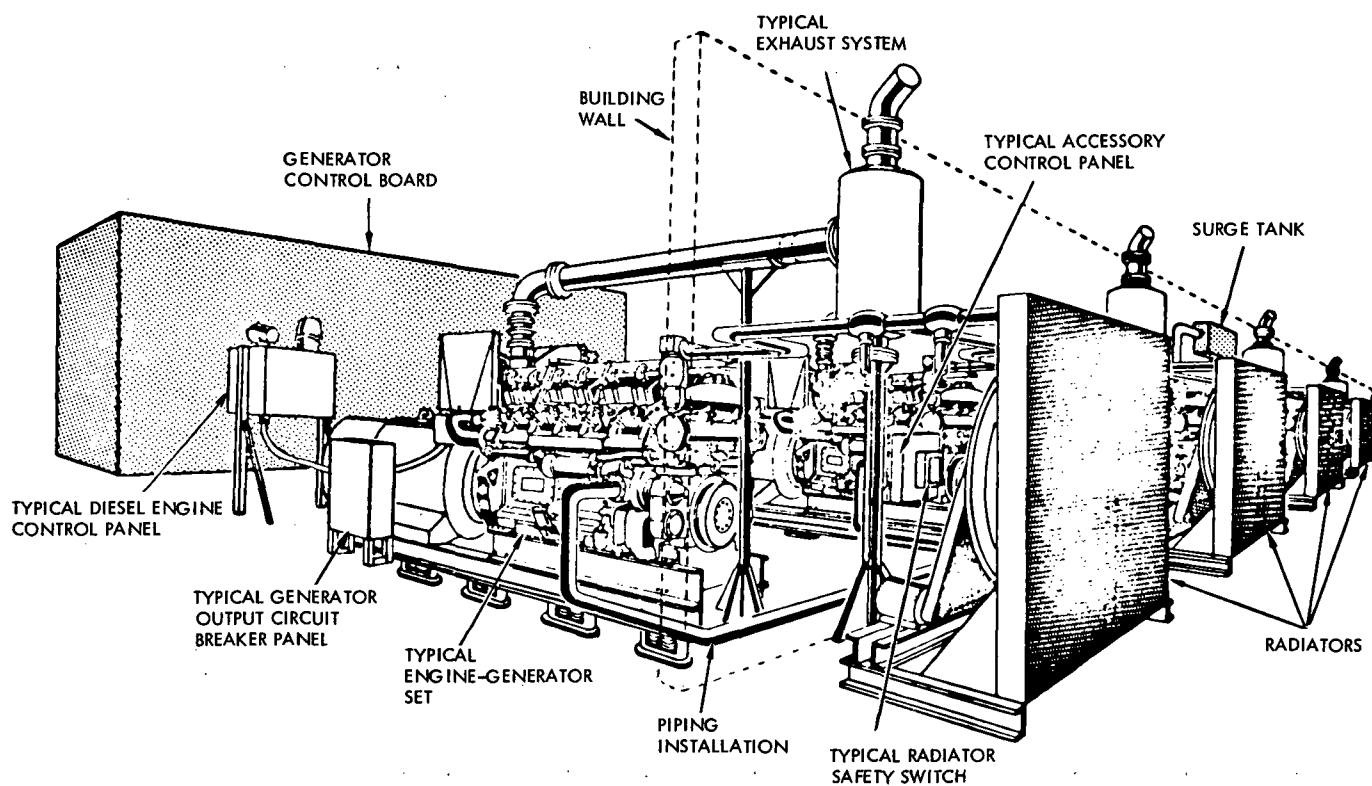


Fig. 1. Single line diagram of 26-m antenna power generation and distribution system



NOTE: FOUR-GENERATOR SET SYSTEM SHOWN

Fig. 2. Typical 26-m antenna engine-generator line-up

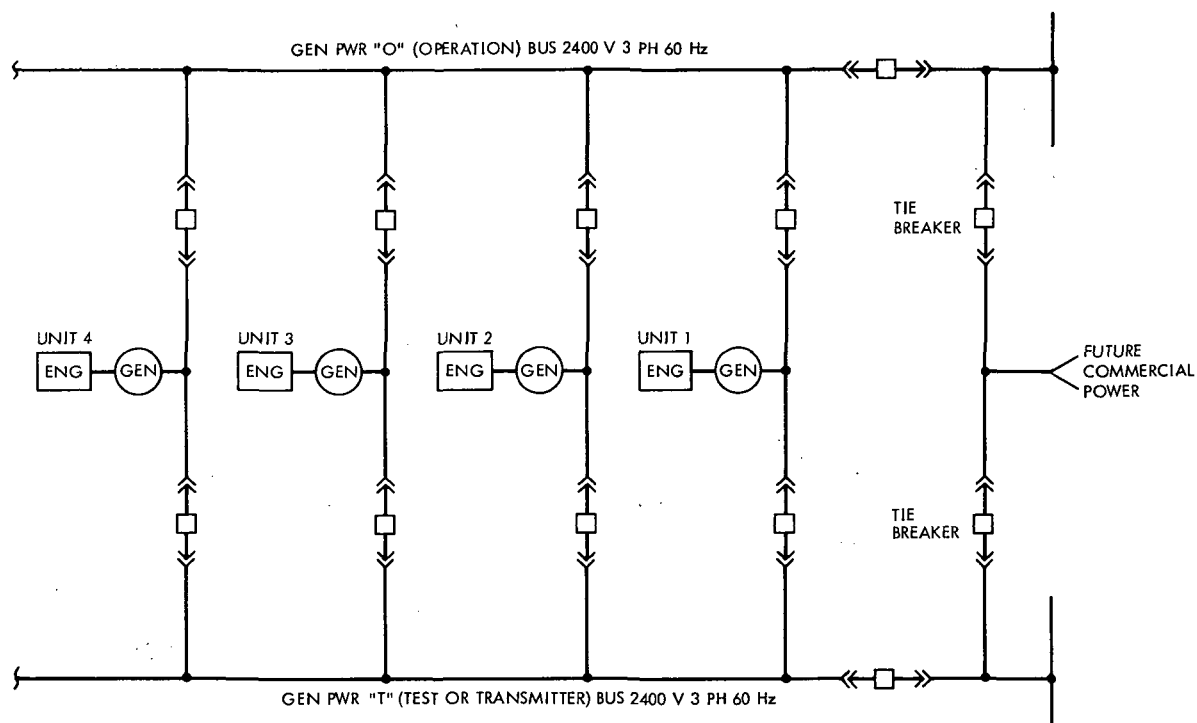
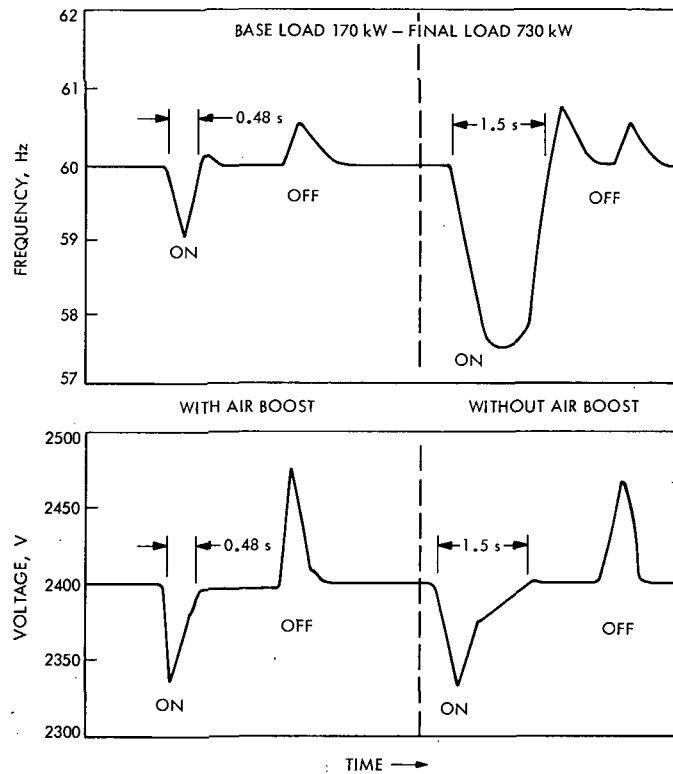
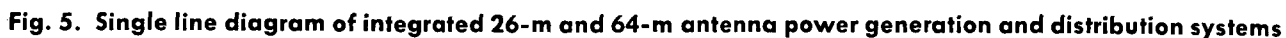


Fig. 3. Single line diagram of 64-m antenna power generation and distribution system



NATIONAL COMMUNICATION SYSTEM REQUIREMENTS:
 STEADY-STATE LIMITS - 2280 TO 2520 V, 59.7 TO 60.3 Hz
 TRANSIENT LIMITS - 1920 TO 2640 V, 58.02 TO 61.98 Hz
 RECOVERY WITHIN 0.5 s

Fig. 4. Voltage and frequency deviations of power systems



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