myer - George Huff - X 5097

CONTRACT NAS 9-10441
~~FINAL REPORT~~

Tech Mon - Ken Land.
5566 EE8

DATA COMPRESSION/ ERROR CORRECTION DIGITAL TEST SYSTEM

APPENDIX 1

OPERATION

Details of Illustrations in this document may be better studied on microfiche

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JANUARY 1972

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APPENDIX 1

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APPENDIX 1

OPERATION

A1-1.0 INTRODUCTION

This section provides DC/EC operating instructions for anticipated operating conditions. The instructions are supported by illustrations and tables for the controls and indication of Radiation-built equipment. For functions of controls and indicators of vendor equipment, refer to the applicable vendor's manual. A thorough knowledge of all DC/EC controls and indication is required before attempting equipment operation.

A1-2.0 CONTROLS AND INDICATORS

A1-2.1 Transmitter Control Panel - A3A4

The Transmitter Control Panel provides a functional representation of the system configuration. Where feasible, inputs and outputs of functional units are brought to jacks on the panel for interconnection and monitoring, and to allow independent use of subsystems of the Transmitter. The jacks on the panel are keyed in Figure A1-2.1-1 and are described in Table A1-2.1-1. The controls are keyed in Figure A1-2.1-2 and are described in Table A1-2.1-2.

Table A1-2.1-1. Transmitter Control Panel Jacks

Index No.	Control or Indicator	Ref Des	Function
1	EXT	P1	External data input to Channel Coder
2	TV IN	P2	Composite video input
3	MUX DATA	P3	Multiplexer data output
4	DATA	P4	Channel coder data output A
5	DATA	P5	Channel coder data output B
6	TOL MON	P6	Analog output proportional to tolerance site
7	BUFFER USAGE	P7	Analog output proportional to Buffer Memory fullness
8	PCM INPUT	P8	PCM Data input to multiplexer
9	DATA	P9	Data input to output buffer amplifier

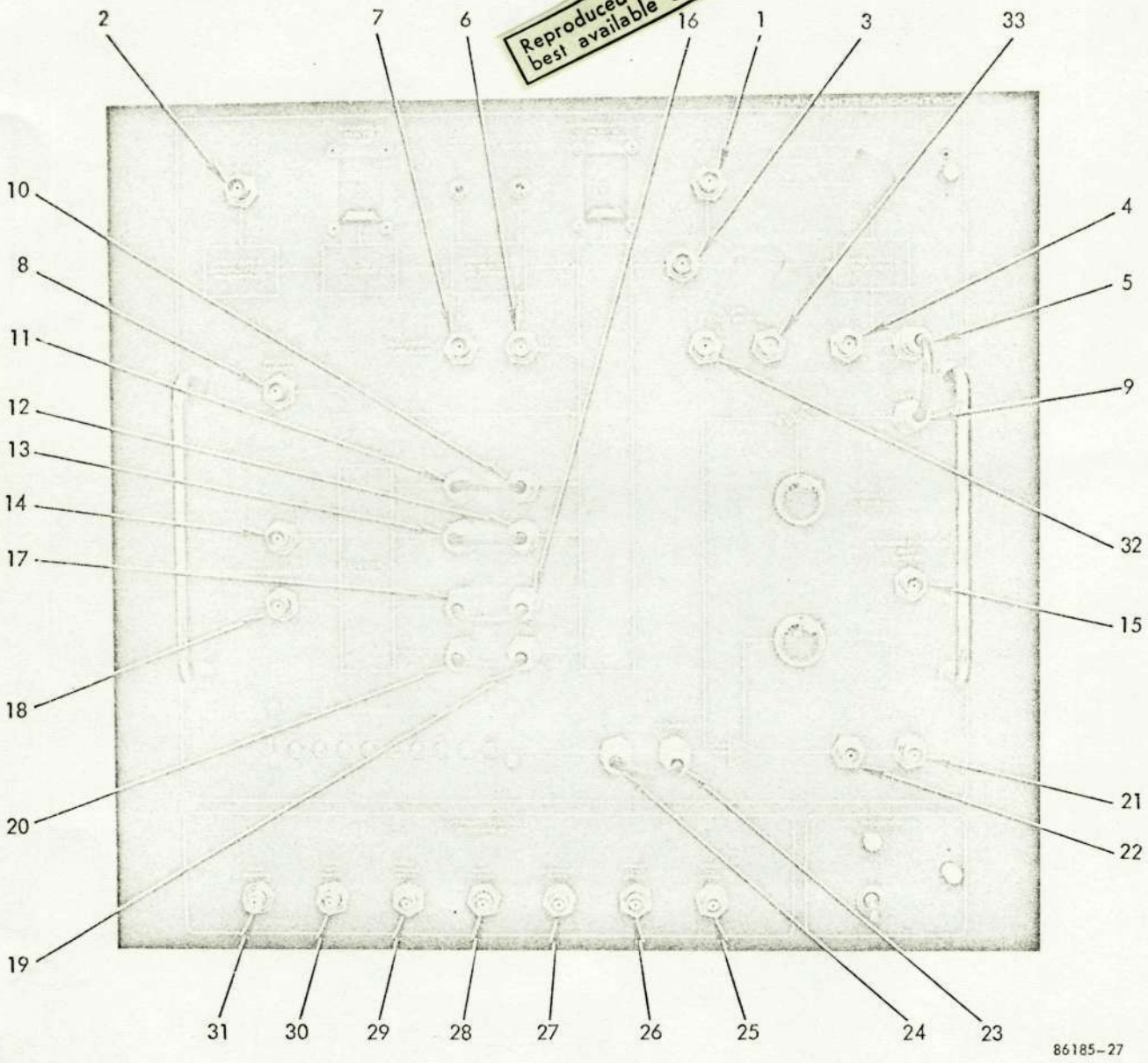

Figure A1-2.1-1. Transmitter Control Panel A3A4 Connectors

Table A1-2.1-1. Transmitter Control Panel Jacks (Continued)

Index No.	Control or Indicator	Ref Des	Function
10	DATA	P10	Audio Channel 1 data input to multiplexer
11	DATA	P11	Audio Channel 1 data output from delta mod
12	CLOCK	P12	Audio Channel 1 clock input to multiplexer
13	CLOCK	P13	Audio Channel 2 clock output from delta mod
14	VOICE CHANNEL 1	P14	Voice Channel 1 input to delta mod
15	BANDSPREAD BIT RATE	P15	Coded Bit Rate clock output
16	DATA	P16	Audio Channel 2 data input to multiplexer
17	DATA	P17	Audio Channel 2 data output from delta mod
18	VOICE CHANNEL 2	P18	Voice Channel 2 input to delta mod
19	CLOCK	P19	Audio Channel 2 clock input to multiplexer
20	CLOCK	P20	Audio Channel 2 clock output from delta mod
21	DATA	P21	Output of output buffer amplifier
22	DATA	P22	Output of output buffer amplifier
23	NOISE	P23	Noise input to output buffer
24	NOISE	P24	Noise output of attenuator
25	COMP SYNC	P25	Output Composite Sync to Camera
26	VERT STN	P26	TV Vert Sync Test Point

Table A1-2.1-1. Transmitter Control Panel Jacks (Continued)

Index No.	Control or Indicator	Ref Des	Function
27	AD SAMPLE RATE	P27	Sample Rate clock output
28	Δ MOD CLOCK	P28	A mod clock output
29	MUX FRAME RATE	P29	Multiplexer frame rate clock output
30	INFO BIT RATE	P30	Information rate clock output
31	PCM CLOCK	P31	PCM clock output
32	QP OUTPUT	P32	Channel I of QP output
33	QP OUTPUT	P33	Channel Q of OP Output

Table A1-2.1-2. Transmitter Control Panel Controls

Index No.	Control or Indicator	Ref Des	Function
1	(Rotary Switch)	S1	Selects mode of channel coder: Fano (R = 1/2); Viterbi (R = 1/2; Viterbi (R= 1/3)
2	INFORMATION RATE (Thumbwheel Switch)	S2	Selects 1-9 Mb/s information rate clock
3	MODE (Toggle Switch)	S3	Selects mode of data reducer: ZOP, ZOI, or STATISTICAL
4	DATA BITS (Toggle Switch)	S4	Selects number of data bits (4,5,6) in a 10-bit TV word for the ZOP and ZOI modes
5	SAMPLE RATE (Thumbwheel Switch)	S5	Selects 1 - 9 MHz. Sample Rate clock.
6	(Rotary Switch)	S6	Selects data input to channel coder
7	(Rotary Switch)	S7	Selects PCM data input to multiplexer: EXT, all 0's, all 1's
8	ON (Toggle Switch)	S8	Power ON/OFF Switch

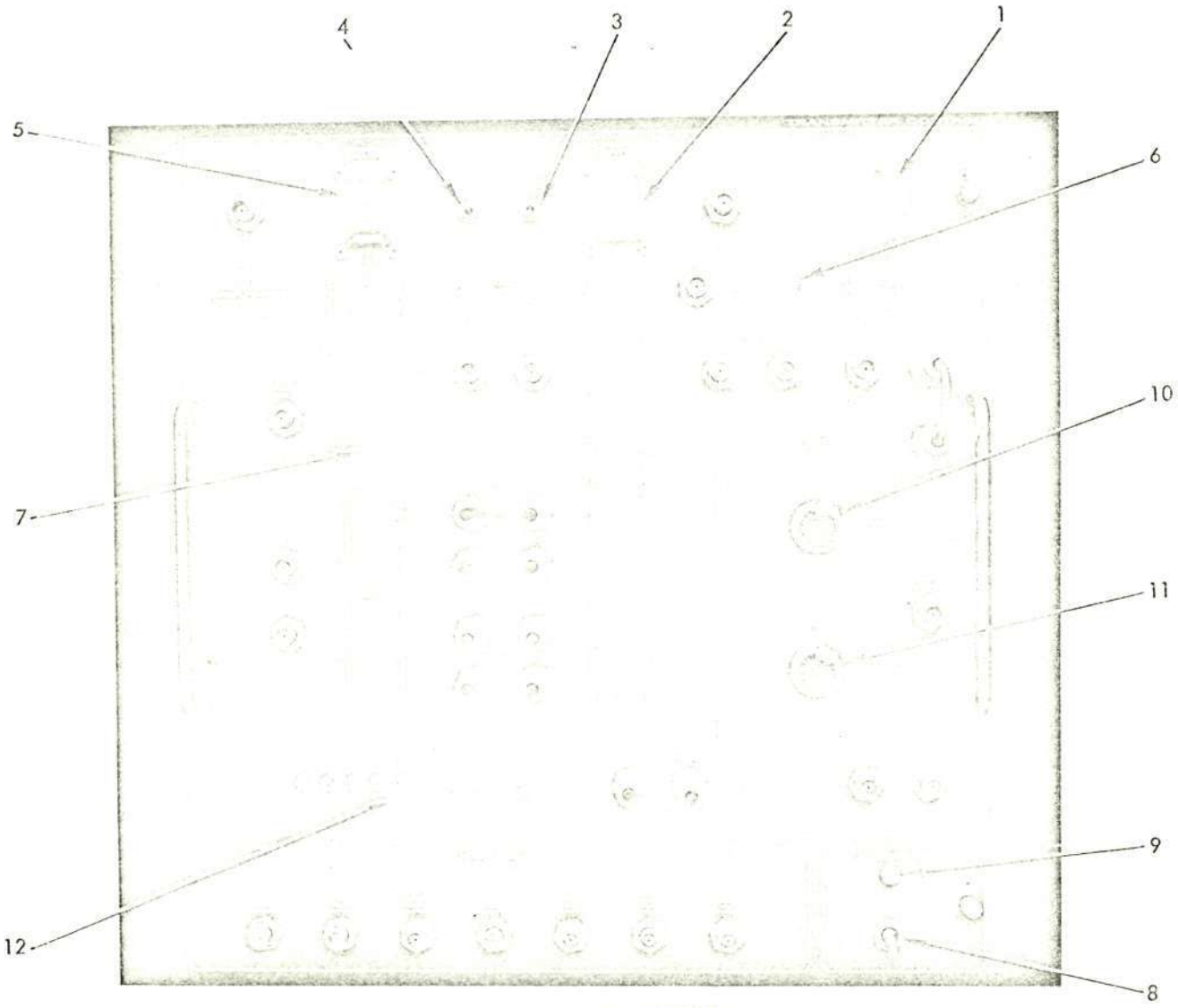

Figure A1-2.1-2. Transmitter Control Panel Controls

Table A1-2.1-2. Transmitter Control Panel Controls (Continued)

Index No.	Control or Indicator	Ref Des	Function
9	AC POWER (Indicator)	DS1	Power ON/OFF Indicator
10	SIGNAL LEVEL (Variable Resistor)	R1	Adjusts the gain of output buffer
11	OFFSET (Variable Resistor)	R2	Adjusts the offset of output buffer
12	NOISE ATTENUATION (Attenuation)	AT1	Attenuates the level of the noise generator

A1-2.2 Transmitter Reducer Switch Panel - A3A2A4

The transmitter Reducer Switch Panel provides control signals for the Transmitter reducer, buffer rate control, and buffer control functions. Figure A1-2.2 depicts the controls. Table A1-2.2 lists the controls and defines their functions.

Table A1-2.2. Transmitter Reducer Switch Panel

Control	Ref Des	Function
TOLERANCE	S1-S4	In fixed tolerance mode, selects tolerance. In adaptive tolerance mode, selects minimum tolerance.
NRS COUNTER BIAS	S6-S10	Selects count to which NRS counter is preset. (Represents desired number of nonredundant samples per 32 input samples) Determined by $NRS = \frac{4.15\ IR - .25}{SR}$
PLUS: MULT/DIV (S-11) 1/2/4 (S-12)		Selects multiplication factor of 4, 2, 1, 1/2 or 1/4 to operate on a positive sample of the NRS Counter in calculating tolerance

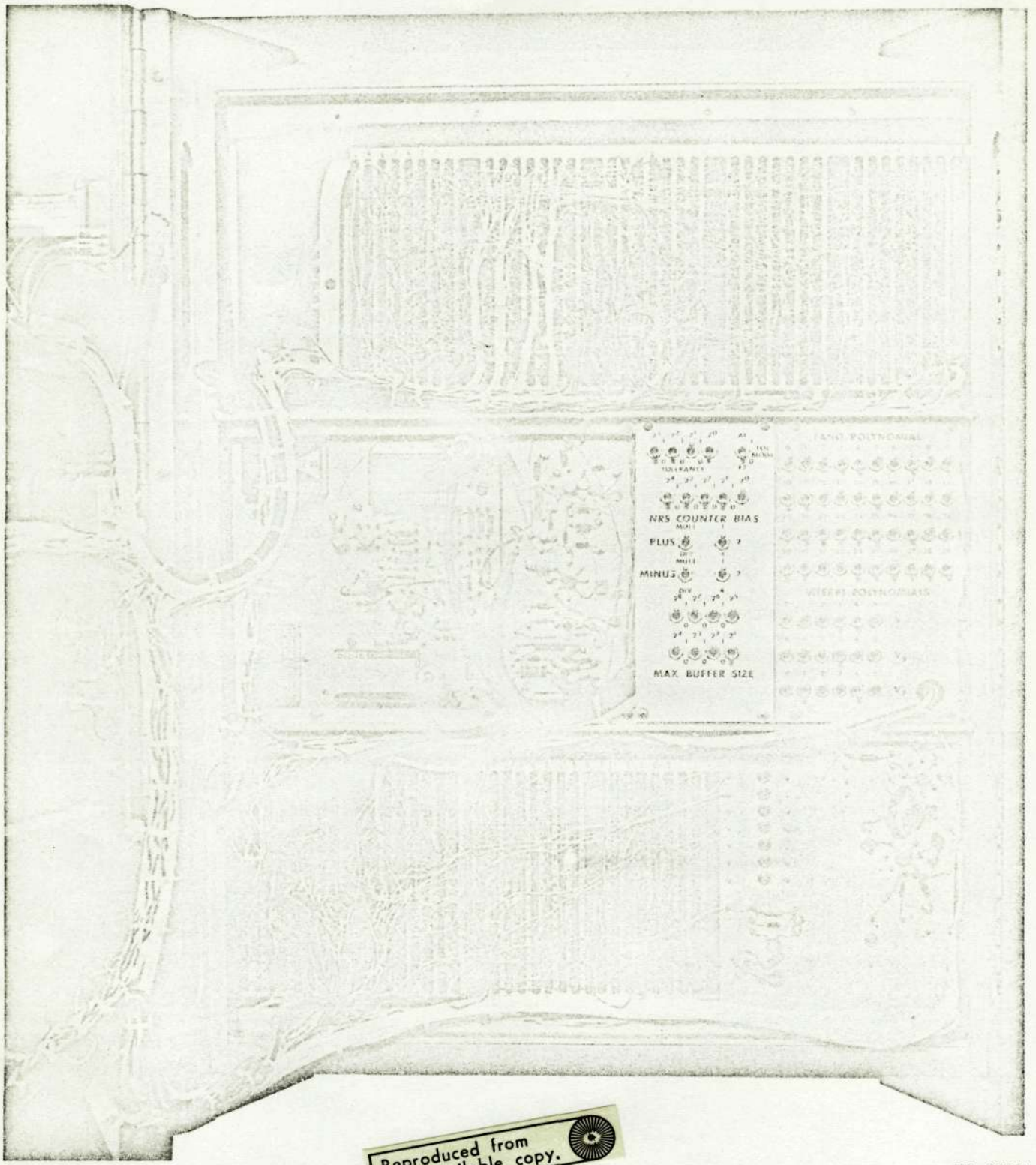

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Figure A1-2.2. Transmitter Reducer - Switch Panel

Table A1-2.2. Transmitter Reducer Switch Panel (Continued)

Control	Ref Des	Function
MINUS: MULT/DIV (S 13) 1/2/4 (S 14)		Selects multiplication factor of 4, 2, 1, 1/2 or 1/4 to operate on a negative sample of the NRS counter in calculating tolerance
MAX BUFFER SIZE	S 15-S22	Selects maximum effective size of transmitter Rate Buffer in adaptive tolerance mode
TOL MODE	S5	Selects Fixed Tolerance or Adaptive Tolerance Mode

A1-2.3 Transmitter Convolutional Coder Switch Panel A3A2A5

The transmitter convolutional switch panel provides the programming for the Fano Polynominal and Viterbi Polynomials. Figure A 1-2.3 depicts the controls.

The Fano Polynomial switches (0 -39) select stages from a 40-bit shift register for modulo-two addition to generate the parity bits when the transmitter is in the Fano (R = 1/2) mode. The switch settings correspond to the coefficients of the generator polynomial for the desired codes.

The Viterbi Polynomial switches (V_1: 0 - 5; V_2: 0 - 5; select stages of a 6-bit shift register for modulo-two addition to generate the coder output in the Viterbi (R = 1/2) mode. The third bank (V_3: 0 - 5) performs the same function in the Viterbi (R = 1/3) mode. The switch settings correspond to the coefficients of the generator polynomials for the desired codes.

A1-2.4 Delta Modulator A3A3A4

The Delta Modulator assembly contains four switches. There are two switches for each of the modulator channels. These switches are used to select the input impedance (600 or 50 ohms) and to select amplitude compression or not. The switches are keyes in Figure A1-2.4 and the functions are called out in Table A1-2.4.

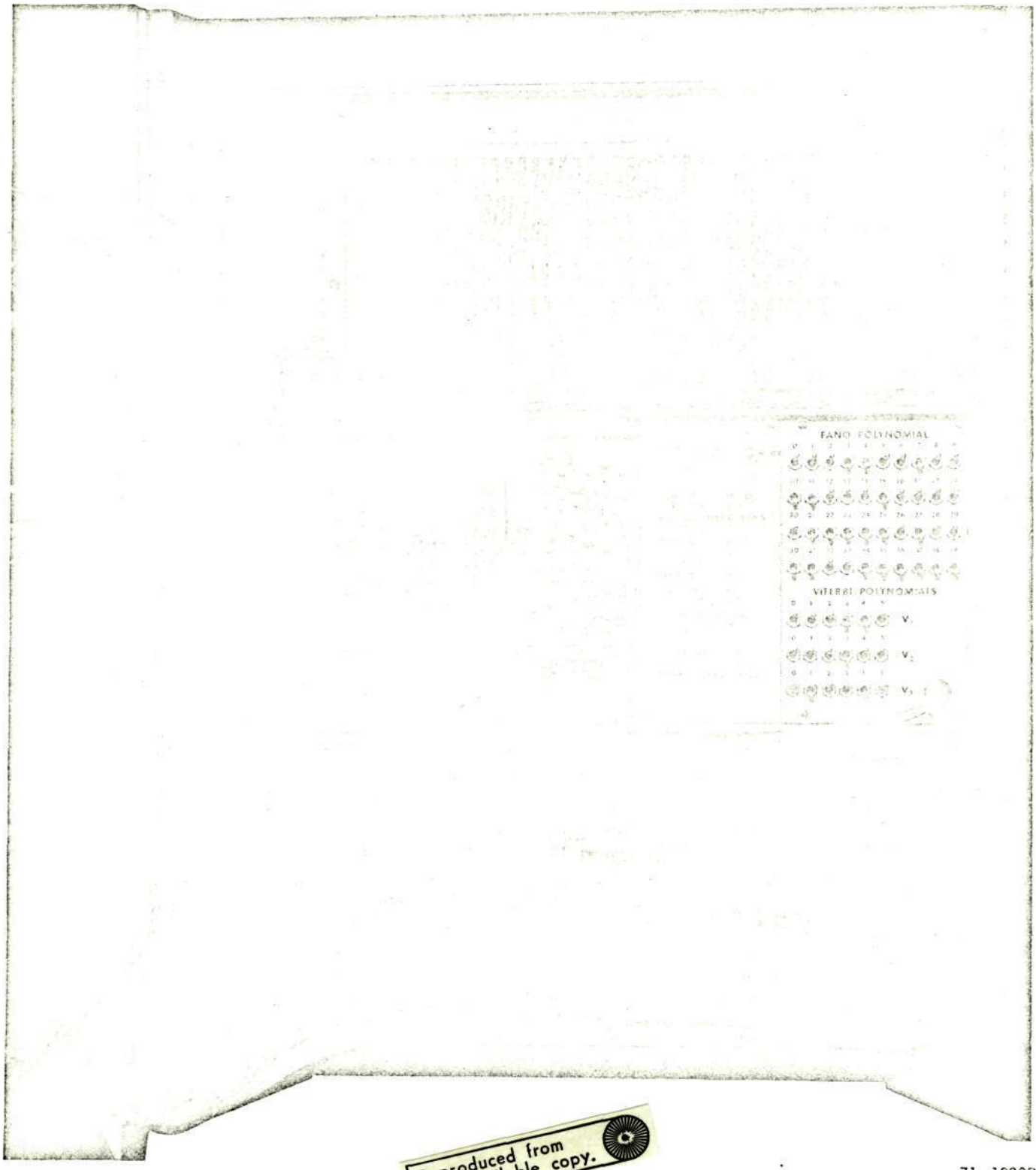


Figure A1-2.3. Transmitter Convolutional Switch Panel

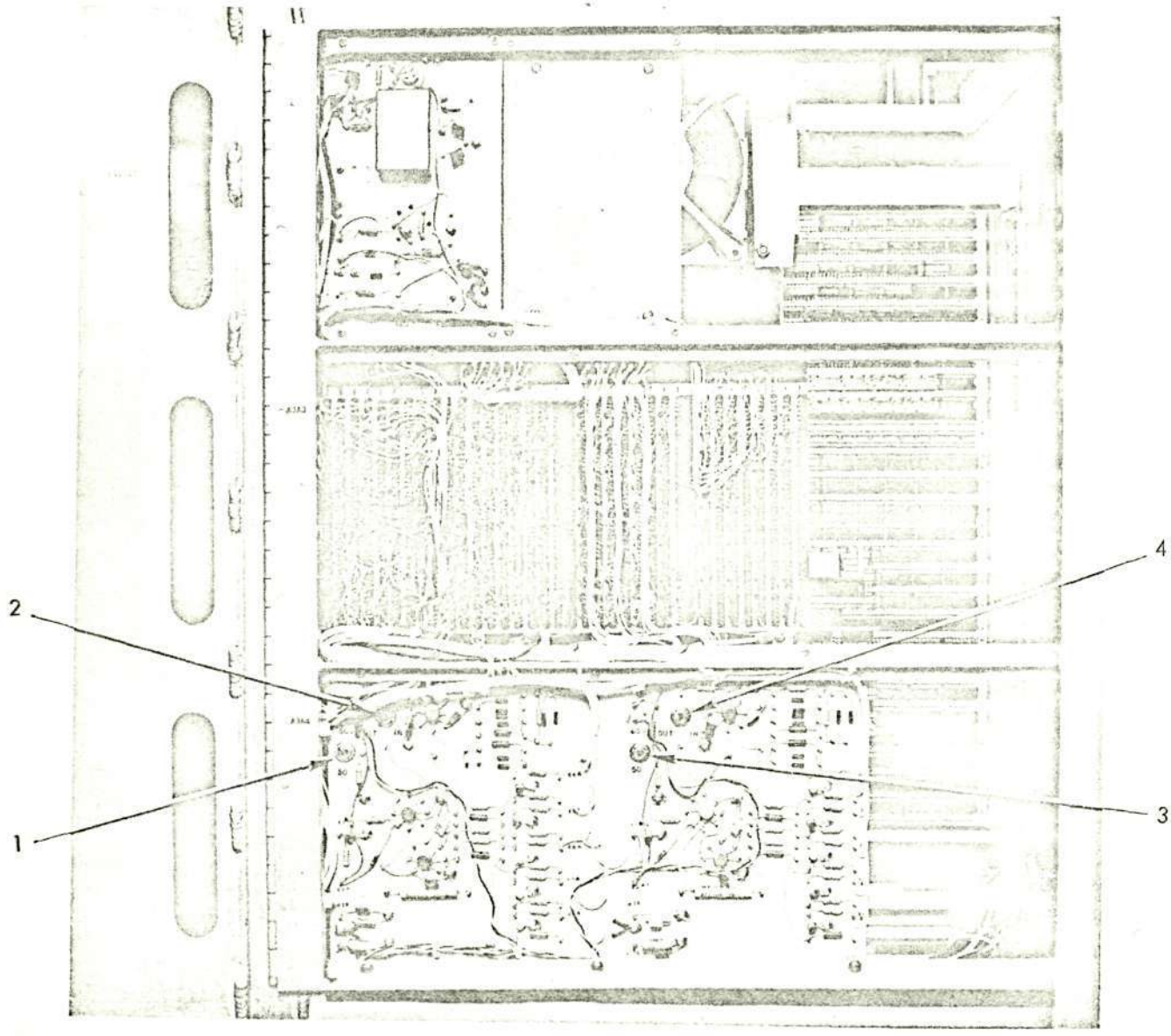


Figure A1-2.4. Delta Modulator

Table A1-2.4

Index No.	Control	Ref Des	Function
1	600/50	S1	Selects Input Impedance of Audio Channel 1
2	IN/OUT	S2	Switches companding in or out for Audio Channel 1
3	600/50	S3	Selects input impedance of Audio Channel 2
4	IN/OUT	S4	Switches companding in or out for Audio Channel 2

A1-2.5 Transmitter AC Panel - A6

The ac panel A6 is mounted at the rear of the rack, and is below the rear door. Table A1-2.5 lists the controls and indicator and defines their functions.

Table A1-2.5

Control or Indicator	Circuit Ref. Des.	Function
Main Power/15A Circuit Breaker	CB1	In ON position, provides ac power to filter box
Running Time, time totalizing meter	M1	Indicates DC/EC transmitter operating hours in tenths, units, tens, hundreds, and thousands of hours
LOGIC POWER/5A, Fuse	F1	Provides protection on ac side of the power supplies
AC INPUT	P1	AC input to the transmitter
AC OUTPUT	P2	AC output for test equipment (limit to 2A)

A1-2.6 Receiver Control Panel - A3

The Receiver Control Panel is arranged to provide a schematic representation of the system configuration. Where feasible, inputs and outputs of functional units are brought to jacks on the panel for interconnection and monitoring, and to allow independent use of sub-systems of the receiver.

The jacks on the panel are keyed in Figure A1-2.6-1, and are described in Table A1-2.6-1. The controls are keyed in Figure A1-2.6-2 and are described in Table A1-2.6-2.

Table A1-2.6-1. Receiver Control Panel Connectors

Index No.	Connector	Ref. Des.	Function
1	BØ - 1/2 QP	P6	Input to Bit Sync A (2A2) for use in both BØ and QP modes
2	1/2 QP	P7	Input to Bit Sync B (2A1) for use in QP mode only
3	EXTERNAL Clock Inputs	P13	External clock input to Bit Sync A when it is to be operated in the simulate (external clock) mode, for both BP and QP.
4	EXTERNAL Clock Input	P14	External clock input to Bit Sync B when it is to be operated in the simulate (external clock) mode for QP only.
5	EXT	P19	External data reference signal input for Comparator B
6	CLOCK	P20	Clock input to Comparator B
7	DATA	P21	Data input to Comparator B
8	ERROR	P25	Error rate output from Comparator B
9	BIT RATE	P27	Bit Rate clock input to Comparator A

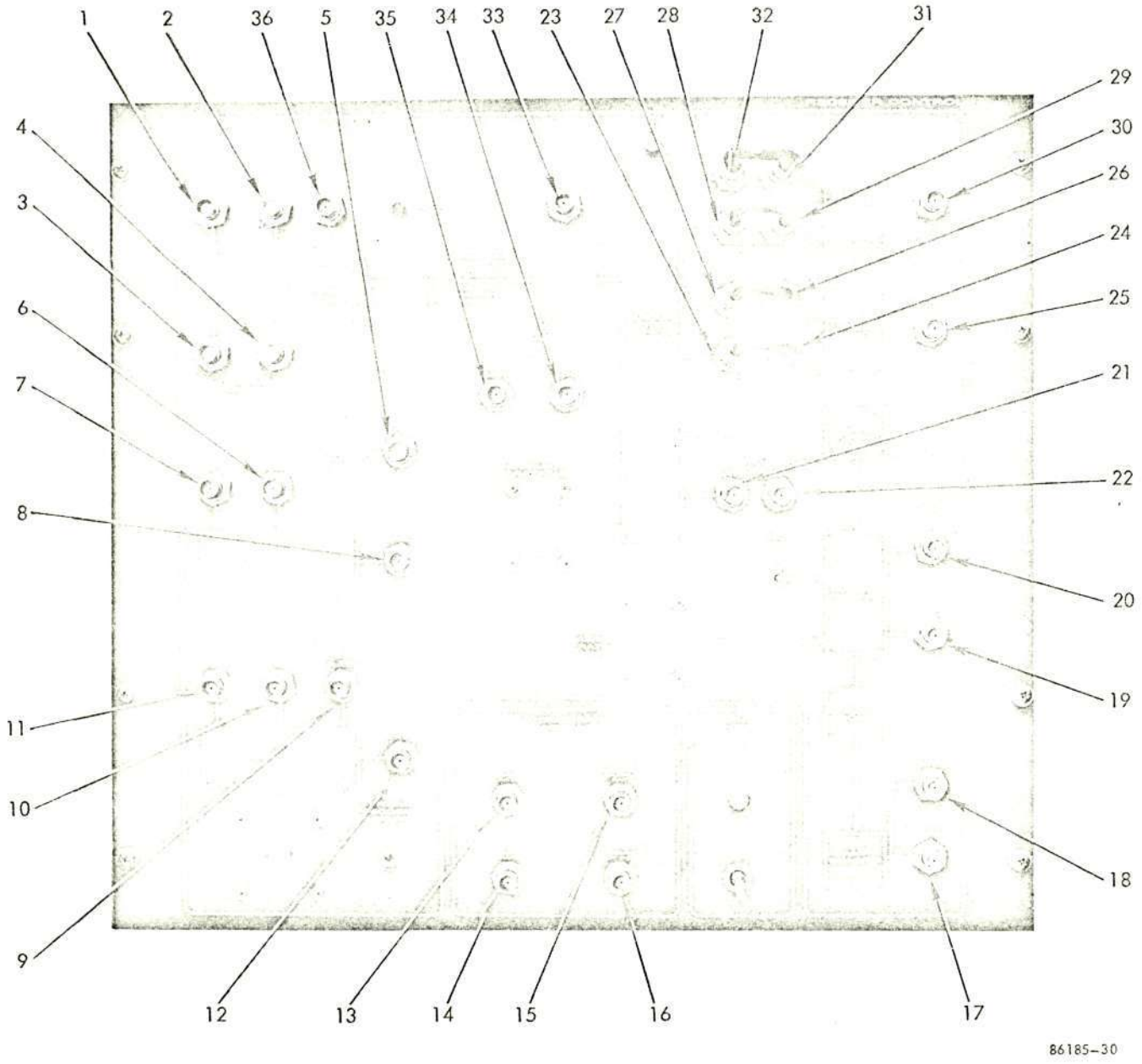


Figure A1-2.6-1. Receiver Control Panel

Table A1-2.6-1. Receiver Control Panel Connectors (Continued)

Index No.	Connector	Ref. Des.	Function
10	DATA 2	P28	Reference data input to Comparator A
11	DATA 1	P29	Data input to Comparator A
12	ERROR	P30	Error rate output from Comparator A
13	FRAME RATE	P33	Frame rate pulse output
14	INFO RATE	P36	Information rate clock output
15	RECONSTR SAMPLE RATE	P32	Sample rate clock output
16	TRANSMIT BIT RATE	P35	Transmit bit rate clock output
17	TV OUT	P34	Video output
18	MONITOR	P31	TV output signal monitor
19	TV SYNC V	P26	Vertical Sync pulse output
20	TV SYNC H	P24	Horizontal sync pulse output
21	PCM DATA	P23	PCM data output from demultiplexer
22	PCM CLOCK	P22	PCM clock output from demultiplexer
23	CLOCK	P16	Audio channel 2 clock output from demultiplexer
24	CLOCK	P15	Audio channel 2 clock input to Voice Demod
25	CHANNEL 2	P12	Audio channel 2 output
26	DATA	P10	Audio channel 2 data input to Voice Demod
27	DATA	P11	Audio Channel 2 data output from Demultiplexer

Table A1-2.6-1. Receiver Control Panel Connectors (Continued)

Index No.	Connector	Ref. Des.	Function
28	CLOCK	P9	Audio channel 1 clock output from Demultiplexer
29	CLOCK	P8	Audio channel 1 clock input to Voice Demod
30	CHANNEL 1	P3	Audio channel 1 output
31	DATA	P1	Audio channel 1 data input to Voice Demod
32	DATA	P2	Audio channel 1 data output from Demultiplexer
33	MONITOR	P4	Group Sync input data monitor
34	CLOCK	P17	External clock input to Group Sync
35	DATA	P18	External data input to Group Sync
36	MONITOR	P5	Bit Sync output monitor

Table A1-2.6-2. Receiver Control Panel Controls and Indicators

Index No.	Control or Indicator	Ref. Des.	Function
1	GOOD DATA (Indicator Light)	DS 2	When illuminated, indicates selected decoder has achieved Branch Synchronization
2	(Selector Switch)	S 1	Selects Viterbi (R = 1/2), Viterbi (R = 1/3), Fano (R = 1/2), or External input data and clock as input to Group Sync

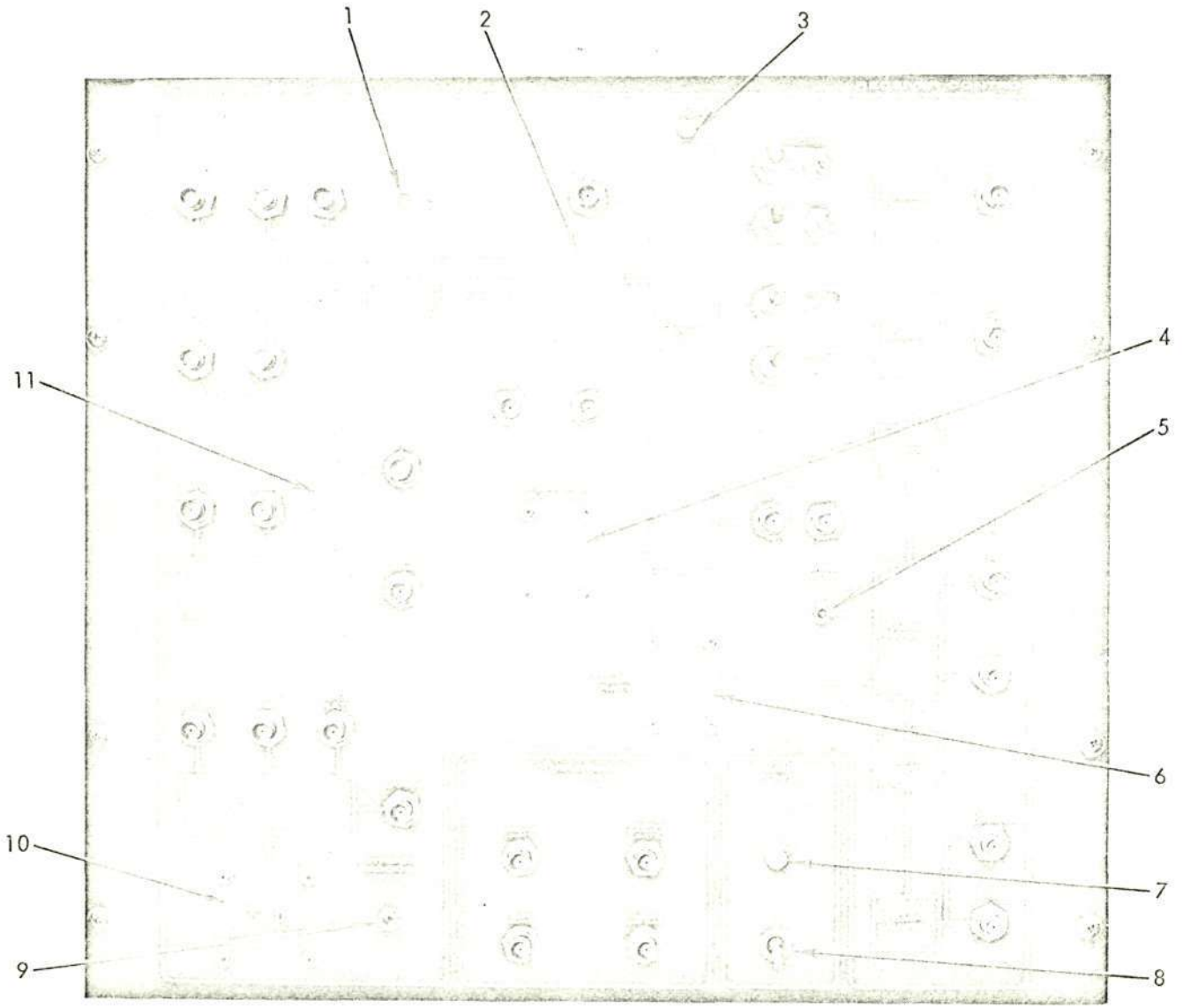


Figure A1-2.6.2. Receiver Control Panel Controls and Indicators

Table A1-2.6-2. Receiver Control Panel Controls and Indicators (Continued)

Index No.	Control or Indicator	Ref. Des.	Function
3	LOCK (Indicator light)	DS 1	When illuminated, indicates Group Sync Lock
4	Information RATE	S 3	Selects 1 to 9 Mb/s information rate
5	DATA BITS	S 4	Selects the number of data bits (4, 5, or 6) in the 10-bit data-plus-time-tag words used in the ZOP/ZOI mode
6	SAMPLE RATE	S 5	Selects 1 to 9 MHz sample rate
7	AC POWER (Indicator Light)	DS 3	Power on/off indicator
8	ON (toggle switch)	S 6	Power on/off Switch
9	VITERBI DECODER DELAY	S 7	Switches fixed Viterbi decoder delay in or out of the reference channel of Comparator A
10	DELAY BITS (Thumbwheel switch)	S 8/9	Selects 0 to 7.5 bits delay for the reference channel of Comparator A
11	REFERENCE	S 2	Selects all 1's, all 0's or an external input as the reference signal for Comparator B

A1-2.7 Delta Demodulator, Group Synchronizer and Reconstructor Mode Controls

Controls for the Delta Demodulators and the Group Synchronizer and the switch for selecting between the ZOP (I) Reconstructor and the Statistical Decoder are shown in Figure A1-2.7 and are described in Table A1-2.7.

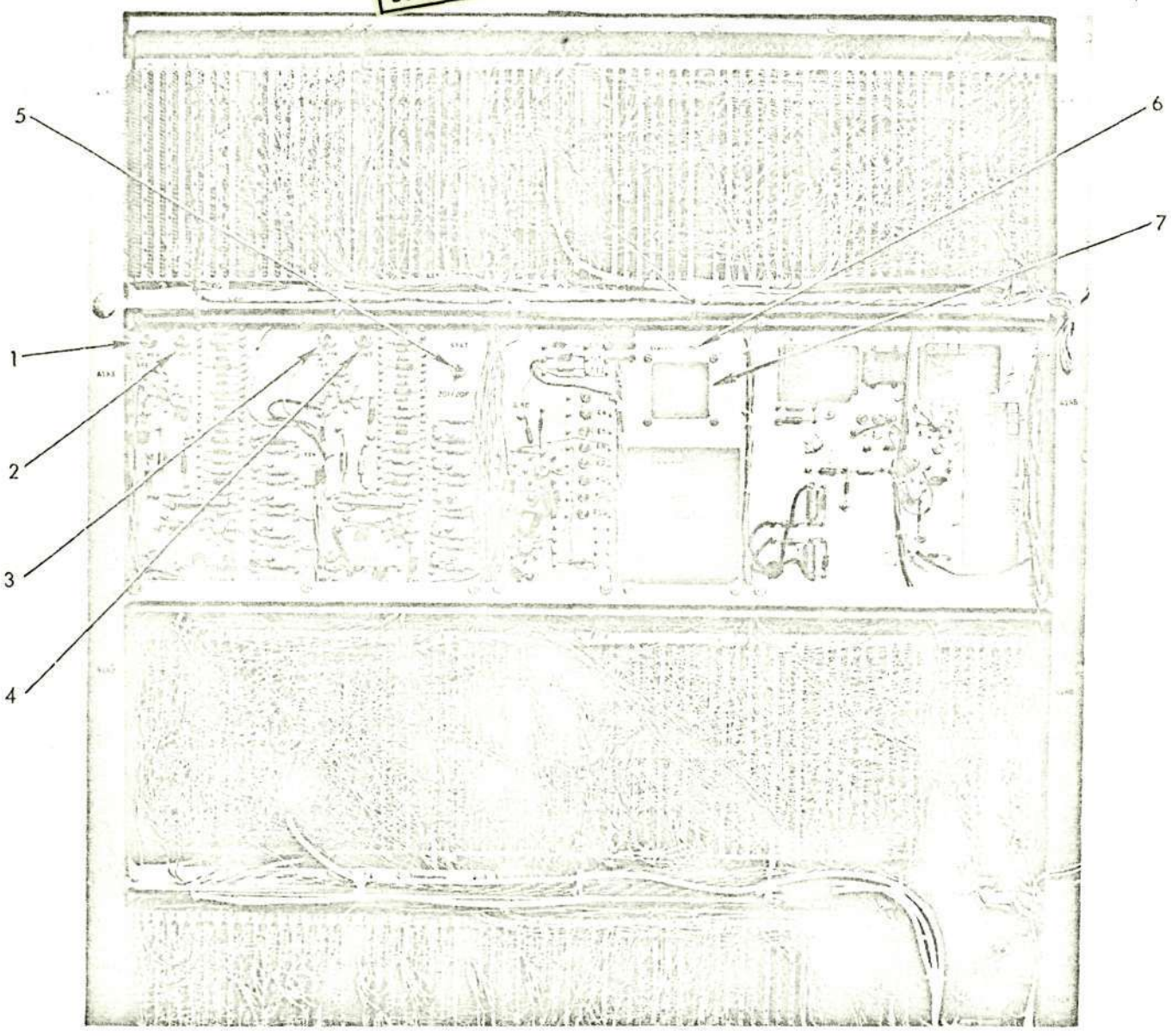


Figure A1-2.7. Delta Demodulator, Group Sync Reconstructor Mode Switches

Table A1-2.7

Index No.	Control	Ref. Des.	Function
1	600/50	S 1	Selects output impedance of Audio Channel 1
2	IN/OUT	S 2	Switches Compander in or out of Audio Channel 1
3	600/50	S 3	Selects output impedance of Audio Channel 2
4	IN/OUT	S 4	Switches Compander in or out of Audio Channel 2
5	STAT-ZOP/ZOI		Selects either the Statistical Decoder or the ZOP/ZOI Reconstructor as the source of digital video words to the D/A Converter
6	SEARCH		Selects the number of errors allowed by the group synchronizer in the search mode
7	LOCK		Selects the number of errors allowed by the group synchronizer in the Lock mode

A1-2.8 Fano Decoder/Buffer Switch Panel - A8A1A14

The Receiver Fano Switch Panel A8A1A14 provides the programming for the Fano polynomial, the Metric Delta, and Self-Test for the Buffer and Fano memories. Figure A2-2.8 depicts the controls; Table A1-2.8 lists the controls and defines their functions.

Table A1-2.8

Control	Circuit Reference Designation	Function
FANO POLYNOMIAL (0-39)	S1 - S40	Selects coefficients for Generator Polynomial used in Fano Decoder
BUFFER TEST	S41	Puts Receiver Rate Buffer Control in a Self-Test mode
MEMORY TEST	S42	Puts the Fano Decoder in a Self-Test mode
TEST DATA	S43	Data of all 1's or all 0's used when the Fano Decoder is in Self-Test mode
DELTA	S44	Selects the Delta size employed in the Fano Decoder
BUFFER SYNC	S45	None
TEST SEQUENCE REPETITION	S46	Used when Buffer is in Self-Test to write one or two patterns in memory
MAXIMUM BUFFER SIZE	S47 - S54	Select the maximum number of words and size of the Buffer memory
TEST SWITCH	S55 - S63	Used when buffer is in Self-Test to set up a Buffer Sync word

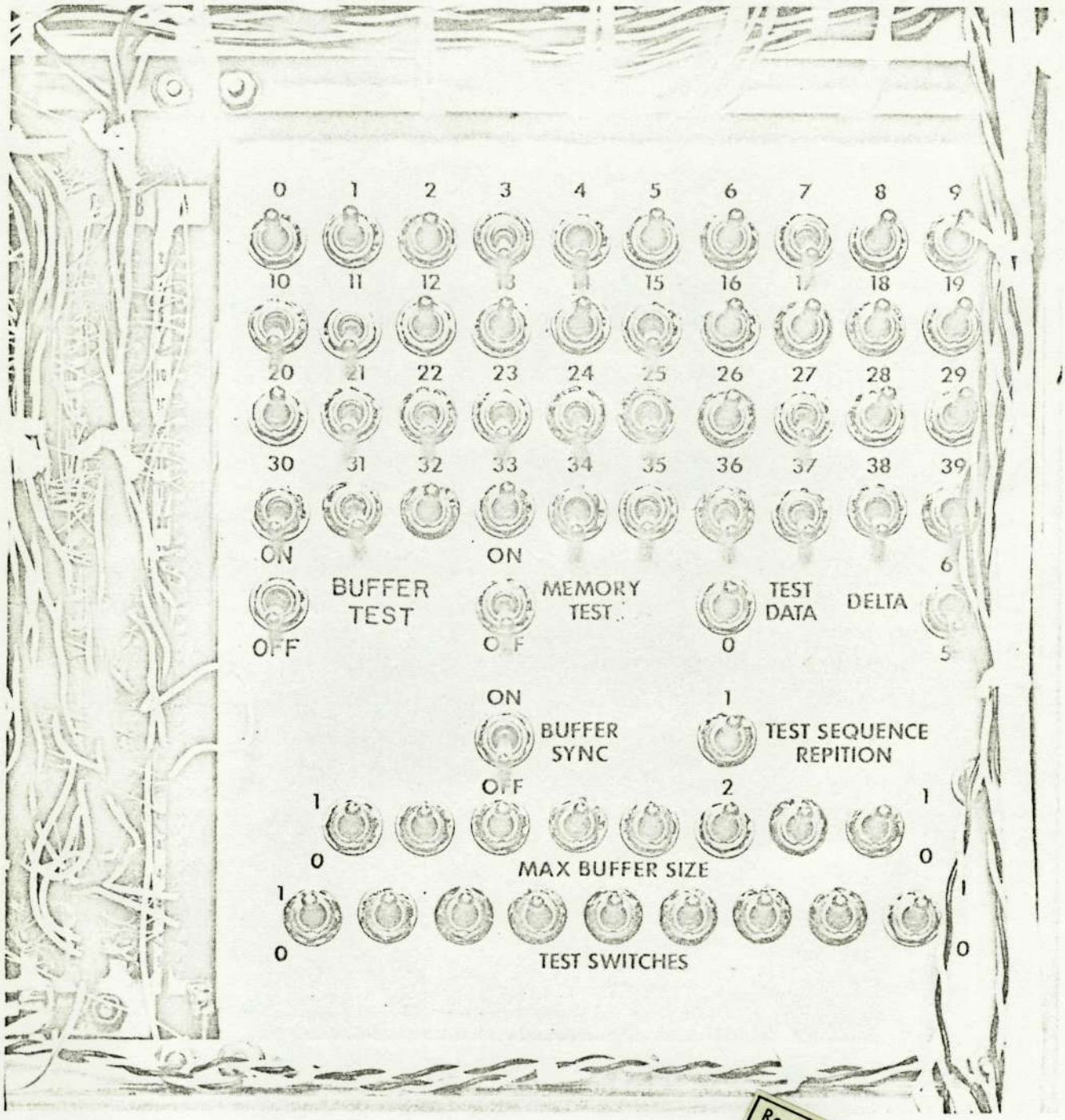


Figure A1-2.8. Fano Decoder/Buffer Switch Panel

A1-2.9 Receiver Viterbi Patch Panel - A8A3A8

The Viterbi patch panel configuration layout is as shown in Figure A1-2.9-1; the pin numbering of a typical plug-in is shown in Figure A1-2.9-2. Figure A1-2.9-3 is a photo showing a typical set of patches installed. The patch panel connects incremental correlations to survivor correlations using the patch plug-in. Each correlation contains 5 bits of data, thus the panel has 5 identical 1 x 8 patches (A_X, A_X+8, A_X+16, A_X+24, A_X+32 are identical where X = 1 -8). Pins 1 - 8 of the plug-in represent the incremental correlations while pins 9 - 16 represent the survivor correlations. The following truth table represents which incremental correlations are connected to the various pins. r_3, r_2, r_1 is a function of the generating polynomial.

PIN	$r_3 r_2 r_1$
1	0 0 0
2	0 0 1
3	0 1 0
4	0 1 1
5	1 0 0
6	1 0 1
7	1 1 0
8	1 1 1

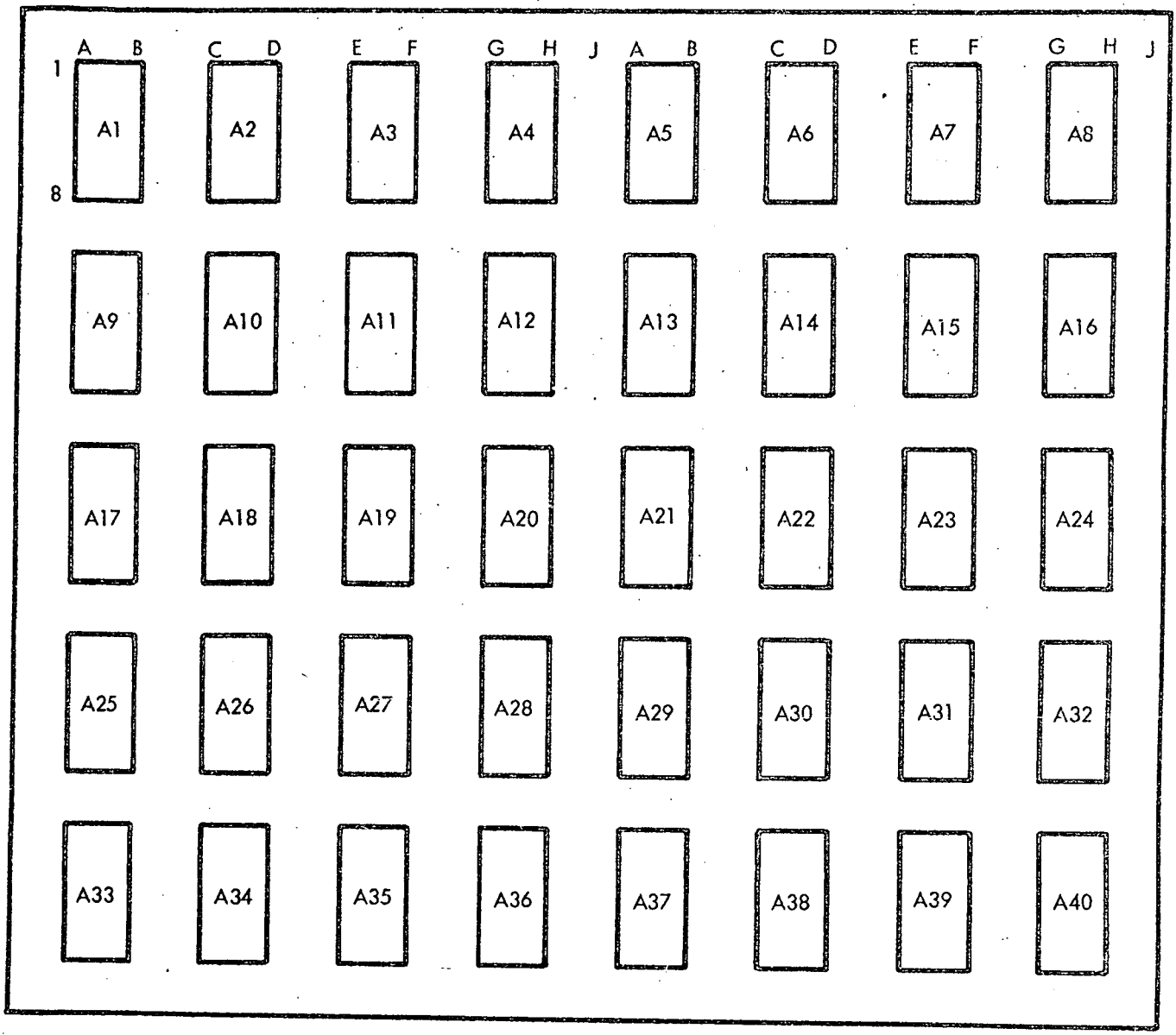
Pin 1 of each patch A1 - A8 are bused together; likewise the same is true for pins 2 - 8. Table A1-2.9-1 lists which outputs represent the varies state. The five most recent received bits make a state. When a "0" or a "1" is shifted in, a new $r_3 r_2 r_1$ is generated. Thus, a connection would be made on a patch plug-in between the present state with a bit in to the corresponding $r_3 r_2 r_1$.

Example: Present state - 00011, input bit - 1 $r_3 r_2 r_1$ - 001

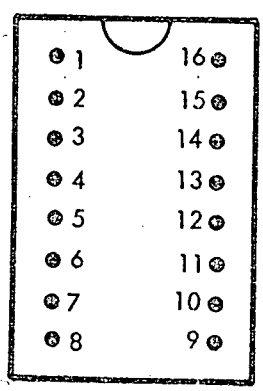
Connection: A1 - 9 to A1 - 2

Table A1-2.9-1. Present State Tabulation

Pin	Present State	Input Bit	Pin	Present State	Input Bit
A1-16	00000	0	A5-16	10000	0
A1-15	00000	1	A5-15	10000	1
A1-14	00001	0	A5-14	10001	0
A1-13	00001	1	A5-13	10001	1
A1-12	00010	0	A5-12	10010	0



A1-2.9-1. Patch Board



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A1-2.9-2. Patch Plug In

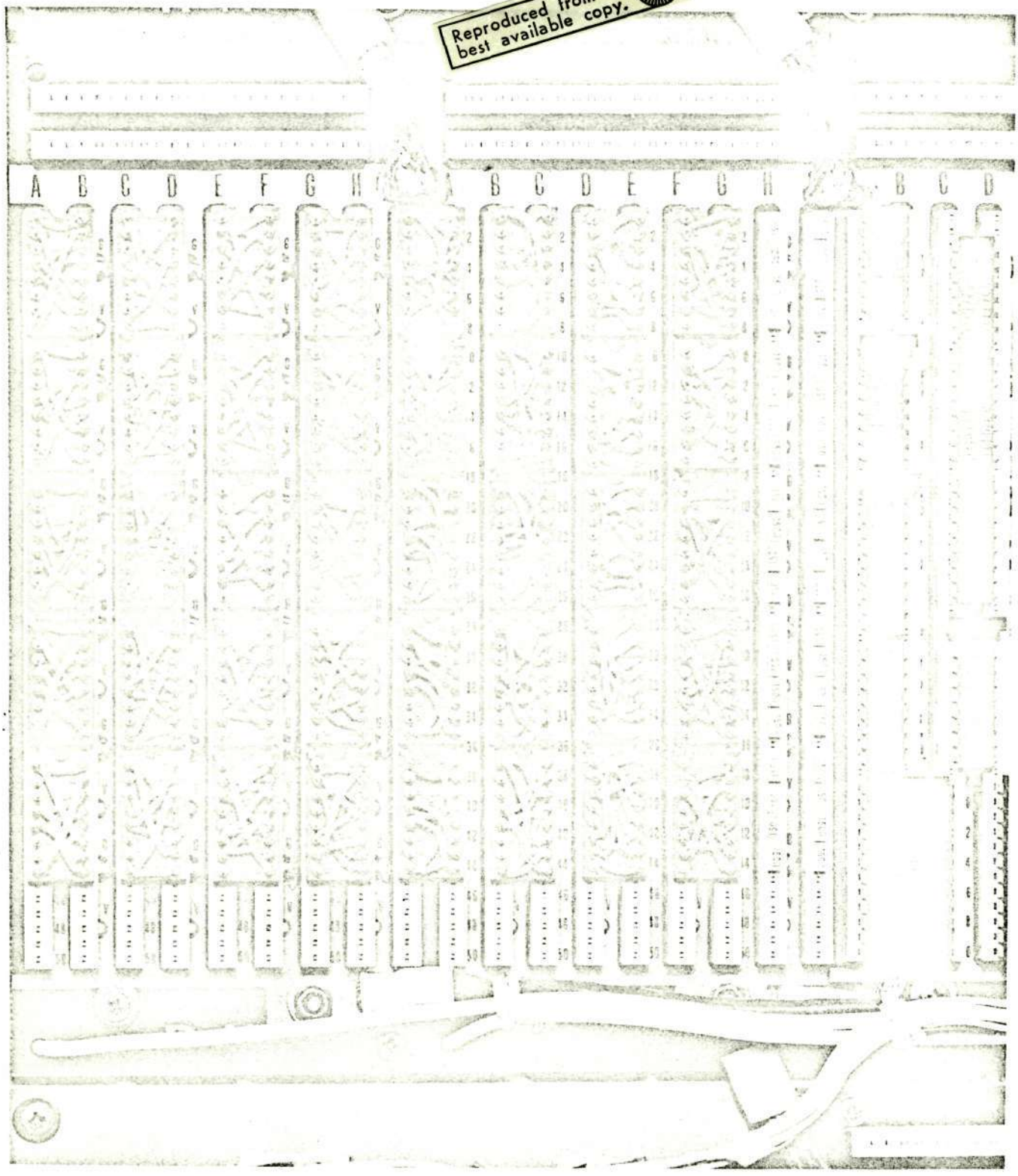

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Figure A1-2.9-3. Viterbi Decoder Patch Panel

Table A1-2.9-1. Present State Tabulation (Continued)

Pin	Present State	Input Bit	Pin	Present State	Input Bit
A1-11	00010	1	A5-11	10010	1
A1-10	00011	0	A5-10	10011	0
A1-9	00011	1	A5-9	10011	1
A2-16	00100	0	A6-16	10100	0
A2-15	00100	1	A6-15	10100	1
A2-14	00101	0	A6-14	10101	0
A2-13	00101	1	A6-13	10101	1
A2-12	00110	0	A6-12	10110	0
A2-11	00110	1	A6-11	10110	1
A2-10	00111	0	A6-10	10111	0
A2-9	00111	1	A6-9	10111	1
A3-16	01000	0	A7-16	11000	0
A3-15	01000	1	A7-15	11000	1
A3-14	01001	0	A7-14	11001	0
A3-13	01001	1	A7-13	11001	1
A3-12	01010	0	A7-12	11010	0
A3-11	01010	1	A7-11	11010	1
A3-10	01011	0	A7-10	11011	0
A3-9	01011	1	A7-9	11011	1
A4-16	01100	0	A8-16	11100	0
A4-15	01100	1	A8-15	11100	1
A4-14	01101	0	A8-14	11101	0

Table A1-2.9-1. Present State Tabulation (Continued)

Pin	Present State	Input Bit	Pin	Present State	Input Bit
A4-13	01101	1	A8-13	11101	1
A4-12	01110	0	A8-12	11110	0
A4-11	01110	1	A8-11	11110	1
A4-10	01111	0	A8-10	11111	0
A4-9	01111	1	A8-9	11111	1

If a rate 1/2 code is used then r_1 and r_2 are the terms generated and r_3 is a "do not care" condition, thus $r_3r_2r_1$-000,100 are equal. In making connections for this condition, care must be taken to distribute the loading equally between the two equal $r_3r_2r_1$, that is if a connection is required between a pin and r_2r_1-00, this connection could be made to $r_3r_2r_1$-000 100.

The table below is a list of the generating polynomials for which patch plug-ins are provided.

		V_1						V_2						V_3					
Rate	Constraint Length	0	1	2	3	4	5	0	1	2	3	4	5	0	1	2	3	4	5
1/3	6	1	1	1	0	0	1	1	1	1	0	1	1	1	0	1	1	0	1
1/3	5	1	0	1	0	1	0	1	1	1	1	1	0	1	1	0	1	1	0
1/3	4	1	1	1	1	0	0	1	1	0	1	0	0	1	0	1	1	0	0
1/2	6	1	1	0	1	0	1	1	0	0	0	1	1	0	0	0	0	0	0
1/2	5	1	1	0	0	1	0	1	0	1	1	1	0	0	0	0	0	0	0
1/2	4	1	1	0	1	0	0	1	1	1	1	0	0	0	0	0	0	0	0
1/2	3	1	0	1	0	0	0	1	1	1	0	0	0	0	0	0	0	0	0

Table A1-2.9-2 is listings for the location of each plug-in for the codes provide

Table A1-2.9-2. Location Tabulation for Plug-Ins

a. K = 6, R = 1/3

Plug-In	Location
-01	A1, A9, A17, A25, A33
-02	A2, A10, A18, A26, A34
-03	A3, A11, A19, A27, A35
-04	A4, A12, A20, A28, A36
-05	A5, A13, A21, A29, A37
-06	A6, A14, A22, A30, A38
-07	A7, A15, A23, A31, A39
-08	A8, A16, A24, A32, A40

b. K = 5, R = 1/3

Plug-In	Location
-09	A1, A5, A9, A13, A17, A21, A25, A29, A33, A37
-10	A2, A6, A10, A14, A18, A22, A26, A30, A34, A38
-11	A3, A7, A11, A15, A19, A23, A27, A31, A35, A39
-12	A4, A8, A12, A16, A20, A24, A28, A32, A36, A40

c. K = 4, R = 1/3

Plug-In	Location
-13	A_{2x-1}; where x = 1, 2, ..., 20
-14	A_{2x}; where x = 1, 2, ..., 20

d. K = 6, R = 1/2

Plug-In	Location
-15	A1, A8, A9, A16, A17, A24, A25, A32, A33, A40
-16	A2, A7, A10, A15, A18, A23, A26, A31, A34, A39
-17	A3, A6, A11, A14, A19, A22, A27, A30, A35, A38
-18	A4, A5, A12, A13, A20, A21, A28, A29, A36, A37

e. K = 5, R = 1/2

Plug-In	Location
-19	A_{4x-3}; where x = 0, 1, ..., 10
-20	A_{4x-2}; where x = 0, 1, ..., 10

Table A1-2.9-2. Location Tabulation for Plug-Ins (Continued)

Plug-In	Location
-21	A_{4x-1}; where x = 0, 1, ..., 10
-22	A_{4x} ; where x = 0, 1, ..., 10

f. K = 4, R = 1/2

Plug-In	Location
-23	A_{2x-1}; where x = 0, 1, ..., 20
-24	A_{2x} ; where x = 0, 1, ..., 20

g. K = 3, R = 1/2

Plug-In	Location
-25	A1 - A40

A1-2.10 Receiver Viterbi Switch Panel - A8A3A10

The Receiver Viterbi Switch Panel A8A3A10 provides control signals for the Viterbi Decoder function. Figure A1-2.10 depicts the controls. Table A1-2.10 gives programming information for the switches.

Table A1-2.10. Programming Information - Viterbi Switch Panel

Quantization	S1	S2	Decoding Depth	S3	S4	S5	Constraint Length	S6	S7
1 Bit	0	1	4	0	0	0	3	0	0
2 Bits	1	0	8	1	0	0	4	1	0
3 Bits	1	1	12	0	1	0	5	0	1
			16	1	1	0	6	1	1
			20	0	0	1			
			24	1	0	1			
			28	0	1	1			
			32	1	1	1			

A1-2.11 Quadraphase Data Conbiner - A9

The Quadraphase assembly contains a switch which selects quadraphase on biphase operation.

A1-2.12 Receiver AC Panel - A7

The AC Panel A7 is mounted at the rear of the left hand rack and is below the rear door. Table A1-2.12 lists the controls and indicator and defines their functions.

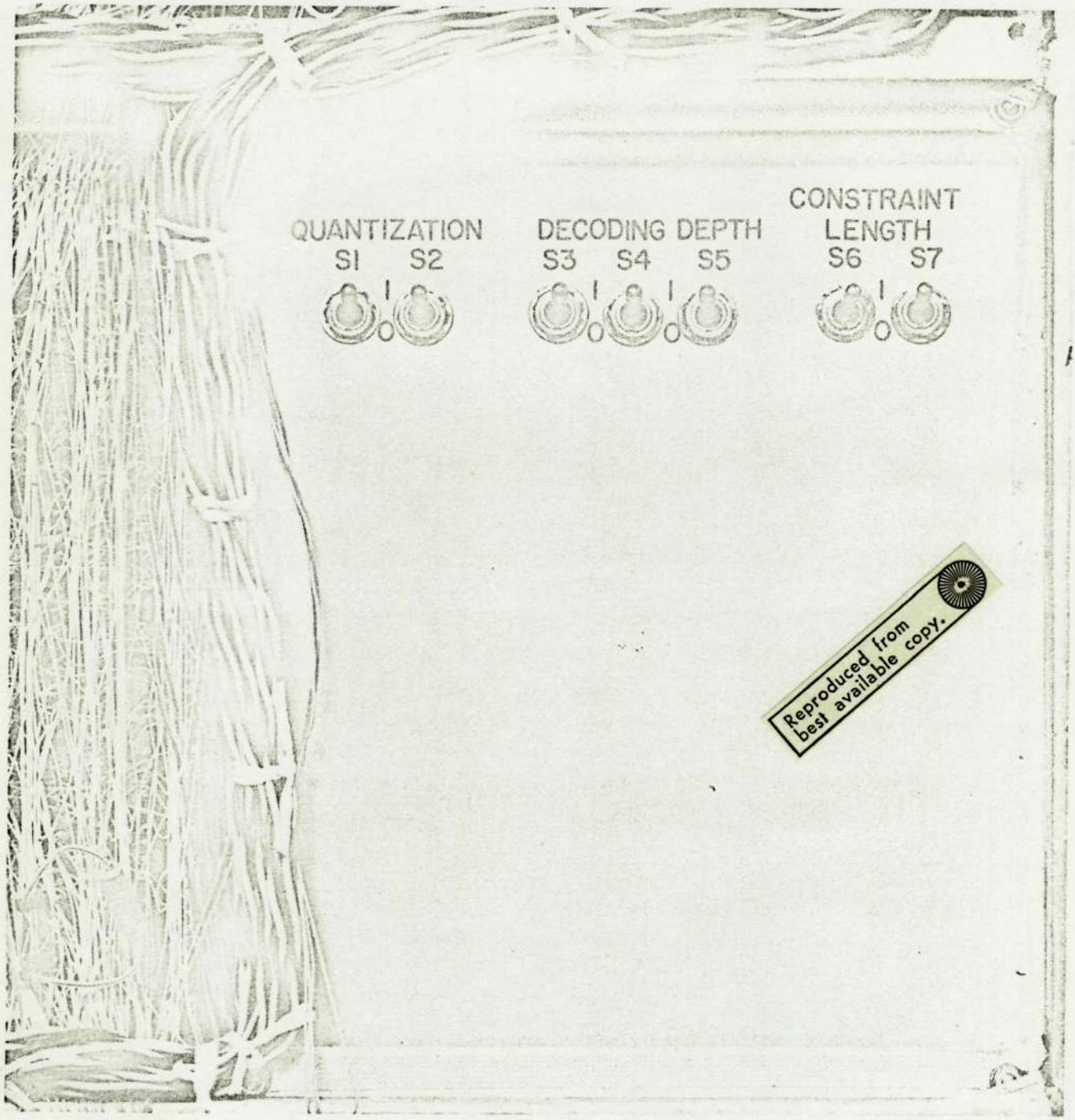

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Figure A1-2.10. Receiver Viterbi Switch Panel

Table A1-2.12

Figure			
CB1	Main Power/50A Circuit Breaker	CB1	In ON position, provides AC power to Receiver
M1	Running Time, Time Totalizing Meter	M1	Indicates DC/EC Receiver operating hours in tenths, units, tens, hundreds, and thousands of hours
F1	Analog Power/2A, Fuse	F1	Provides protection on the AC side of the +15 and -15 analog power supplies
P1	AC Output	P1	AC output for test equipment (limit to 2A)
Input	AC Input	--	

A1-3.0 OPERATING PROCEDURE

The DC/EC Test Set is placed into normal operation by the Transmitter Control Panel and the Receiver Control Panel. If the DC/EC has not been operated after a long period of idleness or after major maintenance, the acceptance test can be performed to verify the operational readiness of the system. Normal operating procedure is as follows:

a. Transmitter

1. Connect TV camera to TV IN (A3A4P2).
2. Select desired SAMPLE RATE (A3A4S5).
3. Select size of sample to 4, 5 or 6 on DATA BITS (A3A4S4).
4. Select Reducer operating MODE to ZØI, ZØP or Statistical (A3A4S3).
5. Select INFORMATION RATE (A3A4S2).
6. Select Channel codes input to be either MUX or EXT (A3A4S6). If EXT, INFO BIT RATE (A3A4P30) should be used as EXT devices clock.
7. Select the channel coder to operate in VITERBI (R = 1/3), VITERBI (R = 1/2) or FANO (R = 1/2) mode (A3A4S1).
8. Select PCM INPUT to be PCM, all 1's, or all 0's (A3A4S7). If PCM selected, the external device should be driven from the PCM CLOCK (A3A4P31). The all 1's or 0's is used with bit error rate test when using the Fano Decoder.
9. Patch channel coder output to Buffer Amplifier input if desired (A3A4P4 to A3A4P9).
10. Patch Delta Modulator channel 1 data and clock to MUX input (data A3A4P10 to A3A4P11; Clock A3A4P12 to A3A4P13).
11. Patch Delta Modulator channel 2 data and clock to multiplexer input (data A3A4P16 to A3A4P17; clock A3A4P19 to A3A4P20).
12. Connect voice to VOICE CHANNELS (A3A4P14 and A3A4P15).
13. Select the desired attenuation on NOISE ATTENUATION DB (A3A4AT1).
14. Patch the noise into the buffer amplifier, if desired (A3A4P24 to A3A4P23).

15. Select the Reducer's tolerance to be fixed or adaptive (A3A2A4S5).

16. Select the Reducer's tolerance (A3A2A4S1 - S4).

17. Select the Rate Control NRS counter bias setting (A3A4A4S6 - S10). Determine the setting log: NRS = 4.15 (IR-.25) (IR = Information Rate and SR = Sample Rate).

18. Select PLUS to calculate TOL as desired (A3A4A4S11 and S12).

19. Select MINUS to calculate TOL as desired (A3A4A4S13 and S14).

20. Select maximum buffer sizes (A3A4A4S15 - S22). Should normally be all 1's.

21. Select the desired coder polynomial (A3A4A5).

22. Plug in the desired amplitude shaping patch (A3A2A2).

23. Place the circuit breaker in the ON position (A6 CB1).

24. Turn on the A/D converter A1.

25. Turn on the Filter A2.

26. Turn on the Memory power supply PS2.

27. Turn on Transmitter Power with the AC power switch (A3A4S8).

b. Receiver

1. Select the input to the GROUP SYNC and DECOM (A3S1). The setting should be the same as the Transmitter (A3A4S1) unless EXT is used.

2. Patch the GROUP SYNC and DECOM voice outputs to the Delta Demodulators (A3P2 to A3P1, A3P9 to A3P8; A3P11 to A3P12; A3P16 to A3P15).

3. Voice outputs are on A3P3 and A3P12.

4. Select INFORMATION RATE (A3S5). Should be the same as Transmitter (A3A4S2).

5. Select sample size on DATA BITS (A3S4). Should be the same as Transmitter (A3A4S4).

6. Select SAMPLE RATE (A3S5). Should be the same as Transmitter (A3A4S5),

7. PCM output, data and clock are on A3P22 and A3P23.

8. Connect TV monitor to TV OUT (A3P34).

9. Comparator A

   (a) To monitor bit error rate on link (i.e., at input of decoder at the Receiver).

   - VITERBI DECODER DELAY to OUT (A3S7).
   - Patch DATA (A3P29) to Transmitter Channel Coder Output (A3A4P5).
   - Patch Bit Sync output MONITOR (A3P5) to DATA 2 (A3P28).
   - Patch TRANSMIT BIT RATE (A3P35) to BIT RATE (A3P27).
   - Patch ERROR (A3P30) to the Counter (M1) INPUT A (use 50-ohm termination). Set the counter to frequency mode.
   - When in operation the DELAY BIT switch is selected to give minimum error reading.
   - A higher bit rate (e.g., 27 Mb/s) cable delays are significant and must be properly matched.

   (b) To Monitor Bit Error Rate over the VITERBI decoder. Same as (a) except:

   - VITERBI DECODER DELAY to IN (A3S7).
   - Patch DATA 1 (A3P29) to Transmitter Mux Data (A3A4P3).
   - Patch DATA 2 (A3P28) to GROUP SYNC and DECOM input monitor (A3P4).
   - Patch INFO RATE (A3P36) to BIT RATE (A3P27).

10. Comparator B - To monitor Bit Error Rate over the Fano Decoder.

   - Set switch A3S2 to same setting as switch A3A4S7 on Transmitter.
   - Patch PCM DATA (A3P16) and CLOCK (A3P15) to DATA (A3P21) and CLOCK (A3P22).
   - Connect counter as explained under Comparator A part b.

11. Plug in the complementary amplitude shaping patch of the one used in the Transmitter (A8A1A6).

12. Select the desired Fano Decoder Polynomial (A8A1A14S1 - S40).

13. Select BUFFER TEST to OFF (A8A1A14S41).

14. Select MEMORY TEST to OFF (A8A1A14S42).

15. Select the desired DELTA (A8A1A14S44).

16. Select the BUFFER SYNC to OFF (A8A1A14S45).

17. Select the desired MAX BUFFER SIZE (A8A1A14S47 - S54). Should be all 1's.

18. Select desired patch to program the VITERBI Patch Panel (A8A3A8).

19. Select VITERBI QUANTIZATION (A8A3A10S1 and S2).

20. Select VITERBI Decoder Depth (A8A3A10S3-S5).

21. Select VITERBI Constraint Length (A8A3A10S6 and S7).

22. Place the circuit breaker in the ON position (A7CB1).

23. Turn on the Bit Sync (A2) (and A1 for QP operation).

24. Turn on the Counter (M1).

25. Turn on the Memory Power Supply (PS3).

26. Turn on the Memory Power Supply (PS4).

27. Turn on Receiver Power with the AC power switch (A3S6).

28. Connect the output of the Transmitter and the Input (BØ) of the Receiver.

The Transmitter and Receiver can also be connected via a Modem and a real or simulated RF link.