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Lockheed

MISSILES & SPACE COMPANY

A GROUP DIVISION OF LOCKHEED AIRCRAFT CORPORATION

SUNNYVALE, CALIFORNIA

7 AS 9- 10742

CR-115719

IMBIMS PHASE B.4

LABORATORY VERIFICATION
OPTICAL SIGNAL COUPLING

Appendix C - Section 12

December 21, 1970
IMSC - A980463

(NASA-CR-115719) LABORATORY VERIFICATION
OPTICAL SIGNAL COUPLING. IMBIMS PHASE B.4,
APPENDIX C, SECTION 12 (Lockheed Missiles
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12.0 Optical Coupler

The purpose of this laboratory verification effort was to design optical couplers that could be used in the IMBIMS "hardwire" mode. One coupler transmits data from the bio-belt to the central data system and the other coupler transmits audio frequencies in the opposite direction, from the central data system to the bio-belt. The objective is to isolate the ground system at the body worn bio-belt electronics and the main ground at the central data system or Biomedical and Behavioral Station. Safety of the subject wearing the bio belt measuring electronics is the ultimate purpose in isolating him from main system ground.

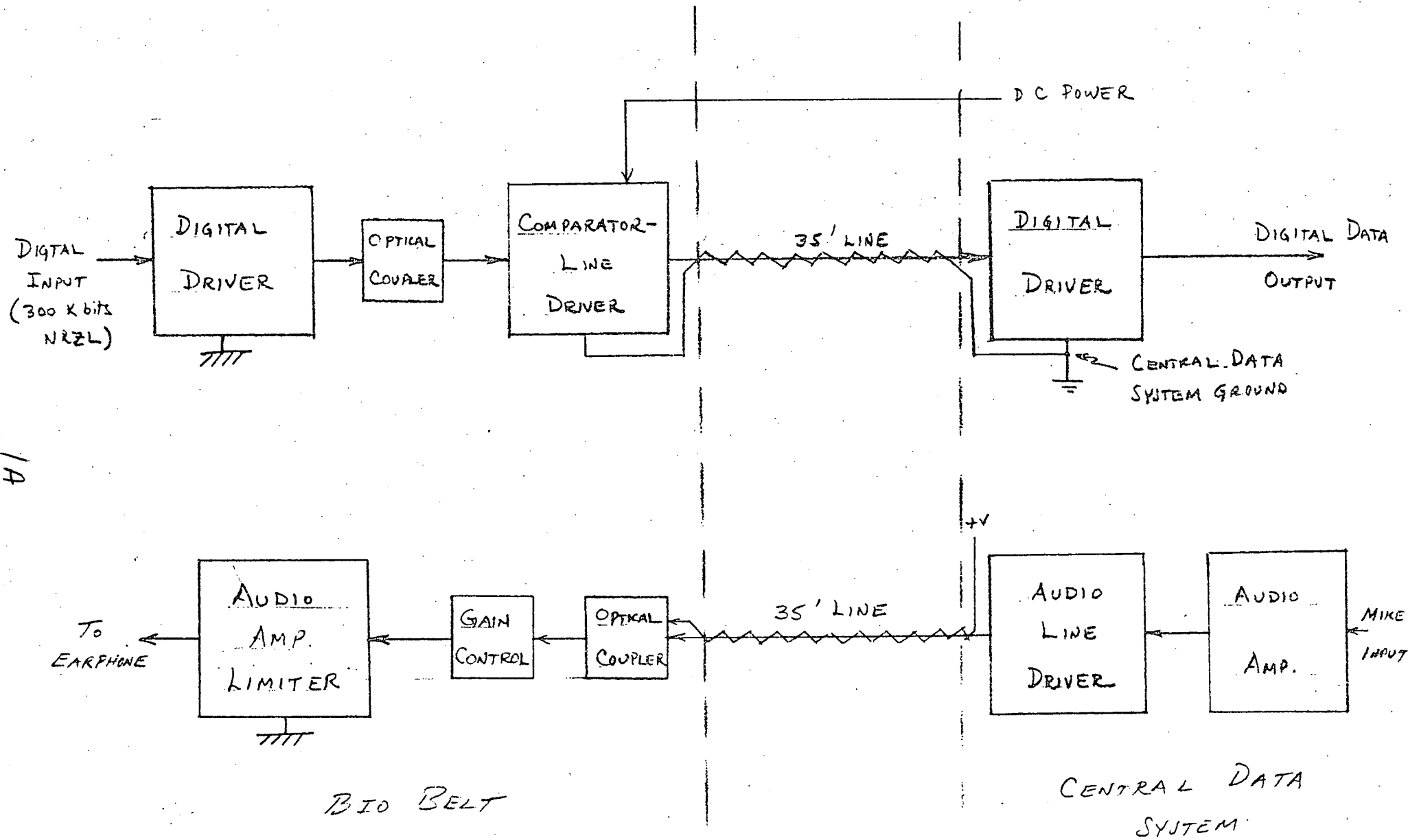
Three deliverable optical couplers have been fabricated, each consisting of an assembly representing the bio-belt isolating couplers and amplifiers, connected by means of 35 foot lines to another assembly of logic and audio circuits representing the central data system.

12.1 Optical Coupler Block Diagram

Figure 6-1 is a block diagram of the optical couplers.

A. Data Optical Coupler - The digital driver shown at the left side of the figure will accept TTL logic level inputs. A single driver is used to drive the Monsanto MCD-1 optical coupler at the data rate of 300 K bits per second. The coupler consists of a light emitting diode (LED) source and a photodiode detector.

In order to avoid noise problems, the output of the photo diode is amplified by a digital comparator circuit which is used as a twisted pair line driver. Power for the comparator circuit is from the central data system supply in order to keep grounds isolated. The digital driver at the central data system is a TTL driver and is capable of driving 7 TTL loads.



OPTICAL COUPLER BLOCK DIAGRAM

FIG 6-1

B. Audio Optical Coupler - On the lower right is shown the microphone audio amplifier which amplifies the output from the Pacific Plantronics Headset model MS 50-59 microphone.

The audio line driver provides an audio modulated current source to the LED located in the MCT-1 optical coupler at the end of the 35 foot line connected to the Bio Belt Assembly. The coupler also contains a phototransistor which detects and amplifies the linear light signal radiated by the LED.

The photo transistor is followed by a screw driver adjusted volume control which adjusts the input to the headset amplifier. The Audio Amplifier Limiter provides more than enough output to drive the Pacific Plantronics Headset model MS 50-59 earphone. Frequency response is down 3 db at approximately 3 cycles at the low end of the audio range and down 3 db at 5000 HZ at the high end. (Coupler and amplifier response)

12.2 Optical Coupler Schematic Diagram Description (Fig. 6-2)

A) Data Optical Coupler - Logic element A1 is a low to high voltage interface element which provides translation from standard TTL logic input levels of zero and + 3 volts to output logic levels of + 12 volts and zero volts respectively. When the output of A1 is at + 12 volts, the LED located in optical coupler A6 draws zero current and the dark leakage current of the photodiode detector, also located in A6, is approximately 15 nanoamps. When the output of A1 is at zero potential, the LED will conduct 25 ma of current and consequently light will be radiated to the photodiode causing a leakage current change of approximately 36 microamps. A corresponding change of voltage of approximately 170 millivolts appears at the positive input terminal of digital comparator A3. This change of voltage is sensed by the comparator and, with the help of voltage divider R10-R11, a positive output swing of approximately 4 volts is produced at the output of A3. This pulse is coupled over a 35 ft. twisted-pair line to the central data system logic element A4 which produces a positive pulse at its output compatible with TTL logic.

Resistors R22 and R12 and capacitor C17 are used as line matching elements to eliminate line reflections that occur when A3 produces a negative output swing as the LED is switched "off".

The digital data output signal will be essentially identical to the digital data input signal with exception to a 500 nanosecond delay. This delay can be minimized by lowering resistor values of R10 and R11 with a consequent increase in power dissipation or by adding a line driver circuit with an active pull-up output configuration.

B) Audio Optical Coupler - The input signal from the MS50-59 microphone is typically ± 1 millivolt peak. The input stage is an LM308 linear amplifier connected in a noninverting amplifier configuration with a closed loop gain of 57. Consequently the voltage swing at the output of A5 will be approximately ± 57 millivolt peak. This signal will modulate the augmented current source configuration consisting of transistors Q1 and Q2 and their associated passive components. The LED located in optical coupler A7 will have a bias current of 10 ma and a ± 44 microamp current variation will be produced in the diode due to the ± 57 millivolt signal applied to the base of the transistor Q2. This modulation current will be detected by the phototransistor also located in A7 and a consequent audio voltage swing of approximately ± 7 millivolts will be produced at the emitter of the phototransistor. If potentiometer R8 is in center position, an audio signal of ± 3.5 mv will appear at the positive input of A2. Linear amplifier A2 is connected in a noninverting amplifier configuration with a closed loop gain of 100. Consequently, the audio voltage swing at the output of A2 will be approximately ± 350 mv peak. If the MS50-59 earphone has a dynamic impedance of 600 ohms, the audio signal swing across the phone will be ± 290 mv peak. This is adequate signal drive for the MS50-59 earphone and consequently the audio vibrations at the mike have been faithfully reproduced at the earphone with a high impedance isolation of the bio-belt ground from the data system ground.

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Checked			TITLE			Model	
Approved			IMBLMS Optical Couplers (Parts List)			Report No.	
Symbol	Part No.	Description	Value	Tol.	Rating	Manufacturer	
R1, R22	RL075121G	Resistor	120 Ω	2%	$\frac{1}{4}$ W		
R2	RL205391G	"	390 Ω	2%	$\frac{1}{4}$ W		
R3, R6	RN55D4751F	"	4.75K	1%	$\frac{1}{4}$ W		
R4	RL075104G	"	100K	2%	$\frac{1}{4}$ W		
R5	RN55D8253F	"	825K	1%	$\frac{1}{4}$ W		
R7, R9, R19	RL075102G	"	1K	2%	$\frac{1}{4}$ W		
R8	2600P-103	Potentiometer	10K	10%	1W	Amphenol	
R10	RL075182G	Resistor	1.8K	2%	$\frac{1}{4}$ W		
R11	RL075751G	"	750 Ω	2%	$\frac{1}{4}$ W		
R12	RC07GF151J	"	150 Ω	5%	$\frac{1}{4}$ W		
R13	RC20GF361J	"	360 Ω	5%	$\frac{1}{4}$ W		
R14	RL075132G	"	1.3K	2%	$\frac{1}{4}$ W		
R15	RL205132G	"	1.3K	2%	$\frac{1}{4}$ W		
R16	RC07GF102J	"	1K	5%	$\frac{1}{4}$ W		
R17	RL075563G	"	56K	2%	$\frac{1}{4}$ W		
R18, R20	RN55D1003F	"	100K	1%	$\frac{1}{4}$ W		
R21	RL075202J	Resistor	2K	2%	$\frac{1}{4}$ W		
C1, C2, C3, C15 C16, C18, C19 C29	150D395X9050B2	Capacitor	3.9 μ f	10%	50V	Sprague	
C4, C6, C7, C8, C9 C11, C12, C13, C14 C17, C21, C23 C24	8121-050-651-154M	"	0.15 μ f	20%	50V	Erie	
C5	150D107X002052	"	100 μ f	20%	20V	Sprague	
C1, C25, C26	CY10C3R3C	"	3.3p f	± 0.25 p f	500V		
C14	150D276X9020R2	"	27 μ t	10%	20V	Sprague	
C17, C21	CY15C331J	"	330p f	5%	500V		
C27	8131-050-651-105M	Capacitor	1 μ t	20%	50V	Erie	
CR1	1N4448	Diode				Fairchild	
CR2	1N750A	Zener Diode	4.7V	5%	$\frac{1}{4}$ W	Motorola	
Q1	2N2907	Transistor				Motorola	
Q2	2N3947	Transistor				Motorola	
CR3, CR4	1N914	Diode				Fairchild	

12.3 Testing

The data channel from the bio-belt circuit to the central data system circuit was checked. This was accomplished by sending the frame sync code and checking that a bit is not lost by using the logic check circuit described in section 12.3.1. A block diagram of the test circuit is shown in Figure 6-3. Logic for the test circuit is shown in Figures 6-6 through 6-8. The audio circuit at the central data system to the bio belt circuit was checked as described in section 12.3.2.

12.3.1 Data Channel Test - Introduction

The logic accepts data from an optical coupling device and a clock signal from a bit synchronizer. The incoming data is checked for the main frame sync pattern. When that pattern is detected a light is turned on and a counter is started. The last state of the counter, which occurs at the same time as the sync detect, turns on another light if the sync pattern is not present.

12.3.1.1 Sync Detect (P1)

The incoming data is routed to an 18-bit shift register and its output (DA01-DA18) is compared to the expected main frame sync pattern: 110110010111001011. When a comparison is made DK10 goes high and sets the Sync-Detect flip-flop-S001(P3).

12.3.1.2 Modulo 1200 Counter (P2)

This counter runs off a 600 KHZ clock that originates from a bit synchronizer. It consists of 2 BCD counters (modulo 10) that increment in the standard pattern and a modulo 12 counter (Fig. 6-4). Count 9 (DC01) of the first BCD counter (C001, 2, 4, 8) acts as the clock for the second BCD counter (C011, 12, 14, 18) and count 9 of the latter (DC02) acts as the clock for the modulo 12 counter.

The input equations for the mod. 12 are:

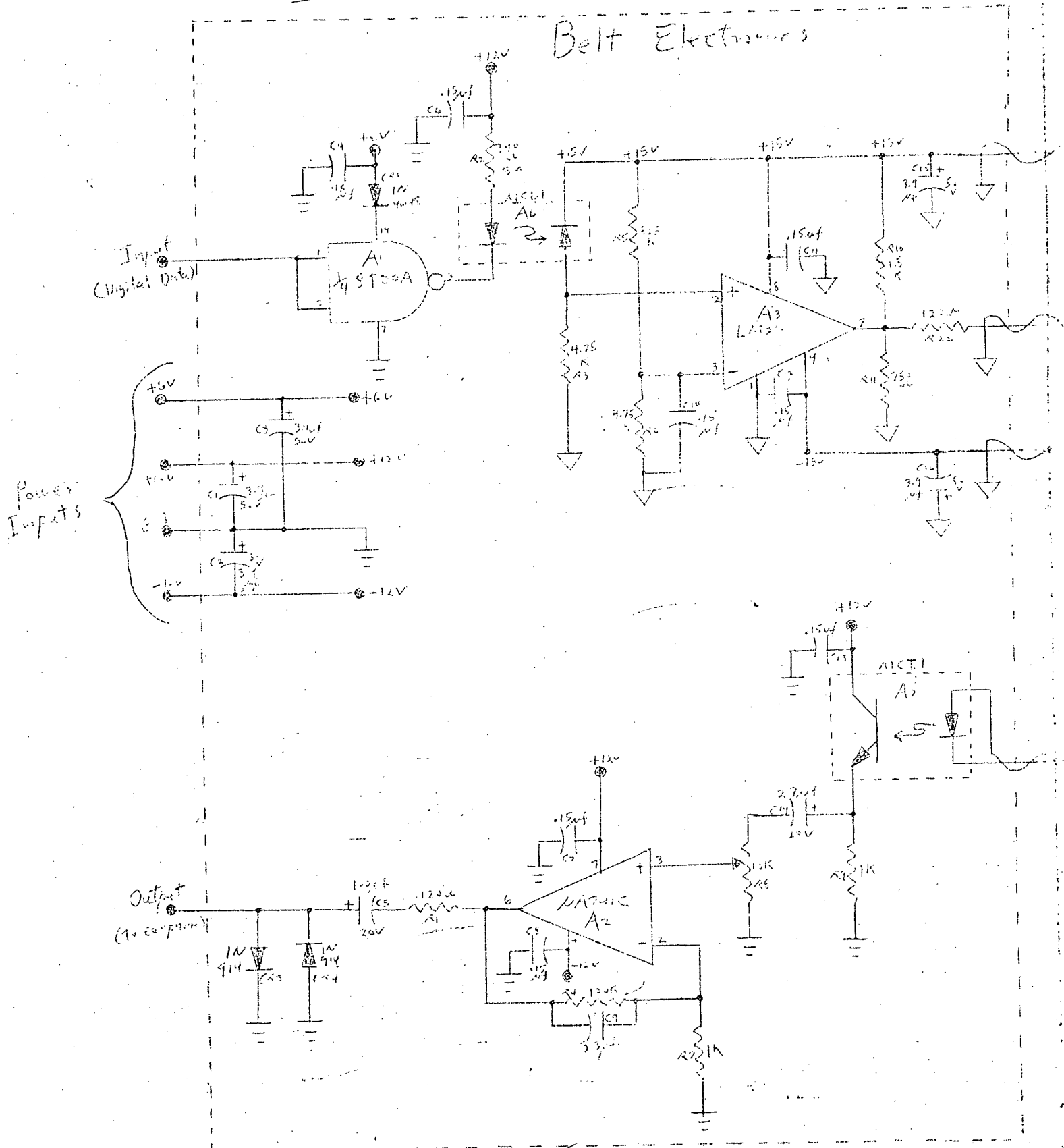
FOLDOUT FRAME

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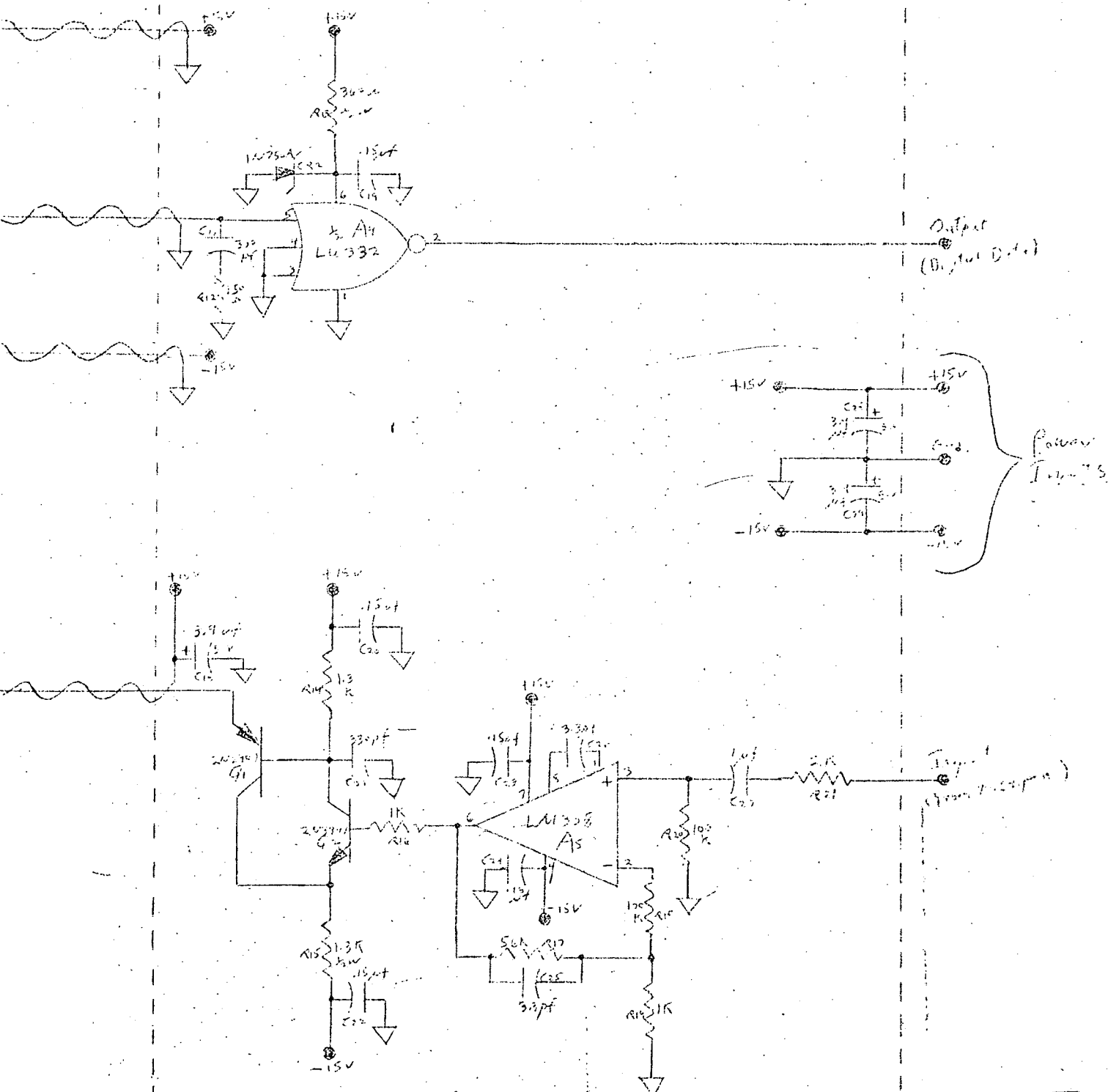
Optical

Belt Electronics



FOLDOUT FRAME 2

Central Data System Electronics

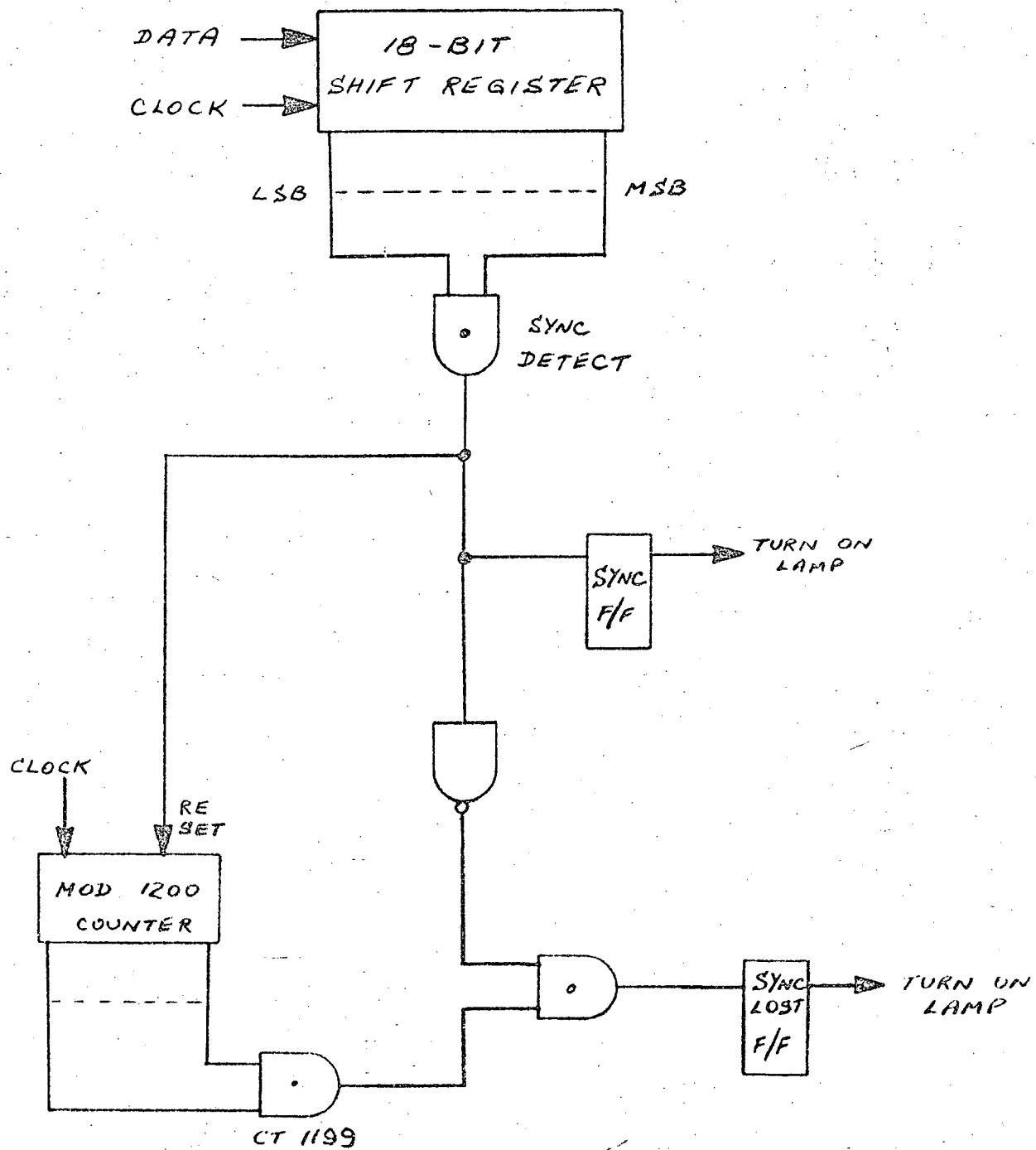


NOTE: $\frac{1}{2}$ BIO-BELT GROUND

$\downarrow$ CENTRAL DATA SYSTEM GROUND



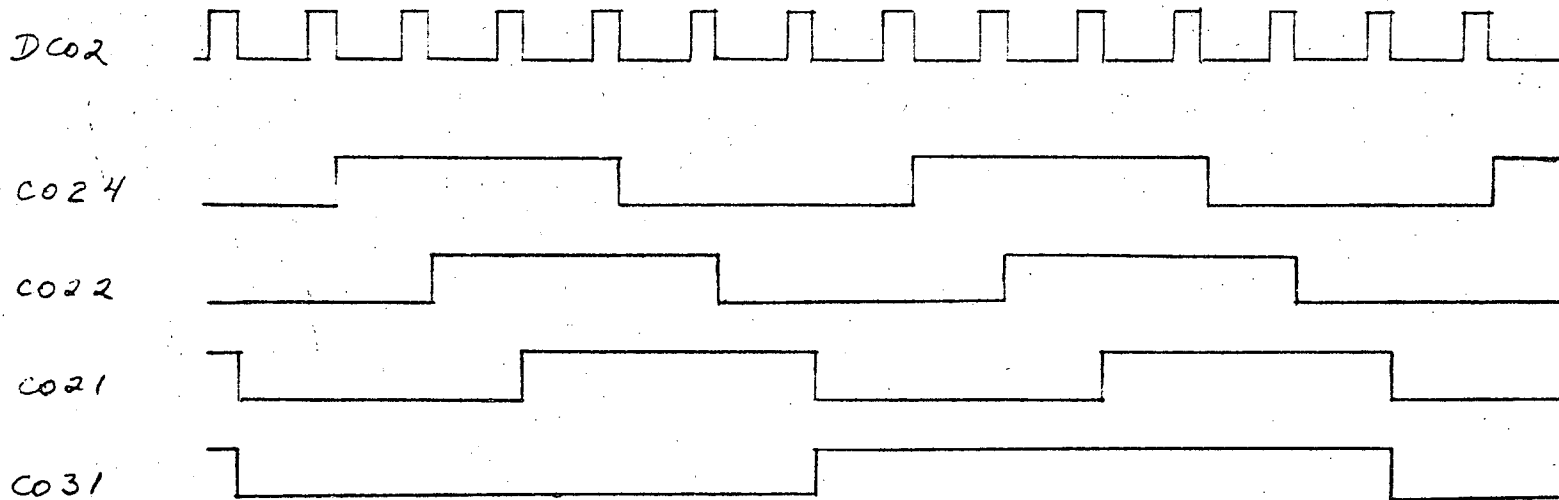
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OPTICAL-COUPLER DEMONSTRATION
BLOCK DIAGRAM

Fig 6-3

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MODULO 12 COUNTER

Fig. 6-4

```

jC024 = *C021
kC024 = C021
jC022 = C024
kC022 = *C024
jC021 = C022
kC021 = *C022
jC031 = "1"
kC031 = "1"
clock = DC02      for C024, C022, C021
        = DC02 · C021 · *C022 for C031

```

The last count of the modulo 1200 counter is decoded (DC04) and used to set the Sync-Lost flip-flop-N001 (P3) - only if no main frame sync is detected.

12.3.1.3 Sync Indicators (P3)

The timing for the two flip flops is indicated in Fig. 6-5 where the dotted lines for DC04 indicate that the signal would occur there if DK10 were not present.

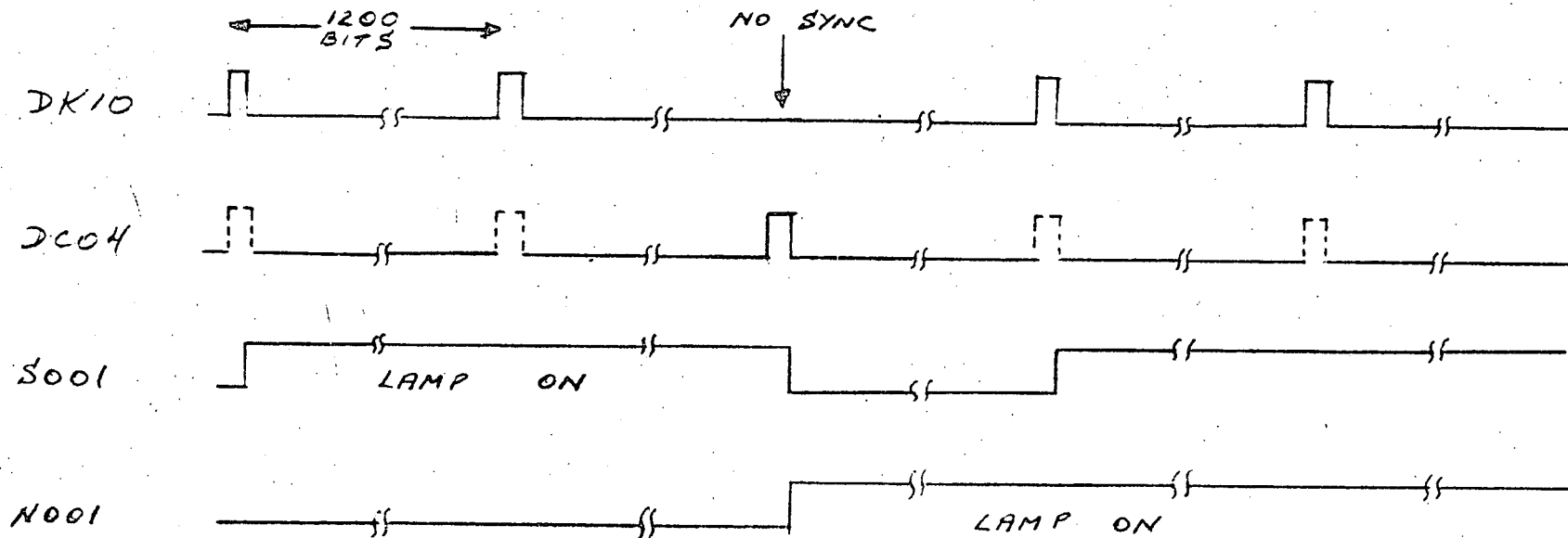
12.3.1.4 Master Reset (P3)

A pulse of 10 ms duration is generated when the power is first turned on. The signal resets all the flip-flops and ensures that counting starts from an all-zero state.

12.3.2 Audio Channel Test

An audio oscillator of ± 1 millivolts peak was fed into the microphone jack of the central data system circuit. Output of the bio-belt circuit headset jack was approximately ± 350 millivolts peak. Output was down 3 db at approximately 3 HZ at the lower end of the pass band and 3 db down at 5000 HZ at the high end.

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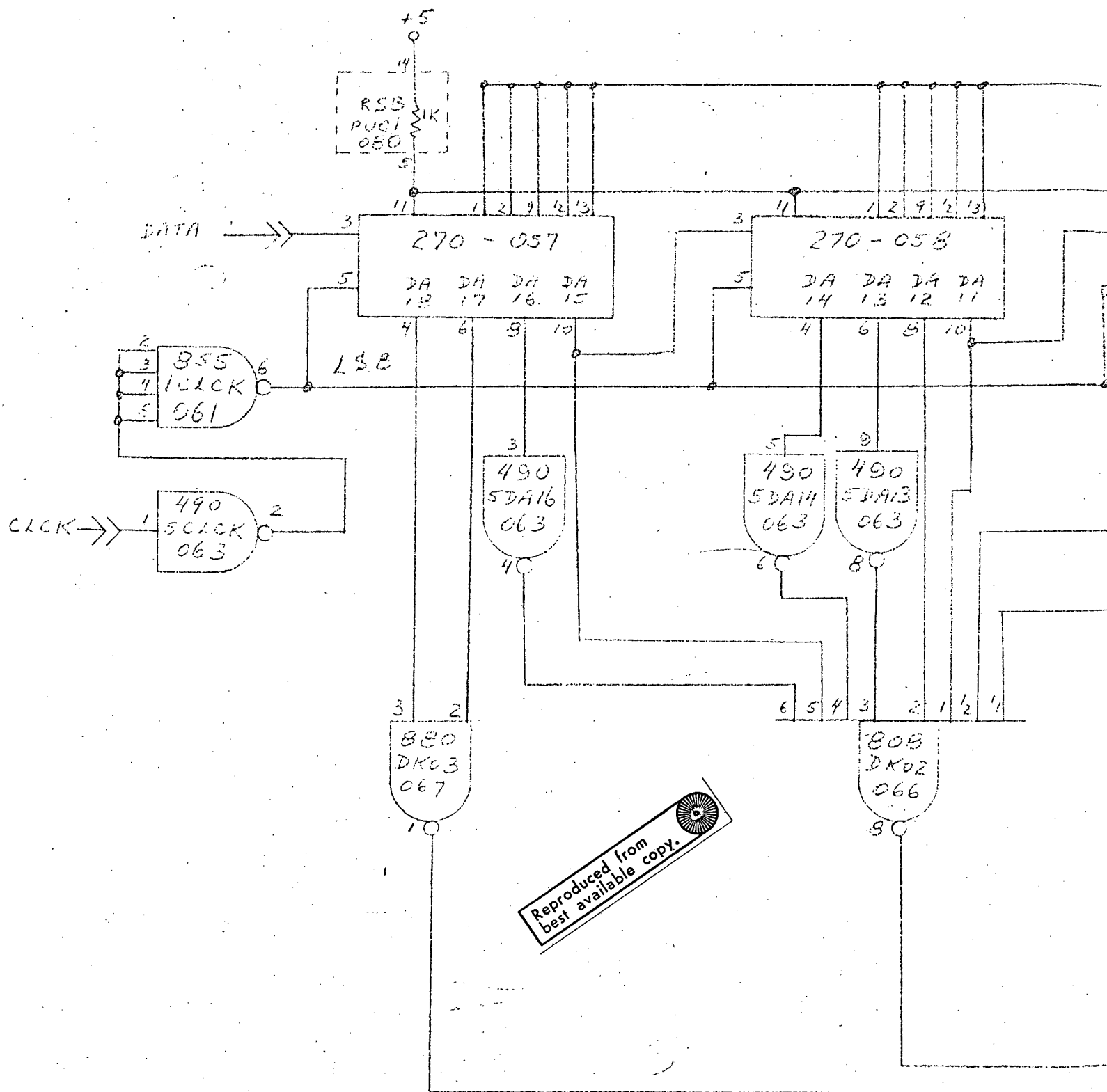


FLIP-FLOP LAMP TIMING

Fig. 6-5

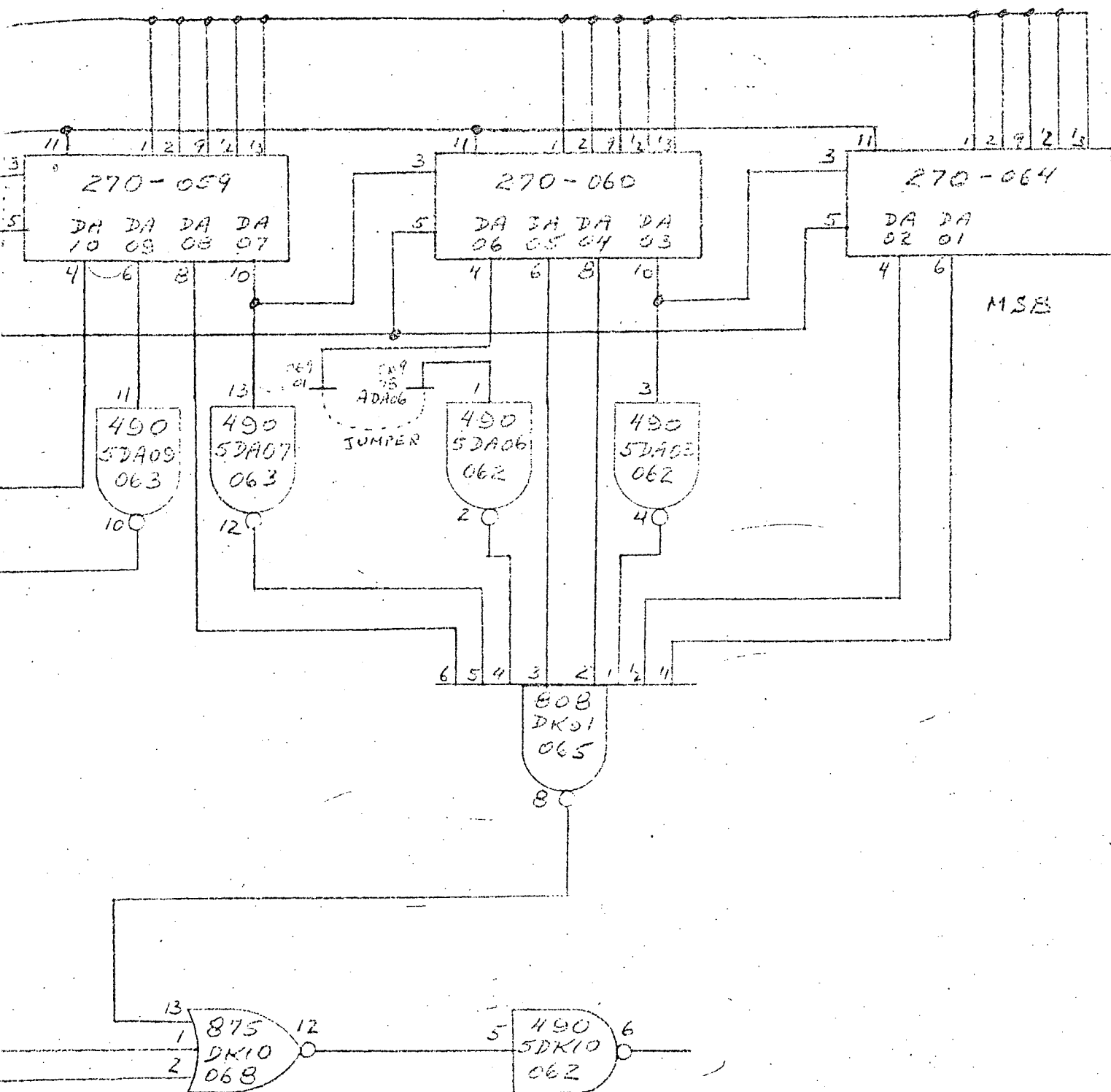
10

FOLDOUT FRAME I



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FOLDOUT FRAME 2



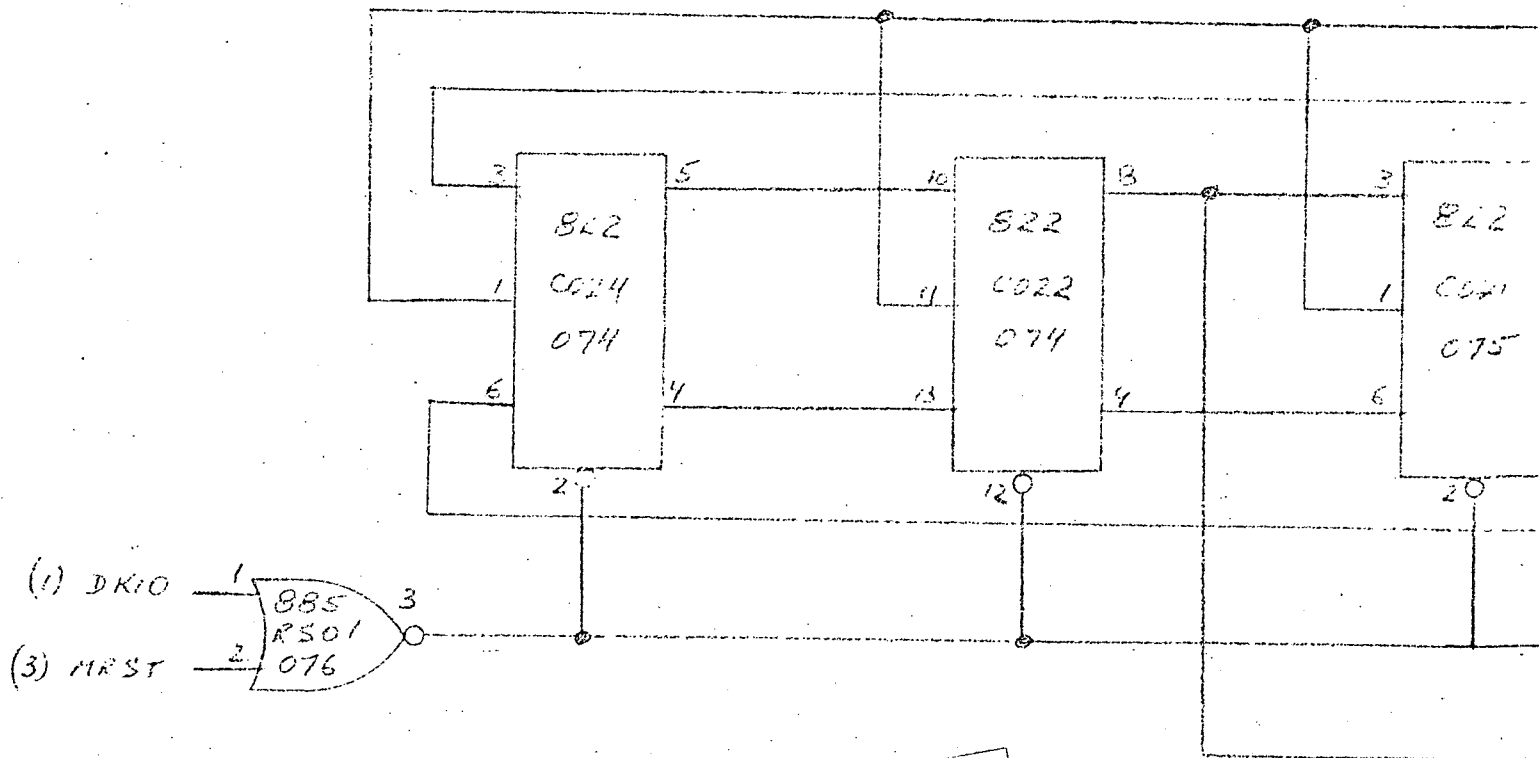
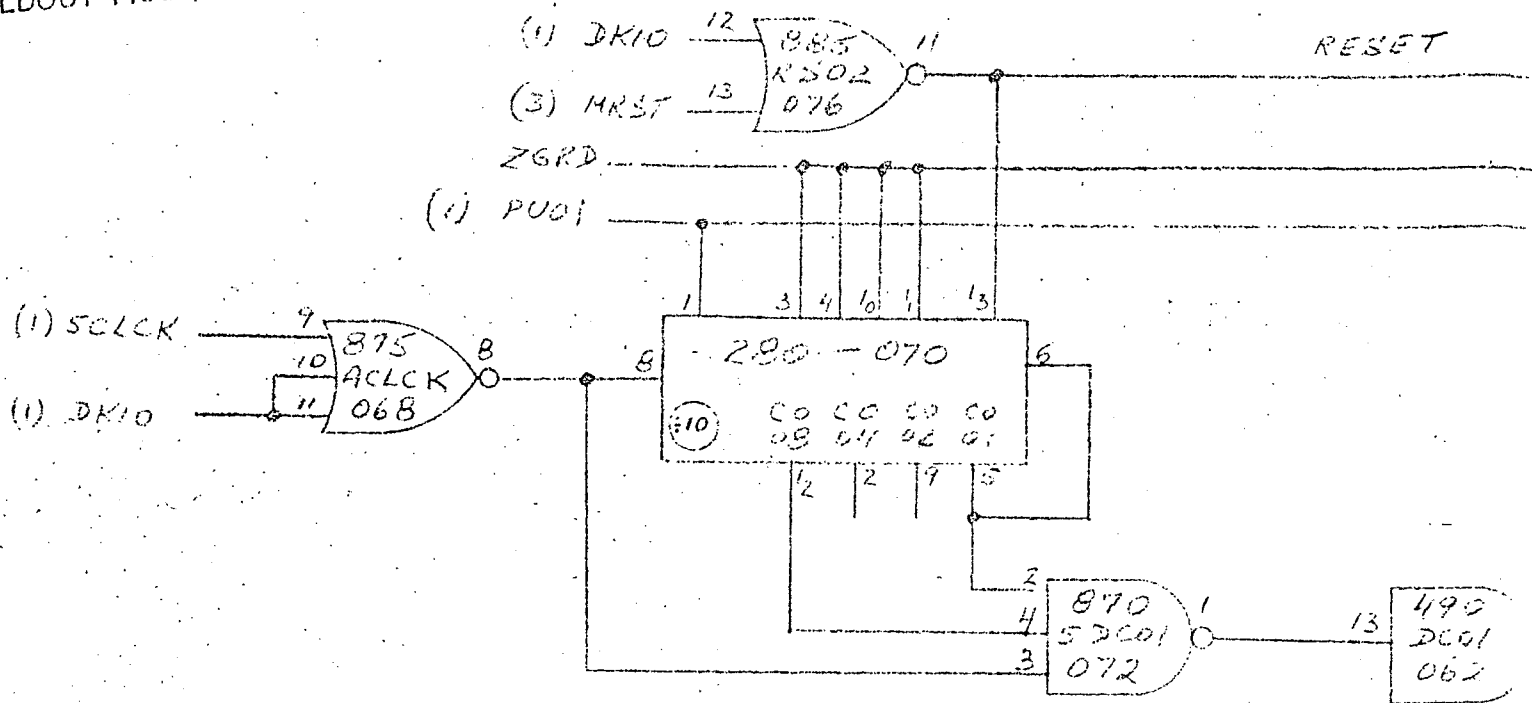
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12

18-BIT SHIFT REGISTER
SYNC DETECT - DK10

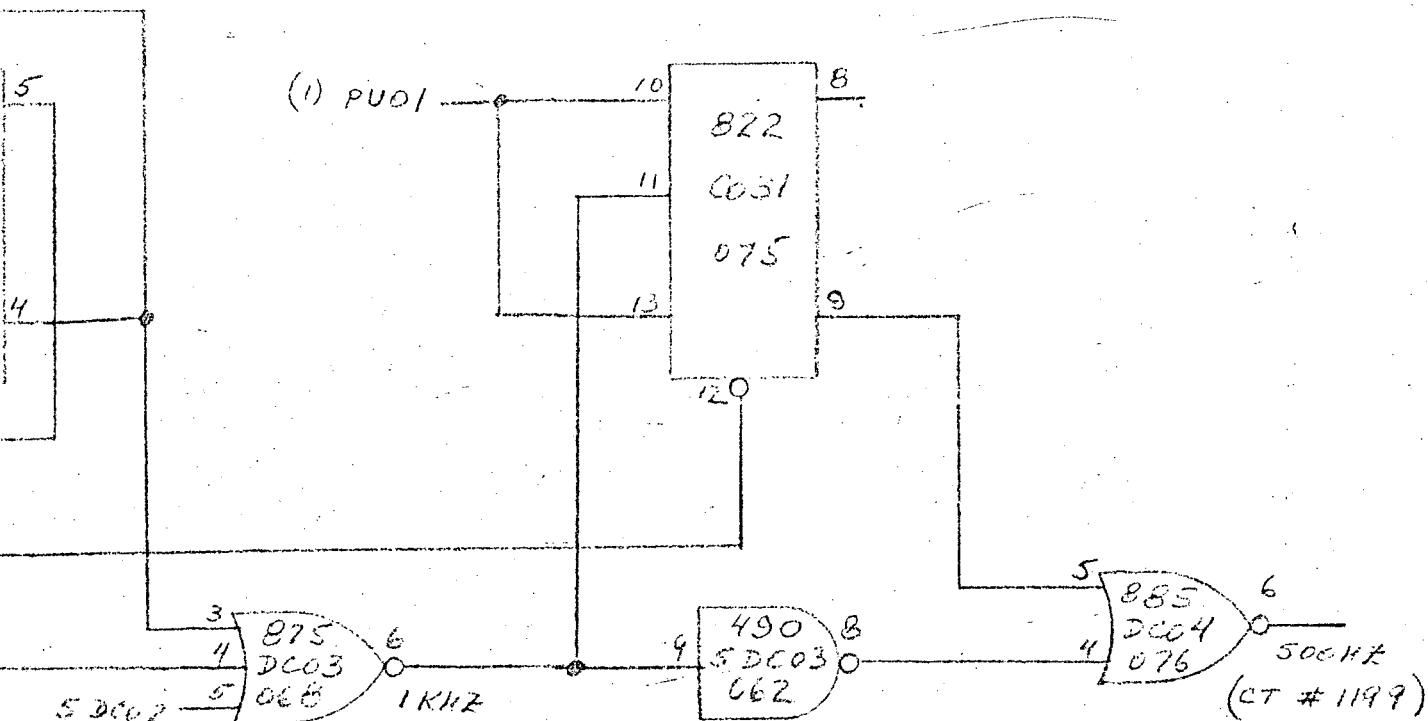
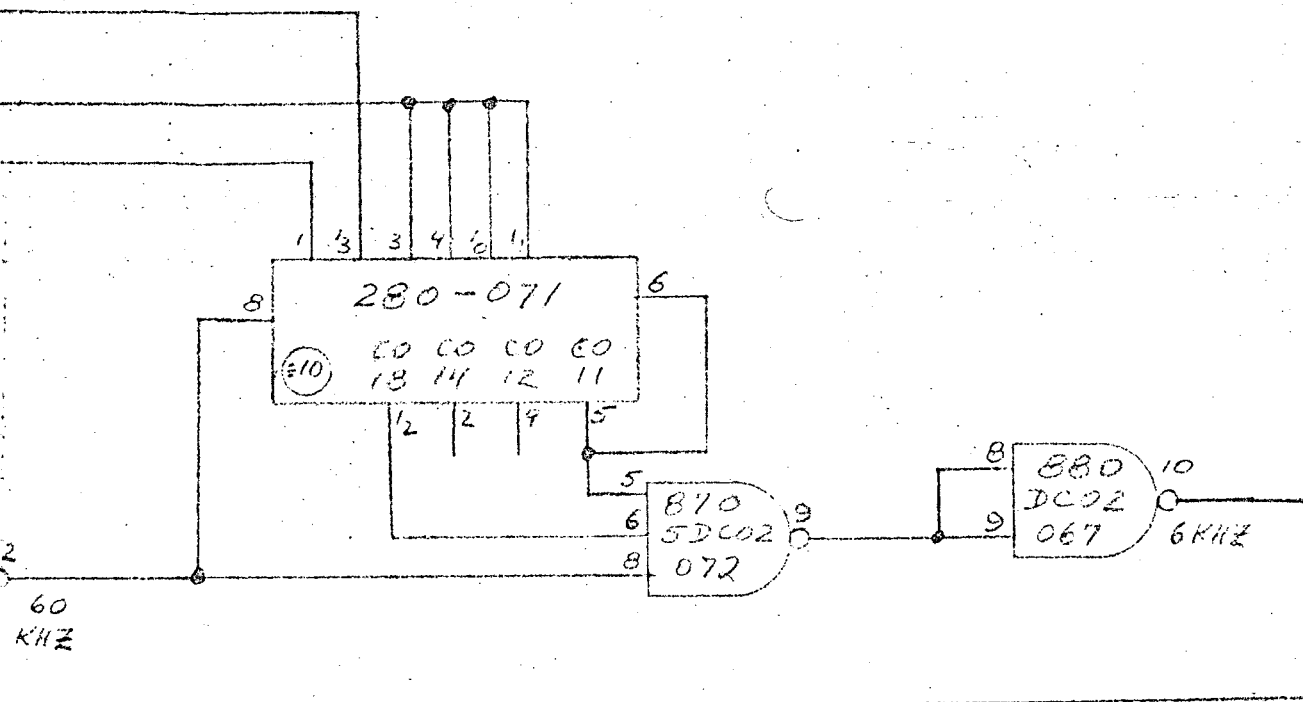
Fr 1-1

FOLDOUT FRAME 1



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FOLDOUT FRAME 2

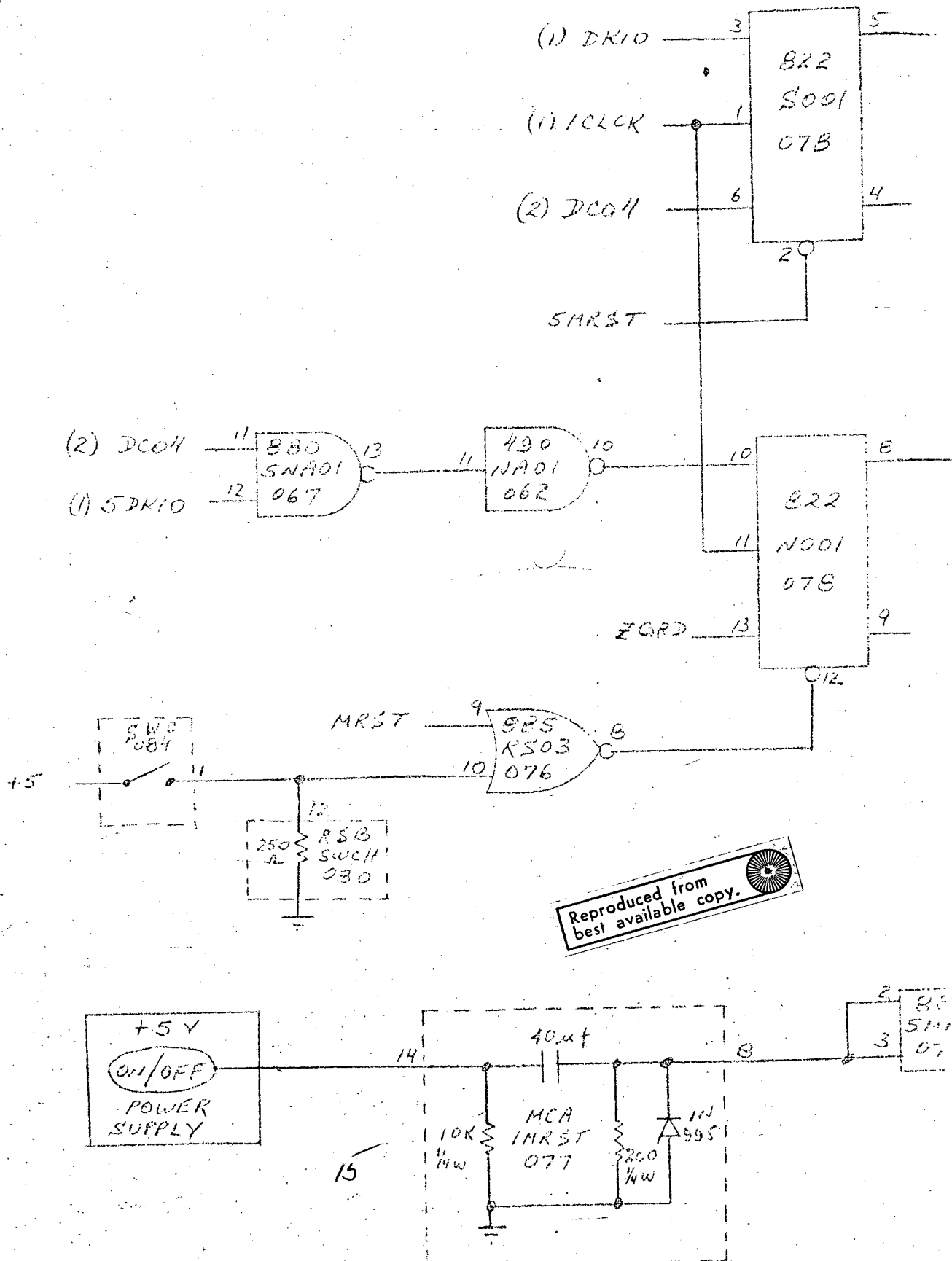


14

P2

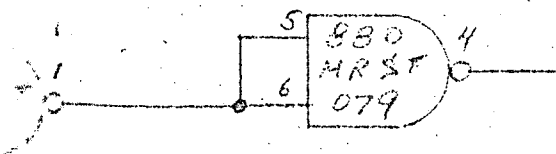
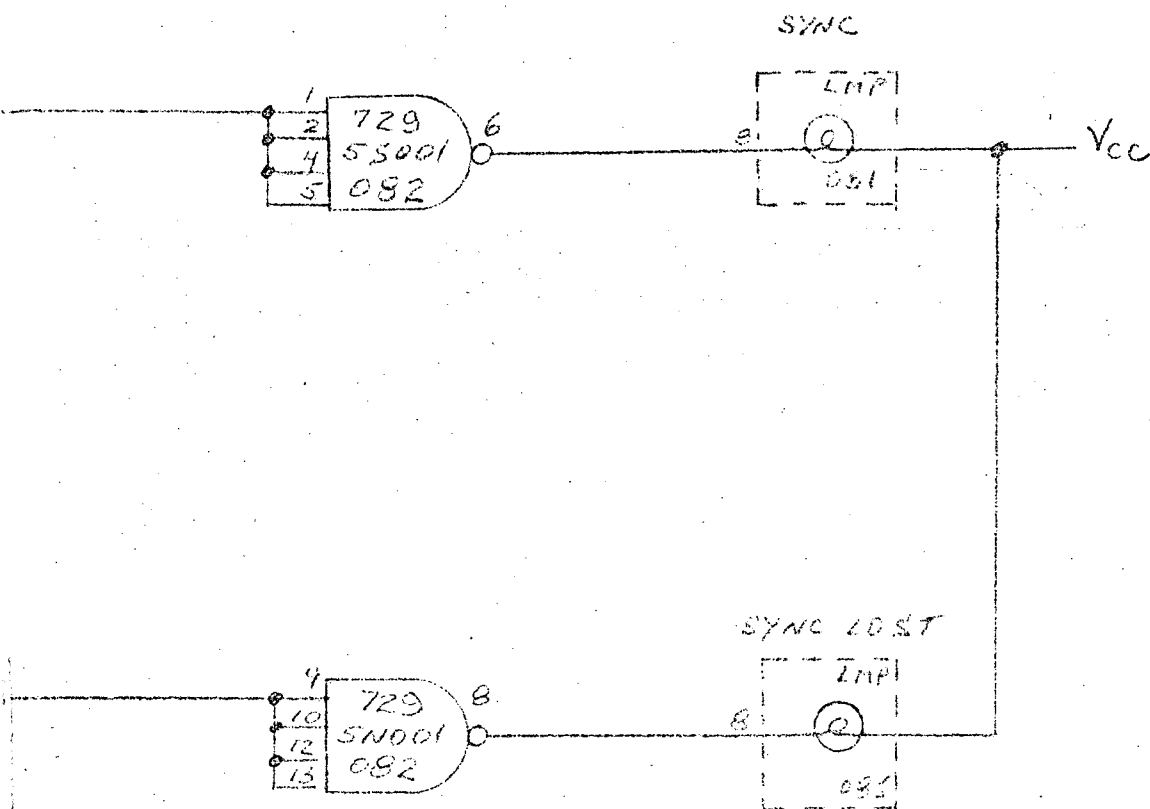
MODULO 1200 COUNTER

FOLDOUT FRAME 1



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FOLDBOOT FRAME 2



16

P3

SYNC-DETECT	FF	S001
SYNC-LOST	FF	N001
MASTER RESET		MRST

Fig. 6-B