Report No. 03-72-27

NASA CR-112099

DEVELOPMENT OF BEAM-LEADED LOW-POWER LOGIC CIRCUITS

Final Report

NASA Contract No. NAS1-10532

March 1972

By Bill Wiley Smith and Farris Malone

TEXAS INSTRUMENTS INCORPORATED
P.O. Box 5012
Dallas, Texas 75222

Langley Research Center
Hampton, Virginia 23365

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Report No. 03-72-27 NASA CR-112099

DEVELOPMENT OF BEAM-LEADED LOW-POWER LOGIC CIRCUITS

Final Report

NASA Contract No. NAS1-10532

By Bill Wiley Smith and Farris Malone

TEXAS INSTRUMENTS INCORPORATED
P.O. Box 5012
Dallas, Texas 75222

Langley Research Center
Hampton, Virginia 23365

NATIONAL AERONAUTICS AND SPACE ADMINISTRATION

Page Intentionally Left Blank

TABLE OF CONTENTS

Section	*Title*	*Page*
I.	SUMMARY	1
II.	INTRODUCTION	3
III.	DISCUSSION	7
	A. Processing	7
	B. Beam Lead Assembly	11
	1. Unmounted Bars	15
	2. Mounted Bars	15
	C. Circuit Descriptions	19
	1. Theory of Operation–BL54L67/BL54L68	22
	2. Resistor Process–1000 Ohm-cm/cm	23
IV.	TESTING AND EVALUATION	27
	A. Probe Test and Lot Qualification	27
	B. Device Characterization	29
V.	RESULTS	33

APPENDIX

BEAM LEAD CIRCUITS SCHEMATICS AND PHOTOGRAPHS 35

LIST OF ILLUSTRATIONS

Figure	*Title*	*Page*
1.	Cross Section of Beam Lead IC Bar	4
2.	Beam Lead Low Power TTL Process Flow	8
3.	Assembly Flow Diagram for Beam Lead Bars	12
4.	Assembly Flow Diagram for Unsealed Beam Lead Headers	13
5.	Beam Lead Transfer Fixture	14
6.	Packaging Method for Unmounted Bars	16
7.	DIP Headers for Beam-Leaded Bars	17
8.	Beam Lead Wobble Bonder	18
9.	CALX Wobble Bonder Collet	20
10.	Micro-Swiss Wobble Bonder Collet	21
11.	BL54L67/BL54L68 Logic Diagram	22
12.	BL54L67/BL54L68 Circuit Schematic	24
13.	Beam Lead Push-Off Tester	28
14.	Beam Lead Format 45	29
15.	Beam Lead Format 50	30
16.	Beam Lead Format 55	30
17.	Circuit Types BL54L00Y and BL74L00Y Schematic	37
18.	Circuit Types BL54L20Y and BL74L20Y Schematic	39
19.	Circuit Types BL54L30Y and BL74L30Y Schematic	41
20.	Circuit Types BL54L55Y and BL74L55Y Schematic	43
21.	Circuit Types BL54L67Y and BL74L67Y Schematic	45
22.	Circuit Types BL54L68Y and BL74L68Y Schematic	49
23.	BL54L00–Quad 2-Input NAND Gate	53
24.	BL54L20–Dual 4-Input NAND Gate	54
25.	BL54L30–Single 8-Input NAND Gate	55
26.	BL54L55–Two-Wide 4-Input AND-OR-INVERT	56
27.	BL54L67–J-K Flip-Flop	57
28.	BL54L68–Dual J-K Flip-Flop	58

LIST OF ABBREVIATIONS AND SYMBOLS

Å = angstroms

atm/cc = atmospheres per cubic centimeter

cm = centimeter

°C = degrees Centigrade

°K = degrees Kelvin

IC = integrated circuit

K ohms = kilo ohms

l/minute = liters per minute

54L = low power transistor transistor logic family

m = meter

μA = microamps

μm = micrometers (microns)

mA = milliamps

nsec = nanoseconds

N-Epi = N-type epitaxial layer

Ω-cm/cm = ohm centimeter per centimeter (ohms per square)

OR = oxide removal

ppm = parts per million

PtSi = platinum silicide

Si_3N_4 = silicon nitride

TiPt = titanium platinum

TTL = transistor transistor logic

V = volts

Development of Beam-Leaded Low-Power Logic Circuits

By Bill Wiley Smith and Farris Malone
Texas Instruments Incorporated

SECTION I
SUMMARY

The technologies of low power TTL and beam lead processing have been merged into a single product family. This family offers the power and thermal advantages of low power (54L), while providing the additional reliability advantages of beam leads. The reduction in the power and heat levels also allows the system designer to take advantage, through beam lead, multichip assemblies, of increased package density to reduce system size and weight.

Page Intentionally Left Blank

SECTION II
INTRODUCTION

The conservation of heat and power as well as the need for increased reliability have placed increasing restrictions upon the systems used in airborne and space applications. This need is not now satisfied by components available to the system users. Therefore, new technologies or combinations of existing technologies that might present a solution to the problem were sought.

The problems in heat and power can be solved by using currently available low-power TTL integrated circuits (54L). This family offers a power reduction, and hence a heat reduction, of an order of magnitude over standard power TTL. This decrease in heat, because of the reduced junction temperature of the operating circuits, also contributes to an increase in system reliability. It also allows the system to be contained in a smaller area without creating a system "hot spot" that would be difficult to cool. The decrease in power also eases the restrictions on resistance of package leads and system interconnects in that the system operates at a much lower current level in both signal and power leads. This reduction in power required also leads to a further system savings by allowing smaller, less costly power supplies to be used.

While the use of low-power TTL does lead to increased system reliability, further reliability increases are needed. This need was satisfied with the advent of beam-leaded devices. The beam lead process eliminates the major cause of integrated circuits component failure, wire bonds. It replaces the wire bond with a bar to package interconnect that is an integral part of the bar's metal system. This beam interconnect, shown in Figure 1, features an electroplated gold beam and an attach cross-sectional area larger than that of a wire bond. A second feature of the beam lead bar is silicon nitride passivated junctions. The silicon nitride acts as an effective block against sodium intrusion creating a hermetic bar. Protection against latent failures is inherent in two aspects of the beam lead process. Since the beam lead bar is not die bonded in the conventional bar attach manner, there does not exist the thermal coefficient factor that frequently causes bar cracking. The beam lead bar is attached to the package through malleable gold beams that absorb the expansion differential. The beam lead bar is separated by a chemical etch instead of by scribing and breaking as are conventional bars. This method of separation eliminates the stresses and cracks caused by scribing and breaking that contribute to bar breakage later in temperature cycling. Thus the reliability features of a beam lead bars are:

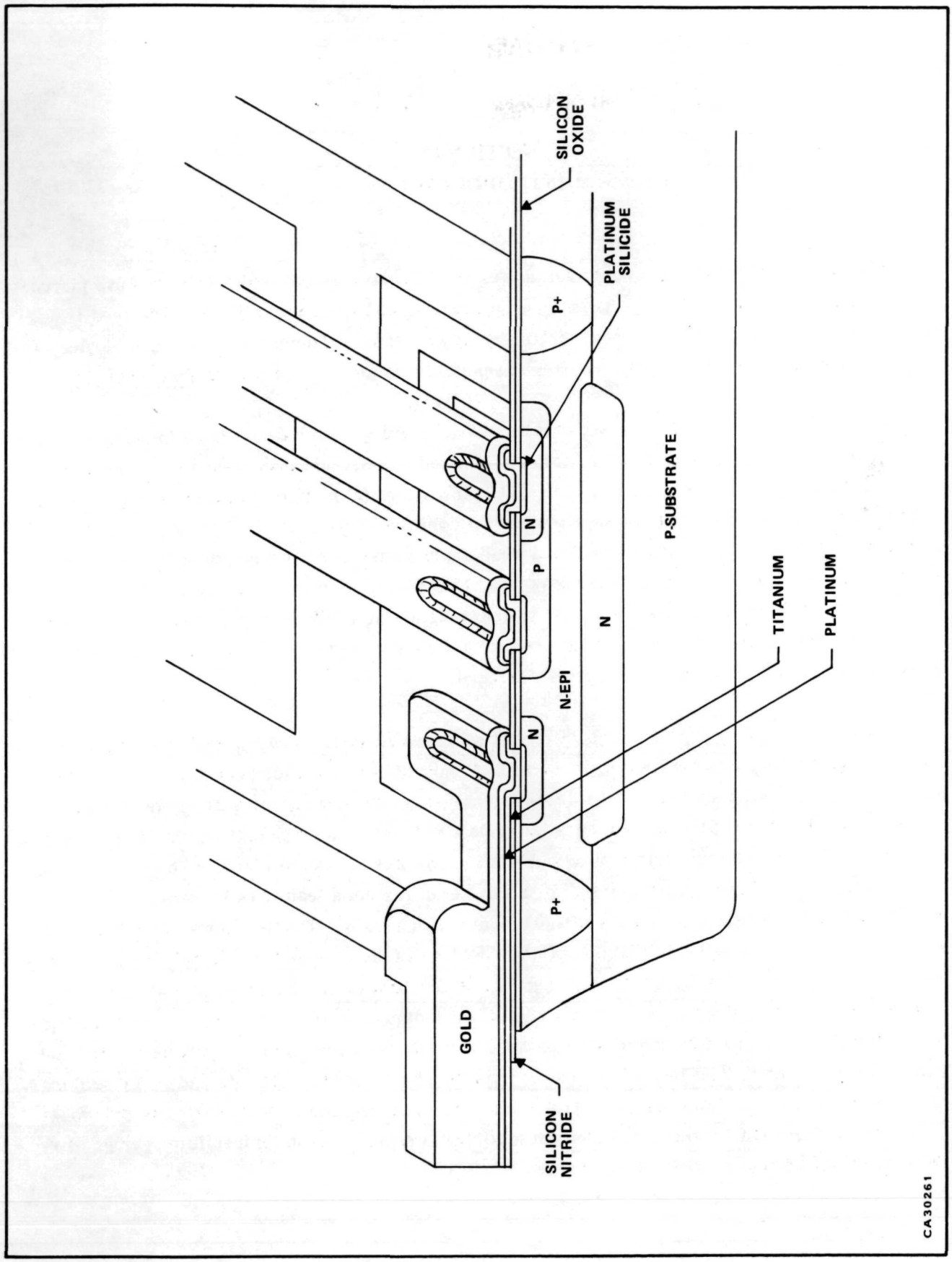


Figure 1. Cross Section of Beam Lead IC Bar

1) Integral bar to package interconnect

2) Silicon nitride junction passivation

3) No high temperature die bond

4) Chemical etch bar separation

The complete solution to the existing problem was not found as a product, thus it was desirable to integrate these two technologies, low-power TTL and beam lead processing, to form a single product family.

Page Intentionally Left Blank

SECTION III
DISCUSSION

A. PROCESSING

The object of applying beam lead processing to the low-power TTL (54L) line has been achieved. The two technologies needed for this program existed as separate operations, but some unknowns needed to be overcome in combining beam leads and low-power TTL into a single product family. In general, a modified 54L diffusion process and the Western Electric[1] beam lead process were used. The standard 54L process had to be modified due to the addition of silicon nitride.

The final beam lead low-power process is presented with a discussion concerning areas that differ from the standard low-power process. Figure 2 is a representation of the process.

The initial steps are identical to the standard 54L process. The process begins with buried layer wafers.

1. Oxidation
2. Isolation Diffusion
3. Base Diffusion
4. Emitter Diffusion

   All high temperature processing is completed at this point on standard parts. On the beam lead parts, however, the silicon nitride film has yet to be deposited. Since the nitride deposition temperature is high enough (1123°K) to reduce the gold concentration used for lifetime control, the gold on the beam lead parts is added after the silicon nitride has been deposited, rather than before or during emitter diffusion, as is common with conventional circuits.

---

1. Hause, S. S. and Whitner, R. A., "Manufacturing Beam-Lead Sealed-Junction Monolithic Integrated Circuits," *Western Electric Engineer* (December 1967), p. 3.

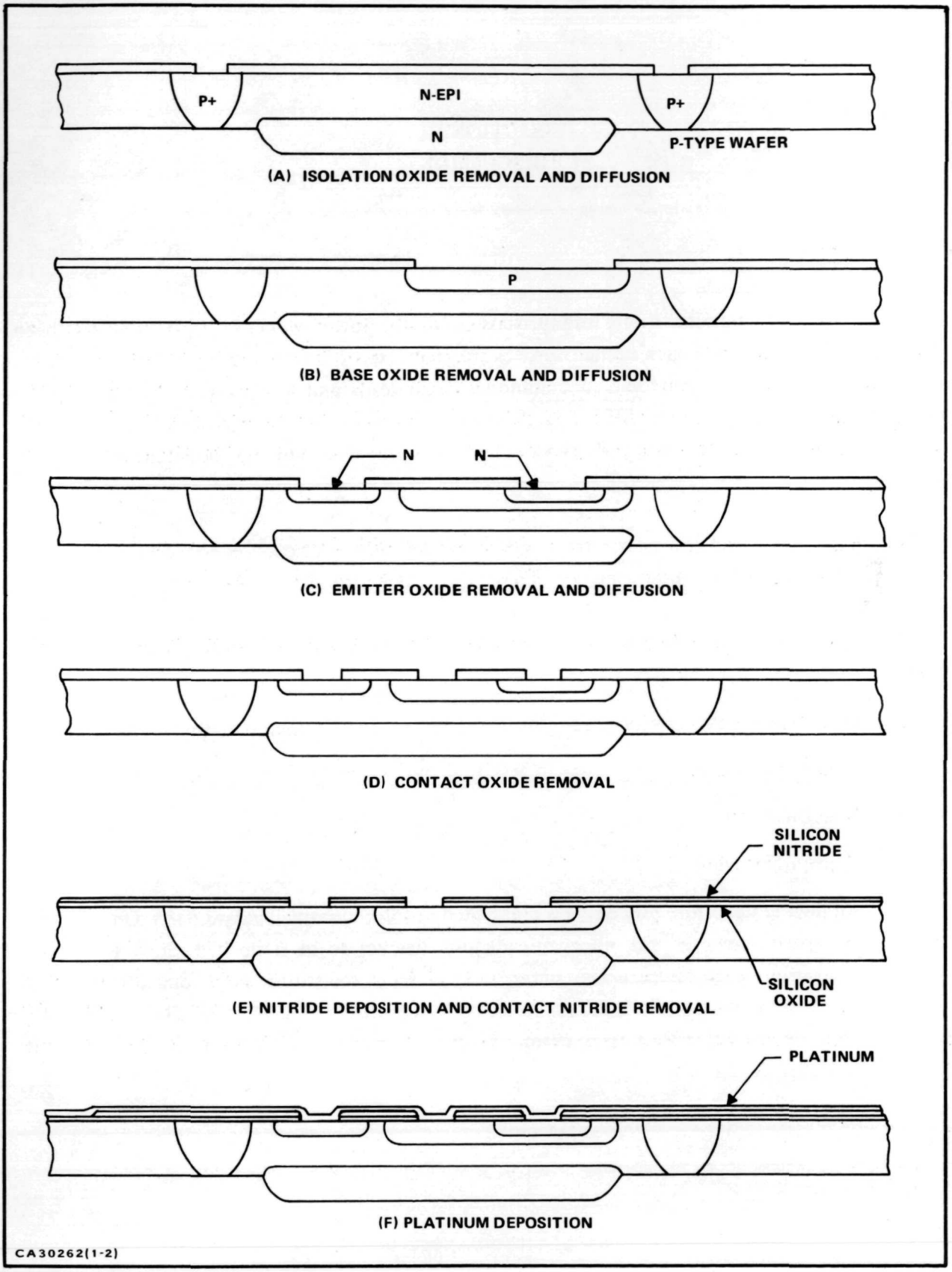


Figure 2. Beam Lead Low Power TTL Process Flow (Sheet 1 of 2)

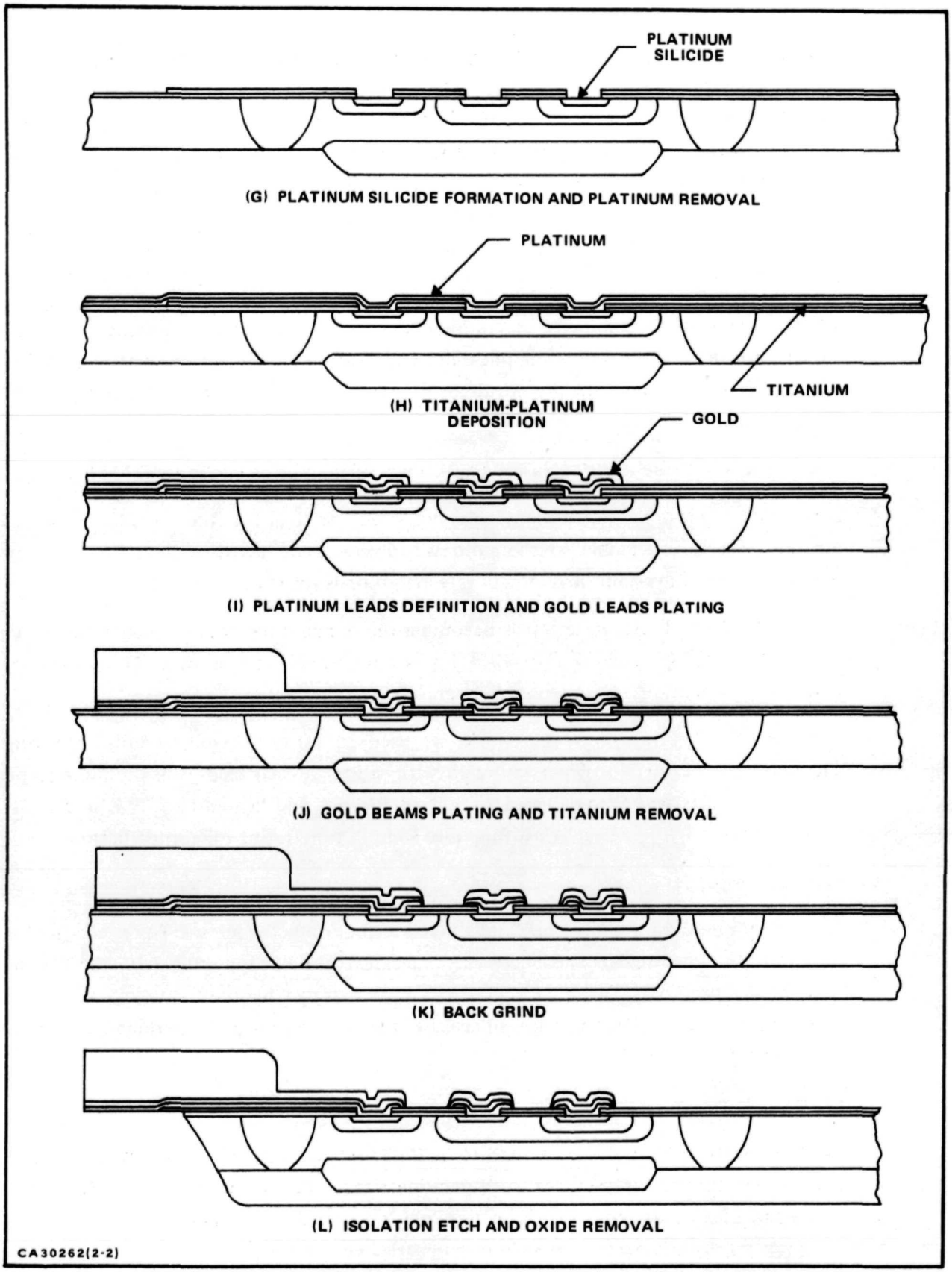


Figure 2. Beam Lead Low Power TTL Process Flow (Sheet 2 of 2)

5. Nitride Film

Silicon nitride is deposited to a thickness of 10^{-7} meters by pyrolytic decomposition of ammonia (NH_3) and silane (SiH_4) at 1123°K. The nitride is not deposited directly onto the silicon surface but a layer (3×10^{-8} meters) of thermal oxide is grown first to serve as a barrier and to prevent an unstable surface condition. The temperature of 1120°K was chosen because previous work has shown that at that temperature and below, amorphous films are formed. It was further shown that an amorphous film forms a better barrier to sodium diffusion than do those deposited as higher temperatures which tend to have larger crystallites.

Contact openings and paths for separation etch must be cut through the nitride film. The silicon nitride is etched in boiling phosphoric acid at 432°K using a mask of photoresist. The oxide that was beneath the nitride in the contact openings is etched in buffered HF using the Si_3N_4 film as a mask.

The checks which are made to ensure consistency of the nitride layers are listed below.

Deposition Conditions. For a silane/ammonia ratio less than 0.1, the film characteristics are more easily repeatable so the ratio was always kept less than that. Further, any deviations from the established growth rate are grounds for rejecting the slice.

Etch Rate. The HF etch rate test is becoming the standard test for acceptable nitride. In using this test, the etch rate of each lot is determined from a pilot. The maximum permissible rate of 49% HF at room temperature is 300 Å/min.

Blocking Tests. Temperature bias tests are used to verify the ion (sodium) blocking capability of the nitride. Water saturated with salt is allowed to dry on the units to be tested. They are then reverse biased to 80% of BV_{CBO} and heated to 575°K under H_2. Any increase in I_{CBO} is usually attributed to sodium penetrating the nitride barrier.

6. Gold Diffusion

Gold is evaporated onto the slices and alloyed in the contact windows. The excess gold is removed by aqua regia. The slices are then diffused at approximately 1350°K to redistribute the gold. The choice of 1350°K is dictated by the requirement to have enough gold in the collector region adjacent to the base to provide the required minimum offset voltage of 60 mV.

7. Gold Leads

Gold is plated over the entire slice to a thickness of 1-2 μm. Lea-Ronal Aurall 292 gold-plating solution is used for this operation (leads) and for beams as well. Leads are formed by chemically removing the excess gold in a cyanide etch using resist as a mask.

8. Beams

Gold beams are plated through a resist pattern to a thickness of 11-17 μm. The beam hardness is important in bonding and must be constantly monitored. Knoop numbers of 60-90 are typical when measured with the Leitz Mini-Load hardness tester using a 5-gm load.

9. Mount and Grind

The metallized slices are mounted metal side down onto a polished sapphire disc and secured by wax and ground to a nominal thickness of 5.7×10^{-3} cm.

Photoresist is then applied to the ground side of the wafer and a separation etch pattern is aligned to the diffusion using an infrared alignment technique. The slices are then etched until the individual bars are separated. Care is taken to etch enough to expose the nitride lip protecting the beams and yet not overetch to such an extent as to expose the beam anchor area.

10. Probe

The wafers are 100% probed from the back while they are still mounted on the sapphire disc. The program used tests the bars to all dc parameters and a full functional series. This is similar to the final test procedures used on conventionally packaged parts (see Section IV). The tighter screen is used because most parts will be used without being mounted in a single chip header.

B. BEAM LEAD ASSEMBLY

The assembly is broken into two parts because of the need to have both mounted and unmounted bars as final products (Figures 3 and 4). The basic flow, until the bond operation, is the same for both bars and mounted parts.

After the 100% probe test, the bars are in a separated form but still mounted in wax to a sapphire disc. The wafers are mounted into a transfer fixture (Figure 5) during the removal of the wax to prevent dislocation of the bars. The wax is dissolved using boiling trichlorethylene. The slice is then removed from the transfer fixture and subjected to a 40X backside inspection. The good bars are removed to another transfer fixture and turned for a 100X frontside inspection. The good bars are now loaded into chip trays for either shipment or for transfer into the bonding operation.

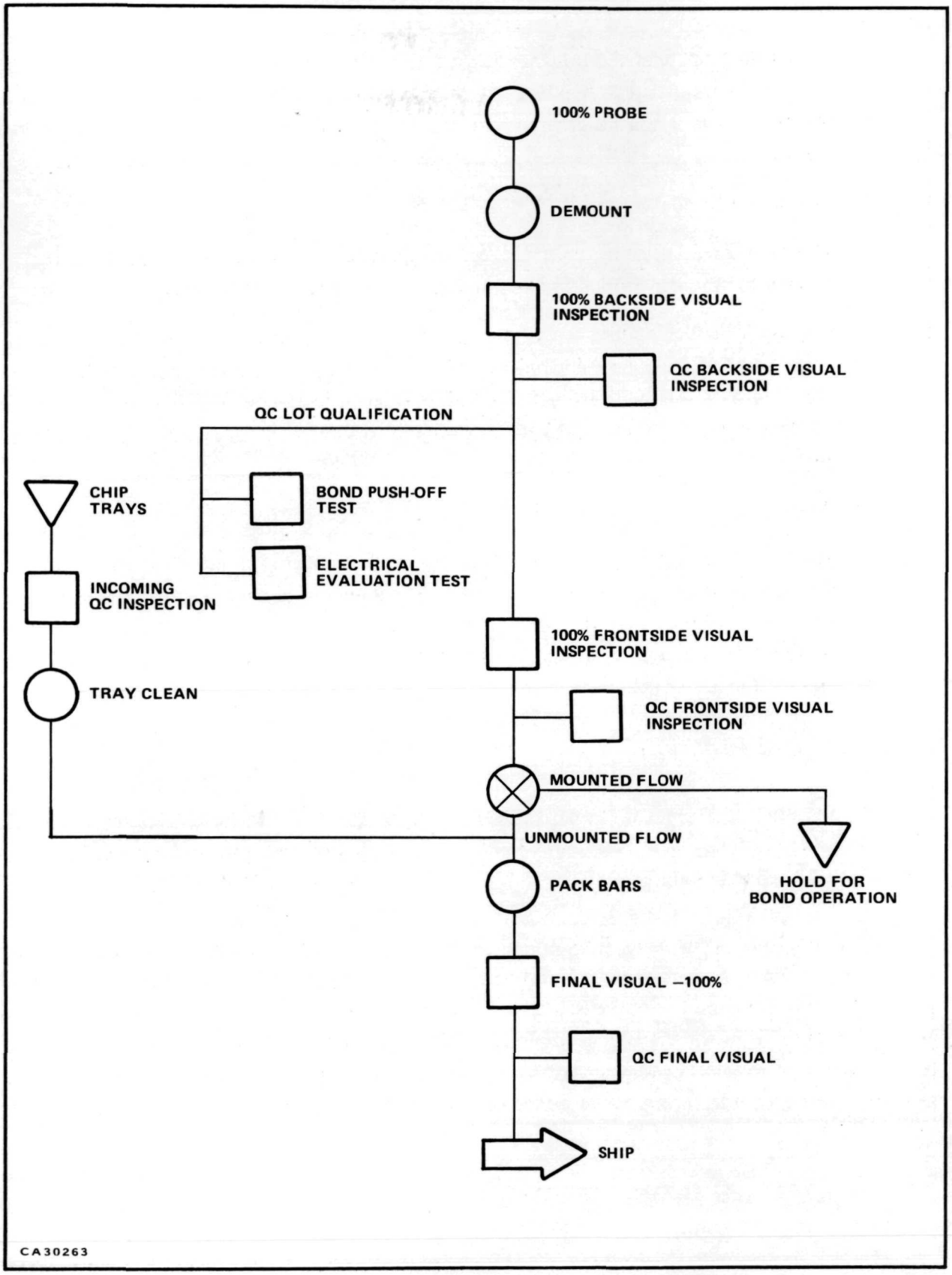


Figure 3. Assembly Flow Diagram for Beam Lead Bars

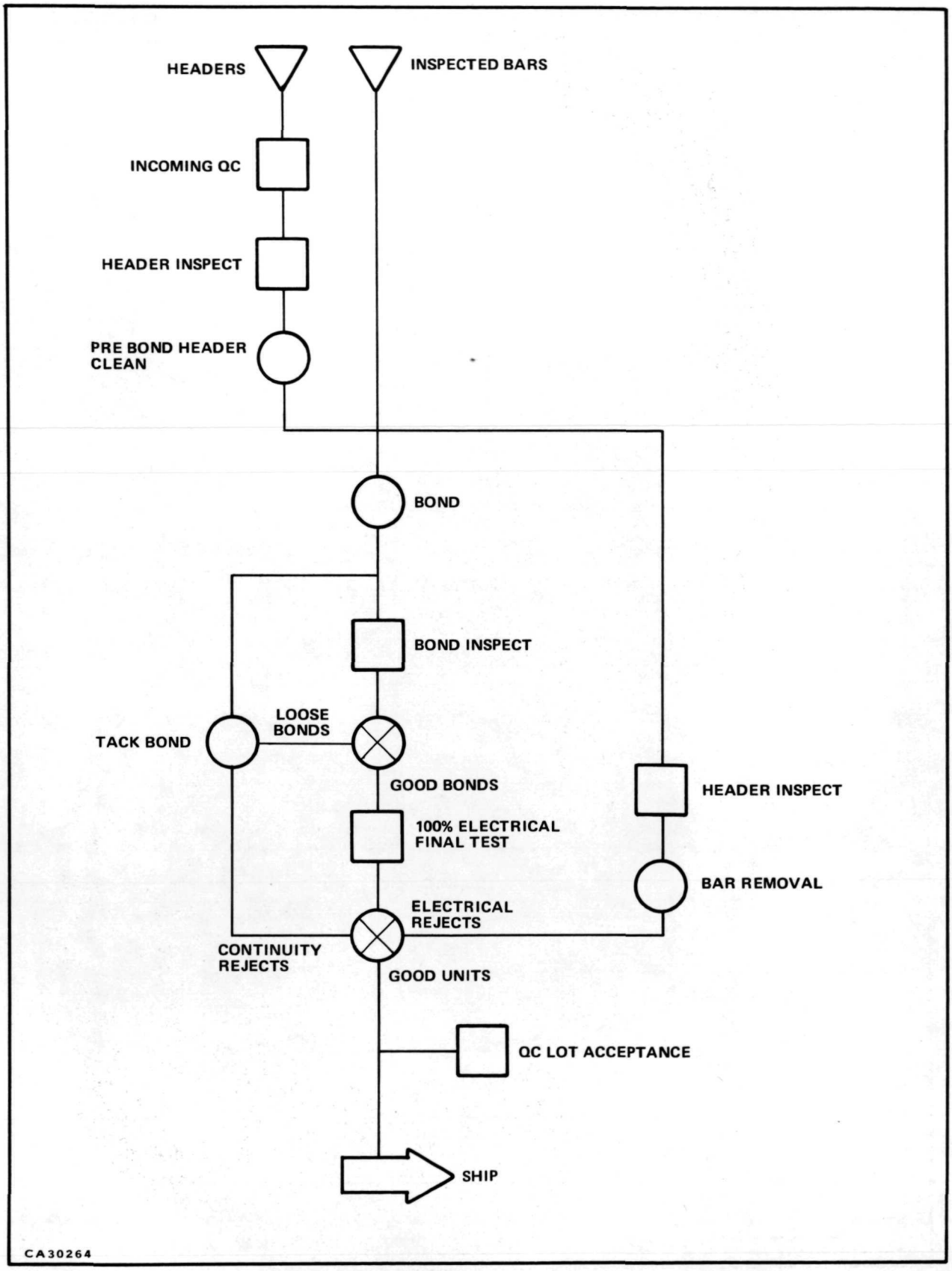


Figure 4. Assembly Flow Diagram for Unsealed Beam Lead Headers

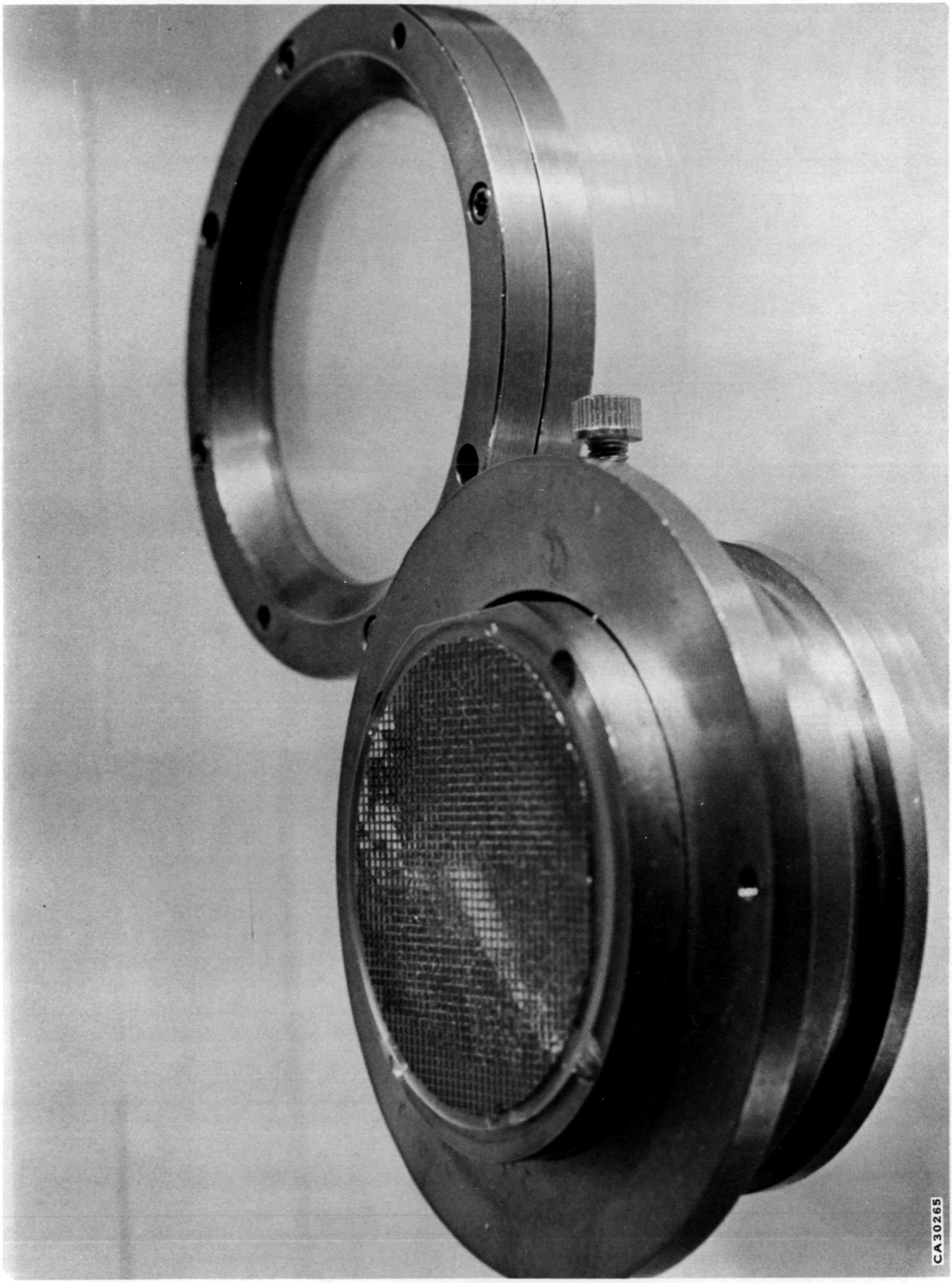


Figure 5. Beam Lead Transfer Fixture

1. Unmounted Bars

The bars are loaded into 2 X 2-inch plastic chip trays after the trays have been cleaned with alcohol. The part number and manufacturer for these trays is listed in Table I.

After a 20X final inspection, the tray is covered by a sheet of lint-free paper and a second tray placed as a lid on top of the first tray as shown in Figure 6. The sandwich is then placed into a clear plastic compact and the compact sealed for shipment.

Table I. Chip Tray Descriptions

Manufacturer	Pocket size inches	No. of pockets	Manufacturers Part no.	Color
Flouroware, Inc.	0.130 X 0.130	100	420-130	Brown
All-Plastics Molding	0.125 X 0.125	121	70-1072-004	Yellow

2. Mounted Bars

Nonlidded headers were used to mount the beam-leaded bars for evaluation. This was done to simplify the development effort and keep the bars exposed during evaluation for study. The headers shown in Figure 7 are constructed of alumina with a gold-plated molymanganese metal system. The leads are brazed to the gold-plated molymanganese. A screened metal package was discarded early in the program due to an unevenness of the beam attach pads. Photo-etching the metal resulted in a bar attach area of sufficient planarity to allow a complete bond. The bonding is done by a Kulicke and Soffa Industries, Inc. wobble bonder. This type of bonder (Figure 8) requires that the bar attach area be extremely coplanar. The requirement was not a problem in this program after the change was made to a photo-etched header.

The wobble bonder collet sizes used to bond the various part types are shown in Table II. The collets of two different manufacturers (Figures 9 and 10) were used on this program. The Calx, Inc. collet is preferred because of its cost advantage and its one-piece construction.

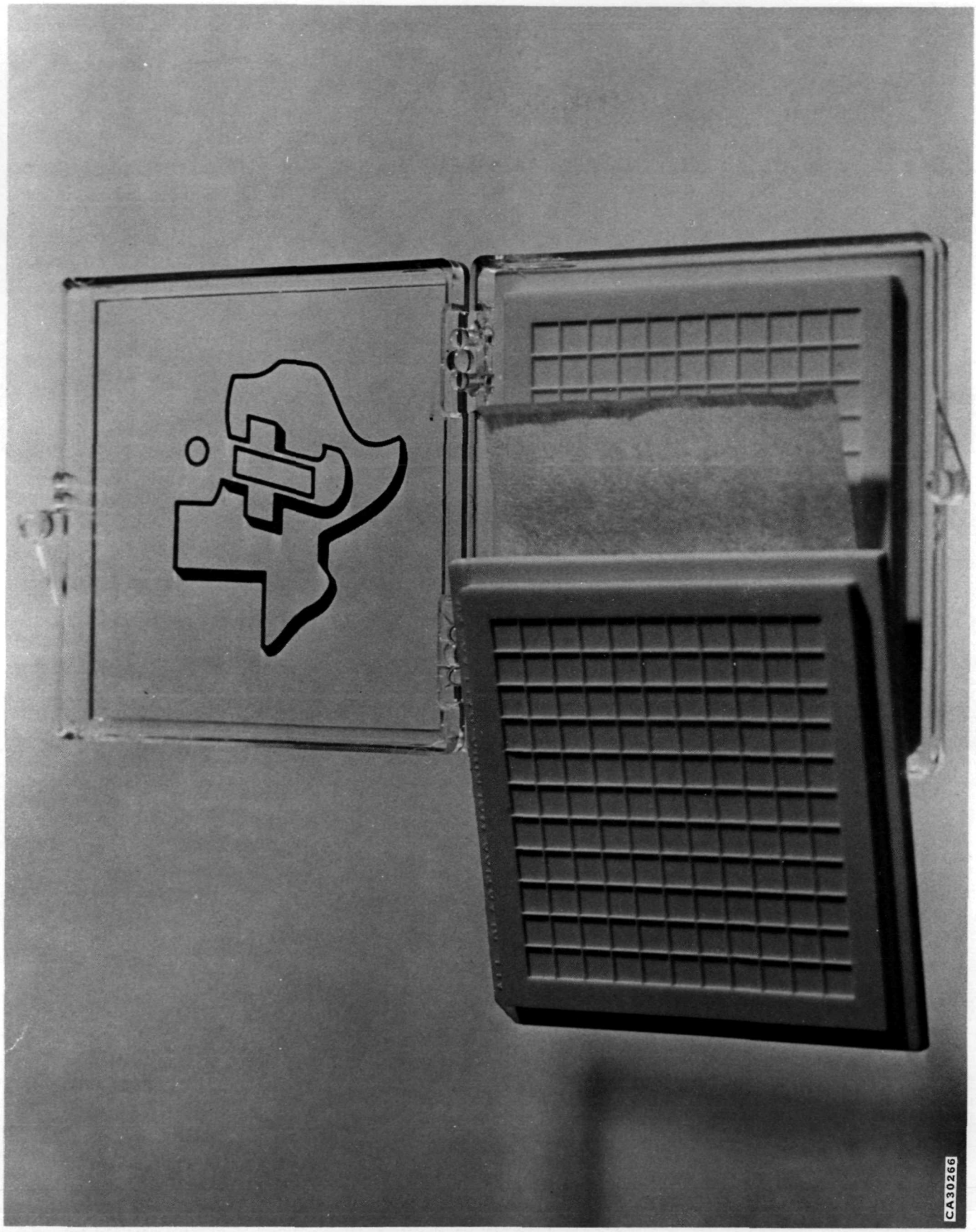


Figure 6. Packaging Method for Unmounted Bars

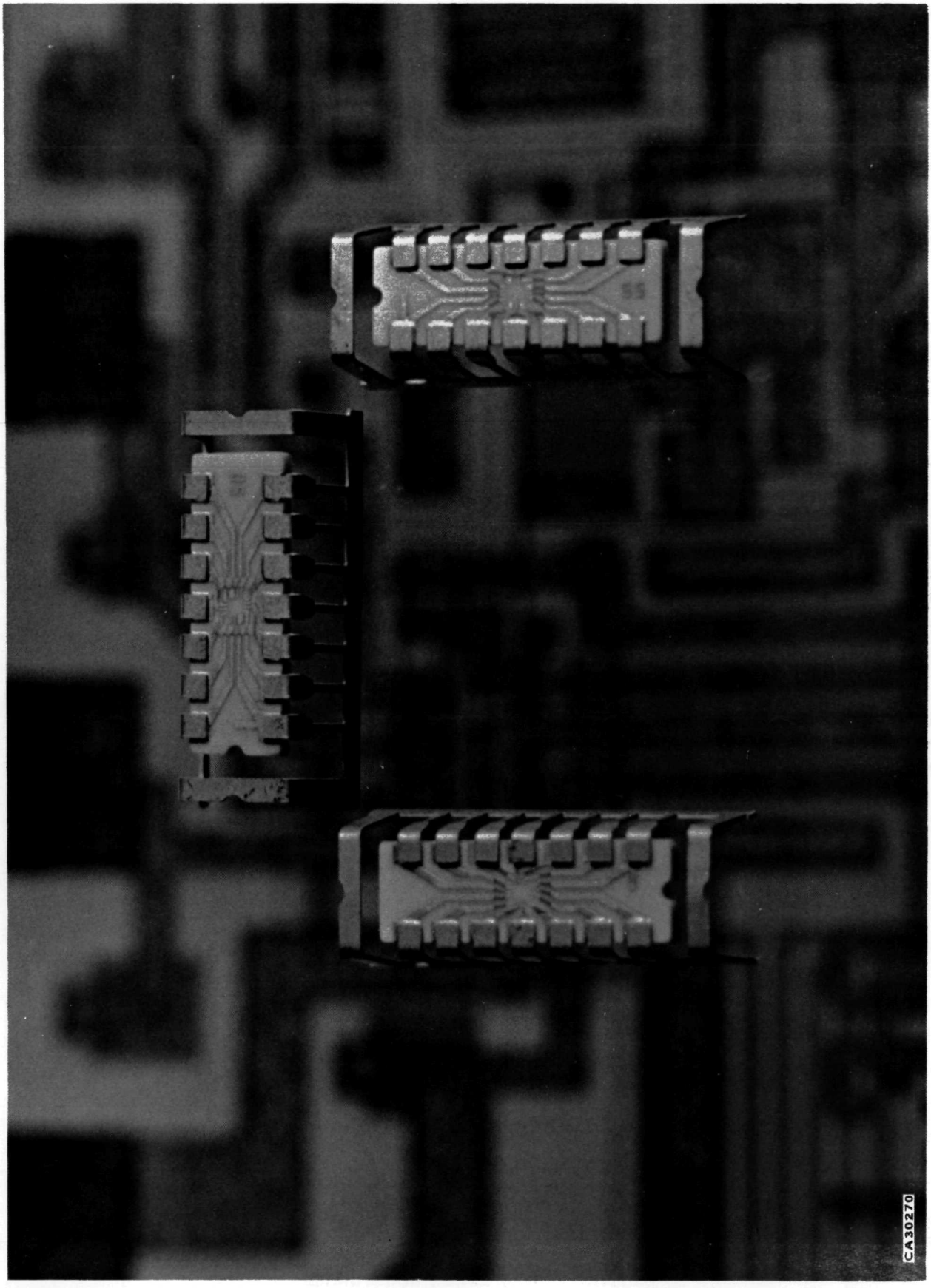


Figure 7. DIP Headers for Beam-Leaded Bars

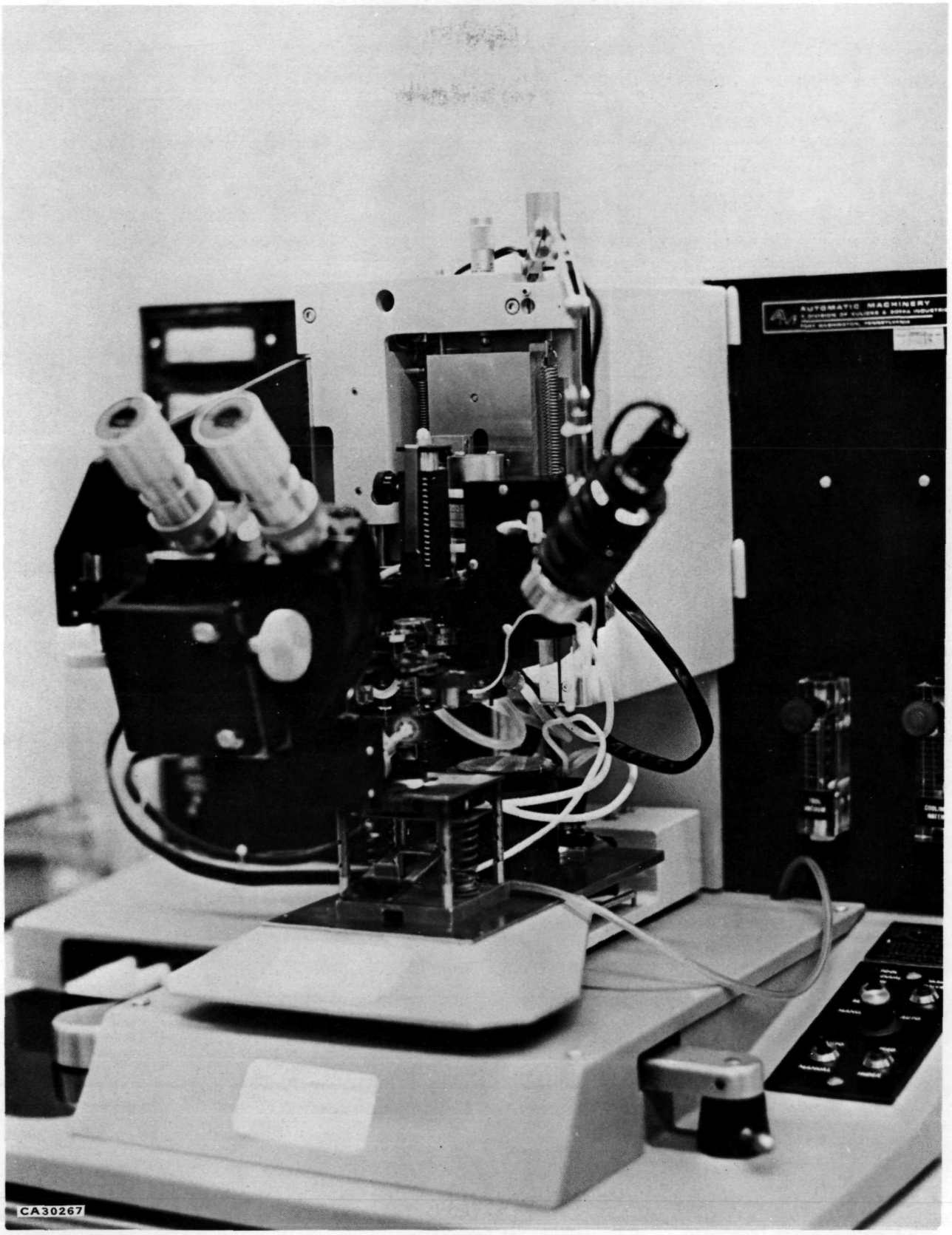


Figure 8. Beam Lead Wobble Bonder

Table II. Wobble Bonder Collet Descriptions

Calx, Inc.

Format	Circuit type	Style	Cavity inch	Wall thickness inch	Crown option	Material
45	BL54L00 BL54L20 BL54L30 BL54L55	1	0.039 X 0.049	0.006	No Crown	Titanium Carbide
50	BL54L67	1	0.049 X 0.049	0.006	No Crown	Titanium Carbide
55	BL54L68	1	0.049 X 0.059	0.006	No Crown	Titanium Carbide

Micro-Swiss, Inc. (K&S)

Format	Circuit type	Cavity Size inch	Manufacturers part number
45	BL54L00 BL54L20 BL54L30 BL54L55	0.039 X 0.049	C5800-202-.039-.049-.006-R
50	BL54L67	0.049 X 0.049	C5800-202-.049-,049-,006-R
55	BL54L68	0.049 X 0.059	C5800-202-.049-.059-.006-R

C. CIRCUIT DESCRIPTIONS

The circuit types developed in beam leads are basically like their counterparts in the standard low-power line (54L). The additions were made to each circuit. A clamp diode was added to each circuit input to dampen oscillation in the input signal and a Darlington stage was added to the top of each output. Refer to the Appendix for exact circuit configurations and for pictures of each part type.

A logic and circuit design change was made in the flip-flop used in the 54L72, single J-K flip-flop, and in the 54L73, Dual J-K flip-flop. This redesign improved the performance of these flip-flops as described in paragraph 1, to such an extent as to make renumbering necessary to avoid confusion. The number change is:

Old Number	New Number
54L72	BL54L67
54L73	BL54L68

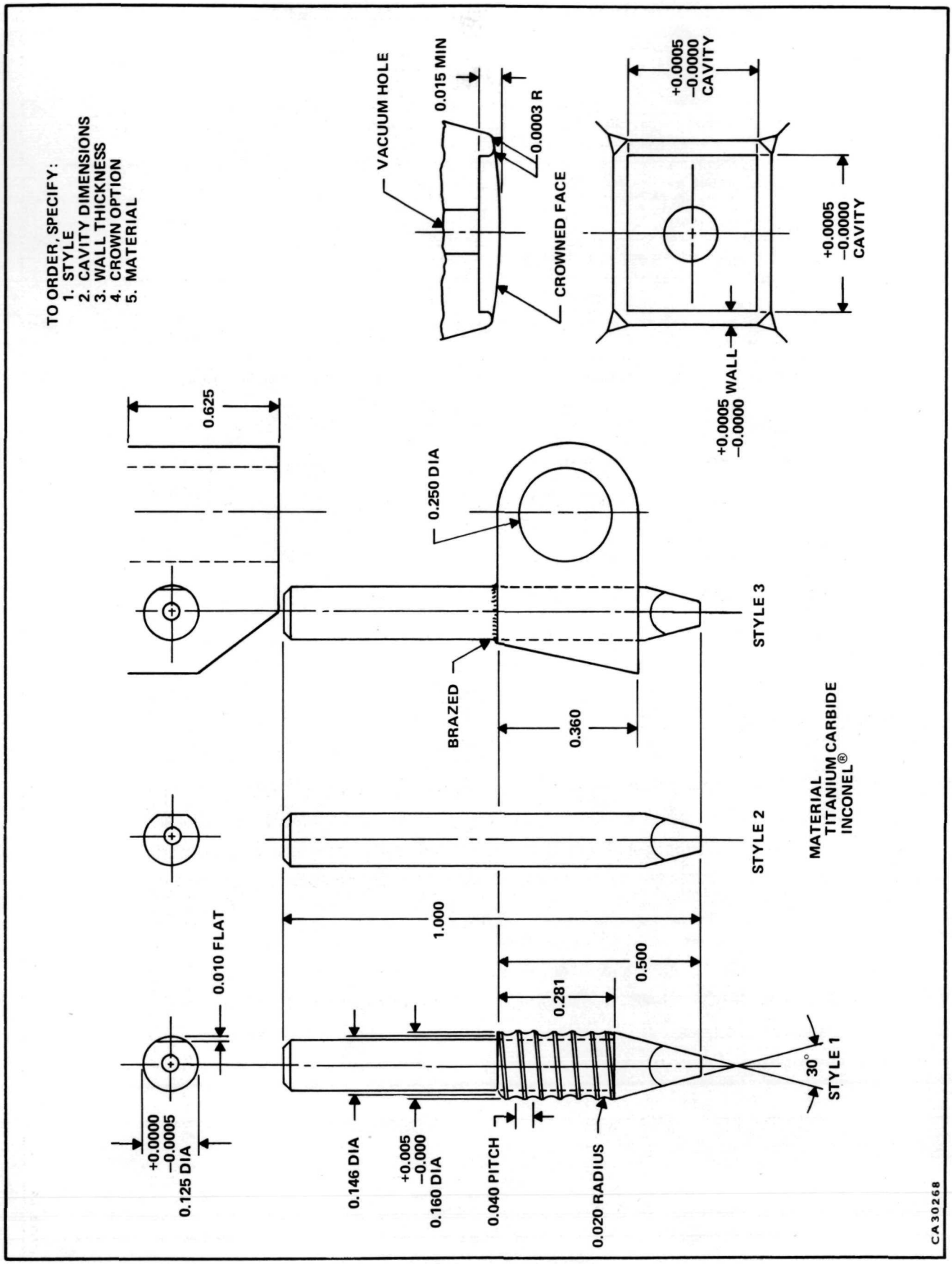


Figure 9. CALX Wobble Bonder Collet

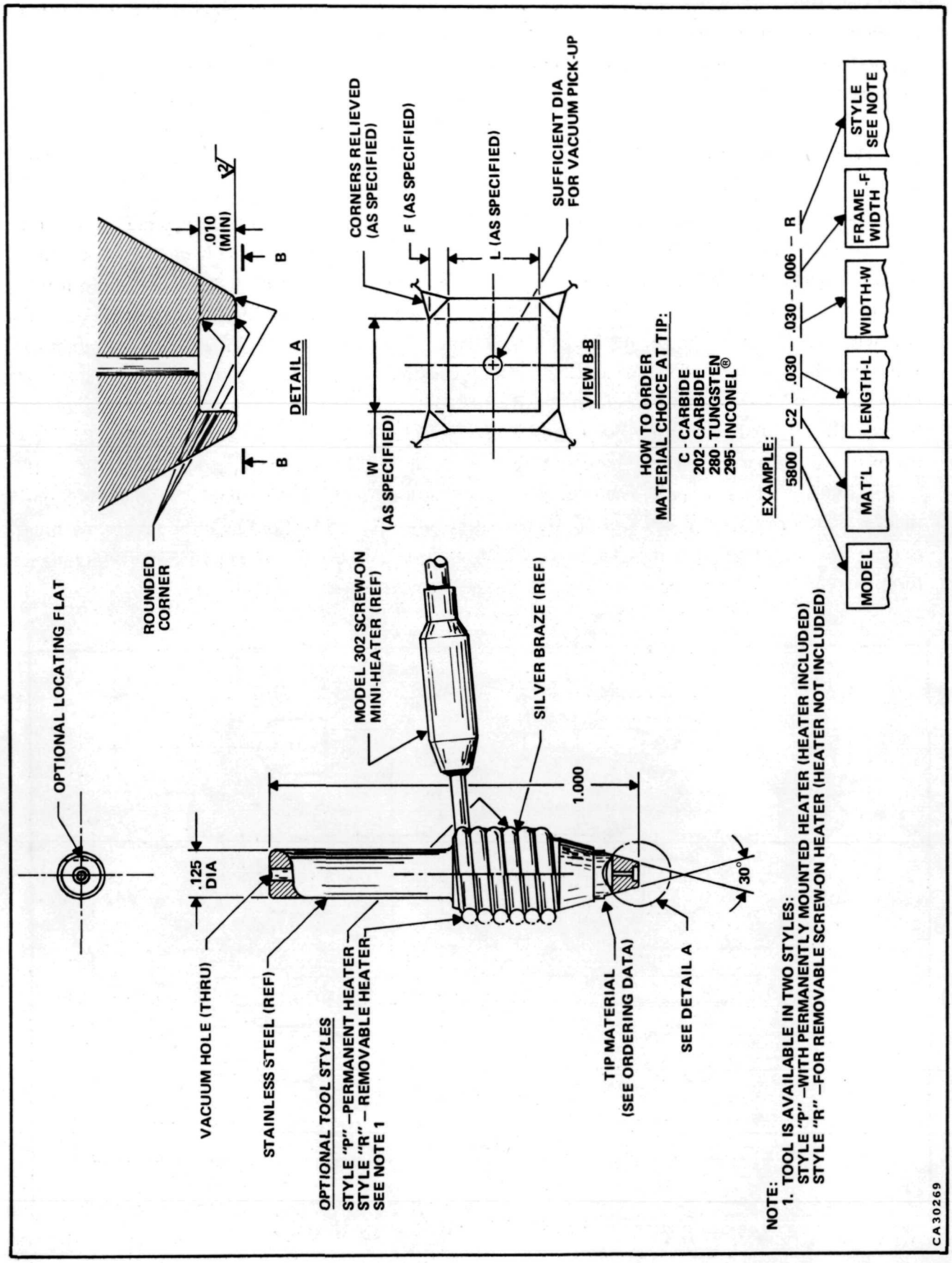


Figure 10. Micro-Swiss Wobble Bonder Collet

The prefix, BL, has been adopted to indicate that the parts are beam leaded. The description of operation of these new circuits as well as their advantages over the standard circuits are discussed below. Also, the process for the 1000 Ω-cm/cm resistor used in the design of the 54L68 is explained.

1. Theory of Operation–BL54L67/BL54L68

The circuit in Figure 11 is an edge-triggered J-K flip-flop which obeys all the same application rules as the catalog SN54L72/74L72. The clock input is ANDED with J and K inputs to lock data out for logical "0" clock inputs. The cross-coupled AND-OR-INVERT GATES of the output, logically lock out data from the J and K NAND gates when the clock is high. Thus there is no way that data can pass through the device except as controlled by the clock. With the clock high, data will enter the J and K NAND gates. If this data is oriented to cause the flip-flop to change state on clocking, a "0" will be input to either the B or D AND gate. This "0" will not disturb the output because the "1" fed back from the other output to the C or F AND gate will predominate. The "1" coupled from either G or H will have no effect on the outputs in this situation as it is ANDED with a "0" from the other output. When the clock is taken low, J and K are disabled, and at the same time, whichever of C or F was causing their respective output to be "on", will be taken low then causing the output to go "off". An internal node is cross-coupled to the opposite side which then turns the "off" side "on". Thus this logic circuit performs its desired function.

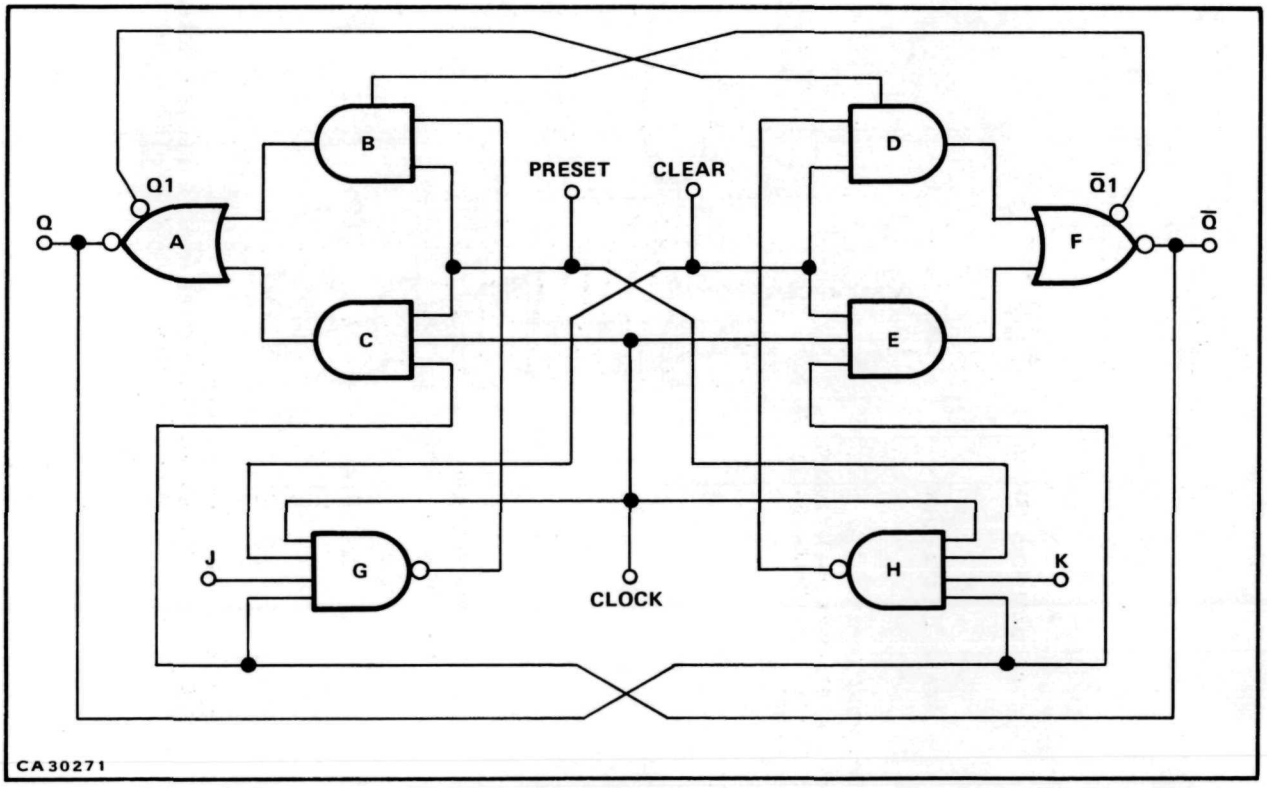


Figure 11. BL54L67/BL54L68 Logic Diagram

One potential ac race exists which must be designed in such a manner as to control the outcome. This race is best described by looking at the Figure 12 circuit schematic. On the negative-going clock, either Q5 or Q20 will be turned off, whichever is "on". Let us just consider the case with Q5 going "off". Its collector will rise and hence allow base current to turn on Q19. This must turn Q19 on prior to the time Q28 goes "off" and turns Q6 "on". The turn-off impedances R1 and R2 and the required voltage swings are used to fix the race. Q5 collector must swing only a few hundred millivolts whereas Q28 collector must swing about 1.3 volts. Hence the race can easily be controlled. The proposed design sets R1 = R2 = 18K ohms. Reducing R1 and R2 is detrimental to the race. So, in the lab, values as low as 6K ohms proved sufficient to maintain the race. Thus, a race problem was avoided.

Advantages of the proposed flip-flop design over the original flip-flop design are:

1) Logic state of J-K inputs may be changed when clock pulse is high if a prescribed setup time is observed.

2) Clock pulse can go to a negative voltage without changing the information at the outputs Q and $\overline{Q}$.

3) The maximum zero level (0.7 V) of the clock and J-K inputs are the same.

4) Increased high state fan-out capabilities due to the Darlington pull up.

5) Increased clock frequency due to reduced gate delays to set up latches.

6) T_{Pd} "0" is faster. T_{Pd} "0" has been reduced from 2 to 1-1/2 propagation delays.

7) Clamp diodes on all inputs. This will keep high currents out of flip-flop inputs for negative input transients.

8) The device does not have a high temperature threshold problem for temperatures up to 473°K.

2. Resistor Process–1000 Ohm-cm/cm

The 1000 ohm-cm/cm resistor process produces a penetration of 2-1/2 Hg lines and a surface concentration of 2.5×10^{18} atoms/cc. (The phosphorus oxide from the emitter process is left over the resistor to act as a barrier to the movement of positive ions.)

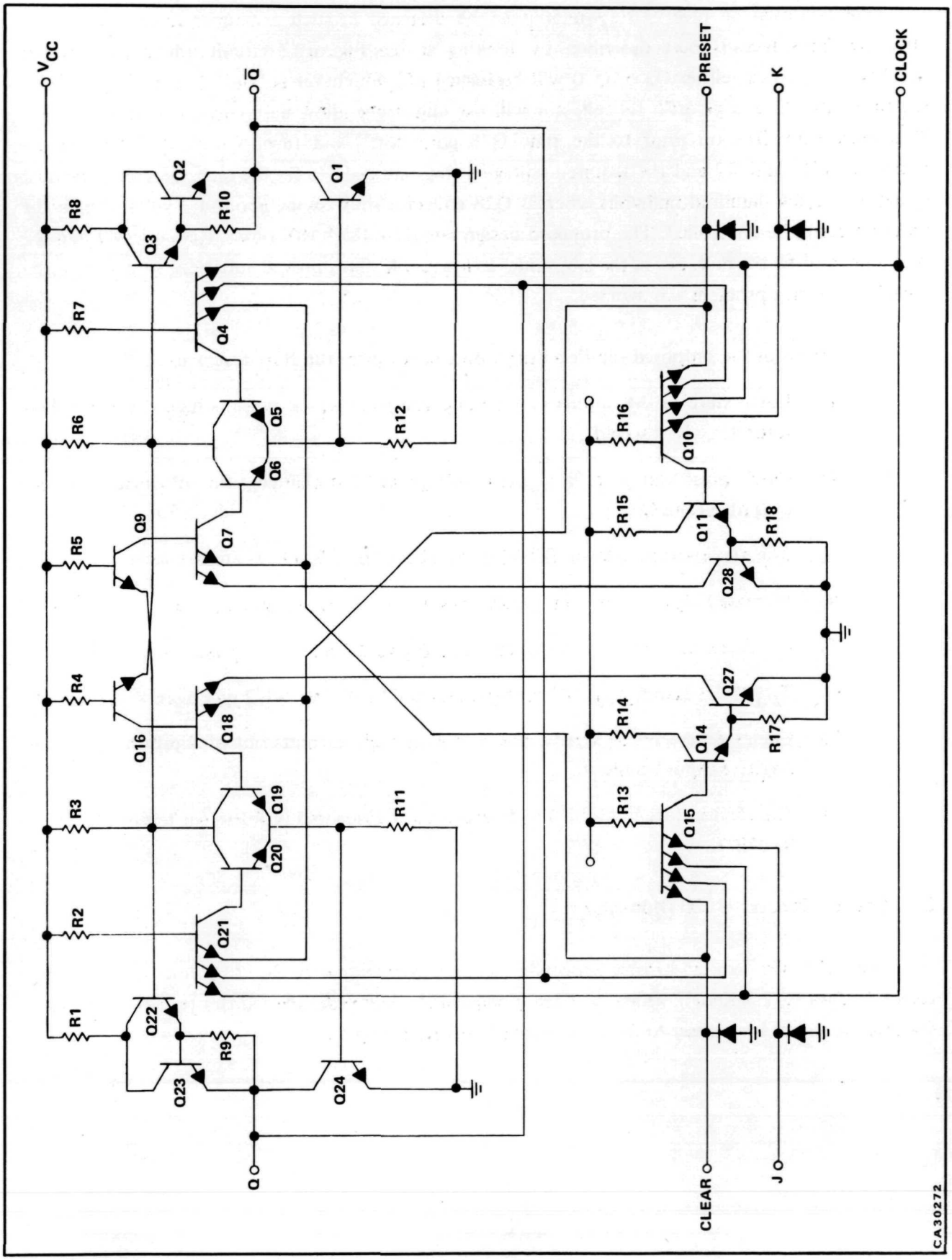


Figure 12. BL54L67/BL54L68 Circuit Schematic

The temperature coefficient for the 240 ohm-cm/cm resistor is 1760 ppm/K° and it is 3016 ppm/K° for the 1000 ohm-cm/cm resistor. The resistor change, ΔR, due to a change in temperature, ΔT, is given by

$$\Delta R = F \times R \times \Delta T \times 10^{-6}$$

where F is the temperature coefficient given above and R is the resistor value at 298° K. The slight increase in the coefficient for the 1000 ohm-cm/cm resistor is due to the slightly lower surface concentration.

Page Intentionally Left Blank

SECTION IV
TESTING AND EVALUATION

A. PROBE TEST AND LOT QUALIFICATION

The primary product of a beam lead family is unmounted bars. These bars must be capable of operation over the full military temperature range, −55°C to 125°C (218°K to 398°K). To meet this criteria, the 100% probe test for beam lead bars must be as stringent as the final test for standard packaged parts. The probe test for standard product is normally used only as a screen to remove the catastrophic rejects. The various product categories are separated at final test. Guaranteeing ac performance is also a problem in beam lead testing because it is extremely difficult to perform switching and propagation delay measurements at probe on a production basis.

The decision was made to perform a full functional test as well as a guard-banded parametric test at the 100% probe test. The guard-bands are set to guarantee the electrical performance of the part over the temperature range specified. In addition to the 100% probe test, a sample from each diffusion lot is taken, mounted on headers and tested for full functional, parametric and ac performance. This sample test serves to qualify the switching and dynamic integrity of the lot since the parameters that effect switching times are diffusion lot dependent.

The beam bond strength is also established on a diffusion lot sample basis. The bar sample is bonded on a gold-plated Kovar substrate. The bars are positioned over a square hole in the Kovar. After a visual inspection to eliminate badly bonded bars from the test, the substrates are placed in the bond strength test machine shown in Figure 13. A square needle sized for the bar under test is inserted into the hole in the Kovar plate and brought to rest against the bar. Force is then exerted by the operator until the bar either breaks or the beams are pushed away from the substrate. The force necessary to cause the failure and the mode of failure are noted by the operator. The pressure is compared with a minimum requirement of 0.7 grams/mil of beam width (1.0×10^6 newton/meter^2). This would set a minimum of 2.1 grams force (0.02 newtons) for each 3 mil (7.62×10^{-3} cm) beam. Initial push-off tests have given the results shown in Table III. Refer to Figures 14 through 16 for format descriptions.

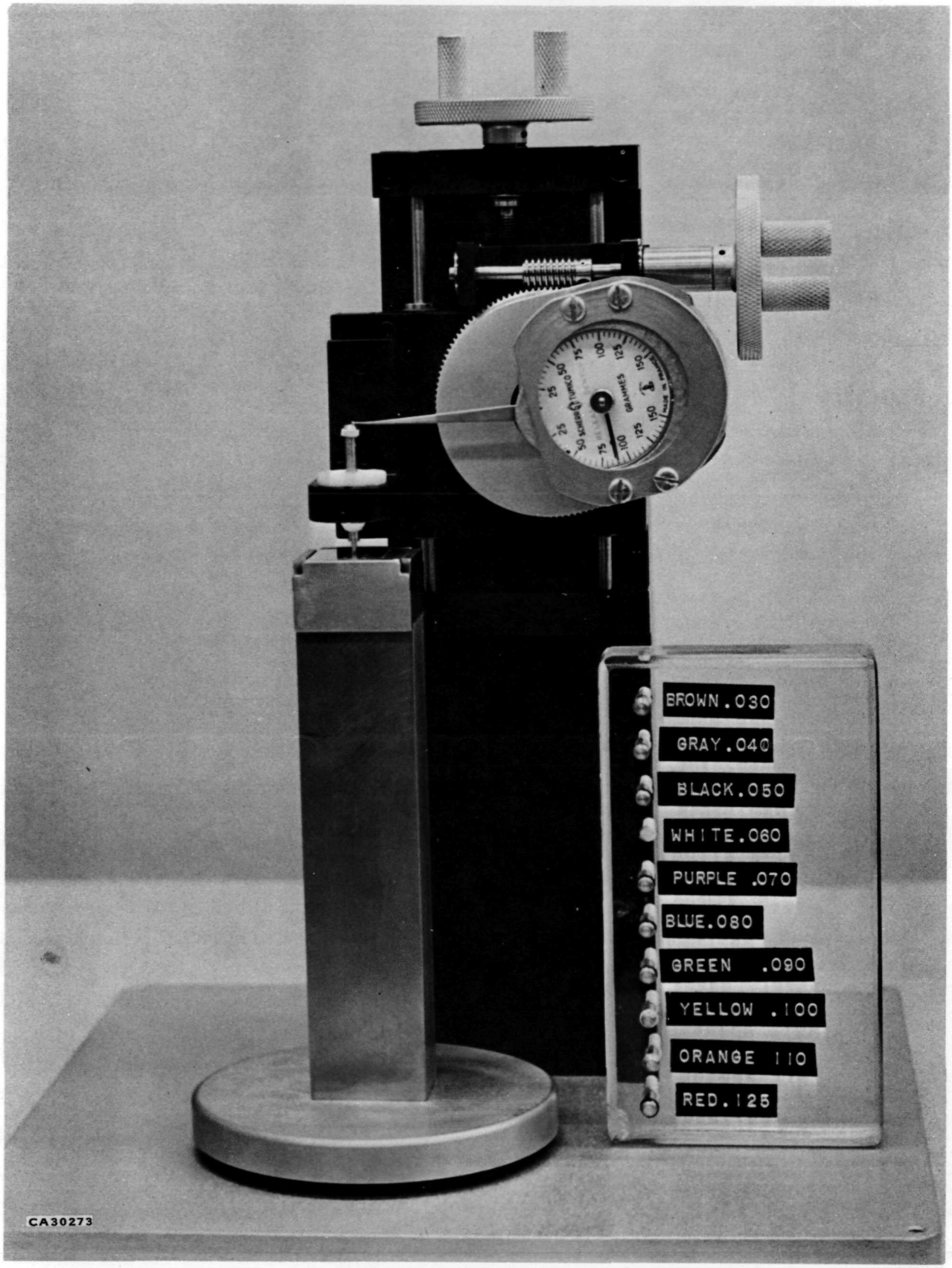


Figure 13. Beam Lead Push-Off Tester

Table III. Bond Push-Off Test Strength

Format No.	No. of beams	Push-off force—newtons		Sample size
		Average	Failure limits	
45	14	0.500	0.304 to 0.637	12
50	16	0.618	0.392 to 0.804	12
55	18	0.658	0.343 to 0.932	12

B. DEVICE CHARACTERIZATION

The mounted bars were subjected to complete dc (parametric and functional) and ac (switching and dynamic) testing as shown in the Appendix, at −55°C, 25°C, and 125°C (218°K, 298°K, and 398°K). These tests were used to screen thermal and ac rejects and to establish the guard-bands required at probe. The results of the evaluation tests in the form of mean values are given in Table IV. In general, the beam-leaded parts compare favorably with the standard low-power TTL.

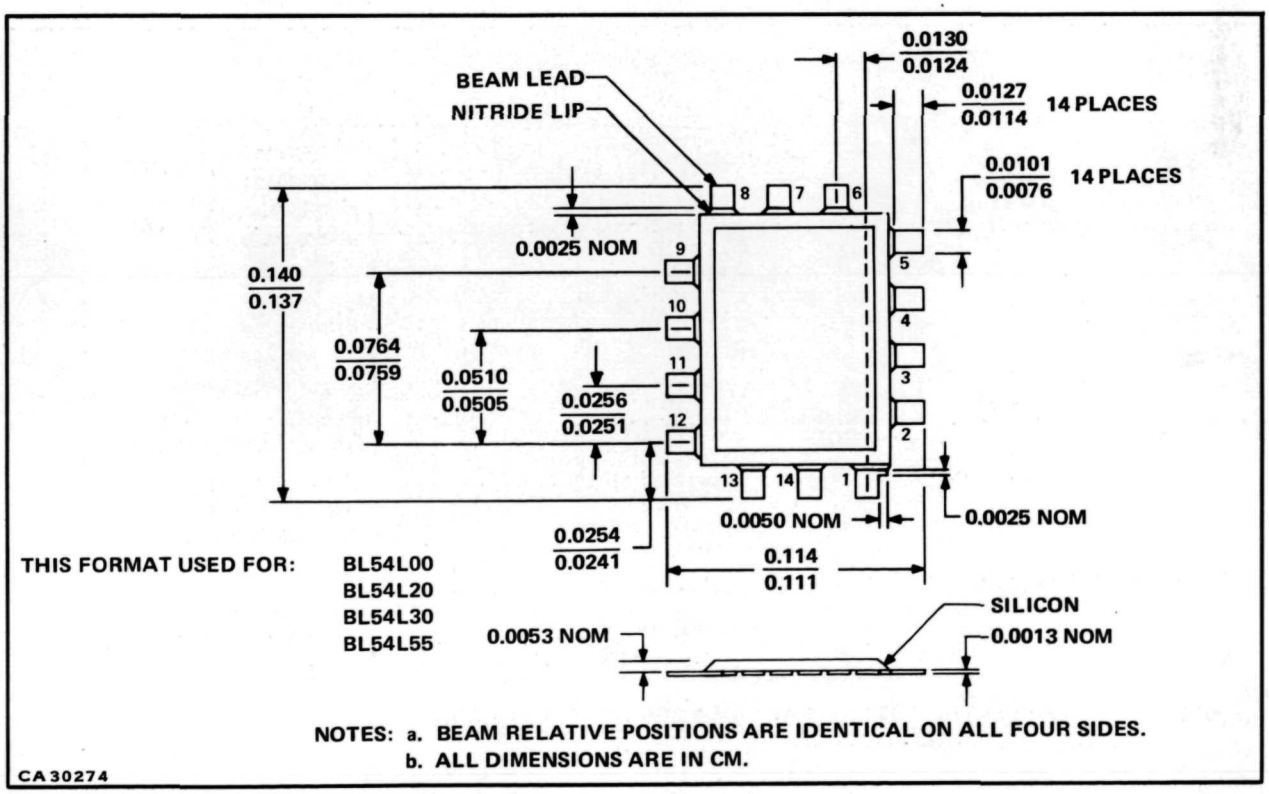


Figure 14. Beam Lead Format 45

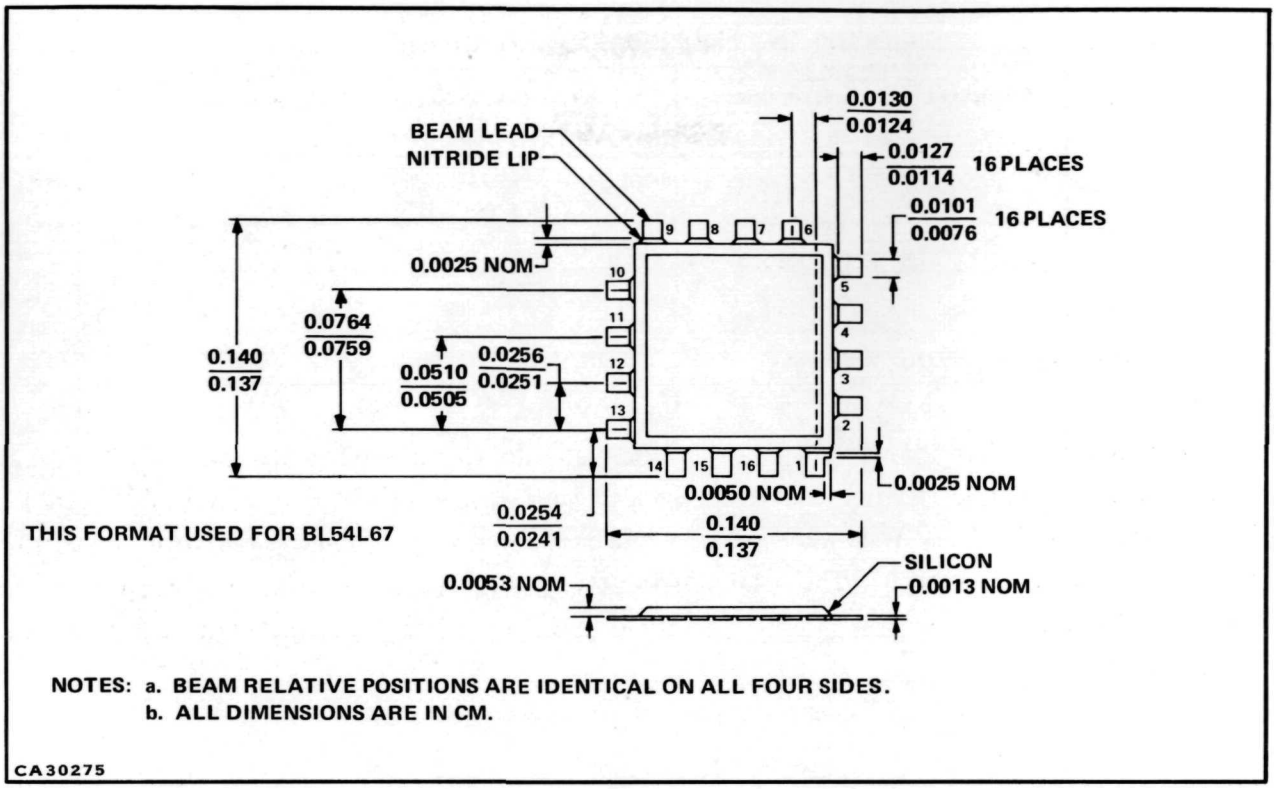


Figure 15. Beam Lead Format 50

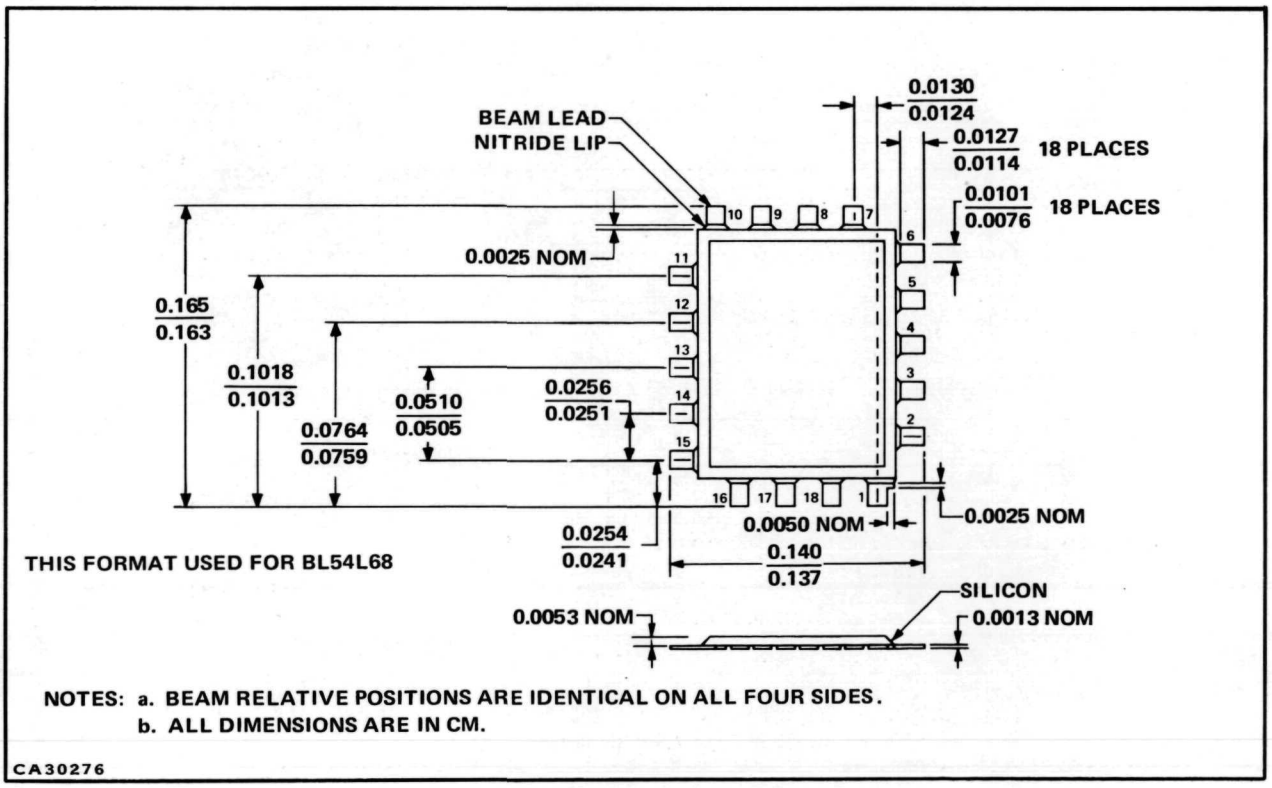


Figure 16. Beam Lead Format 55

Table IV. Beam Lead Evaluation (Mean Values)

Circuit	TA	I_I μA	I_{IH} μA	V_{OL} volts	V_{OH} volts	I_{IL} mA	I_{OS} mA	I_{CCH} mA	I_{CCL} mA	V_I volts	T_{PHL} nsec	T_{PLH} nsec
BL54L00	Spec	<100	<10	<0.3	>2.4	<−0.18	>−3 <−15	<0.8	<2.04	<−1.5	<60	<60
	125°C	8.411	5.493	0.182	2.932	−0.116	−9.146	0.578	1.387	−1.114	31.13	41.757
	25°C	7.197	4.273	0.162	2.882	−0.128	−10.045	0.595	1.505	−1.186	34.202	29.332
	−55°C	5.479	3.732	0.135	2.799	−0.138	−10.374	0.612	1.549	−1.296	51.951	30.912
BL54L20	Spec	<100	<10	<0.3	>2.4	<−0.18	>−3 <−15	<0.4	<1.02	<−1.5	<60	<60
	125°C	3.719	4.015	0.181	3.03	−0.103	−8.526	0.232	0.60	−1.237	37.572	45.175
	25°C	6.850	6.167	0.157	3.012	−0.115	−9.622	0.254	0.656	−1.317	43.504	31.552
	−55°C	–	–	0.135	2.816	−0.125	−10.102	–	0.805	−1.370	49.893	22.490
BL54L30	Spec	<100	<10	<0.3	>2.4	<−0.18	>−3 <−15	<0.33	<0.51	<−1.5	<100	<60
	125°C	5.996	2.745	0.196	2.810	−0.101	−7.701	0.115	0.292	−1.149	76.131	53.110
	25°C	3.330	2.026	0.148	2.845	−0.118	−9.141	0.128	0.328	−1.214	81.985	35.517
	−55°C	4.734	1.868	0.137	2.813	−0.129	−9.627	0.132	–	−1.281	99.162	28.649
BL54L55	Spec	<100	<10	<0.3	>2.4	<−0.18	>−3 <−15	<0.4	<0.65	<−1.5	<60	<90
	125°C	9.067	4.671	0.170	2.879	−0.101	−8.459	0.334	0.376	−1.230	39.552	51.434
	25°C	9.665	3.967	0.150	2.919	−0.114	−9.577	0.347	0.402	−1.297	45.241	38.983
	−55°C	6.699	3.258	0.127	2.806	−0.123	−10.097	0.365	0.419	−1.355	57.260	28.606

		I_I, mA		I_{IH}, mA			V_{OL} Volts	V_{OH} Volts	I_{IL}, mA			I_{OS} mA	
Circuit	TA	J or K	Preset Clear-Clock	J or K	Preset or Clear	Clock	Max	Min	J or K	Preset or Clear	Clock	Min	Max
BL54L67	Spec	<100	<200	<10	<30	<40	<0.3	>2.4	<−0.18	<−0.54	<−0.72	>−3	<−15
	125°C	–	–	–	–	3.110	0.189	3.241	−0.078	−0.156	−0.365	−8.424	
	25°C	–	–	–	–	2.638	0.166	3.058	−0.087	−0.173	−0.401	−9.817	
	−55°C	–	–	–	1.175	2.707	0.130	2.805	−0.089	−0.177	−0.399	−8.702	
BL54L68	Spec	<100	<200	<10	<30	<40	<0.3	>2.4	<−0.18	<−0.54	<−0.72	>−3	<−15
	125°C	–	–	–	0.132	1.761	0.203	3.026	−0.025	−0.053	−0.094	−7.299	
	25°C	–	–	–	0.062	1.609	0.177	2.956	−0.029	−0.059	−0.113	−8.254	
	−55°C*	–	–	–	–	–	–	–	–	–	–	–	

				t_{PLH}, nsec		t_{PHL}, nsec		
Circuit	TA	I_{CC} mA	V_I volts	Clock	Preset or Clear	Clock	Preset or Clear	Preset or Clear
BL54L67	Spec	<1.44	<−1.5	<75	<75	<150	<150	<200
	125°C	0.997	−1.029	44.448	43.87	40.909	47.732	56.384
	25°C	1.086	−1.101	35.512	31.049	39.459	44.475	50.474
	−55°C	1.071	−1.101	33.395	36.038	52.143	61.422	64.671
BL54L68	Spec	<2.88	<−1.5	<75	<75	<150	<150	<200
	125°C	1.344	−0.896	62.313	54.073	57.522	53.154	60.056
	25°C	1.513	−0.981	48.032	43.028	58.578	54.812	59.664
	−55°C	–	–	–	–	–	–	–

*Test on BL54L68 at −55°C was invalid due to frosting of package.

These results are for a sample size of 50 pieces.

Some problems were encountered in the testing of the parts at −55°C (218°K). The equipment used to lower the ambient temperature employs compressed nitrogen gas. Although the gas is relatively dry, a frost forms on the parts. This causes a problem because of the fine line definition on the headers shown in Figure 7, particularly on the low current dc and all ac measurements. To overcome the problem, Dow Corning 62-047WE, Junction Coating Resin was used to coat the top of the headers. Several parts were damaged in this operation because of operator error in using excessive air pressure to spray the parts. The high pressure forced the face of the bars into contact with metallization on the header causing an electrical short circuit. Further testing needs to be performed on the coating method to be used on future beam lead assemblies. Most of the units used for the evaluation were not coated because of this problem. The incompleteness of the data in Table IV reflects inaccurate data caused by the problem of units frosting at low temperature.

SECTION V
RESULTS

The objective of the program to beam lead selected parts of the low-power TTL (54L) family has been met. The circuits and electrical performance reflected in the data sheets (Appendix) meet or exceed the standard part type's values. This inventory of parts now forms a base for use in systems in which heat, power, size, weight, and reliability are controlling factors.

Also, the process has been established for processing future parts to be added to the beam-leaded low-power TTL family.

Page Intentionally Left Blank

APPENDIX
BEAM LEAD CIRCUITS SCHEMATICS AND PHOTOGRAPHS

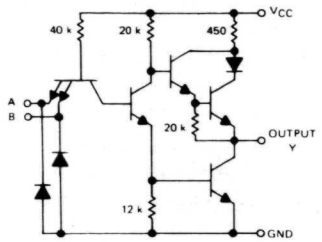
Page Intentionally Left Blank

BEAM-LEAD LOW-POWER TTL CHIPS

CIRCUIT TYPES BL54L00Y, BL74L00Y QUADRUPLE 2-INPUT POSITIVE-NAND GATES

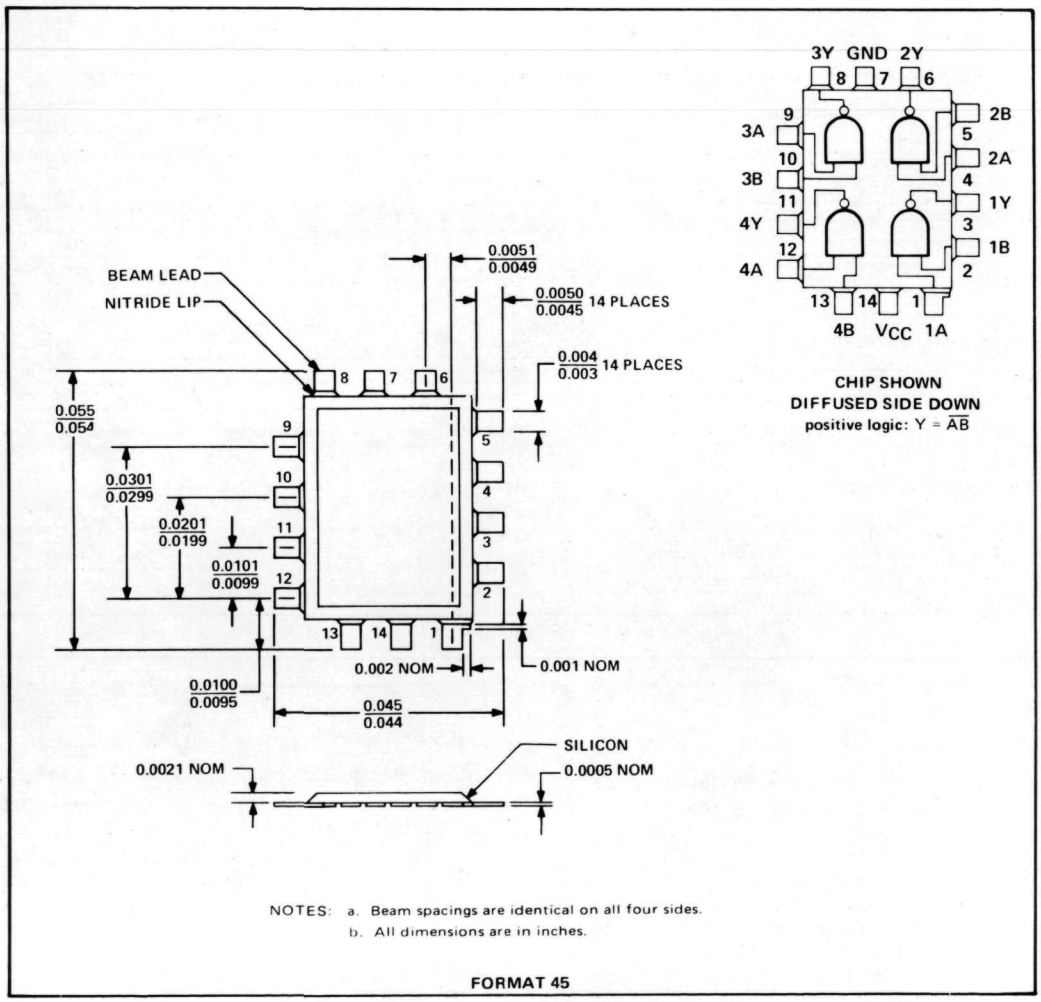
- BL54L00Y/BL74L00Y Chips When Assembled Display Characteristics Similar to SN54L00/SN74L00
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

schematic (each gate)



Resistor values are nominal in ohms.

mechanical data and logic



NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

FORMAT 45

1271

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES BL54L00Y, BL74L00Y
BULLETIN NO. DL-S7111582, DECEMBER 1971

Figure 17. Circuit Types BL54L00Y and BL74L00Y Schematic (Sheet 1 of 2)

CIRCUIT TYPES BL54L00Y, BL74L00Y
QUADRUPLE 2-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L00Y Circuits . . . . . −55°C to 125°C
BL74L00Y Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	BL54L00Y			BL74L00Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

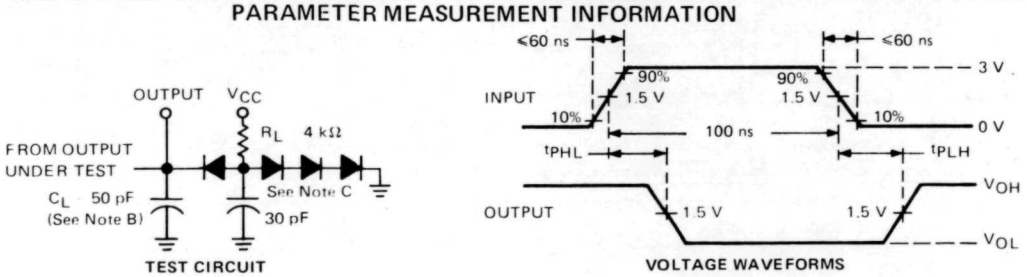
PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA		−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	−3	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.51	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			31	60	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveform is supplied by a generator having the following characteristics: PRR = 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 1–PROPAGATION DELAY TIMES

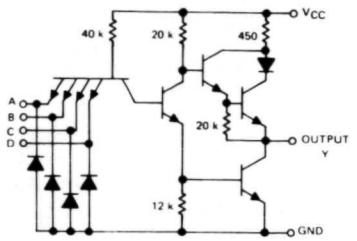
Figure 17. Circuit Types BL54L00Y and BL74L00Y Schematic (Sheet 2 of 2)

BEAM-LEAD LOW-POWER TTL CHIPS

CIRCUIT TYPES BL54L20Y, BL74L20Y DUAL 4-INPUT POSITIVE-NAND GATES

- BL54L20Y/BL74L20Y Chips When Assembled Display Characteristics Similar to SN54L20/SN74L20
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

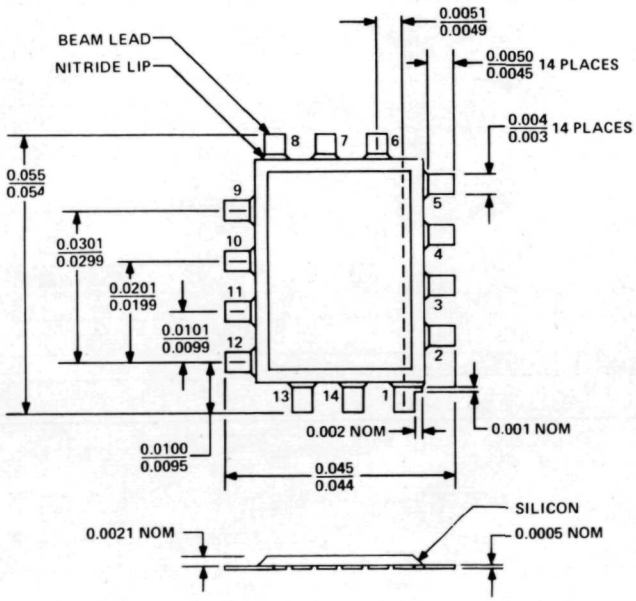
schematic (each gate)

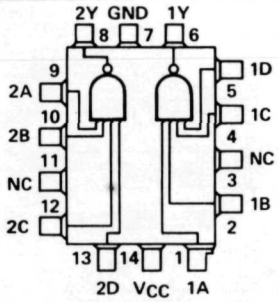


Resistor values are nominal in ohms

CIRCUIT TYPES BL54L20Y, BL74L20Y
BULLETIN NO. DL-S 7111583, DECEMBER 1971

mechanical data and logic





NC—No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN
positive logic: $Y = \overline{ABCD}$

NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

FORMAT 45

1271

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 18. Circuit Types BL54L20Y and BL74L20Y Schematic (Sheet 1 of 2)

CIRCUIT TYPES BL54L20Y, BL74L20Y
DUAL 4-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage (see Note 1) . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L20Y Circuits . . . . . −55°C to 125°C
BL74L20Y Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	BL54L20Y			BL74L20Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

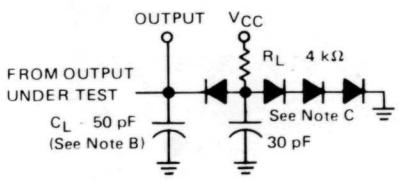
PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA		−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	−3	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V		0.2	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.51	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device types.
§Not more than one output should be shorted at a time.

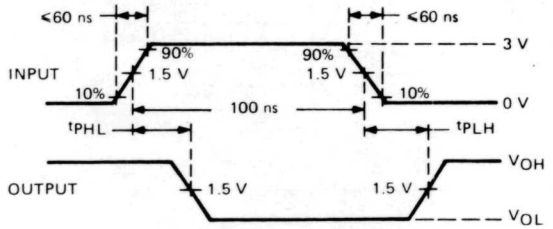
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			31	60	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator having the following characteristics: PRR = 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 1–PROPAGATION DELAY TIMES

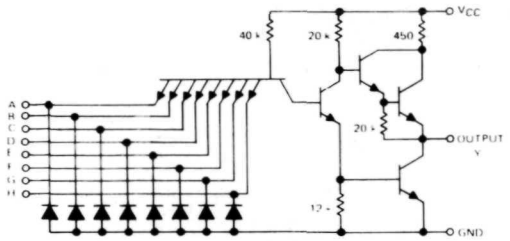
Figure 18. Circuit Types BL54L20Y and BL74L20Y Schematic (Sheet 2 of 2)

BEAM-LEAD LOW-POWER TTL CHIPS

CIRCUIT TYPES BL54L30Y, BL74L30Y 8-INPUT POSITIVE-NAND GATES

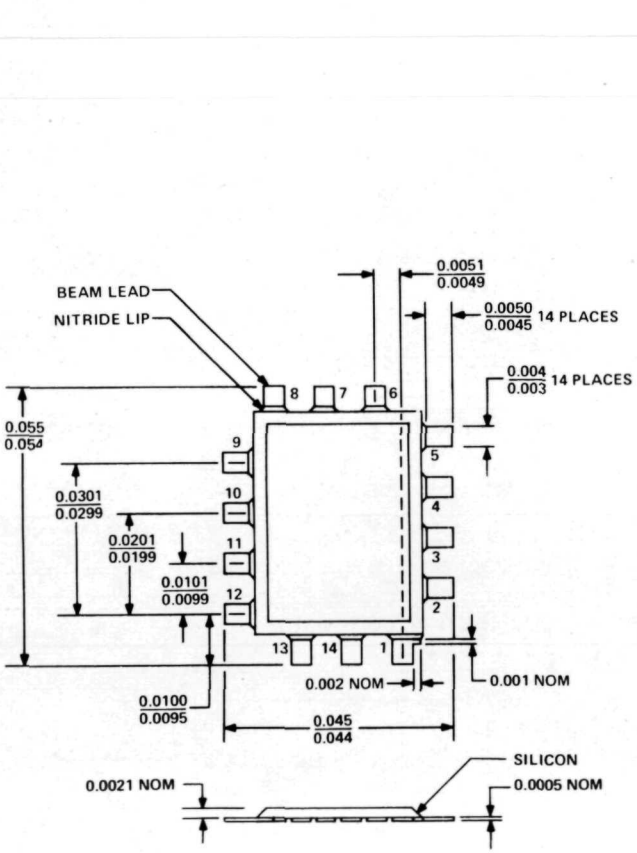
- BL54L30Y/BL74L30Y Chips When Assembled Display Characteristics Similar to SN54L30/SN74L30
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

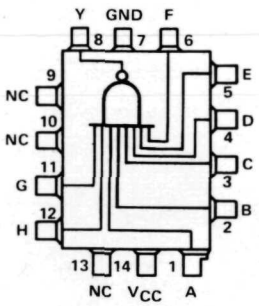
schematic



Resistor values are nominal in ohms.

mechanical data and logic





NC—No internal connection

CHIP SHOWN
DIFFUSED SIDE DOWN

positive logic: $Y = \overline{ABCDEFGH}$

NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

FORMAT 45

1271

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

CIRCUIT TYPES BL54L30Y, BL74L30Y
BULLETIN NO. DL-S 7111584, DECEMBER 1971

Figure 19. Circuit Types BL54L30Y and BL74L30Y Schematic (Sheet 1 of 2)

CIRCUIT TYPES BL54L30Y, BL74L30Y
8-INPUT POSITIVE-NAND GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		8 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range:	BL54L30Y Circuits	−55°C to 125°C
	BL74L30Y Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	BL54L30Y			BL74L30Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

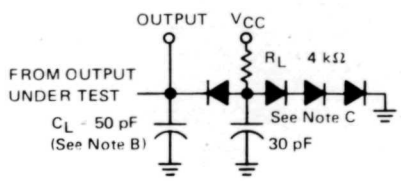
PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA		−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	−3	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V		0.33	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.51	mA

† For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§ Not more than one output should be shorted at a time.

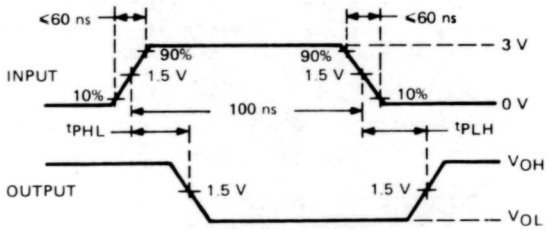
switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		35	60	ns
t_{PHL}	Propagation delay time, high-to-low-level output			70	100	ns

PARAMETER MEASUREMENT INFORMATION



TEST CIRCUIT



VOLTAGE WAVEFORMS

NOTES: A. The input waveform is supplied by a generator having the following characteristics: PRR = 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 1–PROPAGATION DELAY TIMES

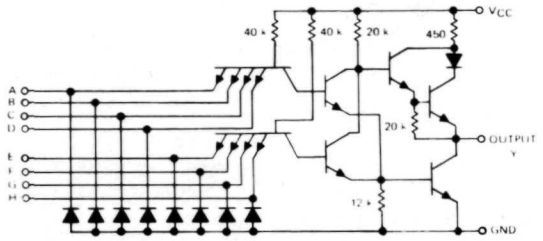
Figure 19. Circuit Types BL54L30Y and BL74L30Y Schematic (Sheet 2 of 2)

BEAM-LEAD
LOW-POWER TTL CHIPS

CIRCUIT TYPES BL54L55Y, BL74L55Y
2-WIDE 4-INPUT AND-OR-INVERT GATES

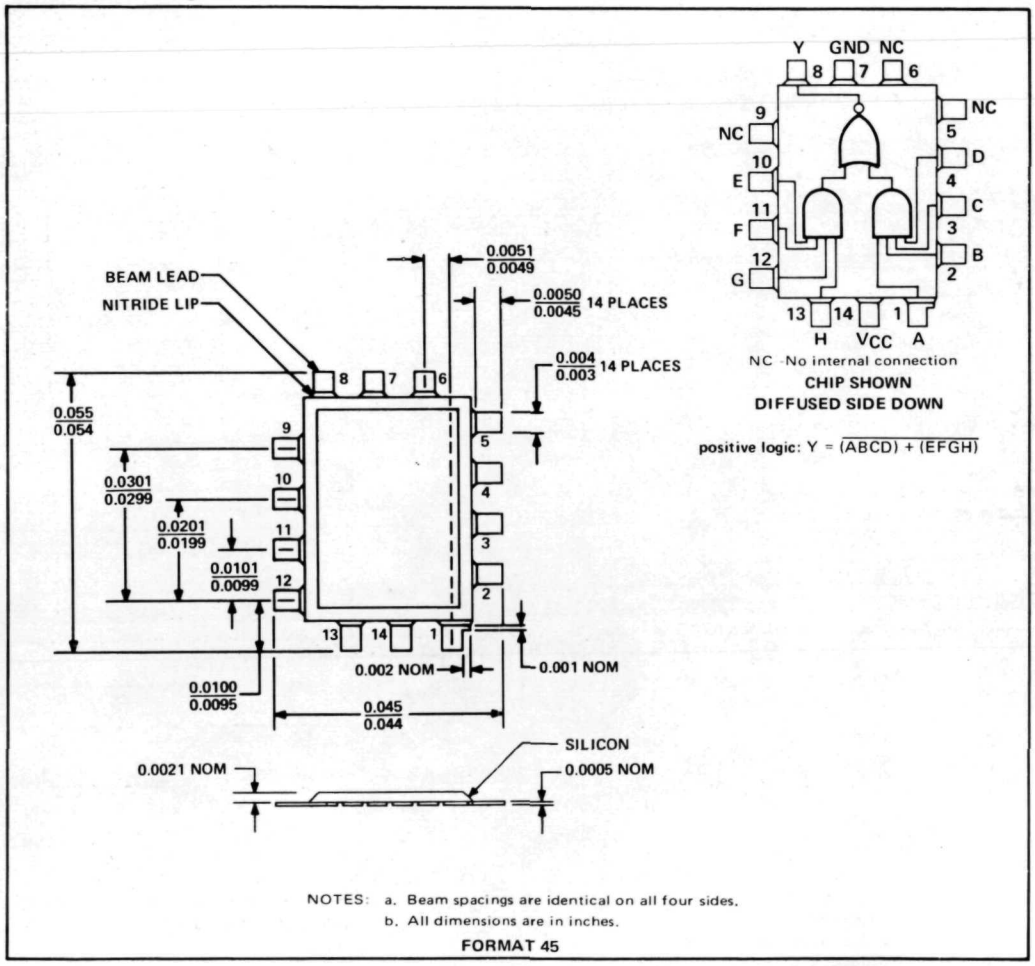
- BL54L55Y/BL74L55Y Chips When Assembled Display Characteristics Similar to SN54L55/SN74L55
- Silicon Nitride Sealed Junction
- Gold Beams
- Available in Chip Form or as Part of a Complex Logic Assembly
- Diode-Clamped Inputs

schematic



Resistor values are nominal in ohms

mechanical data and logic



NOTES: a. Beam spacings are identical on all four sides.
b. All dimensions are in inches.

FORMAT 45

1271

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 20. Circuit Types BL54L55Y and BL74L55Y Schematic (Sheet 1 of 2)

CIRCUIT TYPES BL54L55Y, BL74L55Y
2-WIDE 4-INPUT AND-OR-INVERT GATES

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1)		8 V
Input voltage (see Note 1)		5.5 V
Interemitter voltage (see Note 2)		5.5 V
Operating free-air temperature range:	BL54L55Y Circuits	−55°C to 125°C
	BL74L55Y Circuits	0°C to 70°C
Storage temperature range		−65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	BL54L55Y			BL74L55Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Operating free-air temperature, T_A	−55		125	0		70	°C

electrical characteristics over recommended operating free-air temperature range

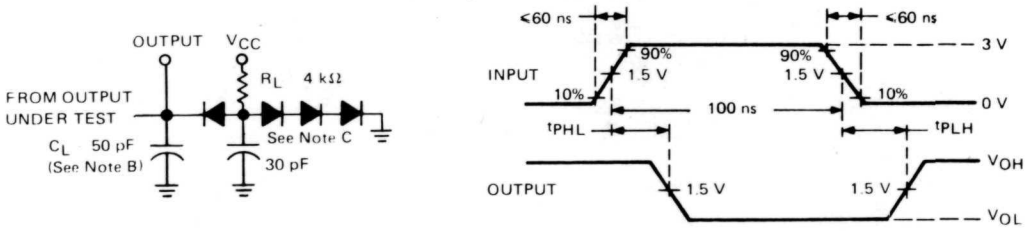
PARAMETER		TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage		2		V
V_{IL}	Low-level input voltage			0.7	V
V_I	Input clamp voltage	V_{CC} = MIN, I_I = −8 mA		−1.5	V
V_{OH}	High-level output voltage	V_{CC} = MIN, V_I = 0.7 V, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage	V_{CC} = MIN, V_I = 2 V, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	V_{CC} = MAX, V_I = 5.5 V		100	μA
I_{IH}	High-level input current	V_{CC} = MAX, V_I = 2.4 V		10	μA
I_{IL}	Low-level input current	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
I_{OS}	Short-circuit output current§	V_{CC} = MAX, V_I = 0	−3	−15	mA
I_{CCH}	Supply current, high-level output (average per gate)	V_{CC} = MAX, All inputs at 0 V		0.4	mA
I_{CCL}	Supply current, low-level output (average per gate)	V_{CC} = MAX, All inputs at 5 V		0.65	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
§Not more than one output should be shorted at a time.

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
t_{PLH}	Propagation delay time, low-to-high-level output	C_L = 50 pF, R_L = 4 kΩ, See Figure 1		50	90	ns
t_{PHL}	Propagation delay time, high-to-low-level output			35	60	ns

PARAMETER MEASUREMENT INFORMATION



NOTES: A. The input waveform is supplied by a generator having the following characteristics: PRR = 500 kHz, Z_{out} = 50 Ω.
B. C_L includes probe and jig capacitance.
C. All diodes are 1N916 or equivalent.

FIGURE 1–PROPAGATION DELAY TIMES

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 20. Circuit Types BL54L55Y and BL74L55Y Schematic (Sheet 2 of 2)

BEAM-LEAD LOW-POWER TTL CHIPS

CIRCUIT TYPES BL54L67Y, BL74L67Y J-K EDGE-TRIGGERED FLIP-FLOPS

- **BL54L67Y/BL74L67Y Chips When Assembled Can Replace SN54L72/SN74L72 in Most Applications**
- **Silicon-Nitride-Sealed Junctions**
- **Gold Beams**
- **Available in Chip Form or as Part of a Complex Logic Assembly**
- **Diode-Clamped Inputs**

TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	$\overline{Q}$
L	L	Q_n	$\overline{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\overline{Q}_n$	Q_n

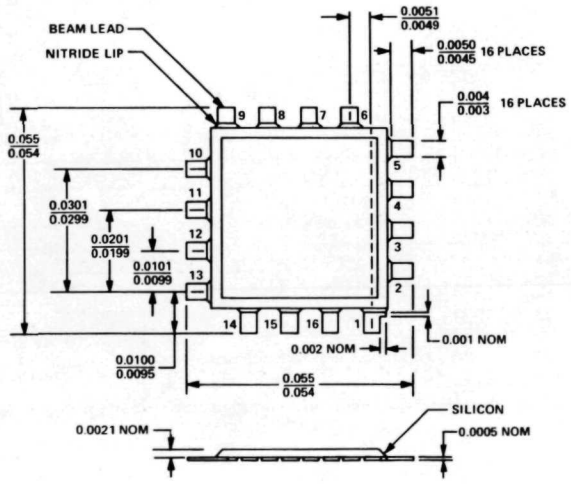
$J = J1 \cdot J2 \cdot J3$
$K = K1 \cdot K2 \cdot K3$
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
H = high level, L = low level
Q_n = level of output Q at t_n
$\overline{Q}_n$ = complement of Q_n or level of output $\overline{Q}$ at t_n
Low input to preset sets Q to high level.
Low input to clear resets Q to low level.
Preset and clear are independent of clock.

description

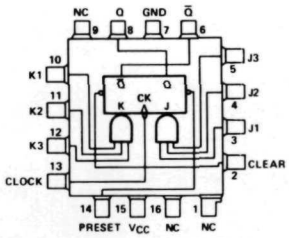
These edge-triggered flip-flop circuits feature gated J and K inputs and asynchronous preset and clear inputs. When the clock goes high, the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change while the clock pulse is high and the bistable will perform according to the truth table, provided that minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

The BL54L67Y chip is characterized for operation over the full military temperature range of −55°C to 125°C; the BL74L67Y is characterized for operation from 0°C to 70°C.

mechanical data



FORMAT 50



CHIP SHOWN
DIFFUSED SIDE DOWN

... Dynamic input activated by a transition from a high level to a low level.

NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

172

PRELIMINARY DATA SHEET: Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 21. Circuit Types BL54L67Y and BL74L67Y Schematic (Sheet 1 of 4)

CIRCUIT TYPES BL54L67Y, BL74L67Y
J-K EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L67Y Circuits . . . . . −55°C to 125°C
BL74L67Y Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	BL54L67Y			BL74L67Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{w(clock)}$	200			200			ns
Width of preset pulse, $t_{w(preset)}$	100			100			ns
Width of clear pulse, $t_{w(clear)}$	100			100			ns
Input setup time, t_{setup} (see Note 3)	30			30			ns
Input hold time, t_{hold} (see Note 4)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTES: 3. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.7	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA		−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any J or K	V_{CC} = MAX, V_I = 5.5 V		100	μA
		Preset, clear, or clock			200	
I_{IH}	High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Preset or clear			30	
		Clock			40	
I_{IL}	Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Preset or clear			−0.54	
		Clock			−0.72	
I_{OS}	Short-circuit output current‡		V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 5		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time.

NOTE 5: I_{CC} is measured with outputs open, clock grounded, and all other inputs at 4.5 V.

172

Figure 21. Circuit Types BL54L67Y and BL74L67Y Schematic (Sheet 2 of 4)

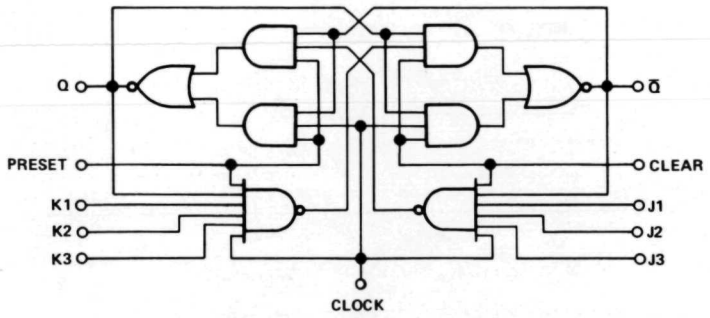
CIRCUIT TYPES BL54L67Y, BL74L67Y
J-K EDGE-TRIGGERED FLIP-FLOPS

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

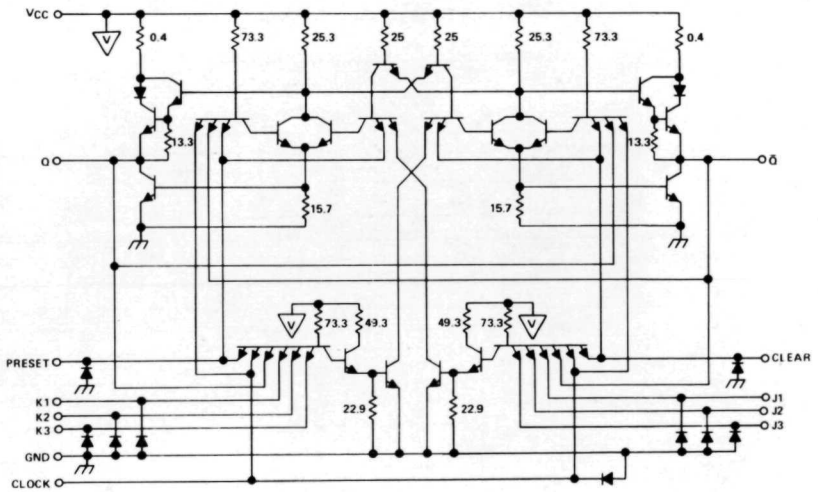
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			C_L = 50 pF,	R_L = 4 kΩ		10		MHz
t_{PLH}	Preset or clear	Q or $\overline{Q}$	C_L = 50 pF,	R_L = 4 kΩ		35	75	ns
t_{PHL}	Preset or clear	$\overline{Q}$ or Q	C_L = 50 pF,	$V_{I(clock)}$ = 2.4 V		60	150	ns
			R_L = 4 kΩ	$V_{I(clock)}$ = 0			200	
t_{PLH}	Clock	Q or $\overline{Q}$	C_L = 50 pF,	R_L = 4 kΩ	10	35	75	ns
t_{PHL}	Clock	Q or $\overline{Q}$	C_L = 50 pF,	R_L = 4 kΩ	10	60	150	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

functional block diagram



schematic

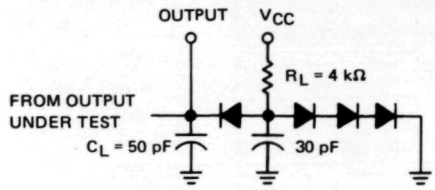


172

Figure 21. Circuit Types BL54L67Y and BL74L67Y Schematic (Sheet 3 of 4)

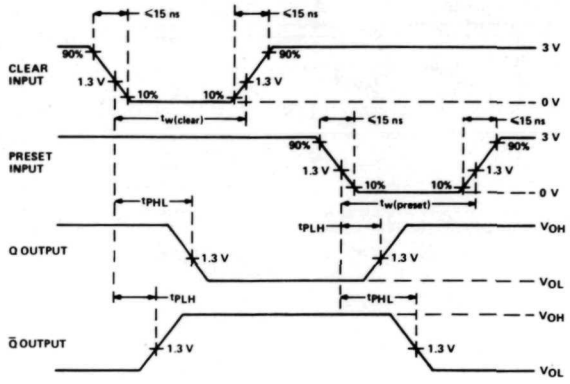
CIRCUIT TYPES BL54L67Y, BL74L67Y
J-K EDGE-TRIGGERED FLIP-FLOPS

PARAMETER MEASUREMENT INFORMATION

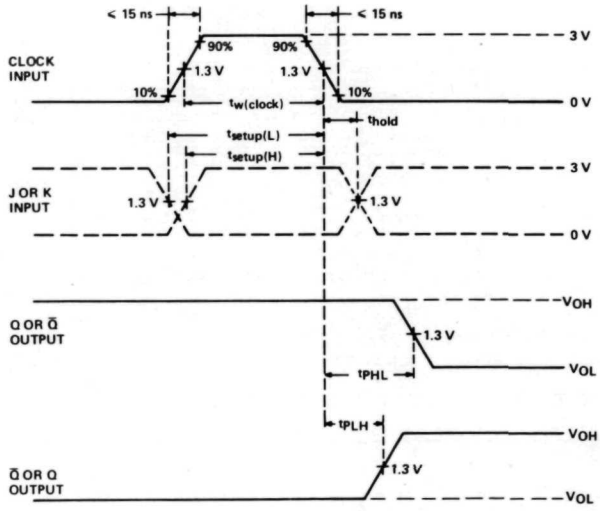


All diodes are 1N916
C_L includes probe and jig capacitance

LOAD CIRCUIT



SWITCHING TIMES FROM ASYNCHRONOUS INPUTS



SWITCHING TIMES FROM SYNCHRONOUS INPUTS

FIGURE 1

Figure 21. Circuit Types BL54L67Y and BL74L67Y Schematic (Sheet 4 of 4)

BEAM-LEAD LOW-POWER TTL CHIPS

CIRCUIT TYPES BL54L68Y, BL74L68Y DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

- **BL54L68Y/BL74L68Y Chips When Assembled Can Replace SN54L73/SN74L73 in Most Applications**
- **Silicon-Nitride-Sealed Junctions**
- **Gold Beams**
- **Available in Chip Form or as Part of a Complex Logic Assembly**
- **Diode-Clamped Inputs**

TRUTH TABLE

INPUTS AT t_n		OUTPUTS AT t_{n+1}	
J	K	Q	$\overline{Q}$
L	L	Q_n	$\overline{Q}_n$
L	H	L	H
H	L	H	L
H	H	$\overline{Q}_n$	Q_n

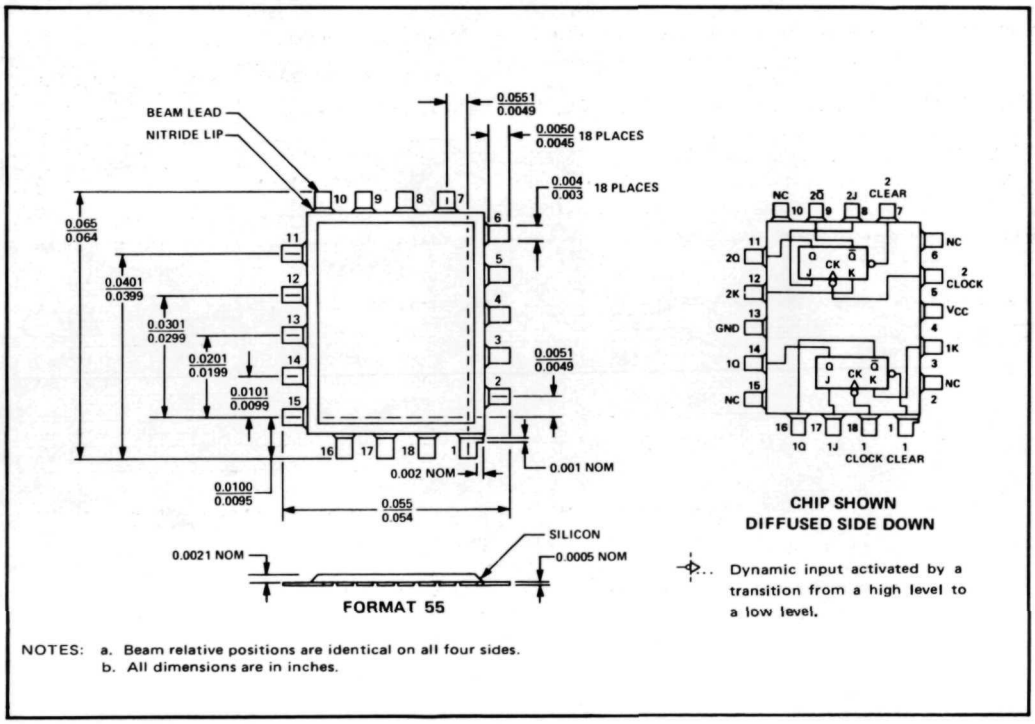
t_n = bit time before clock pulse
t_{n+1} = bit time after clock pulse
H = high level, L = low level
Q_n = level of output Q at t_n
$\overline{Q}_n$ = complement of Q_n or level of output $\overline{Q}$ at t_n
Low input to clear resets Q to low level.
Clear is independent of clock.

description

These edge-triggered dual flip-flop circuits feature individual J, K, clock, and asynchronous clear inputs to each flip-flop. When the clock goes high, the inputs are enabled and data will be accepted. The logic levels of the J and K inputs may be allowed to change while the clock pulse is high and the bistable will perform according to the truth table, provided that minimum setup and hold times are observed. Input data is transferred to the outputs on the negative-going edge of the clock pulse.

The BL54L68Y chip is characterized for operation over the full military temperature range of −55°C to 125°C; the BL74L68Y is characterized for operation from 0°C to 70°C.

mechanical data



NOTES: a. Beam relative positions are identical on all four sides.
b. All dimensions are in inches.

172

PRELIMINARY DATA SHEET:
Supplementary data may be published at a later date.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 22. Circuit Types BL54L68Y and BL74L68Y Schematic (Sheet 1 of 4)

CIRCUIT TYPES BL54L68Y, BL74L68Y
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)

Supply voltage, V_{CC} (see Note 1) . . . . . 8 V
Input voltage . . . . . 5.5 V
Interemitter voltage (see Note 2) . . . . . 5.5 V
Operating free-air temperature range: BL54L68Y Circuits . . . . . −55°C to 125°C
BL74L68Y Circuits . . . . . 0°C to 70°C
Storage temperature range . . . . . −65°C to 150°C

NOTES: 1. Voltage values are with respect to network ground terminal.
2. This is the voltage between two emitters of a multiple-emitter input transistor.

recommended operating conditions

	BL54L68Y			BL74L68Y			UNIT
	MIN	NOM	MAX	MIN	NOM	MAX	
Supply voltage, V_{CC}	4.5	5	5.5	4.75	5	5.25	V
Normalized fan-out from each output, N			10			10	
Width of clock pulse, $t_{w(clock)}$	200			200			ns
Width of clear pulse, $t_{w(clear)}$	100			100			ns
Input setup time, t_{setup} (see Note 3)	30			30			ns
Input hold time, t_{hold} (see Note 4)	0			0			ns
Operating free-air temperature, T_A	−55		125	0		70	°C

NOTES: 3. Setup time is the interval immediately preceeding the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its recognition.
4. Hold time is the interval immediately following the negative-going edge of the clock pulse during which interval the data to be recognized must be maintained at the input to ensure its continued recognition.

electrical characteristics over recommended operating free-air temperature range

PARAMETER			TEST CONDITIONS†	MIN	MAX	UNIT
V_{IH}	High-level input voltage			2		V
V_{IL}	Low-level input voltage				0.7	V
V_I	Input clamp voltage		V_{CC} = MIN, I_I = −8 mA		−1.5	V
V_{OH}	High-level output voltage		V_{CC} = MIN, I_{OH} = −100 μA	2.4		V
V_{OL}	Low-level output voltage		V_{CC} = MIN, I_{OL} = 2 mA		0.3	V
I_I	Input current at maximum input voltage	Any J or K	V_{CC} = MAX, V_I = 5.5 V		100	μA
		Clear, or clock			200	
I_{IH}	High-level input current	Any J or K	V_{CC} = MAX, V_I = 2.4 V		10	μA
		Clear			30	
		Clock			40	
I_{IL}	Low-level input current	Any J or K	V_{CC} = MAX, V_I = 0.3 V		−0.18	mA
		Clear			−0.54	
		Clock			−0.72	
I_{OS}	Short-circuit output current‡		V_{CC} = MAX	−3	−15	mA
I_{CC}	Supply current		V_{CC} = MAX, See Note 5		1.44	mA

†For conditions shown as MIN or MAX, use the appropriate value specified under recommended operating conditions for the applicable device type.
‡Not more than one output should be shorted at a time.

NOTE 5: I_{CC} is measured with outputs open, clocks grounded, and all other inputs at 4.5 V.

TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 22. Circuit Types BL54L68Y and BL74L68Y Schematic (Sheet 2 of 4)

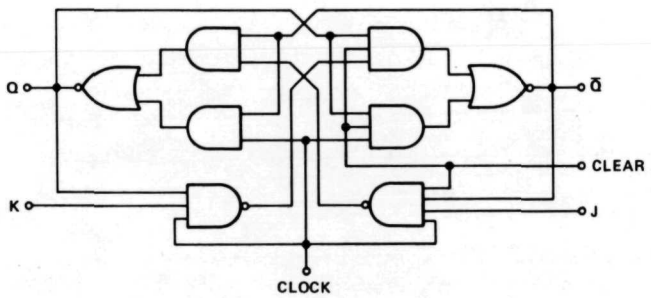
CIRCUIT TYPES BL54L68Y, BL74L68Y
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

switching characteristics, V_{CC} = 5 V, T_A = 25°C, N = 10, see figure 1

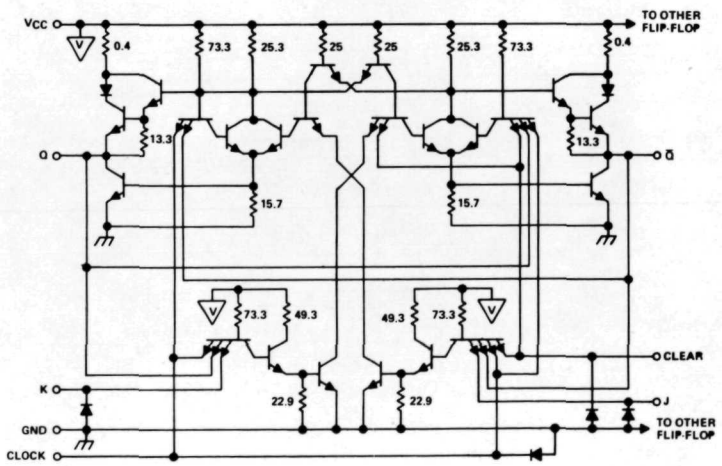
PARAMETER§	FROM (INPUT)	TO (OUTPUT)	TEST CONDITIONS		MIN	TYP	MAX	UNIT
f_{max}			C_L = 50 pF,	R_L = 4 kΩ		10		MHz
t_{PLH}	Clear	$\overline{Q}$	C_L = 50 pF,	R_L = 4 kΩ		35	75	ns
t_{PHL}	Clear	Q	C_L = 50 pF, R_L = 4 kΩ	$V_{I(clock)}$ = 2.4 V		60	150	ns
				$V_{I(clock)}$ = 0			200	
t_{PLH}	Clock	Q or $\overline{Q}$	C_L = 50 pF,	R_L = 4 kΩ	10	35	75	ns
t_{PHL}	Clock	Q or $\overline{Q}$	C_L = 50 pF,	R_L = 4 kΩ	10	60	150	ns

§ f_{max} ≡ maximum clock frequency
t_{PLH} ≡ propagation delay time, low-to-high-level output
t_{PHL} ≡ propagation delay time, high-to-low-level output

functional block diagram (each flip-flop)



schematic (each flip-flop)

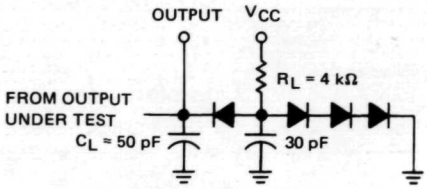


TEXAS INSTRUMENTS
INCORPORATED
POST OFFICE BOX 5012 • DALLAS, TEXAS 75222

Figure 22. Circuit Types BL54L68Y and BL74L68Y Schematic (Sheet 3 of 4)

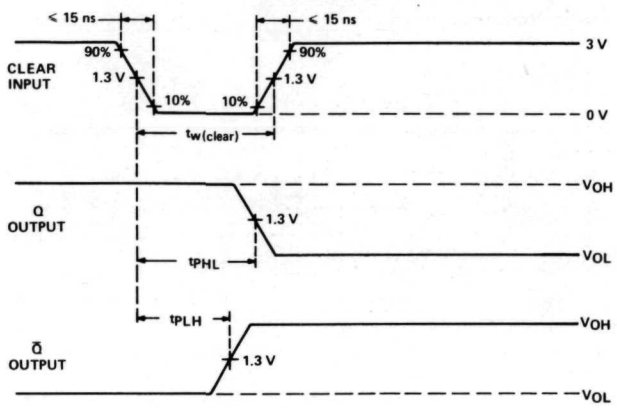
CIRCUIT TYPES BL54L68Y, BL74L68Y
DUAL J-K EDGE-TRIGGERED FLIP-FLOPS

PARAMETER MEASUREMENT INFORMATION

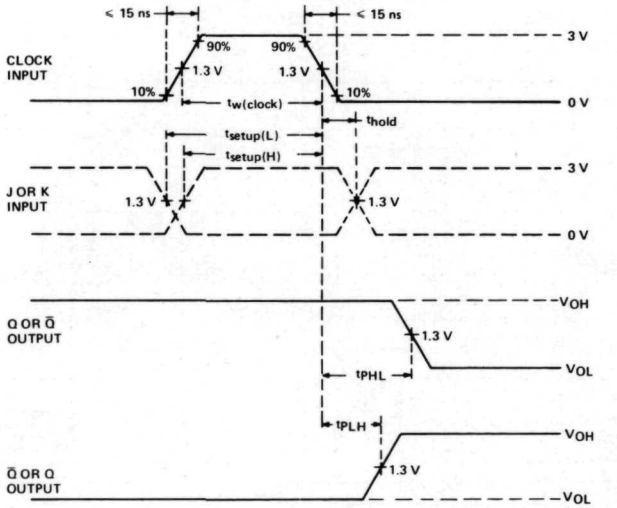


All diodes are 1N916.
C_L includes probe and jig capacitance.

LOAD CIRCUIT



SWITCHING TIMES FROM CLEAR INPUT



SWITCHING TIMES FROM SYNCHRONOUS INPUTS
FIGURE 1

Figure 22. Circuit Types BL54L68Y and BL74L68Y Schematic (Sheet 4 of 4)

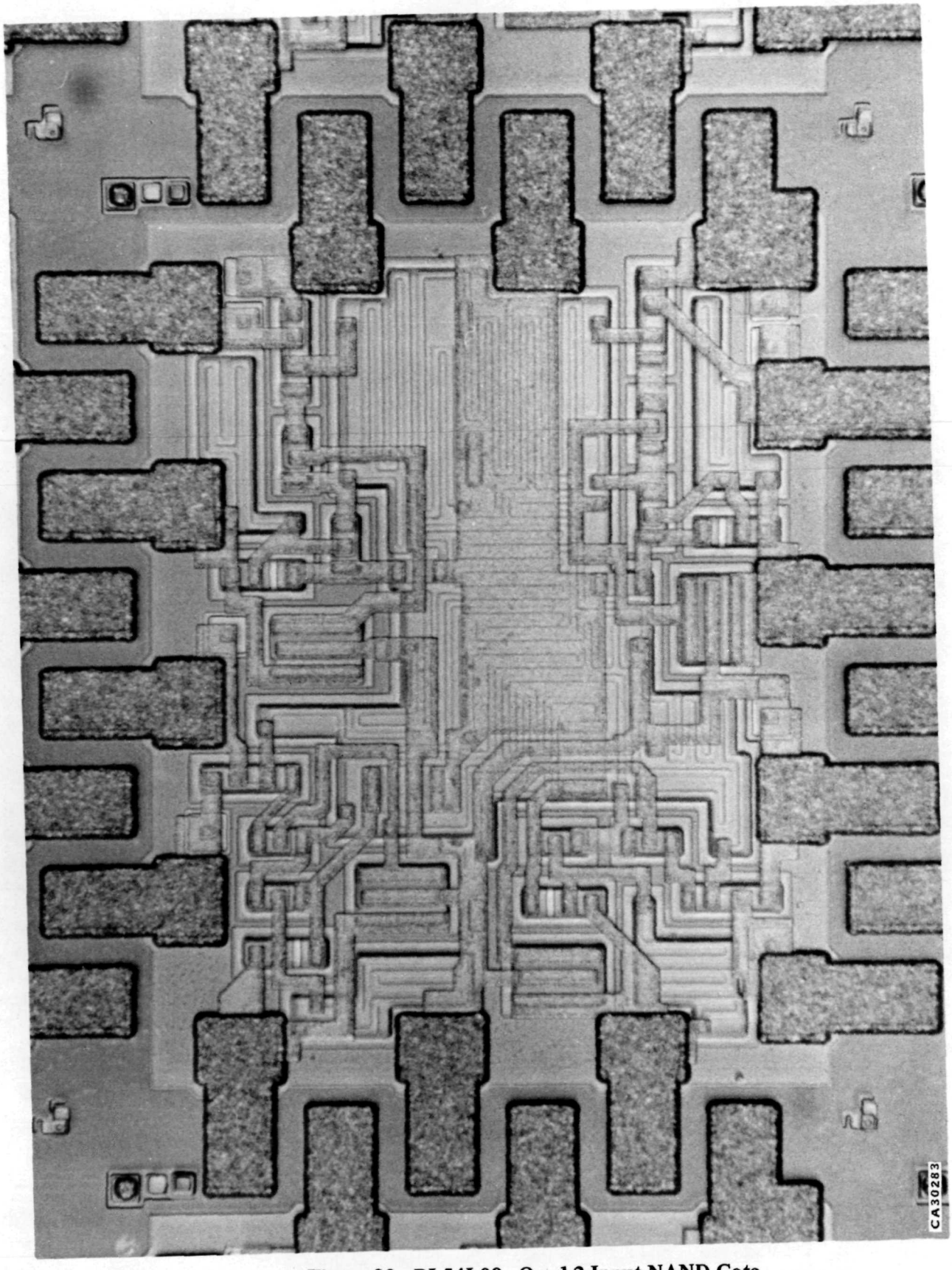


Figure 23. BL54L00–Quad 2-Input NAND Gate

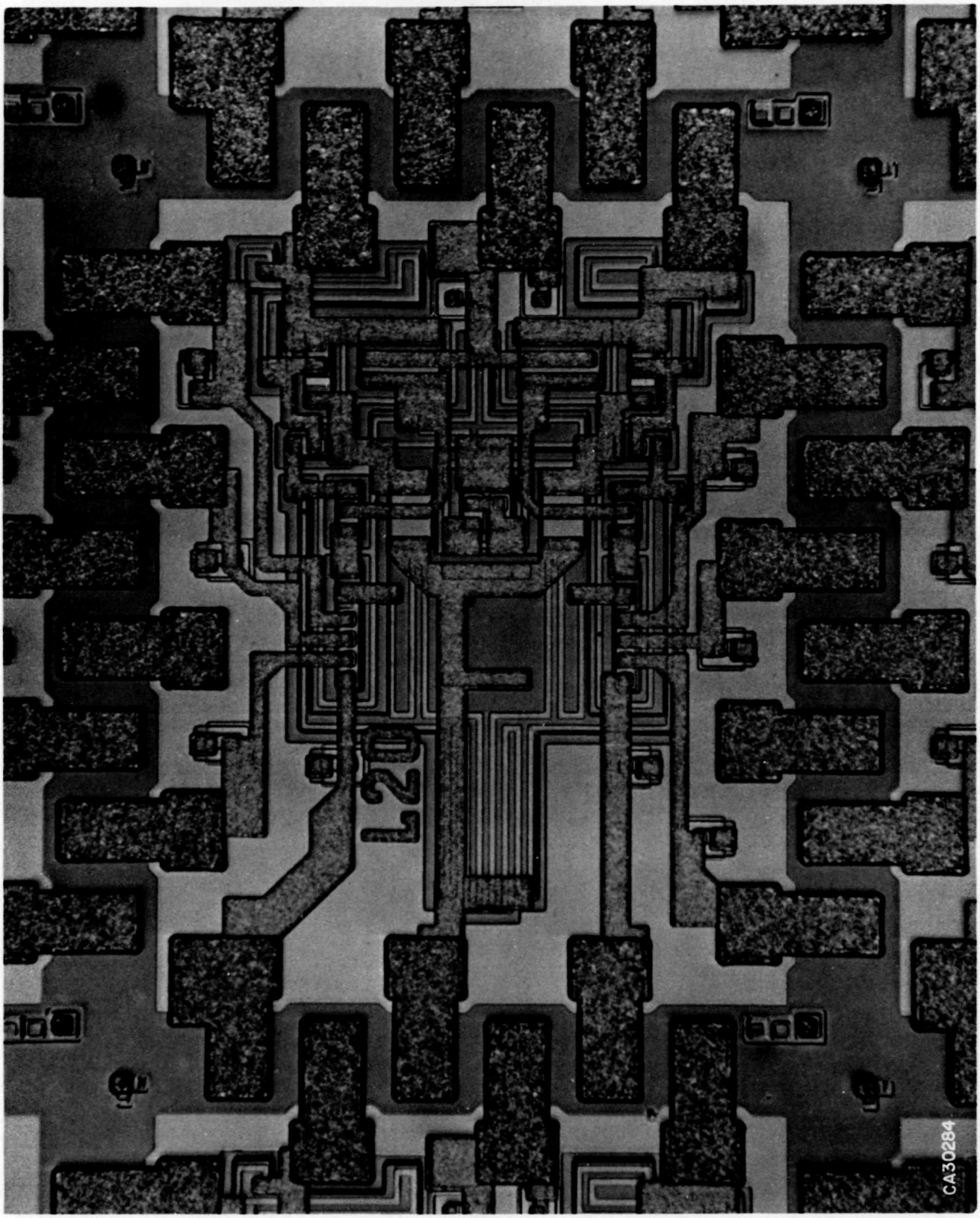


Figure 24. BL54L20–Dual 4-Input NAND Gate

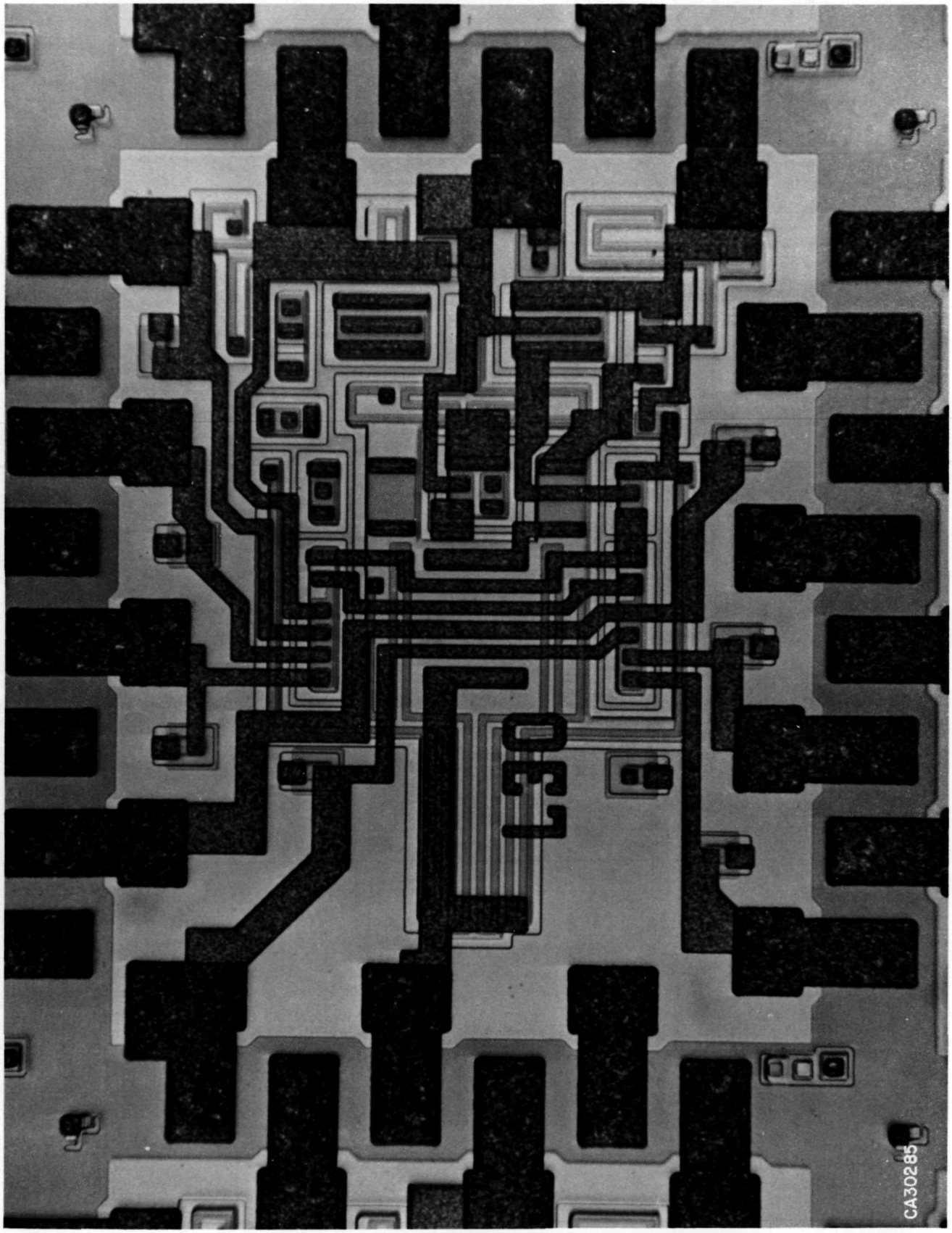


Figure 25. BL54L30–Single 8-Input NAND Gate

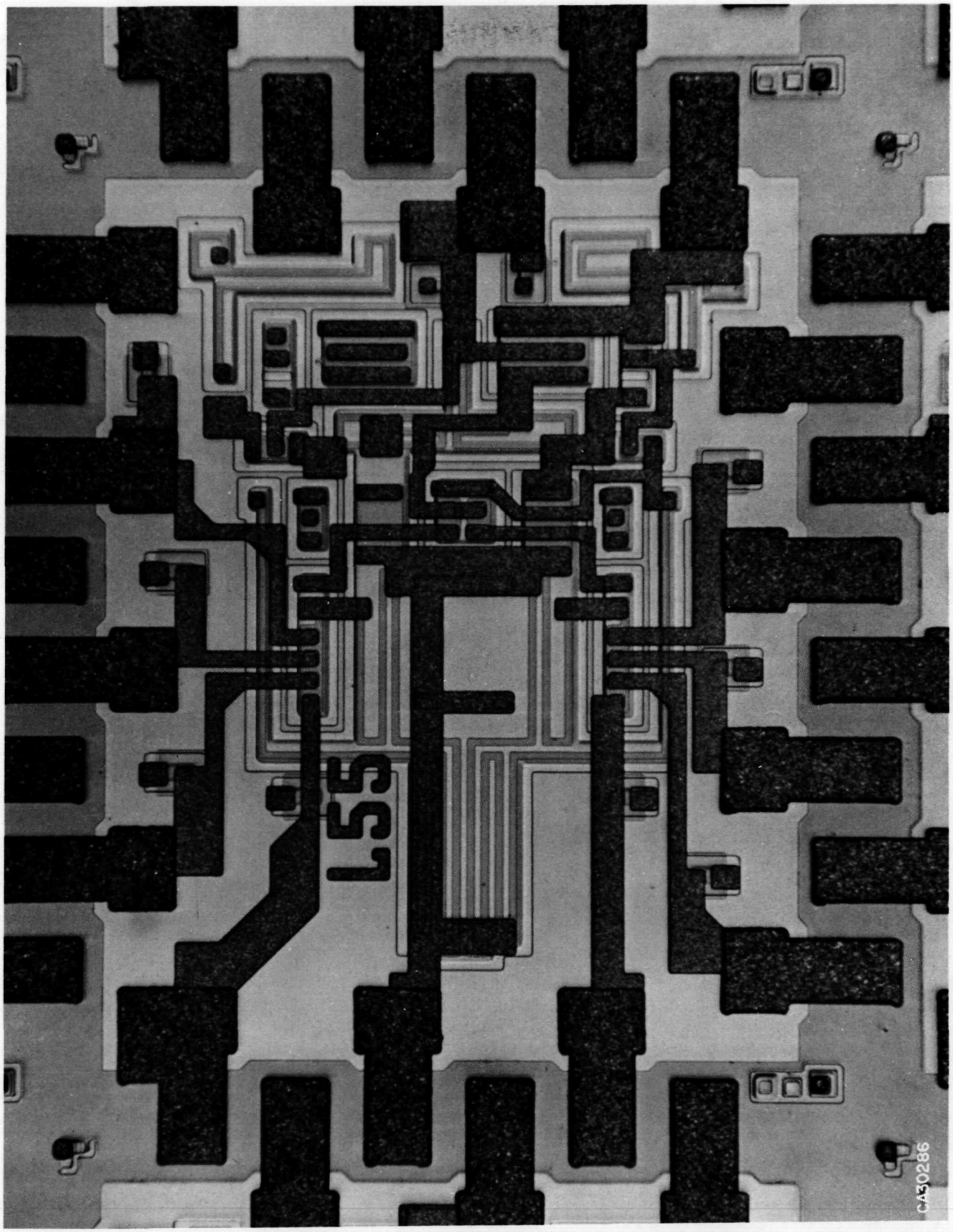


Figure 26. BL54L55–Two-Wide 4-Input AND-OR-INVERT

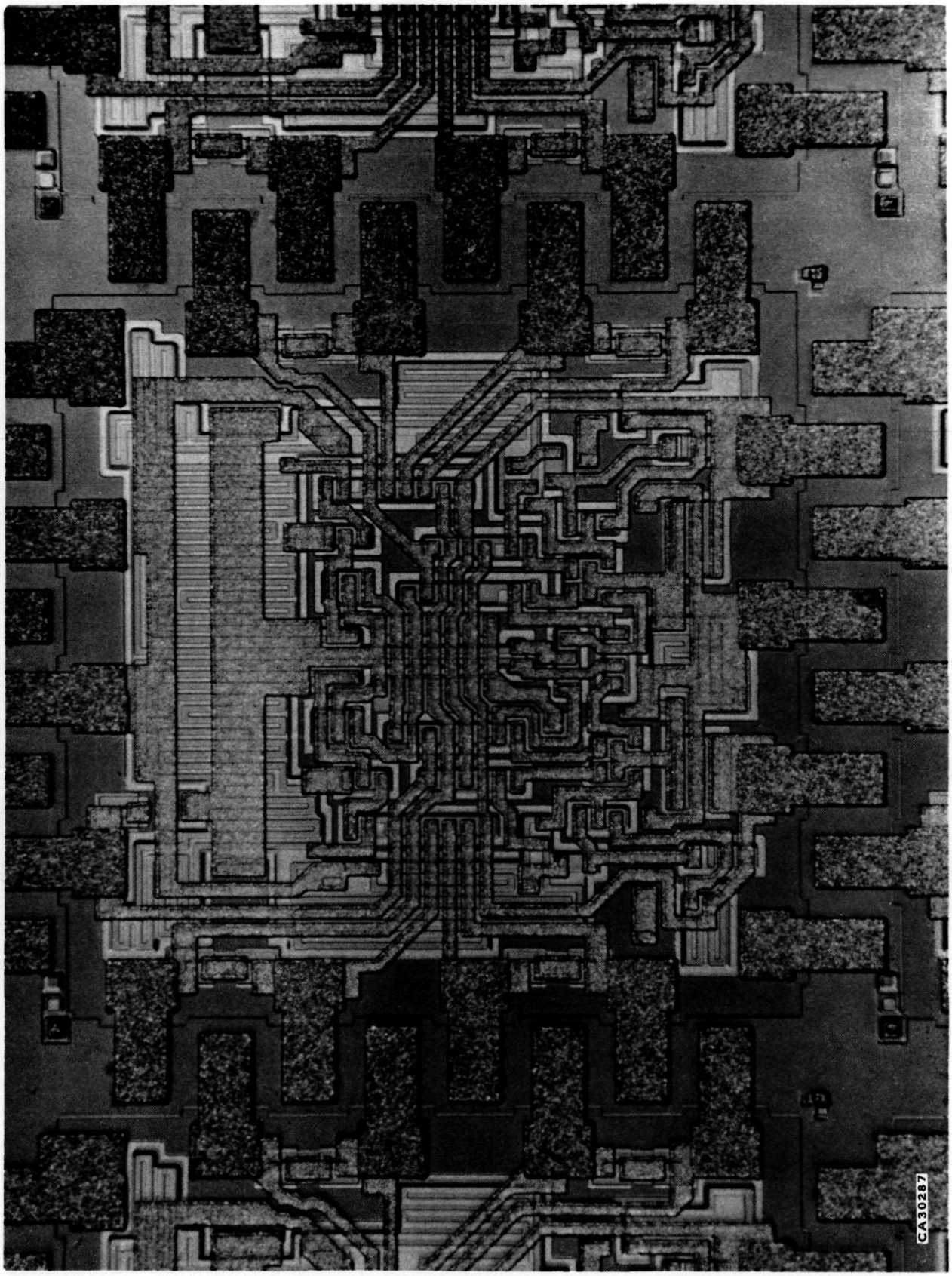


Figure 27. BL54L67—J-K Flip-Flop

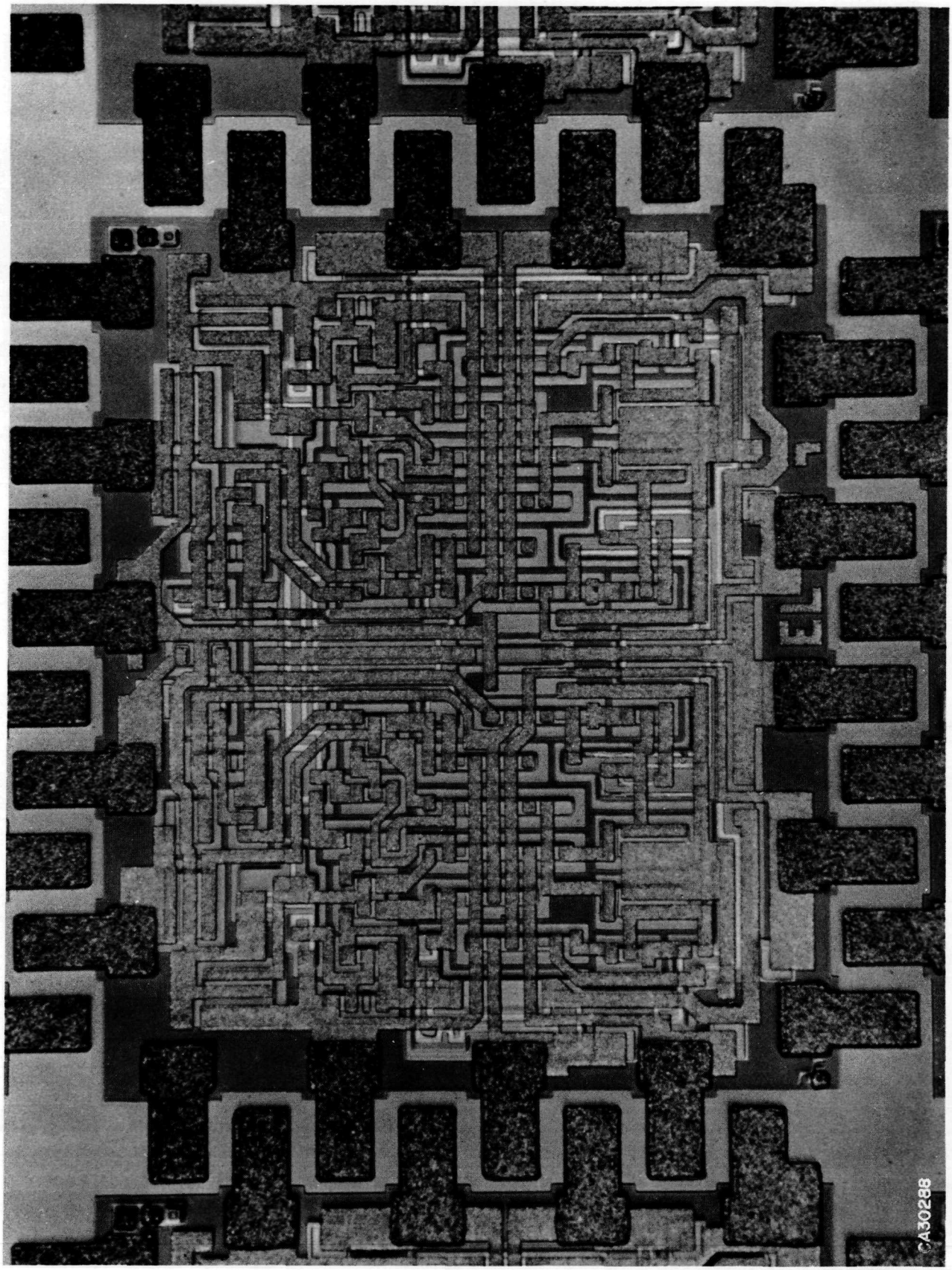


Figure 28. BL54L68—Dual J-K Flip-Flop