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Methods of Measurement for Semiconductor Materials, Process Control, and Devices

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January 1 to March 31, 1972

Methods of Measurement for Semiconductor Materials, Process Control, and Devices

Quarterly Report, January 1 to March 31, 1972

W. Murray Bullis, Editor

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Washington, D.C. 20234

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FOREWORD

The Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices was undertaken in 1968 to focus NBS efforts to enhance the performance, interchangeability, and reliability of discrete semiconductor devices and integrated circuits through improvements in methods of measurement for use in specifying materials and devices and in control of device fabrication processes. These improvements are intended to lead to a set of measurement methods which have been carefully evaluated for technical adequacy, which are acceptable to both users and suppliers, which can provide a common basis for the purchase specifications of government agencies, and which will lead to greater economy in government procurement. In addition, such methods will provide a basis for controlled improvements in essential device characteristics, such as uniformity of response to radiation effects.

The Program is supported by the National Bureau of Standards,[*] the Defense Nuclear Agency,[†] the U.S. Navy Strategic Systems Project Office,[§] the U.S. Navy Electronics Systems Command,[+] the Air Force Weapons Laboratory,[¶] the Air Force Cambridge Research Laboratories,[#] the Advanced Research Projects Agency,[×] the Atomic Energy Commission,[**] and the National Aeronautics and Space Administration.[††] Although there is not a one-to-one correspondence between the tasks described in this report and the cost centers through which the Program is supported, the concern of certain sponsors with specific parts of the program is reflected in planning and conduct of the work.

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[*] Through Research and Technical Services Cost Centers 4251126, 4251127, 4252128, and 4254115.

[†] Through Order EA072-810. (NBS Cost Center 4259522).

[§] Administered by U.S. Naval Ammunition Depot, Crane, Indiana through Project Orders PO-2-0023 and PO-2-0054. (NBS Cost Center 4259533).

[+] Through Project Order PO-2-1034. (NBS Cost Center 4252534).

[¶] Through Delivery Order F29601-71-F-0002. (NBS Cost Center 4252535).

[#] Through Project Order Y72-873. (NBS Cost Center 4251536).

[×] ARPA Order 1889 Monitored by Space and Missile Systems Organization under MIPR FY76167100331. (NBS Cost Center 4254422).

[**] Division of Biology and Medicine. (NBS Cost Center 4254425).

[††] Through Order S-70003-G, Goddard Space Flight Center. (NBS Cost Center 4254429).

METHODS OF MEASUREMENT FOR SEMICONDUCTOR MATERIALS, PROCESS CONTROL, AND DEVICES

QUARTERLY REPORT
JANUARY 1 TO MARCH 31, 1972

This quarterly progress report, fifteenth of a series, describes NBS activities directed toward the development of methods of measurement for semiconductor materials, process control, and devices. Significant accomplishments during this reporting period include development of a procedure to correct for the substantial differences of transistor delay time, a device characteristic frequently used as a screen in radiation hardness assurance tests, as measured with different instruments or with the same instrument at different frequencies; association of infrared response spectra of poor quality germanium gamma-ray detectors with spectra of detectors fabricated from portions of a good crystal that had been degraded in known ways; and confirmation of the excellent quality and cosmetic appearance of ultrasonic bonds made with aluminum ribbon wire. Work is continuing on measurement of resistivity of semiconductor crystals; study of gold-doped silicon; development of the infrared response technique; evaluation of wire bonds and die attachment; and measurement of thermal properties of semiconductor devices, delay time and related carrier transport properties in junction devices, and noise properties of microwave diodes. Supplementary data concerning staff, standards committee activities, technical services, and publications are included as appendixes.

Key Words: Aluminum wire; base transit time; carrier lifetime; die attachment; electrical properties; epitaxial silicon; gamma-ray detectors; germanium; gold-doped silicon; infrared response; methods of measurement; microelectronics; microwave diodes; nuclear radiation detectors; probe techniques (a-c); resistivity; ribbon wire bonding; semiconductor devices; semiconductor materials; semiconductor process control; silicon; thermal resistance; thermographic measurements; ultrasonic bonding; wire bonds.

1. INTRODUCTION

This is the fifteenth quarterly report to the sponsors of the Joint Program on Methods of Measurement for Semiconductor Materials, Process Control, and Devices. It summarizes work on a wide variety of measurement methods that are being studied at the National Bureau of Standards. Since the Program is a continuing one, the results and conclusions reported here are subject to modification and refinement.

INTRODUCTION

The work of the Program is divided into a number of tasks, each directed toward the study of a particular material or device property or measurement technique. This report is subdivided according to these tasks. Highlights of activity during the quarter are given in section 2. Section 3 deals with tasks on methods of measurement for materials; section 4, with those on methods of measurement for process control; and section 5, with those on methods of measurement for devices. References for each section are listed in a separate subsection at the end of that section.

The report of each task includes the long-term objective, a narrative description of progress made during this reporting period, and a listing of plans for the immediate future. Additional information concerning the material reported may be obtained directly from individual staff members connected with the task as indicated throughout the report. The organization of the Joint Program staff and telephone numbers are listed in Appendix A.

An important part of the work that frequently goes beyond the task structure is participation in the activities of various technical standardizing committees. The list of personnel involved with this work given in Appendix B suggests the extent of this participation. Additional details of current standardization activities not associated with a particular task are given in section 2.

Background material on the Program and individual tasks may be found in earlier reports in this series as listed in Appendix D. From time to time, publications are prepared that describe some aspect of the program in greater detail. Current publications of this type are also listed in Appendix D. Reprints or copies of such publications are usually available on request to the author.

2. HIGHLIGHTS

Significant accomplishments during this reporting period include development of a procedure to correct for the substantial differences of transistor delay time, a device characteristic frequently used as a screen in radiation hardness assurance tests, as measured with different instruments or with the same instrument at different frequencies; association of infrared response spectra of poor quality germanium gamma-ray detectors with spectra of detectors fabricated from portions of a good crystal that had been degraded in known ways; and confirmation of the excellent quality and cosmetic appearance of ultrasonic bonds made with aluminum ribbon wire. Highlights of these and other technical activities are presented in this section; details are given in subsequent sections of the report. This section concludes with a summary of standardization activities not associated with a specific task being carried out by program staff members.

Resistivity — Principal effort was concentrated on study of the capacitance-voltage method; detailed investigations of the discrepancies between results obtained with this and the four-probe method were initiated with experimental study of the influence of series resistance on the capacitance measurement. An instrument was designed and constructed to measure the loading of the probes in a four-probe array. Standardization efforts undertaken in cooperation with ASTM Committee F-1 on Electronics included completion of preliminary analysis of the interlaboratory test of measurement of the resistivity of epitaxial layers by the four-probe method. Work continued on development of procedures for analysis of the results obtained to date in the study of current and probe-force dependence of the four-probe method.

Gold-Doped Silicon — The model which includes a gold-related shallow acceptor state was used successfully to predict the dependence of resistivity on gold concentration in p-type silicon of both higher and lower resistivity than had been studied previously and, at high gold concentrations, in initially n-type silicon. In the study of the properties of interstitial gold, electrical measurements on specimens diffused with gold for very short times at high temperatures gave results similar to those on specimens with the same gold concentration obtained from longer diffusions at lower temperatures. This result can be explained even though the electrical properties of substitutional and interstitial gold are dissimilar if it is assumed that the rate for the conversion of interstitial to substitutional gold is rapid compared with the diffusion time. Investigation of diode recovery methods for measuring carrier lifetime was resumed. Preliminary results suggest that the previously observed differences in lifetime as determined by the reverse recovery and open circuit voltage decay methods may arise because of variations in the dependence of the storage-time-to-lifetime ratio on the forward-to-reverse-current ratio in the reverse recovery method.

HIGHLIGHTS

Infrared Methods — Study of infrared response (IRR) spectra obtained from lithium-drifted germanium detectors showed that spectra observed to date can be grouped into five types: one representative of good quality detectors and four representative of poor quality detectors. Three of the latter have been matched by spectra from diodes fabricated from a good quality crystal that had been degraded in a known manner. Th substantial progress has been made in identifying the causes of poor crystal quality from IRR spectra.

Die Attachment Evaluation — Analysis of heat flow to determine the limitations of the thermal response technique for detecting poor die adhesion in semiconductor devices continued. Curves were generated from which a lower limit of the transient thermal response normalized to heating power needed for maximum sensitivity to voids in the die attachment of semiconductor devices can be determined. It was also established that the thermal response technique is relatively insensitive to voids that are located in areas laterally removed from the junction used to sense the chip temperature. Initial experiments to apply the transient thermal response technique to transistors with poor die adhesion indicated that the transistors could be operated in a diode mode with the collector shorted to the base without exceeding the current handling limitations of the base lead and metallization.

Wire Bond Evaluation — In the continuing study of ultrasonic bonding of aluminum ribbon wire, pull strength measurements were made on magnesium-doped wire. The results confirmed the previous work on silicon-doped wire in which the use of a bonding schedule with longer time and lower power than normally used resulted in increased bond strength and improved cosmetic appearance. Measurements of pull strength of single-level round wire bonds as a function of pulling hook position were repeated on several different substrates. In all tests, the second bond was epoxied so that the dominant failure mode was rupture at the heel of the first bond. There was considerable variability in pull strength exhibited by groups of bonds on different substrates, although the changes in pull strengths with hook position, normalized to that found at the center position of the pulling hook, were, in each case, in agreement with those calculated by resolution of forces. Calculations showed that the temperature distribution in a transistor bond loop under conditions of slow thermal cycling is lin[illegible] rather than exponential as heretofore assumed. Recalculation of flexure as a function of loop height yielded small but detectable changes from the original calculations. A considerable effort during the quarter was directed toward standardization activities and dissemination of information on wire bonding and bond evaluation.

Thermal Properties of Devices — Work continued to determine the origins of the frequently observed difference between the straight line extrapolation to zero power

of the measured value of the temperature sensitive parameter as a function of power and the d-c calibration value at the zero power level. Work on diodes and diode-connected transistors indicated that the cause might lie partially in the charge distribution disturbance caused by switching off the collector voltage when measuring thermal resistance. Measurements made by switching only the emitter suggested that this method yields values of junction temperature that are more nearly the same as the values measured with an infrared microradiometer than are values measured by switching both the emitter and the collector. Work also continued in the investigation of the physical mechanisms of thermal hysteresis, the temperature and current density dependence of common-emitter current gain, h_{FE}, and hot-spot initiation and stabilization. It was found that in an area of sharp hot-spot formation the temperature sensitivity of h_{FE} was greater at lower collector currents than at higher collector currents and that h_{FE} was also larger at hot-spot formation at lower currents than at hot-spot formation at higher currents. These observations are in accord with the need for greater power to form current constrictions as collector current is increased.

Microwave Device Measurements — Several changes have been made in the X-band mixer measurement system in order to improve the repeatability of the incremental conversion loss measurement, and to allow the direct measurement, without calculation, of the mixer i-f output conductance by a load perturbation method that also uses the mixer output voltage change resulting from the incremental modulation. Several factors have been suspected of causing the lack of repeatability: mechanical changes in the waveguide system due to forces used in changing diodes, drifts in microwave power or other system characteristics due to temperature or line voltage changes or to aging of components, diode-to-holder contact imperfection, and changes in the diodes themselves due to mechanical shock (moving the whisker) or to temperature changes. Each factor is being examined independently.

Carrier Transport in Junction Devices — A general approach has been developed for determining the location and magnitude of delay-time error-producing sources arising from extraneous pickup at the measurement frequency, and this approach has been tested by applying it to the NBS model of the Sandia bridge. With these sources so characterized, their influence on subsequent transistor measurements can be reduced greatly. The results of this work can explain previously observed differences in measurements of delay time of transistors. Several preliminary steps have been taken toward an interlaboratory comparison of transistor scattering-parameter measurements. Measurements were made as a function of frequency with various bias conditions for three transistor types, the effects of case temperature on the S-parameters were determined qualitatively, the equation widely used to relate h_{fe} to

S-parameters was verified, and the S-parameters of an R-C network on a transistor header were measured to determine its suitability for use as a calibration standard.

Standardization Activities — Many of the standardization activities undertaken by program staff are broader than the technical tasks described in the following sections. These activities involve general staff support in committees, liaison between committees, coordination of efforts which may encompass a variety of tasks, and participation in areas where no direct in-house technical effort is underway. Standardization activities directly related to particular task areas are reported with the appropriate tasks.

Nine program staff members attended the regular winter meeting of ASTM Committee F-1 on Electronics in New Orleans. Three staff members chaired section meetings; the Interconnection Bonding Section continued to show vitality with 40 attendees representing 31 organizations (see section 4.2.). Documents on methods of measuring carrier lifetime by photoconductive decay and by surface photovoltage were presented to the Lifetime Section. The previously prepared draft procedure, for measuring thickness of thin oxide and metal layers (NBS Tech. Note 475, p. 24) was discussed by the Dielectrics Section; with only minor revisions the document is being used as the basis of a round robin test coordinated by a program staff member.

The modified collaborative reference program to provide silicon wafer resistivity standards (NBS Tech. Notes 717, p. 7, and 727, p. 8) was described to the F-1 Advisory Committee. The manner and extent to which this program is carried out is contingent on the response of the Committee. Other standards work on resistivity methods is reported in section 3.1.

A request from the Defense Nuclear Agency for assistance by Committee F-1 in the development of standard methods of measurement in support of assurance of radiation hardness of semiconductor devices was presented to the F-1 Advisory Committee. The Committee expressed its interest in this work and its intent to expand the activities of Committee F-1 to include it.

As a result of discussions and interest by the Hermeticity Section, the helium mass spectrometer leak test procedure was further modified and extended. Procedures were developed for determining the limits of leak size for which the test is applicable; these are particularly significant for large volume packages, such as those of hybrid microcircuits, which cannot be subjected to high pressures. In addition, a go, no-go test was included explicitly in the procedure.

After the F-1 meeting, four documents were edited at the committee level.

HIGHLIGHTS

Most activity in connection with EIA-JEDEC Committees was in the thermal measurements area (see section 5.1.). In addition extensive comments were made on the Proposed Standard for the Measurement of Small-Signal Transistor Scattering Parameters, being prepared by Task Group 5 of Committee JC-24 on Low Power Transistors.

A program staff member attended the Second Conference on the Definition of Pressing Problems and Projected National Needs in Radiometry and Photometry at NBS in February. This group, now known as the Council for Optical Radiation Measurements (CORM), includes within its scope standards for emission from light emitting diodes. This important area is of considerable relevance to semiconductor device users; close liaison is being maintained with CORM.

A new group concerned with assembly and testing of components intended for non-military applications has been established in the IEEE Manufacturing Technology Group. A program staff member attended a meeting of this group in March; continuing liaison is expected to provide both identification of serious problem areas for program planning considerations and a forum for getting results of the work to the industry.

3. SEMICONDUCTOR MATERIALS

3.1. RESISTIVITY

Objective: To develop methods suitable for use throughout the electronics industry for measuring resistivity of bulk, epitaxial, and diffused silicon wafers.

Progress: Principal effort was concentrated on study of the capacitance-voltage method; detailed investigations of the discrepancies between results obtained with this and the four-probe method were initiated with experimental study of the influence of series resistance on the capacitance measurement. An instrument was designed and constructed to measure the loading of the probes in a four-probe array. Standardization efforts undertaken in cooperation with ASTM Committee F-1 on Electronics included completion of preliminary analysis of the interlaboratory test of measurement of the resistivity of epitaxial layers by the four-probe method. Work continued on development of procedures for analysis of the results obtained to date in the study of current and probe-force dependence of the four-probe method.

Standardization Activities — Lower order polynomial curve fit approximations to the temperature coefficient for silicon resistivity (NBS Tech. Note 727, pp. 7-8) were presented for discussion at the January meeting of the Resistivity Section of ASTM Committee F-1. The consensus favored the higher order curve fits previously reported (NBS Tech. Note 560, pp. 6-7) which cover the entire range of resistivity. In response to a request by the section, work was initiated on the development of tables derived from these polynomials which are suitable for linear interpolation.

(J. R. Ehrstein)

The round-robin experiment to determine interlaboratory precision of four-probe measurements of the resistivity of silicon epitaxial wafers deposited on opposite conductivity type substrates being conducted in cooperation with ASTM Committee F-1 has been completed by five of the nine participating laboratories. Measurements are being made on each of six specimens at a single specified current level and probe loading and on three resistance boxes each containing a standard resistor and, in each of the four measuring arms, a resistor of value 2000 times that of the standard. Preliminary analysis of the data summarized in table 1 suggests that the variability in this test is substantially smaller than that observed in similar earlier experiments.

(F. H. Brewer)

Measurements were made as part of a round-robin experiment on capacitance-voltage (C-V) measurements in cooperation with ASTM Committee F-1. Measurements of capacitance as a function of voltage and measurements of device area were made on two diodes on each of five epitaxial specimens. In addition the capacitance of four reference capacitors was measured.

(R. L. Mattis)

Table 1 — Preliminary Results of Multilaboratory Test of Four-Probe Method for Epitaxial Resistivity Measurement[a]

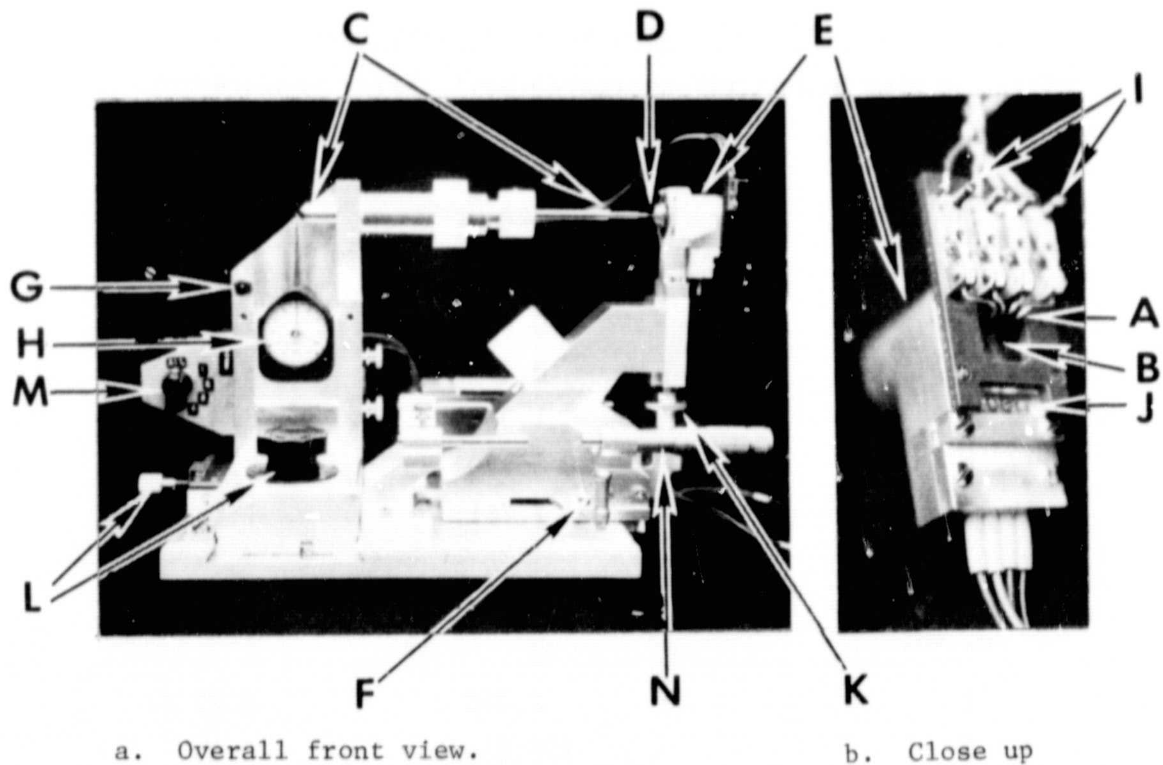
Specimen No.	Type	$\bar{\rho}$ [b]	s [c]
1a	p/n	13.33 Ω·cm	3.44 %
2	p/n	0.8879	3.03
3a	p/n	0.4473	3.49
4	n/p	1.336	3.73
5	n/p	0.1494	0.93
6	n/p	7.761	1.53

Resistor Box No.	$\bar{R}$ [d]	s [c]
1	2.010 Ω	0.27 %
2	100.01	0.01
3	998.77	0.31

[a] Five laboratories reporting
[b] Multilaboratory resistivity grand average
[c] Relative sample standard deviation
[d] Multilaboratory resistance grand average

Probe Loading — Although it is necessary to control the probe loading when measuring the resistivity of silicon with a four-probe array, no standard procedures exist at present to measure or adjust the loading force. In response to the need for such procedures, an instrument has been designed and built to facilitate the measurement and adjustment of the tensioning springs which are used to load the probe tips. The instrument, pictured in figure 1, was designed to minimize two significant sources of error in such measurements: friction in parts linking the probe tips to the force gage and inaccuracy in simulating the working position of the probe tips while measuring the spring tension. Recirculating bearing sleeves to reduce friction in the push rod assembly and a set of electrical contacts to sense the position of the probe points were employed.

To adjust the instrument, the position locator tips (A) are set so that they just touch the tensioning springs (B) when the probes are depressed to their working position. To measure the probe loading, the push rod (C) is lined up with a probe



a. Overall front view. b. Close up

A Position Locator Tips
B Probe Tensioning Springs
C Push Rod
D Probe Tips
E Probe Assembly
F Operator Lever
G Indicator Light
H Dynamometer Force Gage
I Position Locator Adjustment Screws
J Probe Tensioning Spring Adjustment Screws
K Vertical Position Adjustment
L Horizontal Position Adjustments
M Position Locator Tip Selector Switch
N Reference Position Indicator (for test purposes only)

Figure 1. Instrument for measuring loading force on tips of four-probe array with close up of the probe assembly and probe position locator mechanism.

tip (D) and the probe assembly (E) is advanced against it by means of the operating lever (F) until the light (G) goes on, indicating that the probe is depressed to its working position, and the probe loading is read from the force gage (H). Tests are now being run to characterize the operation of the instrument.

(F. H. Brewer and G. P. Spurlock)

Capacitance-Voltage Methods — Efforts were directed toward investigation of the causes of observed differences between doping density values deduced from four-probe resistivity measurements and doping density *vs*. depth profiles measured by the C-V method. The failure of the C-V doping density profile to reach a plateau and the

consistently lower doping density measured by the C-V method were discussed previously (NBS Tech. Note 727, pp. 9-10).

In the first phase of the study the specimen was considered to be composed of a two-element network consisting of a contact resistance R in series with the depletion capacitance C. Such a network is equivalent to a capacitance C' in parallel with a resistance R'. To measure R a previously profiled diode from each of the six slices which had been profiled was measured as a function of bias voltage using a capacitance bridge. The bridge measures C' and R' whereas the meter which is normally used measures only capacitance. The values of C' and R' measured by the bridge were transformed into the equivalent series capacitance and resistance, C and R. The capacitance values were altered only slightly in this transformation. The transformed equivalent R values for the six diodes ranged from 48 to 778 Ω and were constant as a function of bias voltage within about ±15 percent for five of the six specimens. The fact that for a given diode the transformed R value is relatively constant with bias voltage suggests that the two-element model which was selected represents a reasonably good approximation to the actual specimen behavior. That this series contact resistance is the only significant resistive component that needs to be included in the model is also borne out by the fact that parallel leakage resistance calculated from the measurement of applied reverse bias and the reverse leakage current is typically tens or hundreds of megohms as compared with a capacitive reactance at 1 MHz associated with the depletion capacitance for the six specimens of from 2.6 to 300 kΩ.

In the second phase of the study the effect of the series resistance on measurements made with the capacitance meter which is normally used in the C-V work was considered. A low-leakage standard capacitor was measured over a range of values with series resistances, R_{ser}, of 10, 30, 100, 300, and 1000 Ω. The capacitance measured by the meter was significantly less than the standard capacitor value on many readings taken with R_{ser} equal to 300 and 1000 Ω. These resistance values overlap the range of actual resistances R which have been encountered in the diodes. Results are shown in figure 2 for R_{ser} of 100, 300, and 1000 Ω. For smaller R_{ser} and for capacitance 300 pF or less the difference between the measured capacitance and the actual value was always less than 2 percent. Since the doping density is approximately proportional to C^2, low capacitance readings in the presence of series resistance lead to an erroneously low doping density such as has been observed in comparison with four-probe data. With reference to figure 2, the difference is observed to be a function of capacitance with a minimum around 10 to 30 pF. If diodes behave similarly to the series R-C circuit, such an effect would lead, on uniformly doped specimens, to measured doping density profiles which are either increasing or decreasing depending on whether the capacitance values in the C-V data were greater than or less than the capacitance at which the minimum

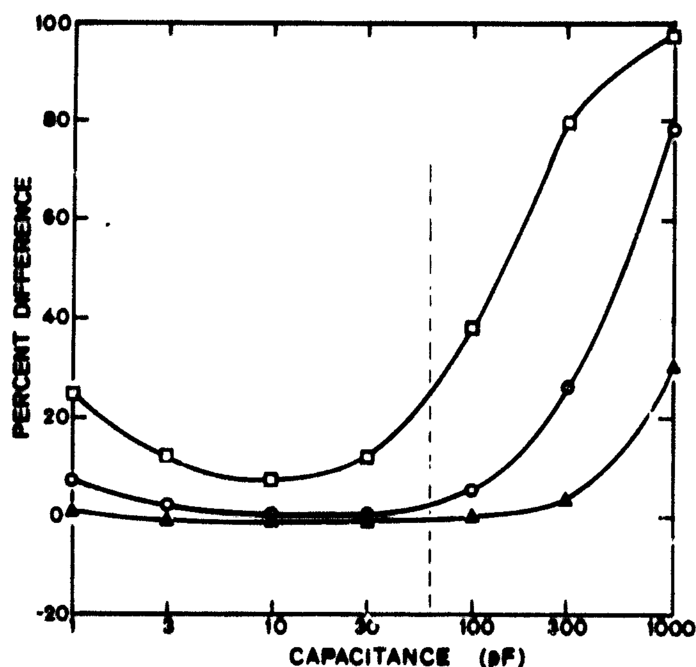


Figure 2. Percent difference between actual capacitance and capacitance as measured with series resistors of 100 (△), 300 (○), and 1000 (□) Ω. Capacitance values encountered in test specimens studied to date for reverse bias between 2 V and breakdown fall to the left of the vertical dashed line.)

difference occurs. However, the measured profiles do not always conform to this predicted behavior.

Preparation of additional specimens for measurement by the four-probe and C-V methods continued. The processing procedure was altered to include aluminum metallization of the finished diodes in order to reduce the resistance in series with the junction depletion capacitance. (R. L. Mattis and D. R. Ricks)

Plans: On the completion of the development of procedures for statistical analysis of data already acquired, experimental study of the current and probe-force dependence of the four-probe method will resume on thin silicon layers epitaxially deposited on opposite conductivity type substrates. Work on vapor-etched bulk silicon wafers will be deferred until the study of epitaxial layers is completed.

Reports on the tabulation of the temperature coefficient of silicon resistivity and on the round-robin experiment to test four-probe resistivity measurements of epitaxial layers will be prepared and presented at the June meeting of ASTM Committee F-1.

Characterization of the instrument for measuring probe loading will be completed.

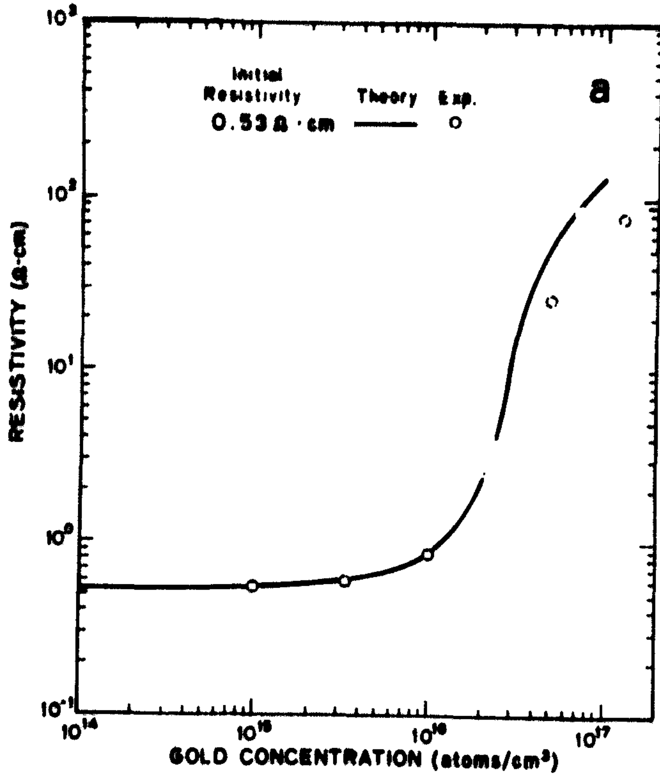
Further work will be undertaken to seek explanations for the discrepancies between four-probe and C-V measurements. Measurements will be made on the metallized devices. Other processing alterations such as sintering of the metallization, sandblasting the back contact and wire bonding will be instituted as seems appropriate. The effect of stray capacitances on the C-V measurement will be considered.

3.2. GOLD-DOPED SILICON

Objective: To characterize n- and p-type silicon doped with gold and to develop a model for the energy-level structure of gold-doped silicon which is suitable for use in predicting its characteristics.

Progress: The model which includes a gold-related shallow acceptor state was used successfully to predict the dependence of resistivity on gold concentration in p-type silicon of both higher and lower resistivity than had been studied previously and, at high gold concentrations, in initially n-type silicon. In the study of the properties of interstitial gold, electrical measurements on specimens diffused with gold for very short times at high temperatures gave results similar to those on specimens with the same gold concentration obtained from longer diffusions at lower temperatures. This result can be explained even though the electrical properties of substitutional and interstitial gold are dissimilar if it is assumed that the rate for the conversion of interstitial to substitutional gold is rapid compared with the diffusion time. Investigation of diode recovery methods for measuring carrier lifetime was resumed. Preliminary results suggest that the previously observed differences in lifetime as determined by the reverse recovery and open circuit voltage decay methods may arise because of variations in the relationship between the lifetime and the storage time in the reverse recovery method.

Resistivity Measurements — Resistivity and Hall effect measurements were made at 25 ± 1°C on Hall bars cut from 0.53-, 1100-, and 2700-Ω·cm p-type wafers diffused with gold at temperatures of 850, 950, 1050, 1150, and 1250°C. The resistivity results are shown in figure 3 along with theoretical curves based on a solution to the charge balance equation to find the Fermi level and, hence, the hole concentration. In these calculations the energies of the gold donor and acceptor states were taken as 0.35 eV and 0.58 eV, respectively, above the valence band [1]. A degeneracy factor of 0.125 was assumed for both the donor and the acceptor states of gold, the energy gap was taken as 1.1057 to fit the intrinsic resistivity data, and the effective masses were taken from the work of Barber [2]. Also included was the additional acceptor impurity state located 0.033 eV above the valence band proposed by Brückner [3] with a concentration which varies as the third power of the gold concentration. Its concentration was taken as 4.5×10^{15} cm^{-3} at a gold concentration of 10^{17} cm^{-3}. Lattice mobility [4] and impurity mobility [5] were combined reciprocally to obtain the hole mobility used in the calculation of the resistivity. The same model was also used to calculate the resistivity as a function of gold concentration for initially n-type silicon with gold concentration greater than the donor concentration. With the exception of a few points, the calculated curves generally fit the previously reported experimental data (NBS Tech. Note 717, pp. 10-12) as shown in figure 4.



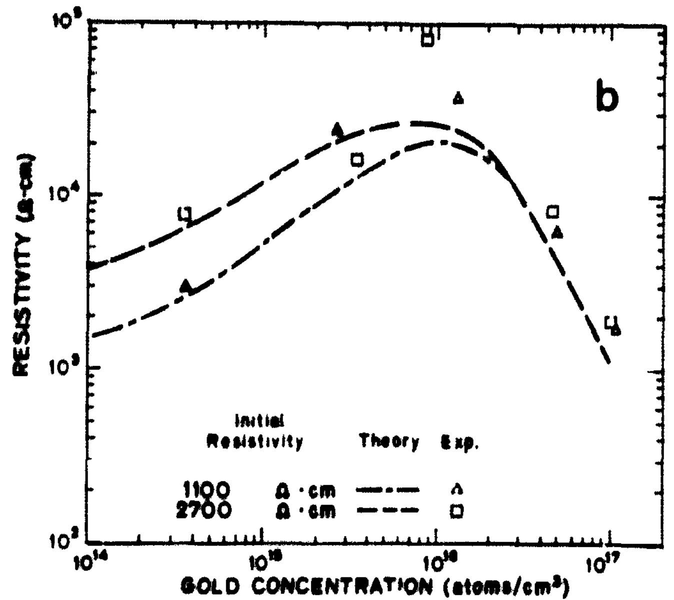


Figure 3. Resistivity as a function of gold concentration in *p*-type silicon. (The parameters used to generate the theoretical curves are given in the text. Error bars are not given for the experimental points. The experimental resistivity values are reproducible within about 5 percent and the standard deviation of the gold determination is estimated to be 10 percent.)

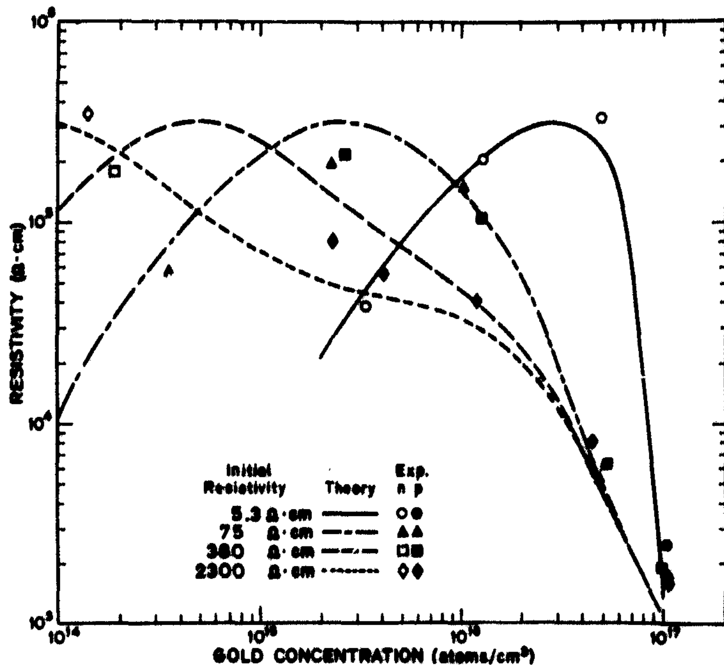


Figure 4. Resistivity as a function of gold concentration in initially *n*-type silicon. (Open symbols represent specimens which remained *n*-type after gold diffusion; solid symbols, specimens which were converted to *p*-type by the addition of gold. The theoretical curves were generated using the model and parameters discussed in the text. Error bars are not given for the experimental points. The standard deviation of the gold determination is estimated to be about 10 percent. Because of the large temperature dependence of the resistivity of near-intrinsic silicon, resistivity values are estimated to be reproducible only to within about 10 percent.)

To examine the effect of interstitial gold on the electrical properties of silicon, diffusions of short duration were done at 950 and 1150°C in both n- and p-type wafers to obtain gold concentrations much lower than the saturation value. Electrical measurements were made on the diffused material and the results compared with data obtained on the same or similar starting material which was diffused to saturation for long times at lower temperatures. The data points for the initially 2300-Ω·cm, n-type silicon at the two lowest gold concentrations in figure 4 were short-time diffusions and are either in agreement with nearby points from long-time diffusions or are close to the calculated curve. The resistivity data on the p-type silicon diffused for short times were in agreement with those obtained on other wafers with the same gold concentration but diffused for much longer times. Thus the resistivity depends only on the gold concentration and not on whether saturation was achieved. Schuman [6] studied the electrical characteristics of silicon diffused with gold for short times and concluded that interstitial and substitutional gold affect the electrical properties of silicon in the same manner. This similarity need not be invoked if the rate for the conversion of interstitial to substitutional gold is very rapid compared to the diffusion time so that the ratio of substitutional to interstitial gold is independent of diffusion time.

The study of the effect of heat treatment on the electrical properties of silicon indicated that resistivity and type changes do occur in high-resistivity crystals subjected to heating at the same times and temperatures used for the gold diffusions. Results on 1100-Ω·cm, p-type wafers, which converted to high-resistivity n-type after a treatment at 1250°C, suggest that about 10^{13} compensating donors per cubic centimetre are introduced by the heat treatment. These results are consistent with the data in figure 3 for 1100- and 2700-Ω·cm specimens where the experimental points have higher resistivity than the calculated curves.

Carrier Lifetime Measurements — Measurements of carrier lifetime by the surface photovoltage (SPV) method [7] continued on bars cut from a number of silicon wafers diffused with gold. In several cases the specimens had been diffused with gold at 850°C for times of 2 to 33 hours. The SPV plots for these specimens did not show a significant linear region using either of two sets of absorption coefficient data. One set, measured on silicon that was not stress relieved [8], has given the more linear plots on wafers of the as-grown crystals. The other set, measured on stress-relieved silicon [9], has given linear plots on specimens that had been gold-diffused to saturation. Apparently a gold diffusion of short duration at 850°C relieves only a portion of the stress which is initially present in the slice while the heating cycle associated with the usual gold diffusion is sufficient to relieve essentially all of the stress in the surface. (W. R. Thurber, A. W. Stallings, and W. M. Bullis)

The investigation into the relationship between the lifetime of minority carriers in semiconductor structures as measured by the reverse recovery (RR) and open circuit voltage decay (OCVD) techniques was resumed. Apparatus that was used in previous experiments was reassembled and tested. The RR apparatus was similar to that described by Owen and Wilkinson [10]; the OCVD apparatus was similar to that described by Lederhandler and Giacoletto [11].

In addition, other, different RR and OCVD apparatus were built to investigate the possibility that previously observed differences between these methods (NBS Tech. Note 560, p. 13) might have been associated with the equipment. The new OCVD equipment utilized a reed relay to isolate the diode under test. The new RR apparatus utilized batteries to forward bias the diode, and was designed so that the bias batteries were isolated by a resistance of a few thousand ohms from the pulse generator which was used to reverse bias the diode. Both new apparatus were isolated from ground so as to eliminate the possibility of ground loops.

RR and OCVD transients of a germanium power diode were studied with the old and new equipment. There were no significant differences in the transient waveforms observed on the old and new RR or OCVD equipment; these results indicated the transient waveforms were related to properties of the diode and were not artifacts of a particular test circuit.

The dependence of the RR and OCVD transients on different values of current-limiting resistance, forward current, and the ratio of the forward to reverse currents was studied to determine those factors which could perturb, or appear to perturb, the lifetime, τ, of the minority carriers in the diodes tested. The results of RR experiments run on four commercial diodes showed that although the same OCVD waveform was observed in all cases, there was no single relationship between the storage time, t_s, and the ratio of the forward and reverse currents, I_f/I_r, which could be applied to all diodes. For three of the four diodes tested the functional relationship between the ratio of the storage time and lifetime and the ratio of the forward and reverse currents was

$$t_s/\tau = \ln\,[1 + (I_f/I_r)] \ ,$$

characteristic of the lumped constant model, but for the fourth diode the functional relationship was

$$\mathrm{erf}\sqrt{t_s/\tau} = [1 + (I_r/I_f)]^{-1} \ ,$$

as derived by Lax and Neustadter [12] for an abrupt junction. Since the ratio of the storage time and carrier lifetime for a particular ratio of forward and reverse current is considerably different in the two cases, the origin of the differences

in functional relationship are being investigated as a possible cause of the discrepancy between the RR and OCVD methods. (D. C. Lewis)

Plans: Sets of p-type wafers with initial resistivities of 0.08, 1, 300, and 2400 Ω·cm, which were diffused with gold this quarter, will be characterized at room temperature by resistivity and Hall effect measurements. Gold diffusions will be started on wafers cut from several n-type silicon crystals. Hall effect and resistivity will be measured as a function of temperature on selected gold-doped silicon specimens to gain information on the nature of the shallow, gold-coupled acceptor states which appear to be influencing the resistivity at high gold concentrations.

The annealing experiments to study gold precipitation will be analyzed after activation analysis results for gold concentration are obtained. Measurements will be made on high-resistivity p-type silicon specimens that were heat treated in an oxygen or argon atmosphere at 950 and 1250°C in a new diffusion tube, prior to its use for gold diffusions, to provide information on the effects of heat treatment without interference from gold contamination. Similar heat treatments will be done on n-type specimens.

Measurements of carrier lifetime by the surface photovoltage method will continue with emphasis on p-type specimens with initial resistivities of 0.08 and 1 Ω·cm. Other absorption coefficient data will be used in the analysis to attempt to obtain straight line plots in specimens diffused for relatively short times.

Additional RR and OCVD measurements will be made in an effort to determine those factors which can alter, or appear to alter, the lifetime of minority carriers in diode structures. Experiments will be undertaken to try to establish the origins of the differences in the functional relationship between the ratio of the storage time and lifetime and the ratio of the forward and reverse currents. The correlation between the carrier lifetime as measured by RR and OCVD will be further investigated.

3.3. INFRARED METHODS

Objective: To study infrared methods for detecting and counting impurity and defect centers in semiconductors and, in particular, to evaluate the suitability of the infrared response technique for this purpose.

Progress: A study of infrared response (IRR) spectra obtained from lithium-drifted germanium detectors showed that spectra observed to date can be grouped into five types: one representative of good quality detectors and four representative of poor quality detectors. Three of the latter have been matched by spectra from diodes

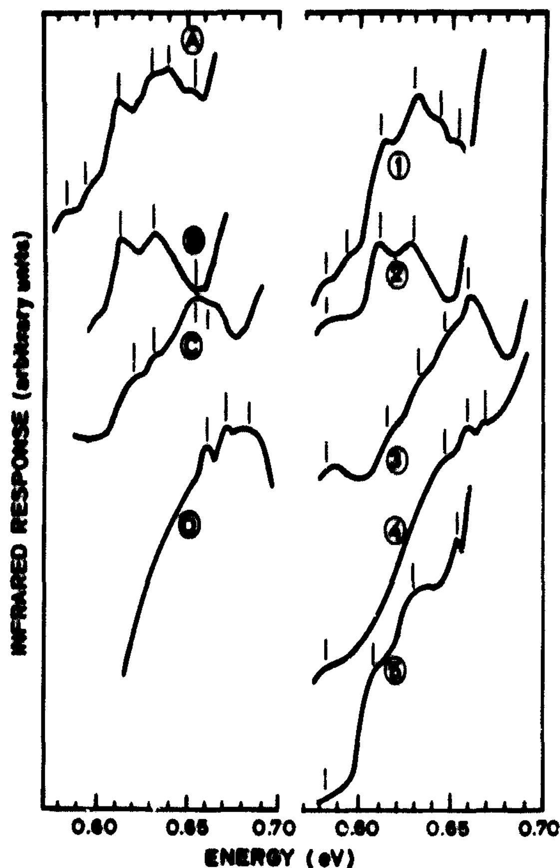


Figure 5. Infrared response spectra obtained from five lithium-drifted germanium diodes fabricated from crystals from five different sources [(1) - (5)] and four diodes fabricated from specimens of another crystal treated in known manners [(A) - (D)]. (Spectral features of interest as indicated by short vertical lines are identified in table 2. The diodes are identified in table 3.)

Table 2 — Characteristics of Infrared Response Spectrum Types

Spectrum[a]	Energy of Minimum (eV)	Energy of Major Features (eV)	Comments
(1), (A)	0.66	0.65, 0.64, 0.63, 0.61, 0.59, 0.58	Rises sharply into bandedge above 0.66 eV.
(2), (B)	0.65	0.63, 0.61	Rises sharply into bandedge above 0.65 eV.
(3), (C)	0.68	0.66, 0.65, 0.64	Rises into bandedge above 0.68 eV; spectrum decreases below 0.66 eV.
(4), (D)	----	0.67, 0.66, 0.65	No prominent minimum; this type shows the least number of spectrum features (fairly featureless from 0.58 to 0.65 eV).
(5)	0.66	0.65, 0.63, 0.61	Small minimum; sharply rises into bandedge above 0.66 eV.

[a] as shown in figure 5

fabricated from a good quality crystal that had been degraded in a known manner. Thus substantial progress has been made in identifying the causes of poor crystal quality from IRR spectra.

The IRR of two lithium-drifted silicon diodes was measured; the silicon detectors were studied both before and after electron irradiation, and energy states present before and after irradiation were tentativoly identified. Long term annealing effects were observed on one of the devices.

Infrared Response Measurements on Germanium — Measurements of infrared response (IRR) continued on lithium-drifted germanium diodes fabricated from specimens of the 85 crystals collected for the germanium study (NBS Tech. Note 472, p. 16). Crystals obtained from a number of different suppliers have been examined. These crystals yield detectors of varying quality; the comparison of their IRR spectra with those of specimens with known crystal parameters has begun.

Figure 5 shows a comparison of IRR spectra obtained from five Ge(Li) detectors fabricated from crystals from five different suppliers [curves (1) through (5)] with spectra obtained from four specimens of one crystal, each treated in a different manner [curves (A) through (D)]. From previous studies and a review of pertinent literature, it has been concluded that, in general, the energy region covered in figure 5, 0.57 to 0.70 eV, is that in which crystalline imperfections are detected; most of the features arising from impurities fall below 0.57 eV in the IRR measurements. The spectra of these detectors exhibit distinct features that serve as the basis for dividing IRR spectra into five types. The characteristics of each type of IRR spectrum are given in table 2.

Of particular interest are the four IRR spectra on the left side of figure 5; each is set opposite the spectrum type on the right for which similar features are shown. These spectra are of diodes all fabricated from specimens of germanium crystal NBS 83. NBS 83-3 (Spectrum A) was a good quality detector, subjected only to the usual lithium-fabrication procedures, which has been used for some time as the standare of comparison with various other diodes measured in the IRR studies. NBS 83-8 (Spectrum B) was irradiated with neutrons from a plutonium-beryllium source at a fluence of approximately 1.3×10^{10} cm^{-2} (NBS Tech. Note 727, pp. 17-19). NBS 83-6 (Spectrum C) was stored at room temperature after lithium diffusion for a considerable period of time and is thus thought to contain lithium precipitates (NBS Tech. Note 717, pp. 13-14). NBS 83-4 (Spectrum D) was heated to 800°C, quenched to room temperature, and is thought to contain approximately 10^{14} cm^{-3} thermal defects [1] (NBS Tech. Note 598, pp. 14-16). That the IRR spectrum of a germanium specimen of known high quality can be modified by specific treatment of a crystal to yield spectra

Table 3 — Summary of Crystal and Diode Characteristics of Germanium Specimens

Spectrum[a]	Diode No.	Material Properties	Detector Properties	Corresponding Reference Diode	Spectrum[a]
(1)	NBS 619	Oxygen conc.: $< 10^{14}$ cm^{-3}	Good diode, slight electron trapping	NBS 83-3: lithium drift only, good detector	(A)
(2)	NBS 76	High Li mobility	Good diode, severe hole trapping	NBS 83-8: neutron-irradiated	(B)
(3)	NBS 91	Low Li mobility, oxygen conc.: 8×10^{14} cm^{-3}	---	NBS 83-6: lithium precipitates	(C)
(4)	NBS 13	High Li mobility, high disloc. density	Very unstable, diode could not be maintained	NBS 83-4: thermal defects	(D)
(5)	NBS 302	---	Poor diode, electron trapping	---	

[a] as shown in figure 5.

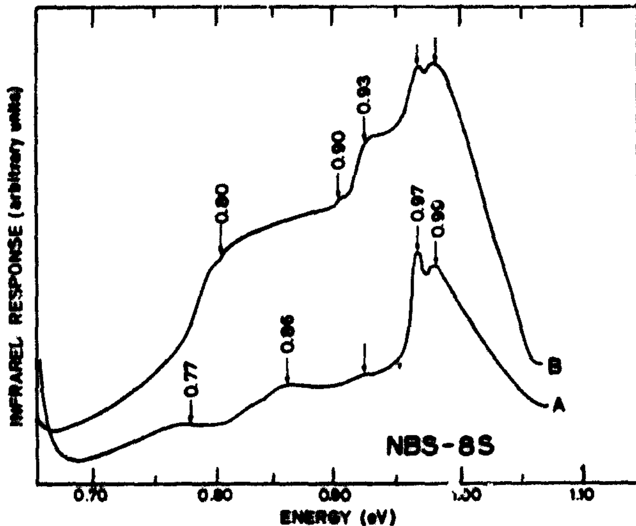


Figure 6. Infrared response spectra of a commercial lithium-drifted silicon detector obtained before (A) and after (B) irradiation with 1.6-MeV electrons.

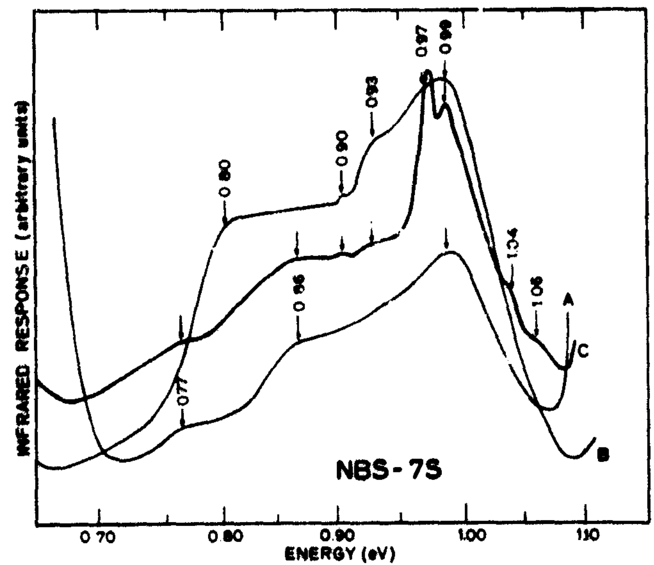


Figure 7. Infrared response spectra of a lithium-drifted silicon detector obtained before (A), immediately after (B), and about 2 months after (C) irradiation with 1.6-MeV electrons.

similar to that of lesser quality crystals, as shown in figure 5, indicates for the first time that the energy region from about 0.57 to 0.70 eV can be used to yield qualitative information on crystalline imperfections in germanium. Table 3 summarizes some of the measured material and detector characteristics of the diodes studied. While it is not possible at present to state with certainty that the known defects can be linked to the test crystals by the IRR spectra alone, it appears likely that further study of these spectra will yield specific information on the causes of poor quality in germanium intended for detector fabrication.

(A. H. Sher, W. J. Keery, and H. E. Dyson)

Infrared Response Measurements on Silicon — Measurements of IRR on electron-irradiated, lithium-drifted silicon detectors continued. Figure 6 shows IRR spectra obtained from a commercial detector, NBS-8S, fabricated from 1000-Ω·cm, float-zoned, boron-doped silicon. Before electron irradiation (curve A), the spectrum exhibits features at 0.77, 0.86, 0.93, 0.97, and 0.99 eV. The first three of these features can be attributed to energy states of divacancies located 0.4 eV below the conduction band, and 0.31 and 0.24 eV above the valence band, respectively [2-4]. The feature at 0.99 eV in the spectrum corresponds to a state 0.18 eV below the conduction band arising from the vacancy-oxygen complex [3]; the feature at 0.86 eV might also be evidence of a lithium-defect interaction [5], while the feature at 0.97 eV has, as yet, not been identified. After room temperature irradiation with 1.6-MeV electrons at a fluence of about 2×10^{14} cm^{-2} (curve B), the features at 0.77 and 0.86 eV are no longer evident, and additional features are observed at 0.80 and 0.90 eV. An energy state 0.38 eV below the conduction band (0.80 eV) has been attributed to the divacancy [4], while a state located 0.27 eV above the valence band (0.90 eV) is thought to arise from lithium precipitates [6].

Figure 7 shows IRR spectra obtained from a lithium-drifted silicon detector before, shortly after, and about 2 months after 1.6-MeV electron irradiation. This detector, NBS-7S, was fabricated in this laboratory from a crystal with essentially similar characteristics to that of NBS-8S. Before irradiation (curve A), the same features are observed as for NBS-8S, except the feature at 0.97 eV appears to be absent. Shortly after irradiation (curve B), the same features are exhibited in the IRR spectrum of NBS-7S as in NBS-8S, except the two peaks at 0.97 and 0.99 eV are not well resolved. Curve C shows the IRR spectrum obtained from NBS-7S after the detector had been stored for about 2 months after the post irradiation measurement without bias at room temperature. That the feature at 0.80 eV has disappeared and those at 0.77 and 0.86 eV are again observed as before irradiation may indicate that some annealing effects took place during room temperature storage, presumably due to the presence of mobile lithium ions. It is also interesting to note that the features at 0.97 and

0.99 eV are as well resolved in curve C as in the spectra of NBS-8S. Features in the spectrum at 1.04 and 1.06 eV are also observed; the upper feature may be related to an energy state about 0.1 eV below the conduction band which has been reported in the literature [7] but not identified with a particular defect.

Since the commercial lithium-drifted silicon detectors used in this study had gold *p*-contacts, approximately 15 to 20 nm thick, through which the infrared radiation must pass, it was necessary to determine what effects, if any, this thin contact had on the measurement of IRR. The infrared transmission of a 0.14-mm thick silicon filter, the thickness used in the measurement of the IRR of silicon detectors, was measured using a thermocouple detector both before and after evaporation of approximately 15 nm of gold onto one side of the filter. No effect was observed in the spectral distribution of the radiation; however, the overall transmission was reduced by a factor of about three as compared to the uncoated filter.

(A. H. Sher, W. J. Keery, Y. M. Liu, and H. E. Dyson)

Plans: The studies of IRR on germanium and silicon diodes will continue with emphasis this next quarter on germanium detectors fabricated from crystals on hand. Efforts to extend the technique to transistors and diodes will continue.

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4. SEMICONDUCTOR PROCESS CONTROL

4.1. DIE ATTACHMENT EVALUATION

Objective: To evaluate methods for detecting poor die attachment in semiconductor devices with initial emphasis on the determination of the applicability of thermal measurements to this problem.

Progress: The analysis of heat flow to determine the limitations of the thermal response technique for detecting poor die adhesion in semiconductor devices was continued. Curves were generated from which a lower limit of the transient thermal response normalized to heating power, $\Delta T_{JC}/P$, needed for maximum sensitivity to voids in the die attachment of semiconductor devices can be determined. It was also established that the thermal response technique is relatively insensitive to voids that are located in areas laterally removed from the junction used to sense the chip temperature. Initial experiments to apply the transient thermal response technique to transistors with poor die adhesion indicated that the transistors could be operated in a diode mode with the collector shorted to the base without exceeding the current handling limitations of the base lead and metallization.

Analysis — Calculations of the steady-state temperature distribution on the top surface of an idealized diode configuration were made to determine (1) the effect of chip and heating source size on the peak temperature difference and (2) the dependence of surface temperature on lateral distance from the source of heat. The three-dimensional Laplace equation [1]:

$$\nabla^2 T = 0,$$

was solved for boundary conditions appropriate to a rectangular semiconductor chip with a rectangular heat source centered on the top surface to represent the power dissipated in the active region. The bottom surface was assumed to be isothermal. All other surfaces were assumed to be adiabatic.

The solutions were obtained in the form of an infinite series. The degree of accuracy depends on the number of terms used to approximate the infinite series. Typical results of the calculation of the peak temperature difference, at the center of the slab, are given in figure 8. The results are presented as the product of peak chip thermal resistance* and thermal conductivity for square chips as a function of chip

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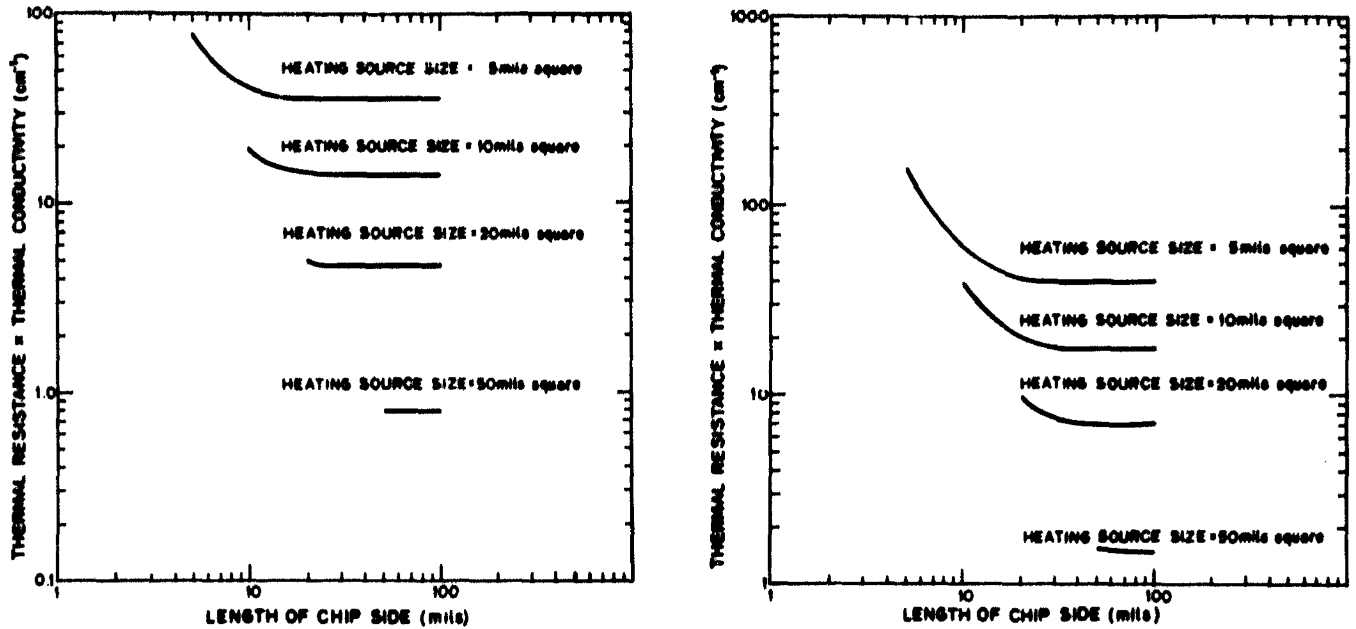
* The so-called peak chip thermal resistance is the steady-state temperature difference between the temperature of the hottest spot, in this case the center of the top surface, and the temperature of the isothermal bottom surface divided by the applied power. Note that this quantity does not include thermal resistance associated either with the die attachment material or with the case.



a. Chip thickness: 5 mils. b. Chip thickness: 10 mils.

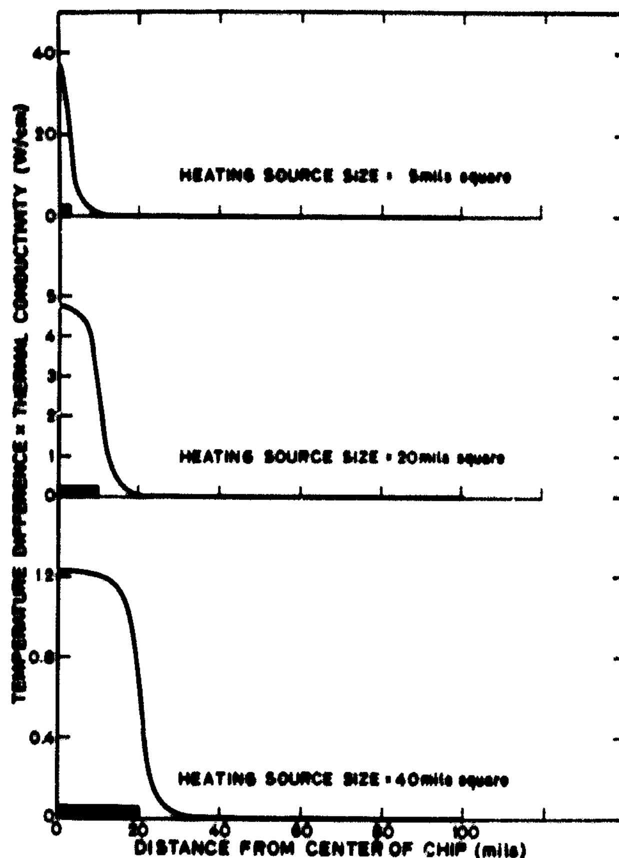
Figure 8. The product of the peak chip thermal resistance between the center of the top surface and the isothermal bottom surface and the thermal conductivity as a function of length of chip side for a square chip with a centrally located square heat source for different chip thicknesses and heating source sizes.

size for various sizes of square heat sources and for chip thicknesses of 5 and 10 mils.* Since the thermal conductivity of silicon is about 1 W/cm·°C, the ordinate can also be read as peak chip thermal resistance in degrees Celsius per watt. For maximum sensitivity to voids in the die attachment, the heating power pulse width for transient thermal response measurements should be long enough that the resulting value of $\Delta T_{JC}/P$ is greater than the peak chip thermal resistance.

Figure 9 shows plots of the product of the temperature difference between points along a perpendicular bisector of an edge on the top surface and the isothermal bottom surface of the chip and the thermal conductivity as a function of position on a 200 mil square chip for various heat source sizes. A chip thickness of 5 mils, power dissipation of 1 W, and a square, centrally located heat source were assumed. The plots indicate that if a void is located only a small distance outside the heat source area it would have little effect on a temperature indicator located at the center of the chip upper surface. Alternatively, if a void caused the temperature distribution indicated, a temperature sensing element located in an area other than near the void would be insensitive to its presence. This type of analysis indicates the difficulties in trying to use the temperature sensitivity of individual elements on integrated circuit chips to indicate the presence of voids in the die attachment material. (R. L. Gladhill and F. F. Oettinger)

* Lateral dimensions of semiconductor chips are customarily given in mils; 40 mils ≈ 1 mm.

Figure 9. The product of the temperature difference between a point along a perpendicular bisector of the edge on the top surface and the thermal conductivity as a function of distance from the center of the chip for a chip 200 mils square and 5 mils thick, a power dissipation of 1 W, and different heating source sizes.



The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes under investigation was continued. A mesa diode, similar to the ones used in the study of diode die attachment evaluation (NBS Tech. Note 727, pp. 25-27), was modeled for calculations with the TRUMP thermal analysis program [2] of the effects of die bond voids of various sizes on the device junction temperature. Initial computations, limited to centrally located voids on an iron-nickel-cobalt alloy, glass-backed TO-5 header and on a solid-steel TO-5 header, indicated that further device modeling modifications are needed if satisfactory results are to be achieved. (W. E. Phillips)

Transistors — Experiments to apply the transient thermal response technique to transistors with poor die adhesion were continued. Based on previous measurements of thermal resistance of a 35-W, triple-diffused transistor connected as a diode (NBS Tech. Note 727, pp. 49-50), it was decided that the diode operating modes suitable for transistor die attachment evaluation might be obtained either by connecting the emitter to the base and using the base-emitter junction. Initial thermal response measurements made on two diode-connected 800-mW transistors indicated that when the transistor was operated in the second of these modes sufficient power can be dissipated in the device without overloading the base lead and base metallization. In this

mode, less than 2 percent of the total current went through the base while 15 to 30 percent of the current went through the base when the emitter and base were connected.

Complete curves of thermal response normalized to heating power were then made on 13 transistors with maximum power ratings ranging from 500 to 800 mW using both the transistor and the emitter-base diode operating modes. In all cases, a sufficient temperature difference was attained in the diode operating mode without exceeding the maximum ratings of the transistors tested. In general, it was found that the difference in the measured thermal response for the two techniques increased as the heating power pulse width was decreased. This is to be expected since thermal response measurements with shorter heating power pulses are more sensitive to temperature and current distribution variations on the chip.

(F. F. Oettinger and R. L. Gladhill)

Plans: The analysis of heat flow to determine the limitations of thermal response techniques for detecting poor die adhesion in the diodes previously investigated will continue using the TRUMP thermal analysis program. The design and fabrication of a die attachment evaluation test circuit capable of measuring thermal response of both diodes and power transistors (in both the diode and transistor operating modes) will be undertaken. Further measurements of thermal response of diode-connected transistors will also be made in order to better understand the usefulness and limitations of this mode of operation for transistor die attachment evaluation.

4.2. WIRE BOND EVALUATION

Objective: To survey and evaluate methods for characterizing wire bond systems in semiconductor devices and, where necessary, to improve existing methods or develop new methods in order to detect more reliably those bonds which will eventually fail.

Progress: In the continuing study of ultrasonic bonding of aluminum ribbon wire, pull strength measurements were made on magnesium-doped wire. The results confirmed the previous work on silicon-doped wire in which the use of a bonding schedule with longer time and lower power than normally used resulted in increased bond strength and improved cosmetic appearance. Measurements of pull strength of single-level round wire bonds as a function of pulling hook position were repeated on several different substrates. In all tests, the second bond was epoxied so that the dominant failure mode was rupture at the heel of the first bond. There was considerable variability in pull strength exhibited by groups of bonds on different substrates, although the changes in pull strengths with hook position, normalized to that found at the center position of the pulling hook, were, in each case, in agreement with those calculated

by resolution of forces. Calculations showed that the temperature distribution in a transistor bond loop under conditions of slow thermal cycling is linear rather than exponential as heretofore assumed. Recalculation of flexure as a function of loop height yielded small but detectable changes from the original calculations. A considerable effort during the quarter was directed toward standardization activities and dissemination of information on wire bonding and bond evaluation.

Ribbon-Wire Bonding — Work on ultrasonic bonding of aluminum ribbon wire equivalent in cross-sectional area to 0.001-in. (25-μm) diameter round wire has continued. The pull strength and cosmetic appearance of bonds made with aluminum (1% magnesium) wire with a tensile strength of about 14 gf (137 mN) and cross-sectional dimensions of 0.0005 by 0.0015 in. (13 by 38 μm) were investigated using single-level bonding substrates. The bonding force was held constant at about 25 gf (245 mN) throughout the investigation, and a loop height of 0.012 in. (300 μm) was used as in previous round wire studies. The same tool was used in all tests.

Measurements of pull strength of bonds made with various values of ultrasonic power and time were in agreement with previous studies using silicon-doped wire (NBS Tech. Note 727, pp. 32-35) that showed that the use of a low-power, long-time bonding schedule resulted in higher pull strengths and better cosmetic appearance than a more conventional high-power, short-time bonding schedule. The present data show that the highest average pull strengths and smallest variations are obtained at tool tip vibration amplitudes of 27 to 32 μin. (0.68 to 0.81 μm) and times of 140 to 285 ms. The groups of bonds made at low power and long time show mean pull strengths of from 11.0 to 12.2 gf (108 to 120 mN) with an average standard deviation of only ±4 percent about the mean. (H. K. Kessler)

Pull Test Evaluation — The study of variables that might affect the sensitivity of the pull test continued. Further analysis of the data obtained previously (NBS Tech. Note 727, pp. 38-42) was carried out, and the experiment to determine the effect of the position of the pulling hook on single-level bonds with the second bond epoxied was repeated. Measurements were performed on bonds made on six different substrates. On one substrate, two independent sets of measurements were performed. As in the past, the wire bonds tested were 0.001-in. (25-μm) diameter aluminum (1% silicon) wire ultrasonically bonded to aluminum pads. These single-level bonds had a bond-to-bond spacing of approximately 0.040 in. (1 mm) and a loop height of approximately 0.012 in. (0.3 mm). Three power settings were used to yield three groups of bonds on each substrate. Bonds made with low power had relatively undeformed heels, those made with intermediate power were deformed but did not exhibit excessive deformation, and those made with a higher power exhibited the greatest deformation. Unless otherwise noted, the average pull strengths discussed are for breakage at the heel of the first bond.

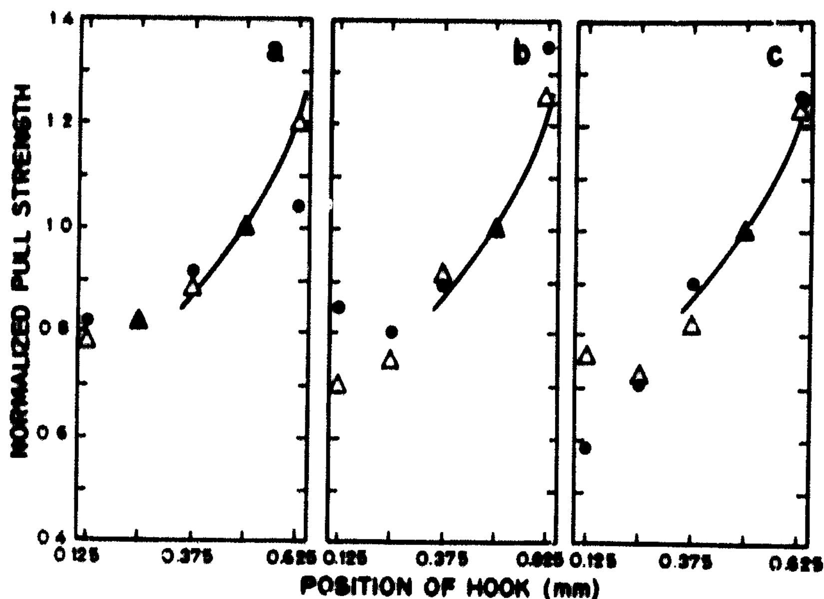


Figure 10. Average pull strength of first bonds as a function of distance between the first bond and the hook used to pull the bond loop. (The bond spacing was 1 mm; the second bond was held with an epoxy drop to eliminate failure of the second bond. Bonds were made with low [a], intermediate [b], and high [c] power. The average pull strength at the center of the loop was 12.1, 7.9, and 7.2 gf [118.6, 77.4, and 70.6 mN], respectively. Values for the sets with the highest [●] and lowest [Δ] pull strengths at each position are presented to indicate the range of results obtained. The solid curves are calculated by resolution of forces.)

Figure 10 shows pull strength data for these bonds normalized to the value obtained at the center of the loop as a function of pulling hook position. In the 1-mm spacing between the first and second bonds, seven hook positions, 0.125 mm apart, were used. The solid line in each case is the curve calculated by resolution of forces (NBS Tech. Note 555, pp. 31-35) for the variation in pull strength as a function of hook position for single-level bonds. For bonds made at all three power levels, the agreement is generally good. However, as the hook is moved toward the first bond, scatter in the data increases substantially.

When the average pull strengths obtained at each position of the pulling hook for the same power group were compared for all seven sets examined (including the one reported last quarter), wide variations were observed. The average difference between highest and lowest for the lower power group was 2.6 gf (25 mN), for the intermediate power group, 3.1 gf (30 mN), and for the high power group, 4.7 gf (46 mN). In general, the bonds made on a particular substrate that exhibited the lowest pull strengths at all hook positions at lower power, also showed the lowest strengths at the other two power settings. Similar results obtain for the group exhibiting the highest pull strengths, etc. It is interesting to note, however, that for the two series of bonds made on the same substrate, the average differences for low, intermediate, and high power settings were 0.5, 1.6, and 0.9 gf (4.9, 15.7, and 8.8 mN), respectively.

Although only bonds in which the break occurred at the heel of the first bond were used in calculating the pull strengths reported, other modes of bond failure were

observed during the course of the experiment. For bonds made at the lowest ultrasonic power setting, many first bond lift-offs were observed at the two hook positions nearest the first bond; at the two hook positions nearest the second bond virtually all bond failures were due to breakage of the wire in the segment near the second bond. For the two higher power settings, no lift-offs were observed, and breakage occurred at the heel of the first bond in nearly every case except for bonds pulled at the three hook positions nearer the second bond, where breakage of the wire was observed in the segment near the second bond. This is consistent with the resolution-of-forces calculation of the ratio of forces in the segments of the wire from the position of the hook to each bond as the hook is moved from the first bond to the second. With the hook near the first bond, the force in the wire is greater for that segment of the wire loop nearest the first bond, and breaks at the heel of the first bond should be almost always observed. At the center position, equal forces are exerted on each bond, but with the second bond held by epoxy, breakage at the first bond heel should be observed. As the hook is placed nearer the second bond a decreasing number of breaks should occur at the heel of the first bond. At a hook position of 0.75 mm, bond failures for the two higher power groups were distributed mainly between first bond heel breaks and wire breaks. At the position nearest the second bond, breakage in the wire at the epoxied second bond accounted for a large proportion of the observed failures. The calculated increase in the force on the segment of wire near the second bond is considerably greater as the hook position is changed from 0.75 to 0.875 mm than it is as the hook position is changed from 0.5 to 0.75 mm.

(?. H. Sher, K. O. Leedy, and C. A. Main)

Bond Failure from Slow Thermal Cycling — Calculations of wire bond flexure due to thermal cycling to determine the dependence of flexure on bond loop height have been reported previously (NBS Tech. Note 717, pp. 23-25). In these calculations it was assumed that the temperature in the wire decreased exponentially with distance from the chip bond. To test this assumption, the aluminum bonding wire was modeled to compute its temperature distribution by means of the TRUMP program [1]. The model was idealized in that the wire and post were assumed collinear with a butt joint. At junction temperatures up to 180°C, corresponding to the rated power input of 500 mW, it was found that the temperature distribution was linear within the wire and that the temperature drop along the wire was two-thirds the junction-to-case temperature difference whether the case was heat sinked or not. Practically all of the remaining third of the temperature drop occurred in the post very close to the butt joint. The physical interpretation of the linear temperature distribution is that heat transfer occurs predominantly by conduction. Radiation is less than a thousandth of the conduction; heat flow by convection is much less than that by radiation. Since the

temperature distribution is linear rather than exponential, four of the previous equations must be changed.

The equation for the wire length, S, in the circular arc model becomes

$$S = S_0\left[1 + \alpha_{Al}\left(\frac{2T_J + T_C}{3} - 23\right)\right] ,$$

where S_0 is the length of the wire at 23°C, α_{Al} is the thermal expansion coefficient for aluminum, T_J is the junction temperature, and T_C is the case temperature. The equations for the length of the die half, a, and the post half, b, of the wire in the triangular model become,

$$a = \frac{S_0}{2}\left[1 + \alpha_{Al}\left(\frac{5T_J + T_C}{6} - 23\right)\right]$$

and

$$b = \frac{S_0}{2}\left[1 + \alpha_{Al}\left(\frac{T_J + T_C}{2} - 23\right)\right] .$$

The modified equation for post height, Y:

$$Y = Y_0\left[1 + \alpha_{\kappa}\left(\frac{19T_C + T_J}{20} - 23\right)\right] ,$$

where Y_0 is the post height at 23°C and α_{κ} is the thermal expansion coefficient of the post alloy, gives a post expansion less than 0.01 percent larger than that obtained previously with the assumption that the post is at the case temperature.

Revised curves of flexure (change in loop height, ΔH_L) plotted against power input to the junction, P_D, (or, equivalently, junction temperature, T_J) are shown in figure 11 for initial loop heights, H_{LO}, of 50, 100, 250, and 500 μm for the circular arc model (dashed lines) and the triangular model (solid lines). The plots resemble those of the previous graph, being nearly linear, and have the same values at low power, but indicate a greater flexure at rated power. The curve for the very high loop height of 500 μm which is also added here shows, as expected, only a small decrease in flexure from that associated with a loop height of 250 μm. (W. E. Phillips)

Standardization and Dissemination — A third successful meeting of the Interconnection Bonding Section of ASTM Committee F-1 was held in connection with the January meeting of the Committee in New Orleans. In addition to developing standard nomenclature and measurement methods, this section is providing a forum for the exchange of ideas and new testing technology. Three invited papers on various aspects of bonding technology were presented. (K. O. Leedy and G. G. Harman)

The use of phased-burst bonding schedules (NBS Tech. Note 727, pp. 35-38) was discussed at the Drexyl University Microcircuit Interconnection Workshop in February.

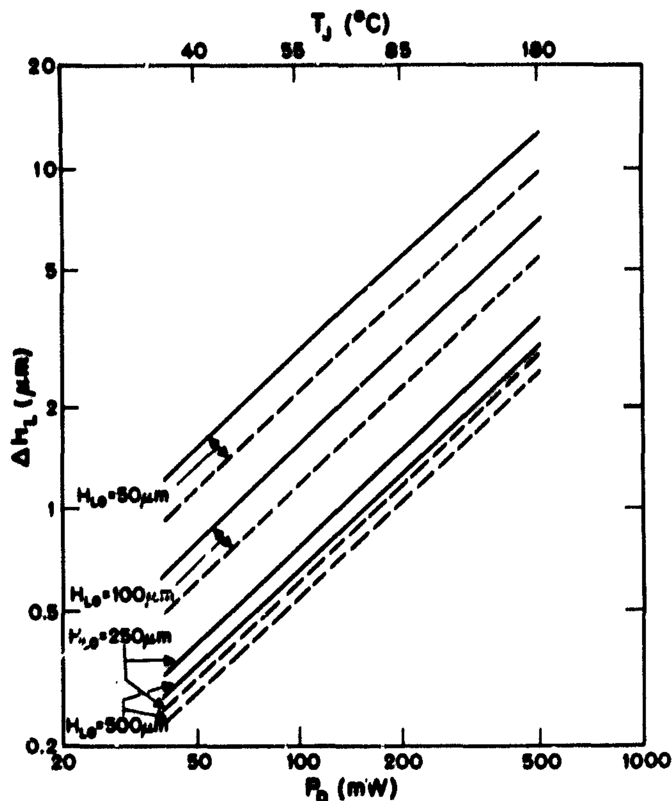


Figure 11. Wire-bond flexure, ΔH_L, as a function of power dissipation, P_D, for triangular (solid lines) and circular arc (dashed lines) bond loops with various values of initial loop height, H_{LO}. (The analysis was made for 1-mil diameter post-to-die aluminum wire bonds in a 500-mW, 50-mA silicon transistor in a TO-18 can with post and header of the usual iron-nickel-cobalt alloy. The junction temperature, T_J, is also indicated.)

An extensive tour of west coast facilities was undertaken in March. Talks on the bond evaluation work carried out at NBS over the past few years were given before local sections of the International Society of Hybrid Microelectronics in San Diego, Los Angeles, San Jose, and Mountain View, California. The results of this work were also discussed extensively at seven semiconductor manufacturing facilities covering discrete devices, monolithic integrated circuits, and both thick film and thin film hybrid circuits. (G. G. Harman)

Bibliography and Critical Review — The critical survey paper is in the final stages of editorial review. The preparation of an annotated bibliography of limited distribution reports was temporarily deferred. (H. A. Schafft)

Plans: Evaluation of ribbon wire for ultrasonic bonding will be completed with a comparison of bond strengths obtained using round and ribbon wires made at the same range of time and power settings. Improvements will be made to equipment used in the work on electronic mixing of bonding tool ultrasonic signals with local oscillators for better understanding and control of bonding; experimental study, deferred this quarter, will resume on completion of these improvements. Experimental and statistical analysis of significant factors affecting the wire bond pull test on single-level substrates will continue. Procedures for the publication of the critical survey paper

will be completed. The preparation of an annotated bibliography of limited distribution reports on wire bonds will be resumed. Standardization and dissemination efforts will continue as appropriate.

4.3. REFERENCES

4.1. Die Attachment Evaluation

1. Lindsted, R. D., and Surty, R. J., Steady-State Junction Temperatures of Semiconductor Chips, *IEEE Trans. Electron Devices* ED-19, 41-44 (1972).

2. Edwards, A. L., TRUMP: A Computer Program for Transient and Steady-State Temperature Distributions in Multidimensional Systems, Lawrence Radiation Laboratory, Univ. of California, Livermore, California, UCRL-14754, Rev. I, 1 May 1968. Available from the National Technical Information Service, Springfield, Virginia 22151.

4.2. Wire Bond Evaluation

1. Edwards, A. L., TRUMP: A Computer Program for Transient and Steady-State Temperature Distributions in Multidimensional Systems, Lawrence Radiation Laboratory, Univ. of California, Livermore, California, UCRL-14754, Rev. I, 1 May 1968. Available from the National Technical Information Service, Springfield, Virginia 22151.

5. SEMICONDUCTOR DEVICES

5.1. THERMAL PROPERTIES OF DEVICES

Objective: To evaluate and improve electrical measurement techniques for determining the thermal characteristics of semiconductor devices.

Progress: Work continued to determine the origins of the frequently observed difference between the straight line extrapolation to zero power of the measured value of the temperature sensitive parameter (TSP) as a function of power and the d-c calibration value at the zero power level. Work on diodes and diode-connected transistors indicated that the cause might lie partially in the charge distribution disturbance caused by switching off the collector voltage when measuring thermal resistance. Measurements made by switching only the emitter suggested that this method yields values of junction temperature that are more nearly the same as the values measured with an infrared microradiometer than are values measured by switching both the emitter and the collector. Work also continued in the investigation of the physical mechanisms of thermal hysteresis, the temperature and current density dependence of common-emitter current gain, h_{FE}, and hot-spot initiation and stabilization. It was found that in an area of sharp hot-spot formation the temperature sensitivity of h_{FE} was greater at lower collector currents, 0.09 A, than at higher collector currents, 0.11 A, and that at hot-spot formation h_{FE} was also larger at lower currents than at higher currents. This observation is in accord with the need for greater power to form current constrictions as collector current is increased.

Standardization Activities — The devices for the preliminary round robin on thermal resistance being conducted in cooperation with EIA-JEDEC Committee JC-25 on Power Transistors have been measured by the third and fourth participants. Work was completed on revising portions of a document on power transistors dealing with thermal characteristics and their measurement that was recently letter balloted in Committee JC-25. The revised document has been submitted to the committee for review and eventual re-balloting.

A test fixture and heat sink to be used for thermal resistance measurements of axial lead signal diodes was designed and fabricated. The measurements are being undertaken as part of a preliminary thermal resistance round-robin experiment being conducted by EIA-JEDEC Committee JC-20 on Signal Diodes.

(F. F. Oettinger and S. Rubin)

Thermal Resistance Methods — Investigation continued into the cause of the frequently observed difference between the straight line extrapolation to zero power of the measured value of the TSP as a function of power and the d-c calibration value at the zero power level (NBS Tech. Note 598, pp. 30-33). Initial measurements on diodes

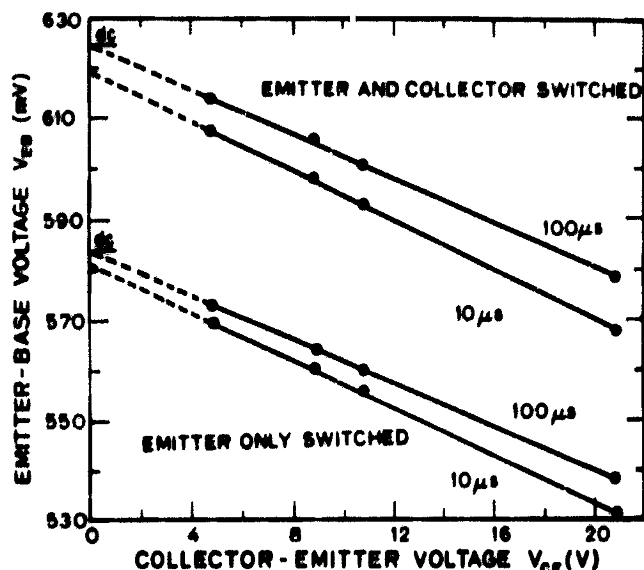


Figure 12. Comparison of emitter-base voltage for a measuring current of 6.5 mA as determined with emitter-only and collector-and-emitter switching for a 35-W, triple diffused, silicon *n-p-n* transistor for delay times of 10 and 100 μs. (During the power pulse the collector current was 500 mA. Case temperature was held at 25°C. The d-c calibration values for collector connected and disconnected, respectively, are also shown for comparison.)

and diode-connected transistors (NBS Tech. Note 727, pp. 47-50) suggested that electrical switching transients are responsible for this difference which occurs for measurements made with delay times less than 50 μs. Additional measurements on diodes and diode-connected transistors further supported this suggestion. As a consequence the grounded-base measuring circuit was modified by shorting out the collector switching transistor so that only the emitter was switched during test. Measurements made using this method resulted in differences about half the magnitude of those using the former collector-and-emitter switching method for a delay time of 10 μs. As an example, the results of measurements made on a 35-W, triple-diffused, silicon *n-p-n* transistor are shown in figure 12. Oscilloscope traces of the emitter-base waveform as a function of elapsed time after the cessation of the power pulse, shown in figure 13, show that the magnitude of the electrical transients of the emitter-base voltage-waveform at a delay time of 10 μs is smaller for emitter-only switching than for emitter-and-collector switching.

In the course of measuring thermal resistance with emitter-only switching, measurements were made on the triple-diffused transistor discussed above in the thermal hysteresis region. As shown in figure 14, the indicated temperature rise at hot-spot initiation ($V_{CE} \approx 180$ V) for emitter-and-collector switching is 37°C while the indicated rise for emitter-only switching is 104°C. Measurements made previously using an infrared microradiometer showed that at hot-spot initiation the temperature of the hot-spot region rises approximately 180°C. The emitter-only switching method thus appears to afford some improvement over the emitter-and-collector switching method for measuring the temperature of a hot spot in a transistor operating in a current-constricted mode. (S. Rubin and F. F. Oettinger)

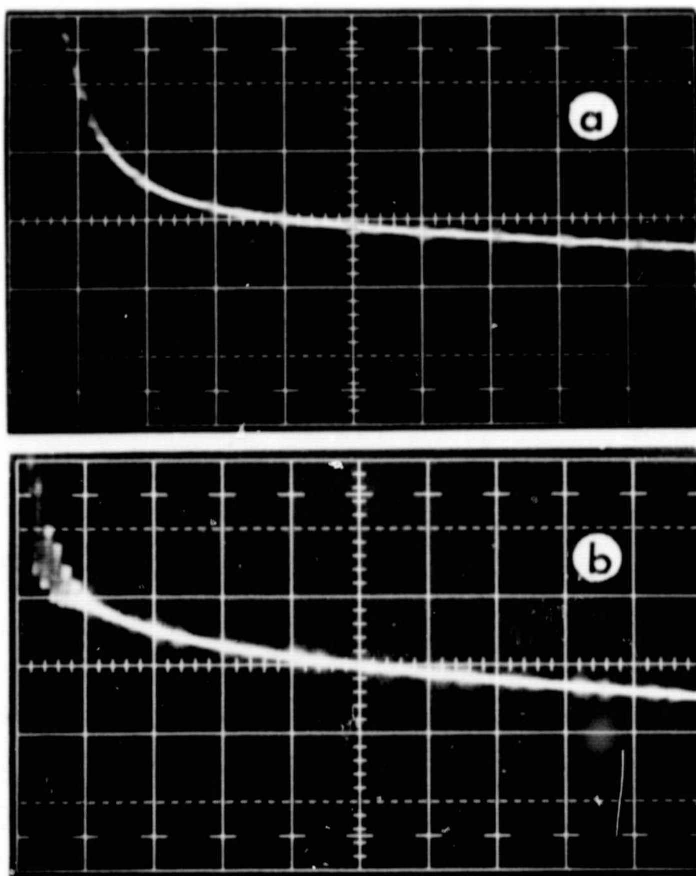


Figure 13. Emitter-base voltage as a function of time after cessation of the power pulse for a measuring current of 6.5 mA for a 35-W, triple diffused, silicon *n-p-n* transistor for emitter-and-collector (a) and emitter-only (b) switching. (During the power pulse the collector current was 500 mA and the collector-emitter voltage was 20 V. Case temperature was held at 25°C. The horizontal scale is 10 microseconds per division, and the vertical scale is 5 millivolts per division.)

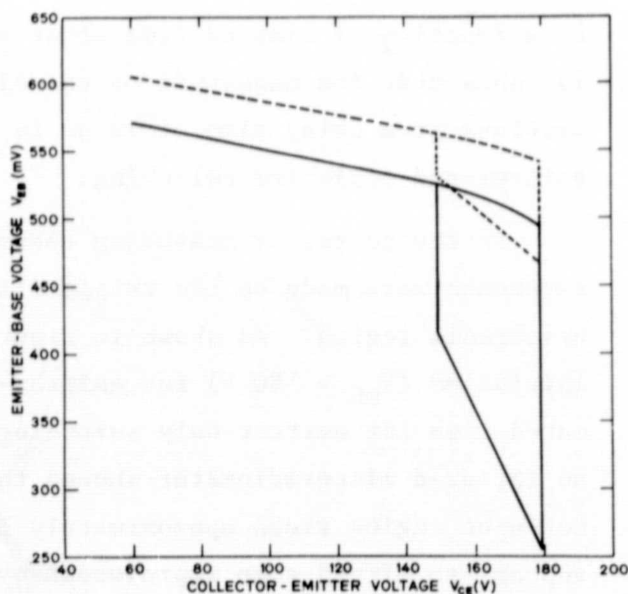


Figure 14. Emitter-base voltage as a function of applied power for a 35-W, triple diffused, silicon *n-p-n* transistor operating in the current-constricted mode for emitter-only (solid line) and emitter-and-collector (dashed line) switching. (During the power pulse the collector current was 100 mA. Measurements were made with a measuring current of 6.5 mA, 10 μs after cessation of the power pulse. The sharp voltage drop at $V_{CE} \approx 180$ V is indicative of the initiation of a hot spot; the magnitude of the drop is directly related to the change in effective junction temperature.)

Screen for Hot Spots — Investigation of the physical mechanisms of the thermal hysteresis effect (NBS Tech. Note 520, pp. 49-52) has been intensified. A better understanding of these mechanisms is expected to aid in the improvement of the previously developed screen for hot spots [1]. Experiments were initiated to determine what roles the temperature and current density dependence of h_{FE} play in the initiation and stabilization of hot-spots and in the thermal hysteresis cycle.

Two possible models have been proposed previously for the observed increase of h_{FE} with decreasing collector-emitter voltage, V_{CE}, while a device is operating with a hot spot or current constriction (NBS Tech. Note 520, pp. 51-52). Briefly, the device could be operating in a region where the gain increases with decreasing temperature (NBS Tech. Note 727, p. 50) or the current density in the constricted region is large enough that the device is operating in a region where h_{FE} increases with decreasing current density. The latter model ruquires that as V_{CE} is decreased, the current density in the constricted region is decreased also.

An experiment was performed which demonstrated for a triple-diffused, 35-W, silicon *n-p-n* transistor that the temperature dependence of h_{FE} could not account for the observed variation of h_{FE} with V_{CE}. While the device was operated in the hot-spot or current-constricted mode the hot-spot temperature was maintained constant by gradually increasing the case temperature as V_{CE} was decreased. For constant hot-spot temperature, h_{FE} increased at a faster rate with decreasing V_{CE} than when the hot spot temperature was allowed to decrease naturally as V_{CE} decreased. This indicates that in the hot-spot mode, h_{FE} is still increasing with temperature for this device.

The role of the temperature variation of h_{FE} in the initiation of a hot spot was also studied. Temperature measurements were made with an infrared microradiometer and thermographic phosphors at a point on a device where a severe hot spot was known to form at values of V_{CE} just a few tenths of a volt below the value at which the hot spot forms. These measurements were made for a narrow range of collector currents (0.09, 0.10, and 0.11 A) to minimize the effect on h_{FE} of varying current density and current distribution within the device. It was found that the temperature immediately before the hot spot formed was lower for the smaller collector currents. Both the rate of increase of h_{FE} with increasing temperature and the magnitude of h_{FE} were larger for the smaller collector currents. This decreasing temperature dependence of h_{FE} with increasing collector current may account for the generally higher power needed to form hot spots at higher collector current levels. (D. L. Blackburn)

Plans: Work on standardization activities related to thermal measurements will continue. The literature search and work on the bibliography on thermal measurements of semiconductor devices will continue. Studies will continue to determine the

validity of the emitter-only switching technique as an improved method for the measurement of transistor thermal resistance for cases of moderate as well as severe current crowding. Experiments will be performed to explore the role of the variation of h_{FE} with current density, to measure the temperature gradient present immediately before the hot spot forms, and to relate thi~ gradient to the magnitude and temperature variation of h_{FE} immediately before the hot spot forms.

5.2. MICROWAVE DEVICE MEASUREMENTS

Objective: To study the problems and uncertainties associated with the measurement of electrical properties of microwave diodes, and to improve the techniques of these measurements.

Progress: Several changes have been made in the X-band mixer measurement system in order to improve the repeatability of the incremental conversion loss measurement on point-contact mixer diodes and to allow the direct measurement, without calculation, of the mixer i-f output conductance by a load perturbation method that also uses the mixer output voltage change resulting from the incremental modulation.

The general requirements for conversion loss measurement repeatability may be seen from the following. Mixer diodes are commonly marketed with standard overall average noise figure limits denoted by suffix letters in 0.5-dB increments; 0.5 dB is considered to be a significant difference as far as system performance is concerned and can drastically affect diode cost. Standard overall average noise figure, expressed in decibels, is equal to the conversion loss plus a term which combines mixer noise and i-f amplifier noise, so that 0.5-dB differences in conversion loss appear as 0.5-dB differences in overall noise figure.

The classification of diodes by these 0.5-dB increments requires a total measurement uncertainty considerably less than this. A total uncertainty of ±0.1 dB with at least 90 percent confidence would seem to be about the largest that could reasonably be considered for such classification. Since these limits could allow a fairly high percentage of the diodes to be misclassified, tighter limits would certainly be desirable, although they would be very difficult to meet. Preliminary measurements have indicated a repeatability for the NBS X-band system somewhat poorer than this for weekly measurement intervals, even excluding obviously unstable diodes. The systematic error uncertainty, which must be added to this, has not yet been established.

Several factors have been suspected of causing the lack of repeatability: mechanical changes in the waveguide system due to forces used in changing diodes, drifts

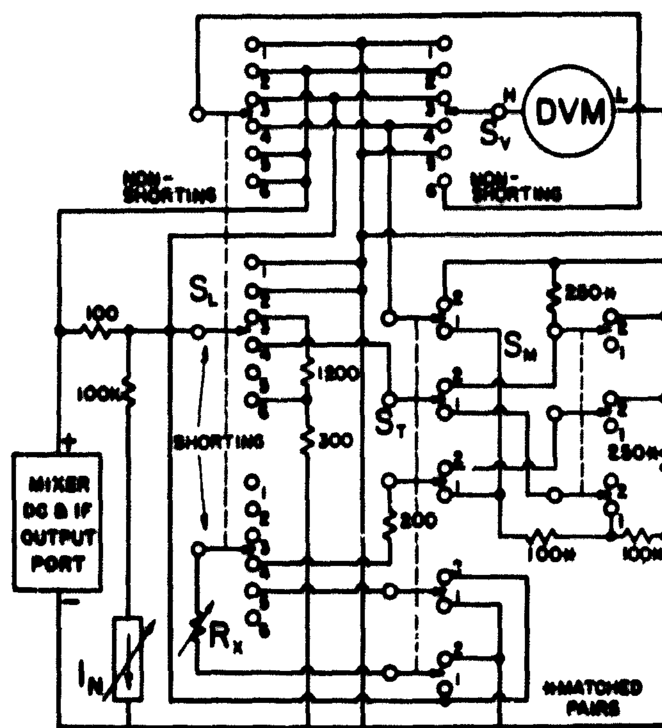
in microwave power or other system characteristics due to temperature or line voltage changes or to aging of components, diode-to-holder contact imperfection, and changes in the diodes themselves due to mechanical shock (moving the whisker) or to temperature changes. Except for contact imperfection, which may be impossible to separate from diode instability, each of these factors has been observed as significantly affecting some measurements, but because of their largely unpredictable nature it is not known how much each contributes to the observed lack of repeatability of the conversion loss measurements as a whole. Each factor is being studied to reduce to the extent possible its influence on the measurement.

Attention has been given to mechanical stability by rigid clamping of the waveguide and, during this reporting period, by transferring the waveguide system to a rigid bench formed from welded L-beams and having an inch-thick aluminum top. Shock-mounted castors allow the bench to be easily moved for rear access with a minimum of distortion of the bench framework due to floor unevenness.

To increase the stability of the local oscillator power, the operational amplifier formerly used in the leveling loop was replaced by one with the lowest temperature coefficient of offset voltage (0.25 μV/°C) currently available for a chopperless type. In addition the operational amplifier power supply was replaced by a more stable type. The other major source of power drift in the leveling loop is the diode detector; an attempt to replace it with a dry calorimeter (thin-film thermocouple) was made, but was unsuccessful because of the exceedingly low voltage developed by the calorimeter. The dry calorimeter is, instead, now being tried as a power monitor to which the r-f power may be directed by a highly repeatable waveguide switch. The power may thereby be checked during a measurement run without removing the mixer.

The mixer output circuit shown in figure 15 has been constructed for use with incremental modulation measurements to permit the direct measurement of i-f conductance and matched-load output voltage. For the i-f conductance measurement, two types of load perturbation methods have been incorporated. One is Mance's method (NBS Tech. Note 592, pp. 57-59), in which a calibrated variable resistor is switched in series with the generator, whose internal resistance is to be determined, and its load. The other is an apparently new method in which the calibrated variable resistor is switched in shunt with the generator and its load. This new circuit was originally developed in order that, for a small load perturbation, the calibrated variable resistance, which at balance is proportional to the generator resistance, would be larger than the latter rather than smaller, as with Mance's method. For a 10:1 arm ratio, this circuit reduces the effect of switch contact resistance in the calibrated variable resistor arm by a factor of 100 as compared with Mance's circuit. For a unity arm ratio, which was needed to increase the sensitivity sufficiently to overcome the

Figure 15. Mixer output circuit for incremental modulation measurements of conversion loss and i-f conductance.



observed voltage instability, the only advantage is that the load is perturbed by a smaller factor (1.5) than in Mance's circuit (2), but at the expense of a larger resistance uncertainty. There is thus a trade off between these circuits, with Mance's offering better repeatability and the new circuit offering less susceptability to systematic error caused by mixer nonlinearity. To test for the significance of the latter, both circuits were incorporated within the i-f chassis. In addition to increasing the sensitivity, the unity arm ratio simplifies the operating procedure by allowing the calibrated variable resistor used in measuring the i-f conductance to be switched across the mixer as the matched load, rather than requiring that its setting be transferred to a second resistor with the decimal point shifted, as was required by the 10:1 arm ratio.

This output circuit has four switches: Switch S_L is used to select the correct load for each operating step and is ordinarily sequenced from position 1 to position 6. Switch S_T is used to select the series (Mance's) or shunt method for the conductance measurement. Switch S_M is used in operating whichever of the methods is selected by switch S_T. Switch S_V is normally left in position 6, which allows the correct voltmeter connection to be selected by switch S_L for each load. In other positions, the voltmeter connection is independent of the load switch setting. This allows, for example, the total mixer output voltage to be monitored as the load is changed. Ease of operation for normal use is thus combined with flexibility for experimental purposes.

Plans: Charts will be prepared to facilitate the rapid and precise conversion of incremental output voltage and i-f conductance data to conversion loss. Using these charts, the repeatability of all previously made diode loss measurements will be evaluated. Further measurements will be made to ascertain the sensitivity of measured quantities to system characteristics such as local oscillator power and output circuit null accuracy to help estimate systematic error uncertainty.

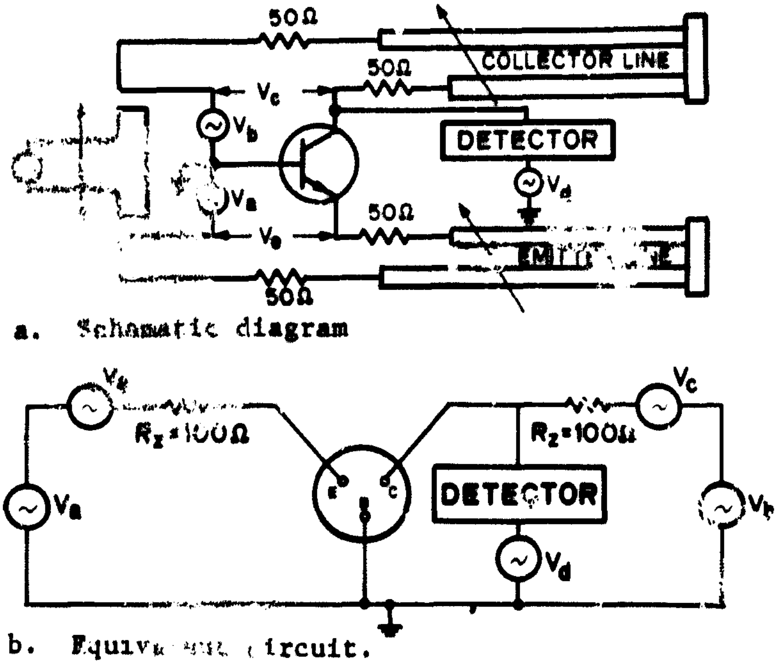
5.3. CARRIER TRANSPORT IN JUNCTION DEVICES

Objective: To improve methods of measurement for charge carrier transport and related properties of junction semiconductor devices.

Progress: A general approach has been developed for determining the location and magnitude of delay-time error-producing sources arising from extraneous pickup at the measurement frequency, and this approach has been tested by applying it to the NBS model of the Sandia bridge. With these sources so characterized, their influence on subsequent transistor measurements can be reduced greatly. The results of this work can explain previously observed differences in measurements of delay time of transistors. Several preliminary steps have been taken toward an interlaboratory comparison of transistor scattering-parameter measurements. Measurements were made as a function of frequency with various bias conditions for three transistor types, the effects of case temperature on the S-parameters were determined qualitatively, the equation widely used to relate h_{fe} to S-parameters was verified, and the S-parameters of an R-C network on a transistor header were measured to determine its suitability for use as a calibration standard.

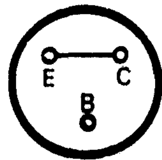
Determination of Delay-Time Error Sources — Previously it has been shown that extraneous coupling at the measurement frequency between various portions of the measurement circuit may have a profound effect on the delay time observed (NBS Tech. Note 727, pp. 53-56). In this quarter, a technique was developed to identify these error sources and to minimize their effects. In the analysis, the measurement circuit, constructed of n connected loops, is treated as known except for the magnitude and phase of an extraneous error-source generator in each loop. These generators are added to the circuit to characterize the effects of undesired signal coupling. The magnitude and phase of these error sources may be calculated if a network of known composition is assumed to be in the transistor socket. With n known networks, the magnitude and phase of all n error-source generators may be determined. These are a property of the particular measurement system and remain constant unless the system is changed. Once the individual error sources are so specified, the delay-time error introduced by these sources can be calculated for any network in the

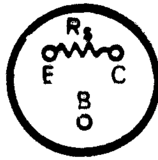
Figure 16. Sandia bridge showing extraneous voltage generators.

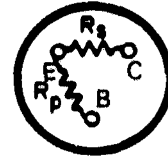


a. Schematic diagram

b. Equivalent circuit.







a. Through short. b. Series resistance. c. Series and parallel resistance.

Figure 17. Non-reactive plug-in elements used to calculate magnitude and phase of extraneous voltage generators.

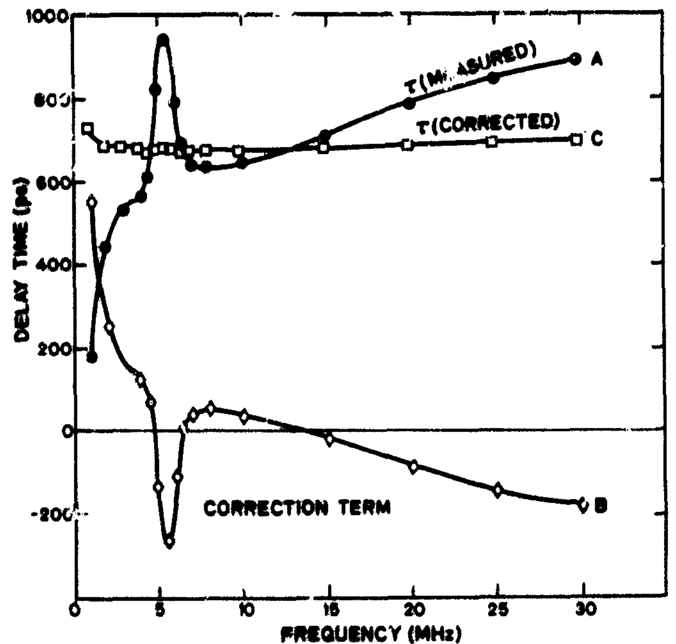


Figure 18. Delay time of an R-C plug-in network as measured as a function of frequency on the Sandia bridge constructed at NBS (A), the correction term appropriate to this bridge for this network (B), and the corrected value of delay time (C).

socket. A correction term, the negative of this error, can then be added to the measured delay time to obtain the correct value. The analysis also permits monitoring the quality of the measurement circuit design, construction, and modifications, since ideally this delay-time error should be zero. To make the calculation for a transistor it is necessary to determine the appropriate equivalent circuit.

As an example, consider the application of this technique to the Sandia bridge. The operation of the bridge, shown schematically in figure 16, is as follows: the controlled signals V_c and V_e are obtained from half-turn loops coupled to a primary loop driven by an r-f generator. The primary loop is adjusted to vary the magnitude of the ratio V_c/V_e. The phase angle between V_c and V_e is varied by adjusting the lengths of the collector and emitter delay lines. These lines are provided with scales calibrated in picoseconds. A reference delay time is first obtained by taking the difference between the scale times on the collector and emitter lines when there is a null at the detector with the emitter terminal of the socket shorted to the collector terminal. The apparent delay time for a network, or transistor, in the socket is then obtained by taking the difference between scale times on the collector and emitter lines and reducing this difference by the reference delay time.

If any of the error sources, V_a, V_b, V_d, is non-zero, a different combination of the amplitudes and phases of V_c and V_e are required for balance than would be required for the ideal case where $V_a = V_b = V_d = 0$. If this different balance can be achieved only by changing the phase between V_c and V_e by varying the length of the emitter or collector lines, an error in the measurement of delay time is introduced. The imaginary components of the error sources referred to the phase of the controlled source V_e are the components which cause delay-time errors. Only for the case of a delay-time network such as a high-gain transistor with negligible base current at the measurement frequency does the emitter-collector short-circuit technique for establishing a delay-time reference remove a major portion of the error introduced by these extraneous generators.

The Sandia bridge constructed at NBS was analyzed with the three non-reactive plug-in units shown in figure 17. The results of this analysis as applied to the measurement of a plug-in R-C delay-time element with a time constant of 665 ps are shown in figure 18. Curve A shows delay time as measured on the bridge, as a function of frequency, using an emitter-collector short for the delay-time reference. Curve B is the correction term calculated from the measurements on the three non-reactive elements. Curve C is the corrected delay time for the network. The latter is nearly independent of frequency, as it should be, but is about 15 percent larger than the value calculated for the network. The nature of this disagreement is being investigated.

For the same measurement system, both theory and experiment show that the severity of the frequency-dependence of the measured delay time depends on the amount of signal current in the base lead. Delay-time measurements are conveniently made by referring them to a delay-time reference established with an emitter-collector short circuit. For the Sandia bridge, this is tantamount to assuming that the correction to be applied is strictly a function of the sum of V_a and V_b, and not a function of V_a and V_b individually. This assumption is not applicable when base current is appreciable; the simple through-short reference technique becomes less and less satisfactory as base current is increased, or as the transistor gain decreases. This is believed to be the reason why the delay-time data previously reported on one transistor showed a significant frequency dependence, while others did not (compare figures 27 and 28 of NBS Tech. Note 727). Since there is also base current in the R-C plug-in networks, the through-short reference technique does not remove all the deleterious effects of the error-source generators V_a and V_b.

For a transistor idealized in that the emitter-base voltage is assumed to be zero and that the only delay time is that associated with the transport of minority carriers across the base and collector junction, it can be shown that the delay time read by the bridge, τ_m, is given by

$$\tau_m = \tau_\alpha - (j/\omega h_{fe})\, Im(V_b/V_e),$$

where τ_α is the true delay time of the transistor. The error term is proportional to $1/h_{fe}$. This suggests that anomalous changes in apparent transistor delay-time may be observed following gain degradation such as might occur after neutron irradiation. The changes quite likely include the signature of the particular measuring setup; this signature can be expected to vary in magnitude and frequency dependence among delay-time instruments. In the case of a real transistor, knowledge of the elements of the equivalent circuit is required to develop an accurate correction term but the general form would be expected to be similar to that of the idealized case.

(D. E. Sawyer)

Interlaboratory Comparison of S-Parameter Measurements — Several preliminary steps have been taken in preparation for an interlaboratory comparison of scattering parameter measurements to be conducted in cooperation with a sponsor.

S-parameters of typical transistors of types 2N709, 2N918, and 2N3960 have been measured to determine optimum biases and frequencies for the determination of f_T from S-parameter data. These transistors were selected as representative types of interest to the sponsor. Present plans are to operate the transistors at a collector-emitter voltage of 5 V, and at eight emitter currents from 1 to 10 mA. For the intercomparison, the participants are to measure the 2N709's and the 2N918's over the frequency

range from 100 MHz to 1 GHz and the 2N3960's from 100 MHz to approximately 2 GHz. From these measurements, for each type, h_{fe} can be obtained as a function of frequency in the transition region where h_{fe} varies from its low-frequency value to a vlaue approaching unity.

The equation for calculating h_{fe} from S-parameters,

$$\overline{h_{fe}} = \frac{-2\,\overline{S_{21}}}{(1-\overline{S_{11}})\,(1+\overline{S_{22}}) + \overline{S_{12}}\,\overline{S_{21}}},$$

is derived from the S-parameter definition of h_{fe} by expressing the input and output currents in terms of the incident and emergent waves of the scattering parameters, and substituting values for these waves obtained by solving the scattering equations for the network when the output of the network is short-circuited. Examination of this equation shows that the sensitivity of h_{fe} to any of the scattering parameters depends upon the value of all the other S-parameters.

This relationship has been determined empirically for typical transistors of the three types. In general, for the bias conditions stated above, the magnitude of h_{fe} varies directly with changes in the magnitude of S_{21}, while changes in the phase of h_{fe} vary from 1 to 1-1/2 times the change in the phase of S_{21}. Changes in either magnitude or phase of S_{12} have a small effect ($\Delta h_{fe} \lesssim 0.1\ \Delta S_{12}$) on either the magnitude or phase of h_{fe}. Changes in either the magnitude or phase of S_{11} and S_{22} produce an inverse change in h_{fe} whose magnitude varies between 25 and 100 percent of the change in the S-parameter.

S-parameter measurements made on an R-C network with a delay-time of 665 ps mounted on a TO-5 transistor header have disclosed series resonances in the vicinity of 200 and 400 MHz caused by the inductance of the leads. An improved version mounted on a TO-72 header is planned for use as a control in the interlaboratory comparison. The resonant frequencies obtained for the TO-5 header device are reasonably close to those computed from a knowledge of the fabrication steps. Measurements such as these made using the S-parameter equipment facilitate the analyses of delay-time instruments, such as the Sandia bridge, designed to operate at lower frequencies, e.g. 1 to 30 MHz, by providing a more accurate representation of the equivalent circuit for the R-C plug-in element.

The effect of case temperature on S-parameter measurements has been determined qualitatively. The results indicate that the power dissipated at any of the proposed bias levels is low enough that temperature effects are not a problem.

(G. J. Rogers and F. H. Brewer)

<u>Plans</u>: The work specifying the error sources in delay-time measurement instruments will continue. The format specifying the laboratory procedure for intercomparison of S-parameter measurements will be completed and tested using an automatic network analyzer facility. It is anticipated that the portion of the project work concerned with the probe measurement of high-frequency characteristics of transistors while the devices are at the wafe- stage of preparation will receive increased attention.

5.4. REFERENCES

5.1. Thermal Properties of Devices

1. Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, *Proceedings of the 1972 IEEE Reliability Physics Symposium*, Las Vegas, Nevada, April 5-7, 1972.

APPENDIX A
JOINT PROGRAM STAFF

Coordinator: J. C. French

Consultant: C. P. Marsden

Semiconductor Characterization Section

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Semiconductor Processing Section

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Mrs. S. A. Davis+	H. K. Kessler	Y. M. Liu
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Electron Devices Section

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Miss B. S. Hope+	Miss C. A. Main§	S. Rubin
R. L. Gladhill	F. F. Oettinger	D. E. Sawyer
F. R. Kelly*		L. R. Williams

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* Part Time

\+ Secretary

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APPENDIX B
COMMITTEE ACTIVITIES

ASTM Committee F-1 on Electronics

- C. F. Bolton, Committee Assistant Secretary
- W. M. Bullis, Editor, Subcommittee 4, Semiconductor Crystals; Leaks, Resistivity, Mobility, Dielectrics, and Compound Semiconductors Sections
- J. R. Ehrstein, Chairman, Resistivity Section; Epitaxial Resistivity, and Epitaxial Thickness Sections
- J. C. French, Committee Editor
- G. G. Harman, Secretary, Interconnection Bonding Section
- K. O. Leedy, Chairman, Interconnection Bonding Section
- T. F. Leedy, Photoresist and Dielectrics Sections
- C. P. Marsden, Committee Secretary
- R. L. Mattis, Lifetime Section
- W. E. Phillips, Chairman, Lifetime Section; Secretary, Subcommittee 4, Semiconductor Crystals; Crystal Perfection, Dielectrics, Encapsulation, Thin Films, and Thick Films Sections
- A. H. Sher, Germanium Section
- W. R. Thurber, Mobility, Germanium, Compound Semiconductors, and Impurities in Semiconductors Sections

ASTM Committee E-10 on Radioisotopes and Radiation Effects

- W. M. Bullis, Subcommittee 7, Radiation Effects on Electronic Materials
- J. C. French, Subcommittee 7, Radiation Effects on Electronic Materials

Electronic Industries Association: Solid State Products Division, Joint Electron Device Engineering Council (JEDEC)

- J. M. Kenney, Microwave Diode Measurements, Committee JC-21 on UHF and Microwave Diodes
- F. F. Oettinger, Chairman, Task Group JC-11.3-1 on Thermal Considerations for Microelectronic Devices, Committee JC-11 on Mechanical Standardization; Technical Advisor, Thermal Resistance Measurements, Committees JC-22 on Rectifier Diodes and Thyristors, JC-20 on Signal Diodes, JC-25 on Power Transistors, and JC-30 on Hybrid Integrated Circuits
- S. Rubin, Chairman, Council Task Group on Galvanomagnetic Devices
- D. E. Sawyer, Task Group JC-24-5 on Transistor Scattering Parameter Measurement Standard, Committee JC-24 on Low Power Transistors
- H. A. Schafft, Technical Advisor, Second Breakdown and Related Specifications, Committee JC-25 on Power Transistors

APPENDIX B

IEEE Electron Devices Group:

J. C. French, Standards Committee

J. M. Kenney, Chairman, Standards Committee Task Force on Microwave Solid-State Devices II (Mixer and Video Detector Diodes)

H. A. Schafft, Chairman, Standards Committee Task Force on Second Breakdown Measurement Standards

IEEE Magnetics Group

S. Rubin, Chairman, Galvanomagnetic Standards Subcommittee

IEEE Parts, Hybrids, and Packaging Group

W. M. Bullis, New Technology Subcommittee, Technical Committee on Hybrid Microelectronics

Society of Automotive Engineers

J. C. French, Subcommittee A-2N on Radiation Hardness and Nuclear Survivability

W. M. Bullis, Planning Subcommittee of Committee H on Electronic Materials and Processes

IEC TC47, Semiconductor Devices and Integrated Circuits:

S. Rubin, Technical Expert, Galvanomagnetic Devices; U.S. Specialist for Working Group 5 on Hall Devices and Magnetroresistive Devices

NMAB *ad hoc* Committee on Materials and Processes for Electron Devices

W. M. Bullis

NMAB *ad hoc* Committee on Materials for Radiation Detection Devices

D. E. Sawyer

APPENDIX C
SOLID-STATE TECHNOLOGY & FABRICATION SERVICES

Technical services in areas of competence are provided to other NBS activities and other government agencies as they are requested. Usually these are short-term, specialized services that cannot be obtained through normal commercial channels. Such services provided during the last quarter are listed below and indicate the kinds of technology available to the program.

1. Channel Electron Multipliers (Y. M. Liu)*

A study was begun for the NASA Goddard Space Flight Center to evaluate the performance and long-term stability of channel electron multipliers to be used in low-energy charged-particle experiments in the NASA Atmosphere Explorer Satellite series.

2. Active Probe (T. F. Leedy)

Fabrication was begun on a field effect transistor to be used as an active probe with a relatively flat band-pass from d-c to 1 MHz with an oscilloscope for the NBS Microwave and Mechanical Instrumentation Section.

3. Thin Metal Films (J. Krawczyk)

Thin films of gold, nickel, or chromium were vacuum evaporated onto various polymeric films for fabrication into piezoelectric and pyroelectric detectors by the NBS Instrumentation Applications Section.

4. Radiation Detectors (A. H. Sher and H. E. Dyson)

A lithium-drifted germanium gamma-ray detector fabricated for the study of germanium materials characteristics was loaned to the NBS Photonuclear Physics Section.

5. Electrical Burnout Studies (W. K. Croll and H. A. Schafft)†

Electrical tests and visual and scanning electron microscope examinations were conducted on 24 devices (SN54L00 and SN54H00 quadruple 2-input positive NAND gates) for the Harry Diamond Laboratories to assist in establishing degradation and failure modes.

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* NBS Cost Center 4254429

† NBS Cost Center 4251541

APPENDIX D
JOINT PROGRAM PUBLICATIONS

Prior Reports:

A review of the early work leading to this Program is given in Bullis, W. M., Measurement Methods for the Semiconductor Device Industry — A Review of NBS Activitiy, NBS Tech. Note 511, December, 1969.

Quarterly reports covering the period since July 1, 1968, have been issued under the title Methods of Measurement for Semiconductor Materials, Process Control, and Devices. These reports may be obtained from the Superintendent of Documents (Catalog Number C.13.46:XXX) where XXX is the appropriate technical note number. Microfiche copies are available from the National Technical Information Service (NTIS), Springfield, Virginia 22151.

Quarter Ending	NBS Tech. Note	Date Issued	NTIS Accession No.
September 30, 1968	472	December, 1968	AD 681330
December 31, 1968	475	February, 1969	AD 683808
March 31, 1969	488	July, 1969	AD 692232
June 30, 1969	495	September, 1969	AD 695820
September 30, 1969	520	March, 1970	AD 702883
December 31, 1969	527	May, 1970	AD 710906
March 31, 1970	555	September, 1970	AD 718534
June 30, 1970	560	November, 1970	AD 719976
September 30, 1970	571	April, 1971	AD 723671
December 31, 1970	592	August, 1971	AD 728611
March 31, 1971	598	October, 1971	AD 732553
June 30, 1971	702	November, 1971	AD 734427
September 30, 1971	717	April, 1972	
December 31, 1971	727	June, 1972	

Current Publications:

As various phases of the work are completed, publications are prepared to summarize the results or to describe the work in greater detail. Copies of most of such publications are available and can be obtained on request to the editor or the author. The following publications appeared during the quarter covered by this report or subsequently.

Schafft, H. A., Wire-Bond Electrical Connections: Testing, Fabrication and Degradation, A Bibliography — 1957-1971, Technical Note 593 (January, 1972).

Thurber, W. R., and Bullis, W. M., Resistivity and Carrier Lifetime in Gold-Doped Silicon, AFCRL Report AFCRL-72-0076, January 31, 1972.

Sher, A. H., Keery, W. J., and Dyson, H. E., Improved Infrared Response Measurements in Semiconductor Nuclear Radiation Detectors, *IEEE Trans. Nucl. Sci.* NS-19, No. 1, 341-344 (February, 1972).

Sher, A. H., and Keery, W. J., Improved Infrared-Response Technique for Determining Impurity and Defect Levels in Semiconductors, *Appl. Phys. Lett.* 20, 120-122 (1 February 1972).

Harman, G. G., and Leedy, K. O., An Experimental Model of the Microelectronic Ultrasonic Wire Bonding Mechanism, *Proceedings of the 1972 IEEE Reliability Physics Symposium,* Las Vegas, Nevada, April 5, 1972.

Oettinger, F. F., and Rubin, S., The Use of Current Gain as an Indicator for the Formation of Hot Spots Due to Current Crowding in Power Transistors, *Proceedings of the 1972 IEEE Reliability Physics Symposium,* Las Vegas, Nevada, April 5, 1972.

Sher, A. H., Liu, Y. M., and Keery, W. K., Infrared-Response Measurements on Radiation-Damaged Si(Li) Detectors, *IEEE Trans. Nucl. Sci.* NS-19, No. 3, 312-317 (June, 1972).

Liu, Y. M., and Coleman, J. A., Radiation Damage Effects by Electrons, Protons and Neutrons in Si(Li) Detectors, *IEEE Trans. Nucl. Sci.* NS-19, No. 3, 346-352 (June, 1972).

Marsden, C. P., Tabulation of Published Data on Electron Devices of the U.S.S.R. Through December 1971, NBS Technical Note 715 (June, 1972). (Supersedes NBS Technical Note 526).

Schafft, H. A., Testing and Fabrication of Wire-Bond Electrical Connections, NBS Technical Note 726 (August, 1972).

Phillips, W. E., Interpretation of Steady-State Surface Photovoltage Measurements in Epitaxial Semiconductor Layers, to be published in *Solid-State Electronics.*