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MODIFICATIONS TO THE MED AND LED SOURCE-ENCODING CIRCUITRY FOR THE IMP H AND J SPACECRAFT

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GODDARD SPACE FLIGHT CENTER
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GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland

NOTE

At the time of publication there exists three sets of MED and LED cards. These are designated:

1. The IMP-H MED and LED Flight

2. The IMP-H MED and LED Flight Spares

3. The IMP-J MED and LED Flight

Sets Nos. 2 and 3 above received all the modifications described herein; set No. 1 did not receive the modification covering "MED-Analysis of new event," page 2 (sub-commutation), and "LED-Analysis of new event," page 3 (sub-commutation). After launch of the No. 1 set, the No. 2 set will be re-designated the IMP-J MED and LED Flight and the No. 3 set redesignated the IMP-J MED and LED Flight Spares.

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MODIFICATIONS TO THE MED AND LED SOURCE-ENCODING CIRCUITRY FOR THE IMP H AND J SPACECRAFT

INTRODUCTION

Subsequent to the publication of the IMP-I reports, X-711-71-345, August 1971, covering the Low-Energy Cosmic Ray Experiment, and report X-711-71-271, August 1971, covering the Medium-Energy Cosmic Ray Experiment, several modifications were made in the method of reading the particle-impact rates and coincident-event analyses in the later IMP series H and J. This report covers the circuitry and fabrication changes made on the MED and LED electronics cards for the IMP H and J. Except for the noted changes, the circuitry and module-matrix arrangement is essentially the same as the IMP-I electronics cards described in the above X reports.

The rates measurement in the IMP-I electronics cards for the received events were initiated in sections of the logic network which were subject to a systems-busy inhibit pulse (called the Priority Logic Inhibit, or PLI) which deactivated this area after an event was accepted for pulse-height analysis. It was later decided that significant information would be provided by the event-impact rates if this inhibit interruption, necessary for event processing, was separated from the rates circuitry to provide a continuous rates measurement. In addition, analysis of the IMP-I transmitted data indicated the desirability of incorporating additional coincident-event threshold detection levels to further discriminate between received particles. What follows describes the new circuitry added to accomplish these functions.

MED–PRIORITY LOGIC INHIBIT BYPASS

A new module, Fig. 1, called the Sectoring Pulse Generator (MED), schematic 1331-925, artwork 02-428, was designed and fabricated to perform the necessary non-valid F and G event inhibiting but without the event-processing inhibit PLI pulse circuitry. This new module was interposed in the MED matrix between the logic and rates-selecting modules and the existing tap-offs from the logic pulse generators were moved back, ahead of the PLI pulse input point. Additional taps were taken from the F and G logic pulse generators for the separate inhibit requirements. Specifically, (1) Event $DI \cdot E \cdot F \cdot \overline{G} \cdot \overline{PLI}$, formerly from the F and G Inhibit Logic module, schematic 1156-764, artwork 02-269, pin 15, then thru a 2A Amplifier module, schematic 1156-786, artwork 02-284, position A-14, now is tapped off the junction of tunnel diodes CR1-CR2 in the F and G Inhibit Logic module as event $DI \cdot E \cdot F$ and sent to pin

10 of the new module. The 2A Amplifier module position A-14 is eliminated. (2) Event $DI \cdot E \cdot \overline{F} \cdot \overline{G} \cdot \overline{PLI}$, formerly from the same F and G Inhibit module, pin 17, then through another 2A Amplifier module, position A-13, is now tapped off the junction of tunnel diodes CR8-CR9 in the F and G Inhibit Logic as event $DI \cdot E$ and sent to pin 12 of the new module. The 2A Amplifier module, position A-13, is eliminated. (3) Event $(D1 + E1)_2 E \cdot \overline{F} \cdot \overline{G} \cdot \overline{PLI}$, formerly from the same F and G Inhibit module, pin 16, then through a 2A Amplifier module, position A-12, is now tapped off the junction of tunnel diodes CR12-CR13 in the F and G Inhibit Logic as event $(D1+ E1)_2 E$ and sent to pin 12 of the new module. The 2A Amplifier module, position A-12, is eliminated.

Three pulse generators in the new module, with input circuit inhibiting, generate the events (1) $DI \cdot E \cdot F \cdot \overline{G}$, (2) $DI \cdot E \cdot \overline{F} \cdot \overline{G}$, and (3) $(D1 + E1)_2 E \cdot \overline{F} \cdot \overline{G}$. Required inhibits Fm and Gm come in on pins 8, 9, and 16, with Gm having two inputs because of different voltage level requirements. New 2A amplifier circuitry is contained within the new module to replace the separate modules eliminated. It is interposed in the matrix section feeding the rates-selecting modules which are (1) Four-input Commutator, schematic 1156-780, artwork 02-300; (2) Two-input Switch and Commutator, schematic 1156-788, artwork 02-285; and (3) Triple two-input Switch A, schematic 1156-779, artwork 02-309.

MED - ANALYSIS OF NEW EVENT

A second module was added to identify and pulse-height analyze a new event $DI \cdot E \cdot \overline{F} \cdot \overline{G} (DI + EI)_1$, by time-sharing it with existing event $DI \cdot E \cdot \overline{F} \cdot \overline{G}$ into pin 10 of the Central Logic module, schematic 1156-761, artwork 02-272. This new module is the Event-Type Sub-Commutator (MED), schematic 1334-952, artwork 02-459. Time sharing is accomplished by sub-commutation from bus A4, pin 13, of the Two-input Switch and Commutator, schematic 1156-788, artwork 02-285.

MED CIRCUIT OPERATION

Figure 3 shows the circuit signal flow; figure 4, the waveforms; and figure 2 the module schematic. The new module consists of a 2-input AND gate, Q3Q4Q5, interposed directly in the pin 10 input line of the Central Logic. One AND input, Q3, receives the $DI \cdot E \cdot \overline{F} \cdot \overline{G}$ event and the other, Q4, receives the output of a 2-input OR gate, CR1-CR2. The OR gate receives event $(D1+ E1)_1$ through diode CR1 which, when coincident with event $DI \cdot E \cdot \overline{F} \cdot \overline{G}$ into Q3, provides an output from the A5 AND gate to pin 10 of the Central Logic.

The other leg of the OR gate, diode CR2, receives a ±3 volt level from a flip-flop used to sub-commutate the A4 input bus from the 2-input switch and commutator, schematic 1156-788. The sub-commutating is performed by ANDing A4 with the set pulse from the Sequence Drive module, schematic 1156-769, artwork 02-280. Fig. 5 is an abbreviated portion of the MED module interconnect showing insertion of the new IMP-H-J modules. The matrix changes (not included) are shown on artwork 02-313 sheets 1 and 2, revision H.

LED - PRIORITY LOGIC INHIBIT BYPASS

A new module, Fig. 6, called the Priority Logic Inhibit Bypass (LED) schematic 1331-924, artwork 02-429, was designed and fabricated to perform the necessary non-valid event inhibiting but without the event-processing inhibit PLI pulse circuitry. This new module was interposed in the LED matrix between the logic and rates-selecting modules, and the existing tap-offs from the logic pulse generators were moved back ahead of the PLI pulse input point. Additional taps were taken from the A and (A+B) logic pulse generators for the separate inhibit requirements. Specifically, (1) Event $A1 \cdot B \cdot \overline{C} \cdot \overline{PLI}$, formerly from pin 15 of the (A+B) Logic module, schematic 1156-782, artwork 02-305, then through a 2A amplifier module, schematic 1156-786, artwork 02-284, position A-7, now is tapped off the junction of tunnel diodes CR7-CR8 in the (A+B) Logic module as event $A1 \cdot B$, and sent to pin 9 of the new module. The 2A amplifier module, position A-7, is eliminated. (2) Event $A1 \cdot \overline{B} \cdot \overline{C} \cdot \overline{PLI}$, formerly from pin 13 of the A Logic module, schematic 1156-783, artwork 02-304, then through a Pulse Generator module, schematic 1156-790, artwork 02-311, position PG-2, now is tapped off the junction of tunnel diodes CR1-CR2, in the A Logic module as event A1, and sent to pin 10 of the new module. Pulse Generator position PG-2 being eliminated. (3) Event $(A+B) \cdot \overline{B} \cdot \overline{C} \cdot \overline{PLI}$, formerly from pin 14 of the A Logic module, then through a Pulse Generator module, position PG-1, now is tapped off the junction of tunnel diodes CR5-CR6 in the A Logic module as event (A+B), and sent to pin 11 of the new module. The Pulse Generator module, position PG-1, being eliminated. The Bm and Cm inhibit functions are tapped off DC Amplifiers, positions A-5 and A-6, and brought to the new module; necessary matching gains are provided within the module.

LED - ANALYSES OF NEW EVENT

The LED has also been modified to identify another event similar to the (A+B) event but with a lower threshold detection level. This new event level has been designated $(A+B)_2$ and the former (A+B) event redesignated $(A+B)_1$.

An input from the encoder commutator bus designated a_6 (formerly a_3) is used to sub-commutate the new $(A+B)_2$ event; when a_6 reads '1' the new event is ANDed with event $A1 \cdot B \cdot \overline{C}$ or event $A1 \cdot B \cdot \overline{C}$, if coincident, and sent to pin 9 of the Central Logic module. When commutator bus a_6 is '0', the $A \cdot B \cdot \overline{C}$ or $A \cdot \overline{B} \cdot \overline{C}$ events are read out in the usual manner. The ANDed outputs are also sent to the 8-Input Switch module, replacing the IA1 and IA2 inputs, where they are counted as rates. Two new modules were added to accomplish this, the Event Type Sub-Commutator (LED), Fig. 7, schematic 1334-955, artwork 02-460, and the Sub-Commutator interface module, Fig. 8, schematic 1334-959, artwork 24-002.

LED CIRCUIT OPERATION

Fig. 9 shows the signal flow for the new LED Event Type Sub-Commutator and Fig. 10 the waveforms. It receives event (A+B) from the junction of resistors R3-R4-R5 in the Emitter Follower module, schematic 1156-785, artwork 02-302. This input, pin 8, is buffered by 2A amplifier circuit, Q1-Q2, then fed to a threshold-detector spiker, Q3-Q4, whose trigger detection level is set by TBD resistor R10. This new threshold detection level identifies the event as $(A+B)_2$. The spiker then triggers a pulse generator, Q5-Q6, which sets the coincident-determining pulse width for the following parallel-input AND gates. The L1 generated pulse width must be wide enough (about 6 microseconds) to catch either (they are mutually exclusive) input event pulse on pins 12 or 13. As shown on waveforms 1334-958, Fig. 10, when coincident, the new event $(A+B)_2$ is ANDed with either event $A1 \cdot B \cdot \overline{C}$ or event $A1 \cdot \overline{B} \cdot \overline{C}$. These new coincident events feed the Central Logic inputs, to be processed and pulse-height analyzed.

The above action occurs only for an encoder commutator A_6 bus state of "1'. For an A_6 bus state of "0", AND gate Q18-Q19 remains closed and the sequence reset pulse on pin 11 of 1334-955 places the A'_6 side of the flip-flop, Q20-Q26, into a "0" (neg.) state. The OR circuit, CR4-CR5, receives this A'_6 bus thru a level-setting TBD resistor, R37, which clamps one leg each of the two parallel AND gates into and ON state (electrically OFF). This permits the regular events to pass through without the presence of new event $(A+B)_2$. TBD resistor R35 is also a level setting resistor for event $(A+B)_2$ feeding diode CR-4. A low-drain input switching module, the Sub Commutator Interface, feeds the A_6 input AND gate, Q18 and Q19.

Fig. 11 is an abbreviated portion of the LED module interconnect showing insertion of the new IMP-H-J modules. The matrix changes (not included) are shown on artwork 02-235, sheets 1 and 2, revision K.

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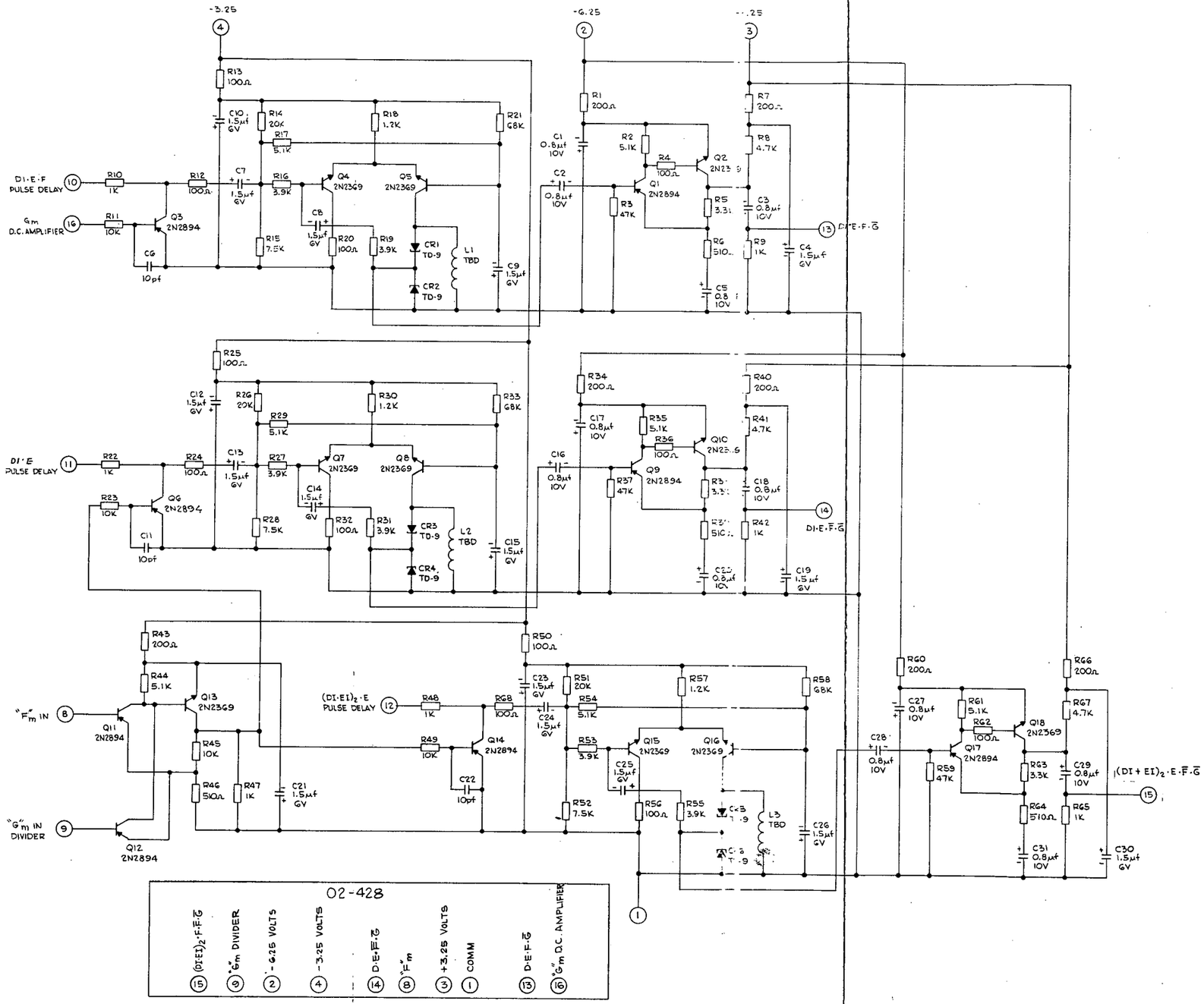

Figure 1. Sectoring Pulse Generator (MED), Schematic 1331-925

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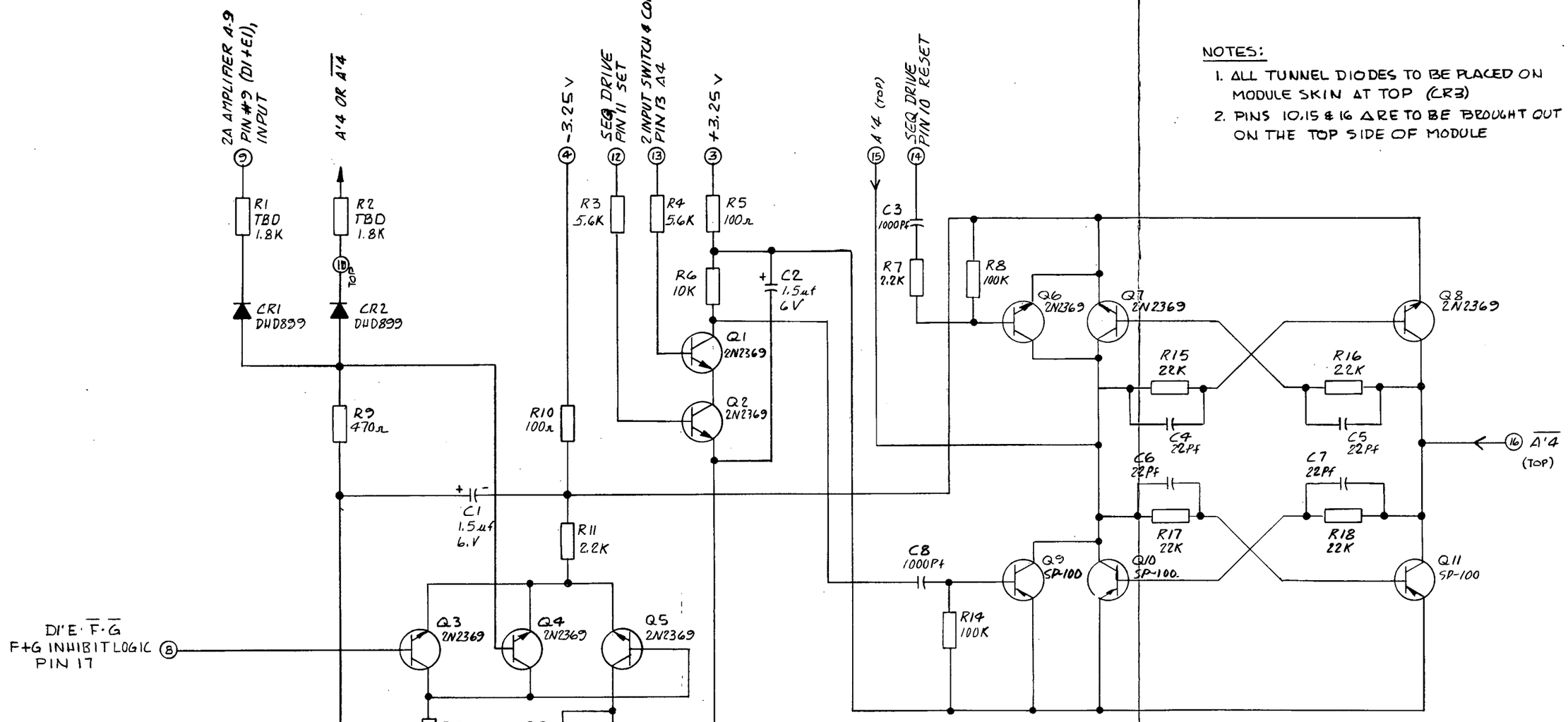

NOTES:

1. ALL TUNNEL DIODES TO BE PLACED ON MODULE SKIN AT TOP (CR3)
2. PINS 10,15 & 16 ARE TO BE BROUGHT OUT ON THE TOP SIDE OF MODULE

Figure 2. Event Type Sub-Commutator (MED), Schematic 1334-952

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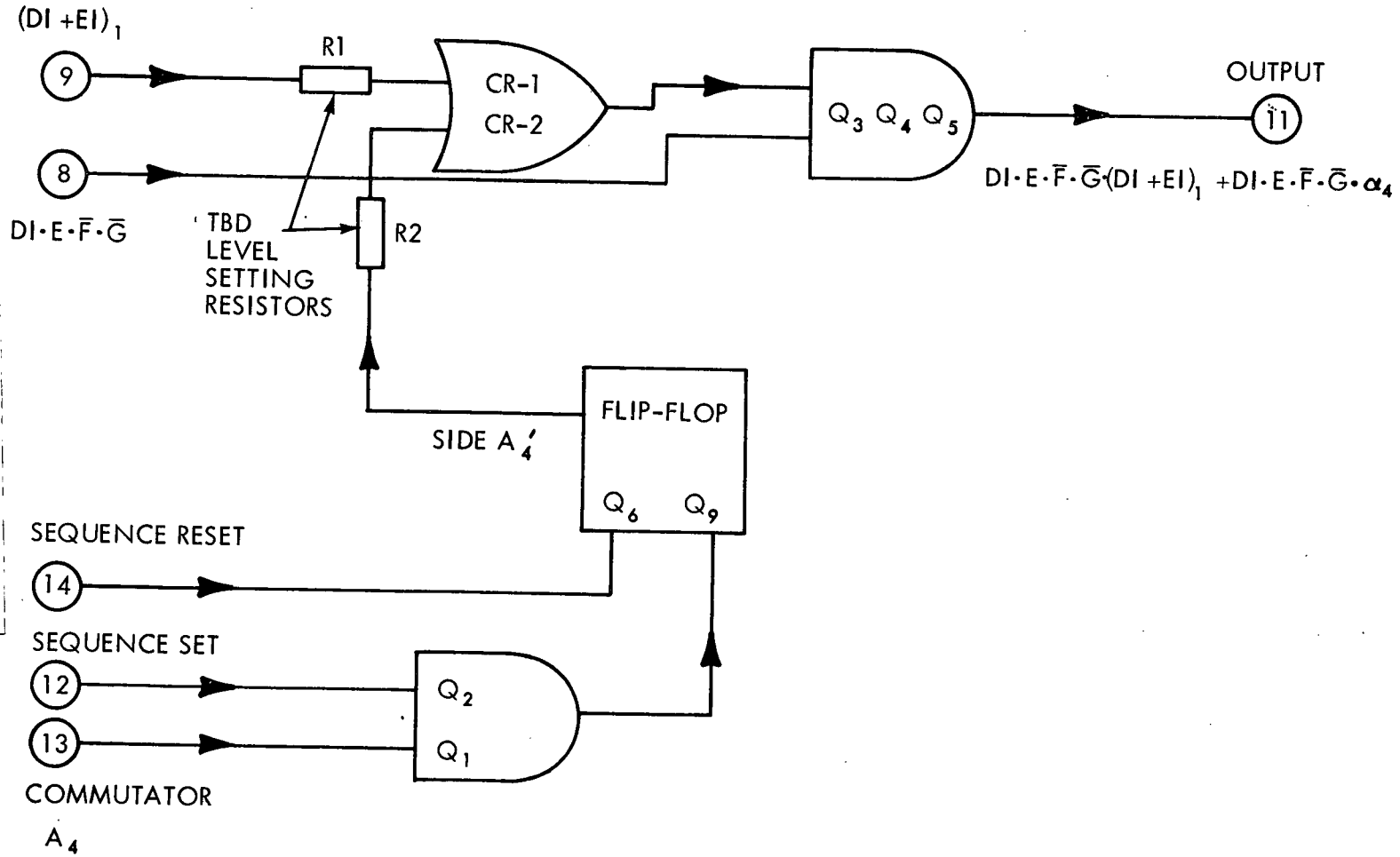

Figure 3. Signal Flow, Event Type Sub-Commutator (MED)

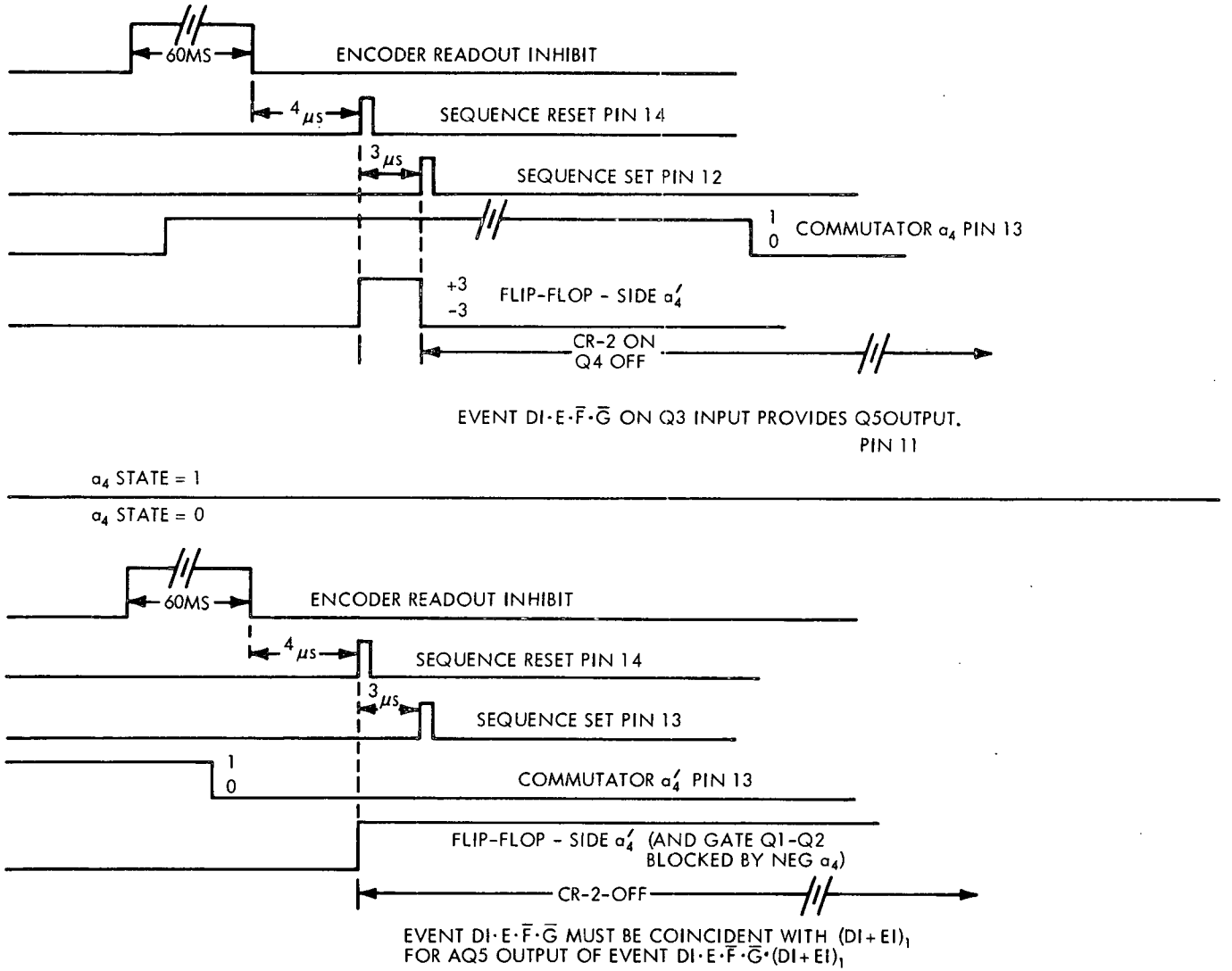

Figure 4. Waveforms, Event Type Sub-Commutator (MED)

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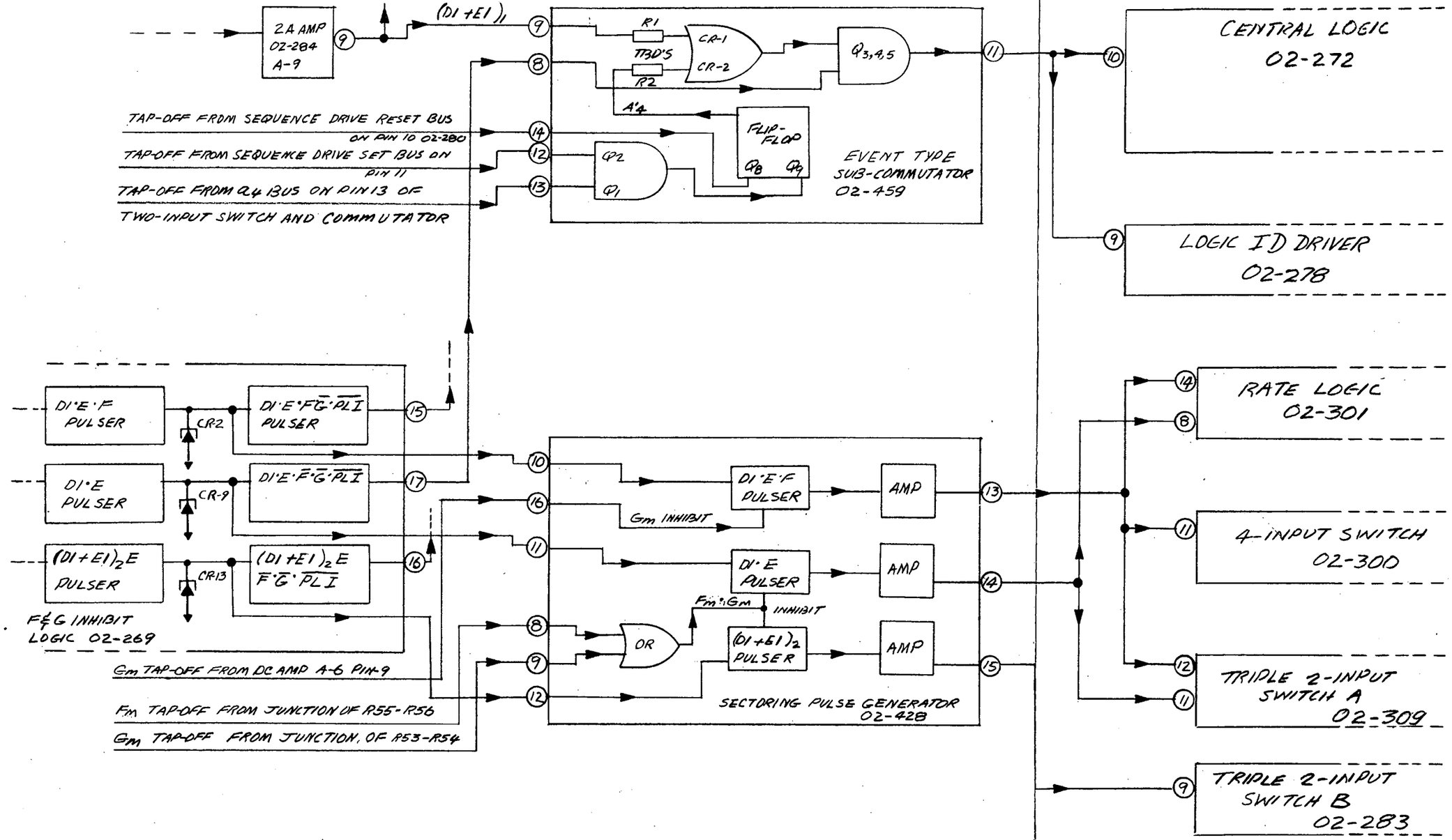

Figure 5. Abbreviated Module Interconnect for MED, IMP H and J (1340-578)

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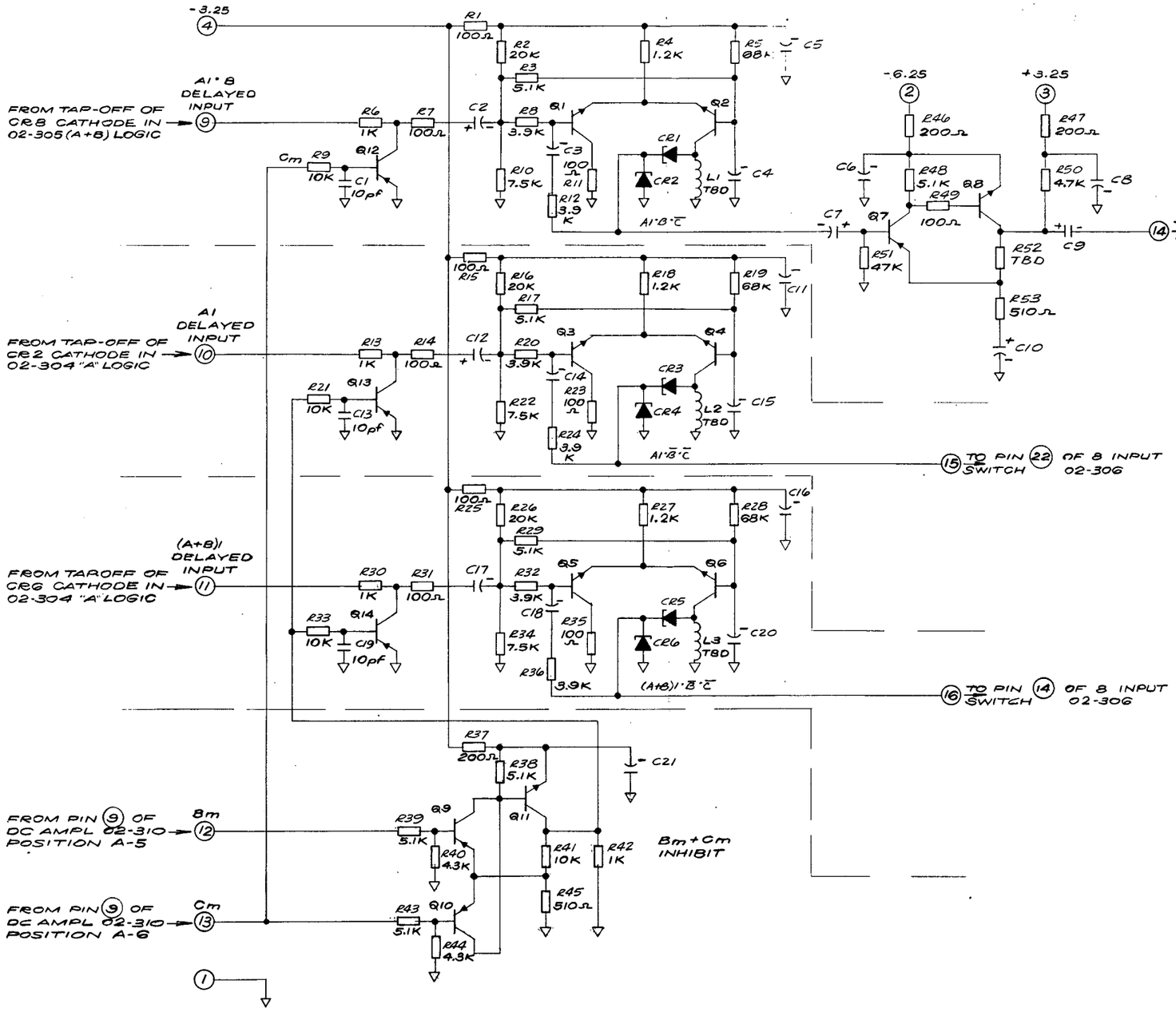

NOTES:

1. EXCEPT AS NOTED:
   ALL CAPACITORS ARE 1.5μf/6V TYPE J.
   ALL PNP TRANSISTORS ARE SP-100.
   ALL NPN TRANSISTORS ABE 2N2369.
2. MATCH BETA'S (OVER 20) FOR PAIRED Q1-Q2; Q3-Q4; Q5-Q6.
   MINIMUM BETA OF 50 FOR Q12; Q13; Q14.
   ALL OTHER BETA'S OVER 20.
3. THESE MODULES REPLACE MODULES IN POSITIONS A-7; PS-2; PS-1.

PIN CODE	
1	COMMON
2	-6.25 VOLTS
3	+3.25 VOLTS
4	-3.25 VOLTS
9	A1' B DELAYED INPUT
10	A1 DELAYED INPUT
11	(A+B)1 DELAYED INPUT
12	Bm INPUT
13	Cm INPUT
14	A1'B'C OUTPUT
15	A1'B'C OUTPUT
16	(A+B)1'B'C OUTPUT

MODULE 02-429

Figure 6. Priority Logic Inhibit Bypass (LED), Schematic 1331-924

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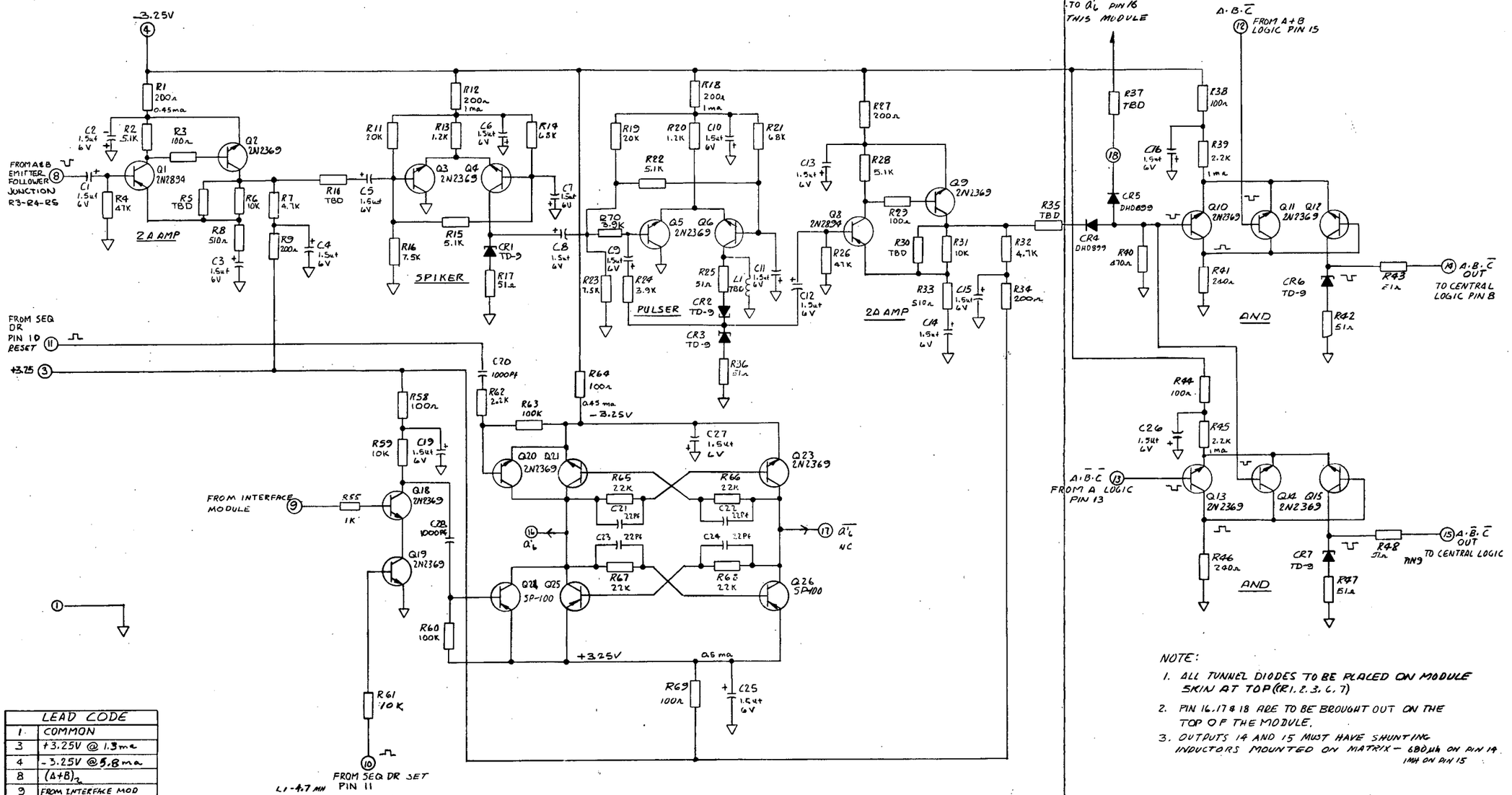

NOTE:

1. ALL TUNNEL DIODES TO BE PLACED ON MODULE SKIN AT TOP (CR1, 2, 3, 6, 7)
2. PIN 16, 17 & 18 ARE TO BE BROUGHT OUT ON THE TOP OF THE MODULE.
3. OUTPUTS 14 AND 15 MUST HAVE SHUNTING INDUCTORS MOUNTED ON MATRIX – 680 μH ON PIN 14, 1 MH ON PIN 15

	LEAD CODE
1	COMMON
3	+3.25V @ 1.3ma
4	-3.25V @ 5.8ma
8	(A+B)$_2$
9	FROM INTERFACE MOD
10	SEQUENCE SET
11	SEQUENCE RESET
12	$A \cdot B \cdot \bar{C}$ INPUT
13	$A \cdot \bar{B} \cdot \bar{C}$ INPUT
14	$A \cdot B \cdot \bar{C}$ OUTPUT
15	$A \cdot \bar{B} \cdot \bar{C}$ OUTPUT
16	a'_L
17	$\bar{a}'_L$
18	a'_L OR $\bar{a}'_L$

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Figure 7. Event Type Sub-Commutator (LED), Schematic 1334-955

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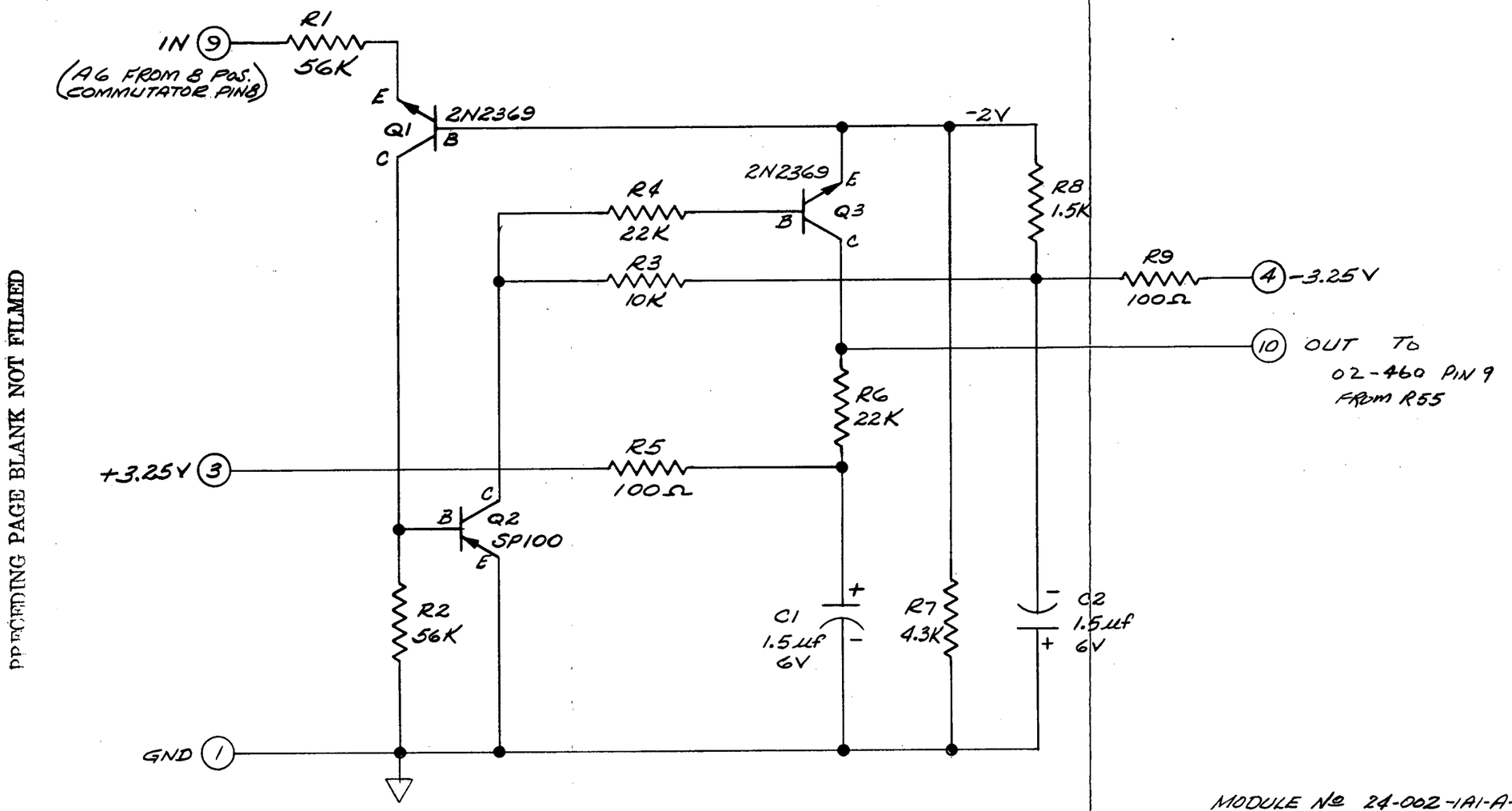

PIN	LEAD CODE
1	GND
3	+3.25
4	-3.25
9	A6 FROM 8 POS. COMM.
10	OUT TO 02-460

MODULE № 24-002-1A1-A-02
(See WAVEFORMS 1334-958)

Figure 8. Sub-Commutator Interface (LED), Schematic 1334-959

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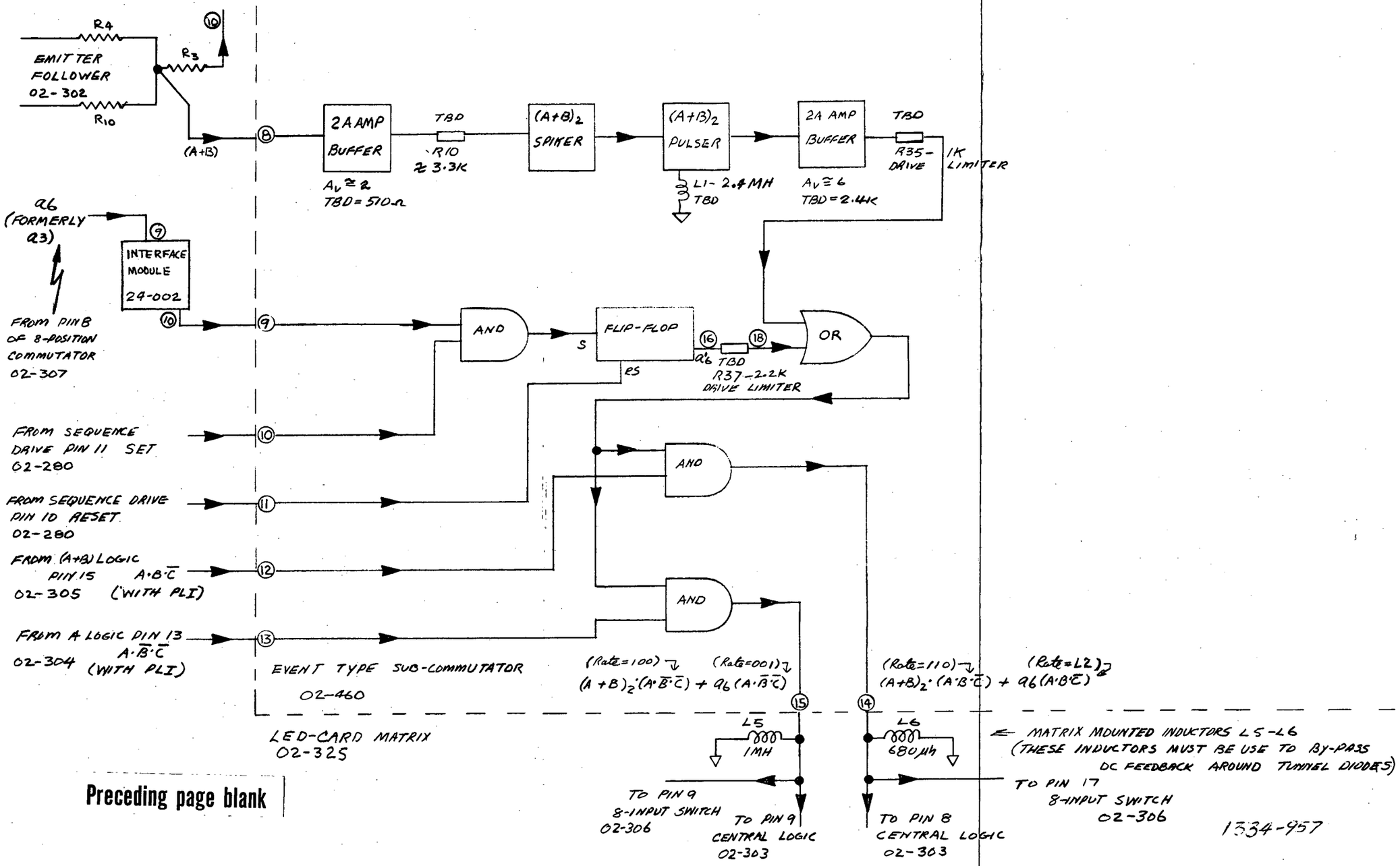

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19.1

Figure 9. Signal Flow, Event Type Sub-Commutator (LED)

19.2

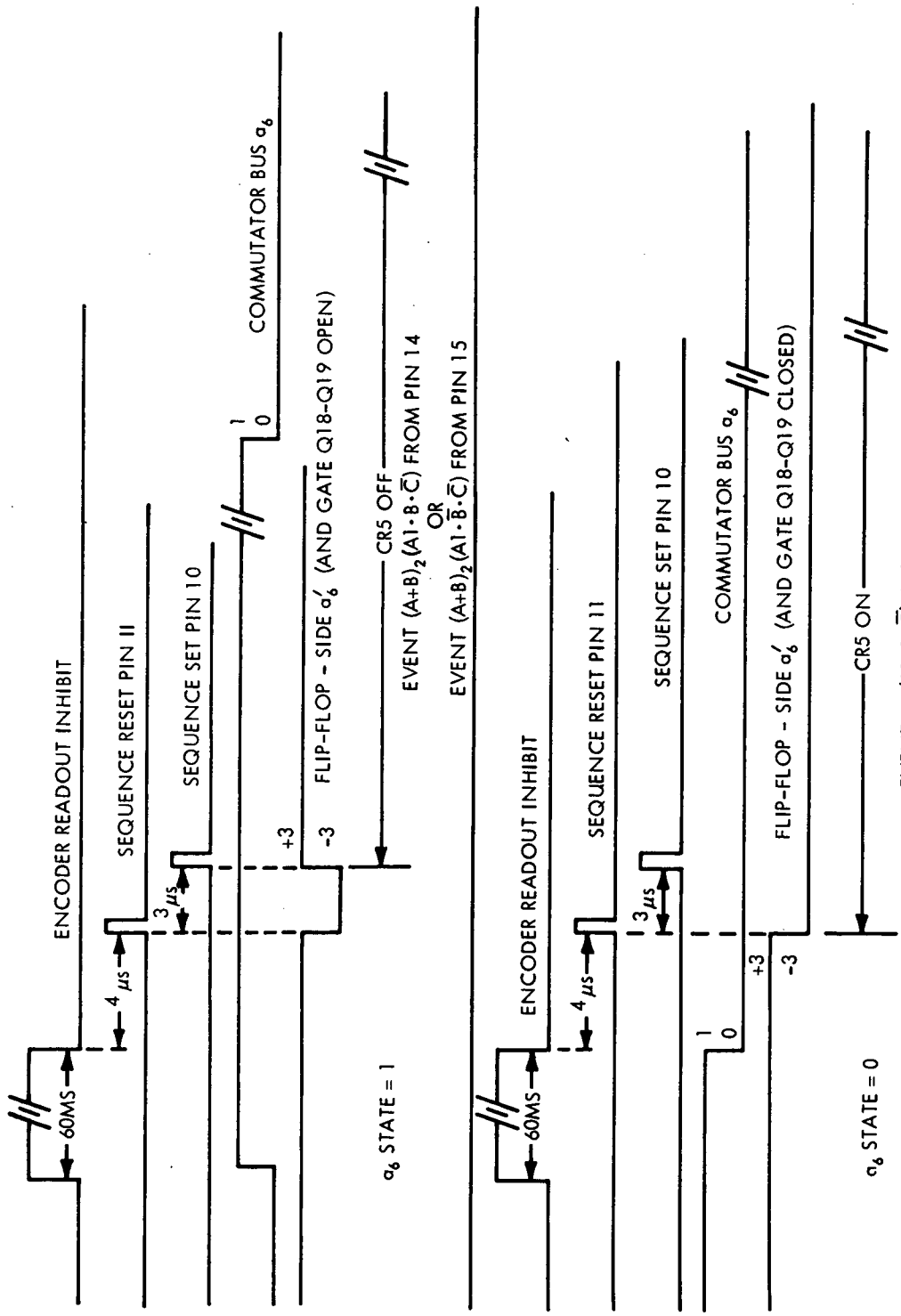

Figure 10. Waveforms, Event Type Sub-Commutator (LED)

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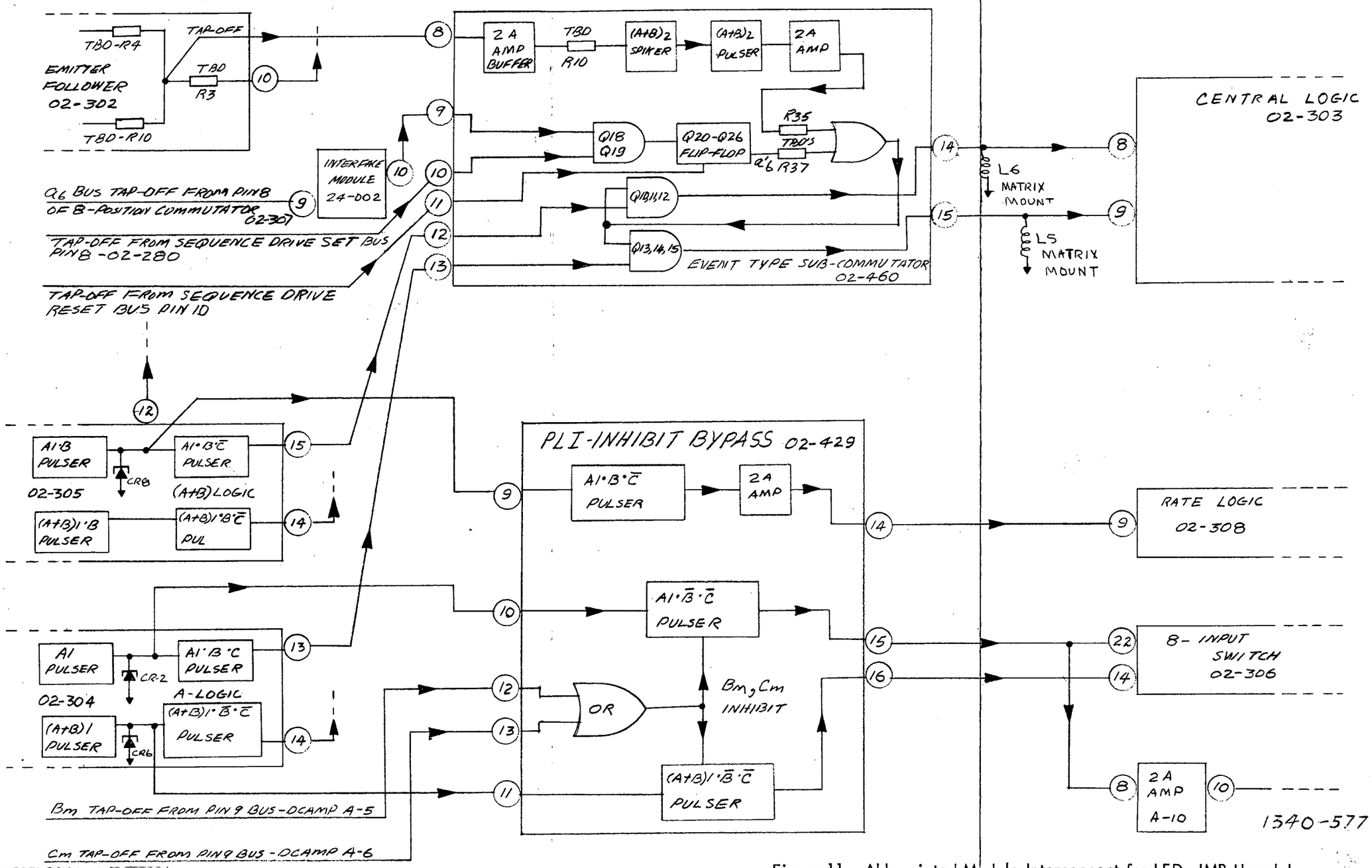

Figure 11. Abbreviated Module Interconnect for LED, IMP H and J

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