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S-BAND MICROCIRCUIT POWER AMPLIFIER

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Final Report

Prepared for
GODDARD SPACE FLIGHT CENTER
Greenbelt, Maryland 20771

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16. Abstract

Final report summarizing research, design, development, and fabrication of a two-stage, solid-state, microcircuit power amplifier operating in the 2.25-GHz region of the S-Band. Output is typically 7.0 watts for an input of approximately 400 mw. Input stage is an MSC 3001 transistor; output stage is an MSC 3005 transistor. Input VSWR is 1.4:1.0, or less. Efficiency of 33.3 percent or more is achieved. Second and third harmonic suppression is 30 db. Operating power is 28 VDC. The entire unit has a length of 3.80 inches, a width of 2.08 inches, and a height of 1.00 inch.

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PREFACE

This report summarizes the work performed by the Systems Division of Radiation, Melbourne, Florida, under Contract NAS5-20197, including production and delivery of one prototype S-Band Microcircuit Power Amplifier (MPA) and twenty flight models. All MPA's were accomplished in conformance with GSFC Specification S-562-P-23, dated 5 May 1969.

Included in the work performed under the subject contract were research of the literature relative to the state of the art, a survey of available devices, experimentation with a number of potential circuit configurations, selection and construction of the final configuration, and tests appropriate to its development and end use.

The S-Band Microcircuit Power Amplifier, as finalized and delivered, fully met the requirements of GSFC Specification S-562-P-23. It is felt that the design approach, technology, and the assembly techniques utilized in the performance of the work, and discussed in Sections 1.0, 2.0, and 3.0. of this report, will form a solid base for future development of similar S-Band technology.

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1.0 DEVELOPMENT

The development effort associated with the S-Band Microcircuit Power Amplifier took place over a period of approximately 12 months, commencing in November 1970. A considerable portion of this effort, in its initial stages, was expended in collecting information on available devices which could be utilized in S-Band power amplifier design. The criteria used in this survey of the state of the art were power efficiency and gain margins.

Following receipt of appropriate vendor information, a number of circuit configurations were constructed and tested. However, because of inadequate device characterizations, the results of these experiments did not come up to expectations in spite of the fact that test jigs had been constructed to permit definitive tests and measurements of all pertinent S-Band parameters.

Among the parameters checked, and which formed design criteria, was transistor parameter spread, especially as it affected the amount of available tuning adjustment. Among other considerations were mechanical packaging and thermal characteristics of the devices under test.

Various mechanical layouts were studied during the development stages of the S-Band Microcircuit Amplifier, with emphasis primarily on three styles of construction. The differences among the three revolved around the number of circuit substrates to be used, the mounting of the device to its heat sink, and the mounting of an output isolator.

The extensive test and selection program resulted in choice of the MSC 3001 device for the input stage of the amplifier and the MSC 3005 for the output stage.

Following preliminary development of the amplifier using the MSC 3001 and MSC 3005, a Preliminary Design Review was held (16 April 1971). In this review, all aspects of the proposed design were investigated and suggestions were made for improvements in size and performance.

For the purpose of selecting the desired MSC 3005 devices, a trip was made to the vendor (Microwave Semiconductor Corporation). The criteria used in selection of the MSC 3005's were power output, efficiency, and gain at 2.3 gigahertz. Thirty devices meeting these critieria were selected.

-transistor

The electrical design effort concentrated on the design of the output circuit to optimize power output from the MSC 3005 ~~transmitter~~. With this data available, the input and interstage circuits were then developed.

In-plant testing of the transistors showed a wider spread of parameters than was anticipated, which caused some difficulty in deriving a suitable circuit. The final design configuration proved to be very satisfactory, however, since it included the ability to adjust circuit parameters to compensate for variations in device parameters.

Fabrication and testing of the prototype unit was completed and the unit was subjected to the Qualification Acceptance Test as described in the test procedure previously submitted to NASA/GSFC. The functional test procedure was altered to allow computer analysis of the test measurements. The test sequence and limits were not altered.

The prototype passed all qualification tests with only a minor deviation, i.e., the input VSWR exceeded the limit of 1.4:1 by a small amount, the amount depending upon temperature and drive conditions. The efficiency degraded from a maximum of 40% (in the center of the band) to a worst-case of 28% at maximum temperature (70°C), the degrading element being the transistors.

An additional test was performed for information purposes only. The unit was subjected to the same temperature extremes (-25°C to 70°C) and a vacuum ranging from 1.5 X 10^{-3} Torr to 1 X 10^{-7} Torr. This data showed no corona problems over the pressure range.

The unit and Qualification Test Data were then forwarded to NASA/GSFC.

The electrical and mechanical characteristics of the final design are presented in table 1-1. Performance is shown in figure 1-1.

Table 1-1. Electrical/Mechanical Characteristics of S-Band MPA

ELECTRICAL CHARACTERISTICS:	
POWER OUTPUT	
TYPICAL (@ 25°C)	7.0 watts
MINIMUM (- 15°C to + 50°C)	6.0 watts
ΔP_o (- 15°C to + 50° C)	± 15% Typical
FREQUENCY	2.25 GHz
HARMONICS (2nd & 3rd)	- 30 db
INPUT VOLTAGE	28 VDC
EFFICIENCY	≥ 33.3%
INPUT LEVEL	≤400 mw
INPUT VSWR	≤1.4:1
MECHANICAL CHARACTERISTICS	
LENGTH	3.80 inches
HEIGHT	1.00 inches
WIDTH	2.08 inches

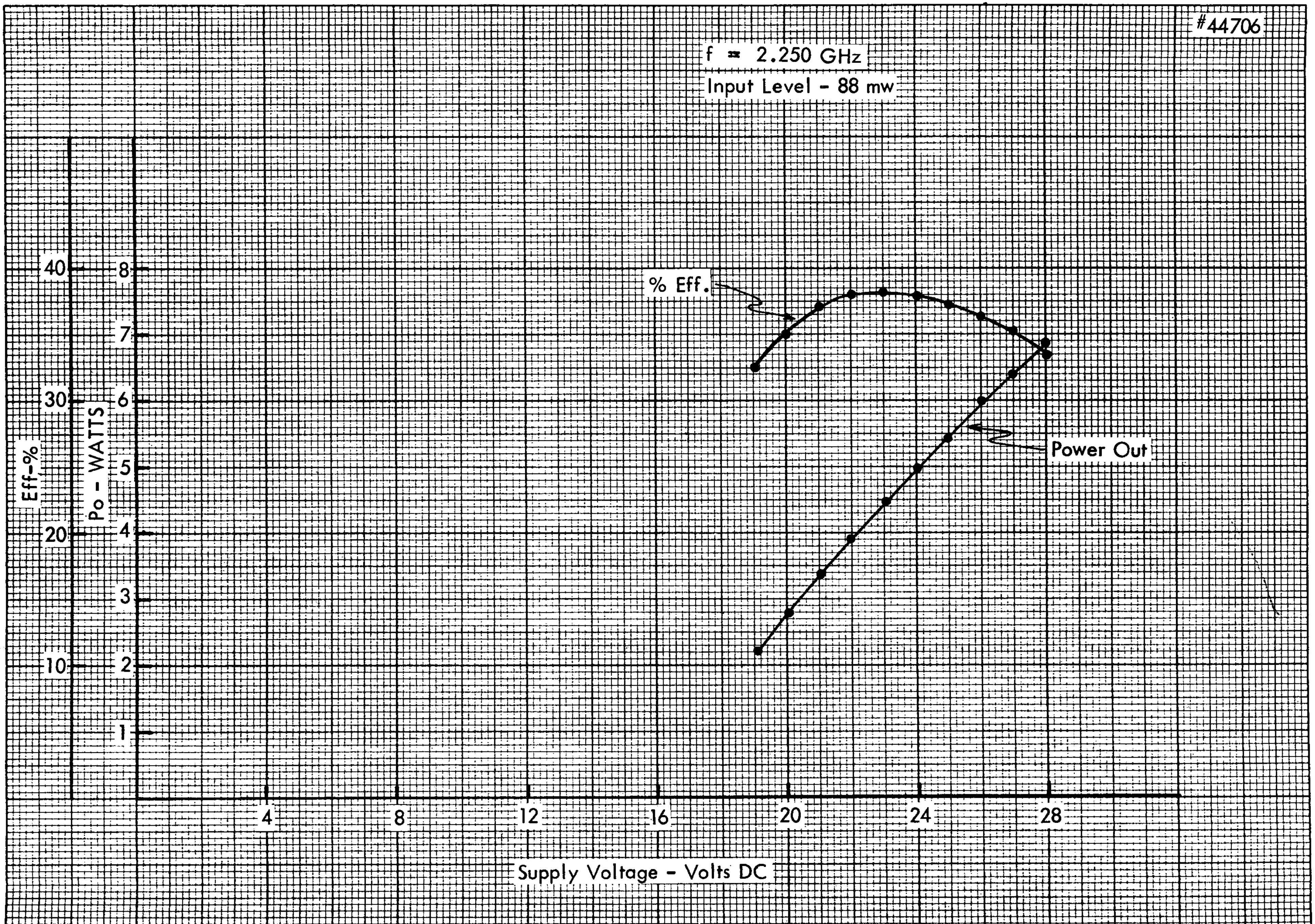

Figure 1-1. Power Output and Efficiency vs Supply Voltage, S-Band MPA Final Design

2.0 FINAL DESIGN

2.1 Device Characterization

The device parameters are of critical importance in the design of the input, output, and interstage matching circuits for the MSC 3001 and MSC 3005. The statistical spread of these parameters over a number of devices required that each matching circuit be adjusted for the specific parameters involved. Device selection was used to minimize circuit adjustment in the design of the S-Band Microcircuit Power Amplifier, but practical considerations, such as device yield, limit the extent to which this method can be employed to reduce the parameter spread. Therefore, it was necessary to carefully characterize parameters of those devices which were used in the prototype and flight units at the power level at which they operate. The method of making these measurements was to mount the device on a test fixture, optimize its performance with tuners on the input and output, and then look into that part of the circuit of interest, using a Hewlett-Packard network analyzer.

The MSC 3005 transistors were selected on the basis of their output power, gain, and collector efficiency. For the vendor visit mentioned in section 1.0, a test circuit was taken to Microwave Semiconductor Corporation in Somerset, N.J., and 30 devices were selected that would produce a minimum of 6.5 watts with a maximum of 1 watt drive (matched with a stub tuner) at a collector efficiency of greater than 35%. This eliminated the need for adjustments on the output circuit, except for the tuning requirement. The devices were then further characterized in Radiation's laboratories to determinine the spread of the input impedance. Typical results for 11 units are given in table 2-1, using the test setup shown in figure 2-1.

The characterization of the MSC 3001 transistors followed a similar process. Since no selection was made on these devices, it was necessary to first characterize their relative performance with respect to power output and efficiency. An output test circuit was designed in which all 25 MSC transistors were operated with the input matched by means of a stub tuner. The resultant data, plotted in figure 2-2, shows the power output capacity of the MSC 3001 devices, which permitted some matching of gain

Table 2-1. MSC 3005 Transistor Profile (Test Frequency 2.25 GHz)

Transistor Number	Input Impedance	Input Drive (mw)	Power Output (watts)	Power Gain (dB)	Collector Current (ma)	DC Input (watts)	Conv. Eff (%)
3	1.4+j6.6	522	6.70	11.10	600	16.80	39.9
4	1.4+j5.4	890	6.60	8.70	600	16.80	39.3
5	1.4+j5.8	940	7.00	8.72	650	18.20	38.5
7	1.5+j5.8	1000	6.70	8.26	620	17.35	38.6
10	1.5+j5.8	1000	6.60	8.20	600	16.80	39.3
11	1.5+j6.4	1000	6.70	8.26	600	16.80	39.9
12	1.4+j6.5	940	7.00	8.72	640	17.90	39.1
13	1.4+j6.70	810	7.00	9.37	620	17.35	40.4
14	1.5+j7.70	920	6.50	8.50	600	16.80	38.7
15	1.5+j6.7	500	6.50	11.14	600	16.80	38.7
16	1.5+j8.5	964	7.00	8.62	620	17.35	40.3

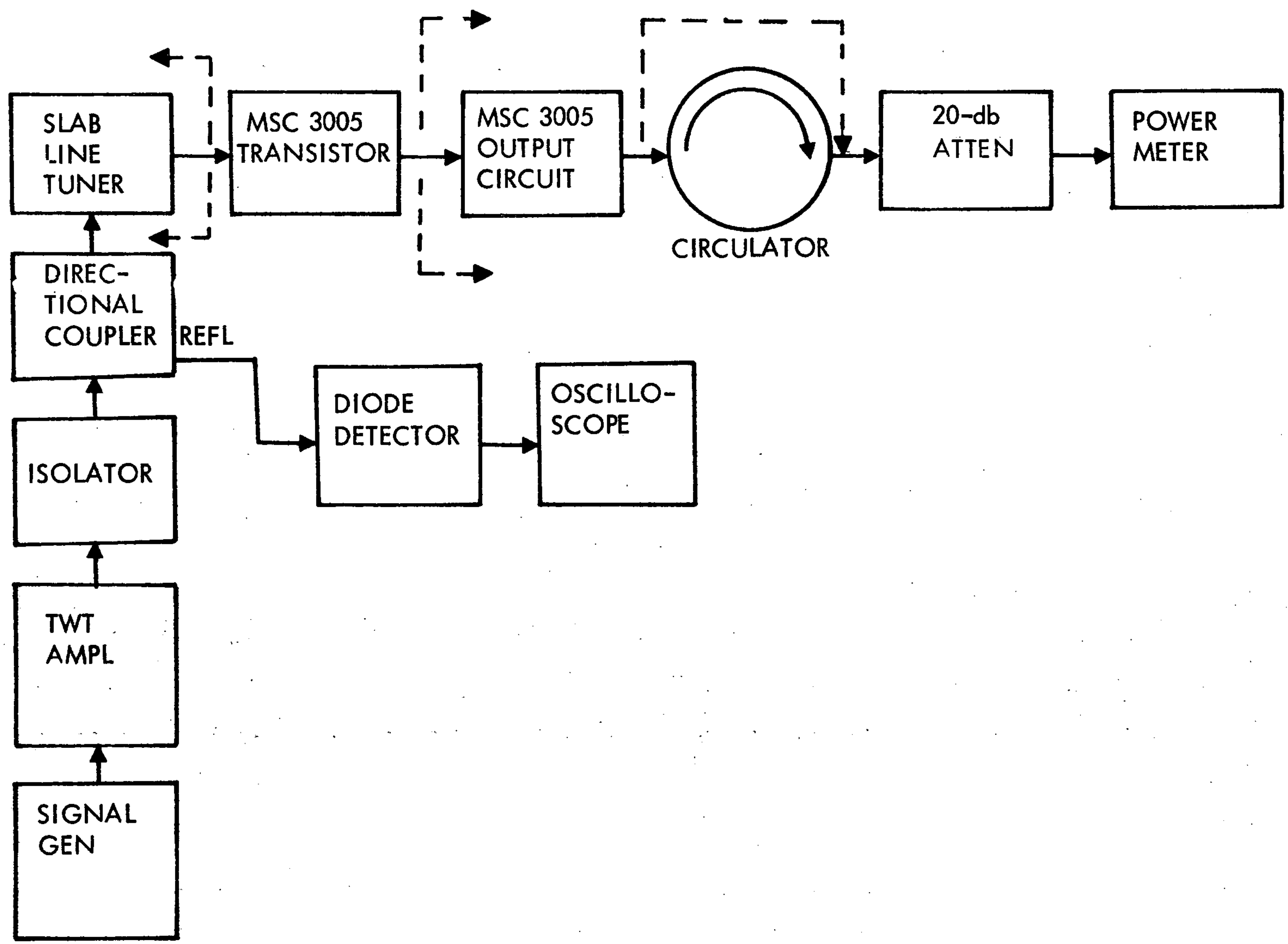

Figure 2-1. Test Setup - Output Circuit Evaluation Using MSC 3005

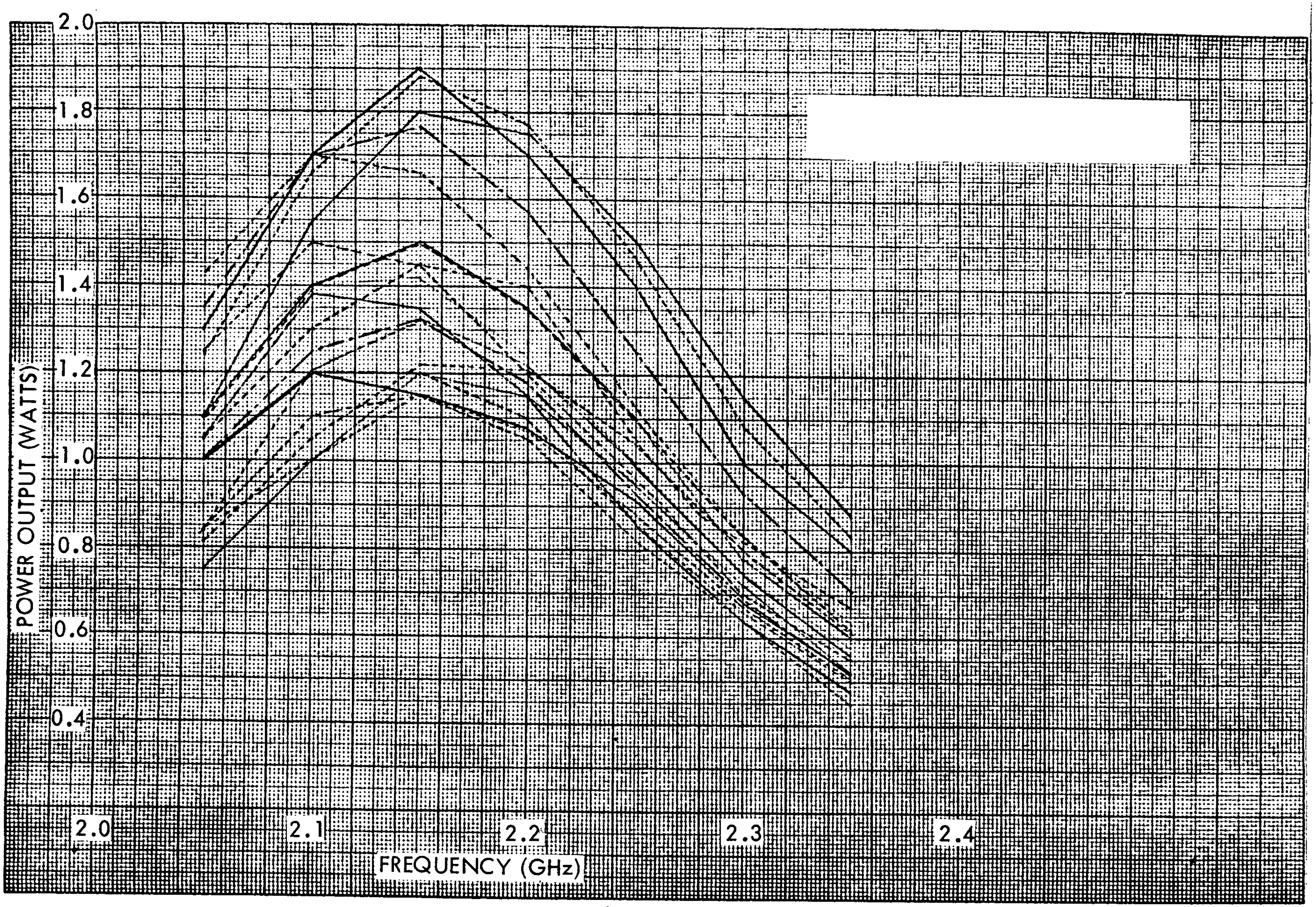

Figure 2-2. Power Output vs Frequency, MSC 3001 Transistors

characteristics between MSC 3005's and MSC 3001's to achieve more uniform overall gain in the final two-stage amplifier. The curves shown in figure 2-2 show that the devices peak out at about 2.15 GHz instead of at band center. This was because the test circuit used was optimum at 100 MHz below band center. However, this data correctly displays relative performance of the devices.

The next step was to perform complete characterization of the MSC 3001 devices. The test setup for this series of tests in shown in figure 2-3. A sample of three transistors was chosen from the spread in figure 2-2. These transistors were then completely characterized for the parameters of interest. This data is shown in table 2-2. The remaining 25 MSC 3001's were similarly characterized at the same time.

2.2 Output Circuit

The finalized output circuit is shown in figure 2-4. This circuit consists of a series of stepped transmission line sections on a 0.5 inch by 1.0 inch substrate, and is the circuit employed in collecting the data shown in table 2-1 using the test setup shown in figure 2-1. The bandwidth of this circuit was evaluated on the computer when driven from the MSC 3005 nominal output impedance and loaded into 50 ohms. The results of this analysis, presented in figure 2-5, show the circuit to have an average 0.2-db bandwidth in excess of 300 MHz. The computer data, as computed, is centered slightly on the low side of band center, 2.25 MHz.

The final design configuration utilizes a variable at the interface of the MSC 3005 collector circuit and the output substrate, in order to accommodate the statistical distribution in the output impedance of the MSC 3005. It was determined that a single-element impedance inverter constructed in microstrip would allow the entire device spread to be matched.

The required variable is shown in figure 2-4 as element "A", where $6.4\ \Omega \leq Zo \leq 15\ \Omega$ and the available length from the edge of the substrate to the edge of the case diameter is used as required. A fixed position of the output device is used, which accommodates an input match more easily and imposes no restriction on the output matching circuit.

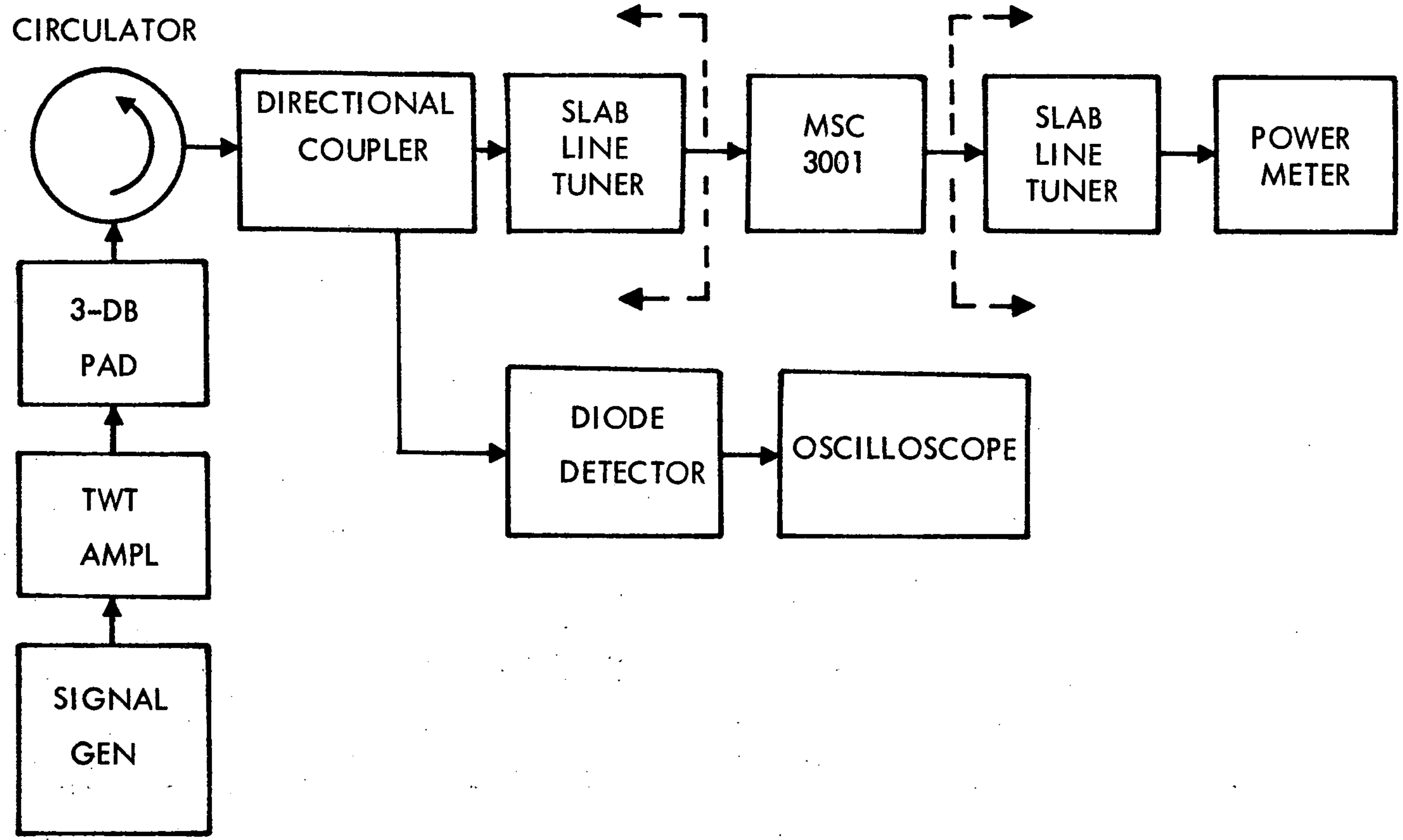

Figure 2-3. Test Setup - MSC 3001 Evaluation

Table 2-2. MSC 3001 Transistor Profile (Test Frequency 2.25 GHz)

Transistor Number	Power Output (watts)	Collector Current (Amp)	Drive Level (W)	Gain (db)	Output Impedance	DC Power In (watts)	Conv. Eff (%)
17	1.15	0.165	0.115	10	6.25-j17.5	4.6	25
4	1.84	0.195	0.170	10.1	6.75-j17.0	5.45	34
6	1.38	0.165	0.142	9.9	6.0-j15.5	4.6	30

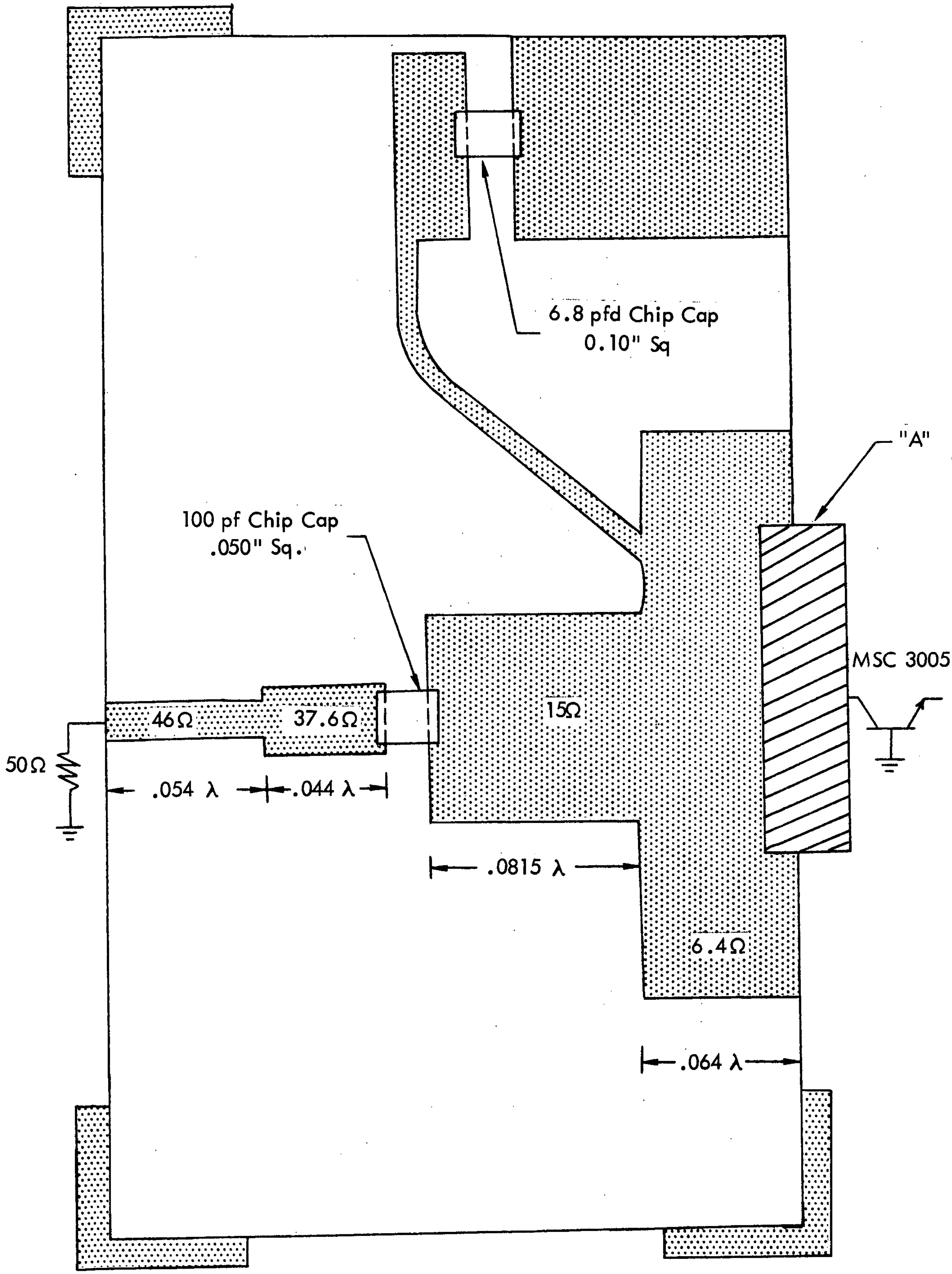

Figure 2-4. MSC 3005 Output Circuit, S-Band MPA

```
ENTER YMIN,YMAX?0.,1.2

AXIS: FROM  0.     TO  1.20   MAJOR INC =  0.20
           I.........I.........I.........I.........I.........I.........I
  2.000   .        +
  2.020   .      +
  2.040   .    +
  2.060   .   +
  2.080   .  +
  2.100   . +
  2.120   . +
  2.140   . +
  2.160   . +
  2.180   .  +
  2.200   .   +
  2.220   .    +
  2.240   .     +
  2.260   .       +
  2.280   .         +
  2.300   .            +
  2.320   .              +
  2.340   .                 +
  2.360   .                    +
  2.380   .                        +
  2.400   .                            +
  2.420   .                                +
  2.440   .                                    +
  2.460   .                                        +
  2.480   .                                             +
  2.500   .                                                 +
COMMAND   ?
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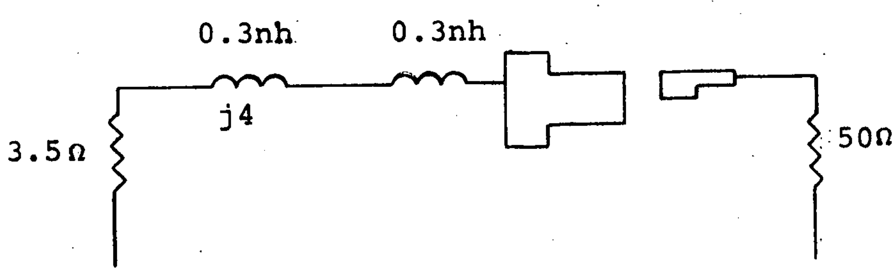
OUTPUT NETWORK




```
STOP

PROGRAM STOP AT 480

USED    10.16 UNITS
FYE
0010.51  CRU    0000.40   TCH     0010.00   KC
```

Figure 2-5. Computer Data, Output Circuit Bandwidth, S-Band MPA (Sheet 1 of 2)

```
ENTER ZG,ZL,F1,F2,NF?3.5,50.,2.0,2.5,25
```

F(GHZ)	VSWR	IL(DB)	PHASE	R IN	X IN	R OUT	X OUT
2.000	1.467	0.1592	96.53	3.322	-1.303	51.78	19.54
2.020	1.397	0.1214	98.44	3.283	-1.117	51.72	16.99
2.040	1.331	.8924E-01	100.4	3.246	-0.9336	51.33	14.48
2.060	1.271	.6294E-01	102.3	3.210	-0.7513	50.64	12.08
2.080	1.217	.4263E-01	104.3	3.174	-0.5704	49.67	9.815
2.100	1.174	.2846E-01	106.3	3.140	-0.3909	48.46	7.736
2.120	1.145	.2054E-01	108.2	3.107	-0.2128	47.05	5.867
2.140	1.139	.1895E-01	110.2	3.075	.3606E-01	45.47	4.226
2.160	1.157	.2373E-01	112.2	3.045	0.1394	43.78	2.822
2.180	1.194	.3490E-01	114.2	3.015	0.3136	42.02	1.652
2.200	1.244	.5244E-01	116.2	2.986	0.4865	40.21	0.7117
2.220	1.303	.7631E-01	118.1	2.958	0.6582	38.39	.1297E-01
2.240	1.367	0.1064	120.1	2.930	0.8287	36.58	-0.5374
2.260	1.437	0.1426	122.1	2.904	0.9981	34.81	-0.8794
2.280	1.512	0.1849	124.0	2.879	1.166	33.10	-1.058
2.300	1.591	0.2329	125.9	2.854	1.333	31.45	-1.091
2.320	1.675	0.2866	127.9	2.830	1.499	29.86	-0.9977
2.340	1.764	0.3457	129.8	2.807	1.664	28.36	-0.7941
2.360	1.857	0.4099	131.6	2.785	1.828	26.93	-0.4960
2.380	1.954	0.4792	133.5	2.764	1.991	25.59	-0.1172
2.400	2.056	0.5531	135.3	2.743	2.153	24.32	0.3297
2.420	2.163	0.6314	137.1	2.723	2.314	23.13	0.8339
2.440	2.274	0.7139	138.9	2.703	2.474	22.01	1.386
2.460	2.390	0.8002	140.7	2.685	2.633	20.96	1.977
2.480	2.511	0.8901	142.4	2.667	2.791	19.98	2.601
2.500	2.636	0.9833	144.1	2.649	2.948	19.06	3.251

```
COMMAND ?
```


Figure 2-5. Computer Data, Output Circuit Bandwidth, S-Band MPA (Sheet 2 of 2)

2.3 Interstage Circuit

The purpose of this circuit is to transform the complex input impedance of the MSC 3005 to the conjugate of the MSC 3001 complex output impedance. This circuit proved to be the most difficult to design, since direct circuit measurements could not be made with standard test equipment operating on a 50-ohm basis. Indirect measurements, such as evaluating a part of the circuit at a time, were necessary. A dummy transistor simulating the MSC 3001 output impedance was constructed to allow the interstage network to be characterized.

A direct impedance transformation in the interstage network is necessary to achieve the required bandwidth. The design of this network in the form of two coupled circuits with an image impedance of 50 ohms to facilitate measurement of the output and input devices independently is not feasible. A bandwidth reduction would occur in this type of network which would not be consistent with the required 100 MHz bandwidth of the amplifier.

The final design form of the interstage network, shown in figure 2-6, has the advantage of very small size without any compromise in the electrical performance capability. A two-degree-of-freedom network is used, with a variable shunt element at the input of the MSC-3005 and a variable series element at the MSC-3001 collector. This network provides for the application of the B+ to the MSC-3001 with shunt feed and allows the use of a biasing resistor in another shunt feed to the MSC-3005 emitter.

The magnitude of the shunt reactance at the collector of the first stage is modified with the shunt impedance looking into the collector

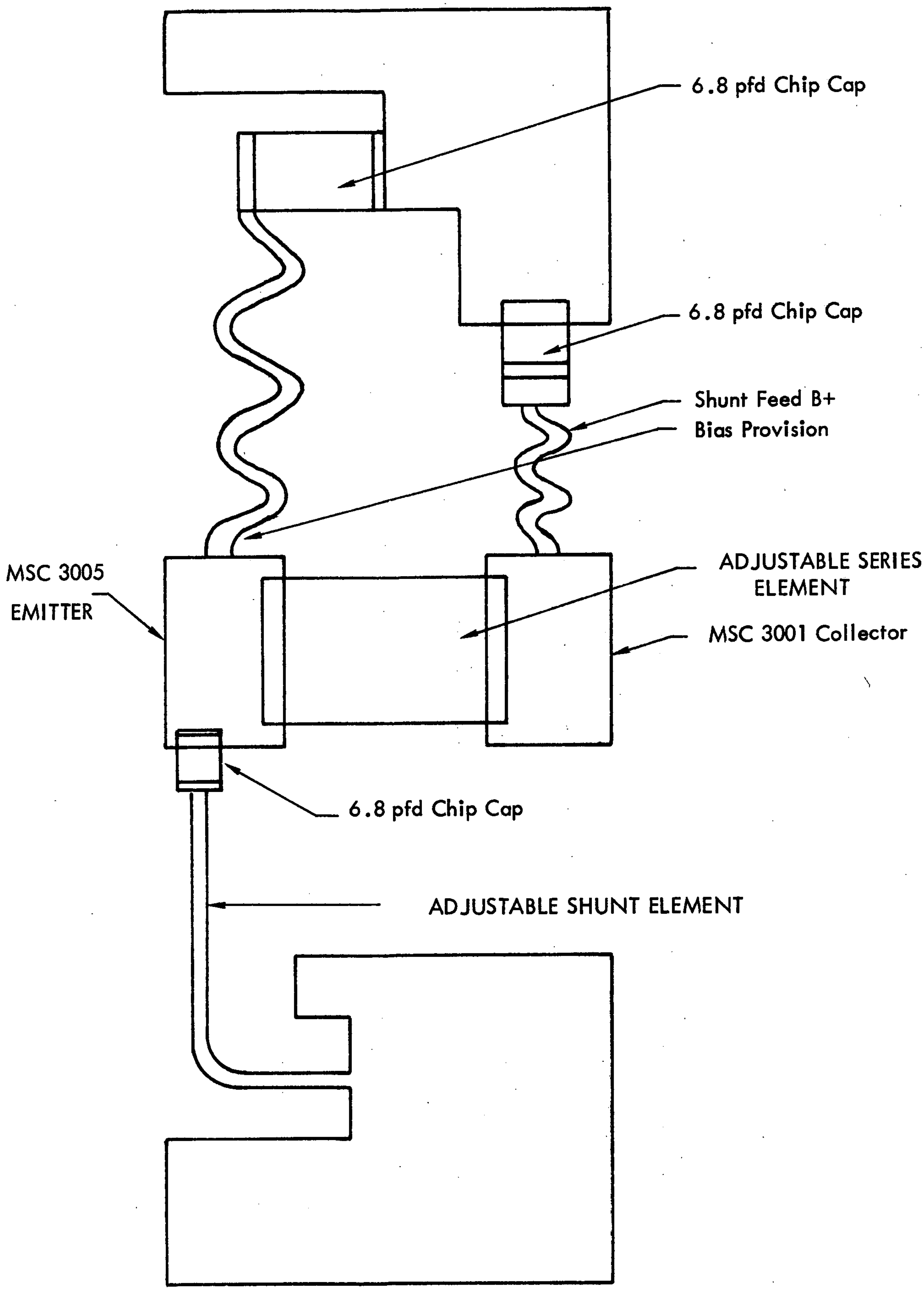


Figure 2-6. Interstage Network, S-Band MPA

feed circuit, and thereby establishes the unique driving point impedance locus desired as an input to the interstage matching network.

2.4 Input Circuit

The purpose of this circuit is to match the MSC 3001 input impedance to 50 ohms. Since the magnitudes of the impedances involved are only slightly greater than 2 to 1, adequate bandwidth can be achieved with a relatively simple network. However, the circuit must be capable of adjustment, since the input VSWR must be held to a value of 1.4 to 1 or less across the band of 2.2 to 2.3 GHz.

The final circuit configuration of the input matching network for the amplifier is shown in figure 2-7.

A three-element network is used to attain the required matching. A two-step inverter is placed in series with the MSC-3001 emitter, followed with a variable element shunt transmission line. The shunt line length is adjusted to obtain the desired value of the reflection coefficient at the input port to the amplifier.

The desired operating point in the circuit is obtained with a shunt feed to the emitter on the substrate. A ferrite type of choke is used in the feed to control the Rp placed in the emitter at the out-of-band frequencies.

Until the MSC 3001 or MSC 3005 is driven to the point where no further power output is obtained with increased drive, the input impedance varies widely with increasing drive (with its accompanying increase in collector current). Increasing the drive beyone this point of power output saturation drives the DC current up and increases the power the device must dissipate. Ideally, therefore, it is desirable to operate both the MSC 3005

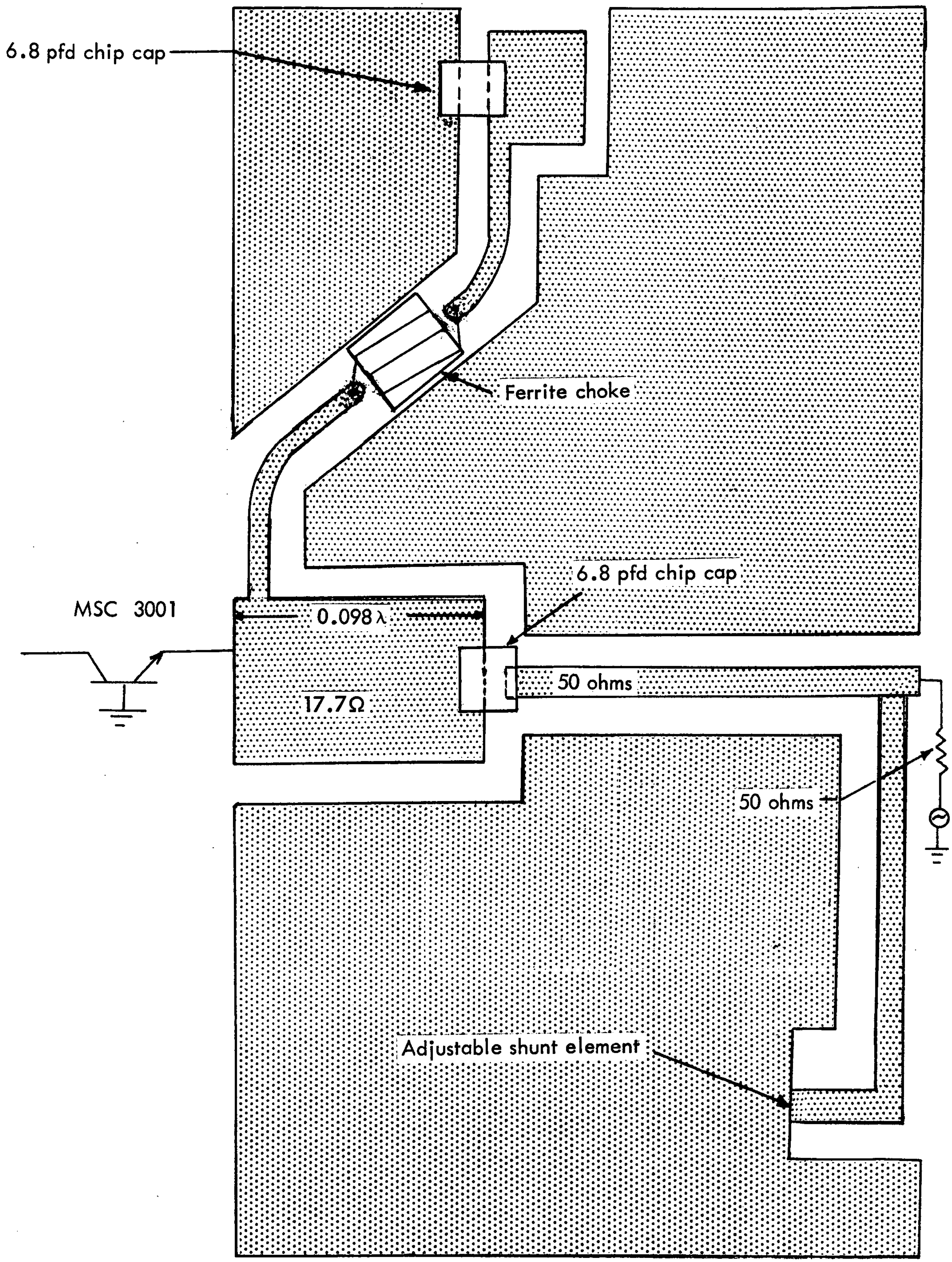


Figure 2-7. Input Matching Network, S-Band MPA

and the MSC 3001 at the drive level at which both are just into saturation. This assures maximum collector efficiency in the MSC 3005 stage and minimizes the input VSWR to the MSC 3001 stage. In order to accomplish this, the devices were selected on a basis of device saturated gain. If the spread of transistor gain was too great to allow both transistors to be operated optimally in saturation, the MSC 3001 was operated at a drive level just sufficient to drive the MSC 3005 into saturation and the resulting MSC 3001 input mismatch was corrected.

3.0 ASSEMBLY AND ALIGNMENT

Reference to the assembly drawing (RAD 417775G-2) will disclose that the chassis assembly is completed with the input, interstage, and output substrates soldered directly onto the chassis. This is the final step in the integrated procedure of assembly and alignment. All connections are made except those to the transistors.

The transistors are then bolted into position with the MSC 3001 device physically located as near to the input substrate as possible, for minimum emitter lead length. The MSC 3005 device is located as near to the output substrate as possible, for minimum collector lead length. All connections are then made to the device collector and emitter leads utilizing a silver base epoxy without hardener.

A general measure of performance is obtained with this test configuration as follows:

a) The output tuning is achieved by adjusting the collector lead inductance. This is done utilizing a narrow piece of copper foil overlaying the collector lead. If the output circuit tunes high, the MSC 3005 device is moved away from the output substrate, and the test is repeated.

b) Interstage tuning is achieved by adjusting the stub length at the MSC 3005 input. The stub length is varied by pressing a shorting bar of copper foil across the stub at the desired location. At this point no tuning is required at the input of the MSC 3001 device.

In general, power output increases about 20% to 30% when final solder connections are made. Most critical of these is the soldering of the transistor base to the chassis.

If the results of this preliminary test are favorable (i.e., both the interstage and output stages can be tuned), the device is then soldered into position utilizing reflow solder techniques.

Once the devices are properly soldered into position, the output and interstage tuning is adjusted with copper foil, as previously described. When optimum tuning is established, the foil is permanently soldered into position. Final adjustments are made by cutting away small increments of the foil after it is soldered into position.

The following considerations apply throughout the assembly and alignment:

a) A noncorrosive, nonactivated flux is utilized when making solder connections, especially those which will react with the chassis material (in this case, aluminum).

b) All surfaces are kept clean during the preliminary testing, when there are no solder connections to the devices. (Fingerprints and other foreign material between the base of the device and the chassis will drastically reduce power output).

c) When the MSC 3005 device is located away from the output substrate for purposes of tuning, power output is lowered considerably. If at all possible, the output is tuned with the MSC 3005 contacting the chassis at the output substrate.

d) The current drain of each stage is monitored separately to avoid exceeding the power rating of the devices.

4.0 THERMAL ANALYSIS

The power amplifier thermal analysis was based on the following assumptions:

1. Continuous operation at 70°C ambient.
2. A 1.75 x 3.5 inch interface surface between the mounting surface (heat sink) and the unit. (Silicone grease is provided at this interface.)
3. The total power dissipation is transferred to the mounting surface by conduction.
4. Power-dissipating transistors are soldered to the housing. The temperature gradient between the transistor flanges and the housing is negligible.
5. The housing is isothermal.

Calculations were run for measured power dissipation at four input frequencies and for the preliminary estimated power. This power distribution is tabulated below (also see table 4-1).

Input Frequency (GHz)	Power (watts) 3001	3005	Total	
---	1.5	15.0	16.5	(Prelim. Est.)
2.175	2.94	10.26	13.2	
2.150	1.96	9.64	11.6	
2.100	1.68	11.32	13.0	
2.075	1.96	12.34	14.3	

The junction-to-flange resistances of the MSC 3001 and 3005 transistors are 35°C/watt and 8.5°C/watt, respectively.

Table 4-1. Power Profile, MSC 3001 - MSC 3005 Amplifier

Freq. (GHz)	MSC 3001 Stage			MSC 3005 Stage			Coll. Eff. MSC 3005 Stage (%)	Total DC Power Input (watts)	Total Device Efficiency (%)
	DC Pwr Input (watts)	RF Pwr Output (watts)	DC Pwr Diss. (watts)	DC Pwr Input (watts)	RF Pwr Output (watts)	Total Pwr Diss * (watts)			
2.175	4.2	1.26	2.94	15.7	6.7	10.26	42.5	19.9	33.5
2.150	2.8	.84	1.96	15.7	6.9	9.64	44.0	18.5	37.0
2.100	2.4	.72	1.68	17.4	6.8	11.32	39.0	19.8	33.0
2.075	2.8	.84	1.96	18.3	6.8	12.34	38.0	21.1	32.0

* Includes RF Power Output of MSC 3001 Stage

Note: MSC 3001 efficiency assumed to be 30%

Calculations

Temperature gradient between the heat sink and housing:

W_T = total unit power dissipation, watts

Contact area = $1.75 \times 3.5 = 6.12\ in^2$ $(0.0425\ ft^2)$

$$T = \frac{3.413\ W}{hA} = \frac{3.413\ W}{100 \times .0425} = 0.446\ W\ ^\circ C$$

3001 Transistor junction temperature:

$$T = 70 + 0.446\ W_T + 35\ W_{3001}\ ^\circ C$$

3005 Transistor junction temperature:

$$T = 70 + 0.466\ W_T + 8.5\ W_{3005}\ ^\circ C$$

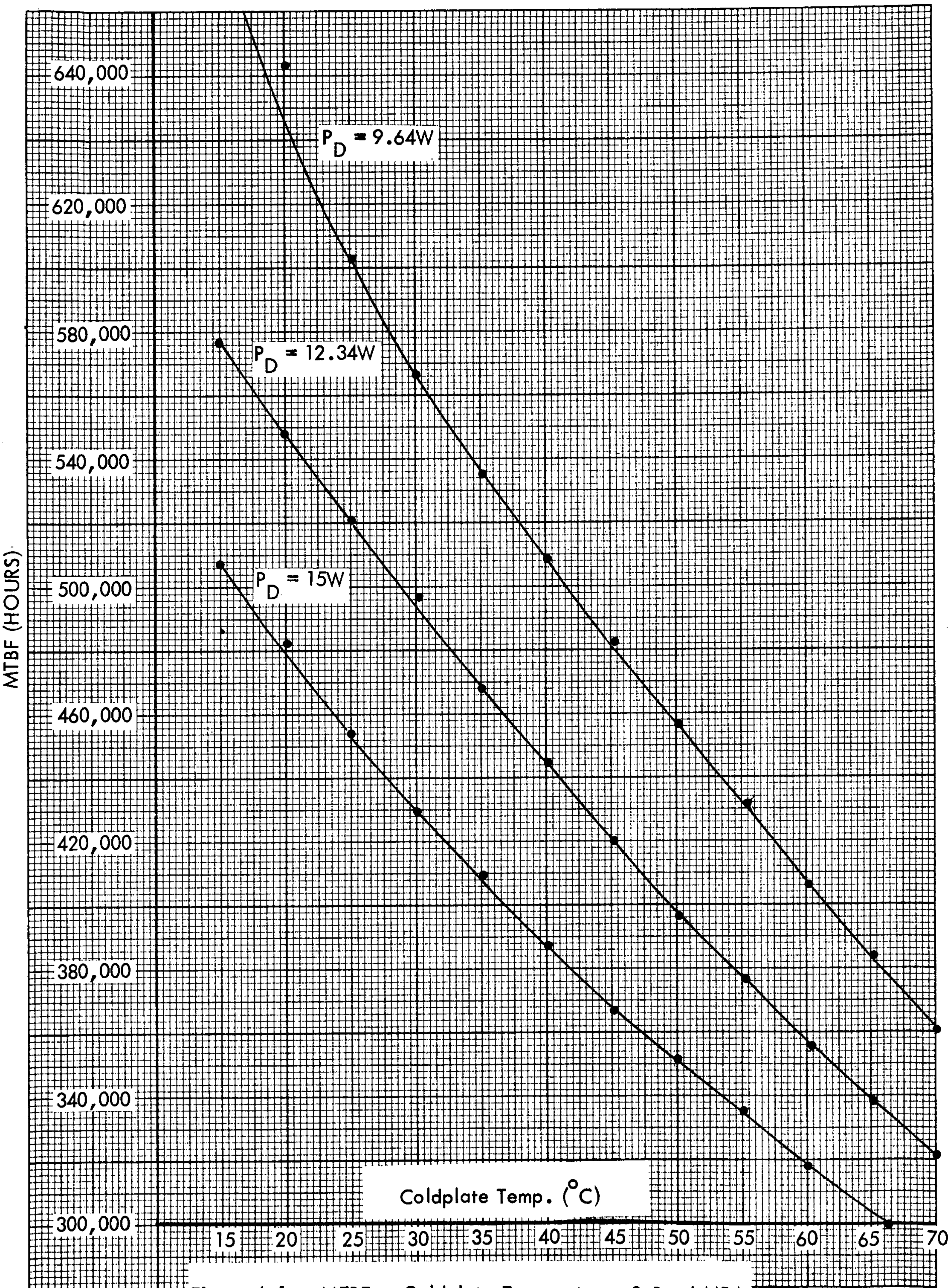
Results

The computed junction temperatures for the estimated and measured power distributions are tabulated below:

Input Frequency (GHz)	Junction Temp. (°C) 3001	3005	
----	130	205	(Prelim. Est.)
2.175	179	163	
2.150	144	157	
2.100	135	172	
2.075	145	181	

All the junction temperatures based on measured power distributions are well below the maximum operating temperature of 200°C specified by the vendor.

Figure 4-1 and table 4-2 depict MTBF vs coldplate temperature for three different power distributions, while TJ vs coldplate temperature will be found in table 4-3.



EUGENE DIETZGEN CO.
MADE IN U. S. A.

NO. 340R-20 DIETZGEN GRAPH PAPER
20 X 20 PER INCH

Figure 4-1. MTBF vs Coldplate Temperature, S-Band MPA

Table 4-2.

S-BAND AMPLIFIER
MTBF VS COLD PLATE TEMPERATURE

TC	PD = 9.64 W		PD = 12.34 W		PD = 15.0 W	
	FR	MTBF	FR	MTBF	FR	MTBF
15	1.474	678426	1.744	573394	1.984	504032
20	1.565	638977	1.835	544959	2.085	479616
25	1.670	598802	1.930	518134	2.210	452488
30	1.775	563380	2.025	493827	2.335	428265
35	1.881	531632	2.141	467071	2.451	407996
40	1.978	505561	2.258	442869	2.588	386398
45	2.087	479156	2.387	418935	2.727	366703
50	2.198	454959	2.528	395569	2.848	351123
55	2.324	430292	2.654	376789	2.984	335120
60	2.470	404858	2.810	355871	3.150	317460
65	2.612	382848	2.952	338753	3.312	301932
70	2.779	359841	3.119	320615		

TC IN DEGREES CENTIGRADE

FR IN FAILURES PER MILLION HOURS

MTBF IN HOURS

Table 4-3.

S-BAND AMPLIFIER

TJ VS COLD PLATE TEMPERATURE

TC	3005 XSTR PD = 9.64 W	3005 XSTR PD = 12.34 W	3005 XSTR PD = 15.0 W	3001 XSTR PD = 1.5 W
15	104	128	150	75
20	109	133	155	80
25	114	138	160	85
30	119	143	165	90
35	124	148	170	95
40	129	153	175	100
45	134	158	180	105
50	139	163	185	110
55	144	168	190	115
60	149	173	195	120
65	154	178	200	125
70	159	183	205*	130

ALL VALUES IN DEGREES CENTIGRADE

* DENOTES DEVICE EXCEEDS MANUFACTURERS RATED TJ